Title	***Reference Design Report for a 15 W Wide Range Input, Dual Output, Non-Isolated Flyback Converter Using InnoSwitch™3-EP INN3673C-H601***
Specification	85 VAC – 277 VAC Input; 5 V / 1.2 A and 12 V / 0.75 A Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	RDR-752
Date	November 17, 2021
Revision	1.2

Summary and Features

- High standby mode efficiency design to deliver up to 49 mA from 5 V with 0.3 W input power at 230 VAC
- Less than 50 mW no-load consumption across input range
- Using highly integrated solution with 725 V rated power MOSFET
- >83% average efficiency at 115 VAC and 230 VAC
- >6 dB conducted EMI margin
- Over-temperature protection with hysteretic recovery
- Auto-restart output short-circuit and open-loop protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a non-isolated flyback converter designed to provide dual output of 5 V at 1.2 A and 12 V at 0.75 A from a wide input range of 85 VAC to 277 VAC. This power supply utilizes the INN3673C-H601 from the InnoSwitch3-EP family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

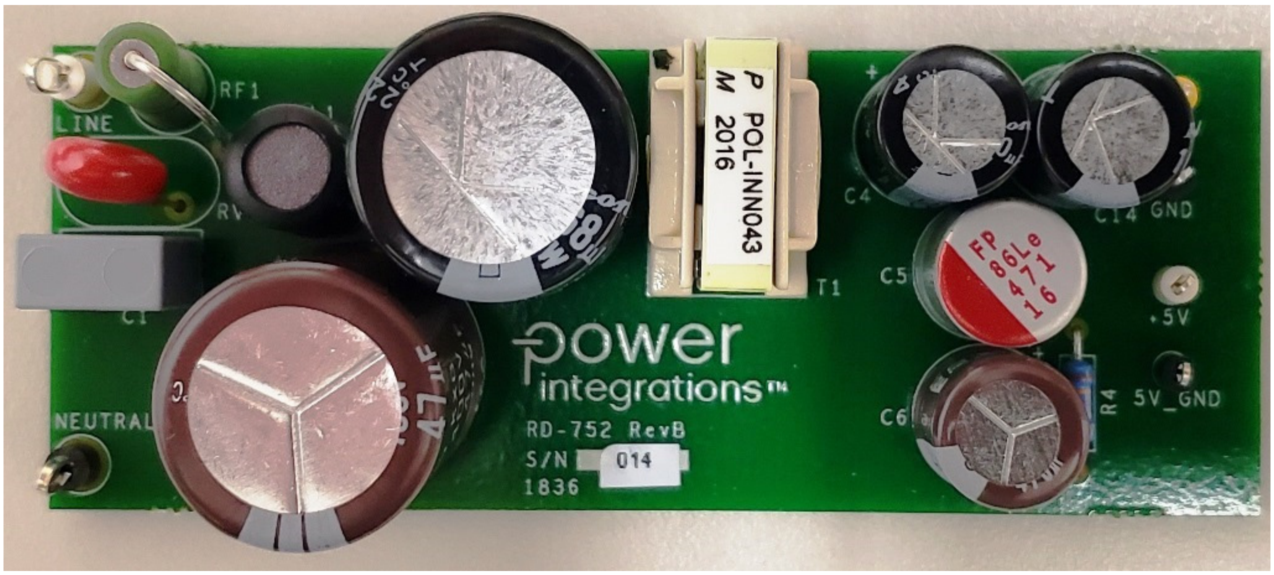


Figure 1 – Populated Circuit Board Photograph, Top.

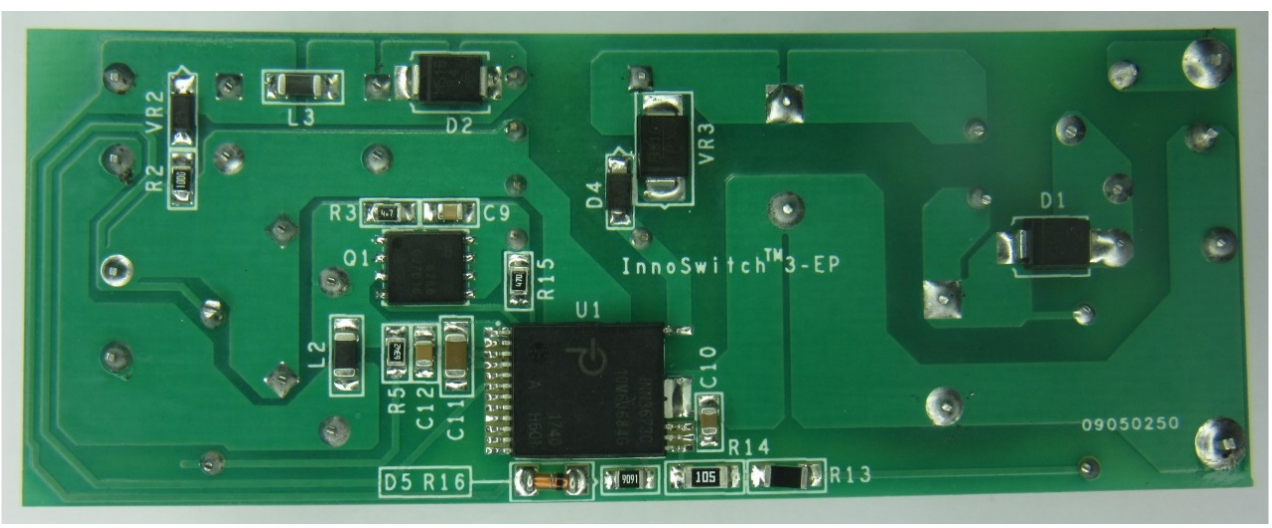


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	277	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				45	mW	230 VAC Input.
Output						
Output Voltage 1	V_{OUT1}		5		V	±5% PCB Connector Side.
Output Current 1	I_{OUT1}		1.2		A	
Output Ripple Voltage 1	$V_{RIPPLE1}$			150	mVpp	Measured at the PCB Connector.
Output Voltage 2	V_{OUT2}		12		V	±10% PCB Connector Side.
Output Current 2	I_{OUT2}	0.02	0.75		A	
Output Ripple Voltage 2	$V_{RIPPLE2}$			200	mVpp	Measured at the PCB Connector.
Continuous Output Power	P_{OUT}			15	W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	80			%	115 and 230 VAC Input.
Environmental						
Conducted EMI	CISPR22B / EN55022B Load floating					Resistive Load, 6 dB Margin.
Safety	IEC950 / UL1950 Class II					Designed to Meet.
Differential Line Surge		1			kV	230 VAC Input.
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic Diagram

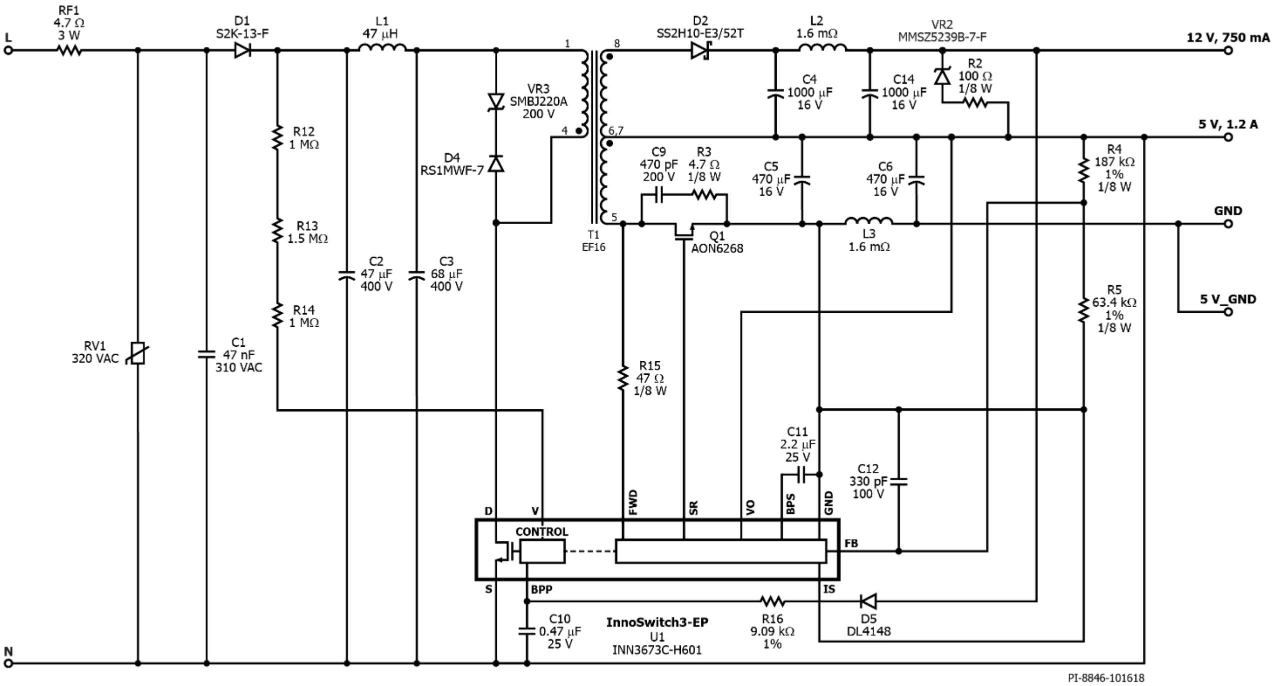


Figure 3 – Schematic Diagram.

4 Circuit Description

The InnoSwitch3-EP family of devices integrates a 725 V rated power MOSFET switch along with both primary-side and secondary-side controllers in a single device. The INN3673C-H601 IC is used in the design of the 15 W non-isolated flyback with dual output of 5 V and 12 V delivering 1.2 A and 0.75 A, respectively.

4.1 *Input Filter and Rectifier*

Resistor RF1 is fusible, flameproof, wire-wound type and functions as a fuse and inrush current limiter which provide protection against catastrophic failure of components of the primary-side and limits the inrush current when the power supply is connected to the AC input supply due to low impedance of the input capacitors, C2 and C3, during start-up operation.

Varistor RV1 clamps the AC input voltage across the power supply against surge and voltage transients.

Input X capacitor C1 and pi filter combination of C2, L1, and C3 attenuate differential mode EMI.

Diode D1 rectifies the AC line voltage to half wave rectified DC and filtered by the input bulk storage capacitors C2 and C3.

4.2 *InnoSwitch3-EP Primary-Side*

The rectified and filtered input voltage is applied to one end of the primary winding of flyback transformer T1. The other side of T1 primary winding is driven by the integrated power MOSFET of IC U1 via the DRAIN (D) pin.

A Zener clamp composed of VR3 and D4 is connected across the primary winding of transformer T1. The primary clamp limits the peak drain voltage of the internal power MOSFET switch of U1 due to the effects of the transformer leakage reactance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C10, when AC is first applied. However, connecting an external current source to the BPP pin significantly decreases no-load input power and improves overall efficiency. This external current source for the BPP pin is tapped from the 12 V output controlled by resistor R16 via diode D5.

Resistors R12, R13, and R14 provide line voltage sensing and provide a current to the V pin of U1 which is proportional to the DC voltage across C3. At approximately 100 VDC, the current through these resistors exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 410 VDC, the current through these resistors exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 *InnoSwitch3-EP Secondary-Side*

The secondary-side of the InnoSwitch3-EP provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Transformer T1 has two secondary windings in an AC-stacked configuration for the dual output of 5 V and 12 V. Each secondary switching voltage is rectified by a synchronous rectifier Q1 and Schottky diode D3 for the 5 V and 12 V output, respectively. The secondary rectified voltages are filtered by low ESR type capacitors, C4 and C5. A post-filter using L2 and C6 for the 5 V output and L3 and C14 for the 12 V output are added to further improve peak-to-peak voltage ripple at the output connector. The RC snubber network, R3 and C9, limits the high frequency ringing across the SR FET Q1.

The gate of Q1 is turned on based on the winding voltage sensed via R15 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensures that it is never turned on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is the output of the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, feeds into the VO pin, and charges the decoupling capacitor C11 via an internal regulator. The power supply enters auto-restart when the sensed output voltage is lower than 3 V.

IC U1 has an internal voltage and current feedback control circuitry. The 5 V output is sensed through the resistor dividers R4 and R5 to keep the output regulation within limits by maintaining 1.265 V across the FB pin. In addition, the decoupling capacitor C12 provides better transient response during output load changes.

The 12 V output is quasi-regulated with the tight coupling between 5 V and 12 V secondary windings. A simple circuit using Zener diode VR2 and resistor R2 clamps the 12 V output up to ~14 V when then the 5 V output is fully loaded.

4.4 *Design Key Points*

The design targets to improve the standby mode efficiency by maximizing the available output power in a given input power required. Standby mode efficiency was optimized with the transformer design and selection of active devices, primary clamp, filter components and bias resistors values.

4.4.1 *Transformer Design*

- Z-winding technique on the primary-side of transformer resulting to low interwinding capacitance and a direct influence on the CV^2f loss

- Lower reflected output voltage (VOR) setting yields to lower secondary peak, rms, and average currents which affects the losses of the output rectifiers
- Proper selection of core material

4.4.2 *Primary Clamp*

- Proper tuning of primary clamp required to meet derated primary MOSFET VDS at maximum input voltage and sufficient margin on EMI performance

4.4.3 *Primary Bias*

- Since the bias voltage for the BPP pin is tapped from the 12 V output, BPP pin bias current appears as a preload to the 12 V rail
- Optimize BPP bias current within 230 μA to 250 μA during standby mode

4.4.4 *Secondary Rectification*

- Using MOSFET for synchronous rectification significantly decreases loss due to lower equivalent $I^2R_{DS(ON)}$
- Otherwise for other output voltage settings, use Schottky rectifiers due to its lower forward voltage and faster reverse recovery time specification compared to fast recovery type of diode.
- Selecting higher current rating of synchronous rectifiers / Schottky diodes of at least three times the actual DC current through the output rectifiers results to lower bulk resistance and, in turn, allowing the device to operate at lower current density. Bigger packages also contribute to better thermal management because of lower thermal resistance

4.4.5 *Filter Components*

- Lower ESR causes capacitor to dissipate less power when subjected to secondary ripple current
- Lower DC resistance directly decreases the dissipation across the ferrite bead

5 PCB Layout

PCB copper thickness is 2 oz. (2.8 mils / 70 μm) unless otherwise stated.

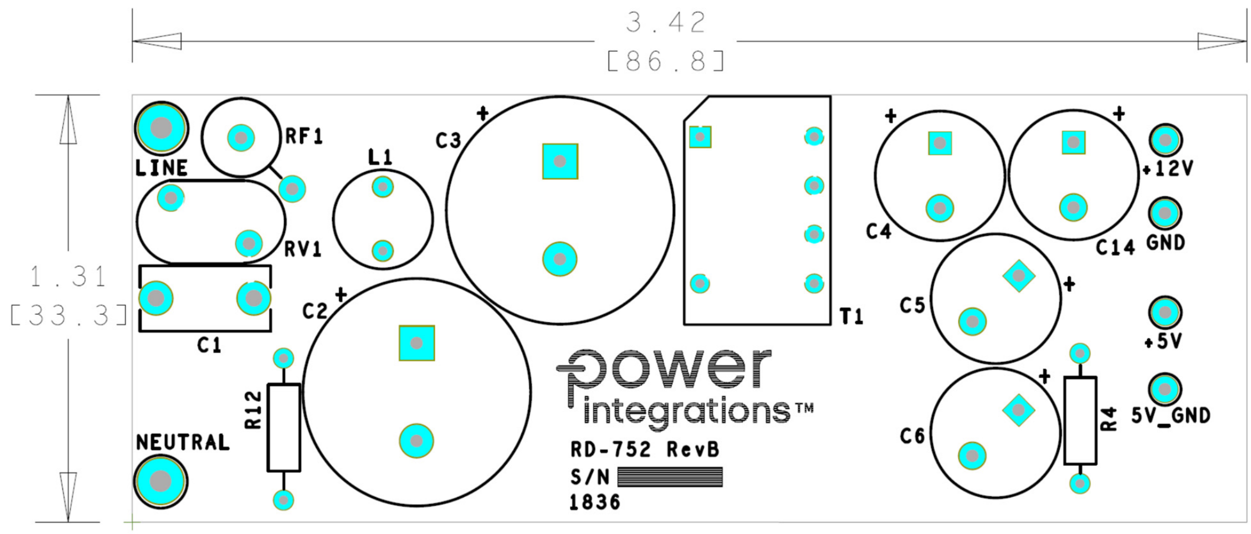


Figure 4 – Printed Circuit Layout, Top.

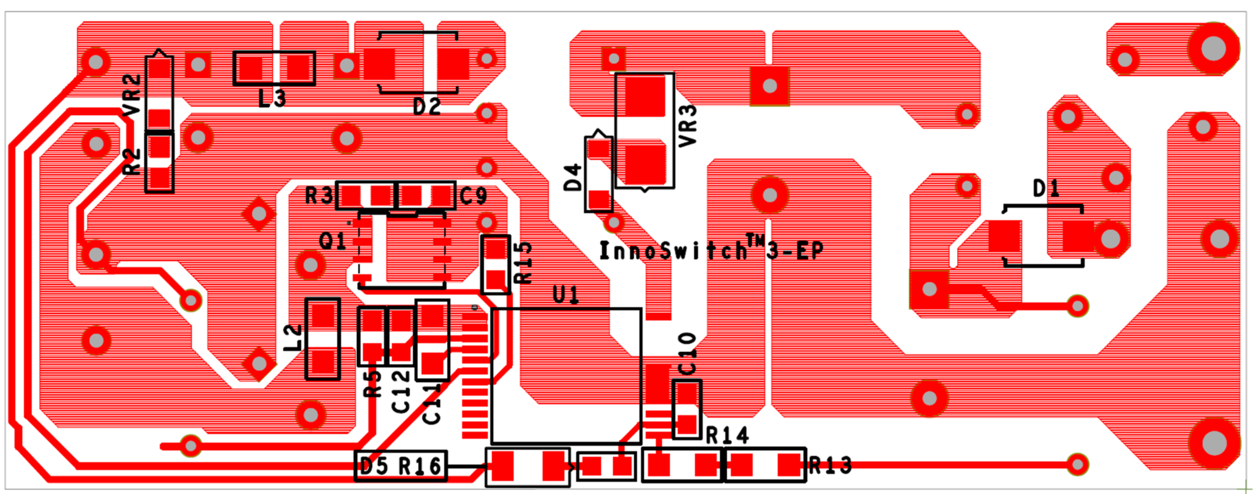


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C1	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
2	1	C2	47 μF, ±20%,400 V, Electrolytic, Low ESR, (18 x 20)	EKXG401ELL470MM20S	Nippon Chemi-Con
3	1	C3	68 μF, ±20%,400 V, Electrolytic, Low ESR, (18 x 22)	400BXW68MEFC18X20	Rubycon
4	2	C4, C14	1000 μF, 16 V, Electrolytic, Gen. Purpose, (10 x 17.5)	16ZLH1000MEFC10X16	Rubycon
5	1	C5	470 μF, 16 V, Electrolytic, Very Low ESR, 10 mΩ, (10 x 12.5)	RNU1C471MDN1PH	Nichicon
6	1	C6	470 μF, 16 V, Electrolytic, Very Low ESR, 53 mΩ, (10 x 12.5)	EKZE160ELL471MJC5S	Nippon Chemi-Con
7	1	C9	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
8	1	C10	0.47 μF, ±10%, 25 V, Ceramic Capacitor, X7R	CGA4J2X7R1E474K125AA	TDK
9	1	C11	2.2 μF, ±10%, 25 V, Ceramic, X7R, 1206	12063C225K4Z2A	AVX Murata
10	1	C12	330 pF, ±10%, 50 V, X7R, Ceramic, -55°C ~ 125°C, MLCC 0805	CL21B331KBANNNC	Samsung
12	1	D1	800 V, 1.5 A, Glass Passivated, DO-214AA	S2K-13-F	Diodes, Inc.
13	1	D2	100 V, 2 A, Schottky, SMD, SMB	SS2H10-E3/52T	Vishay
14	1	D4	1000 V, 1 A, Gen. Purpose, Fast Recovery ≤500 ns, trr = 500 ns, SOD123F	RS1MWF-7	Diodes, Inc.
15	1	D5	100 V, 0.200 A, Gen. Purpose, LL34, DO-213AC, MINI-MELF, SOD-80	FDLL4148	ON Semi
16	1	L1	47 μH, ±10%, Unshielded, Wirewound Inductor, 1.56 A, 140 mΩ Max, Radial Inductor Assembly	RLB0914-470KL PM-R30047	Bourns Premier Magnetics
17	2	L2, L3	FERRITE BEAD, 50 Ω, 1206, 1LN, 1.6 mΩ	BLM31SN500SN1L	Murata
19	1	Q1	MOSFET, N-CH, 60 V, 44 A (Tc), 56 W (Tc), SMT, 8DFN, 8-DFN (5x6)	AON6268	Alpha & Omega Semi
20	1	R2	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
21	1	R3	RES, 4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
22	1	R4	RES, 187 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-187K	Yageo
23	1	R5	RES, 63.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6342V	Panasonic
24	1	R12	RES, 1 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-1M0	Yageo
25	1	R13	RES, 1.5 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ155 V	Panasonic
26	1	R14	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105 V	Panasonic
27	1	R15	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
28	1	R16	RES, 9.09 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9091V	Panasonic
29	1	RF1	RES, 4.7 Ω, ±5%, 3 W, TH, Axial, Fusible, Safety, Wirewound	FW30A4R70JA	Bourns
30	1	RV1	320 VAC, 26 J, 7 mm, RADIAL	V320LA7P	Littlefuse
31	1	T1	Bobbin, Vertical, EF16, 8 Pins, mates with core 99-00063-00 Transformer	B66308W1108T001 POL-INN043	TDK Premier Magnetics
32	1	U1	InnoSwitch3-EP Integrated Circuit, INSOP24D	INN3673C-H601	Power Integrations
33	1	VR2	DIODE ZENER 9.1 V 500 mW SOD123	MMSZ5239B-7-F	Diodes, Inc.
34	1	VR3	TVS DIODE, 220 VWM, 356 VC, SMB	SMBJ220A	Bourns

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	LINE	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	1	NEUTRAL	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	+12 V	Test Point, YEL, Miniature THRU-HOLE MOUNT	5004	Keystone
4	1	+5 V	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone

5	2	GND, 5 V_GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

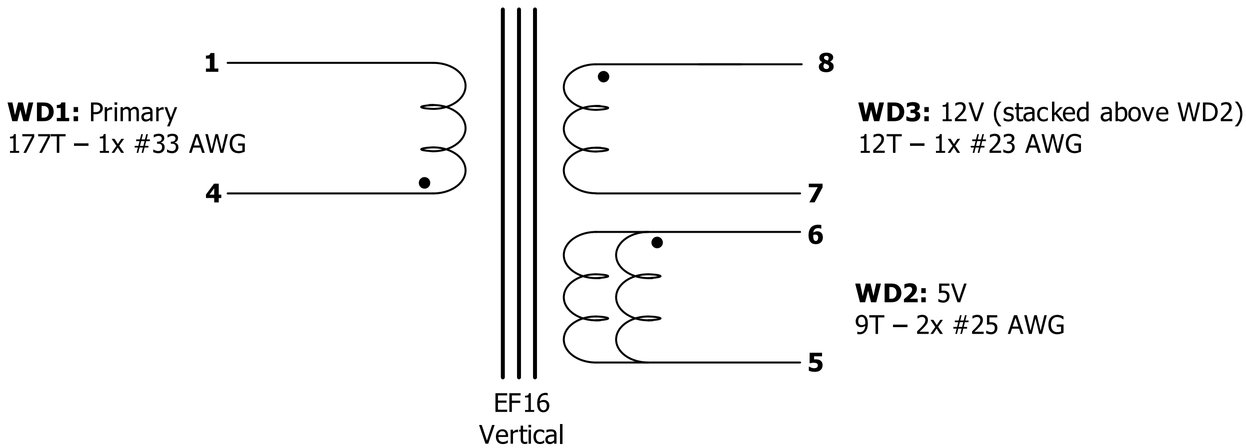


Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specification*

Electrical Strength	1 sec, 60 Hz, from pins 5-8 to pins 1,4	3000 VAC
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 1 V_{RMS}.	2017 μH ±5%
Primary Leakage Inductance	Pins 1-4, with pins 5-8 shorted, measured at 100 kHz, 0.4 V_{RMS}.	75 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EF16, Ferrite Core N87 gapped for ALG of 72nH/T². Part Number: B66307G0000X187 EPCOS TDK.
[2]	Bobbin: EF16 Vertical.
[3]	Magnet Wire: #33 AWG, Double Coated.
[4]	Magnet Wire: #25 AWG, Double Coated.
[5]	Magnet Wire: #23 AWG, Double Coated.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 10 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 4.5 mm Wide.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

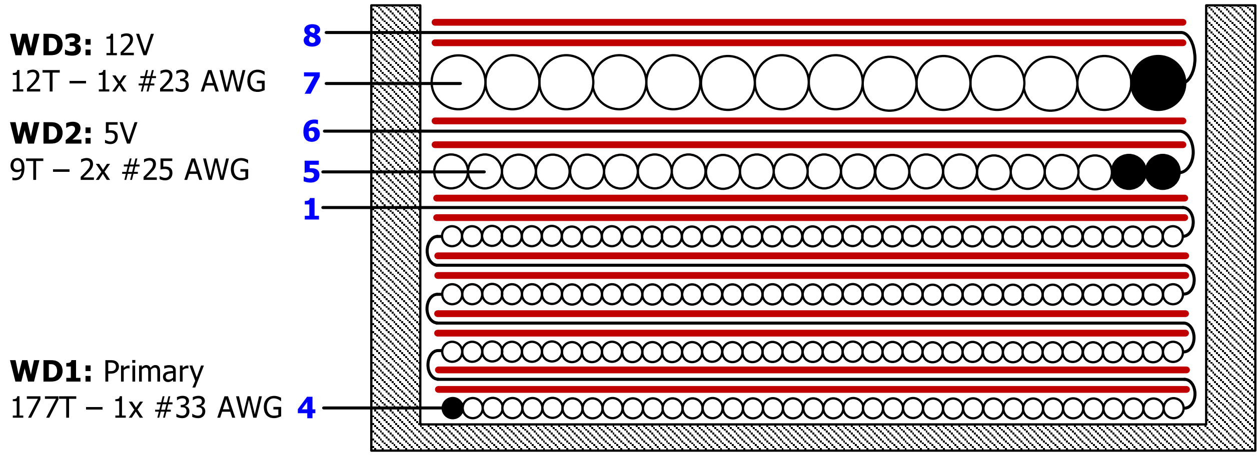
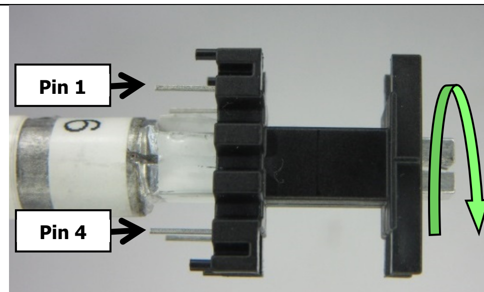
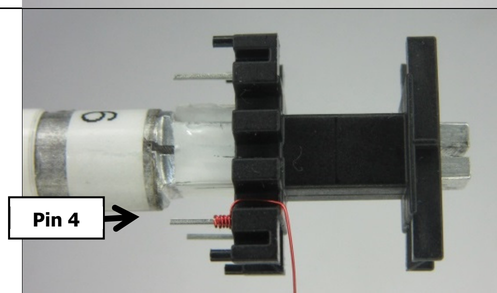
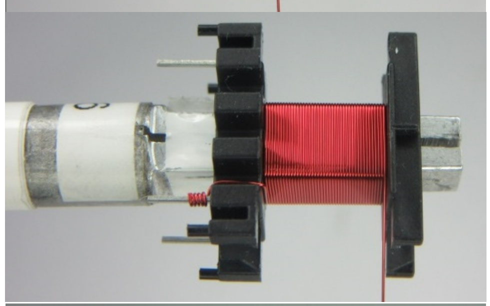
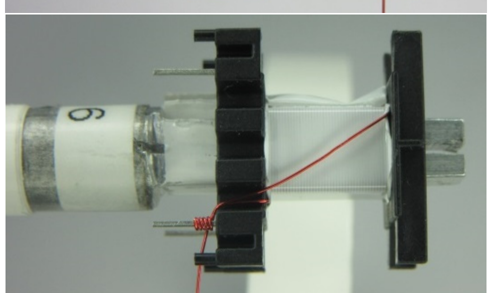
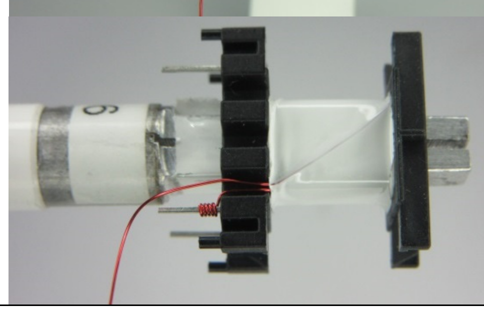


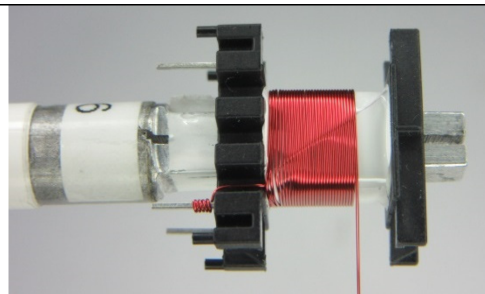
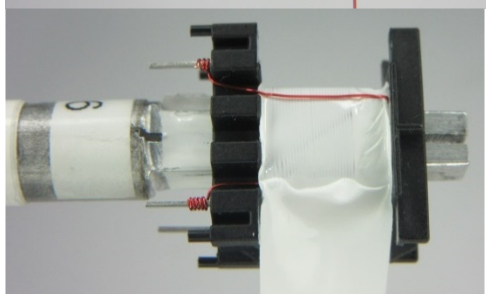
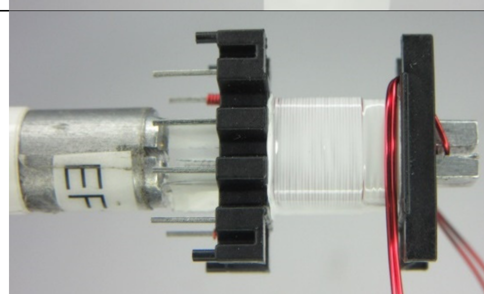
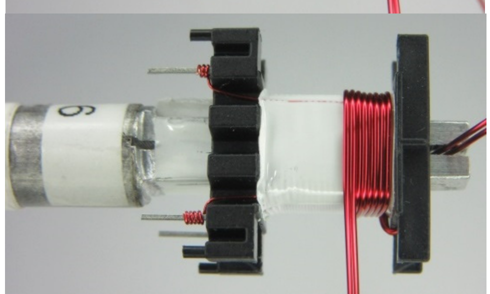
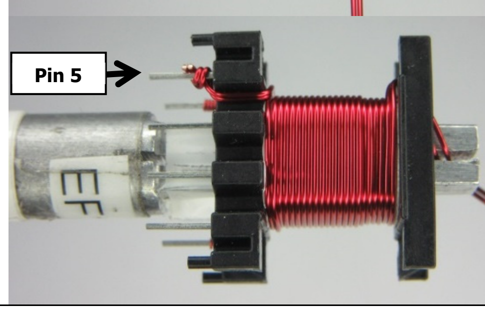
Figure 7 – Transformer Build Diagram.

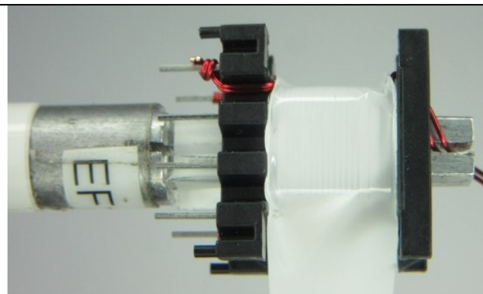
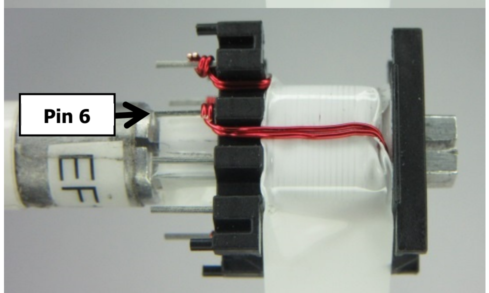
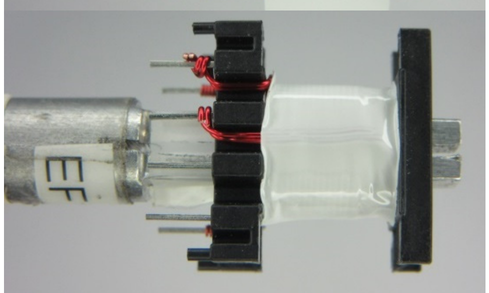
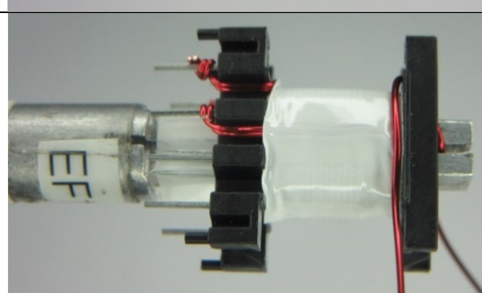
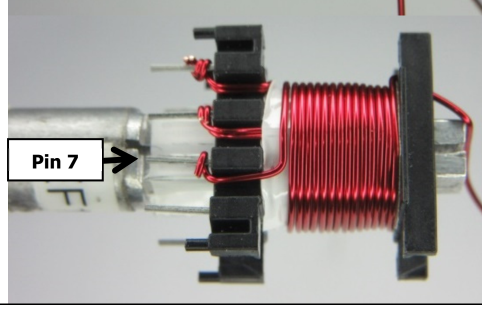
7.5 *Transformer Instructions*

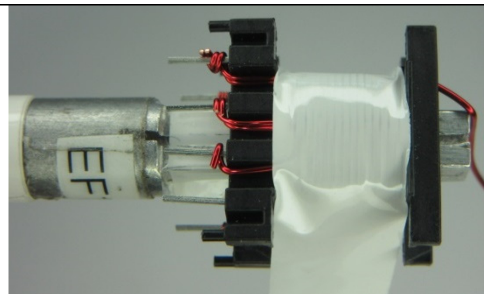
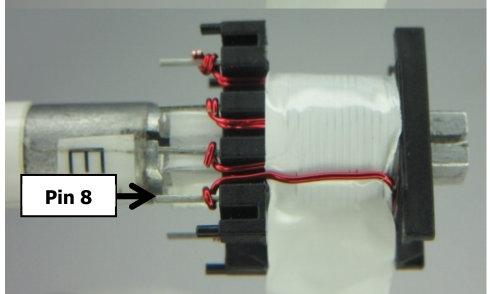
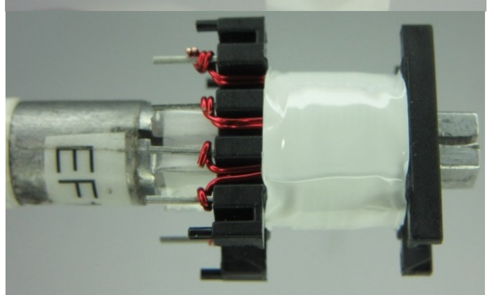
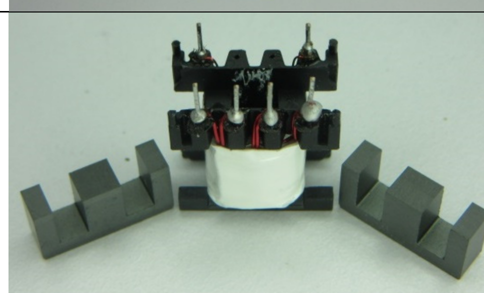
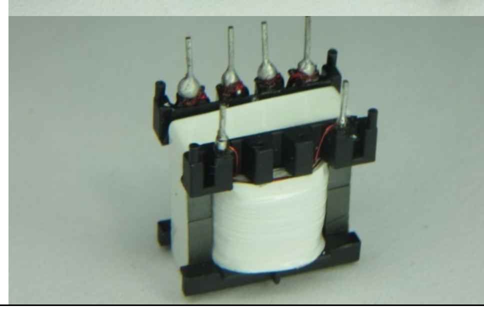
Winding Preparation	Remove unused pin 2 and pin 3. For the purpose of these instructions, bobbin is oriented on winder such that primary-side is on the left side with pin 4 at the bottom. Winding direction is clockwise direction.
WD1 Primary	Start at pin 4, wind 177 turns (x1 filar) of wire Item [3] in 4 layers using Z-winding configuration with tight tension (Layer 1 – 46T, Layer 2 – 45T, Layer 3 – 44T, Layer 4 – 42T).
Insulation	At the end of *each* layer, add 1 layer of tape Item [6]. Bring the wire back to the left. And add another one-half layer of tape Item [6]. Terminate at pin 1 after the fourth layer of winding.
WD2 5 V	Start winding at the right side of the bobbin with 9 turns (x2 filar) of wire Item [4]. Terminate winding at pin 5.
Insulation	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD2 to pin 6 and add another 1 layer of tape Item [6].
WD3 12 V	Start winding at the right side of the bobbin with 12 turns (x1 filar) of wire Item [5]. Terminate winding at pin 7.
Insulation	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD3 to pin 8 and add another 1 layer of tape Item [6].
Finish	Gap core halves for 2017 μH inductance. Wrap core halves with tape Item [7]. Coat with varnish Item [8].

7.6 *Winding Illustrations*

Winding Preparation		Remove unused pin 2 and pin 3. For the purpose of these instructions, bobbin is oriented on winder such that primary-side is on the left side with pin 4 at the bottom. Winding direction is clockwise direction.
WD1 Primary **and** **Insulation**		Start at pin 4, wind 177 turns (x1 filar) of wire Item [3] in 4 layers using Z-winding configuration with tight tension
		Layer 1 – 46T, Layer 2 – 45T, Layer 3 – 44T, Layer 4 – 42T.
		At the end of each layer, add 1 layer of tape Item [6]. Bring the wire back to the left.
		Add another one-half layer of tape Item [6].

WD1 **Primary** **and** **Insulation**	 	At the end of the 4th winding layer, add one turn of tape Item [6] and terminate wire at pin 1. Add another one-half layer of tape Item [6].
WD2 **5 V**	  	Start winding at the right side of the bobbin with 9 turns (x2 filar) of wire Item [4]. Terminate winding at pin 5.

Insulation	  	Add 1 layer of tape Item [6] for insulation. Terminate the floating start of WD2 to pin 6. Add another 1 layer of tape Item [6].
WD3 12 V	  	Start winding at the right side of the bobbin with 12 turns (x1 filar) of wire Item [5]. Terminate winding at pin 7.

Insulation		Add 1 layer of tape Item [6] for insulation.
		Terminate the floating start of WD3 to pin 8.
		Add another 1 layer of tape Item [6].
Finish		Gap core halves for 2017 μH inductance.
		Wrap core halves with tape Item [7]. Coat with Varnish Item [8].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-EP_Flyback_042018; Rev.1.2; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN			85	V	Minimum AC input voltage
4	VIN_MAX	277		277	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	47.0		47.0	uF	Input capacitor
8	VOUT	5.00		5.00	V	Output voltage at the board
9	PERCENT_CDC			0		Cable drop compensation required
10	IOUT	3.000		3.000	A	Output current
11	POUT		Info	15.00	W	The specified output power exceeds the device power capability: Verify thermal performance if no other warnings
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
15	**PRIMARY CONTROLLER SELECTION**					
16	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
17	DEVICE_GENERIC	INN36X3		INN36X3		Generic device code
18	DEVICE_CODE			INN3673C		Actual device code
19	POUT_MAX			12	W	Power capability of the device based on thermal performance
20	RDSON_100DEG			7.88	Ω	Primary MOSFET on time drain resistance at 100 degC
21	ILIMIT_MIN			0.511	A	Minimum current limit of the primary MOSFET
22	ILIMIT_TYP			0.550	A	Typical current limit of the primary MOSFET
23	ILIMIT_MAX			0.589	A	Maximum current limit of the primary MOSFET
24	VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
25	VDRAIN_ON_MOSFET			1.30	V	Primary MOSFET on time drain voltage
26	VDRAIN_OFF_MOSFET			560.3	V	Peak drain voltage on the primary MOSFET during turn-off
27	**WORST CASE ELECTRICAL PARAMETERS**					
28	FSWITCHING_MAX	75000		75000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
29	VOR	100.0		100.0	V	Secondary voltage reflected to the primary when the primary MOSFET turns off
30	VMIN			98.16	V	Valley of the rectified minimum input AC voltage at full load
31	KP			0.68		Measure of continuous/discontinuous mode of operation
32	MODE_OPERATION			CCM		Mode of operation
33	DUTYCYCLE			0.508		Primary MOSFET duty cycle
34	TIME_ON			9.48	us	Primary MOSFET on-time
35	TIME_OFF			6.56	us	Primary MOSFET off-time
36	LPRIMARY_MIN			1916.3	uH	Minimum primary inductance
37	LPRIMARY_TYP			2017.1	uH	Typical primary inductance

38	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
39	LPRIMARY_MAX			2118.0	uH	Maximum primary inductance
40	**PRIMARY CURRENT**					
41	IPEAK_PRIMARY			0.547	A	Primary MOSFET peak current
42	IPEDESTAL_PRIMARY			0.157	A	Primary MOSFET current pedestal
43	IAVG_PRIMARY			0.164	A	Primary MOSFET average current
44	IRIPPLE_PRIMARY			0.447	A	Primary MOSFET ripple current
45	IRMS_PRIMARY			0.248	A	Primary MOSFET RMS current
46	**SECONDARY CURRENT**					
47	IPEAK_SECONDARY			10.765	A	Secondary winding peak current
48	IPEDESTAL_SECONDARY			3.094	A	Secondary winding current pedestal
49	IRMS_SECONDARY			5.203	A	Secondary winding RMS current
50	**TRANSFORMER CONSTRUCTION PARAMETERS**					
51	**CORE SELECTION**					
52	CORE	Custom	Info	Custom		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
53	CORE CODE	EF16		EF16		Core code
54	AE	20.10		20.10	mm^2	Core cross sectional area
55	LE	37.60		37.60	mm	Core magnetic path length
56	AL	1000		1000	nH/turns^2	Ungapped core effective inductance
57	VE	756.0		756.0	mm^3	Core volume
58	BOBBIN	Vertical		Vertical		Bobbin
59	AW	22.30		22.30	mm^2	Window area of the bobbin
60	BW	10.00		10.00	mm	Bobbin width
61	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
62	**PRIMARY WINDING**					
63	NPRIMARY			177		Primary turns
64	BPEAK			3589	Gauss	Peak flux density
65	BMAX			3217	Gauss	Maximum flux density
66	BAC			1290	Gauss	AC flux density (0.5 x Peak to Peak)
67	ALG			64	nH/turns^2	Typical gapped core effective inductance
68	LG			0.367	mm	Core gap length
69	LAYERS_PRIMARY			4		Number of primary layers
70	AWG_PRIMARY			33	AWG	Primary winding wire AWG
71	OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
72	OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
73	CMA_PRIMARY			202	Cmil/A	Primary winding wire CMA
74	**SECONDARY WINDING**					
75	NSECONDARY			9		Secondary turns
76	AWG_SECONDARY			20	AWG	Secondary winding wire AWG
77	OD_SECONDARY_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation
78	OD_SECONDARY_BARE			0.812	mm	Secondary winding wire outer diameter without insulation
79	CMA_SECONDARY			212	Cmil/A	Secondary winding wire CMA
80	**BIAS WINDING**					
81	NBIAS			23		Bias turns
82	**PRIMARY COMPONENTS SELECTION**					
83	**Line undervoltage**					
84	BROWN-IN REQURED			68.0	V	Required AC RMS line voltage brown-in threshold
85	RLS			3.38	MΩ	Connect two 1.69 MOhm resistors to the V-pin for the required UV/OV threshold
86	BROWN-IN ACTUAL			67.8	V	Actual AC RMS brown-in threshold

87	BROWN-OUT ACTUAL			61.3	V	Actual AC RMS brown-out threshold
88	Line overvoltage					
89	OVERVOLTAGE_LINE			282.5	V	Actual AC RMS line over-voltage threshold
90	**Bias diode**					
91	VBIAS			12.0	V	Rectified bias voltage
92	VF_BIAS			0.70	V	Bias winding diode forward drop
93	VREVERSE_BIASDIODE			62.72	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
94	CBIAS			22	uF	Bias winding rectification capacitor
95	CBPP			0.47	uF	BPP pin capacitor
96	**SECONDARY COMPONENTS**					
97	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
98	RFB_LOWER			34.00	kΩ	Lower feedback resistor
99	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
100	**MULTIPLE OUTPUT PARAMETERS**					
101	**OUTPUT 1**					
102	VOUT1			5.00	V	Output 1 voltage
103	IOUT1	1.20		1.20	A	Output 1 current
104	POUT1			6.00	W	Output 1 power
105	IRMS_SECONDARY1			1.923	A	Root mean squared value of the secondary current for output 1
106	IRIPPLE_CAP_OUTPUT1			1.503	A	Current ripple on the secondary waveform for output 1
107	AWG_SECONDARY1			24	AWG	Wire size for output 1
108	OD_SECONDARY1_INSULATED			0.815	mm	Secondary winding wire outer diameter with insulation for output 1
109	OD_SECONDARY1_BARE			0.511	mm	Secondary winding wire outer diameter without insulation for output 1
110	CM_SECONDARY1			385	Cmils	Bare conductor effective area in circular mils for output 1
111	NSECONDARY1			9		Number of turns for output 1
112	VREVERSE_RECTIFIER1			24.85	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
113	SRFET1	Auto		SI2318CDS		Secondary rectifier (Logic MOSFET) for output 1
114	VF_SRFET1			0.061	V	SRFET on-time drain voltage for output 1
115	VBREAKDOWN_SRFET1			40	V	SRFET breakdown voltage for output 1
116	RDSON_SRFET1			51.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
117	**OUTPUT 2**					
118	VOUT2	12.00		12.00	V	Output 2 voltage
119	IOUT2	0.750		0.750	A	Output 2 current
120	POUT2			9.00	W	Output 2 power
121	IRMS_SECONDARY2			1.202	A	Root mean squared value of the secondary current for output 2
122	IRIPPLE_CAP_OUTPUT2			0.939	A	Current ripple on the secondary waveform for output 2
123	AWG_SECONDARY2			26	AWG	Wire size for output 2
124	OD_SECONDARY2_INSULATED			0.709	mm	Secondary winding wire outer diameter with insulation for output 2
125	OD_SECONDARY2_BARE			0.405	mm	Secondary winding wire outer diameter without insulation for output 2

126	CM_SECONDARY2			240	Cmils	Bare conductor effective area in circular mils for output 2
127	NSECONDARY2			22		Number of turns for output 2
128	VREVERSE_RECTIFIER2			60.52	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
129	SRFET2	Auto		AOD2816		Secondary rectifier (Logic MOSFET) for output 2
130	VF_SRFET2			0.022	V	SRFET on-time drain voltage for output 2
131	VBREAKDOWN_SRFET2			80	V	SRFET breakdown voltage for output 2
132	RDSON_SRFET2			29.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
133	**OUTPUT 3**					
134	VOUT3			0.00	V	Output 3 voltage
135	IOUT3			0.000	A	Output 3 current
136	POUT3			0.00	W	Output 3 power
137	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
138	IRIPPLE_CAP_OUTPUT3			0.000	A	Current ripple on the secondary waveform for output 3
139	AWG_SECONDARY3			0	AWG	Wire size for output 3
140	OD_SECONDARY3_INSULATED			0.000	mm	Secondary winding wire outer diameter with insulation for output 3
141	OD_SECONDARY3_BARE			0.000	mm	Secondary winding wire outer diameter without insulation for output 3
142	CM_SECONDARY3			0	Cmils	Bare conductor effective area in circular mils for output 3
143	NSECONDARY3			0		Number of turns for output 3
144	VREVERSE_RECTIFIER3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
145	SRFET3	Auto		NA		Secondary rectifier (Logic MOSFET) for output 3
146	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
147	VBREAKDOWN_SRFET3			NA	V	SRFET breakdown voltage for output 3
148	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3
149	PO_TOTAL			15.00	W	Total power of all outputs
150	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
151	**TOLERANCE ANALYSIS**					
152	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
153	CORNER_ILIMIT	TYP		0.550	A	Current limit corner to be evaluated
154	CORNER_LPRIMARY	TYP		2017.1	uH	Primary inductance corner to be evaluated
155	MODE_OPERATION			CCM		Mode of operation
156	KP			0.752		Measure of continuous/discontinuous mode of operation
157	FSWITCHING			62551	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
158	DUTYCYCLE			0.51		Steady state duty cycle
159	TIME_ON			8.120	us	Primary MOSFET on-time
160	TIME_OFF			7.87	us	Primary MOSFET off-time
161	IPEAK_PRIMARY			0.52	A	Primary MOSFET peak current

162	IPEDESTAL_PRIMARY			0.129	A	Primary MOSFET current pedestal
163	IAVERAGE_PRIMARY			0.164	A	Primary MOSFET average current
164	IRIPPLE_PRIMARY			0.390	A	Primary MOSFET ripple current
165	IRMS_PRIMARY			0.244	A	Primary MOSFET RMS current
166	CMA_PRIMARY			205.000	Cmil/A	Primary winding wire CMA
167	BPEAK			3192	Gauss	Peak flux density
168	BMAX			2941	Gauss	Maximum flux density
169	BAC			1106	Gauss	AC flux density (0.5 x Peak to Peak)

9 Performance Data

9.1 *Efficiency*

9.1.1 *Average Efficiency Measured across PCB Connector*

9.1.1.1 85 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
85	471.6	18.06	5.0	1200	5.94	10.95	749.7	8.21	78.4
85	358.1	13.08	4.9	900	4.43	10.92	562.4	6.138	80.8
85	252.8	8.66	5.0	600	2.99	11.04	374.8	4.139	82.4
85	139.7	4.27	5.0	300	1.50	11.05	187.3	2.07	83.7
						Average Efficiency (%)			**81.3**

9.1.1.2 115 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
115	367.3	17.25	4.9	1200	5.92	10.94	749.7	8.202	81.9
115	286.5	12.82	5.0	900	4.48	11.03	562.3	6.204	83.3
115	203.1	8.50	5.0	600	2.99	11.05	374.8	4.141	83.9
115	113.4	4.23	5.0	300	1.50	11.05	187.3	2.071	84.5
						Average Efficiency (%)			**83.4**

9.1.1.3 230 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
230	224.4	16.73	5.0	1200	5.96	11.04	749.7	8.273	85.1
230	176.9	12.57	5.0	900	4.48	11.05	562.3	6.215	85.1
230	126.5	8.41	5.0	600	2.99	11.05	374.8	4.143	84.9
230	70.7	4.26	5.0	300	1.5	11.06	187.3	2.071	83.8
						Average Efficiency (%)			**84.7**

9.1.1.4 265 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
265	204.1	16.71	5.0	1200	5.96	11.04	749.7	8.273	85.2
265	161.1	12.58	5.0	900	4.48	11.05	562.3	6.215	85.0
265	115.3	8.43	5.0	600	3.00	11.06	374.8	4.144	84.7
265	64.6	4.29	5.0	300	1.5	11.06	187.3	2.071	83.2
						Average Efficiency (%)			**84.5**

9.1.1.5 277 VAC

Input Measurement			Output 1 Measurement			Output 2 Measurement			
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
277	198.1	16.72	5.0	1200	5.96	11.04	749.7	8.273	85.1
277	156.5	12.59	5.0	900	4.48	11.06	562.4	6.219	85.0
277	112.0	8.44	5.0	600	3.00	11.06	374.8	4.144	84.6
277	62.9	4.30	5.0	300	1.5	11.06	187.3	2.071	83.0
						Average Efficiency (%)			**84.4**

9.1.2 *Full Load Efficiency vs. Line*

Test Condition: Soak for 10 minutes and 5 minutes for each line/step

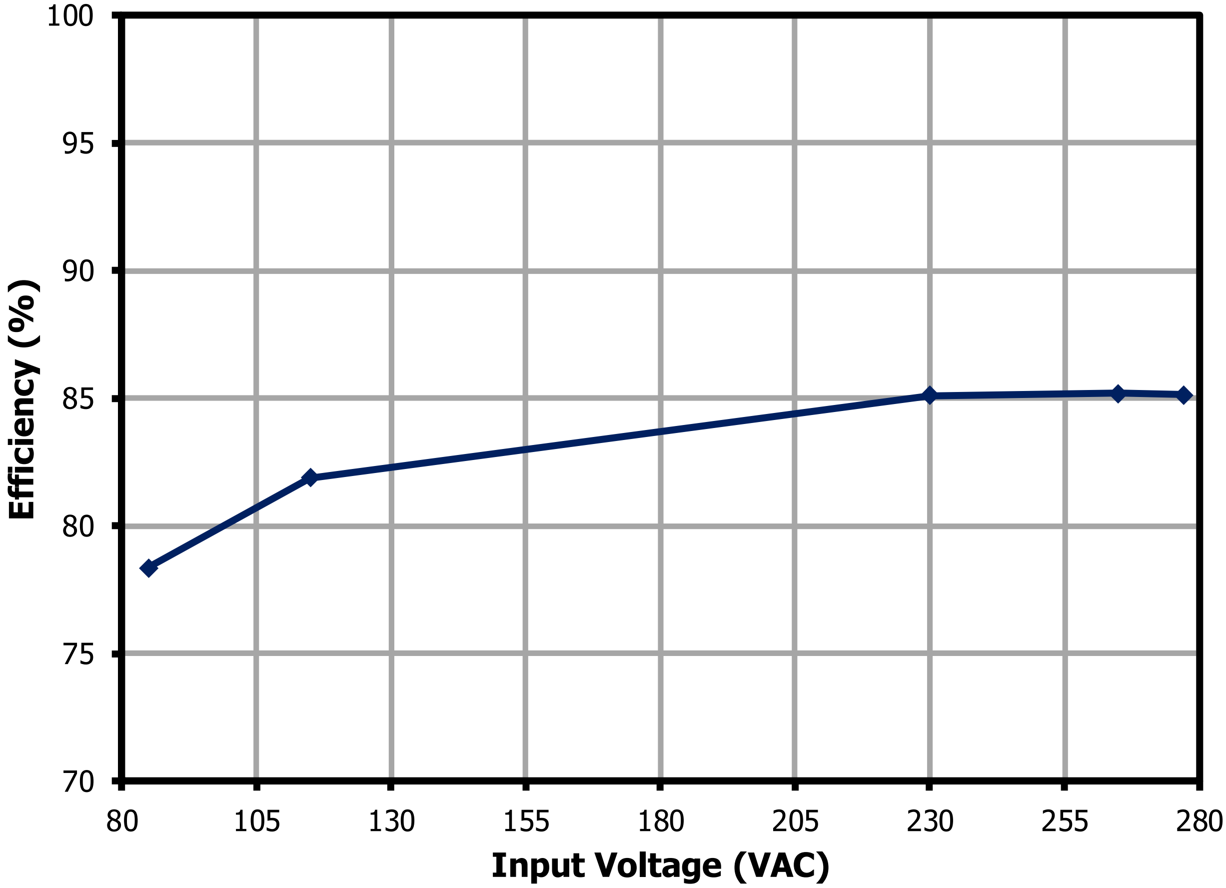


Figure 8 – Full Load Efficiency vs. Input AC Line Voltage.

9.1.3 *Efficiency vs. Load*

Test Condition: Soak for 10 minutes and 5 minutes for each line/step

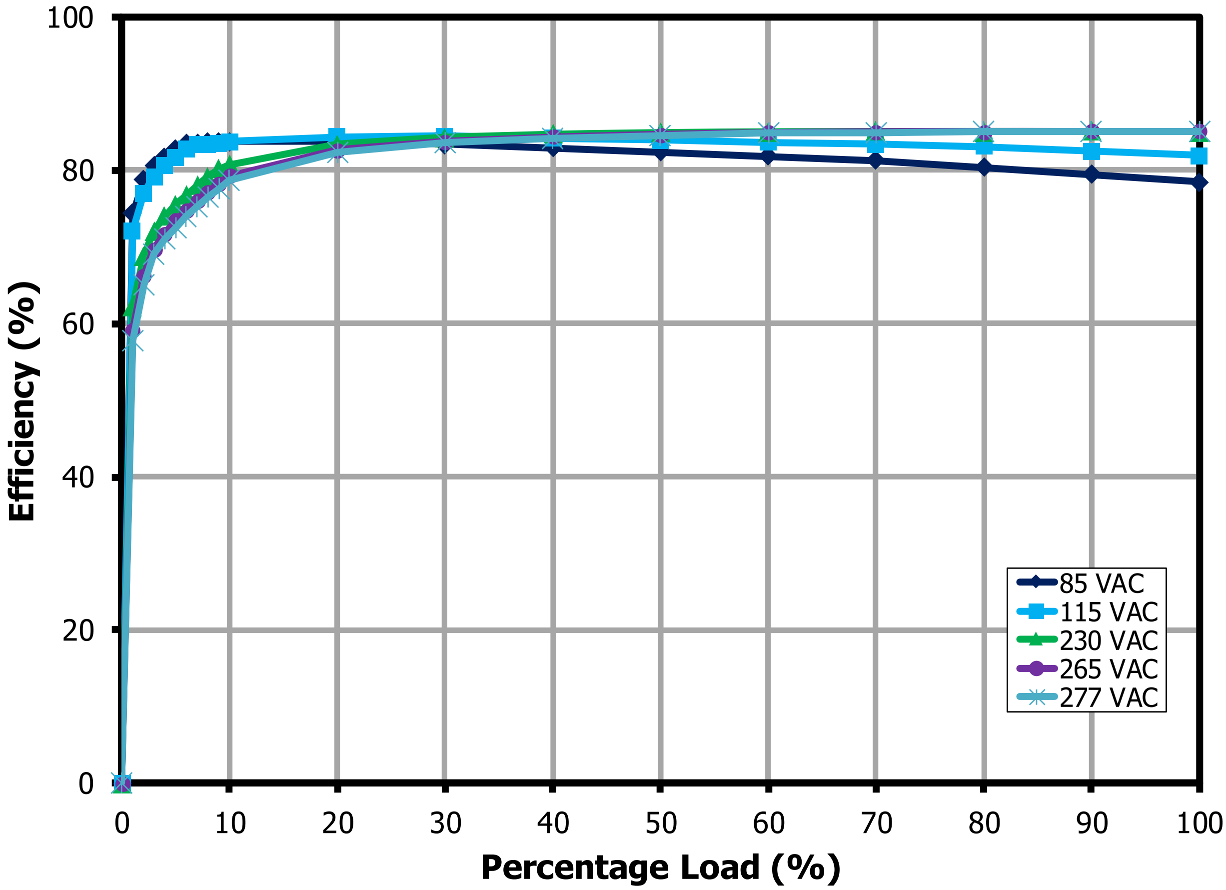


Figure 9 – Efficiency vs. Percentage Load.

9.1.4 *Standby Mode Efficiency*

Test Condition: Soak at full load for 5 minutes and decrease load to standby mode for 5 minutes for each line step.

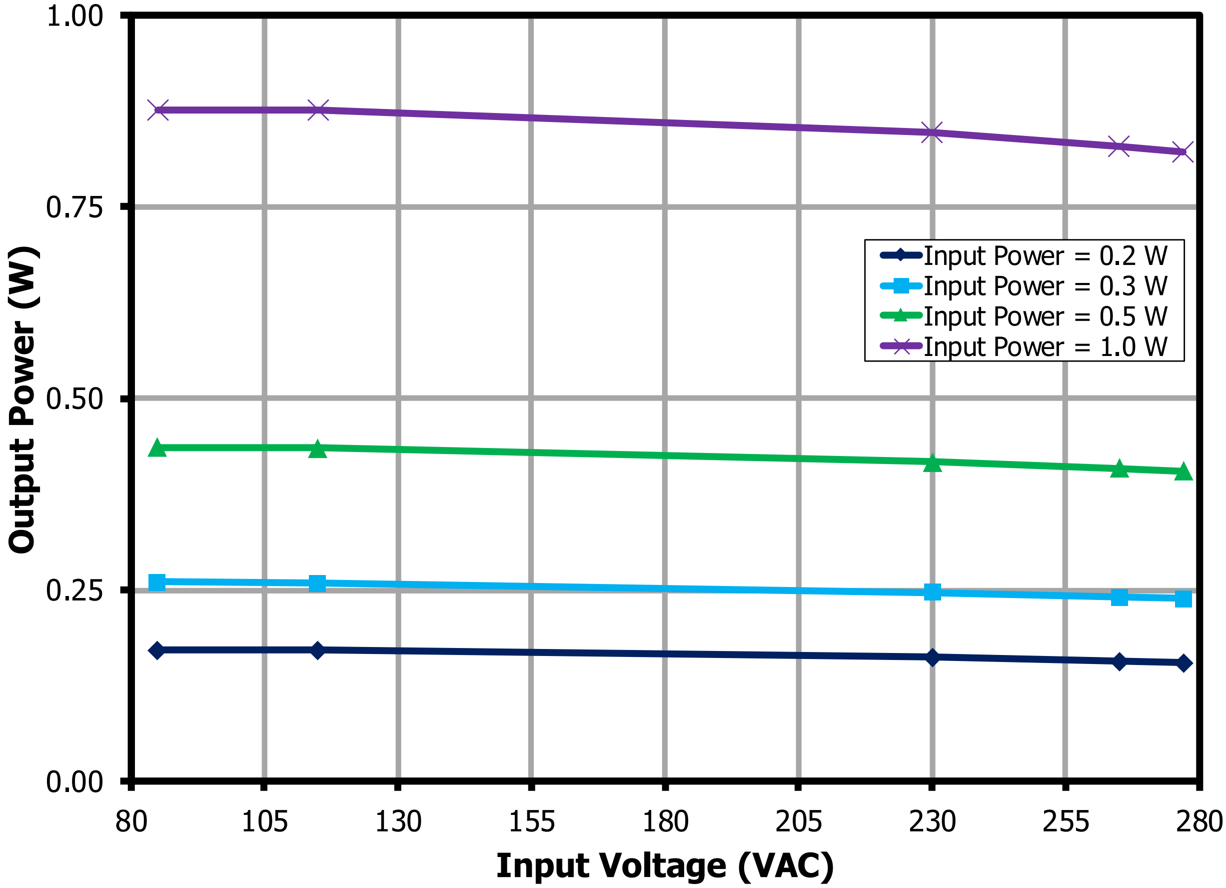


Figure 10 – Available Output Power per Input Power.

9.1.4.1 0.2 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	12.9	0.20	5.0	34	0.17	12.99	0.000	0.000	85.6
115	11.2	0.20	5.0	34	0.17	12.95	0.000	0.000	85.4
230	8.6	0.20	5.0	32	0.16	12.78	0.000	0.000	81.3
265	8.4	0.20	5.0	31	0.16	12.73	0.000	0.000	78.4
277	8.3	0.20	5.0	31	0.16	12.71	0.000	0.000	77.7

9.1.4.2 0.3 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	16.6	0.30	5.0	52	0.26	13.21	0.000	0.000	86.4
115	14.1	0.30	5.0	51	0.26	13.16	0.000	0.000	86.0
230	10.4	0.30	5.0	49	0.25	12.99	0.000	0.000	81.9
265	9.7	0.30	5.0	48	0.24	12.96	0.000	0.000	80.1
277	9.6	0.30	5.0	47	0.24	12.96	0.000	0.000	79.5

9.1.4.3 0.5 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	24.1	0.50	5.0	87	0.44	13.25	0.000	0.000	87.3
115	20.0	0.50	5.0	87	0.44	13.41	0.000	0.000	87.1
230	13.5	0.50	5.0	82	0.42	13.25	0.000	0.000	83.4
265	12.7	0.50	5.0	81	0.41	13.21	0.000	0.000	81.7
277	12.4	0.50	5.0	81	0.41	13.20	0.000	0.000	81.1

9.1.4.4 1.0 W Input Power

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
85	41.4	1.00	5.0	175	0.88	13.99	0.000	0.000	87.5
115	34.0	1.00	5.0	175	0.88	13.94	0.000	0.000	87.5
230	21.9	1.00	5.0	169	0.85	13.73	0.000	0.000	84.5
265	20.1	1.00	5.0	166	0.83	13.69	0.000	0.000	82.7
277	19.6	1.00	5.0	165	0.82	13.68	0.000	0.000	82.1

9.2 ***No-Load Input Power***

Soak for 15 minutes and 3 minutes integration time for each line/step.

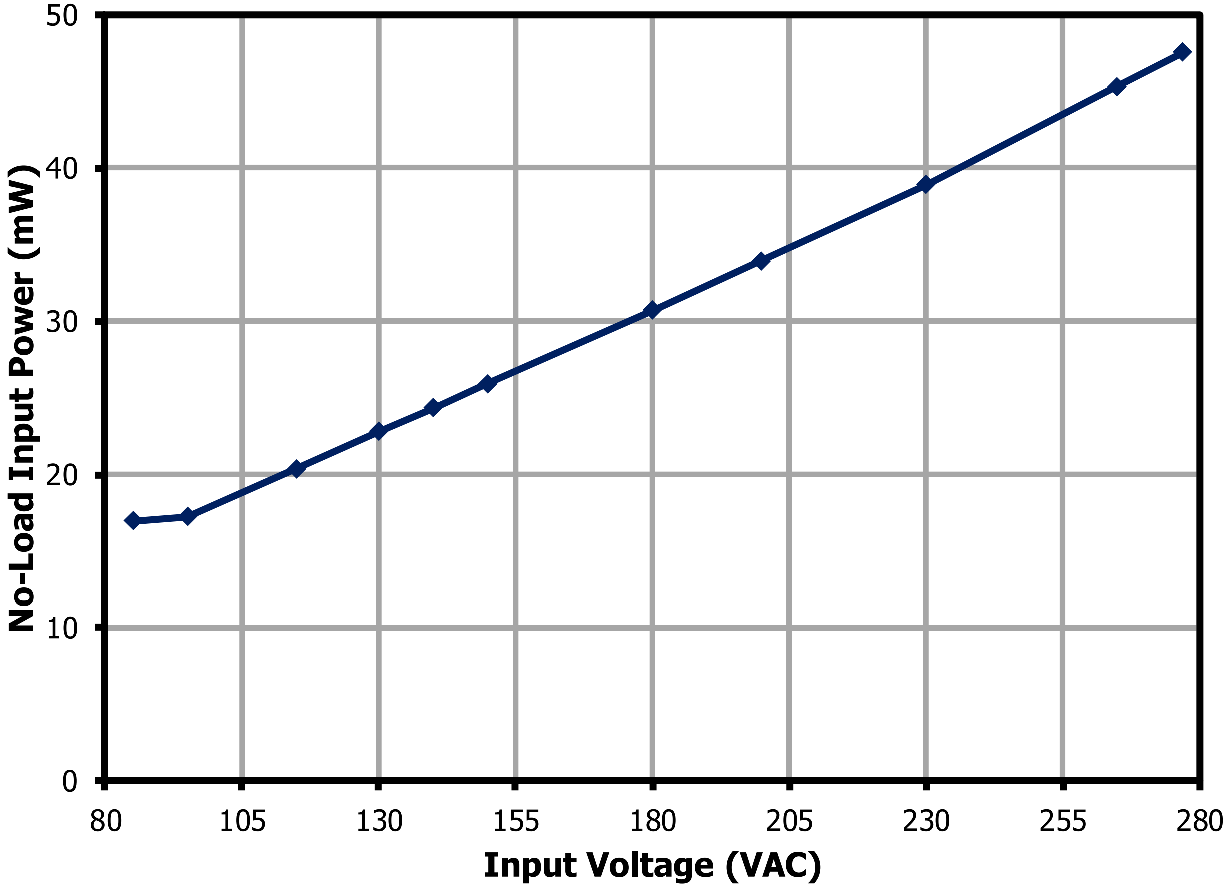


Figure 11 – No-Load Input Power vs. Input Line Voltage (Room Temperature).

9.3 *Line Regulation*

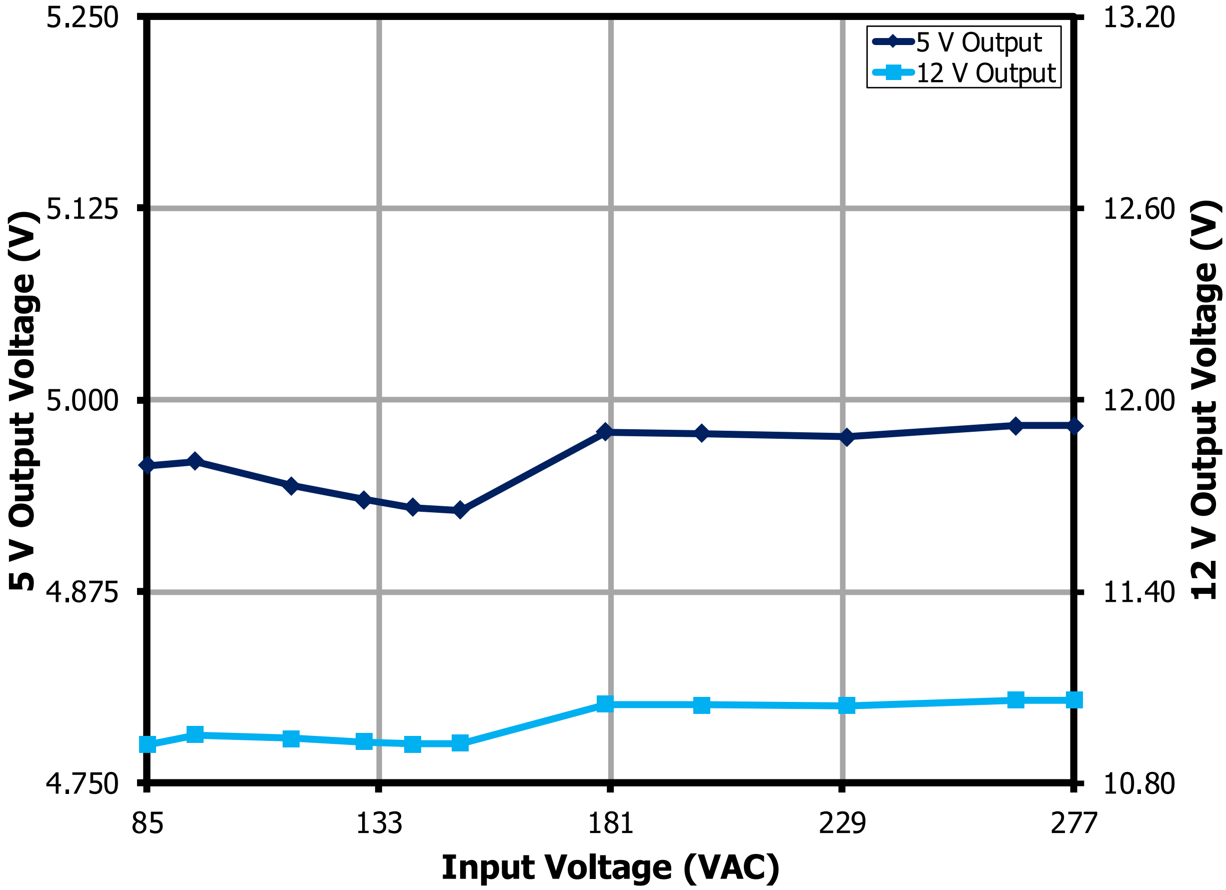


Figure 12 – Line Regulation.

9.4 ***Load Regulation***

9.4.1 *5 V Load Regulation with Balanced Load*

Test Condition: Simultaneous load change across 5 V and 12 V output

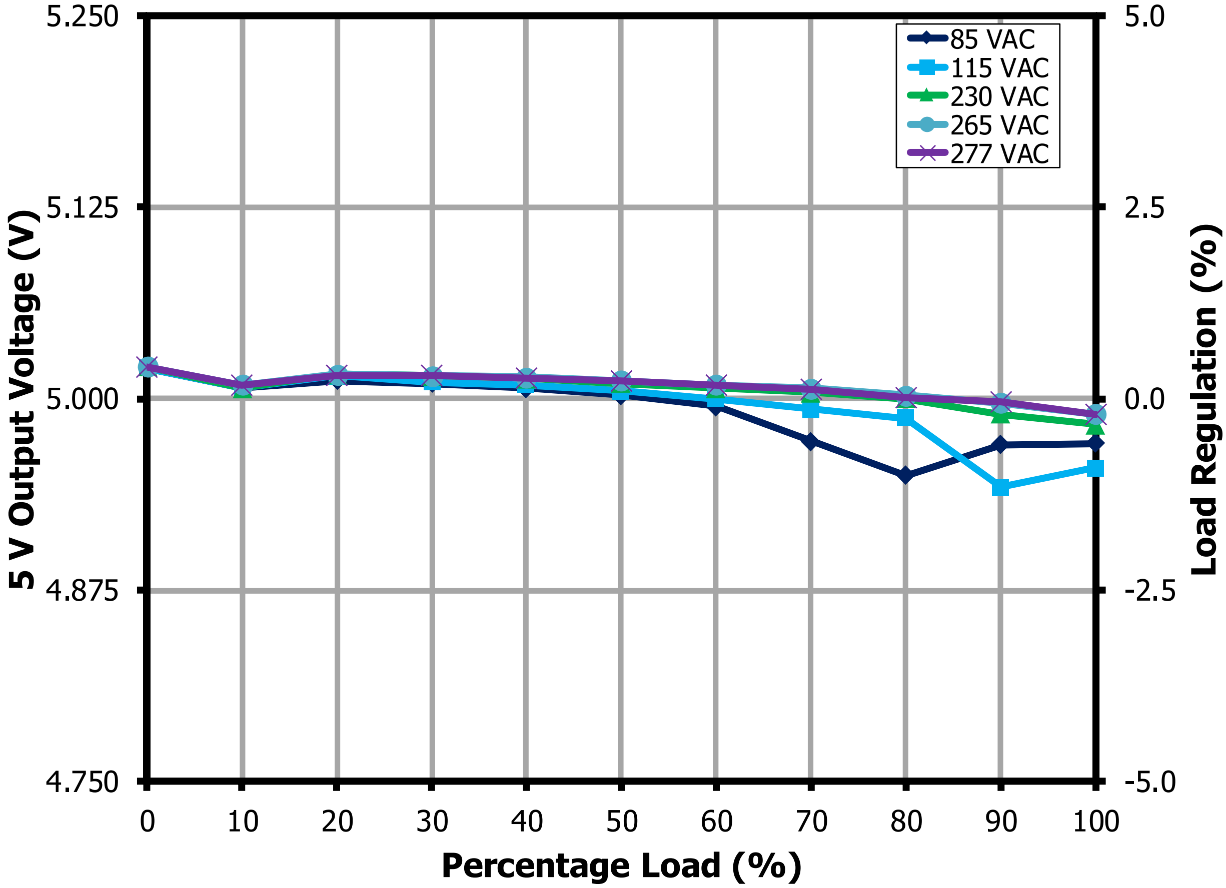


Figure 13 – 5 V Load Regulation with Balanced Load.

9.4.2 *12 V Load Regulation with Balanced Load*

Test Condition: Simultaneous load change across 5 V and 12 V output

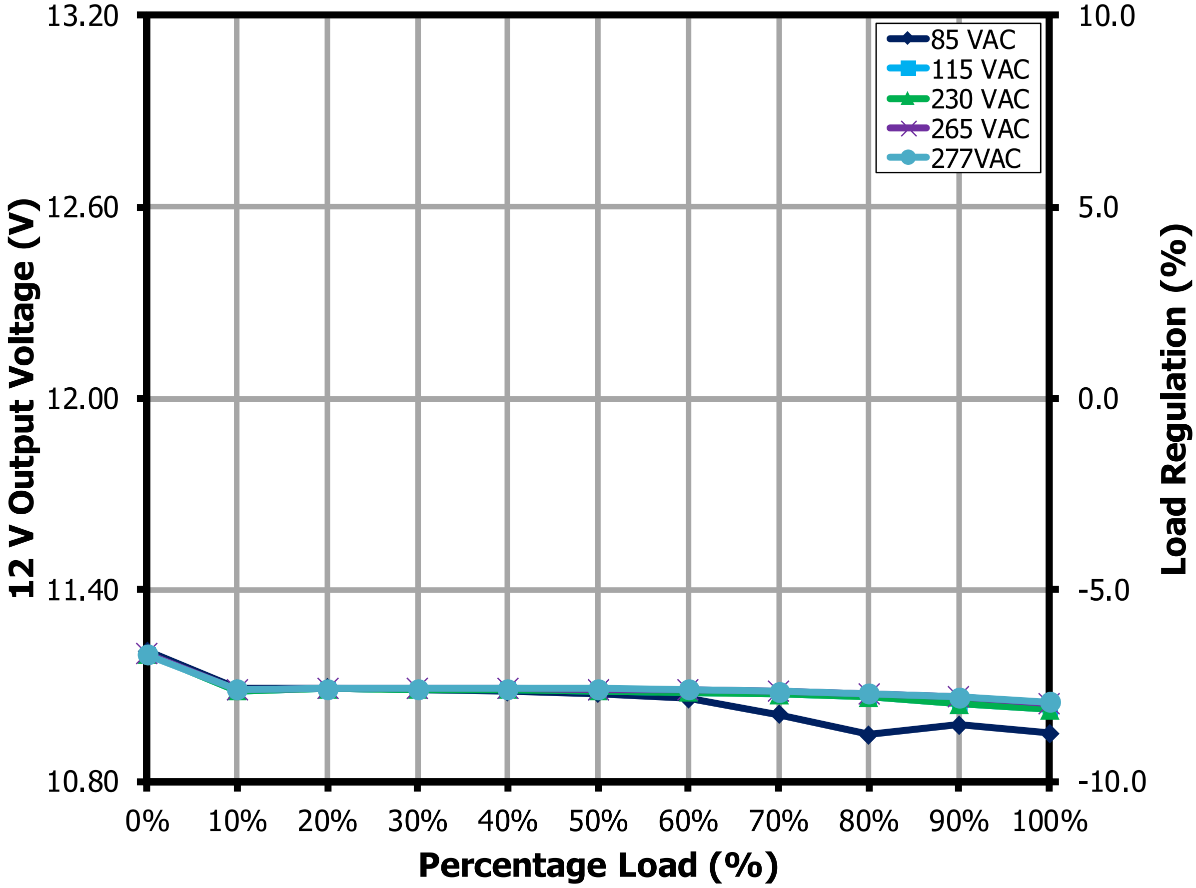


Figure 14 – 12 V Load Regulation with Balanced Load.

9.4.3 *5 V Load Regulation with Fixed Full Load Across 12 V Output*

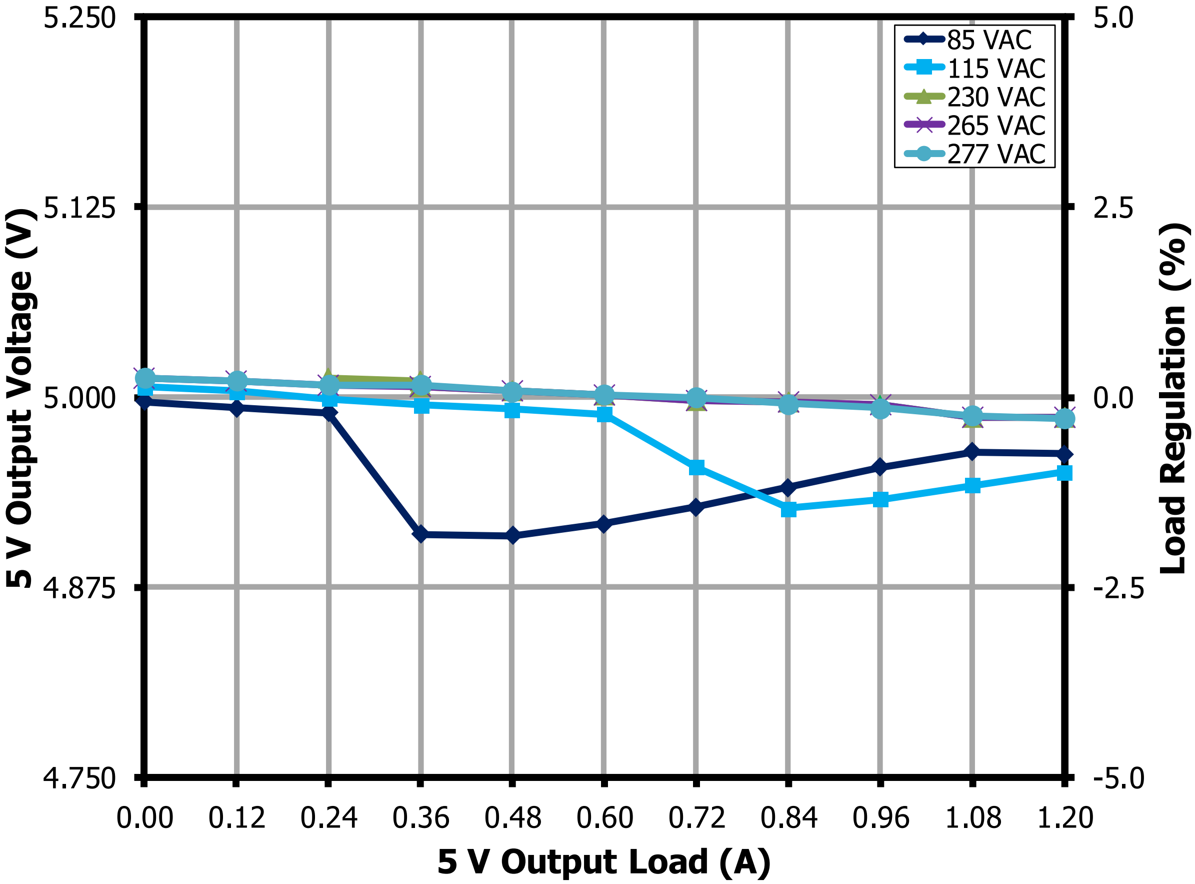


Figure 15 – 5 V Load Regulation with Fixed Full Load Across 12 V Output.

9.4.4 *5 V Load Regulation with Fixed Minimum Load Across 12 V Output*

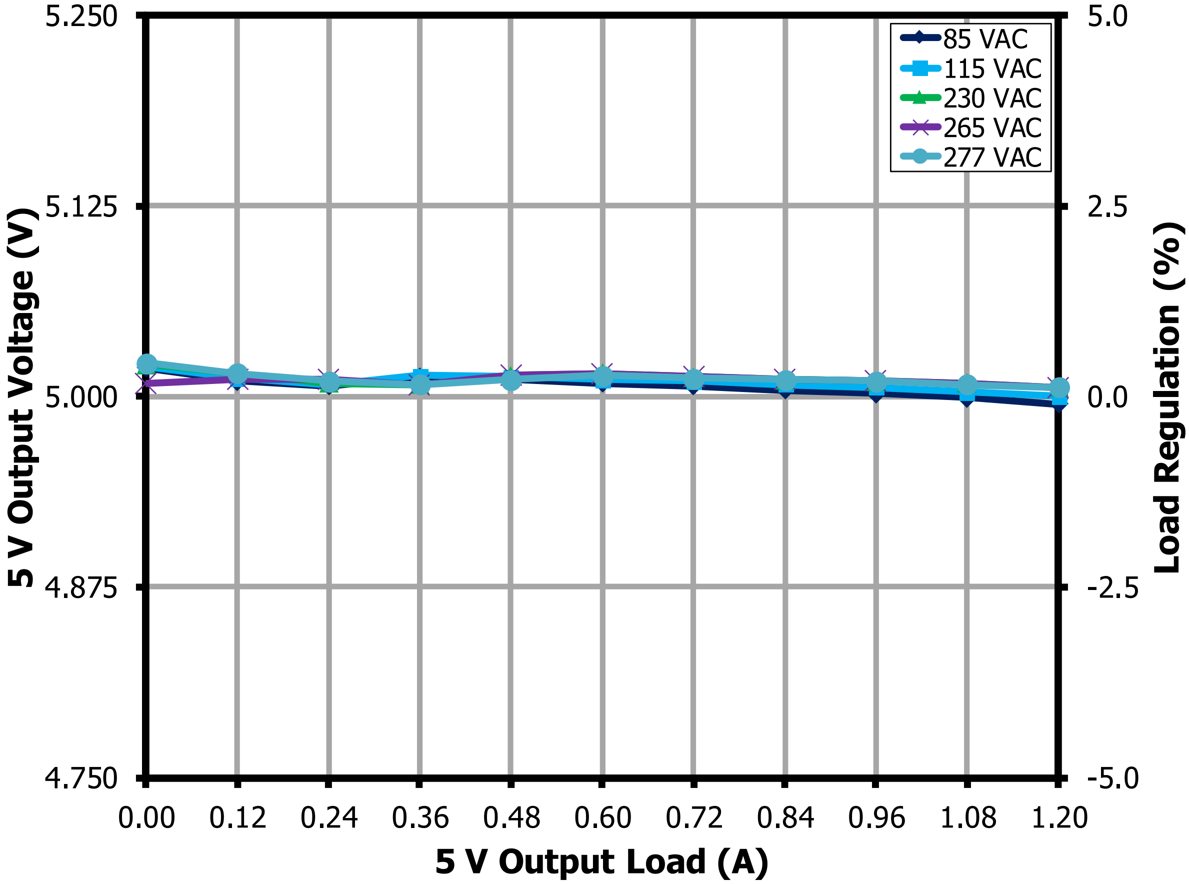


Figure 16 – 5 V Load Regulation with Fixed Minimum Load Across 12 V Output.

9.4.5 *12 V Load Regulation with Fixed Full Load Across 5 V Output*

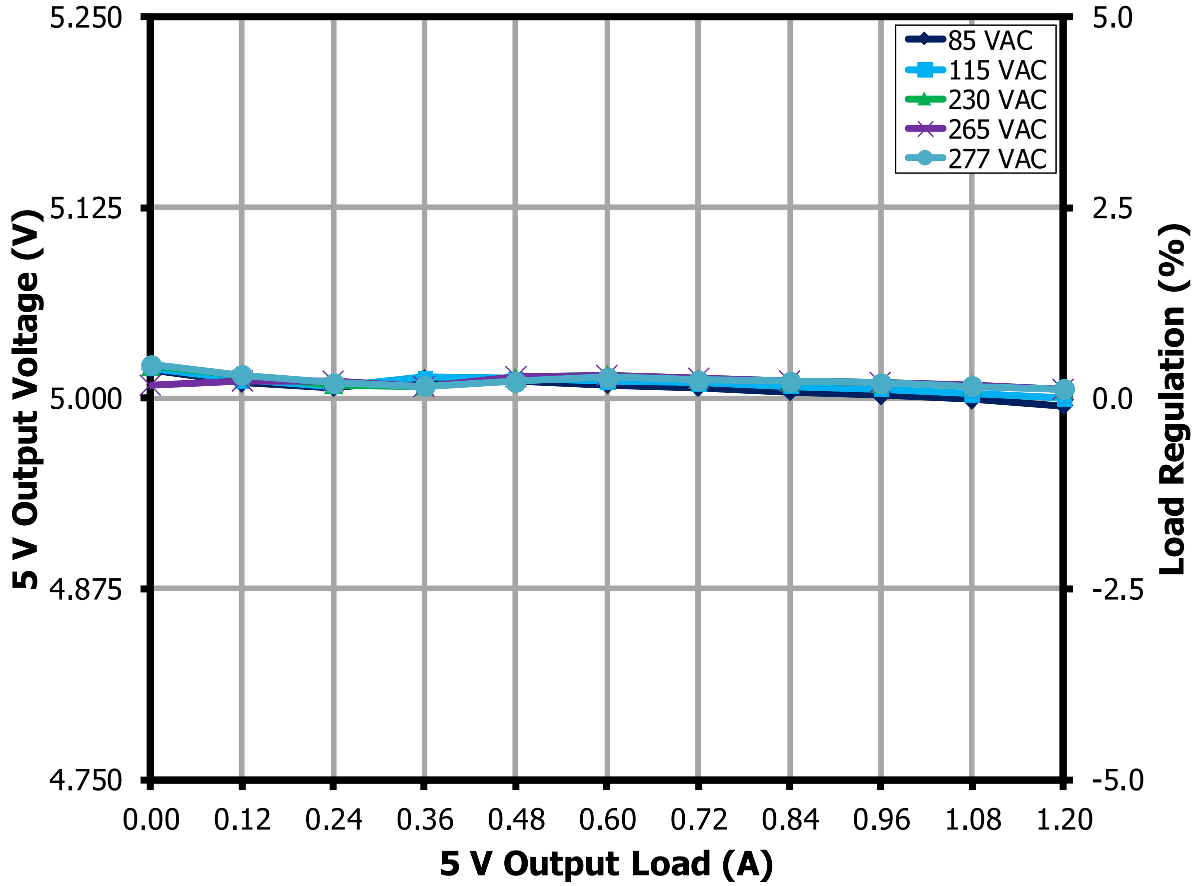


Figure 17 – 12 V Load Regulation with Fixed Full Load Across 5 V Output.

9.4.6 *12 V Load Regulation with Fixed Minimum Load Across 5 V Output*

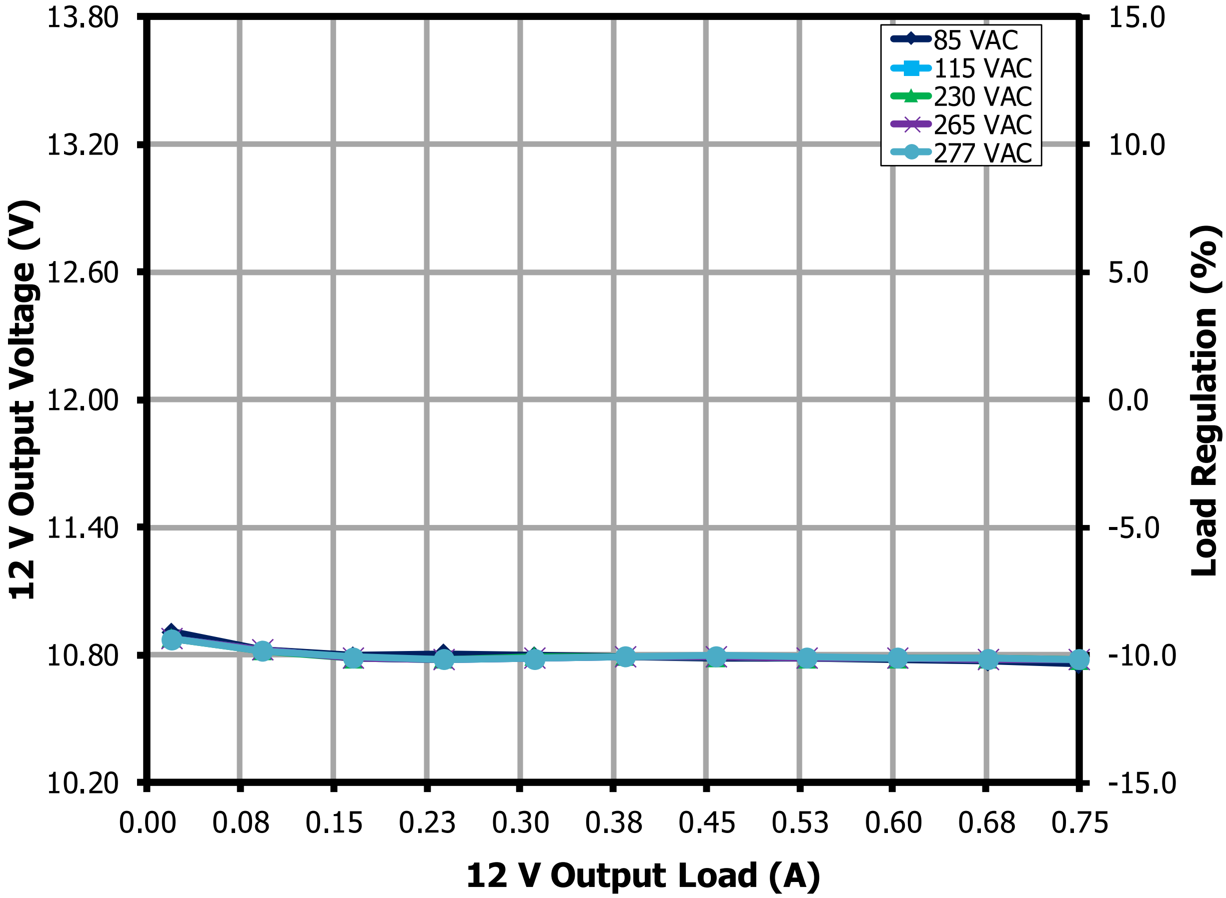


Figure 18 – 12 V Load Regulation with Fixed Minimum Load Across 5 V Output.

10 Test Waveforms

10.1 *Load Transient Response*

10.1.1 *5 V and 12 V 0% - 100% Load Change*

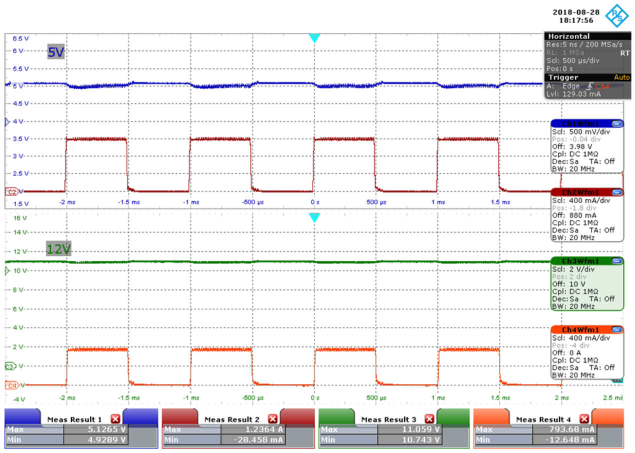


Figure 19 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.743 V.

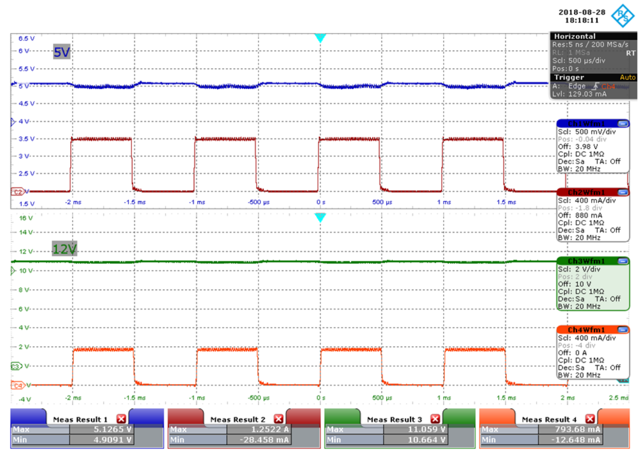


Figure 20 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.9091 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.664 V.

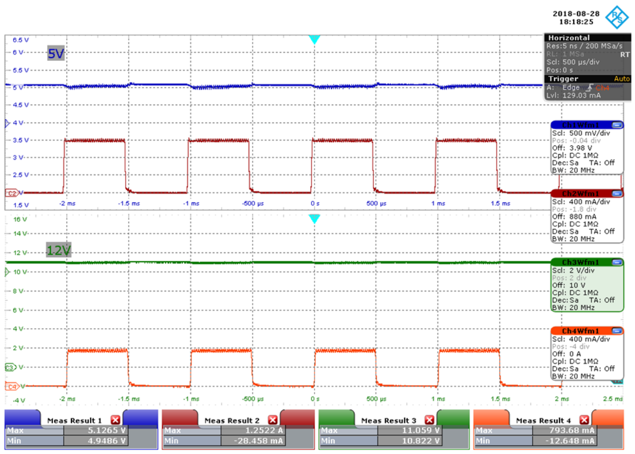


Figure 21 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V .

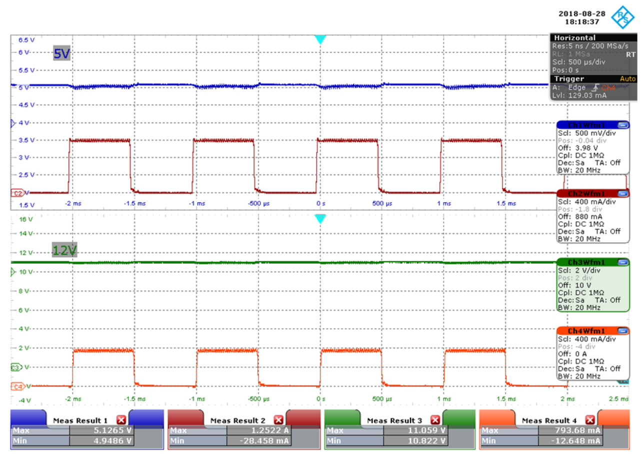


Figure 22 – 277 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.9486 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V.

10.1.2 *5 V and 12 V 0% - 50% Load Change*

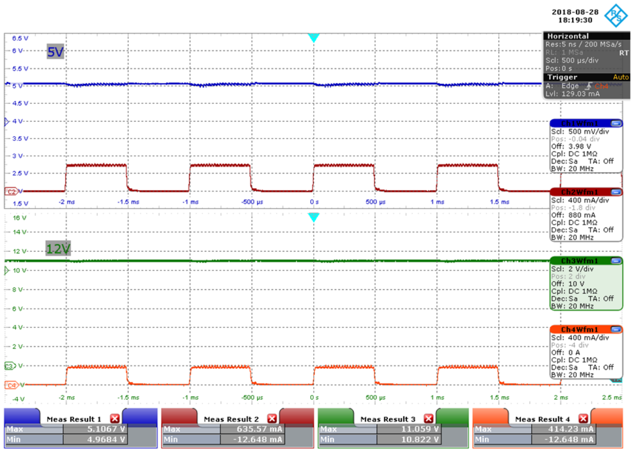


Figure 23 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V.

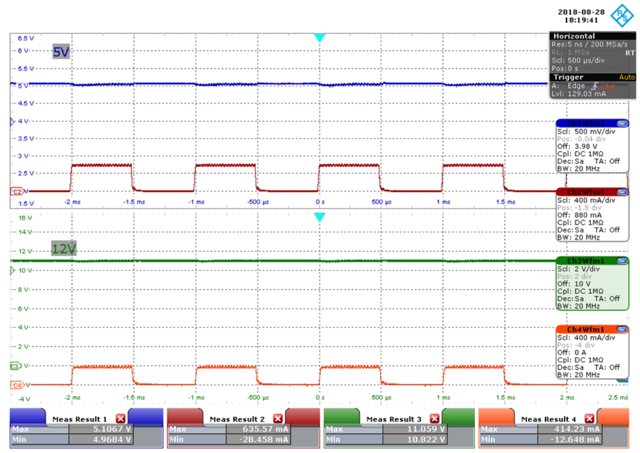


Figure 24 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V.

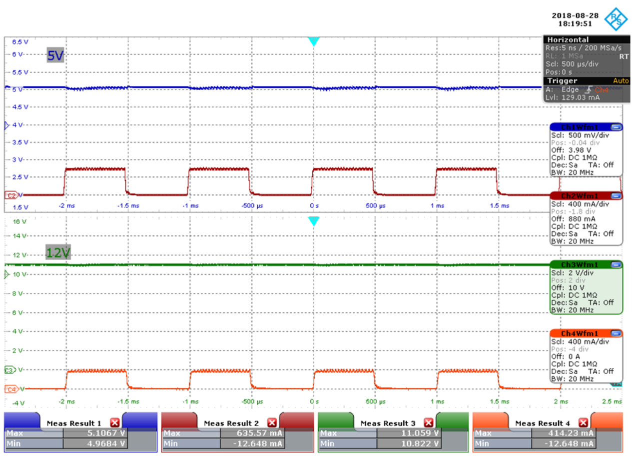


Figure 25 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V.

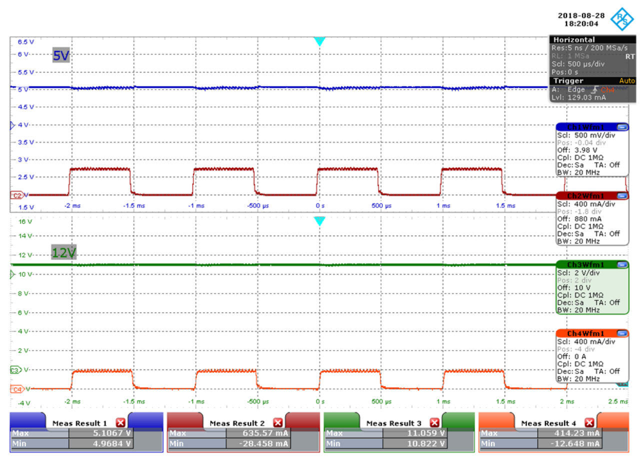


Figure 26 – 277 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9684 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.822 V.

10.1.3 *5 V 0% - 100% Load Change, 12 V Fixed 100% Load*

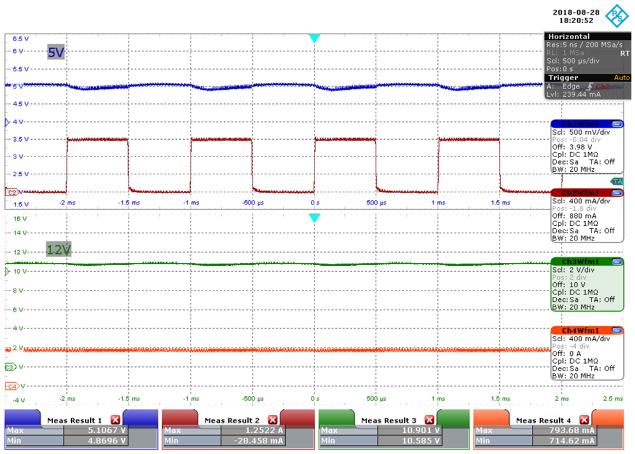


Figure 27 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.8696 V.
12 V_{MAX}: 10.901 V, 12 V_{MIN}: 11.585 V.

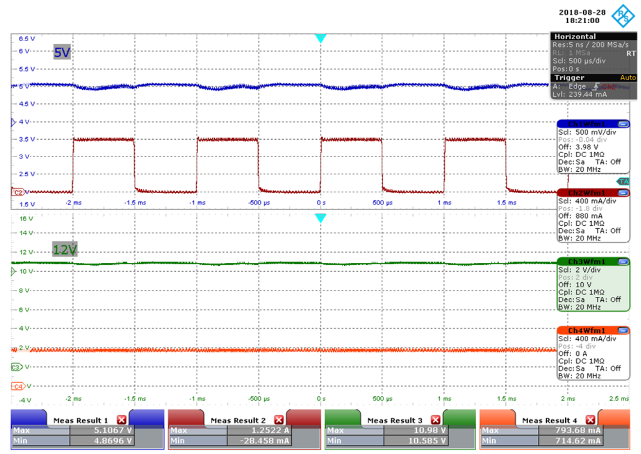


Figure 28 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.8696 V.
12 V_{MAX}: 10.98 V, 12 V_{MIN}: 10.585 V.

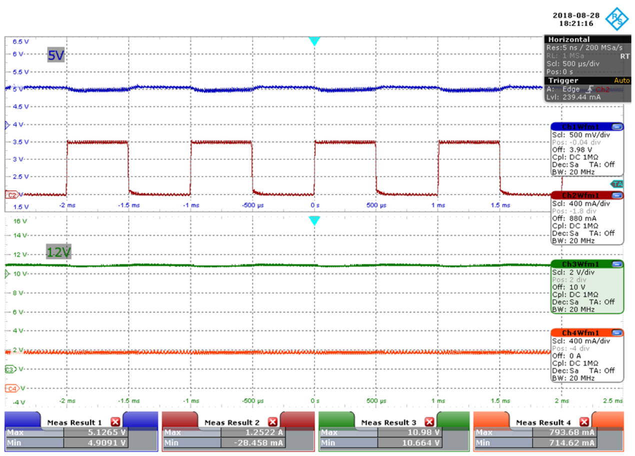


Figure 29 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.9091 V.
12 V_{MAX}: 10.98 V, 12 V_{MIN}: 10.664 V.

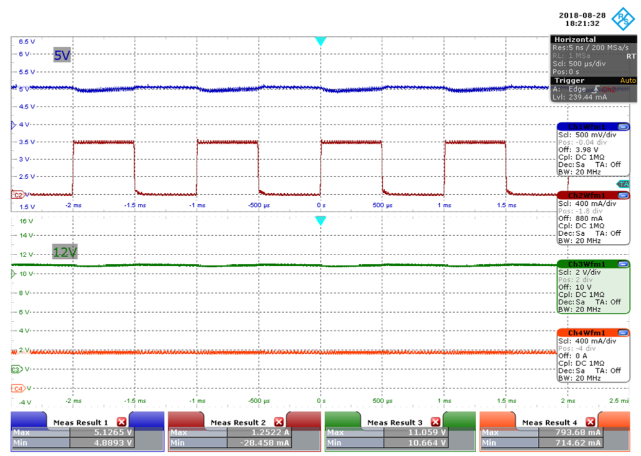


Figure 30 – 277 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 µs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 µs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 µs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 µs / div.
5 V_{MAX}: 5.1265 V, 5 V_{MIN}: 4.8893 V.
12 V_{MAX}: 11.059 V, 12 V_{MIN}: 10.664 V.

10.1.4 *12 V 0% - 100% Load Change, 5 V Fixed 100% Load*

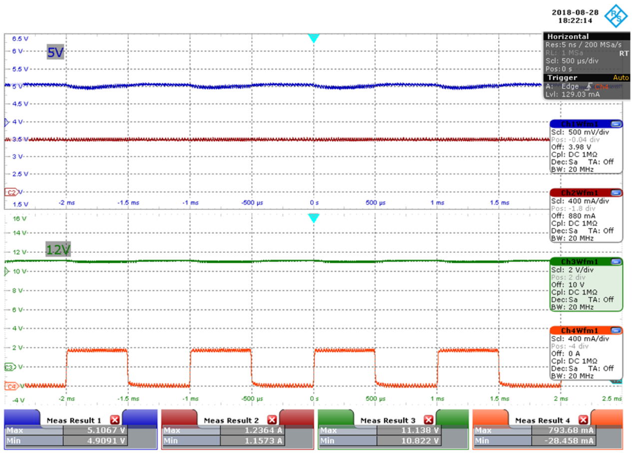


Figure 31 – 85 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 μs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 μs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 μs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 μs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9091 V.
12 V_{MAX}: 11.138 V, 12 V_{MIN}: 10.822 V.

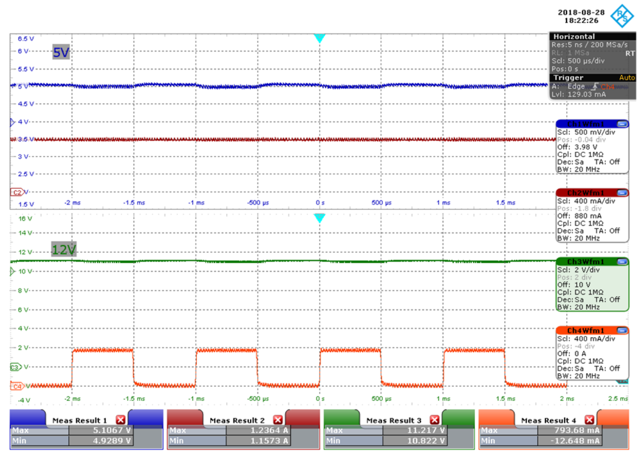


Figure 32 – 115 VAC 60 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 μs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 μs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 μs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 μs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.217 V, 12 V_{MIN}: 10.822 V.

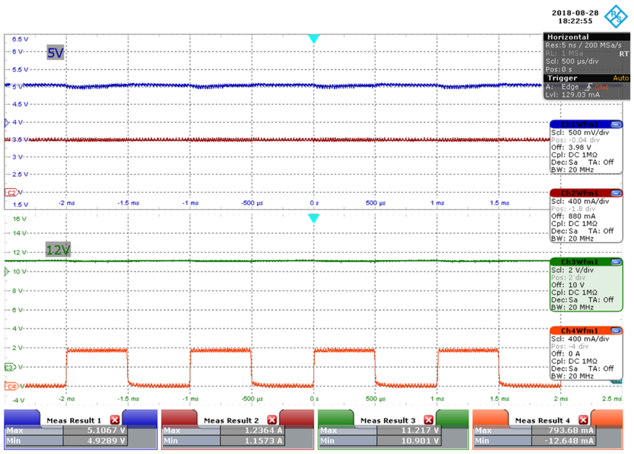


Figure 33 – 230 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 μs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 μs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 μs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 μs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.271 V, 12 V_{MIN}: 10.901 V.

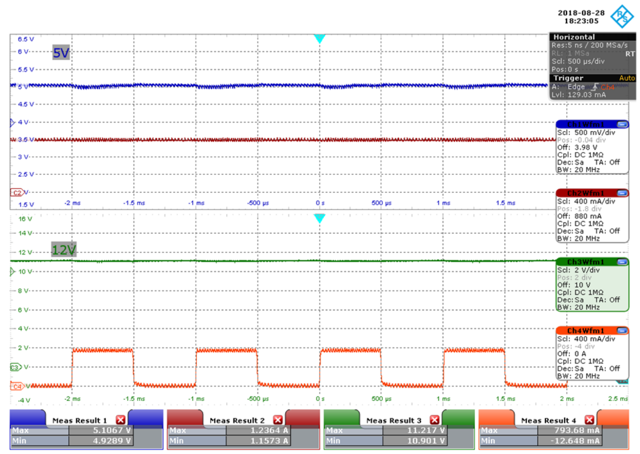


Figure 34 – 277 VAC 50 Hz.
CH1: 5 V_{OUT}, 500 mV / div., 500 μs / div.
CH2: 5 V I_{LOAD}, 400 mA / div., 500 μs / div.
CH3: 12 V_{OUT}, 2 V / div., 500 μs / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 500 μs / div.
5 V_{MAX}: 5.1067 V, 5 V_{MIN}: 4.9289 V.
12 V_{MAX}: 11.217 V, 12 V_{MIN}: 10.901 V.

10.2 ***Output Voltage at Start-up***

10.2.1 *CC mode*

10.2.1.1 100% Load

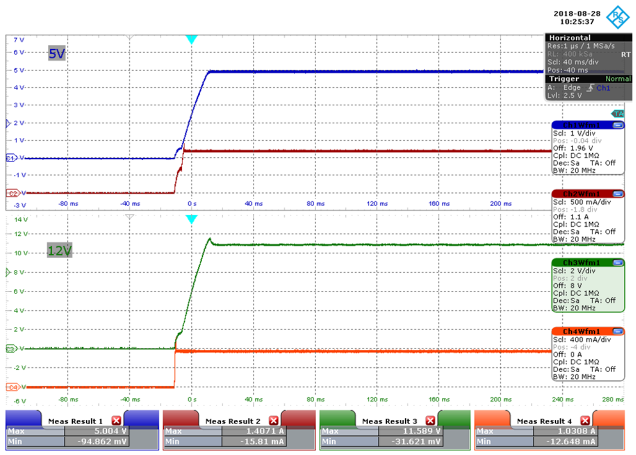


Figure 35 – 85 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

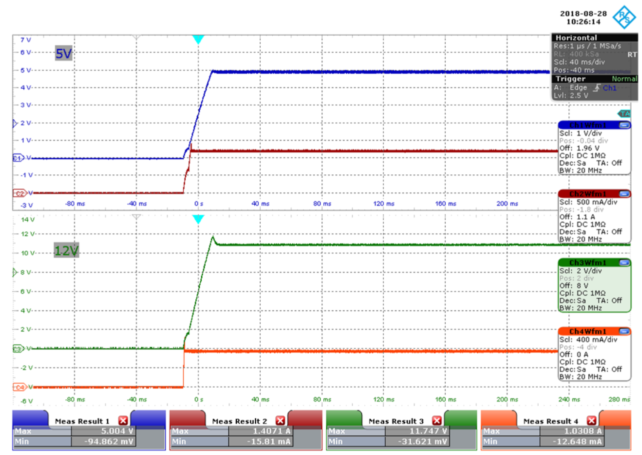


Figure 36 – 115 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

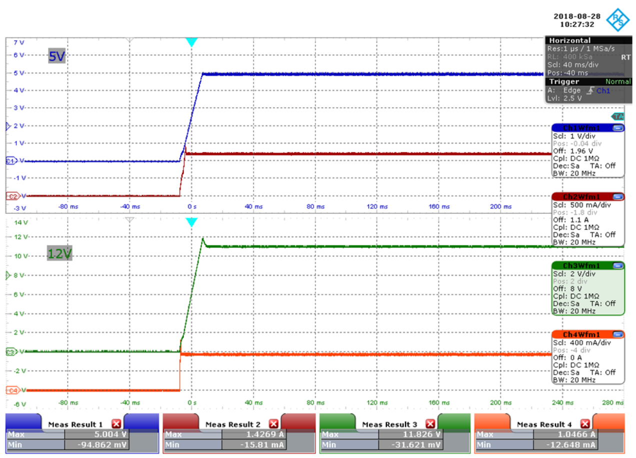


Figure 37 – 230 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

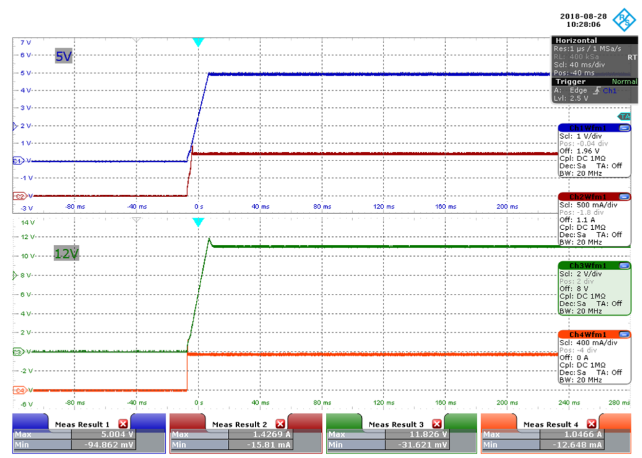


Figure 38 – 277 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

10.2.1.2 0% Load

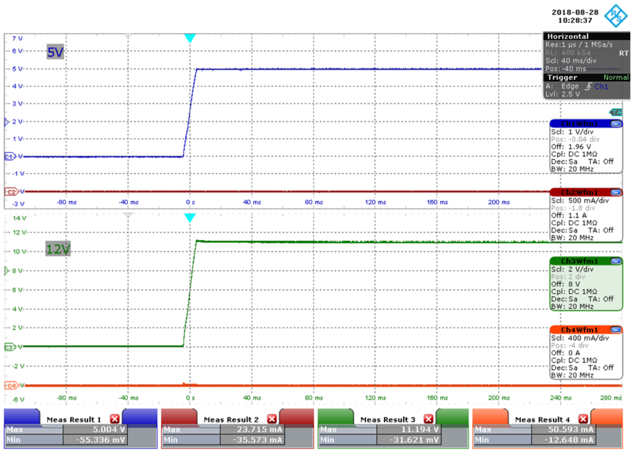


Figure 39 – 85 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

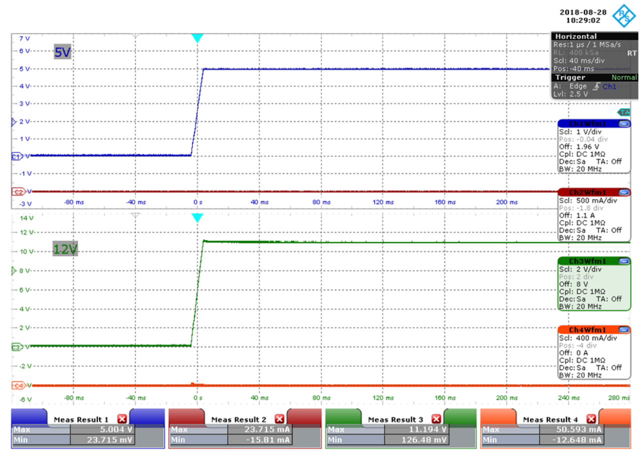


Figure 40 – 115 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

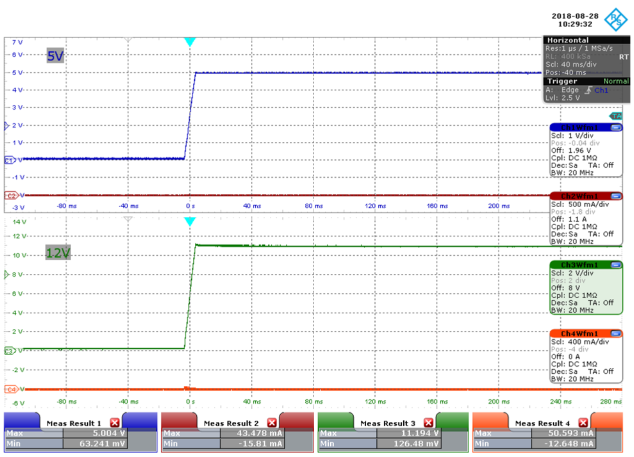


Figure 41 – 230 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

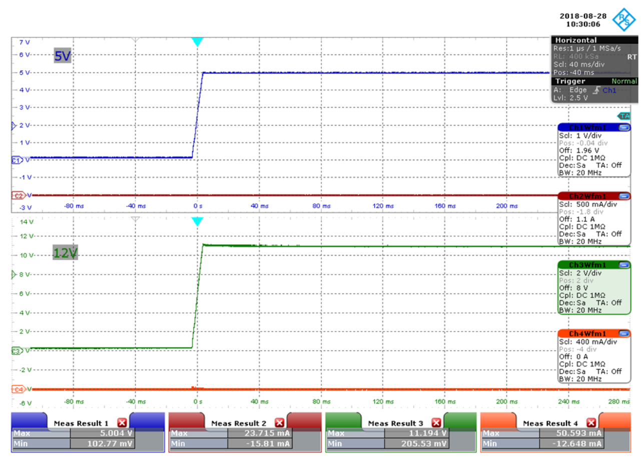


Figure 42 – 277 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

10.2.2 *CR mode*

10.2.2.1 100% Load

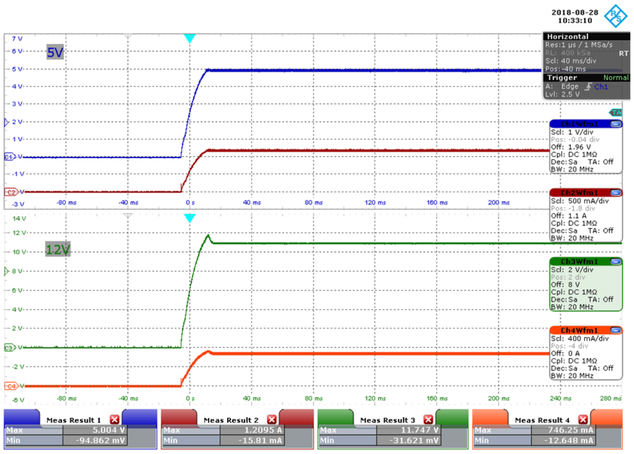


Figure 43 – 85 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

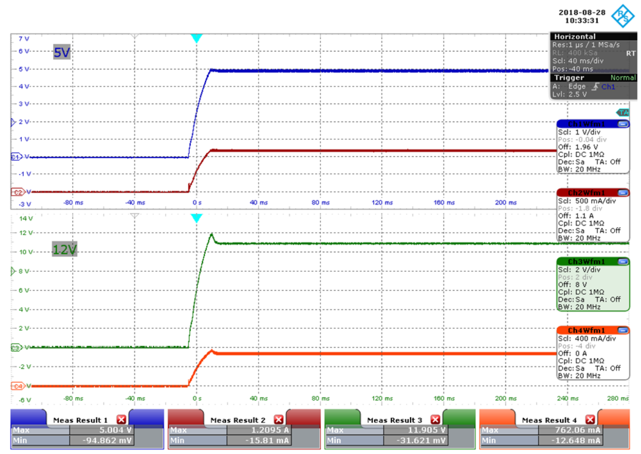


Figure 44 – 115 VAC 60 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

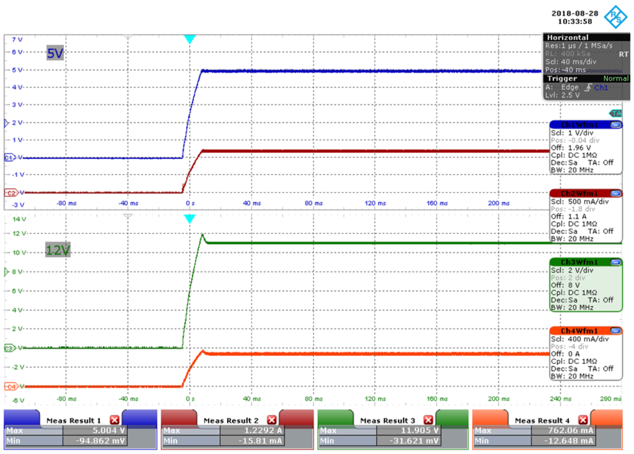


Figure 45 – 230 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

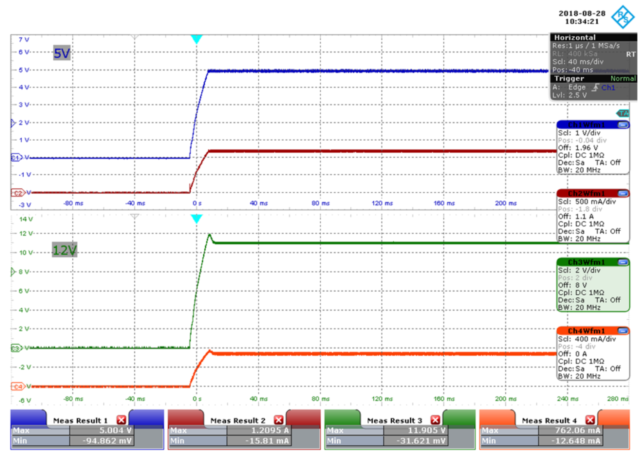


Figure 46 – 277 VAC 50 Hz, Full Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

10.2.2.2 0% Load

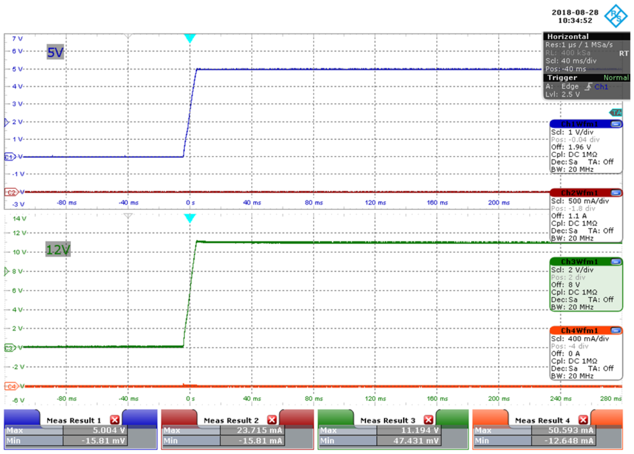


Figure 47 – 85 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

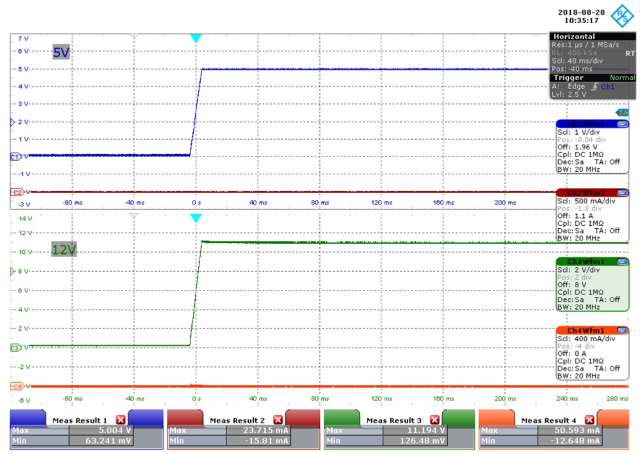


Figure 48 – 115 VAC 60 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

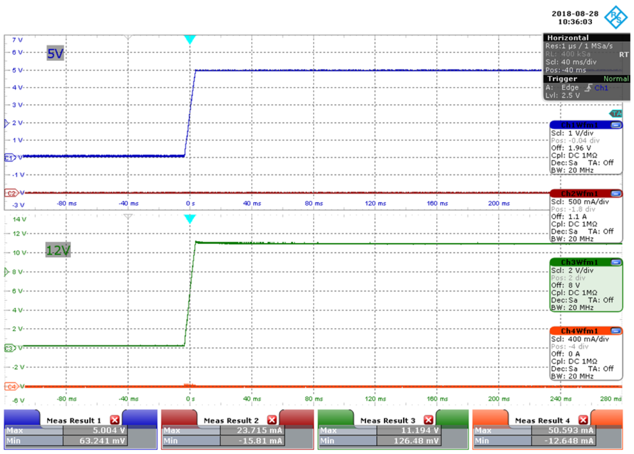


Figure 49 – 230 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

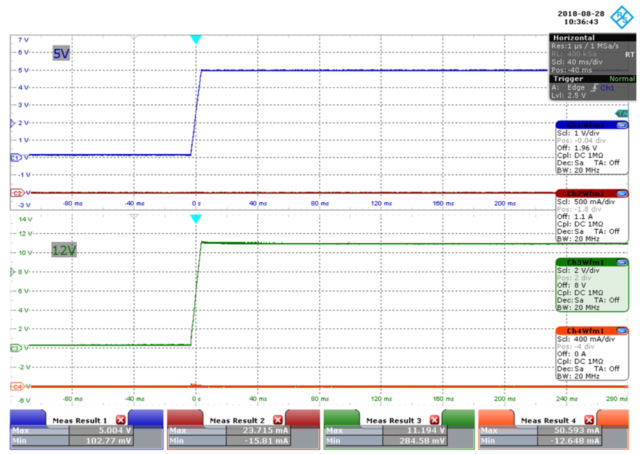


Figure 50 – 277 VAC 50 Hz, No-Load Start-up.
CH1: 5 V_{OUT}, 1 V / div., 40 ms / div.
CH2: 5 V I_{LOAD}, 500 mA / div., 40 ms / div.
CH3: 12 V_{OUT}, 2 V / div., 40 ms / div.
CH4: 12 V I_{LOAD}, 400 mA / div., 40 ms / div.

10.3 ***Switching Waveforms***

10.3.1 *Primary MOSFET Drain-Source Voltage and Current at Normal Operation*

10.3.1.1 100% Load

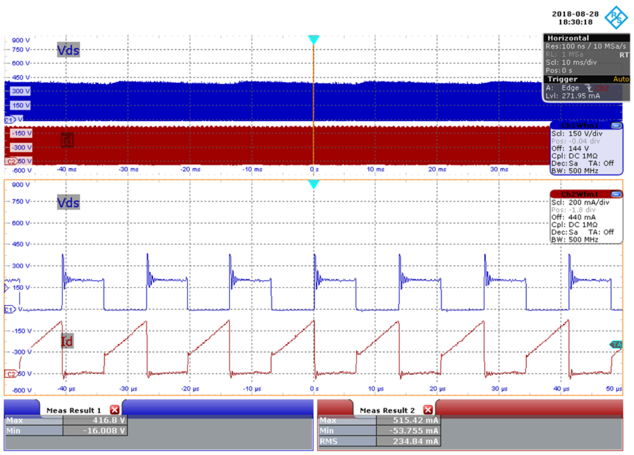


Figure 51 – 85 VAC 60 Hz, Full Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 416.8 V, $I_{DS(MAX)}$ = 515.42 mA.

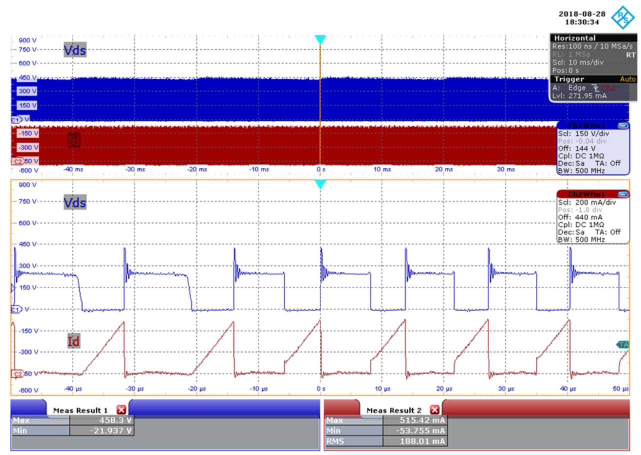


Figure 52 – 115 VAC 60 Hz, Full Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 458.3 V, $I_{DS(MAX)}$ = 515.42 mA.

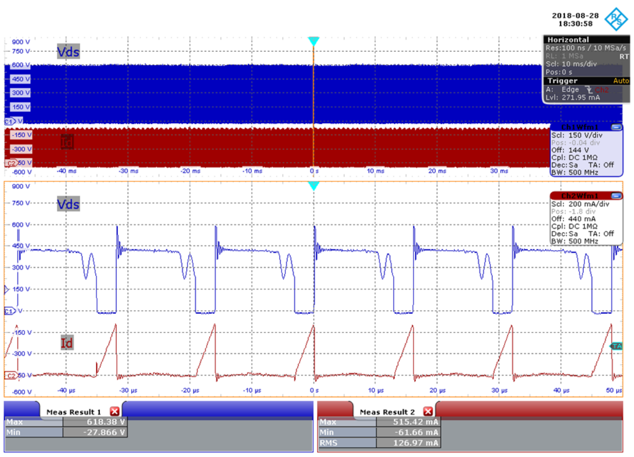


Figure 53 – 230 VAC 50 Hz, Full Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 618.38 V, $I_{DS(MAX)}$ = 515.42 mA.

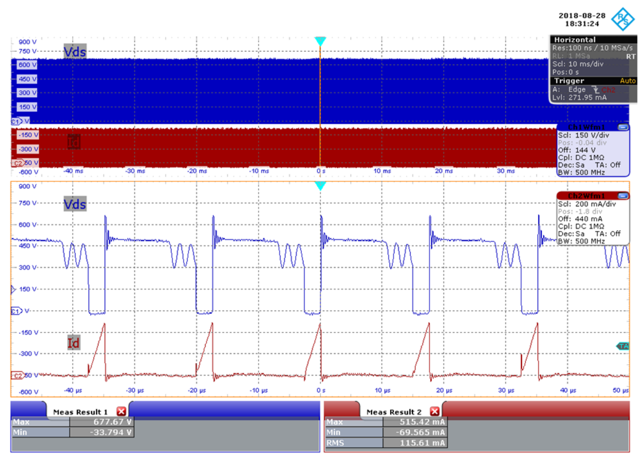


Figure 54 – 277 VAC 50 Hz, Full Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 677.67 V, $I_{DS(MAX)}$ = 515.42 mA.

10.3.1.2 0% Load

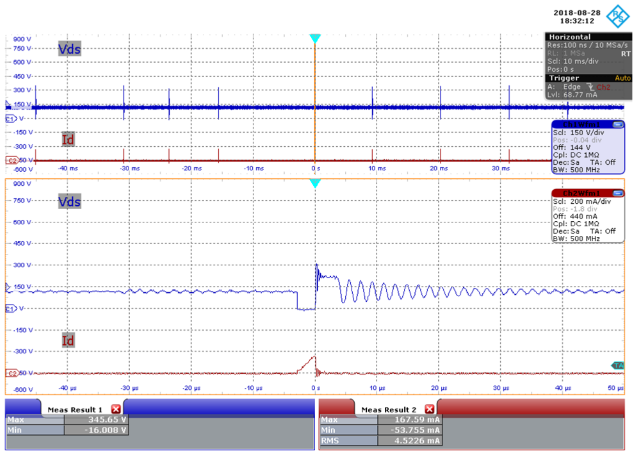


Figure 55 – 85 VAC 60 Hz, No-Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 345.65 V, $I_{DS(MAX)}$ = 167.59 mA.

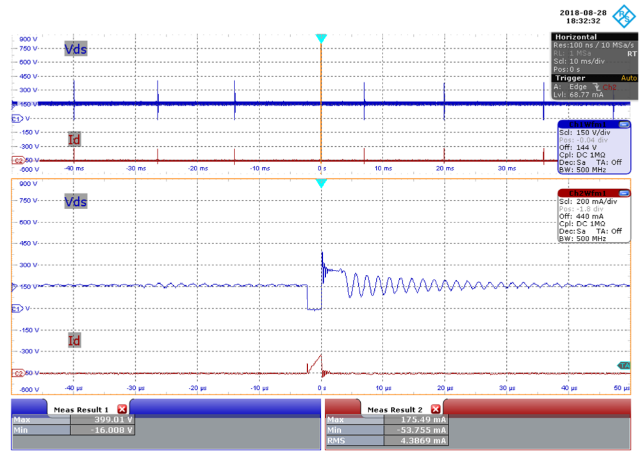


Figure 56 – 115 VAC 60 Hz, No-Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 399.01 V, $I_{DS(MAX)}$ = 175.49 mA.

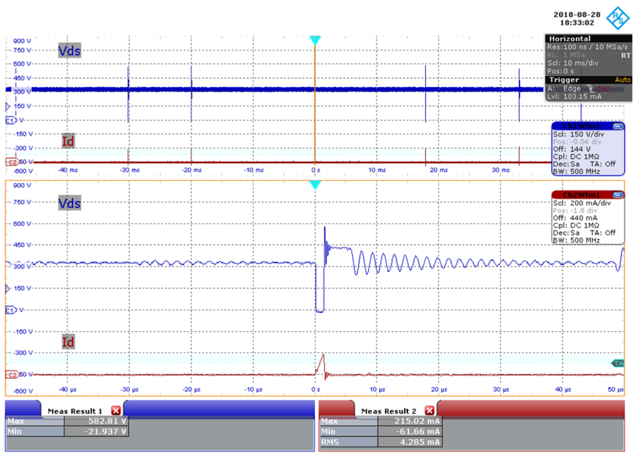


Figure 57 – 230 VAC 50 Hz, No-Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 582.81 V, $I_{DS(MAX)}$ = 215.02 mA.

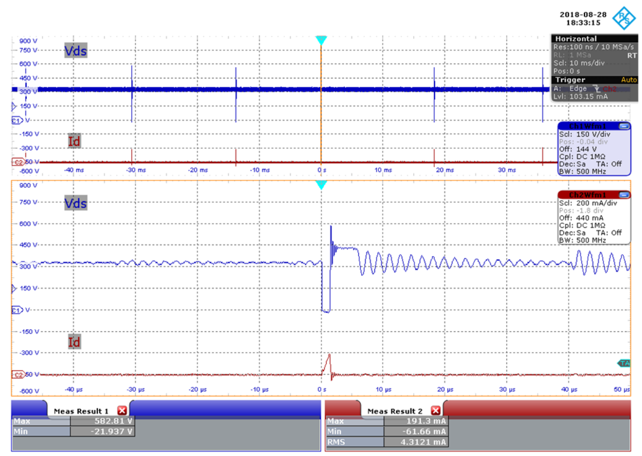


Figure 58 – 277 VAC 50 Hz, No-Load.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 10 µs / div.
$V_{DS(MAX)}$ = 582.81 V, $I_{DS(MAX)}$ = 191.3 mA.

10.3.2 *Primary MOSFET Drain-Source Voltage and Current at Start-up Operation*

10.3.2.1 100% Load

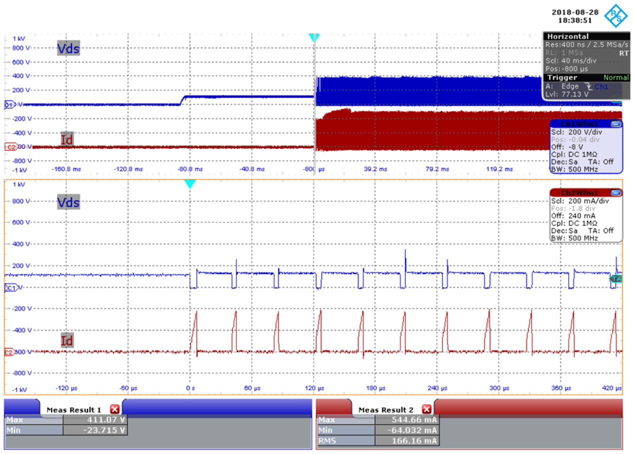


Figure 59 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 411.07 V, $I_{DS(MAX)}$ = 544.66 mA.

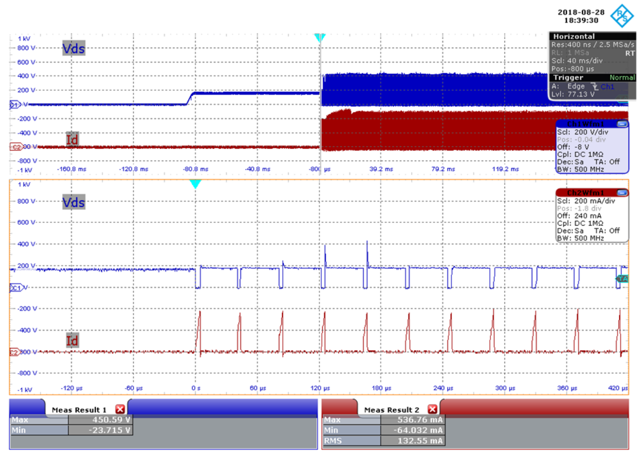


Figure 60 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 450.59 V, $I_{DS(MAX)}$ = 536.76 mA.

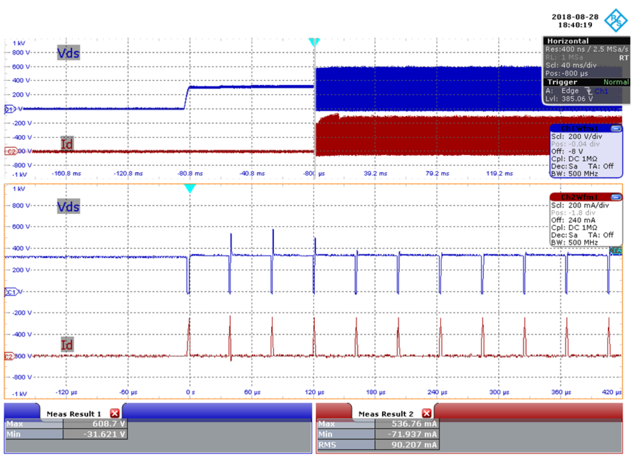


Figure 61 – 230 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 608.7 V, $I_{DS(MAX)}$ = 536.76 mA.

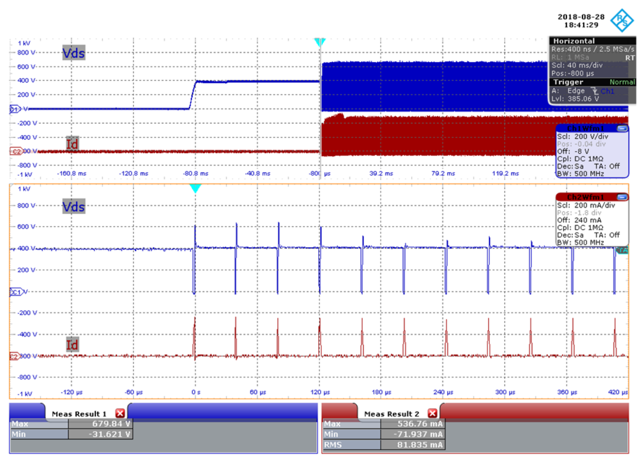


Figure 62 – 277 VAC 50 Hz, Full Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 679.84 V, $I_{DS(MAX)}$ = 536.76 mA.

10.3.2.2 0% Load

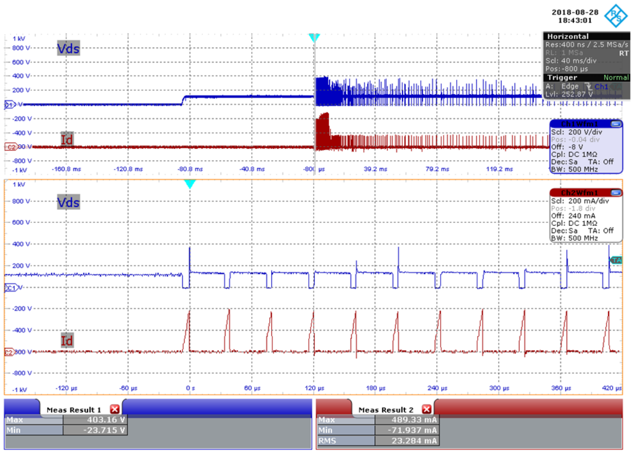


Figure 63 – 85 VAC 60 Hz, No-Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 403.16 V, $I_{DS(MAX)}$ = 489.33 mA.

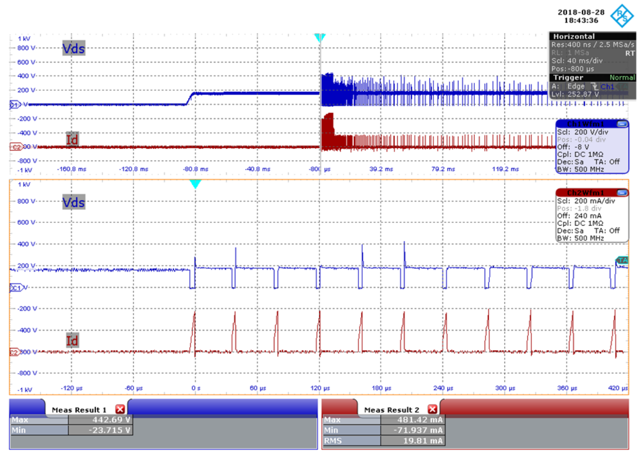


Figure 64 – 115 VAC 60 Hz, No-Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 442.69 V, $I_{DS(MAX)}$ = 481.42 mA.

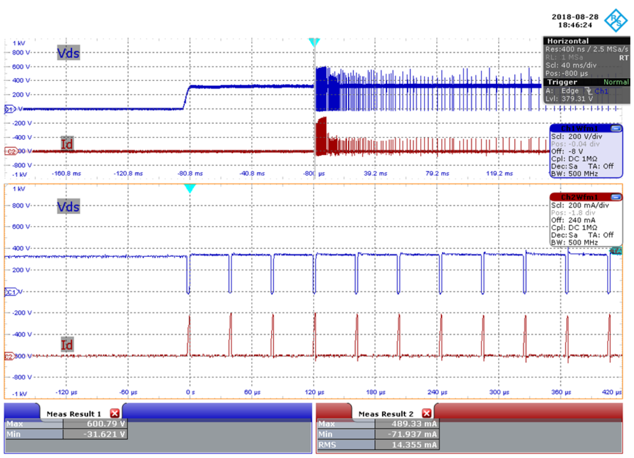


Figure 65 – 230 VAC 50 Hz, No-Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 600.79 V, $I_{DS(MAX)}$ = 489.33 mA.

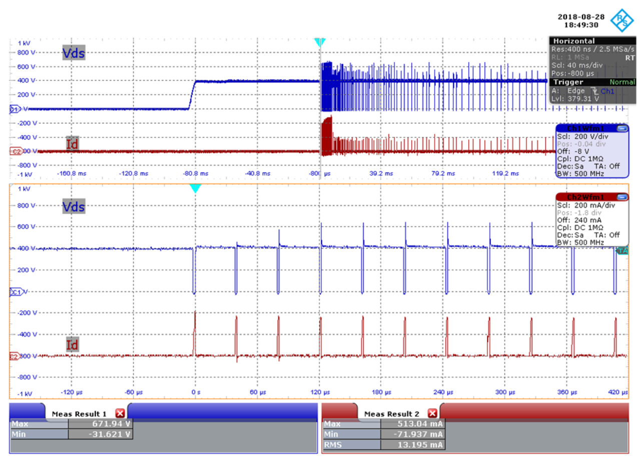


Figure 66 – 277 VAC 50 Hz, No-Load Start-up.
CH1: V_{DS}, 200 V / div., 40 ms / div.
CH2: I_{DS}, 200 mA / div., 40 ms / div.
Zoom: 60 µs / div.
$V_{DS(MAX)}$ = 671.94 V, $I_{DS(MAX)}$ = 513.04 mA.

10.3.3 *5 V Output Synchronous Rectifier Voltage at Normal Operation*

10.3.3.1 100% Load

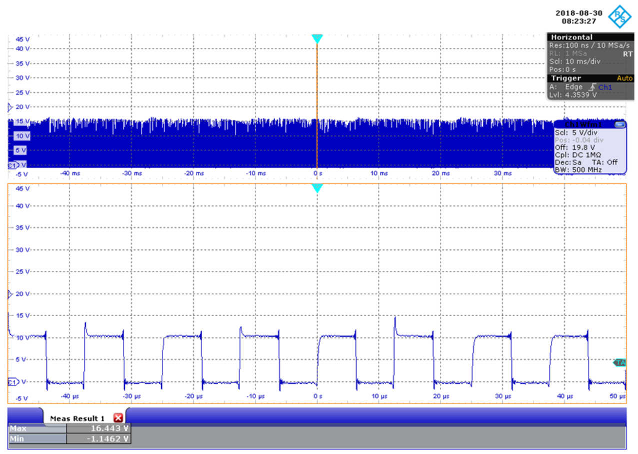


Figure 67 – 85 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 16.443 V.

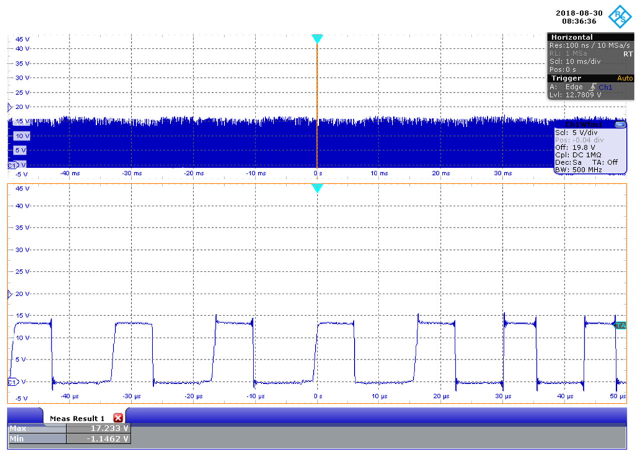


Figure 68 – 115 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 17.233 V.

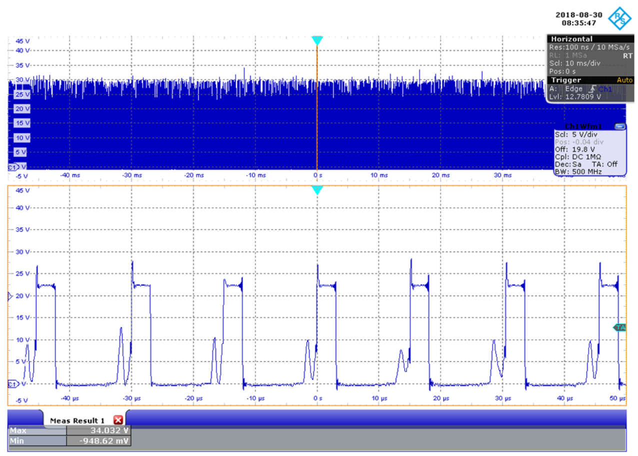


Figure 69 – 230 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 34.032 V.

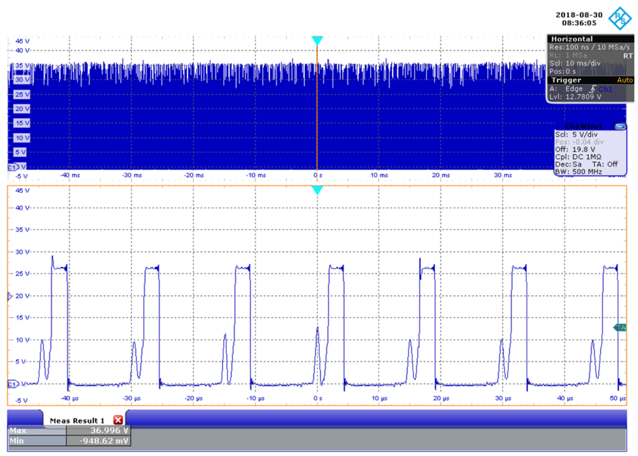


Figure 70 – 277 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 36.996 V.

10.3.3.2 0% Load

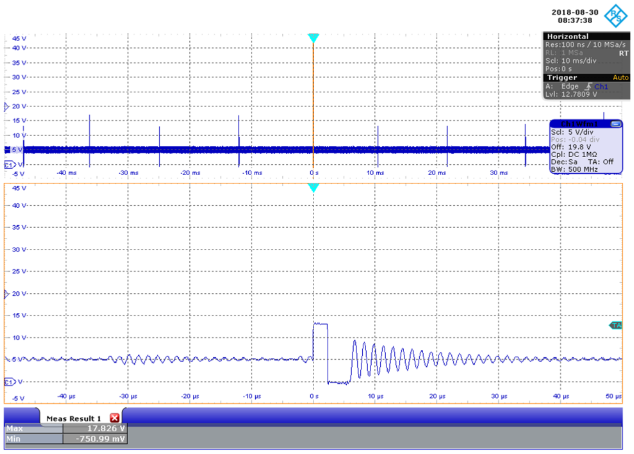


Figure 71 – 85 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 17.826 V.

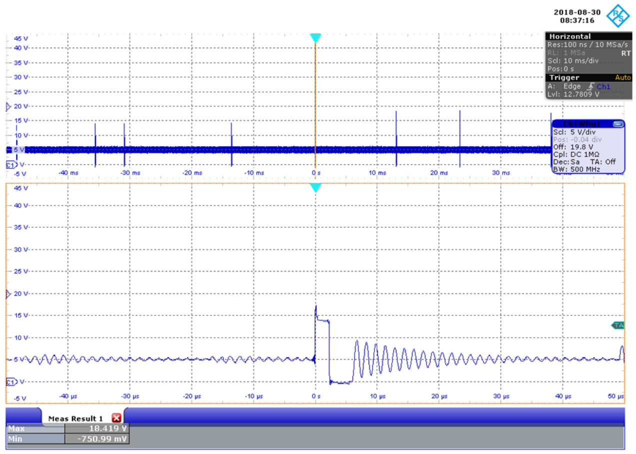


Figure 72 – 115 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div..
5 V PIV_{MAX} = 18.419 V

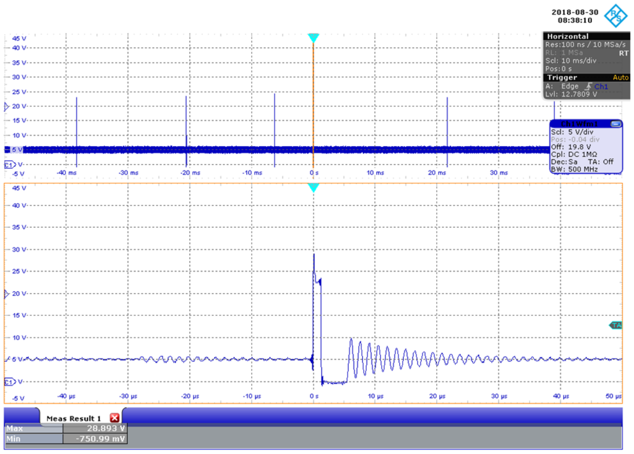


Figure 73 – 230 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 28.893 V.

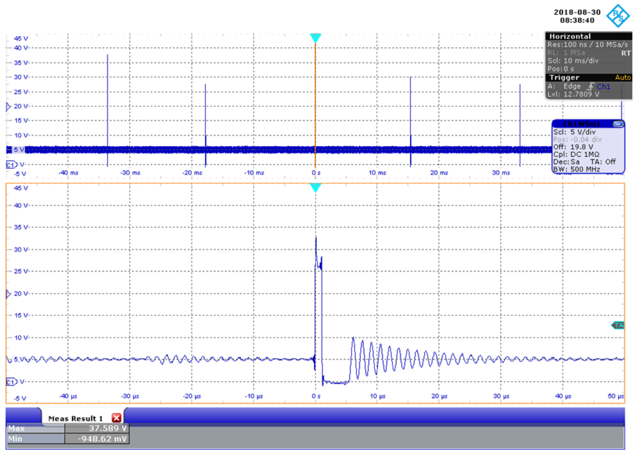


Figure 74 – 277 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 10 µs / div.
5 V PIV_{MAX} = 37.589 V.

10.3.4 *5 V Output Synchronous Rectifier Voltage at Start-up Operation*

10.3.4.1 100% Load

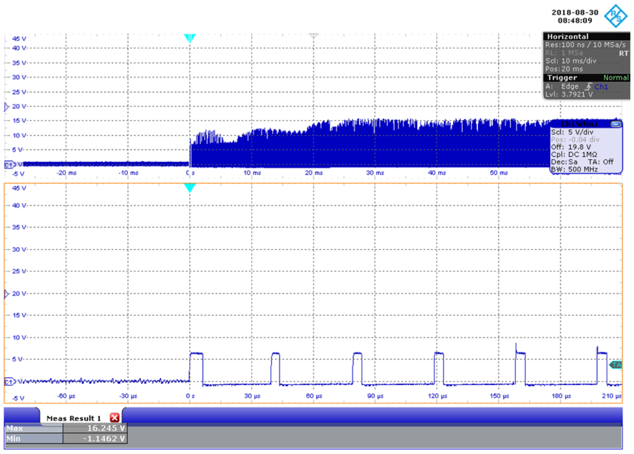


Figure 75 – 85 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 16.245 V.

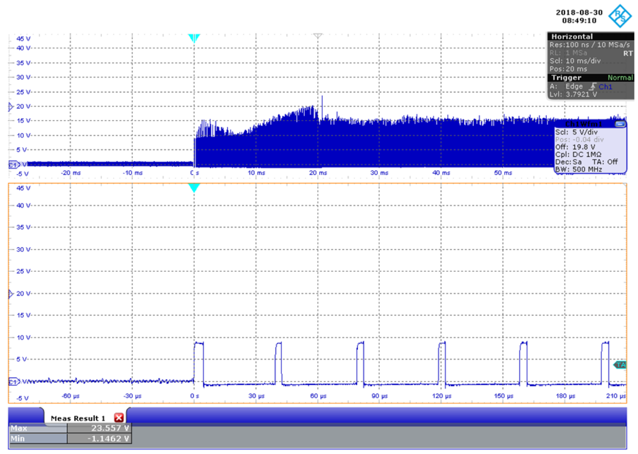


Figure 76 – 115 VAC 60 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 23.557 V.

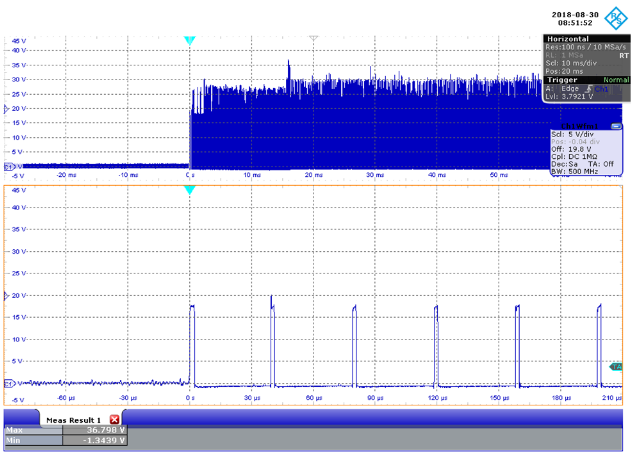


Figure 77 – 230 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 36.798 V.

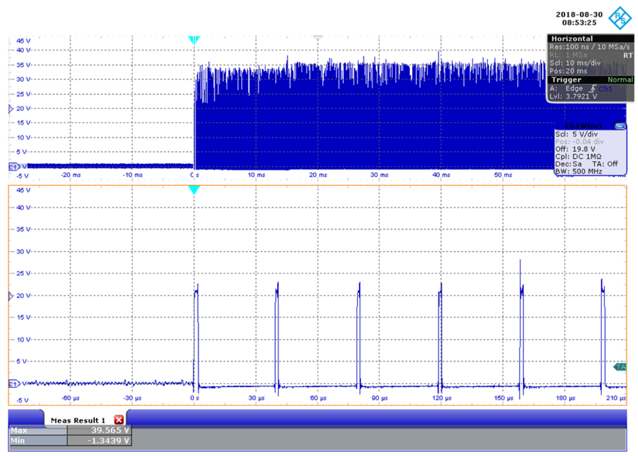


Figure 78 – 277 VAC 50 Hz, Full Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 μs / div.
5 V PIV_{MAX} = 39.565 V.

10.3.4.2 0% Load

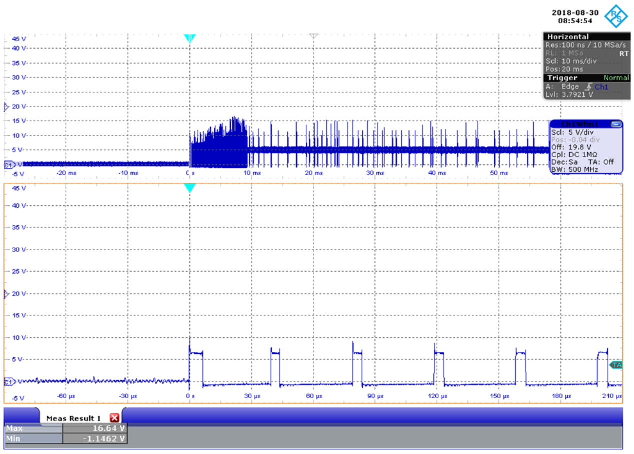


Figure 79 – 85 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 µs / div.
5 V PIV_{MAX} = 16.64 V.

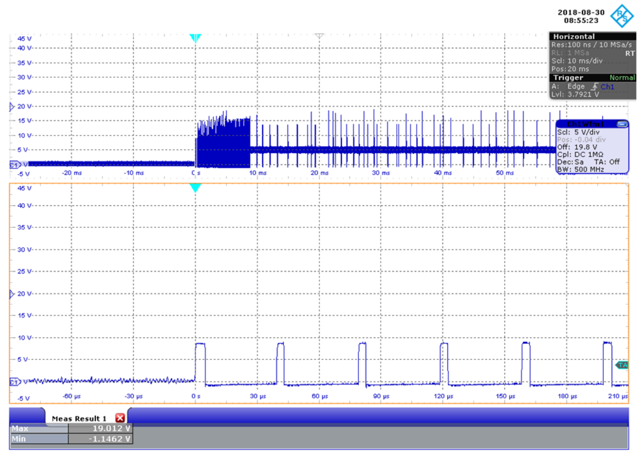


Figure 80 – 115 VAC 60 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 µs / div.
5 V PIV_{MAX} = 19.012 V.

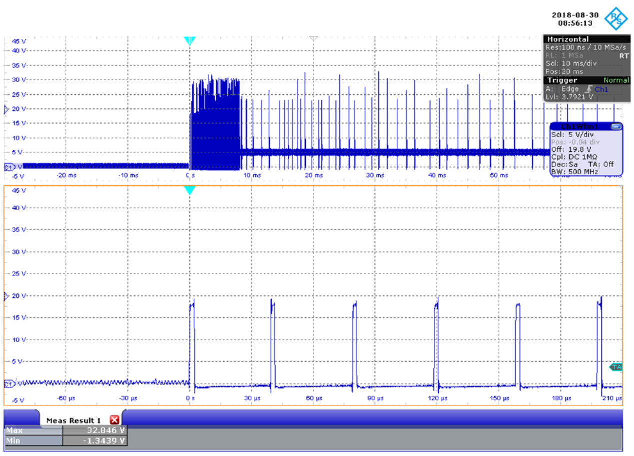


Figure 81 – 230 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 µs / div.
5 V PIV_{MAX} = 32.846 V.

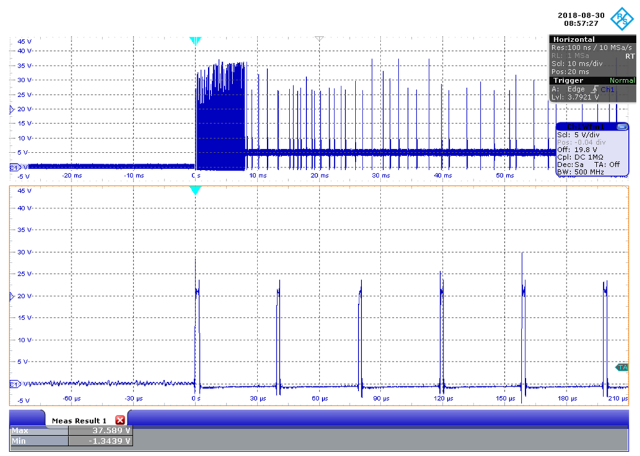


Figure 82 – 277 VAC 50 Hz, No-Load.
CH1: 5 V_{FWL_DIODE}, 5 V / div., 10 ms / div.
Zoom: 30 µs / div.
5 V PIV_{MAX} = 37.589 V.

10.3.5 *12 V Output Diode Voltage at Normal Operation*

10.3.5.1 100% Load

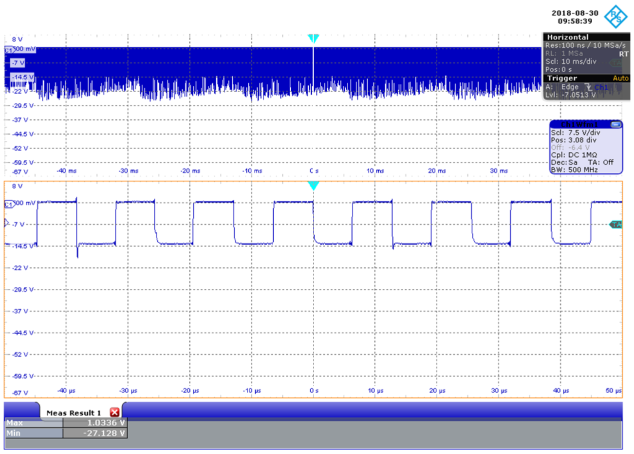


Figure 83 – 85 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 27.128 V.

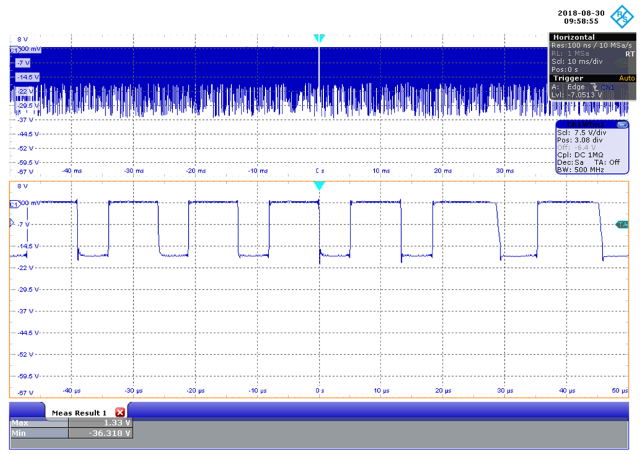


Figure 84 – 115 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 36.318 V.

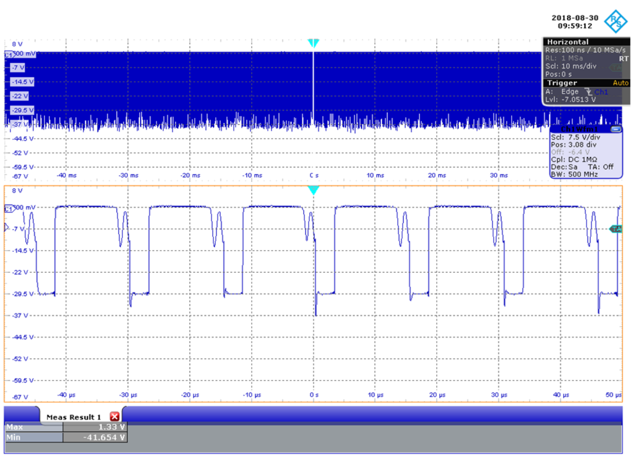


Figure 85 – 230 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 41.654 V.

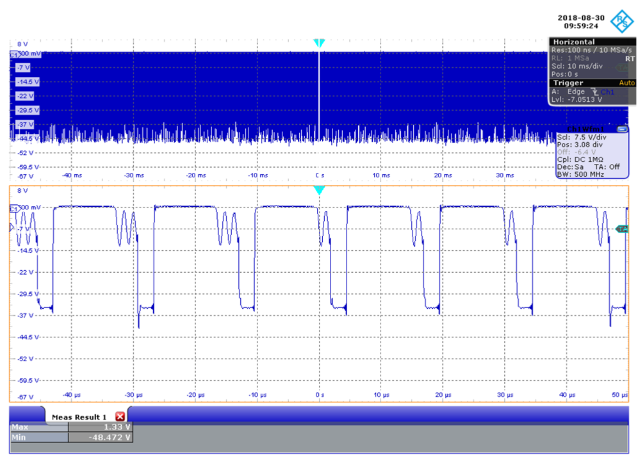


Figure 86 – 277 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 48.472 V.

10.3.5.2 0% Load

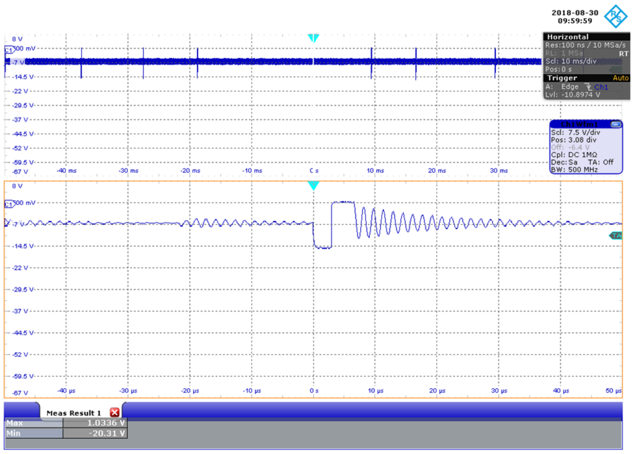


Figure 87 – 85 VAC 60 Hz, No-Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 20.31 V.

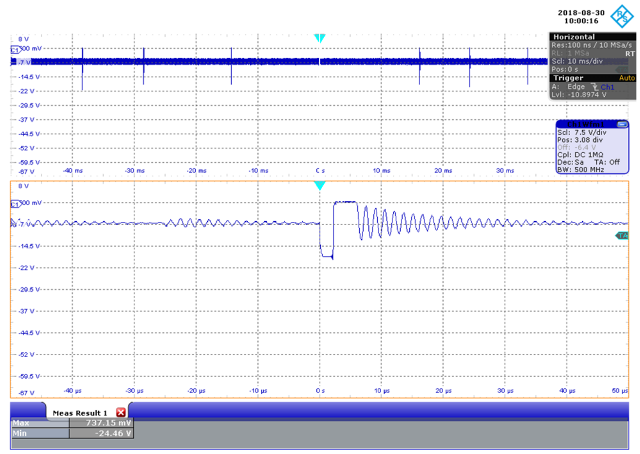


Figure 88 – 115 VAC 60 Hz, No-Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 24.46 V.

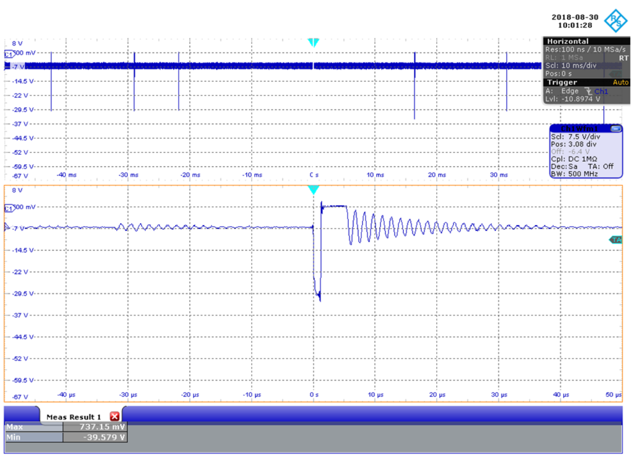


Figure 89 – 230 VAC 50 Hz, No-Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 39.579 V.

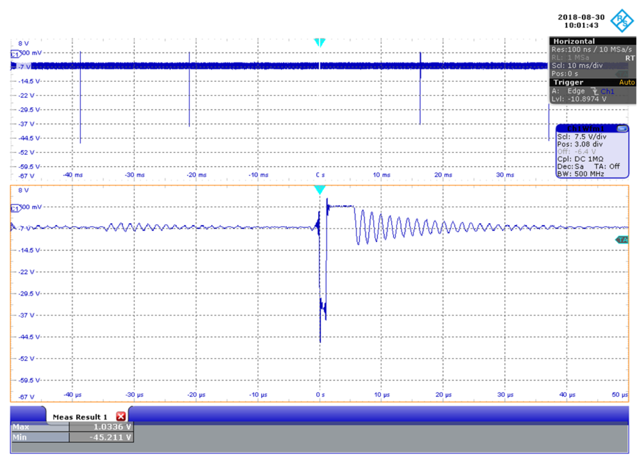


Figure 90 – 277 VAC 50 Hz, No-Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 10 μs / div.
12 V PIV_{MAX} = 45.211 V.

10.3.6 *12 V Output Diode Voltage at Start-up Operation*

10.3.6.1 100% Load

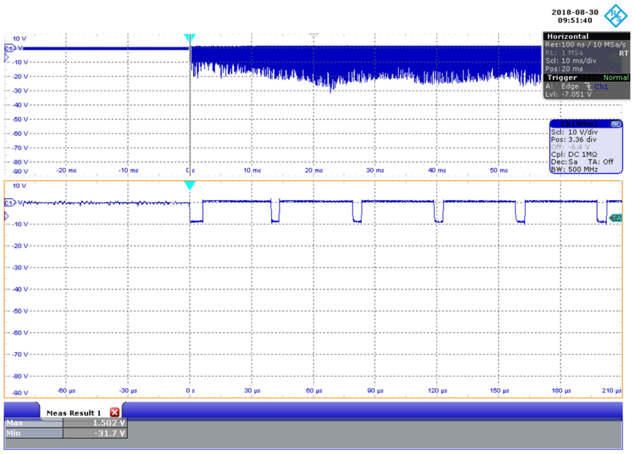


Figure 91 – 85 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 31.7 V.

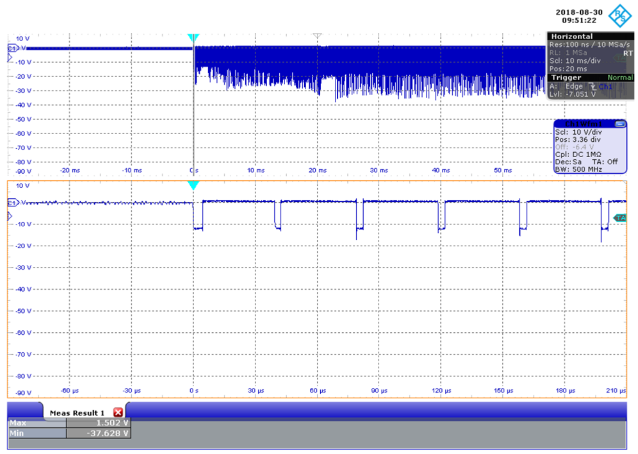


Figure 92 – 115 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 37.628 V.

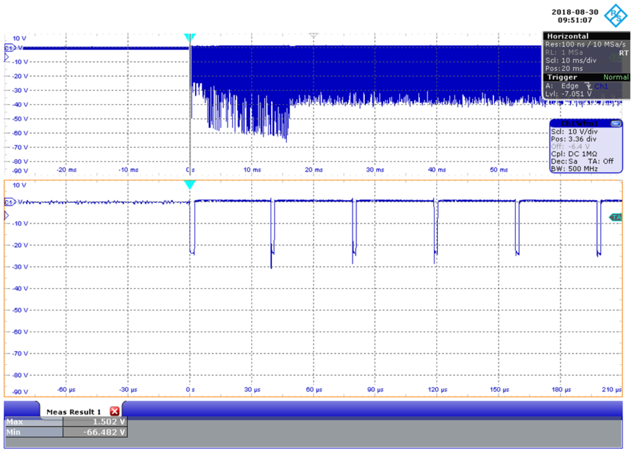


Figure 93 – 230 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 66.482 V.

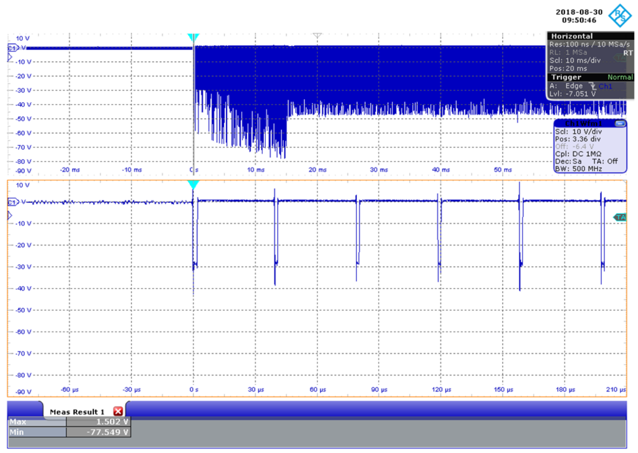


Figure 94 – 277 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 77.549 V.

10.3.6.2 0% Load

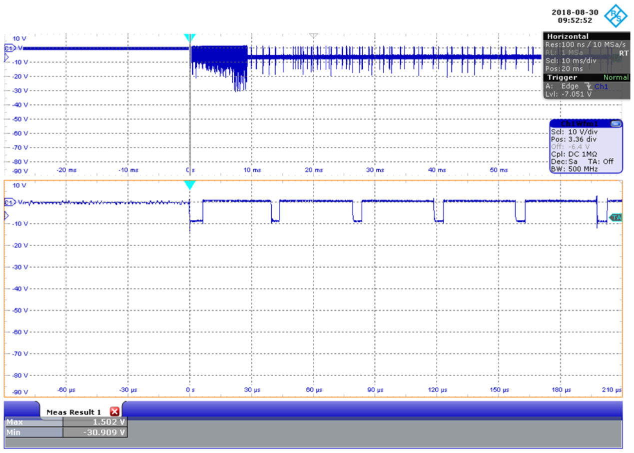


Figure 95 – 85 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE},7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 30.909 V.

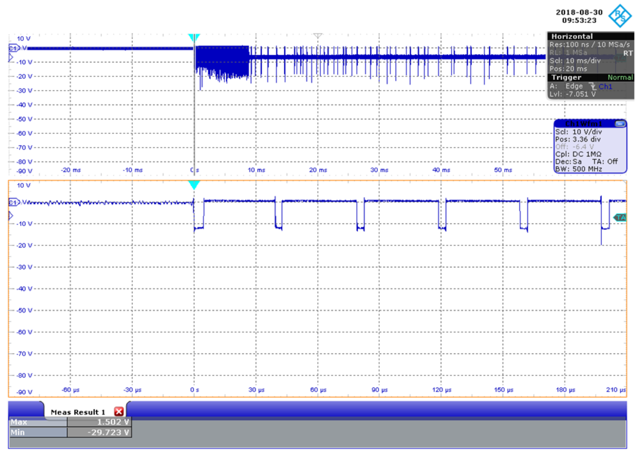


Figure 96 – 115 VAC 60 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 29.723 V.

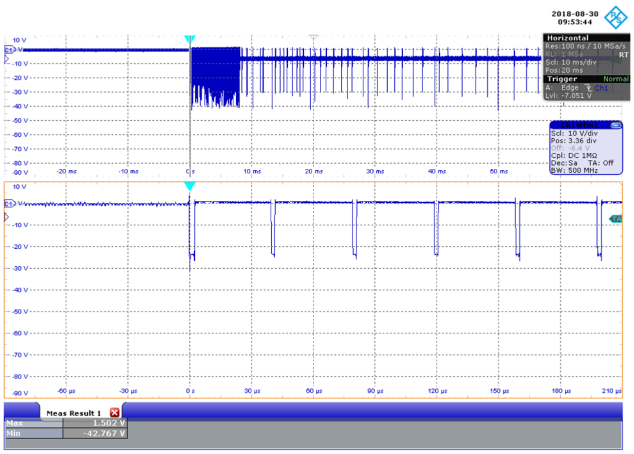


Figure 97 – 230 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 42.767 V.

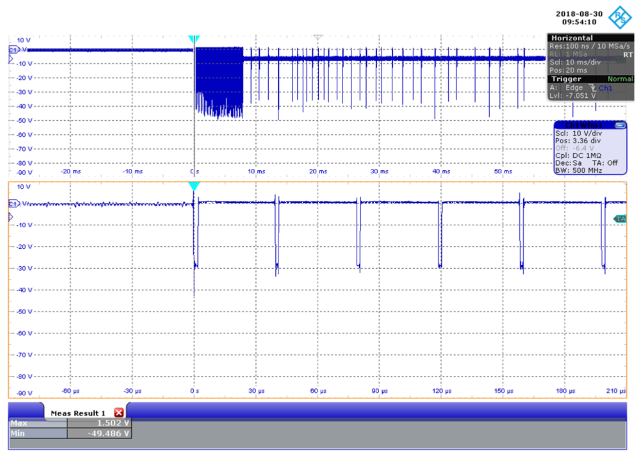


Figure 98 – 277 VAC 50 Hz, Full Load.
CH1: 12 V_{FWL_DIODE}, 7.5 V / div., 10 ms / div.
Zoom: 30 µs / div.
12 V PIV_{MAX} = 49.486 V.

10.4 *Brown-in / Brown-out Test*

No abnormal overheating or voltage overshoot / undershoot was observed during and after 0.1 V / s brown-in and brown-out test.

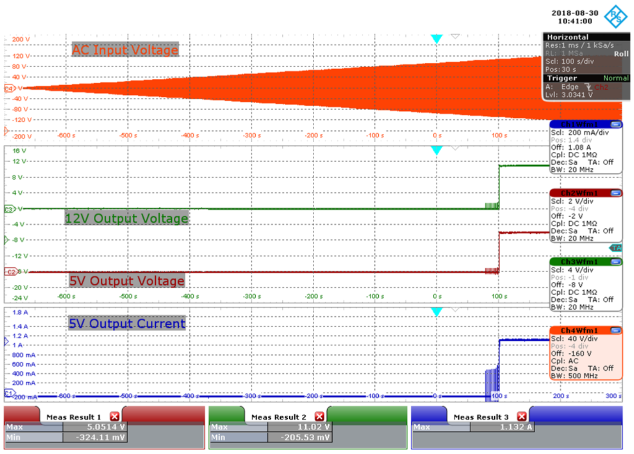


Figure 99 – Brown-in Test.
0 to 85 VAC 0.1 V / s.
CH1: 5 V I_{OUT}, 200 mA / div., 100 s /div.
CH2: 5 V_{OUT}, 2 V / div., 100 s / div.
CH3: 12 V_{OUT}, 4 V / div., 100 s / div.
CH4: AC_{IN}, 40 V / div., 100 s / div.
Highest Average Input Power: 17.24 W at 75.188 VAC.

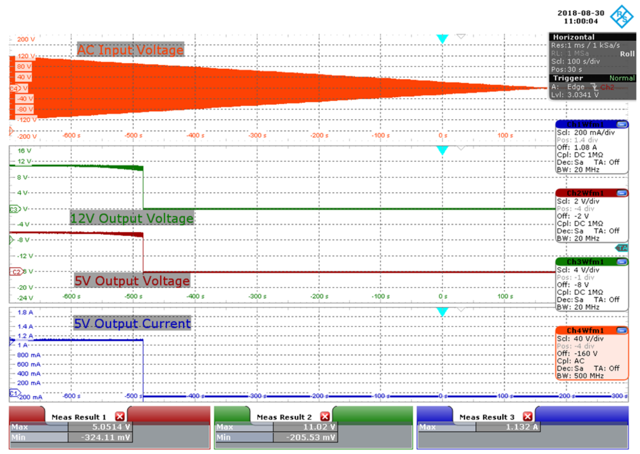


Figure 100 – Brown-out Test.
85 to 0 VAC 0.1 V / s.
CH1: 5 V I_{OUT}, 200 mA / div., 100 s /div.
CH2: 5 V_{OUT}, 2 V / div., 100 s / div.
CH3: 12 V_{OUT}, 4 V / div., 100 s / div.
CH4: AC_{IN}, 40 V / div., 100 s / div.
Highest Average Input Power: 17.84 W at 63.43 VAC.

10.5 ***Fault Conditions***

10.5.1 *Output Short-Circuit*

Test Condition: 5 V and 12 V output are shorted at the end of the cable.

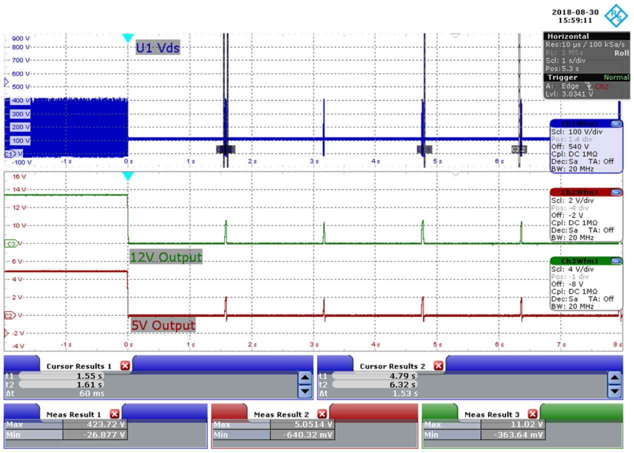


Figure 101 – 85 VAC, Short-Circuit during Normal Running Operation.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
$t_{AR(ON)}$: 60 ms.
$t_{AR(OFF)}$: 1.53 s.

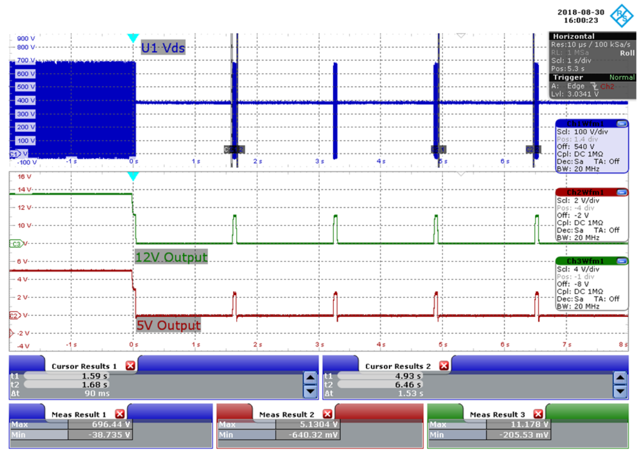


Figure 102 – 277 VAC, Short-Circuit during Normal Running Operation.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
$t_{AR(ON)}$: 90 ms.
$t_{AR(OFF)}$: 1.53 s.

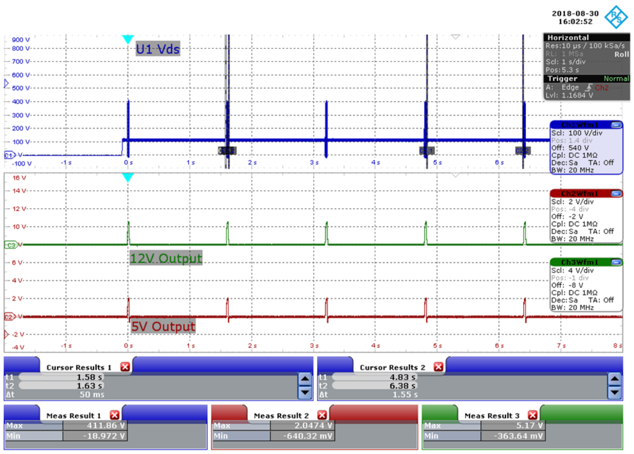


Figure 103 – 85 VAC, Short-Circuit during Start-up.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
$t_{AR(ON)}$: 50 ms.
$t_{AR(OFF)}$: 1.55 s.

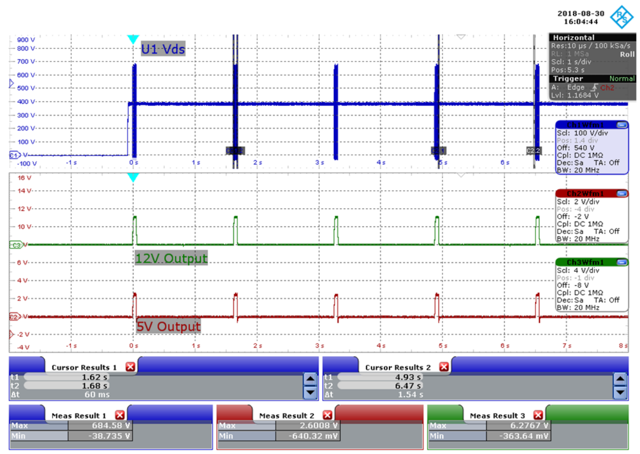


Figure 104 – 277 VAC, Short-Circuit during Start-up.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
$t_{AR(ON)}$: 60 ms.
$t_{AR(OFF)}$: 1.54 s.

10.5.2 *Line Overvoltage*

Test Condition: Line Overvoltage Protection set to 290 VAC

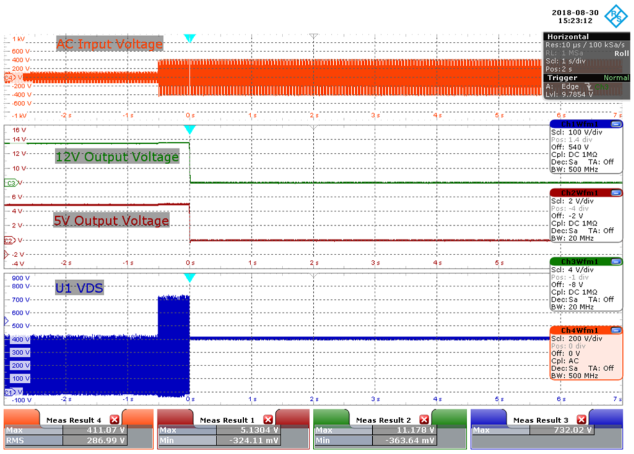


Figure 105 – Line Overvoltage during Normal Running Operation from 85 VAC.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s / div.

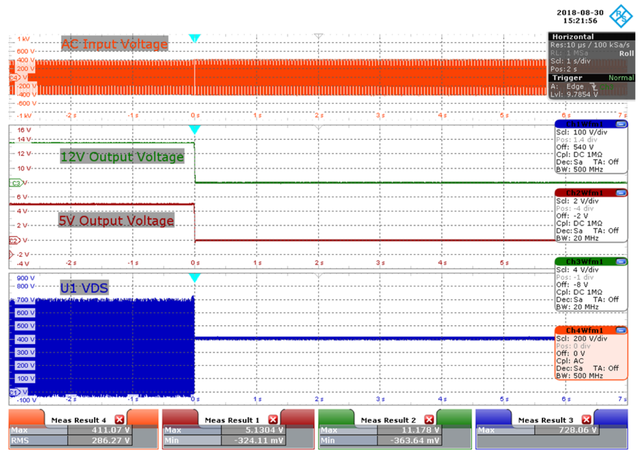


Figure 106 – Line Overvoltage during Normal Running Operation from 277 VAC.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s / div.

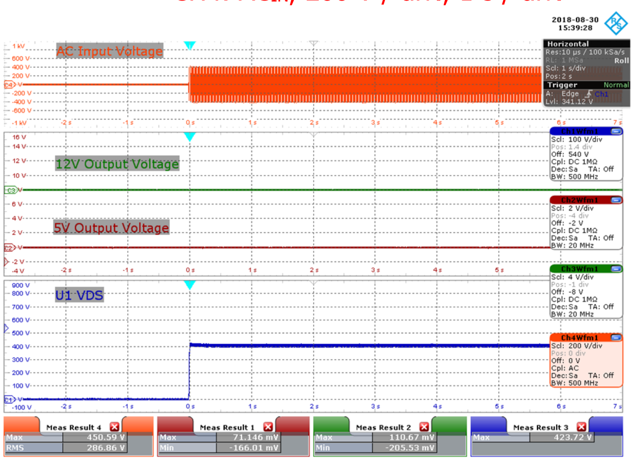


Figure 107 – Lined Overvoltage during Start-up.
CH1: U1 V_{DS}, 100 V / div., 1 s / div.
CH2: 5 V_{OUT}, 2 V / div., 1 s / div.
CH3: 12 V_{OUT}, 4 V / div., 1 s / div.
CH4: AC_{IN}, 200 V / div., 1 s / div.

10.6 ***Output Ripple Measurements***

10.6.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

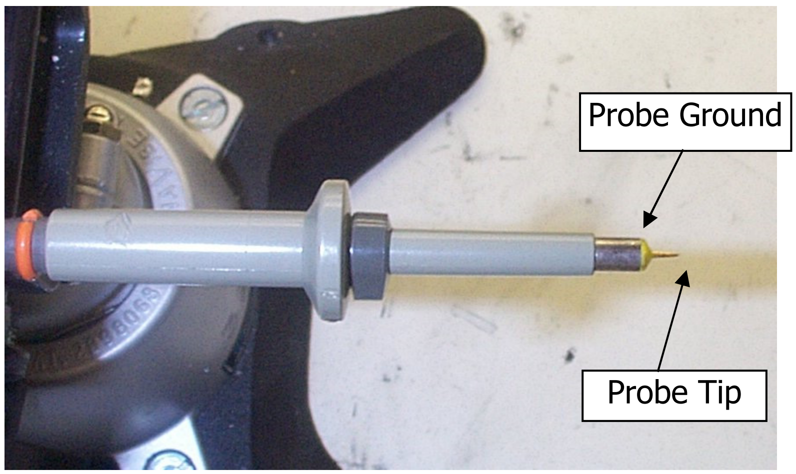


Figure 108 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

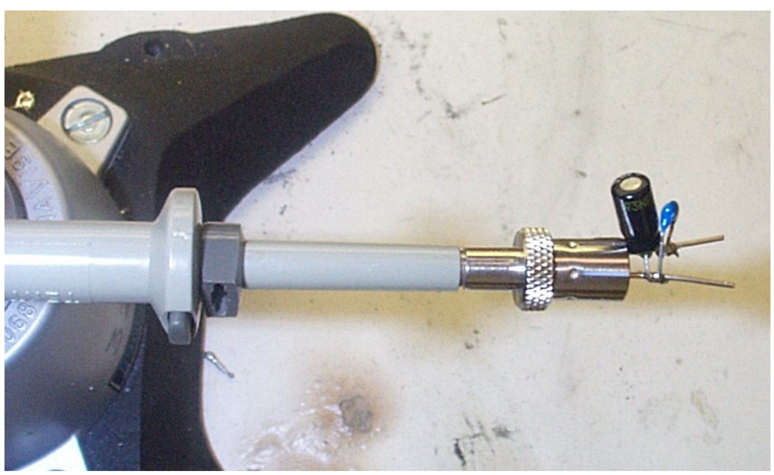


Figure 109 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.6.2 *Measurement Results*

Test Condition: Room Temperature, measured across the PCB connector

10.6.2.1 100% Load Condition

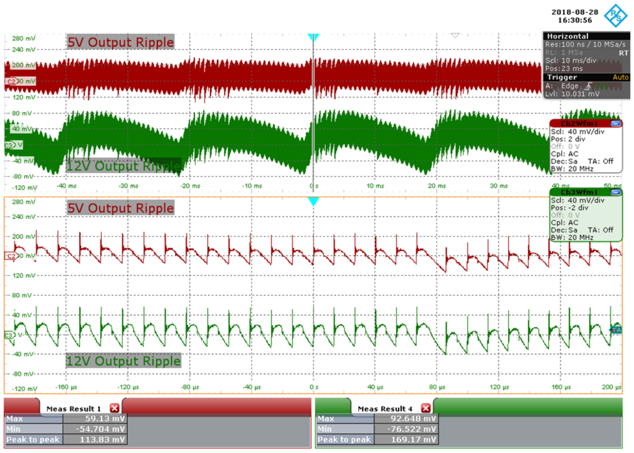


Figure 110 – 85 VAC 60 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 113.83 mV.
12 V Output Ripple = 169.17 mV.

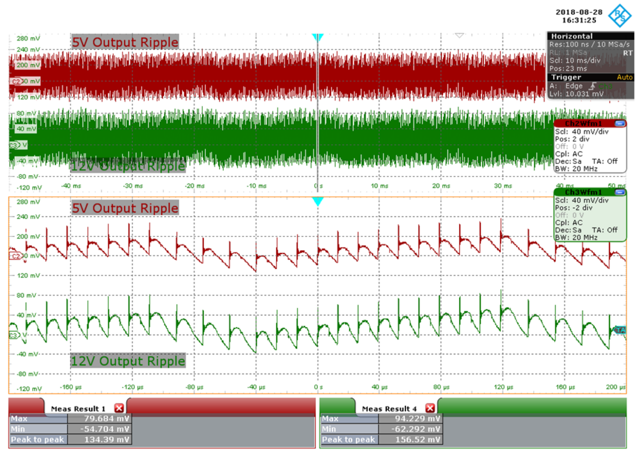


Figure 111 – 115 VAC 60 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 134.39 mV.
12 V Output Ripple = 156.62 mV.

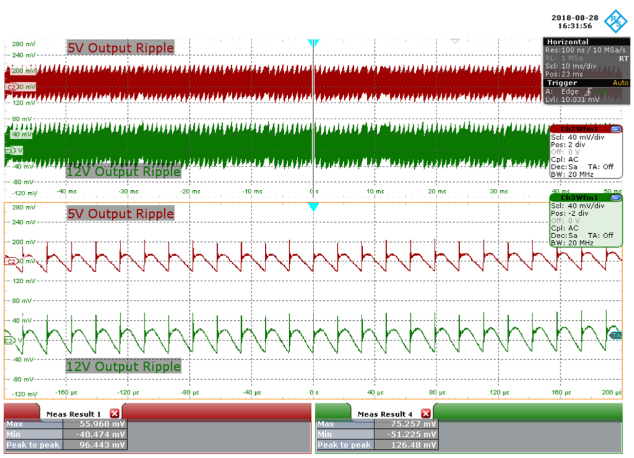


Figure 112 – 230 VAC 50 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 96.443 mV.
12 V Output Ripple = 128.48 mV.

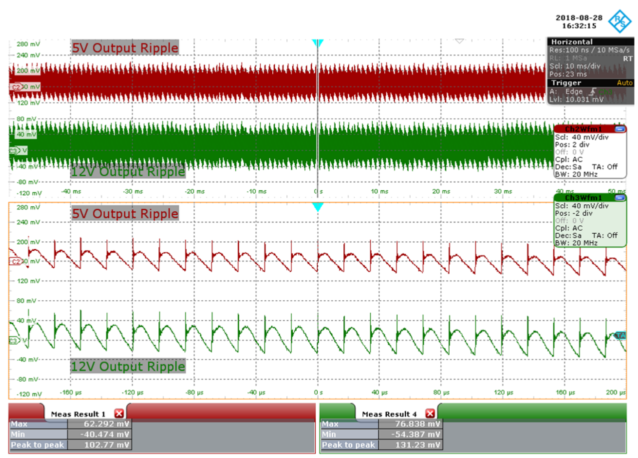


Figure 113 – 277 VAC 50 Hz, 100% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 102.77 mV.
12 V Output Ripple = 131.23 mV.

10.6.2.2 75% Load Condition

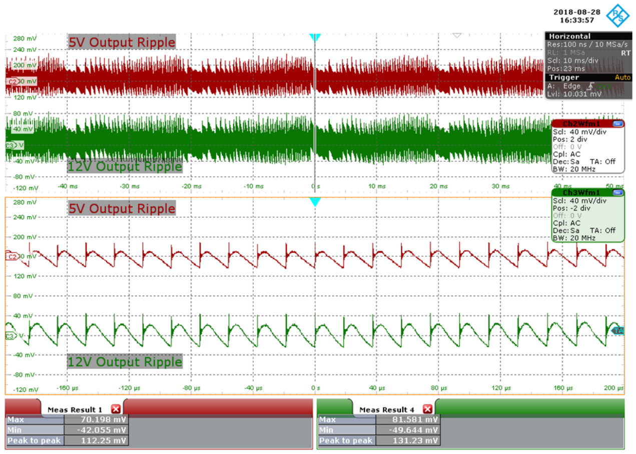


Figure 114 – 85 VAC 60 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 112.25 mV.
12 V Output Ripple = 131.23 mV.

Figure 115 – 115 VAC 60 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 85.375 mV.
12 V Output Ripple = 110.67 mV.

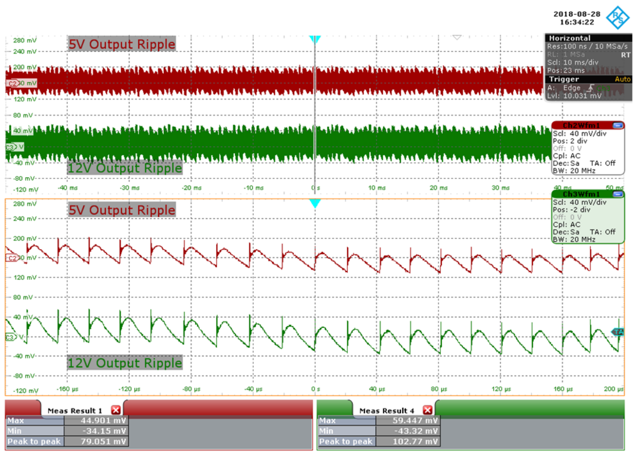


Figure 116 – 230 VAC 50 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 79.051 mV.
12 V Output Ripple = 102.77 mV.

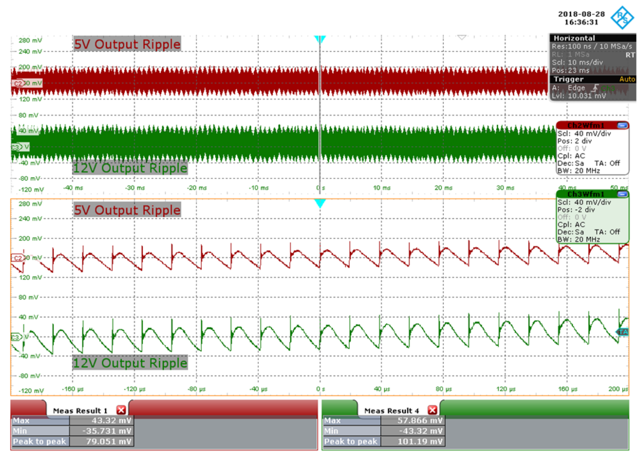


Figure 117 – 277 VAC 50 Hz, 75% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 79.051 mV.
12 V Output Ripple = 101.19 mV.

10.6.2.3 50% Load Condition

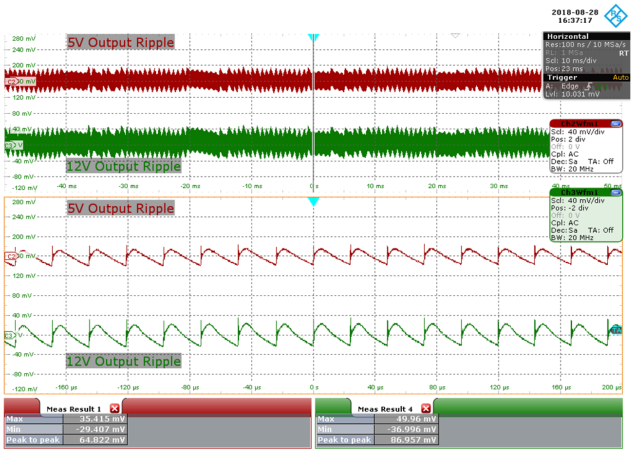


Figure 118 – 85 VAC 60 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 64.822 mV.
12 V Output Ripple = 86.957 mV.

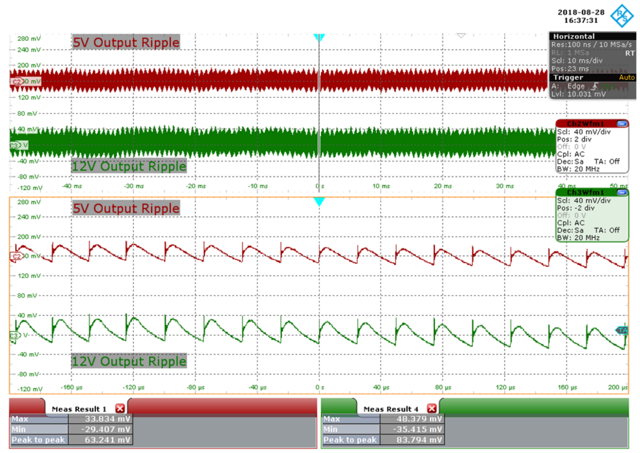


Figure 119 – 115 VAC 60 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 63.241 mV.
12 V Output Ripple = 83.794 mV.

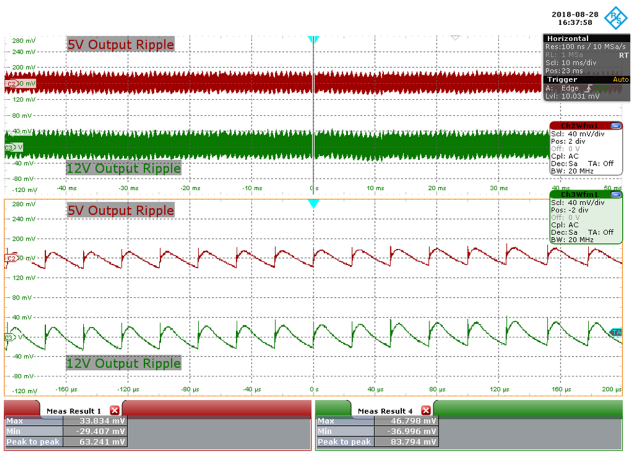


Figure 120 – 230 VAC 50 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 63.241 mV.
12 V Output Ripple = 83.794 mV.

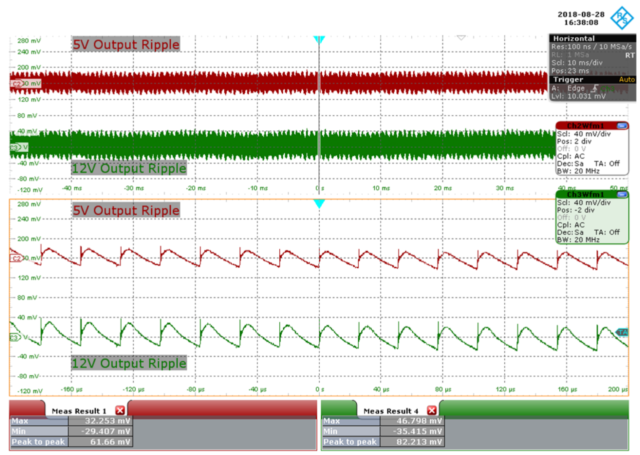


Figure 121 – 277 VAC 50 Hz, 50% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 61.66 mV.
12 V Output Ripple = 82.213 mV.

10.6.2.4 25% Load Condition

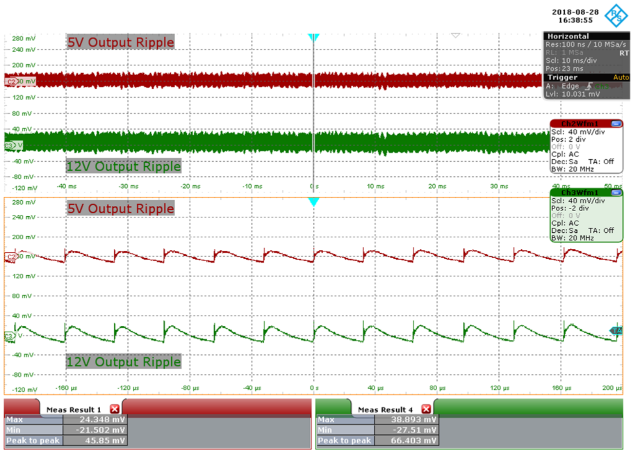


Figure 122 – 85 VAC 60 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 45.85 mV.
12 V Output Ripple = 66.403 mV.

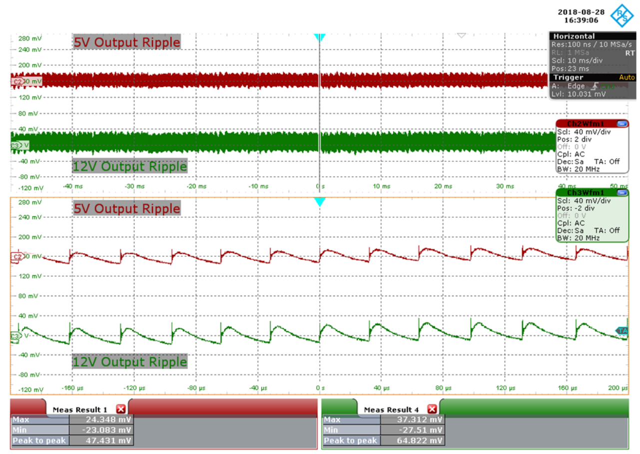


Figure 123 – 115 VAC 60 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 47.431 mV.
12 V Output Ripple = 64.622 mV.

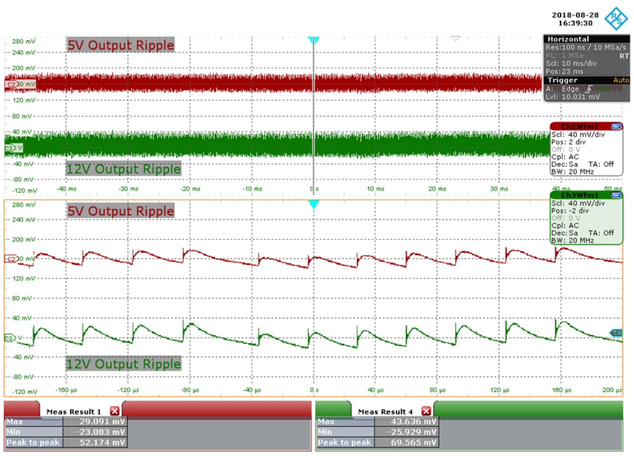


Figure 124 – 230 VAC 50 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 52.174 mV.
12 V Output Ripple = 69.565 mV.

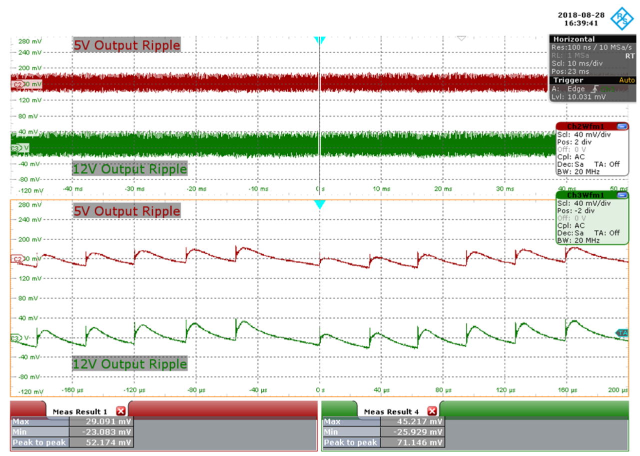


Figure 125 – 277 VAC 50 Hz, 25% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 µs / div.
5 V Output Ripple = 52.174 mV.
12 V Output Ripple = 71.146 mV.

10.6.2.5 0% Load Condition

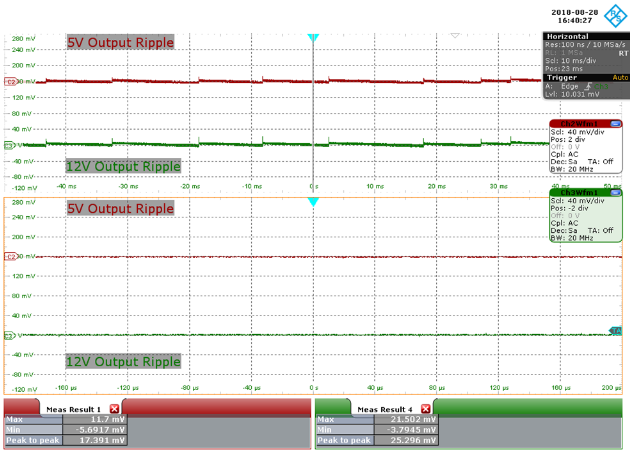


Figure 126 – 85 VAC 60 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 17.391 mV.
12 V Output Ripple = 25.296 mV.

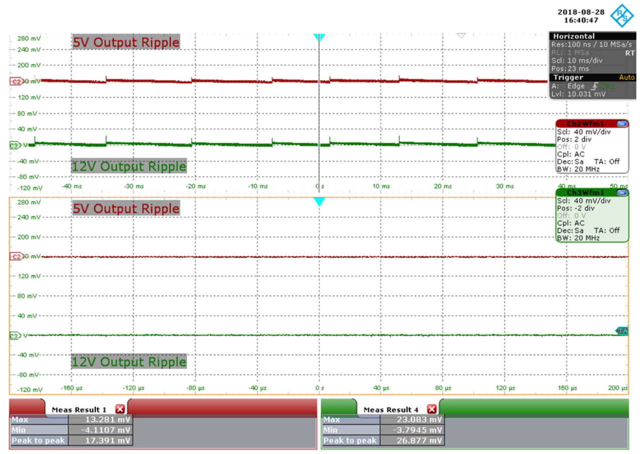


Figure 127 – 115 VAC 60 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 17.391 mV.
12 V Output Ripple = 26.877 mV.

Figure 128 – 230 VAC 50 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40 mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 20.553 mV.
12 V Output Ripple = 30.04 mV.

Figure 129 – 277 VAC 50 Hz, 0% Load.
CH2: 5 V_{OUT}, 40 mV / div., 10 ms / div.
CH3: 12 V_{OUT}, 40mV / div., 10 ms / div.
Zoom: 40 μs / div.
5 V Output Ripple = 18.972 mV.
12 V Output Ripple = 30.04 mV.

10.6.3 *Ripple at Hot and Cold Temperatures*

10.6.3.1 85 VAC, 60 Hz

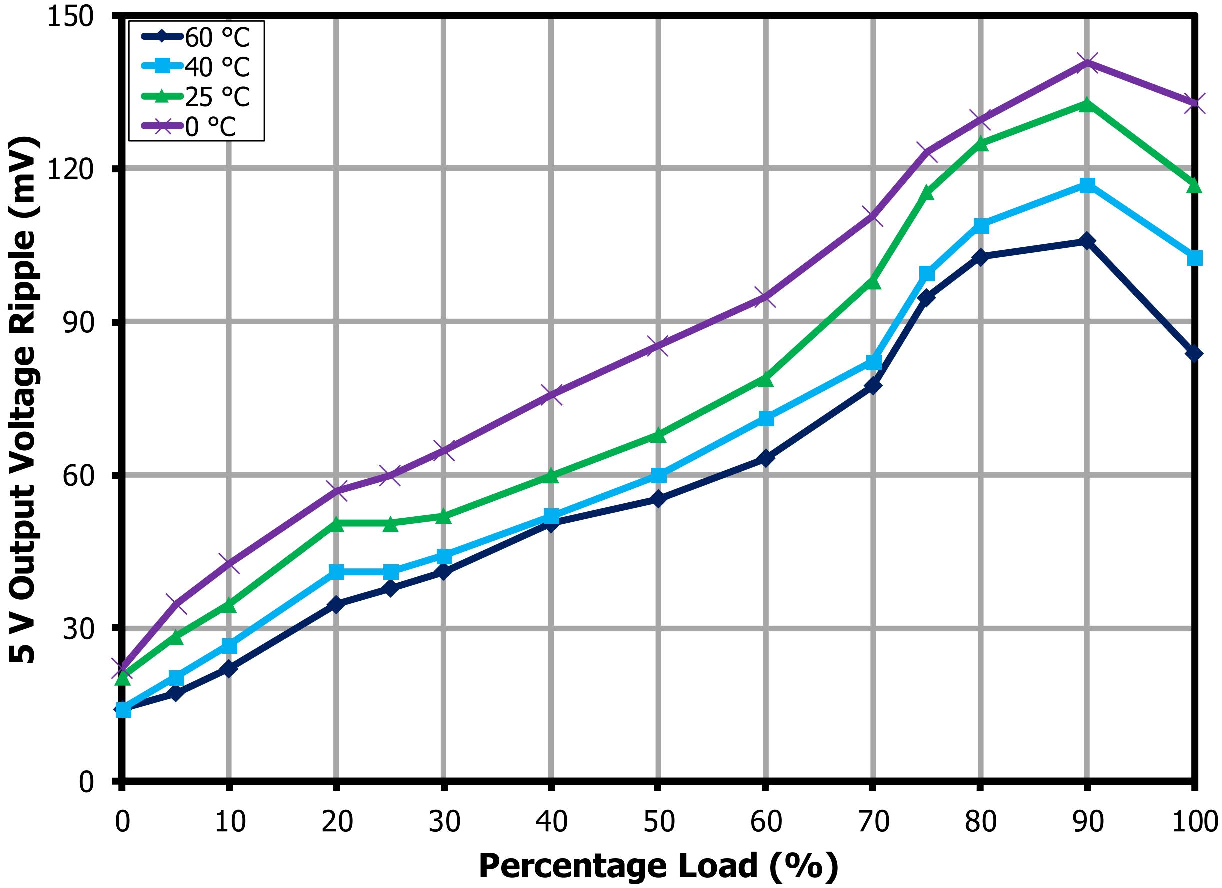


Figure 130 – 5 V Output Ripple at 85 VAC, 60 Hz.

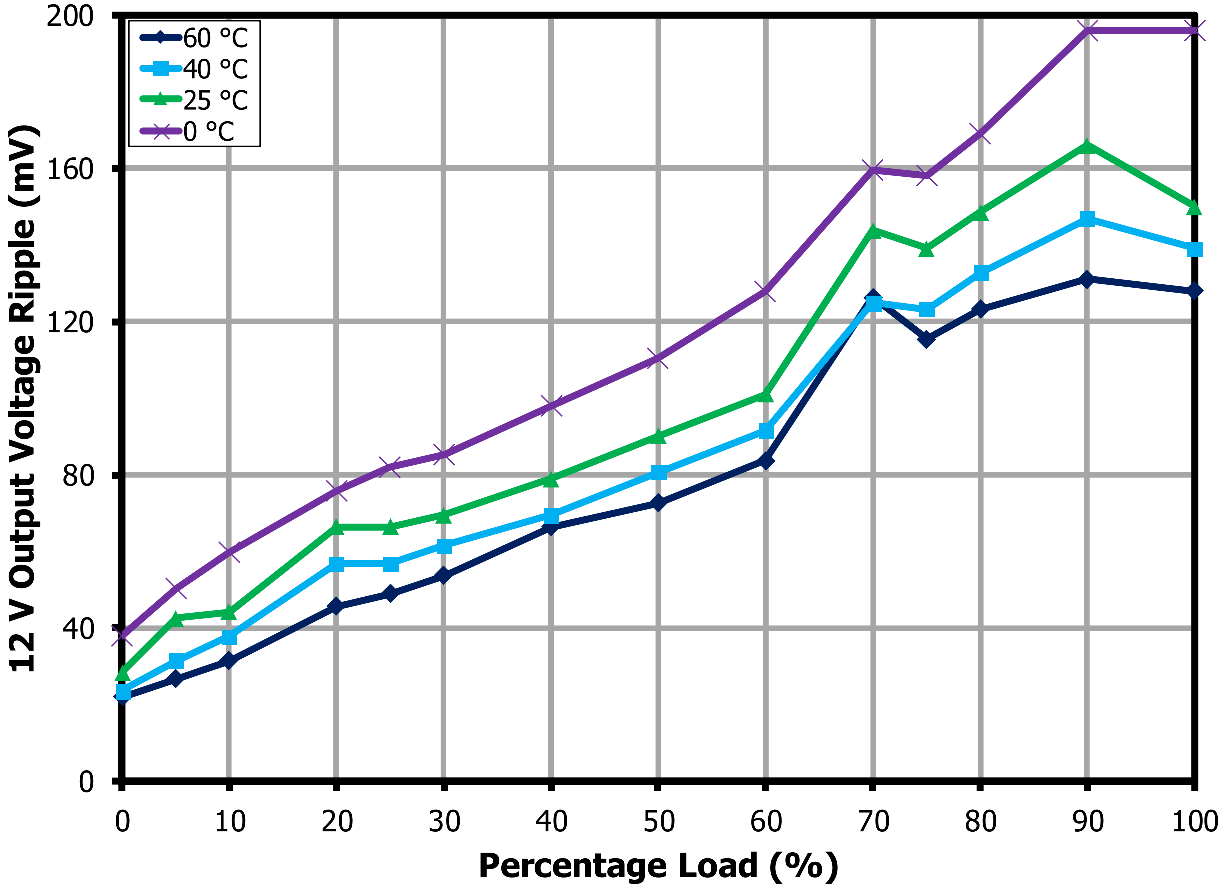


Figure 131 – 12 V Output Ripple at 85 VAC, 60 Hz.

10.6.3.2 115 VAC, 60 Hz

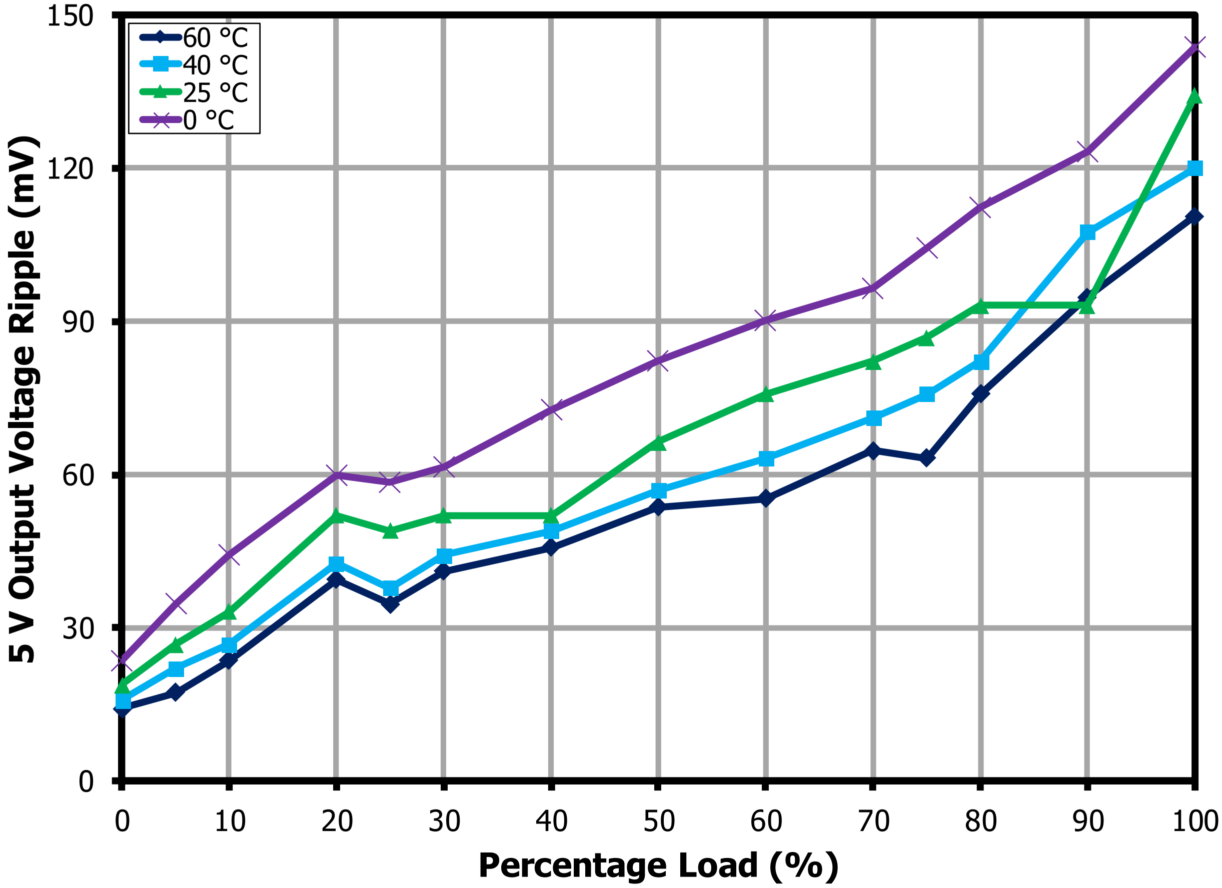


Figure 132 – 5 V Output Ripple at 115 VAC, 60 Hz.

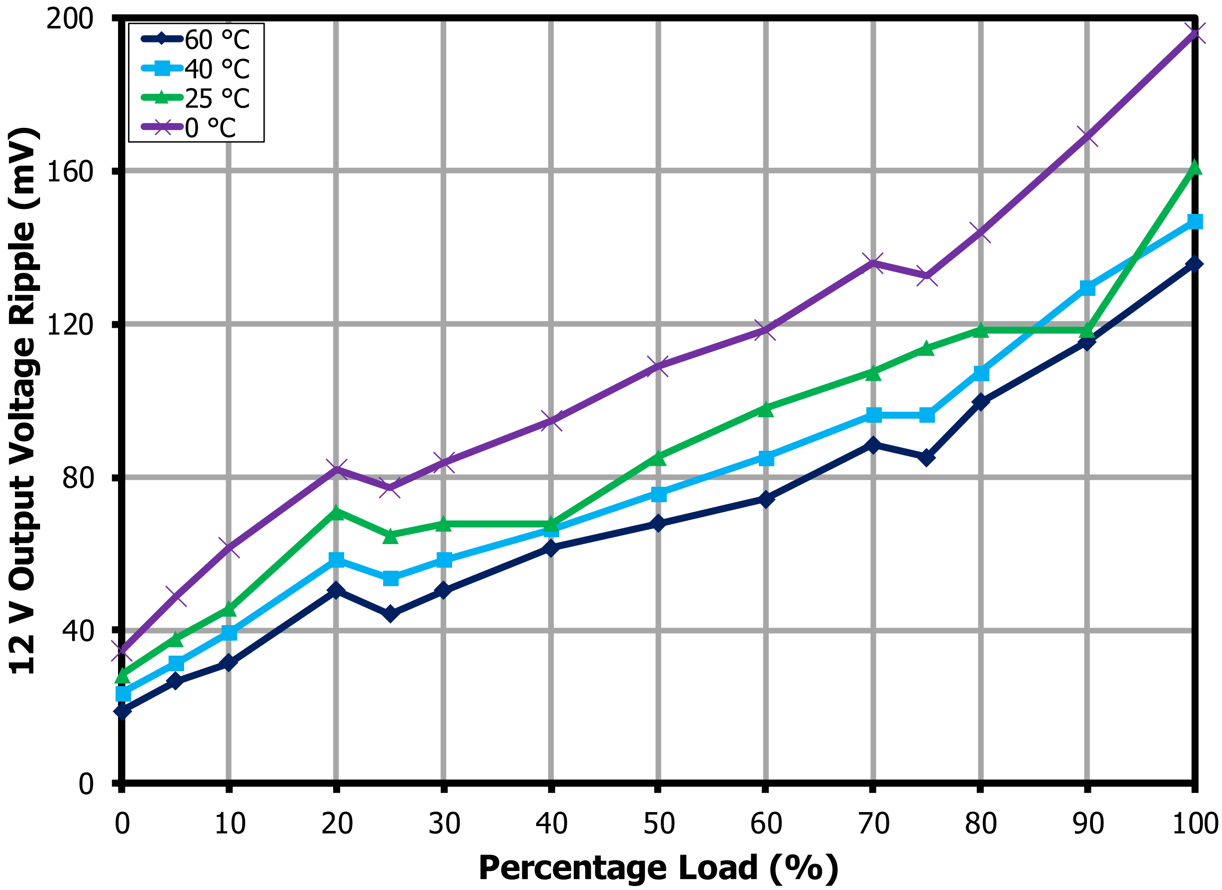


Figure 133 – 12 V Output Ripple at 115 VAC, 60 Hz.

10.6.3.3 230 VAC, 50 Hz

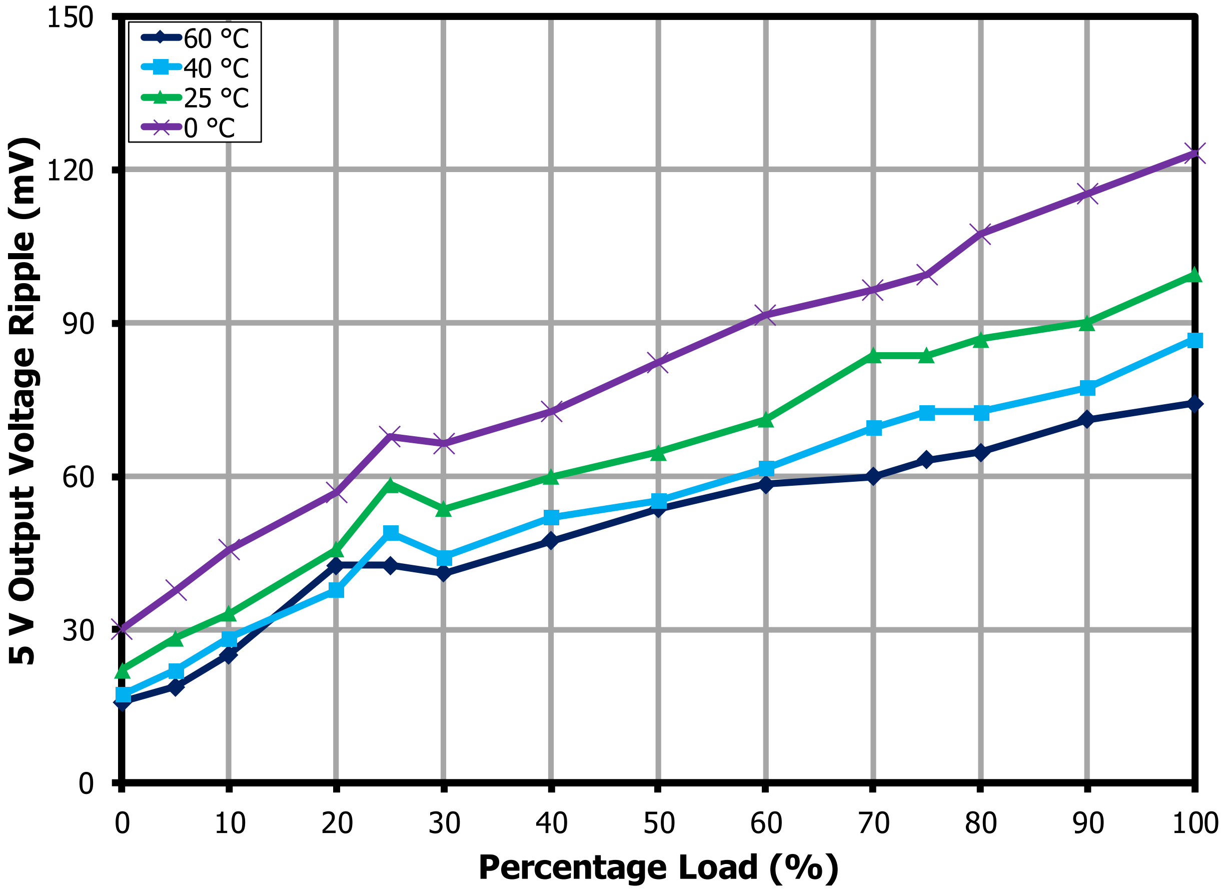


Figure 134 – 5 V Output Ripple at 230 VAC, 50 Hz.

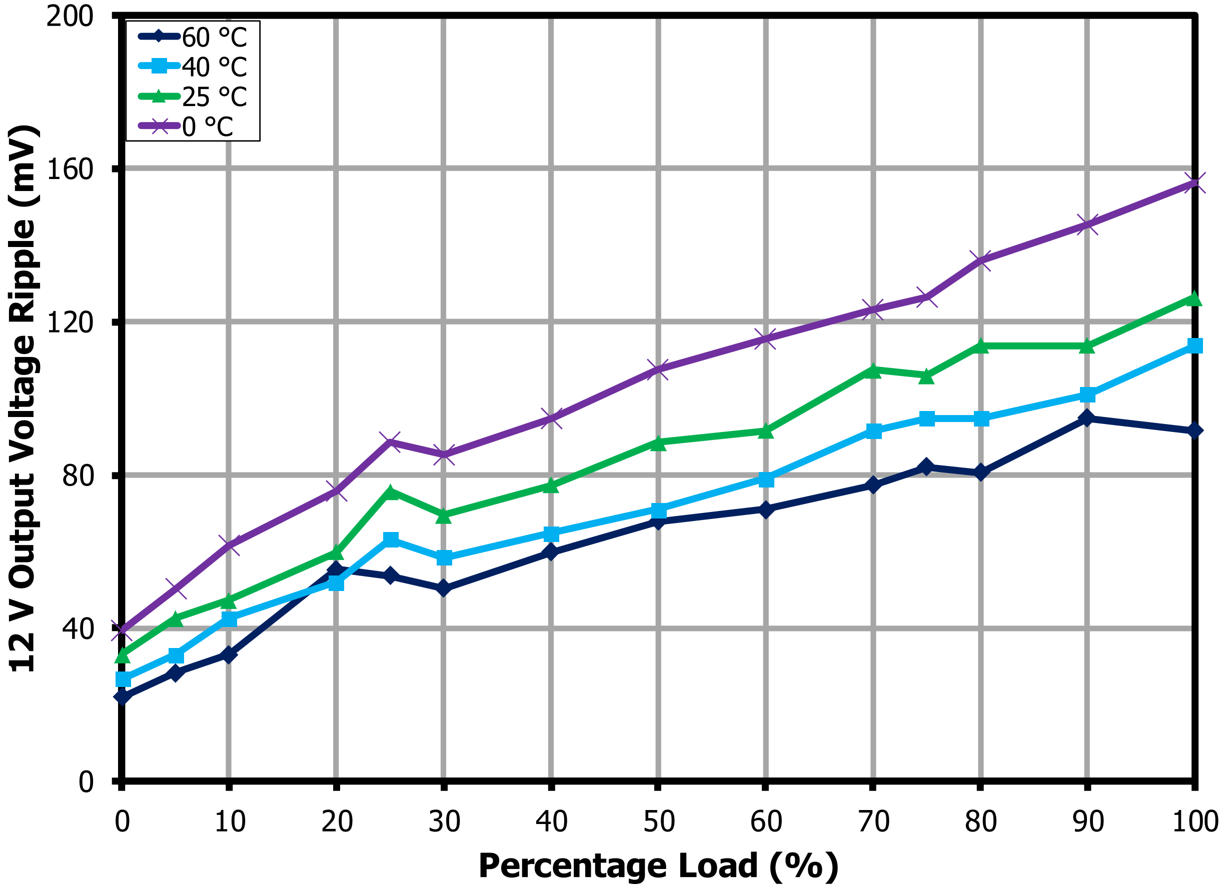


Figure 135 – 12 V Output Ripple at 230 VAC, 50 Hz.

10.6.3.4 277 VAC, 50 Hz

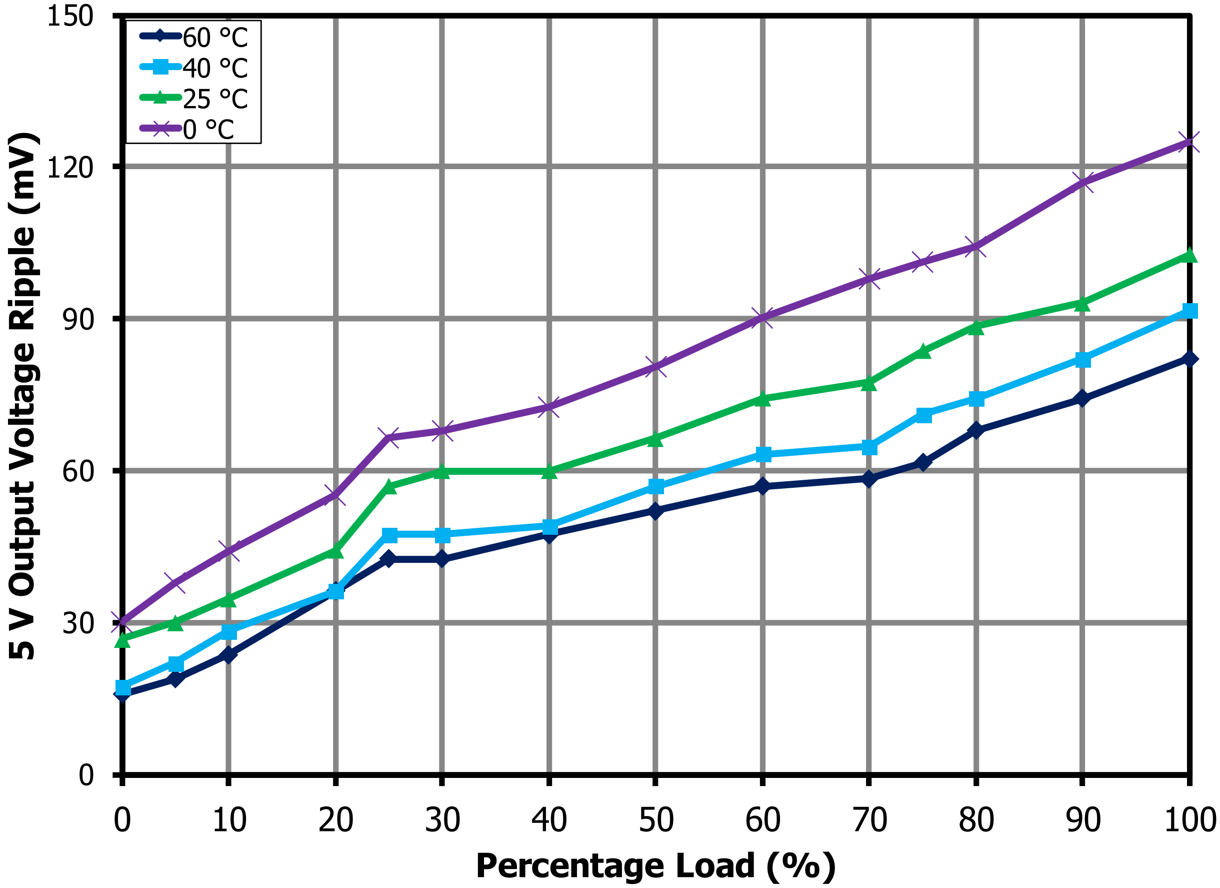


Figure 136 – 5 V Output Ripple at 277 VAC, 50 Hz.

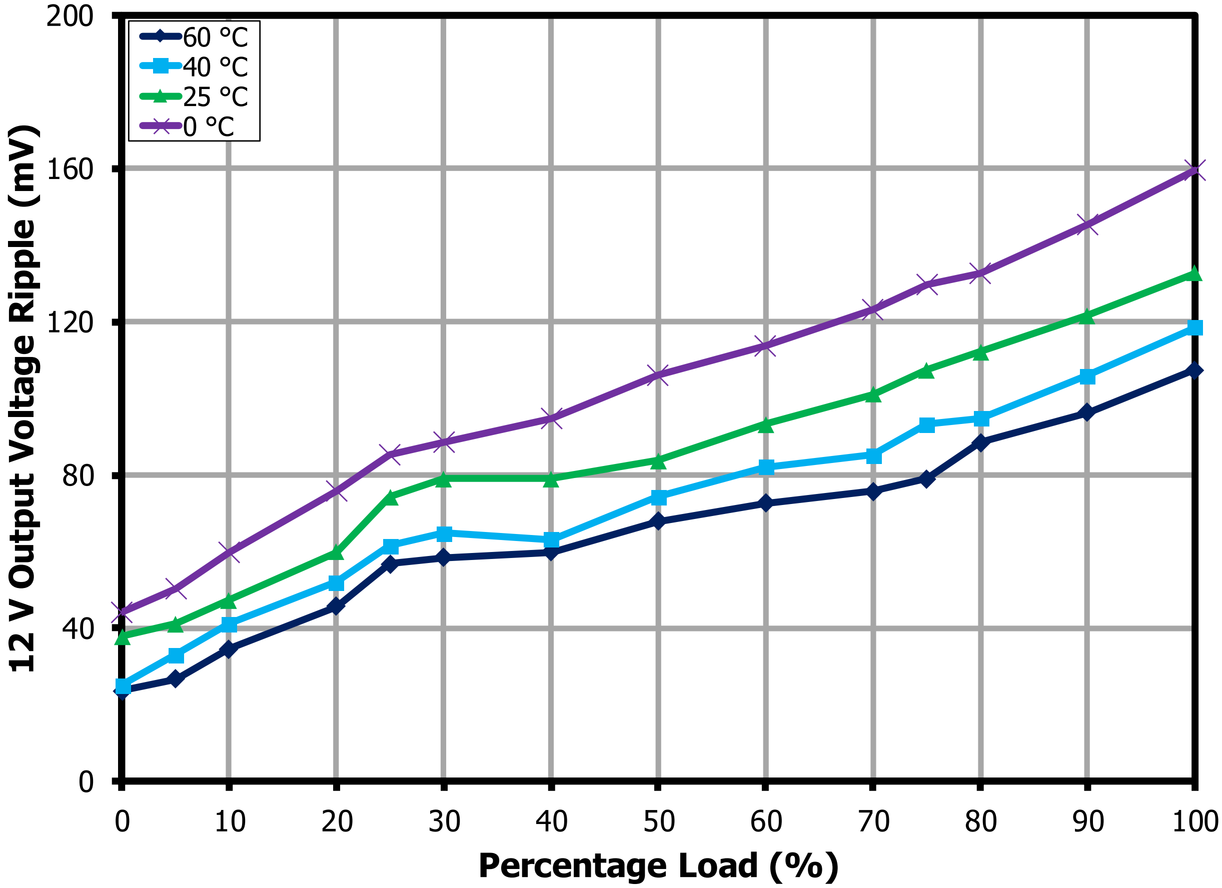


Figure 137 – 12 V Output Ripple at 277 VAC, 50 Hz.

11 Thermal Performance

11.1 *Room Temperature Thermal Scan*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using Thermal Camera. Soak time at full load is 2 hours.

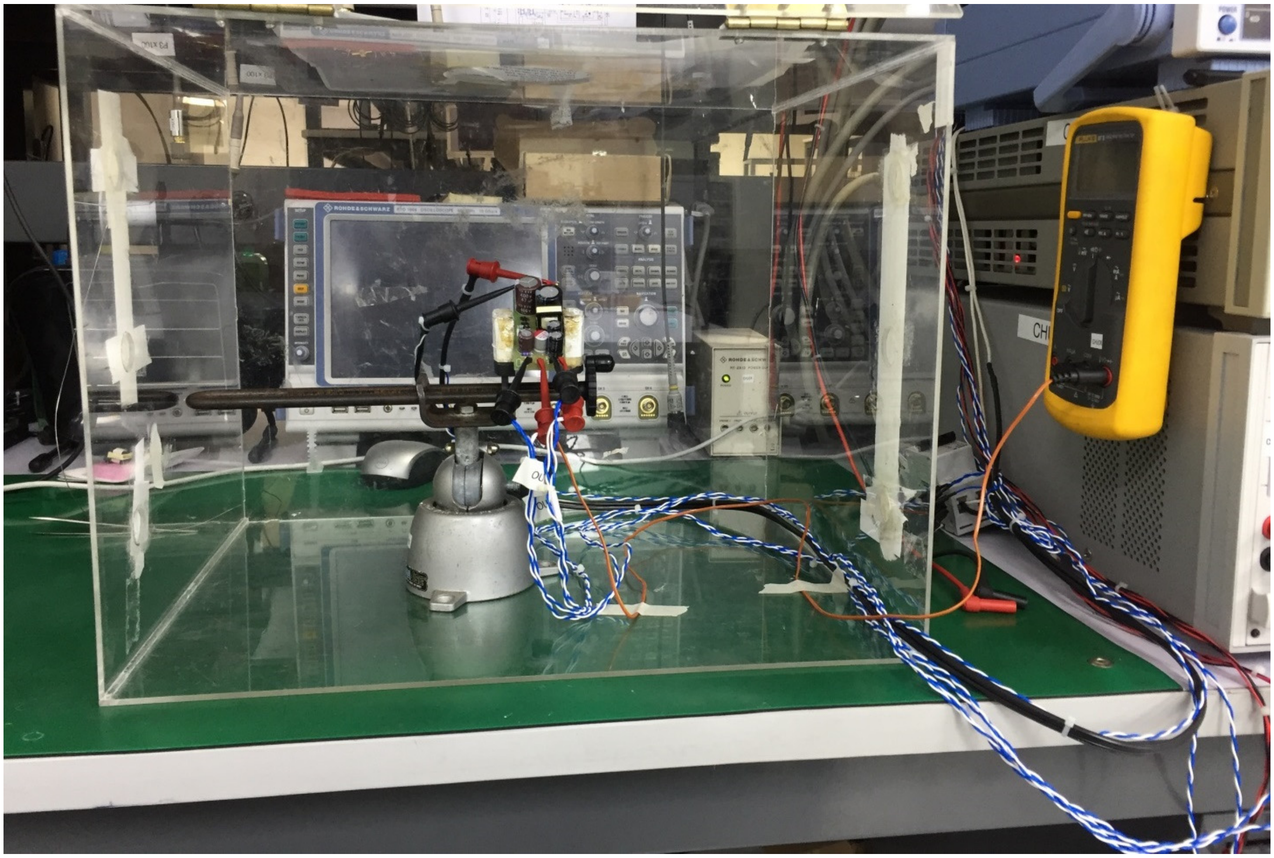


Figure 138 – Thermal Performance Set-up Using an Acrylic Box.

11.1.1 *85 VAC*

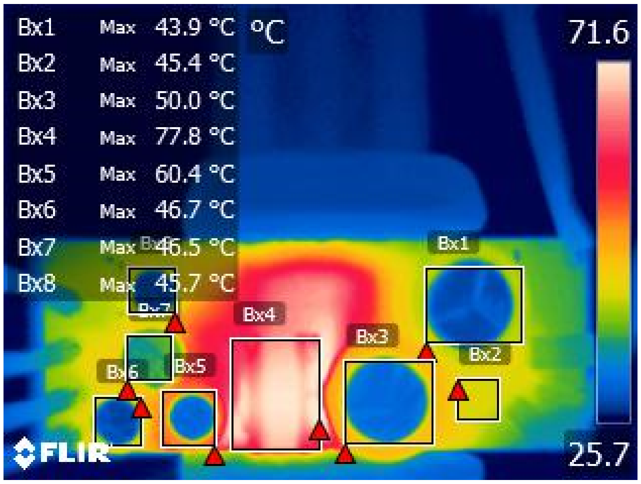


Figure 139 – 85 VAC, Full Load. Top Side.

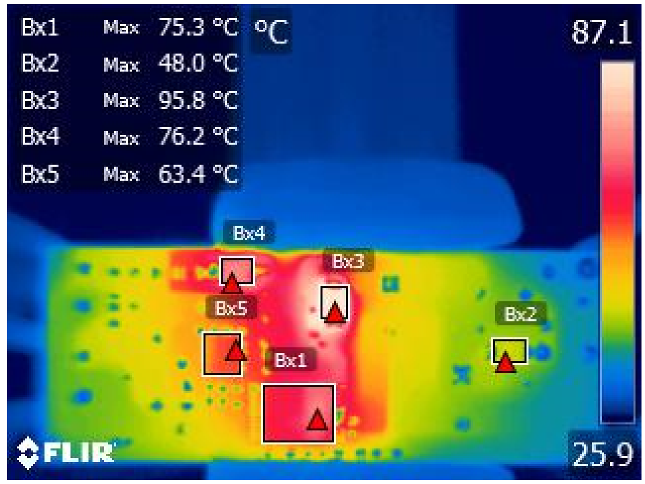


Figure 140 – 85 VAC, Full Load. Bottom Side.

Component	Temperature (ºC)
INN3673C IC (U1)	75.3
Input Rectifier (D1)	48.0
Input Capacitor (C2)	43.9
Input Choke Filter (L1)	45.4
Input Capacitor (C3)	50.0
Transformer (T1)	77.8
Zener Diode Clamp (VR3)	95.8
12 V Output Diode (D2)	76.2
5 V Output Synchronous Rectifier (Q1)	63.4
12 V Output Capacitor (C4)	60.4
12 V Output Capacitor (C14)	46.7
5 V Output Capacitor (C5)	46.5
5 V Output Capacitor (C6)	45.7
Ambient Temperature	25.1

11.1.2 *115 VAC*

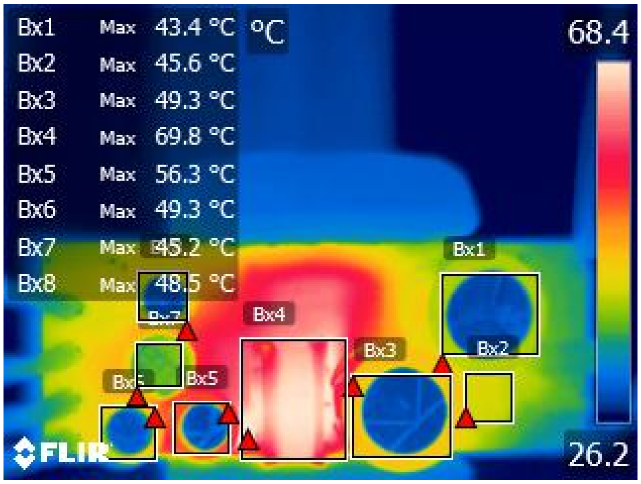


Figure 141 – 115 VAC, Full Load. Top Side.

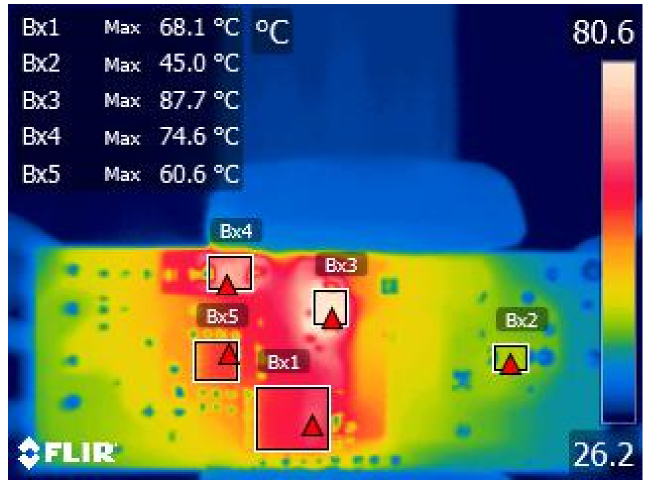


Figure 142 – 115 VAC, Full Load. Bottom Side.

Component	Temperature (ºC)
INN3673C IC (U1)	68.1
Input Rectifier (D1)	45.0
Input Capacitor (C2)	43.4
Input Choke Filter (L1)	45.6
Input Capacitor (C3)	49.3
Transformer (T1)	69.8
Zener Diode Clamp (VR3)	87.7
12 V Output Diode (D2)	74.6
5 V Output Synchronous Rectifier (Q1)	60.6
12 V Output Capacitor (C4)	56.3
12 V Output Capacitor (C14)	49.3
5 V Output Capacitor (C5)	45.2
5 V Output Capacitor (C6)	48.5
Ambient Temperature	25.0

11.1.3 *230 VAC*

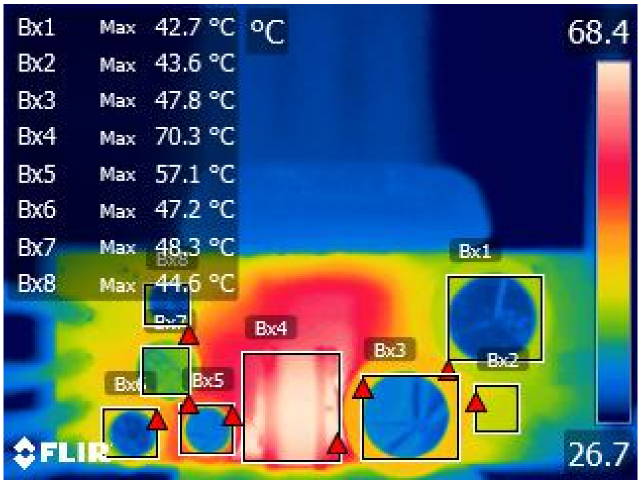


Figure 143 – 230 VAC, Full Load. Top Side.

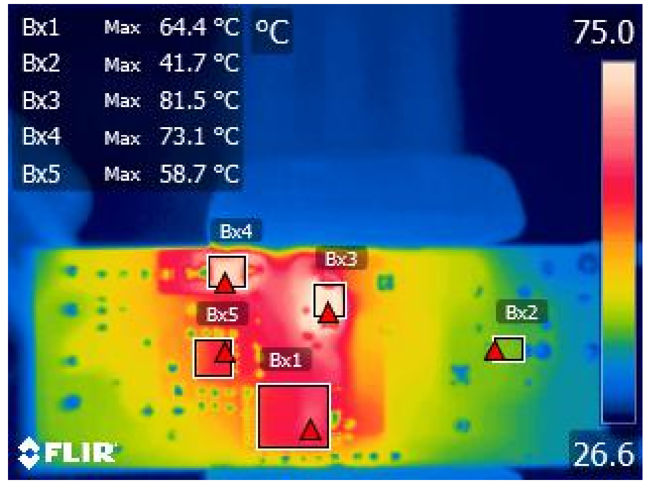


Figure 144 – 230 VAC, Full Load. Bottom Side.

Component	Temperature (°C)
INN3673C IC (U1)	64.4
Input Rectifier (D1)	41.7
Input Capacitor (C2)	42.7
Input Choke Filter (L1)	43.6
Input Capacitor (C3)	47.8
Transformer (T1)	70.3
Zener Diode Clamp (VR3)	81.5
12 V Output Diode (D2)	73.1
5 V Output Synchronous Rectifier (Q1)	58.7
12 V Output Capacitor (C4)	57.1
12 V Output Capacitor (C14)	47.2
5 V Output Capacitor (C5)	48.3
5 V Output Capacitor (C6)	44.6
Ambient Temperature	25.3

11.1.4 *277 VAC*

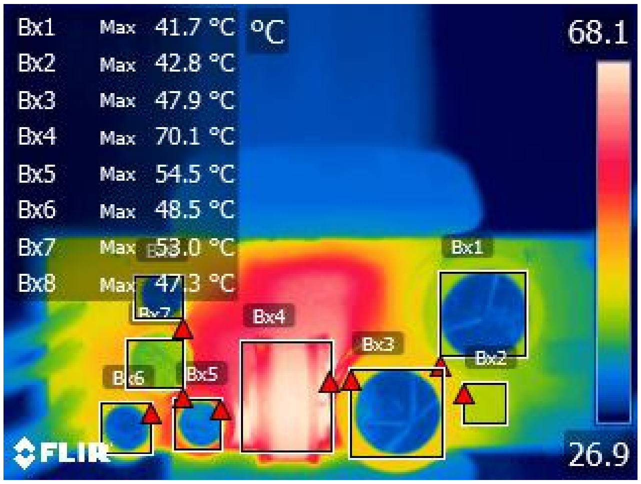


Figure 145 – 277 VAC, Full Load. Top Side.

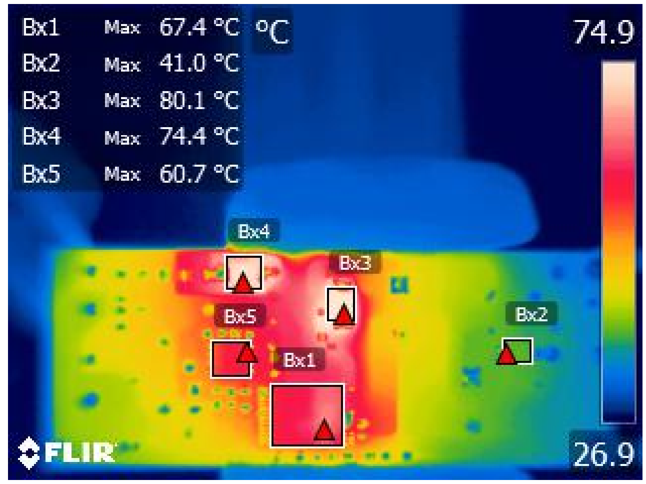


Figure 146 – 350 VAC, Full Load.

Component	Temperature (ºC)
INN3673C IC (U1)	67.4
Input Rectifier (D1)	41.0
Input Capacitor (C2)	41.7
Input Choke Filter (L1)	42.8
Input Capacitor (C3)	47.9
Transformer (T1)	70.1
Zener Diode Clamp (VR3)	80.1
12 V Output Diode (D2)	74.4
5 V Output Synchronous Rectifier (Q1)	60.7
12 V Output Capacitor (C4)	54.5
12 V Output Capacitor (C14)	48.5
5 V Output Capacitor (C5)	53.0
5 V Output Capacitor (C6)	47.3
Ambient Temperature	25.4

11.2 *70 °C Ambient Thermal Performance*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Ambient temperature inside enclosure is 70 ºC. Temperature was measured using type T thermocouple. Soak time at full load is 1 hour.

Figure 147 – Thermal Performance Set-up using Thermal Chamber.

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11.2.1 *85 VAC*

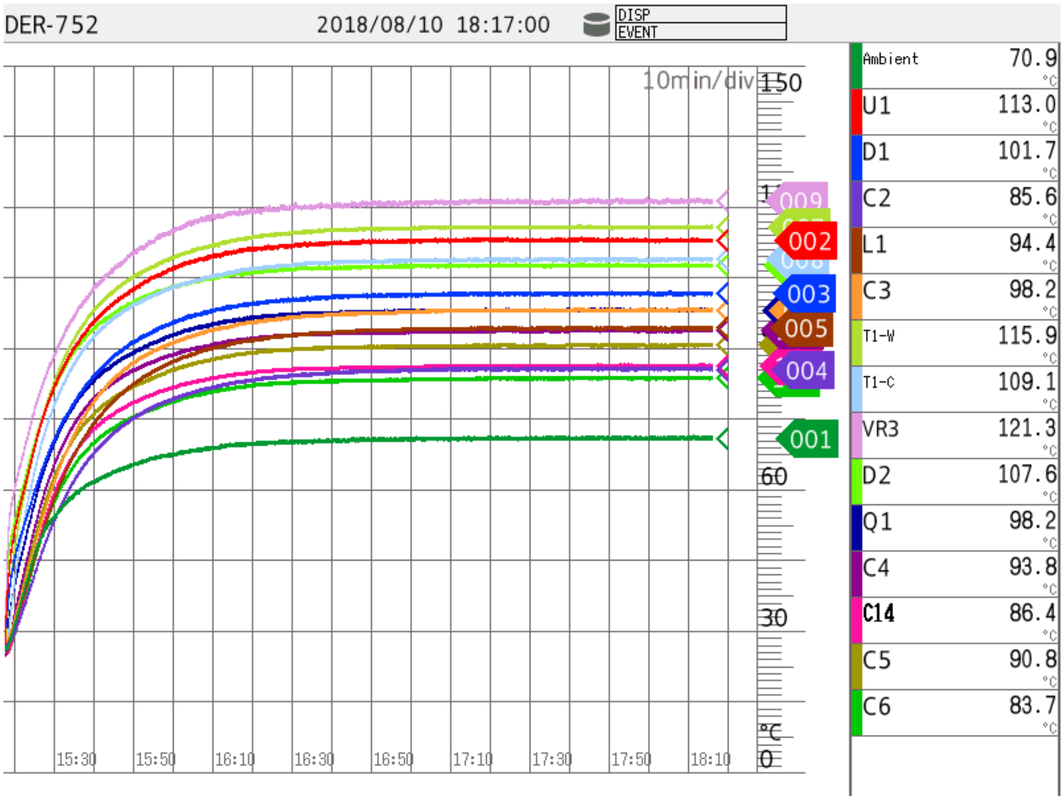


Figure 148 – Thermal Performance at 70 ºC (85 VAC).

Component	Temperature (ºC)
INN3673C IC (U1)	113.0
Input Rectifier (D1)	101.7
Input Capacitor (C2)	85.6
Input Choke Filter (L1)	94.4
Input Capacitor (C3)	98.2
Transformer-Winding (T1-W)	115.9
Transformer-Core (T1-C)	109.1
Zener Diode Clamp (VR3)	121.3
12 V Output Diode (D2)	107.6
5 V Output Synchronous Rectifier (Q1)	98.2
12 V Output Capacitor (C4)	93.8
12 V Output Capacitor (C14)	86.4
5 V Output Capacitor (C5)	90.8
5 V Output Capacitor (C6)	83.7
Ambient Temperature	70.9

11.2.2 *277 VAC*

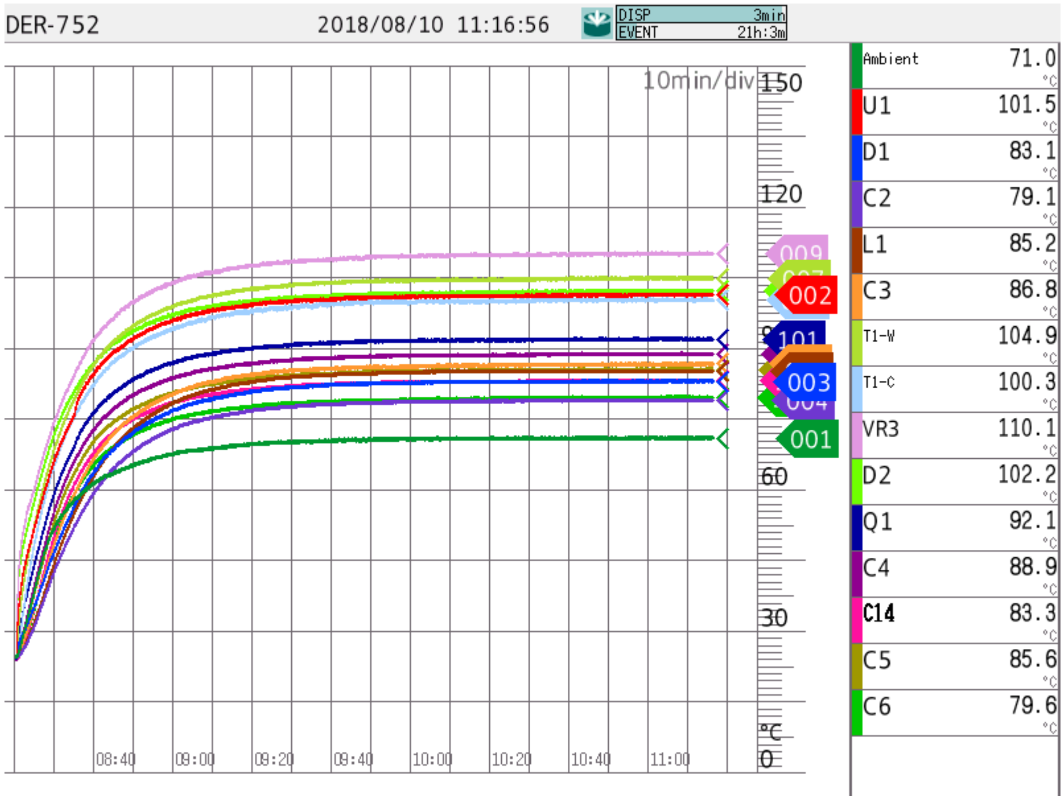


Figure 149 – Thermal Performance at 70 ºC (277 VAC).

Component	Temperature (ºC)
INN3673C IC (U1)	101.5
Input Rectifier (D1)	83.1
Input Capacitor (C2)	79.1
Input Choke Filter (L1)	85.2
Input Capacitor (C3)	86.8
Transformer-Winding (T1-W)	104.9
Transformer-Core (T1-C)	100.3
Zener Diode Clamp (VR3)	110.1
12 V Output Diode (D2)	102.2
5 V Output Synchronous Rectifier (Q1)	92.1
12 V Output Capacitor (C4)	88.9
12 V Output Capacitor (C14)	83.3
5 V Output Capacitor (C5)	95.6
5 V Output Capacitor (C6)	79.6
Ambient Temperature	71.0

11.3 *Over-Temperature Protection*

11.3.1 *85 VAC*

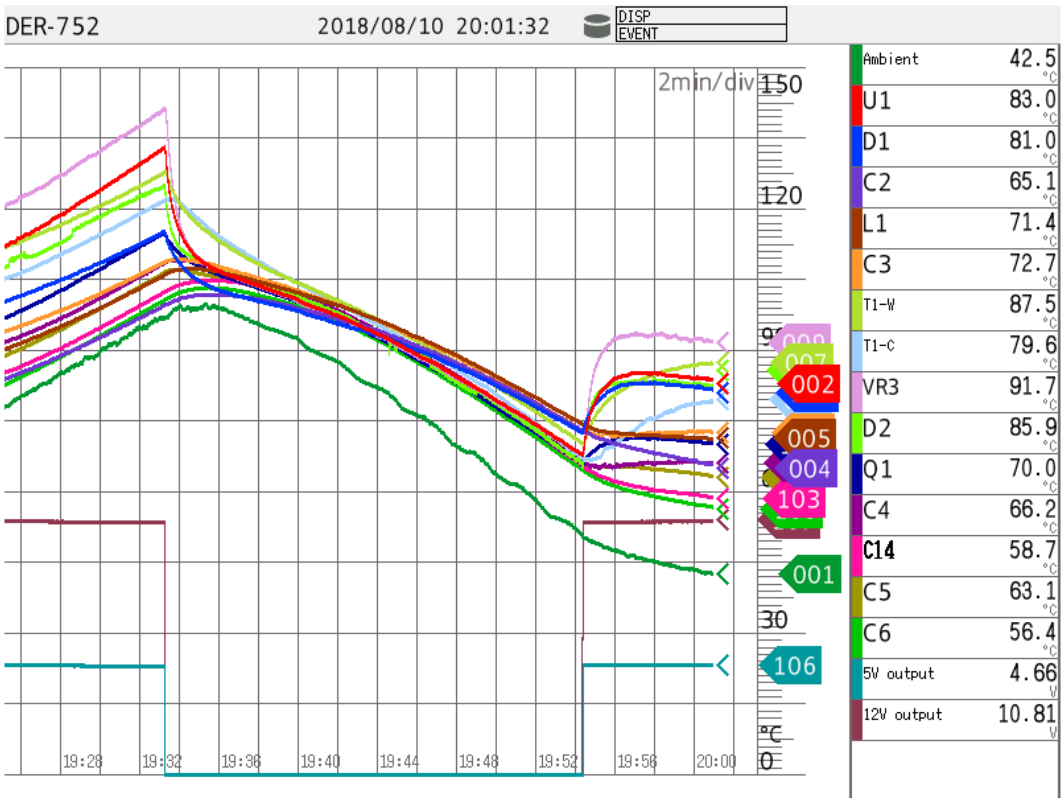


Figure 150 – 85 VAC Over-Temperature Protection.

Component	Temperature (ºC) At OTP Trigger	Temperature (ºC) At Recovery
INN3673C IC (U1)	133.1	67.9
Input Rectifier (D1)	115.2	72.6
Input Capacitor (C2)	99.6	73.0
Input Choke Filter (L1)	106.0	74.4
Input Capacitor (C3)	108.8	73.0
Transformer-Winding (T1-W)	127.8	70.3
Transformer-Core (T1-C)	121.8	67.1
Zener Diode Clamp (VR3)	141.3	67.6
12 V Output Diode (D2)	125.0	65.9
5 V Output Synchronous Rectifier (Q1)	115.0	65.8
12 V Output Capacitor (C4)	108.5	66.0
12 V Output Capacitor (C14)	102.4	65.4
5 V Output Capacitor (C5)	106.5	66.3
5 V Output Capacitor (C6)	100.7	64.6
Ambient Temperature	97.0	50.5

11.3.2 *277 VAC*

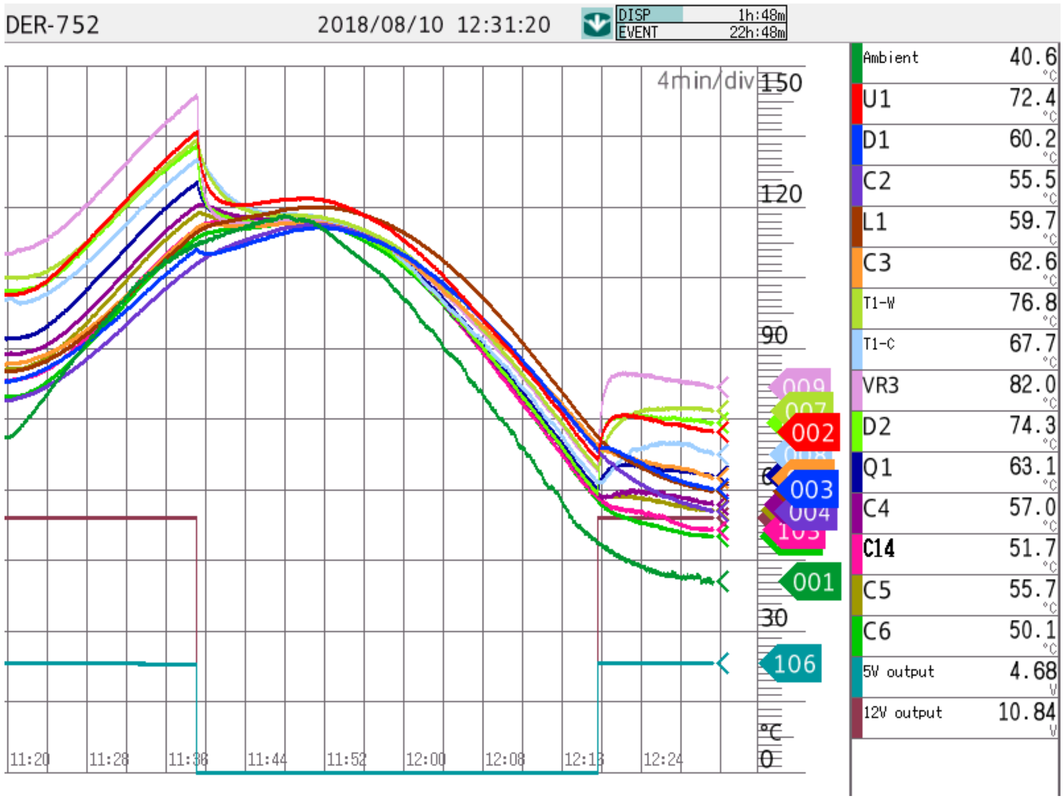


Figure 151 – 277 VAC Over-Temperature Protection.

Component	Temperature (ºC) At OTP Trigger	Temperature (ºC) At Recovery
INN3673C IC (U1)	136.0	66.5
Input Rectifier (D1)	111.1	68.6
Input Capacitor (C2)	108.1	68.4
Input Choke Filter (L1)	114.7	71.4
Input Capacitor (C3)	115.6	69.5
Transformer-Winding (T1-W)	134.3	64.6
Transformer-Core (T1-C)	130.1	61.8
Zener Diode Clamp (VR3)	143.8	64.1
12 V Output Diode (D2)	133.1	59.3
5 V Output Synchronous Rectifier (Q1)	125.2	60.1
12 V Output Capacitor (C4)	120.4	59.3
12 V Output Capacitor (C14)	115.5	58.5
5 V Output Capacitor (C5)	118.6	59.1
5 V Output Capacitor (C6)	113.5	57.8
Ambient Temperature	112.2	48.9

12 Conducted EMI

12.1 ***Test Set-up***

12.1.1 *Equipment and Load Used*

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC and 115 VAC.

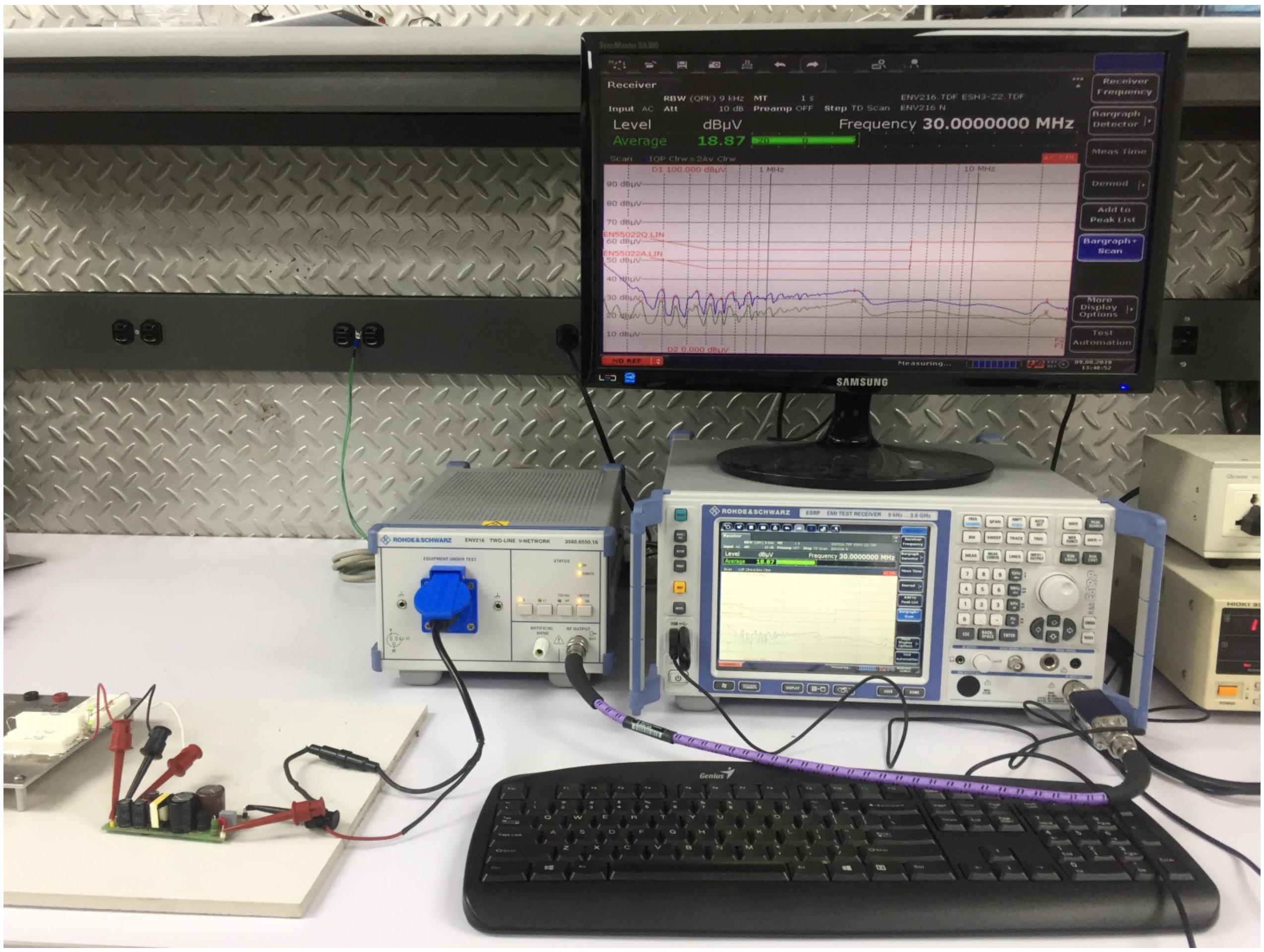
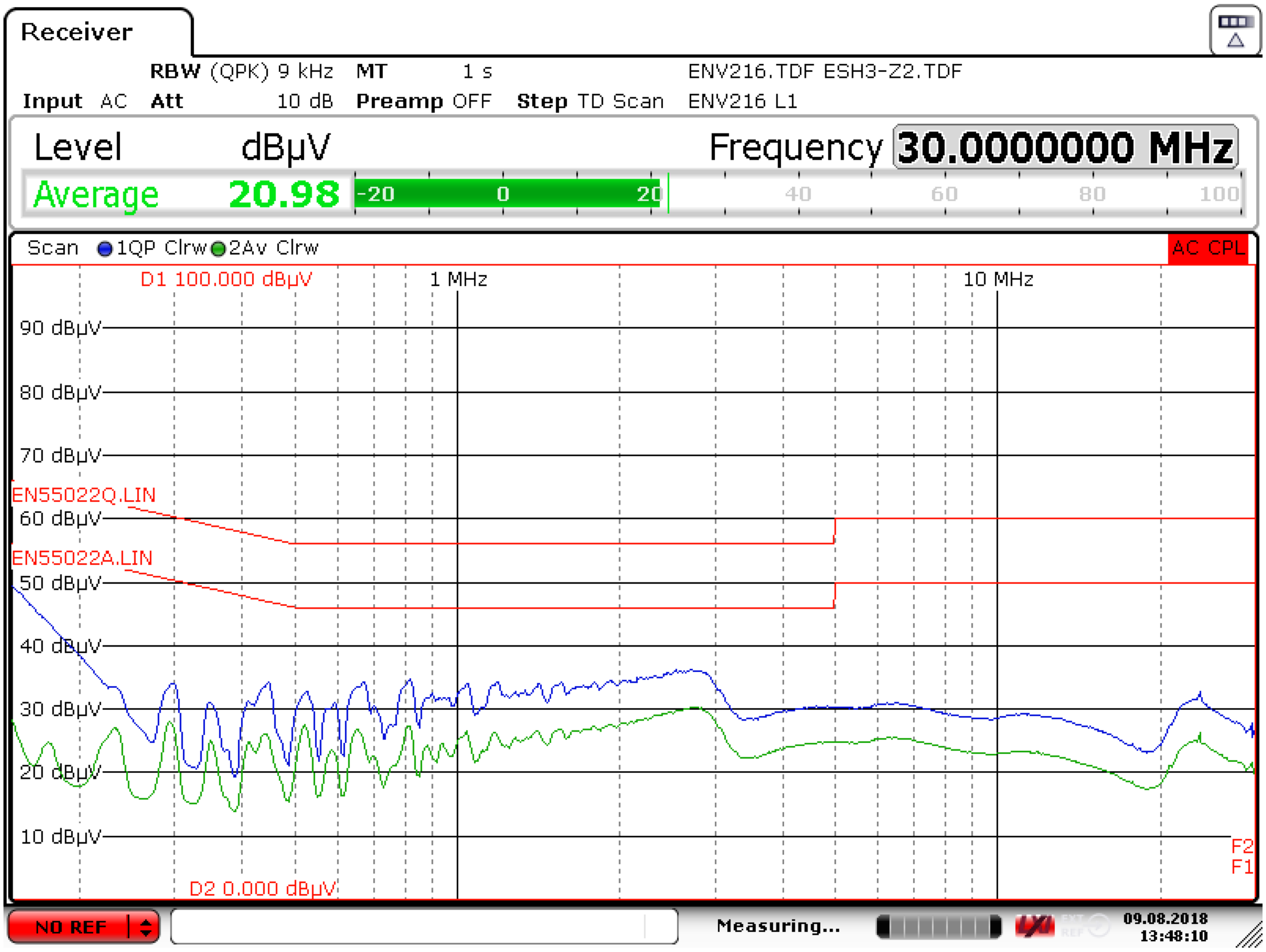


Figure 152 – Conducted EMI Test Set-up.

12.2 ***15 W Resistive Load, Floating Output***

12.2.1 *115 VAC, Line*



Date: 9.AUG.2018 13:48:10

Figure 153 – Floating Ground EMI at 115 VAC, Line.

12.2.2 *115 VAC, Neutral*

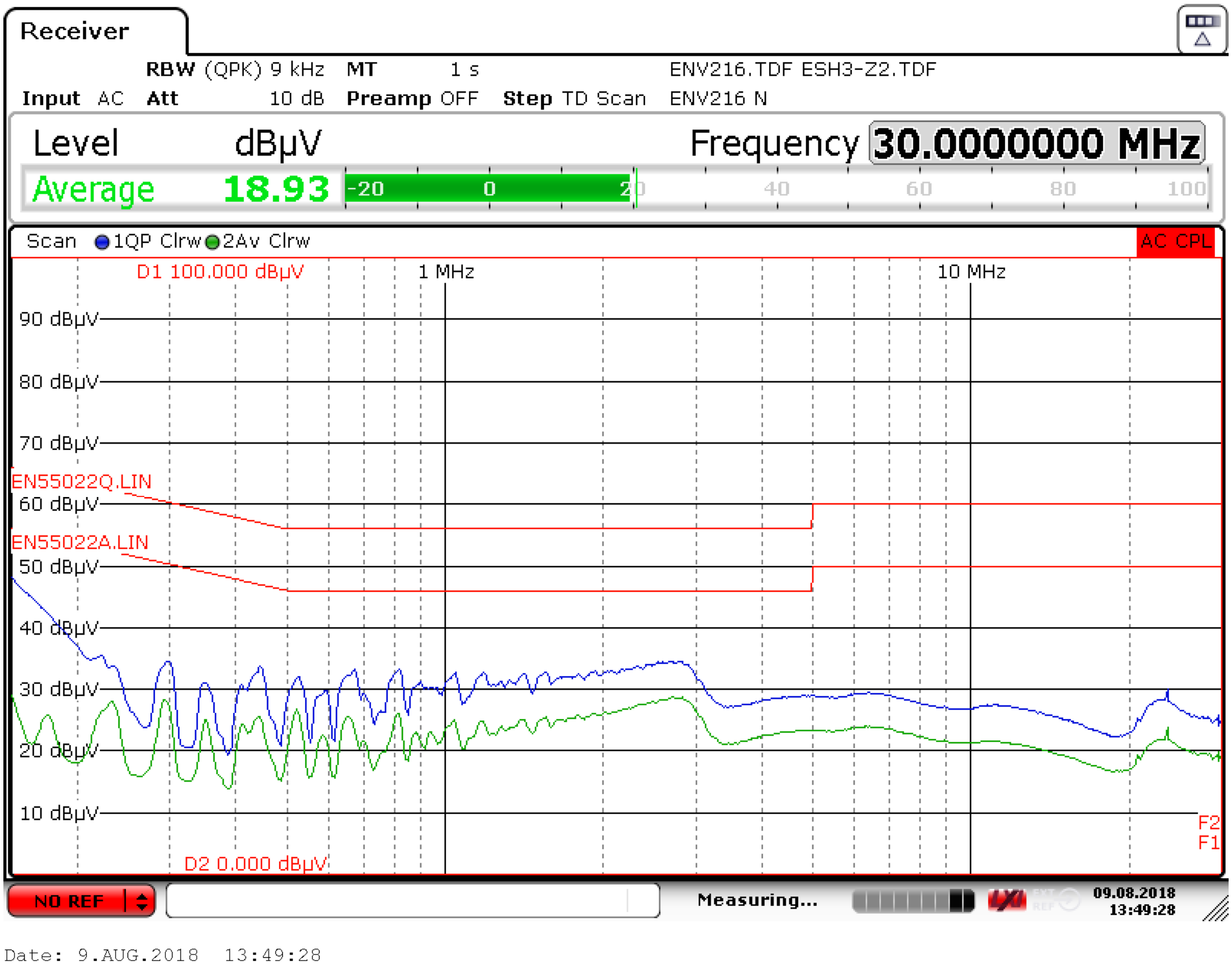
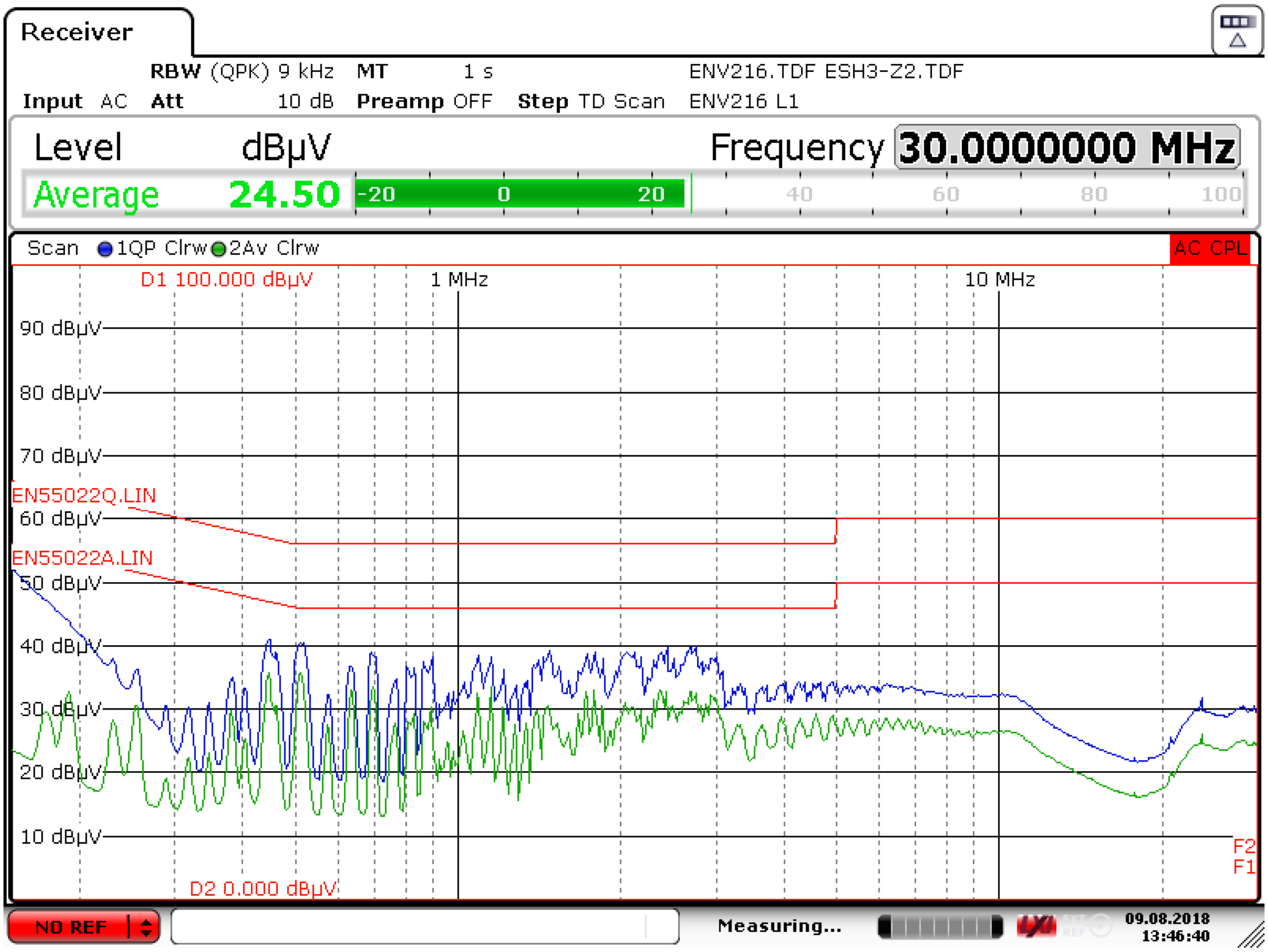


Figure 154 – Floating Ground EMI at 115 VAC, Neutral.

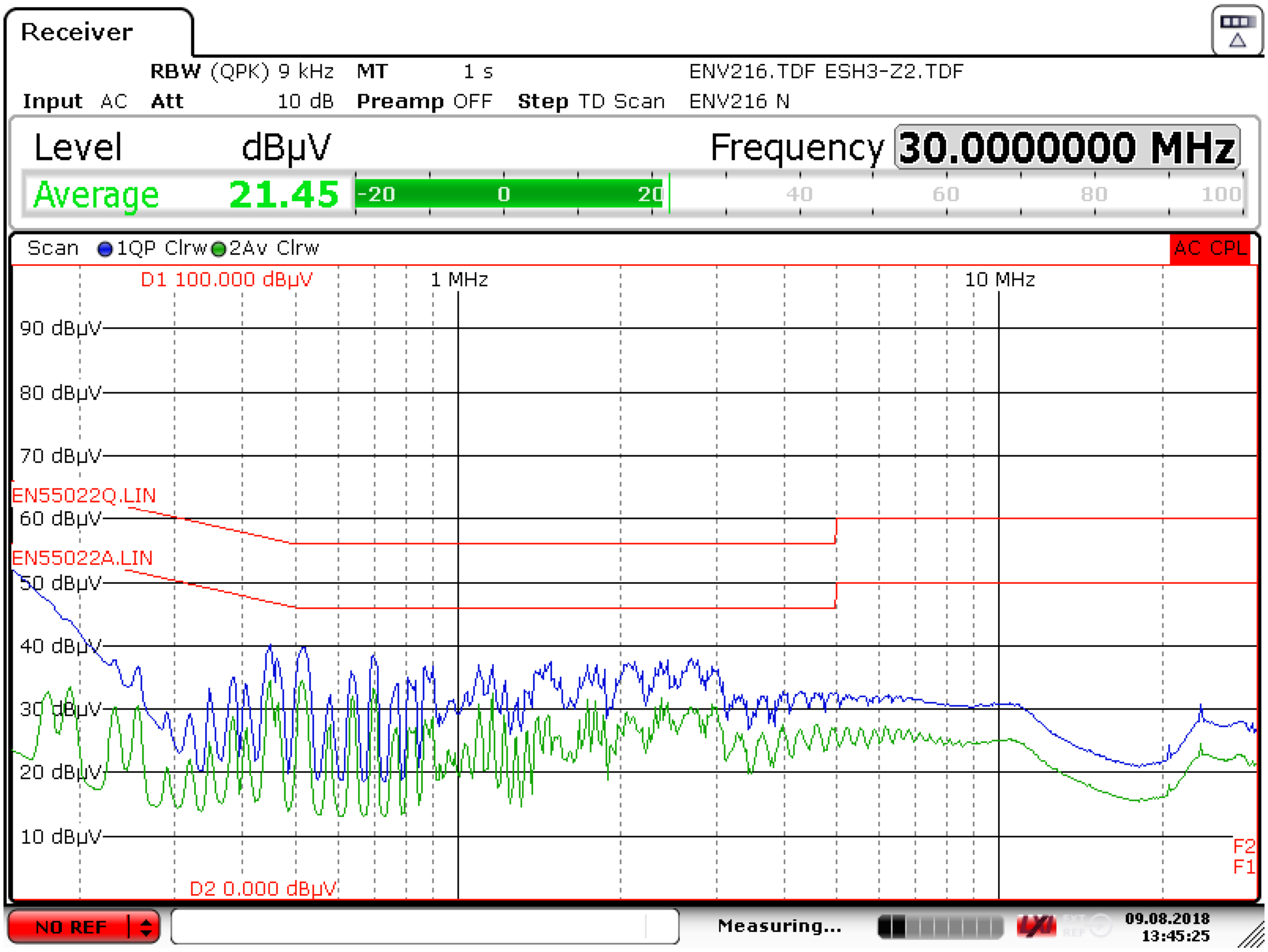
12.2.3 *230 VAC, Line*



Date: 9.AUG.2018 13:46:40

Figure 155 – Floating Ground EMI at 230 VAC, Line.

12.2.4 *230 VAC, Neutral*



Date: 9.AUG.2018 13:45:25

Figure 156 – Floating Ground EMI at 230 VAC, Neutral.

13 Line Surge

The unit was subjected to ±1000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 *Differential Surge Test*

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Note: In all PASSED results, no damage and no auto-restart were observed.

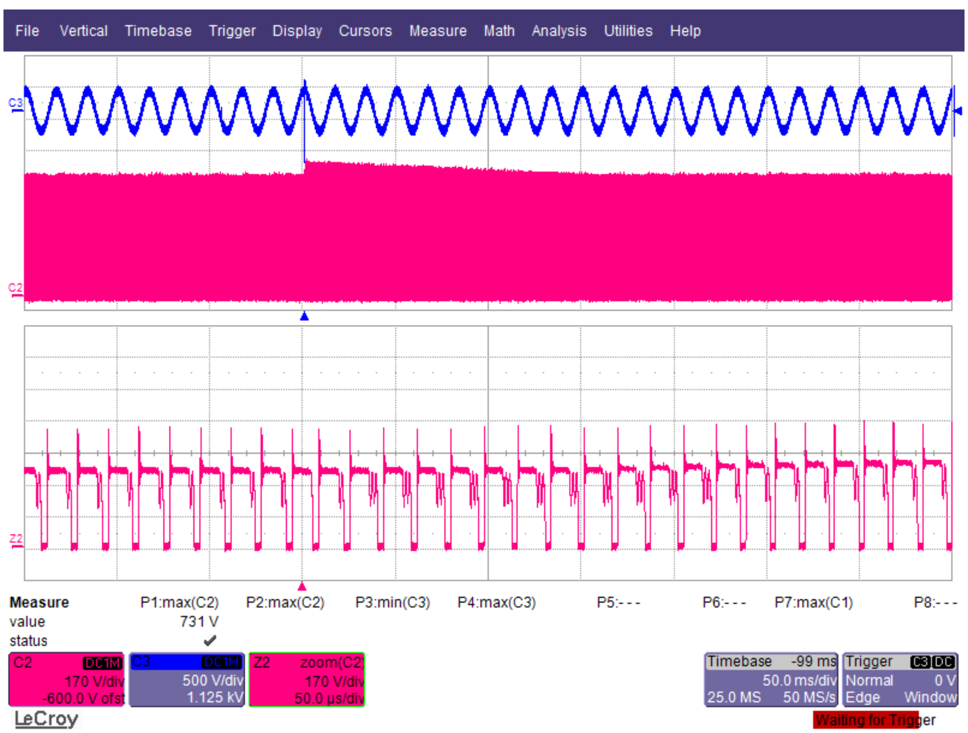


Figure 157 – Input AC Voltage vs. U1 MOSFET V_{DS} during 1 kV Differential Surge.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
31-Oct-18	CE	1.0	Initial Release.	Apps & Mktg
11-Jun-20	KM	1.1	Converted to RDR.	Apps & Mktg
17-Nov-21	KM	1.2	Added Magnetics Supplier. Updated Format	Apps & Mktg

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