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## Design Example Report

<b>Title</b>	<b><i>45 W USB PD 3.0 with 3.3 V - 16 V PPS Power Supply Using InnoSwitch™ 3-Pro INN3368C-H301 and VP302</i></b>
<b>Specification</b>	85 VAC – 264 VAC Input; 5 V, 3 A; 9 V, 3 A; 15 V, 3 A; 20 V, 2.25 A 3.3 V – 16 V PPS Outputs
<b>Application</b>	Mobile Phone Charger
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	DER-704
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### **Summary and Features**

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
  - I<sup>2</sup>C interface enables low pin count USB PD controller (10 pin)
  - Sophisticated telemetry and comprehensive protection features
- USB PD 3.0 with PPS highly optimized low pin count USB PD controller VP302
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Meets DOE6 and CoC V5 2016 efficiency requirement (>1% efficiency margin)
- Micro stepping of voltages and CC thresholds in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- <30 mW no-load input power
- Integrated thermal protection
- 20 mV voltage step / 50 mA current step in PPS mode

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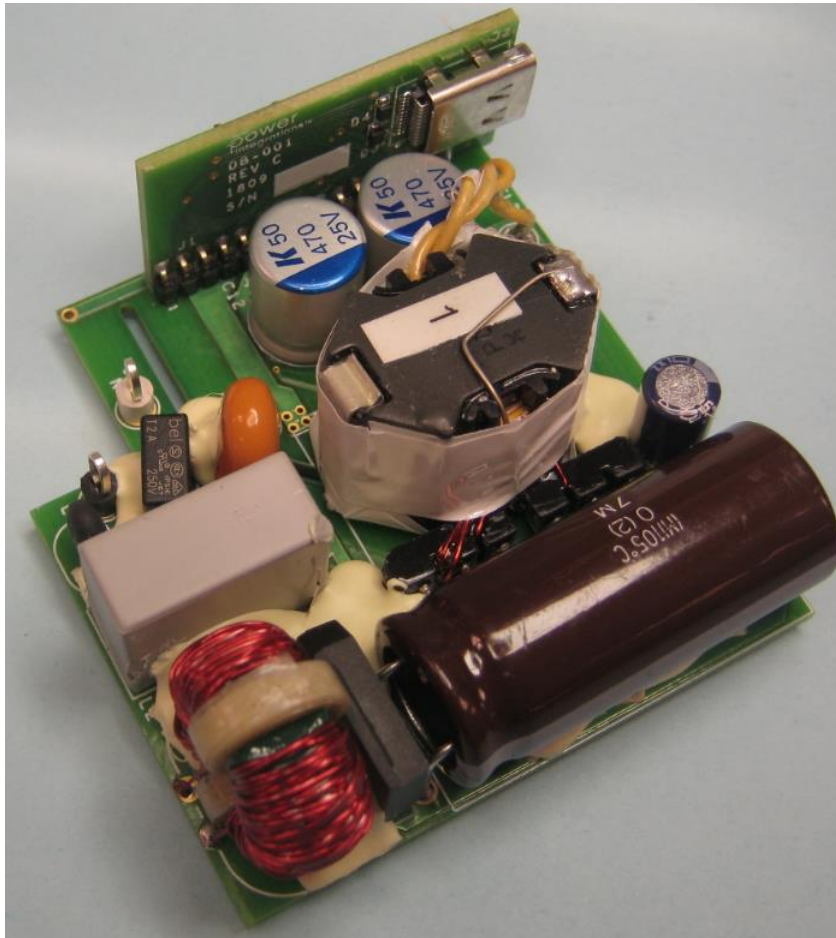
**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

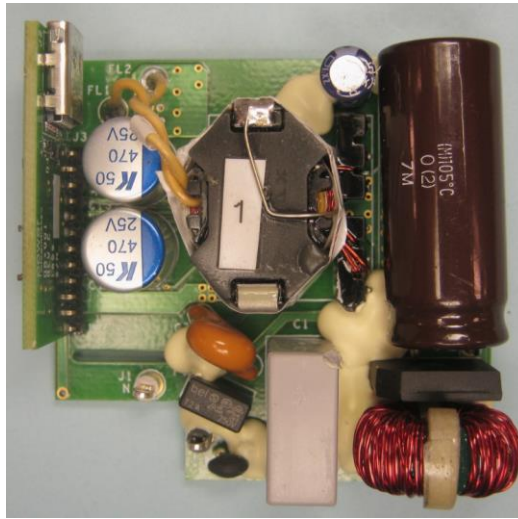
## 1 Introduction

This document is an engineering report describing a 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V 2.25 A USB PD PPS power supply. This power supply uses InnoSwitch3-Pro INN3368C-H301 IC and VP302 USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

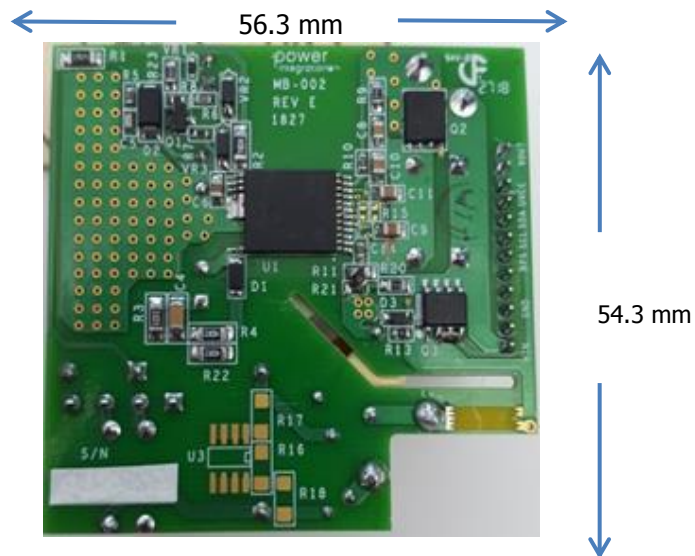
This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data



**Figure 1** – Populated Circuit Board Photograph, Entire Assembly.



**Figure 2** – Populated Circuit Board Photograph, Top.

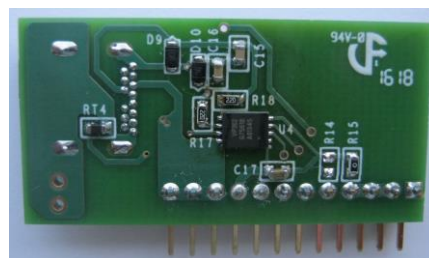
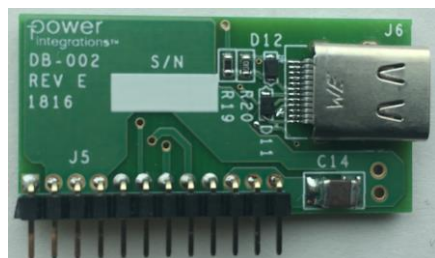


**Figure 3** – Populated Circuit Board Photograph, Bottom.

Maximum total height:  
23.56 mm



**Figure 4** Populated Circuit Board Photograph, Side View.



**Figure 5** – Populated Circuit Board Photograph, Daughter Board, Front and Rear.

## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	85		264	VAC	2 Wire – no P.E.
Frequency	$f_{LINE}$	47	50/60	64	Hz	
No-load Input Power (85 VAC)			34	40	mW	Measured at 85 VAC.
<b>Output</b>						
Output Voltage	$V_{OUT}$		5.0		V	$\pm 3\%$
Output Ripple Voltage	$V_{RIPPLE}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 m $\Omega$ . 20 MHz Bandwidth.
Output Current	$I_{OUT}$		3.0		A	
Efficiency	$\eta$	86.5			%	
Continuous Output Power	$P_{OUT}$			15	W	
<b>Output</b>						
Output Voltage	$V_{OUT}$		9.0		V	$\pm 3\%$
Output Ripple Voltage	$V_{RIPPLE}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 m $\Omega$ . 20 MHz Bandwidth.
Output Current	$I_{OUT}$		3.0		A	
Efficiency	$\eta$	88			%	
Continuous Output Power	$P_{OUT}$			27	W	
<b>Output</b>						
Output Voltage	$V_{OUT}$		15.0		V	$\pm 3\%$
Output Ripple Voltage	$V_{RIPPLE}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 m $\Omega$ . 20 MHz Bandwidth.
Output Current	$I_{OUT}$		3.0		A	
Efficiency	$\eta$	87.3			%	
Continuous Output Power	$P_{OUT}$			45	W	
<b>Output</b>						
Output Voltage	$V_{OUT}$		20.0		V	$\pm 3\%$
Output Ripple Voltage	$V_{RIPPLE}$			200	mV	At End of Cable. Cable Needs a Resistance of 100 m $\Omega$ . 20 MHz Bandwidth.
Output Current	$I_{OUT}$		2.25		A	
Efficiency	$\eta$	87.3			%	
Continuous Output Power	$P_{OUT}$			45	W	
Maximum Programmable Output Voltage	$V_{OUT}$	16			V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT}$	3.3			V	APDO Minimum Voltage.
PPS Voltage Step	$V_{OUT}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{OUT}$		50		mA	PPS current Step (USB PD 3.0).
<b>Conducted EMI</b>		Meets CISPR22B / EN55022B				
Ambient Temperature	$T_{AMB}$	0		40	$^{\circ}C$	Free Convection, Sea Level.

**Note:** To use this design for a charger/adaptor, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

### 3 Schematics

#### 3.1 Schematic [Part A - Mother Board]

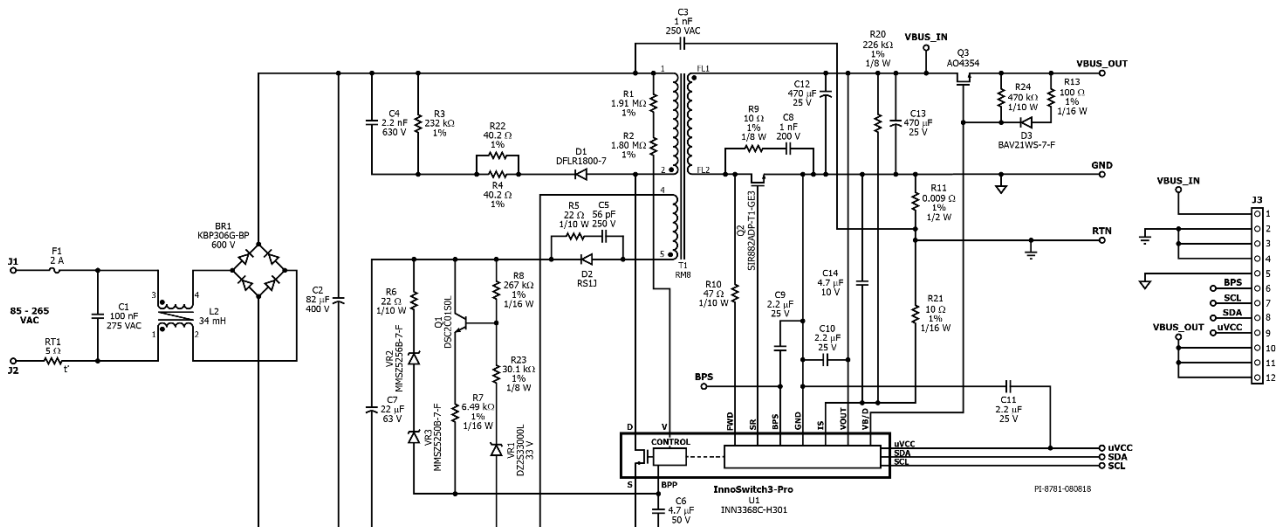


Figure 6 – Schematic of Mother Board.

### 3.2 Schematic [Part B - Daughter Board]

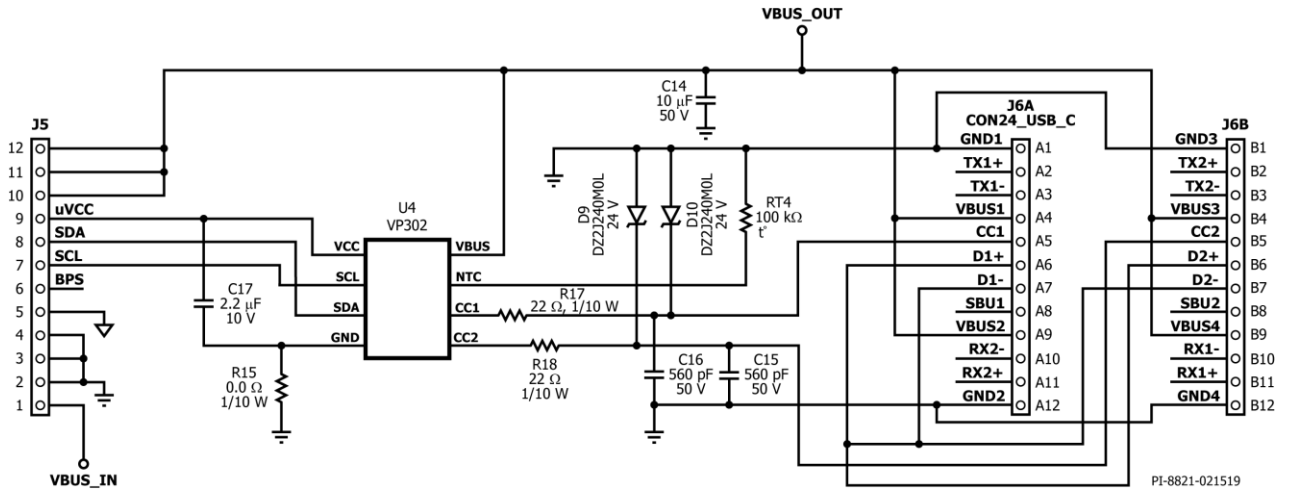


Figure 7 – Schematic of Daughter Board.

## 4 Circuit Description

### 4.1 *Mother Board Circuit Description*

#### 4.1.1 Input Rectifier and Filter

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L2 with capacitor C1 and C3 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across C2. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

#### 4.1.2 InnoSwitch3-Pro IC Primary

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the InnoSwitch3-Pro IC U1. Resistors R1 and R2 provide input voltage sense protection for undervoltage and overvoltage conditions.

A low cost RCD clamp formed by diode D1, resistors R3, R4 and R22, and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C6 when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C7. Resistor R7 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U1. A linear regulator comprising resistor R8, R23, BJT Q1 and Zener diode VR1 ensures sufficient current flows through R7 such that the internal current source is not required to charge C6 during normal operation. The RC network comprising of resistor R5 and capacitor C5 offers damping to the high frequency ringing in the voltage across diode D2 which reduces radiated EMI.

Zener diodes VR2 and VR3 offer primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes a current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the  $I_{SD}$  threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R6 limits the current injected to BPP pin.



#### 4.1.3 InnoSwitch3-Pro IC Secondary

The secondary-side of the InnoSwitch3-Pro IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q2 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R9 and C8.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately  $V_{SR(TH)}$ . Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C9 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to 3.0 V. Below this level the unit enters auto-restart until the output load is reduced. Capacitor C10 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

Output current is sensed by monitoring the voltage drop across resistor R11 between the IS and SECONDARY GROUND pins. A threshold of approximately 32 mV reduces losses. A decoupling capacitor C14 is needed between the IS and SECONDARY GROUND pin to improve CC accuracy. Resistors R12 and R20 provide a positive slope to the CC characteristic. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current. When the output current is below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I<sup>2</sup>C interface.

N-MOSFET Q3 forms the bus switch and is controlled by the VB/D pin on the InnoSwitch3-Pro IC. When the bus switch is opened, resistor R13 and diode D3 are needed from the source of the MOSFET to its gate for providing a voltage discharge path for capacitor C14 on the daughter board.

## 4.2 ***Daughter Board Circuit Description***

### 4.2.1 USB Type-C and PD Interface

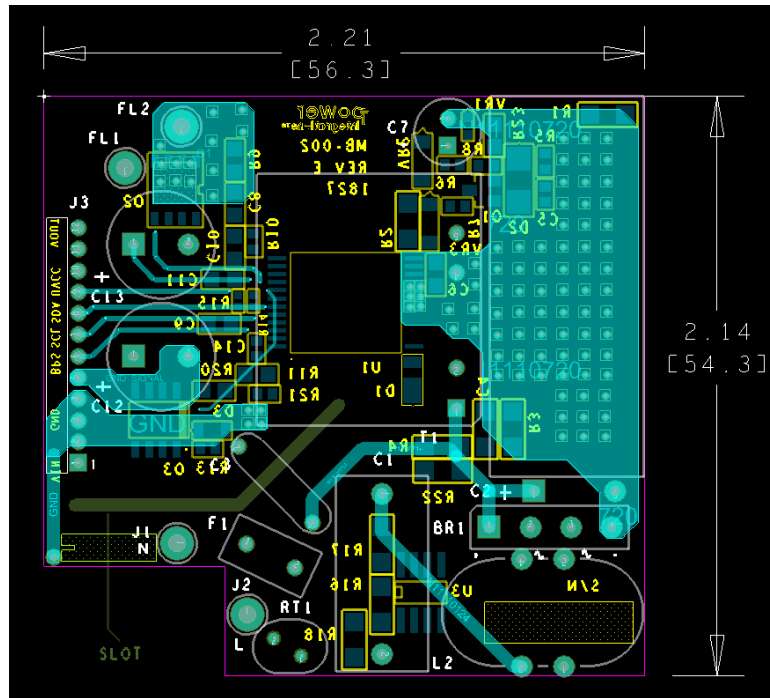
In this design, VP302 U4 is the USB Type-C and PD controller. Output of the InnoSwitch3-Pro IC powers the VP302 device through the uVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

VP302 IC communicates with InnoSwitch3-Pro IC through the I<sup>2</sup>C interface using the SCL and SDA pins through which it sets the CV, CC, V<sub>KP</sub>, OVA and UVA parameters. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I<sup>2</sup>C interface.

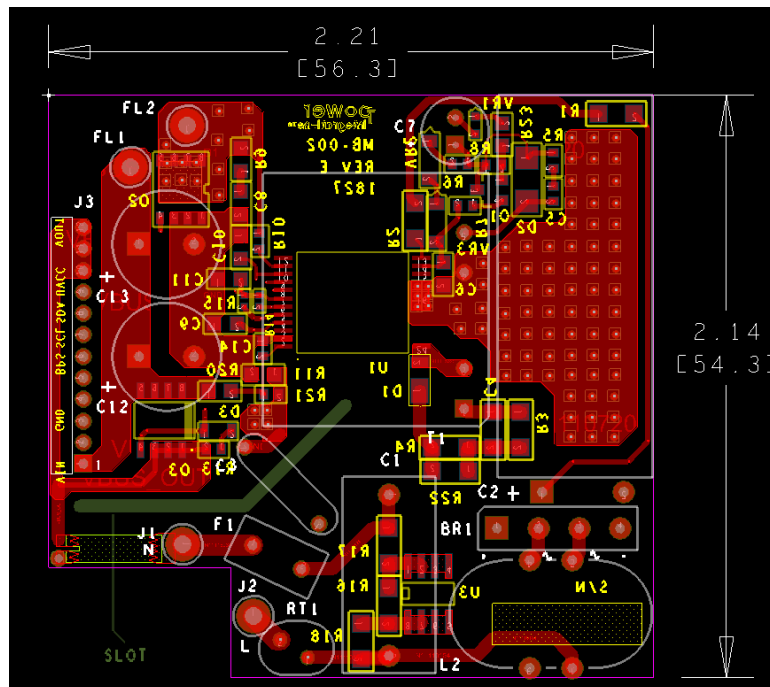
Capacitor C17 provides decoupling to the VP302 IC. Capacitors C15, C16; resistors R17, and R18; TVS D9, D10, D11 and D12 provide protection from ESD to pins CC1, CC2, D+ and D-. Thermistor RT4 connected to pin 7 (NTC) of the VP302 IC provides temperature detection functionality for the Type-C connector.

### 5 PCB Layout

PCB thickness is 0.062 inches.



**Figure 8** – Printed Circuit Layout, Mother Board, Top.



**Figure 9** – Printed Circuit Layout, Mother Board, Bottom.

**Note:** Component references U3, R14, R15, R17 and R18 although present in the layout; they are not to be populated.



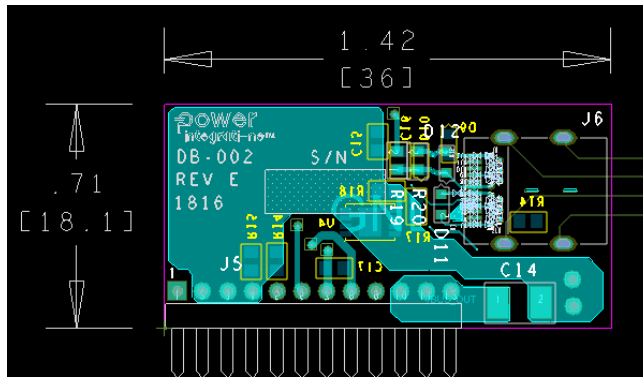


Figure 10 – Printed Circuit Layout, Daughter board, Top.

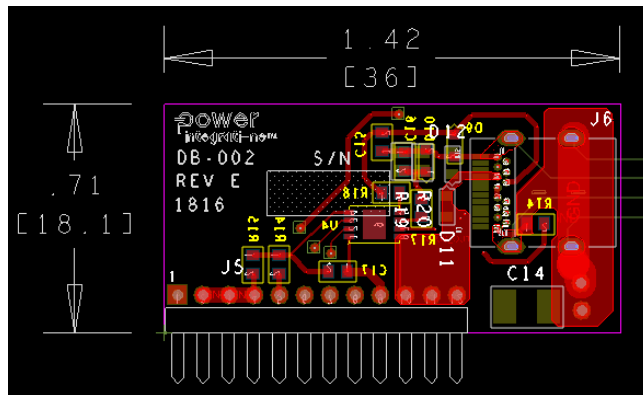
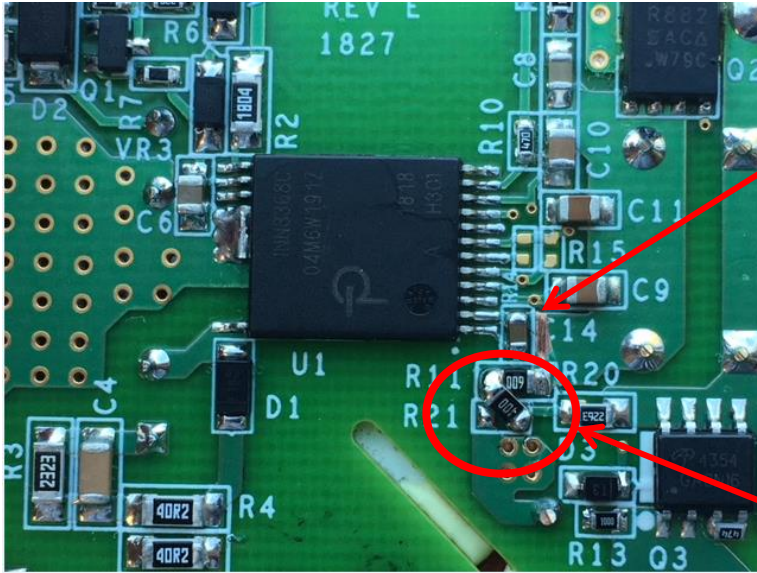


Figure 11 – Printed Circuit Layout, Daughter Board, Bottom.

**Note:** Component reference R15 although present in the layout, is not to be populated.

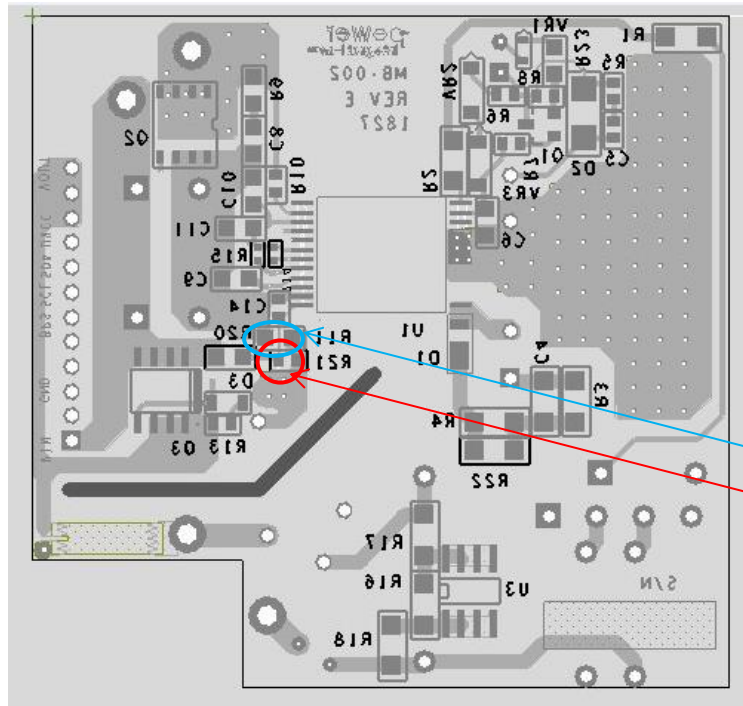
### 5.1 PCB Modifications



Notch created on PCB. This is done in order to ensure Kelvin connection to  $R_{SENSE}$  from GND pin.

R21: 10  $\Omega$ ; One end of the resistor is placed on top of R11. This is done in order to ensure Kelvin connection to  $R_{SENSE}$  from IS pin.

Figure 12 – Modifications done on Printed Circuit Board, Bottom.

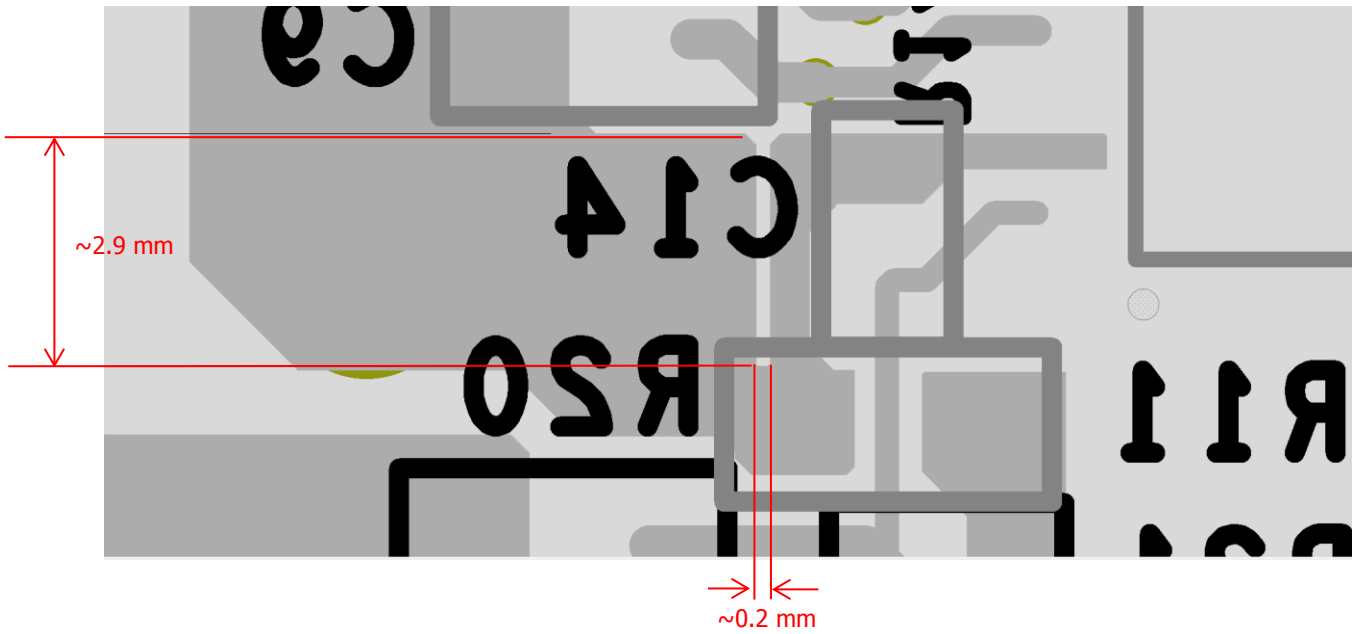


R11; 9 m $\Omega$

R21: 10  $\Omega$ ; Left edge of resistor is de-soldered from pad and soldered on top of R11

Figure 13 – Modification 1; Repositioning of R21 on Printed Circuit Board image, Bottom.





**Figure 14** – Modification 2; Etching Away of Copper on Printed Circuit Board Image, Bottom. Kelvin Sensing from GND Pin to Sense Resistor R11.

## 6 Bill of Materials – Mother Board

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	J1 J2	Test point, THRU-HOLE Mount	5010	Keystone
2	1	BR1	600 V, 3 A, Bridge Rectifier, GBP	KBP306G-BP	Micro Commercial
3	1	C1	100 nF, 275VAC, Film, X2	F1772-410-2000	Vishay
4	1	C2	82 $\mu$ F, 400 V, Electrolytic, Low ESR, (14.5 x 35)	EPAG401ELL820MU35S	Nippon Chemi-Con
5	1	C3	1 nF, Ceramic, Y1	440LD10-R	Vishay
6	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
7	1	C5	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
8	1	C6	4.7 $\mu$ F, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
9	1	C7	22 $\mu$ F, 63, Electrolytic, Low ESR, 1000 m $\Omega$ , (6.3 x 11.5)	ELXZ630ELL220MFB5D	Nippon Chemi-Con
10	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
11	3	C9, C10, C11	2.2 $\mu$ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
12	2	C12 C13	470 $\mu$ F, 25 V, $\pm$ 20%, Al Organic Polymer, Gen. Purpose, Can, 15 m $\Omega$ , 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
13	1	C14	4.7 $\mu$ F, 10 V, Ceramic, X5R, 0603	C1608X5R1A475M/0.50	TDK
14	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
15	1	D2	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
16	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
18	1	L2	34 mH, Toroidal Common Mode Choke, custom	32-00345-00	Power Integrations
19	1	Q1	NPN, 100V, 20 Ma, SOT23-3	DSC2C01S0L	Panasonic
20	1	Q2	100 V, 60 A, 8.7 m $\Omega$ , N-Channel, PowerPAK SO-8	SIR882ADP-T1-GE3	Vishay
21	1	Q3	MOSFET, N-CH, 30 V, 23 A (Ta), 3.1W (Ta), 3.7 m $\Omega$ (@ 20 A, 10 V), 8SOIC	AO4354	Alpha & Omega Semi
22	1	R1	RES, 1.91 M $\Omega$ , 1%, 1/4 W, Thick Film, 1206	RMCF1206FT1M91	Stackpole
23	1	R2	RES, 1.80 M $\Omega$ , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
24	1	R3	RES, 232 k $\Omega$ , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2323V	Panasonic
25	2	R4 R22	RES, 40.2 $\Omega$ , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF40R2V	Panasonic
26	2	R5 R6	RES, 22 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
27	1	R7	RES, 6.49 k $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF6491V	Panasonic
28	1	R8	RES, 267 k $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2673V	Panasonic
29	1	R9	RES, 10 $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
30	1	R10	RES, 47 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
31	1	R11	RES, 0.009 $\Omega$ , 0.5 W, 1%, 0805	CRF0805-FZ-R009ELF	Bourns
32	1	R13	RES, 100 $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
33	1	R20	RES, 226 k $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2263V	Panasonic
34	1	R21	RES, 10 $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
35	1	R23	RES, 30.1 k $\Omega$ , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3012V	Panasonic
36	1	R24	RES, 470 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ474V	Panasonic
37	1	RT1	NTC Thermistor, 5 $\Omega$ , 1 A	MF72-005D5	Cantherm
38	1	T1	Bobbin, RM8, Vertical, 12 pins	P-803	Pin Shine
39	1	U1	InnoSwitch3-Pro, InSOP24D package	INN3368C-H301	Power Integrations
40	1	VR1	33 V, 5%, 200 mW, SSMINI-2	DZ2S33000L	Panasonic
41	1	VR2	DIODE ZENER 30 V 500 mW SOD123	MMSZ5256B-7-F	Diodes, Inc.
42	1	VR3	DIODE ZENER 20 V 500 mW SOD123	MMSZ5250B-7-F	Diodes, Inc.

## 7 Bill of Materials – Daughter Board

Item	Qty	Ref Des	Description	Mfg
1	1	C14	10 $\mu$ F, 35 V, Ceramic,Y5V, 1210	Taiyo Yuden
2	2	C15 C16	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	Samsung
3	1	C17	2.2 $\mu$ F, 10 V, Ceramic, X5R, 0603	Murata
4	2	D9 D10	DIODE, ZENER, 24 V, 200 mW, SMINI2	Panasonic
5	1	J5	15 Position (1 x 15) header, 2 mm pitch, Right Angle	Sullins Connector
6	1	J6	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material!, Superspeed+, Receptacle Connector, 24 Position, SMT, Right Angle, TH	Würth
7	1	R15	RES, 0 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	Panasonic
8	2	R17 R18	RES, 22 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	Panasonic
9	1	R19	DNP	
10	1	R20	DNP	
11	1	RT4	NTC Thermistor, 100 k $\Omega$ , 3%, 0603	Murata
12	1	U4	VP302 IC, USB PD Type-C Controller for SMPS	VIA Labs
13	2	D11 D12	DNP	





## 8 Transformer Specification

### 8.1 Electrical Diagram

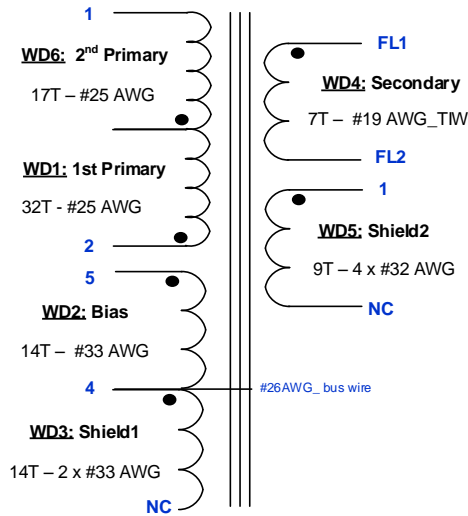


Figure 15 – Transformer Electrical Diagram.

### 8.2 Electrical Specifications

<b>Electrical Strength</b>	1 second, 60 Hz, from ins 1-5 to leads FL1-FL2.	3000 VAC
<b>Primary Inductance</b>	Pins 1-2, all other open, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	502 μH, ±5%
<b>Resonant Frequency</b>	Pins 1-2, all other open.	1200 kHz (Min.)
<b>Primary Leakage</b>	Pins 1-2, with leads FL1-FL2 shorted, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	9.0 μH (Max.)

### 8.3 Material List

Item	Description
[1]	Core: RM8, TDK-PC45; or equivalent. Gapped ALG: 213nH/T <sup>2</sup> .
[2]	Bobbin: RM8, Vertical, 12 pins (6/6), in-line, PI#: 25-00041-00; or Equivalent.
[3]	Magnet Wire: #25 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #32 AWG, Double Coated.
[6]	Magnet Wire: #19 AWG, Triple Insulated Wire.
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9.0 mm Wide.
[8]	Bus Wire: #26 AWG, Alpha Wire, Tinned Copper; or Equivalent.
[9]	Clip: Epcos, Clamp RM8, MF#: B65812A2203X; or Equivalent.
[10]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 27.5 mm x 58.0 mm.
[11]	Varnish: Dolph BC-359; or Equivalent.

### 8.4 Transformer Build Diagram

- WD6: 2<sup>nd</sup> Primary**      17T – #25 AWG
- WD5: Shield2**            9T – 4 x #32 AWG
- WD4: Secondary**        5T – # 21AWG\_TW
- WD3: Shield 1**        14T – 2 x #33 AWG  
*(wound interleave with...)*
- WD2: Bias**              14T – #33 AWG
- WD1: 1st Primary**      32T - #25 AWG

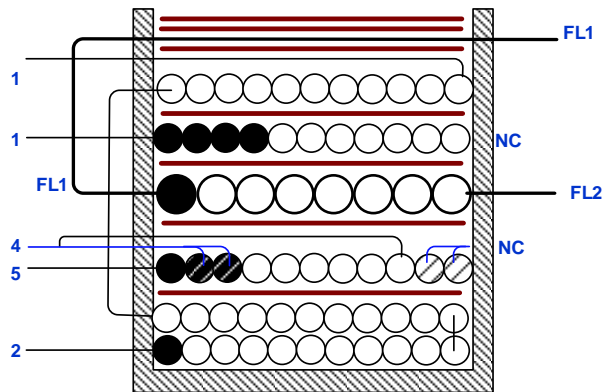


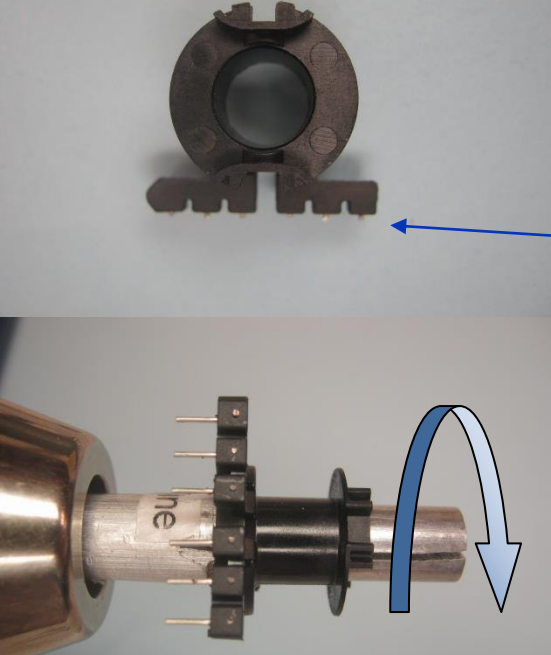
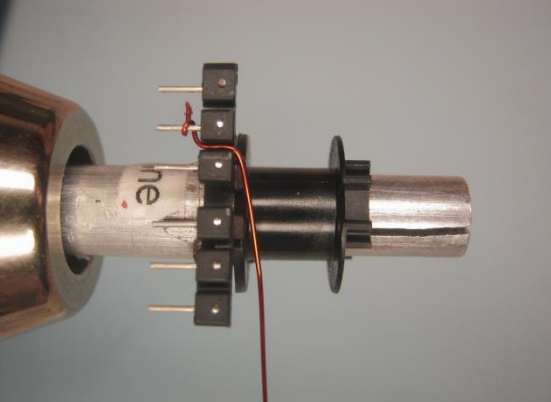
Figure 16 – Transformer Build Diagram.

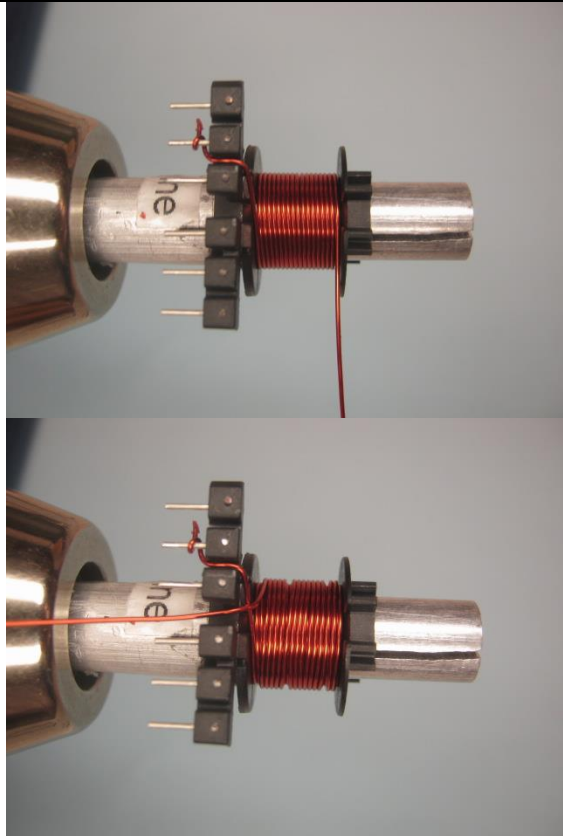
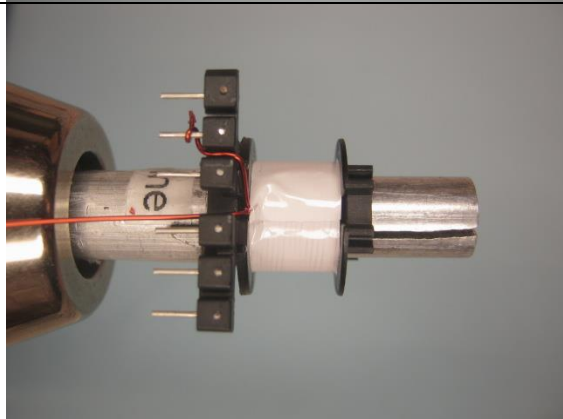
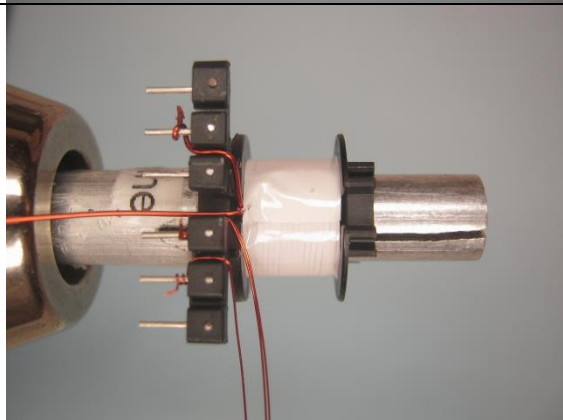
### 8.5 Transformer Construction

<b>Winding Preparation</b>	Trim off the secondary bottom flange and cut short all side pins of bobbin Item [2]. (see picture below). Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for purpose of these instructions.
<b>WD1 1<sup>st</sup> Primary</b>	Start at pin 2, wind 32 turns of wire Item [3] in 2 layers, with tight tension, from left to right then right to left. At the last turn, exit the wire; leave floating enough length for WD6-2 <sup>nd</sup> Primary.
<b>Insulation</b>	1 layer of tape Item [7].
<b>WD2 Bias &amp; WD3 Shield 1</b>	Start at pin 5 with single wire Item [4] for Bias winding, and pin 4 with 2 wires also Item [4] for Shield1 winding. Wind all 3 wires in parallel 14 turns from left to right. At the last turn, bring the single wire back to the left and terminate at pin 4 for Bias winding, and cut short 2 wires No-connect for Shield 1 winding.
<b>Insulation</b>	1 layer of tape Item [7].
<b>WD4 Secondary</b>	Start from left slot of secondary side of bobbin, use single wire Item [6], leaves floating ~ 2", mark as FL1 and wind 5 turns from left right with tight tension. At the last turn exit the wires at right slot of secondary bobbin and leave floating ~ 2" and mark as FL2.
<b>Insulation</b>	1 layer of tape Item [7].
<b>WD5 Shield 2</b>	Start at pin 1, wind 9 quad-filar turns of wire Item [5], from left to right evenly. At the last turn, cut short wires as No-connect.
<b>Insulation</b>	1 layer of tape Item [7].
<b>WD6 2<sup>nd</sup> Primary</b>	Now take the wire floating from WD1, continue winding 17 turns from left to right. At the last turn bring the wire back to the left and finish at pin 1.
<b>Insulation</b>	1 layer of tape Item [8], bring wires floating FL1 to the right and add 2 layers of tape for secure windings.
<b>Finish</b>	Gap cores to get 513 μH, secure with clips Item [9] (pins of clips should be on top and cut short), and solder bus wire Item [8] to pin 4 and to top of clip. Varnish with Item [11]. Place 2 layers of tape Item [9] at bottom core and wrap up to the body of transformer. 1 layer of tap Item [8] wrap around the transformer. (See pictures below).



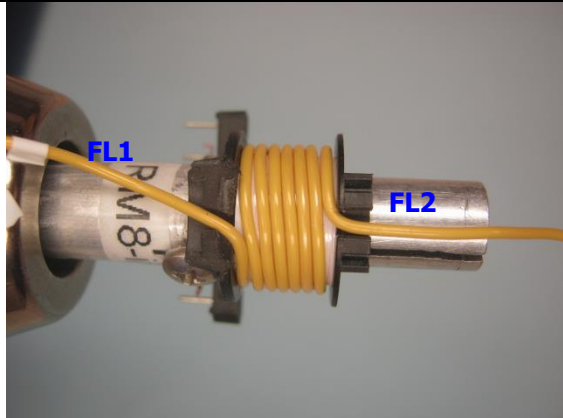

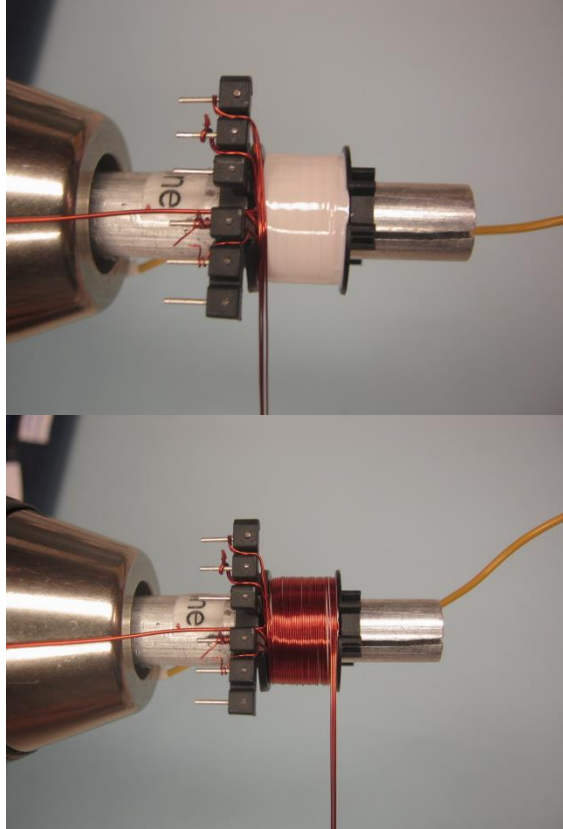
8.6 **Winding Illustrations**

<p><b>Winding Preparation</b></p>		<p>Trim off the secondary bottom flange and cut short all side pins of bobbin Item [2]. (see picture below). Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for purpose of these instructions.</p>
<p><b>WD1 1<sup>st</sup> Primary</b></p>		<p>Start at pin 2, wind 32 turns of wire Item [3] in 2 layers, with tight tension, from left to right then right to left. At the last turn, exit the wire; leave floating enough length for WD6-2<sup>nd</sup> Primary.</p>

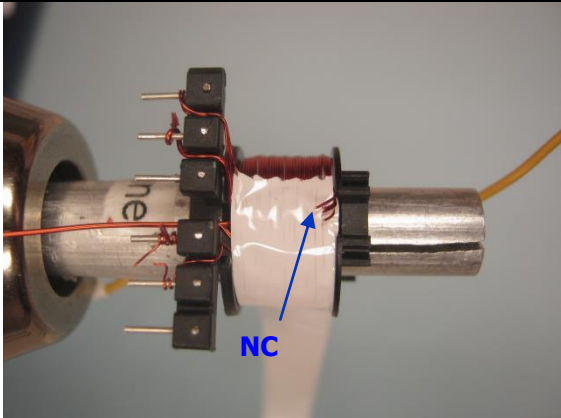
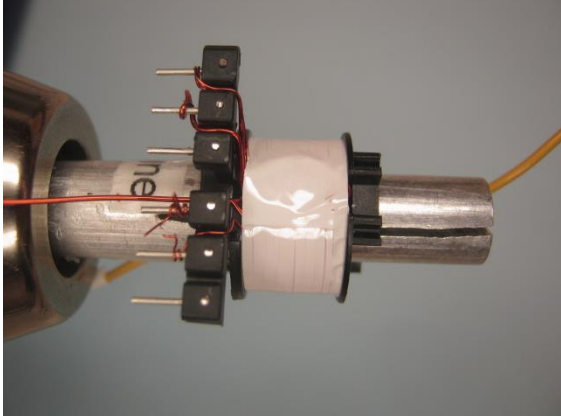
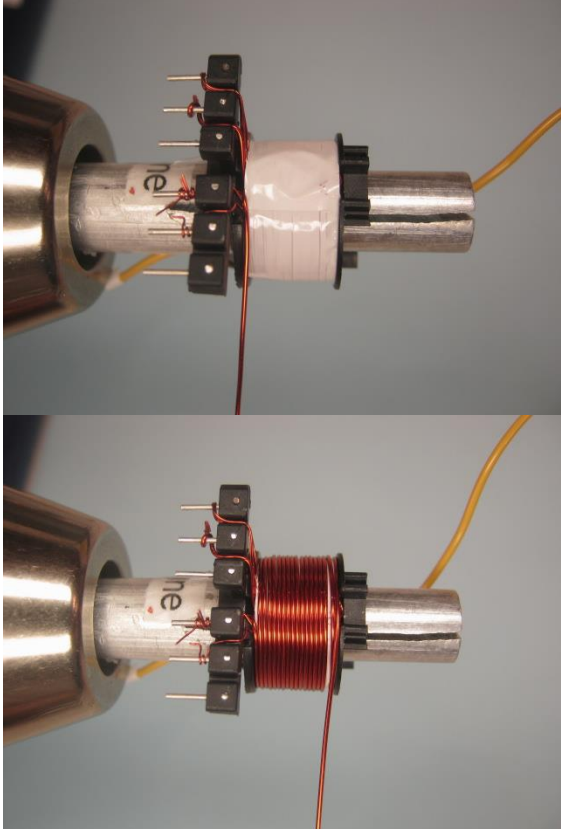
		
<p><b>Insulation</b></p>		<p>1 layer of tape Item [7].</p>
<p><b>WD2 Bias &amp; WD3 Shield 1</b></p>		<p>Start at pin 5 with single wire Item [4] for Bias winding, and pin 4 with 2 wires also Item [4] for Shield1 winding. Wind all 3 wires in parallel 14 turns from left to right. At the last turn, bring the single wire back to the left and terminate at pin 4 for Bias winding, and cut short 2 wires no-connect for Shield 1 winding.</p>

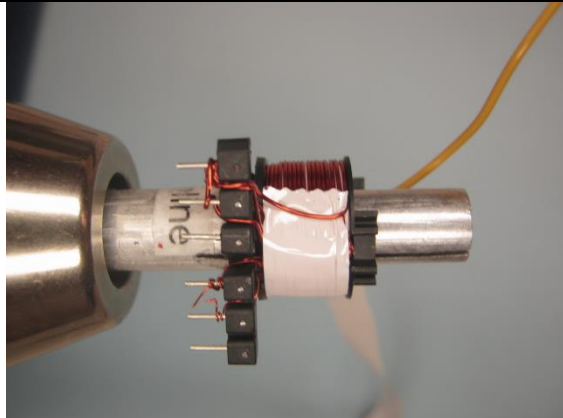
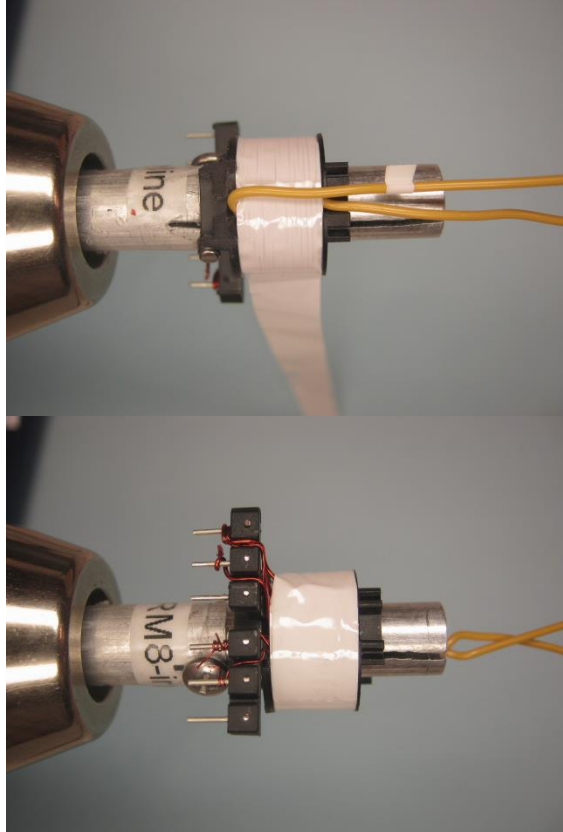
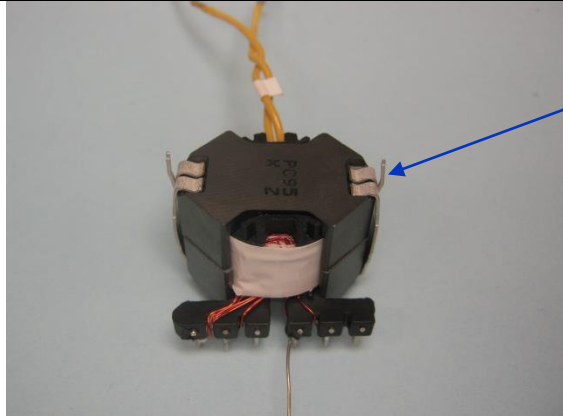


<p><b>Insulation</b></p>		<p>1 layer of tape Item [7].</p>
<p><b>WD4 Secondary</b></p>		<p>Start from left slot of secondary side of bobbin, use single wire Item [6], leaves floating ~2", mark as FL1 and wind 5 turns from left right with tight tension. At the last turn exit the wires at right slot of secondary bobbin and leave floating ~2" and mark as FL2.</p>

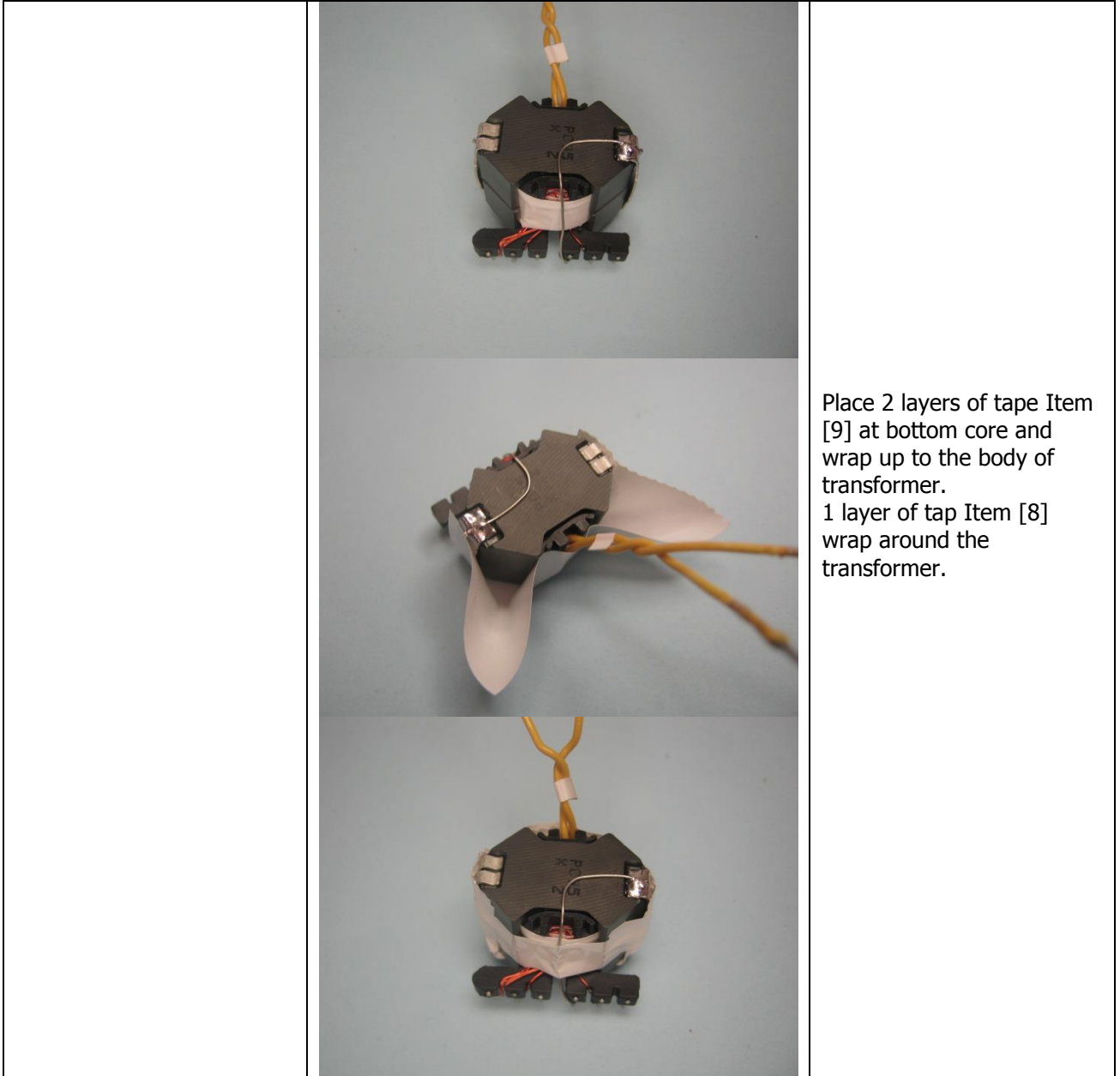
		
<p><b>Insulation</b></p>		<p>1 layer of tape Item [7].</p>
<p><b>WD5 Shield 2</b></p>		<p>Start at pin 1, wind 9 quad-filar turns of wire Item [5], from left to right evenly. At the last turn, cut short wires as No-connect.</p>



		
<p><b>Insulation</b></p>		<p>1 layer of tape Item [7].</p>
<p><b>WD6 2<sup>nd</sup> Primary</b></p>		<p>Now take the wire floating from WD1, continue winding 17 turns from left to right. At the last turn bring the wire back to the left and finish at pin 1.</p>

		
<p><b>Insulation</b></p>		<p>1 layer of tape Item [8], bring wires floating FL1 to the right and add 2 layers of tape for secure windings.</p>
<p><b>Finish</b></p>		<p>Gap cores to get 513 <math>\mu</math>H, secure with clips Item [9] (pins of clips should be on top and cut short), and solder bus wire Item [8] to pin 4 and to top of clip. Varnish with Item [11].</p>

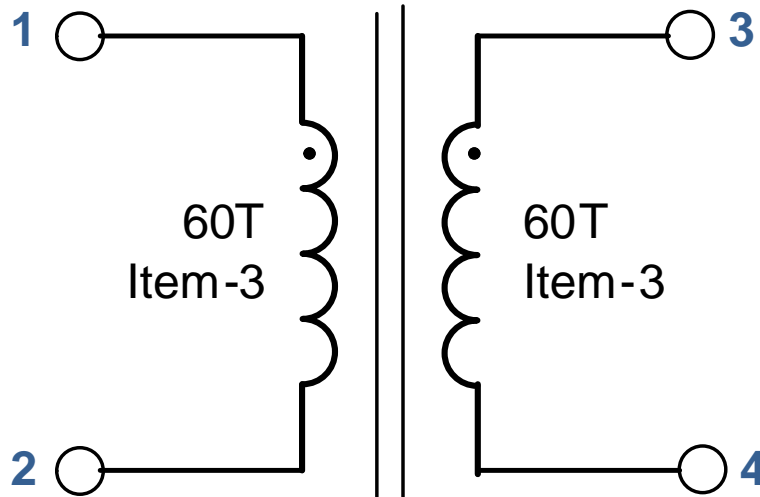




## 9 Common Mode Choke Specifications

### 9.1 34 mH Common Mode Choke (L1)

#### 9.1.1 Electrical Diagram



**Figure 17** – Inductor Electrical Diagram.

#### 9.1.2 Electrical Specifications

<b>Winding Inductance</b>	Pin 1-pin 2 (pin 3-pin 4), all other windings open, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	34 mH, ±20%
<b>Winding Leakage Inductance</b>	Short pin 2 and pin 4, then measure between pin 1 and pin 3.	>80 μH

#### 9.1.3 Material List

Item	Description
[1]	Toroidal Core: Encom T16-10-7C, PI#: 32-00343-00.
[2]	Margin Tape: Polyester Web, 3M 44 or Equivalent, 3.2 mm Wide; or Equivalent.
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

9.1.4 Illustrations



Figure 18 – L1 Front View.

9.1.5 Winding Instructions

Item	Description
[1]	Put margin tape Item [2] into the toroid Item [1] to make 2 equal sections.
[2]	Use ~4½ ft of Item [3], start as pin 1 for the 1st section, wind 24 turns for 1st layer, then wind 12 turns for each layer: 2nd, 3rd, and 4th, and end as pin 2 (see illustrations).
[3]	Do the same for another 2nd section of toroid but wind symmetrically, start as pin 3 and end at pin 4.
[4]	Varnish Item [4].
[5]	Note: all wires should be left ~1.5" floating. Make sure to label each terminal.

## 10 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_042018; Rev.1.0; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
<b>2</b>	<b>APPLICATION VARIABLES</b>					
3	VAC_MIN			85	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	82.0		82.0	uF	Input capacitance
<b>9</b>	<b>SETPOINT 1</b>					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.250		2.250	A	Output current 1
12	POUT1			45.00	W	Output power 1
13	EFFICIENCY1	0.89		0.89		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
<b>16</b>	<b>SETPOINT 2</b>					
17	VOUT2	15.00		15.00	V	Output voltage 2
18	IOUT2	3.000		3.000	A	Output current 2
19	POUT2			45.00	W	Output power 2
20	EFFICIENCY2	0.90		0.90		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
<b>23</b>	<b>SETPOINT 3</b>					
24	VOUT3	9.00		9.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			27.00	W	Output power 3
27	EFFICIENCY3	0.89		0.89		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
<b>30</b>	<b>SETPOINT 4</b>					
31	VOUT4	5.00		5.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			15.00	W	Output power 4
34	EFFICIENCY4	0.86		0.86		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
<b>37</b>	<b>SETPOINT 5</b>					
38	VOUT5	3.00		3.00	V	Output voltage 5
39	IOUT5	3.000		3.000	A	Output current 5
40	POUT5			9.00	W	Output power 5
41	EFFICIENCY5	0.84		0.84		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
<b>44</b>	<b>SETPOINT 6</b>					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
<b>51</b>	<b>SETPOINT 7</b>					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
<b>58</b>	<b>SETPOINT 8</b>					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8



62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8
<b>65</b>	<b>SETPOINT 9</b>					
66	VOOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
<b>72</b>	<b>VOLTAGE_CDC</b>	<b>0.000</b>		<b>0.000</b>	<b>V</b>	<b>Cable drop compensation desired at full current</b>
<b>76</b>	<b>PRIMARY CONTROLLER SELECTION</b>					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
79	VDRAIN_BREAKDOWN	650		650	V	Device breakdown voltage
80	DEVICE_GENERIC	Auto		INN33X8		Device selection
81	DEVICE_CODE			INN3368C		Device code
82	PDEVICE_MAX			50	W	Device maximum power capability
83	RDSON_25DEG			0.99	$\Omega$	Primary MOSFET on-time resistance at 25°C
84	RDSON_100DEG			1.53	$\Omega$	Primary MOSFET on-time resistance at 100°C
85	ILIMIT_MIN			1.683	A	Primary MOSFET minimum current limit
86	ILIMIT_TYP			1.850	A	Primary MOSFET typical current limit
87	ILIMIT_MAX			2.017	A	Primary MOSFET maximum current limit
88	VDRAIN_ON_MOSFET			0.89	V	Primary MOSFET on-time voltage drop
89	VDRAIN_OFF_MOSFET			583.31	V	Peak drain voltage on the primary MOSFET during turn-off
<b>93</b>	<b>WORST CASE ELECTRICAL PARAMETERS</b>					
94	FSWITCHING_MAX	79000	Info	79000	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
95	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
96	VMIN			82.75	V	Valley of the rectified minimum input AC voltage at full load
97	KP			0.734		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			CCM		Mode of operation
99	DUTYCYCLE			0.631		Primary MOSFET duty cycle
100	TIME_ON			11.89	us	Primary MOSFET on-time
101	TIME_OFF			4.83	us	Primary MOSFET off-time
102	LPRIMARY_MIN			477.5	$\mu$ H	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			502.7	$\mu$ H	Typical primary magnetizing inductance
104	LPRIMARY_TOL			5.0		Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			527.8	$\mu$ H	Maximum primary magnetizing inductance
<b>107</b>	<b>PRIMARY CURRENT</b>					
108	Iavg_PRIMARY			0.584	A	Primary MOSFET average current
109	IPEAK_PRIMARY			1.873	A	Primary MOSFET peak current
110	IPEDESTAL_PRIMARY			0.433	A	Primary MOSFET current pedestal
111	IRIPPLE_PRIMARY			1.873	A	Primary MOSFET ripple current
112	IRMS_PRIMARY			0.854	A	Primary MOSFET RMS current

114 SECONDARY CURRENT						
115	IPEAK_SECONDARY			13.114	A	Secondary MOSFET peak current
116	IPEDESTAL_SECONDARY			3.029	A	Secondary MOSFET pedestal current
117	IRMS_SECONDARY			5.280	A	Secondary MOSFET RMS current
118	IRIPPLE_CAP_OUT			4.346	A	Output capacitor ripple current
122 TRANSFORMER CONSTRUCTION PARAMETERS						
123 CORE SELECTION						
124	CORE	RM8	Info	RM8		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME			PC95RM08 Z		Core code
126	AE			64.0	mm <sup>2</sup>	Core cross sectional area
127	LE			38.0	mm	Core magnetic path length
128	AL			5290	nH	Ungapped core effective inductance per turns squared
129	VE			2430	mm <sup>3</sup>	Core volume
130	BOBBIN NAME			B-RM08-V		Bobbin name
131	AW			30.0	mm <sup>2</sup>	Bobbin window area
132	BW			8.80	mm	Bobbin width
133	MARGIN			0.0	mm	Bobbin safety margin
135 PRIMARY WINDING						
136	NPRIMARY			49		Primary winding number of turns
137	BPEAK			3475	Gauss	Peak flux density
138	BMAX			3112	Gauss	Maximum flux density
139	BAC			1552	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			209	nH	Typical gapped core effective inductance per turns squared
141	LG			0.369	mm	Core gap length
142	LAYERS_PRIMARY			3		Primary winding number of layers
143	AWG_PRIMARY	25		25		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.518	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.455	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			375.4	Cmils/A	Primary winding wire CMA
148 SECONDARY WINDING						
149	NSECONDARY			7		Secondary winding number of turns
150	AWG_SECONDARY			19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			243.9	Cmils/A	Secondary winding wire CMA
155 BIAS WINDING						
156	NBIAS			22		Bias winding number of turns
160 PRIMARY COMPONENTS SELECTION						
161 LINE UNDERVOLTAGE						
162	BROWN-IN REQUIRED	75.00		75.00	V	Required line brown-in threshold
163	RLS			3.74	MΩ	Connect two 1.87 MΩ resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			74.98	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			67.82	V	Actual brown-out threshold using standard resistors
167 LINE OVERVOLTAGE						
168	OVERVOLTAGE_LINE		Warning	312.52	V	The device voltage stress will be higher than 90% of the breakdown voltage when overvoltage is triggered
170 BIAS WINDING						



171	VBIAS			9.00	V	Rectified bias voltage at the lowest output setpoint
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			176.61	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			4.70	uF	BPP pin capacitor
<b>179</b>	<b>SECONDARY COMPONENTS SELECTION</b>					
<b>180</b>	<b>RECTIFIER</b>					
181	VDRAIN_OFF_SRFET			73.33	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	Auto		SiR878AD P		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			18.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
<b>188</b>	<b>VARIABLE OUTPUTS ANALYSIS</b>					
<b>189</b>	<b>TOLERANCE CORNER</b>					
190	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
191	CORNER_ILIMIT	TYP		1.850	A	Current limit corner to be evaluated
192	CORNER_LPRIMARY	TYP		502.7	uH	Primary inductance corner to be evaluated
<b>194</b>	<b>SETPOINT SELECTION</b>					
195	SETPOINT	5		5		Select the setpoint which needs to be evaluated
196	FSWITCHING			23795.3	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
197	VOR			21.6	V	Voltage reflected to the primary winding when the primary MOSFET turns off
198	VMIN			111.41	V	Valley of the minimum input AC voltage
199	KP			1.212		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			DCM		Mode of operation
201	DUTYCYCLE			0.138		Primary MOSFET duty cycle
202	TIME_ON			5.80	us	Primary controller's maximum on-time
203	TIME_OFF			36.23	us	Primary controller's minimum off-time
<b>205</b>	<b>PRIMARY CURRENT</b>					
206	I AVG_PRIMARY			0.089	A	Primary MOSFET average current
207	IPEAK_PRIMARY			1.284	A	Primary MOSFET peak current
208	IPEDESTAL_PRIMARY			0.000	A	Primary MOSFET current pedestal
209	IRIPPLE_PRIMARY			1.284	A	Primary MOSFET ripple current
210	IRMS_PRIMARY			0.275	A	Primary MOSFET RMS current
<b>212</b>	<b>SECONDARY CURRENT</b>					
213	IPEAK_SECONDARY			8.987	A	Secondary MOSFET peak current
214	IPEDESTAL_SECONDARY			0.000	A	Secondary MOSFET pedestal current
215	IRMS_SECONDARY			4.376	A	Secondary MOSFET RMS current
216	IRIPPLE_CAP_OUT			3.185	A	Output capacitor ripple current
<b>218</b>	<b>MAGNETIC FLUX DENSITY</b>					
219	BPEAK			3035	Gauss	Peak flux density
220	BMAX			2058	Gauss	Maximum flux density
221	BAC			1029	Gauss	AC flux density (0.5 x Peak to Peak)

**Notes:**

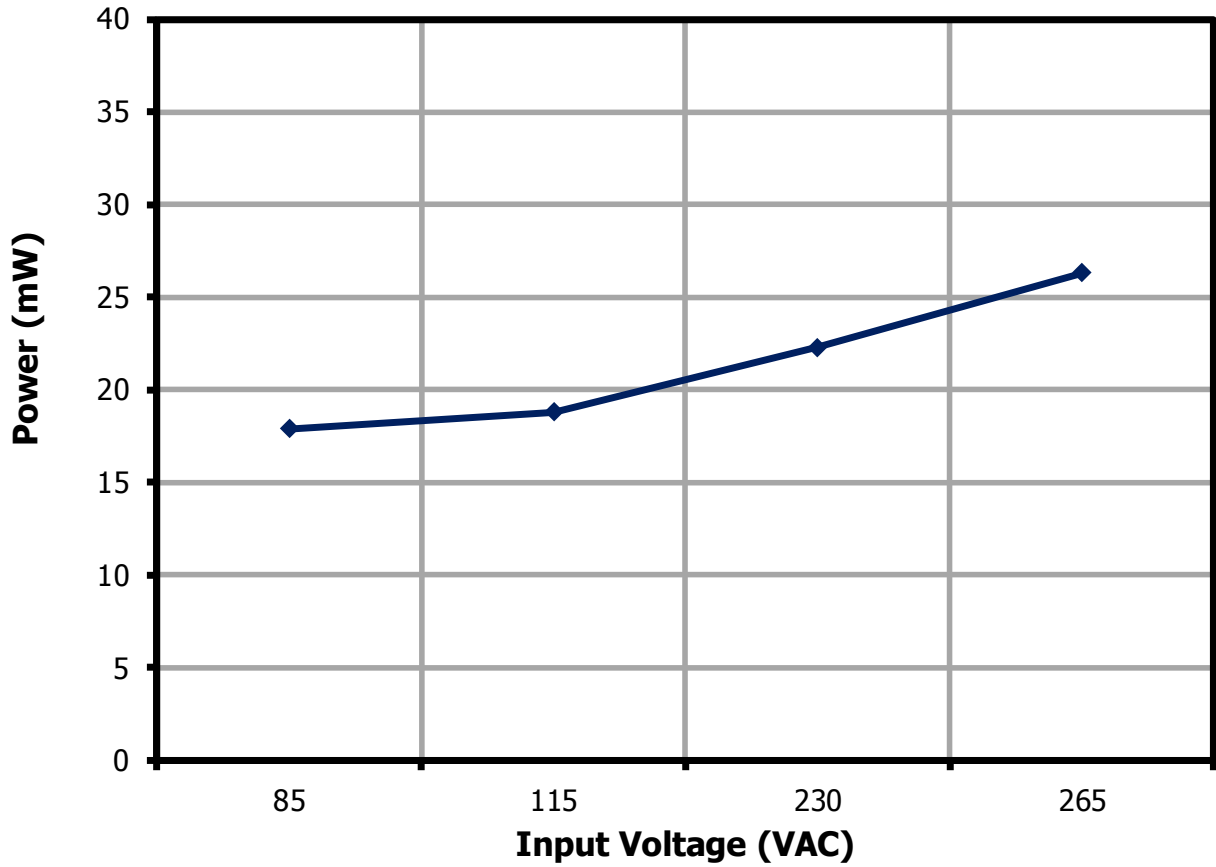
1. (Fswitching) Info1: Audible Noise results when the device is operating typically between 7-11 kHz region. The audible noise reduction engine inside InnoSwitch3-Pro IC prevents the device from switching at these frequencies. Hence, this alert can be ignored.
2. (RM8 Core) Info1: We find that there is sufficient space on the core for all windings on the prototype. This warning can be ignored.
3. (Overvoltage Line) Warning: We find that there is sufficient margin above the datasheet specified breakdown voltage at normal operating voltage of 265 VAC. This warning is for abnormal operating conditions and can be ignored.





## 11 Performance Data

### 11.1 *No-Load Input Power at 5 VOUT*



**Figure 19** – No-Load Input Power vs. Input Line Voltage, Room Temperature.



11.1.1 Average Efficiency Requirements

Test	Power (W)	Average	Average	10% Load	Average	Average	10% Load
Model		<6 V Voltage	<6 V Voltage	<6 V Voltage	>6 V Voltage	>6 V Voltage	>6 V Voltage
Regulation		New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
	9.9	78.6%	78.9%	69.7%			
	15	81.4 %	81.8%	72.5%			
	27				86.6%	87.3%	77.3%
	45				87.72%	88.85%	78.85%

11.1.2 Average Efficiency Summary

Power (W)	V <sub>OUT</sub> (V)	Average		10% Load	
		115 VAC	230 VAC	115 VAC	230 VAC
9.9	3.3	86.60	84.30	82.82	76.57
15	5	88.87	88.09	85.99	82.41
27	9	89.65	89.69	84.07	80.54
45	15	89.70	90.38	84.71	83.17
	20	89.13	89.79	81.22	79.75



## 11.2 **Average Efficiency (On Board) and 10% Load at 115 VAC Input**

### 11.2.1 3.3 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	10.07	86.20	
75	7.51	86.88	
50	4.95	87.14	86.60
25	2.40	86.17	
10	0.91	82.82	

### 11.2.2 5.0 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	15.18	88.25	
75	11.26	88.92	
50	7.57	89.34	88.87
25	3.65	88.98	
10	1.31	85.99	

### 11.2.3 9.0 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	27.70	89.36	
75	21.04	89.82	
50	13.45	90.05	89.65
25	5.91	89.38	
10	1.72	84.07	

### 11.2.4 15.0 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	45.24	89.75	
75	33.98	89.98	
50	22.65	89.90	89.70
25	11.32	89.18	
10	4.54	84.71	

## 11.2.5 20.0 V Output

% Load	P <sub>OUT</sub> (W)	Efficiency (%)	Average Efficiency (%)
100	45.04	89.82	
75	33.82	89.79	
50	22.53	89.46	89.13
25	11.23	87.47	
10	4.51	81.22	

11.3 **Average Efficiency (On Board) at 230 VAC Input and 10% Load**

## 11.3.1 3.3 V Output

% Load	P <sub>OUT</sub> (W)	Efficiency (%)	Average Efficiency (%) [100%-25%]
100	10.13	85.47	
75	7.54	85.47	
50	4.97	84.75	84.20
25	2.41	81.12	
10	0.92	76.57	

## 11.3.2 5.0 V Output

% Load	P <sub>OUT</sub> (W)	Efficiency (%)	Average Efficiency (%) [100%-25%]
100	15.25	88.50	
75	11.29	88.75	
50	7.59	88.47	88.09
25	3.65	86.62	
10	1.31	82.41	

## 11.3.3 9.0 V Output

% Load	P <sub>OUT</sub> (W)	Efficiency (%)	Average Efficiency (%) [100%-25%]
100	27.81	90.25	
75	21.08	90.38	
50	13.46	90.1	89.69
25	5.91	88.03	
10	1.71	80.54	

## 11.3.4 15.0 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	45.31	90.99	
75	34.05	91.01	
50	22.67	90.62	90.38
25	11.32	88.89	
10	4.534	83.17	

## 11.3.5 20.0 V Output

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%) [100%-25%]</b>
100	45.04	91.00	
75	33.79	90.76	
50	22.52	90.08	89.79
25	11.22	87.32	
10	4.51	79.75	

### 11.4 Efficiency Across Load

#### 11.4.1 5 V Output

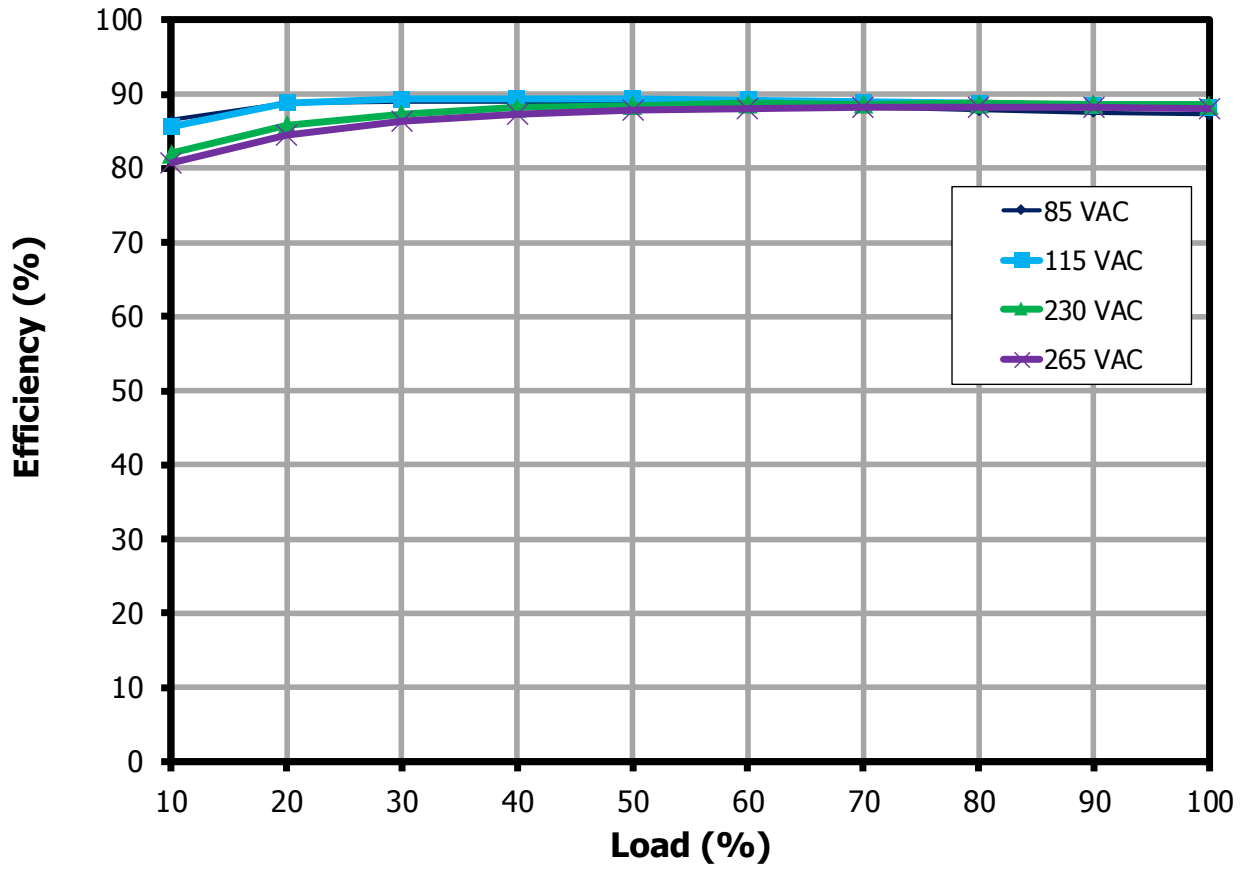


Figure 20 – 5 V Output Efficiency (%) vs. Load (%).

11.4.2 9 V Output

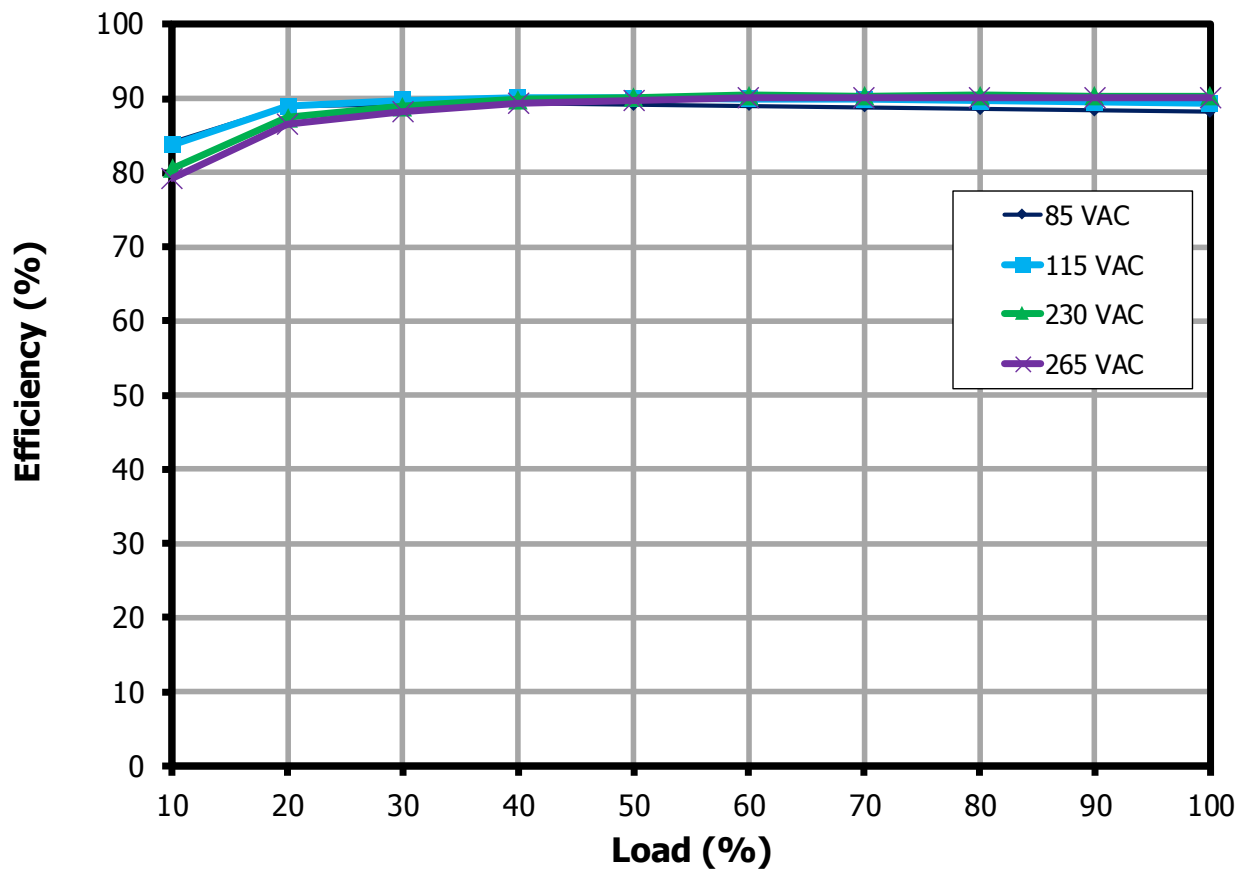


Figure 21 – 9 V Output Efficiency (%) vs. Load (%).



11.4.3 15 V Output

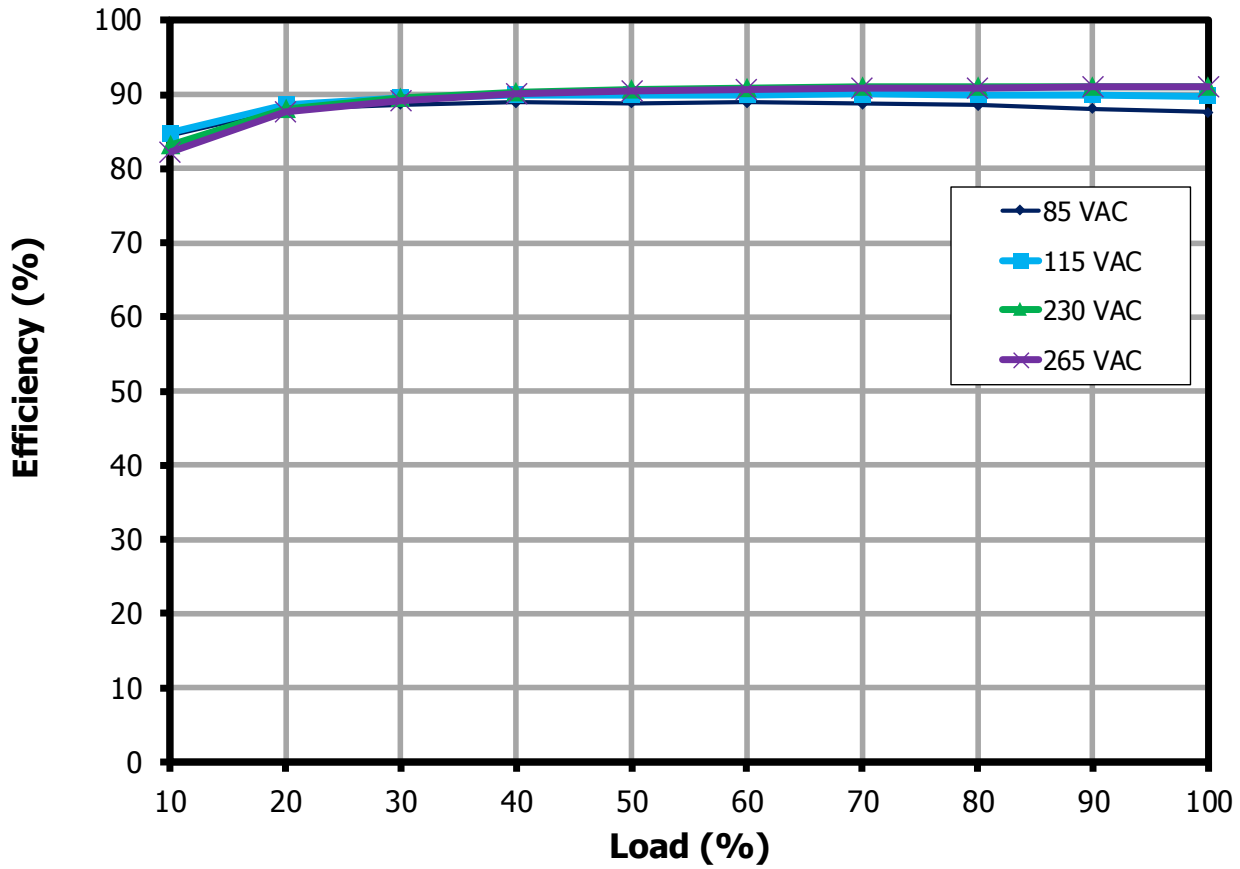


Figure 22 – 15 V Output Efficiency (%) vs. Load (%).



11.4.4 20 V Output

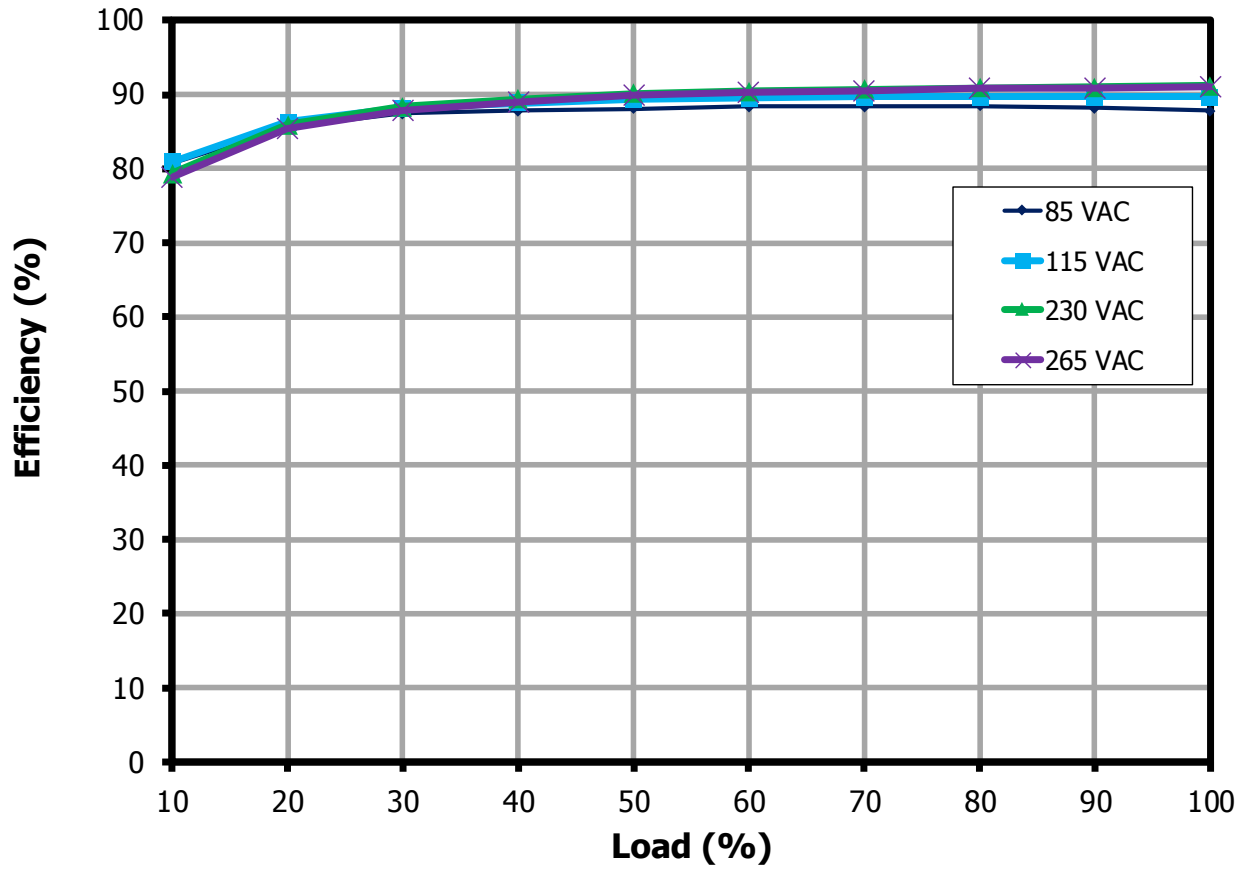
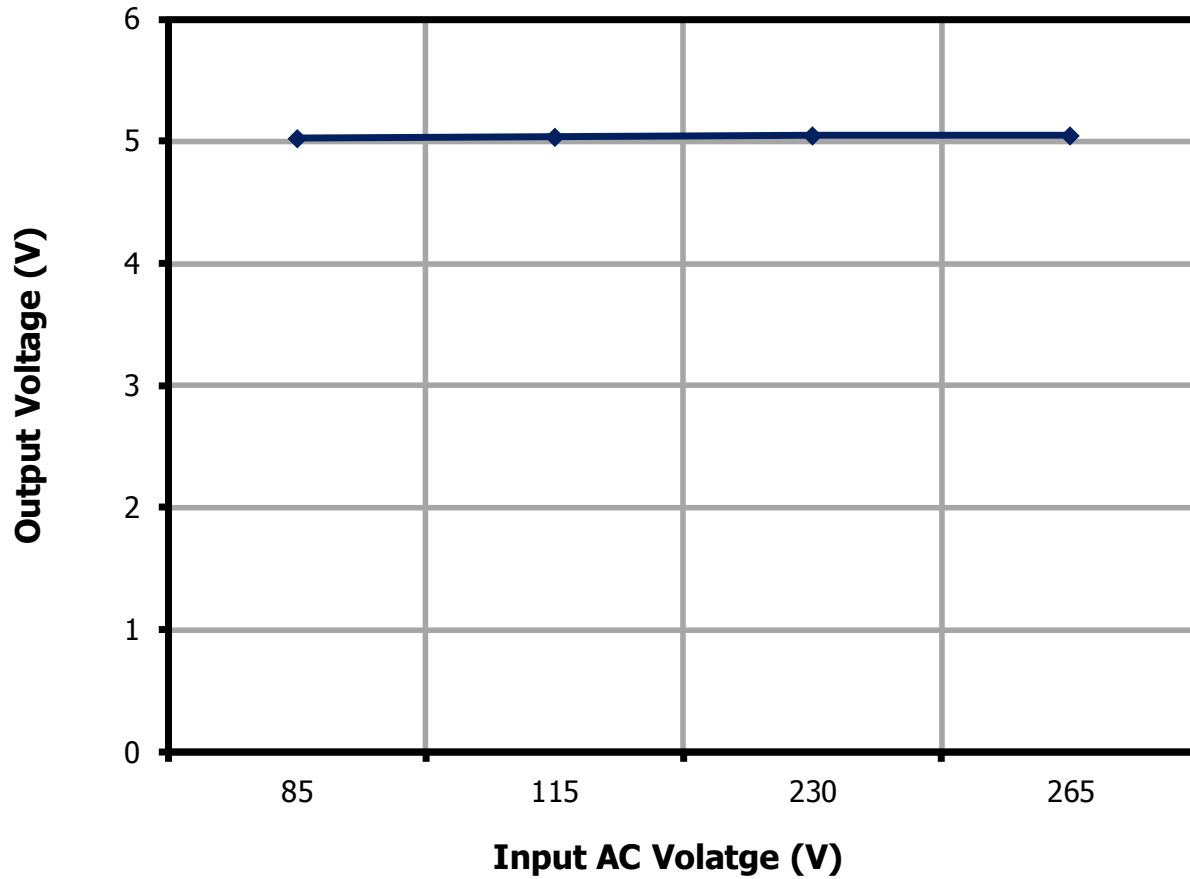


Figure 23 – 20 V Output Efficiency (%) vs. Load (%).



### 11.5 *Line Regulation (On Board)*

#### 11.5.1 5.0 V Output



**Figure 24** – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

11.5.2 9.0 V Output

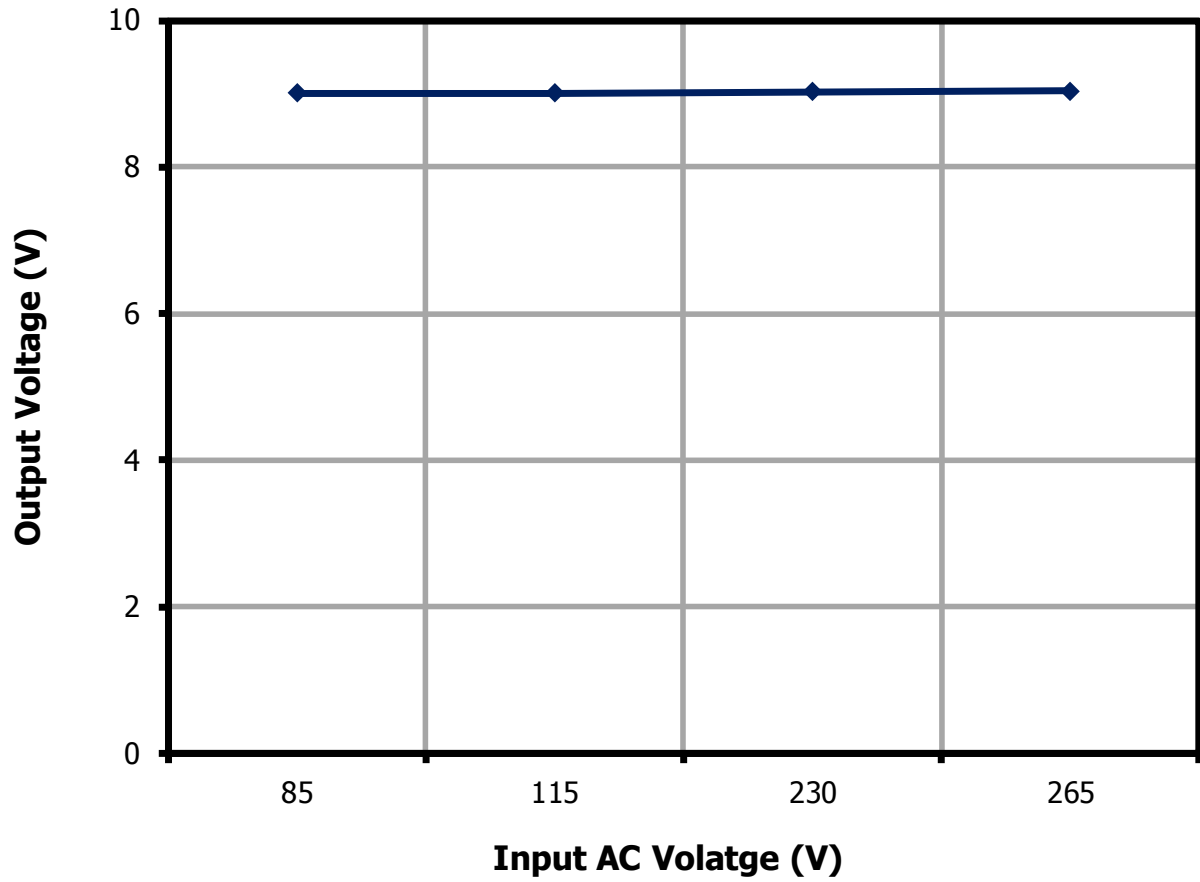


Figure 25 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.



11.5.3 15.0 V Output

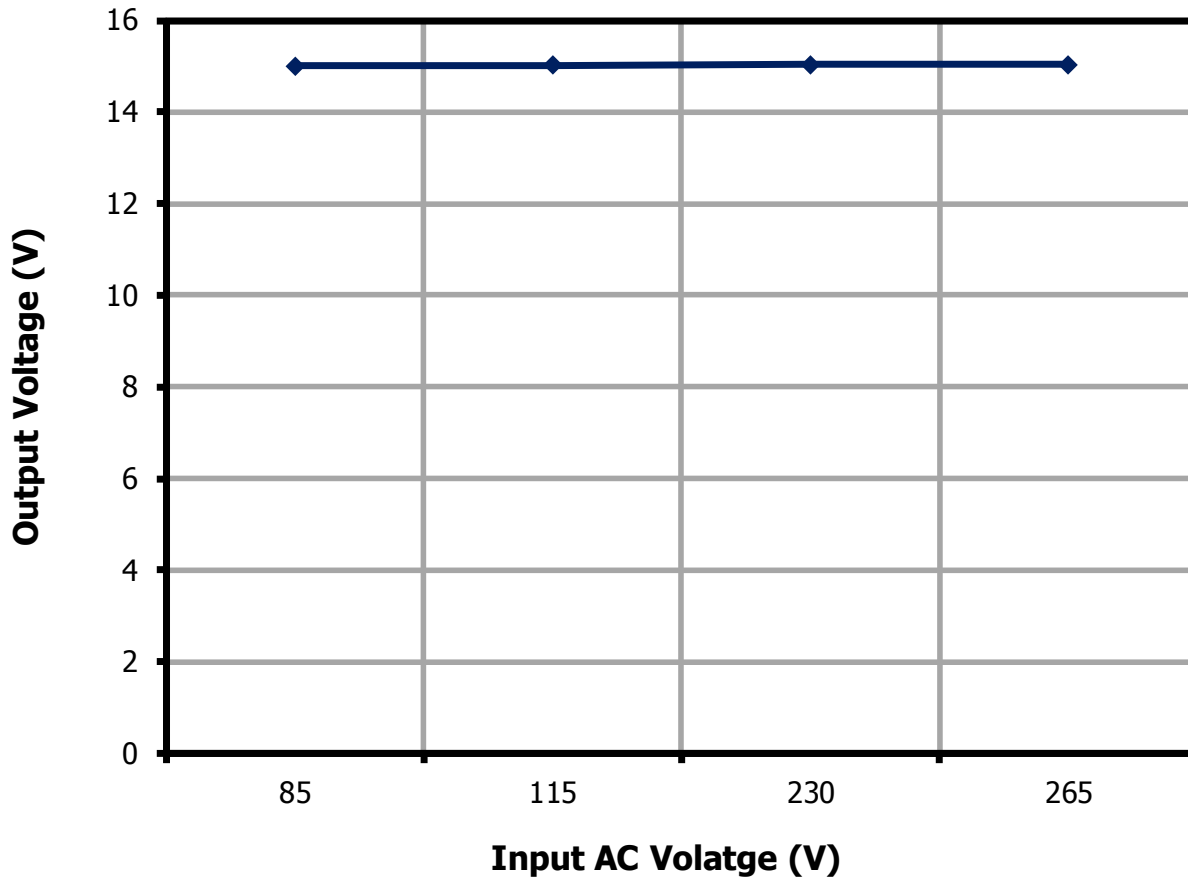
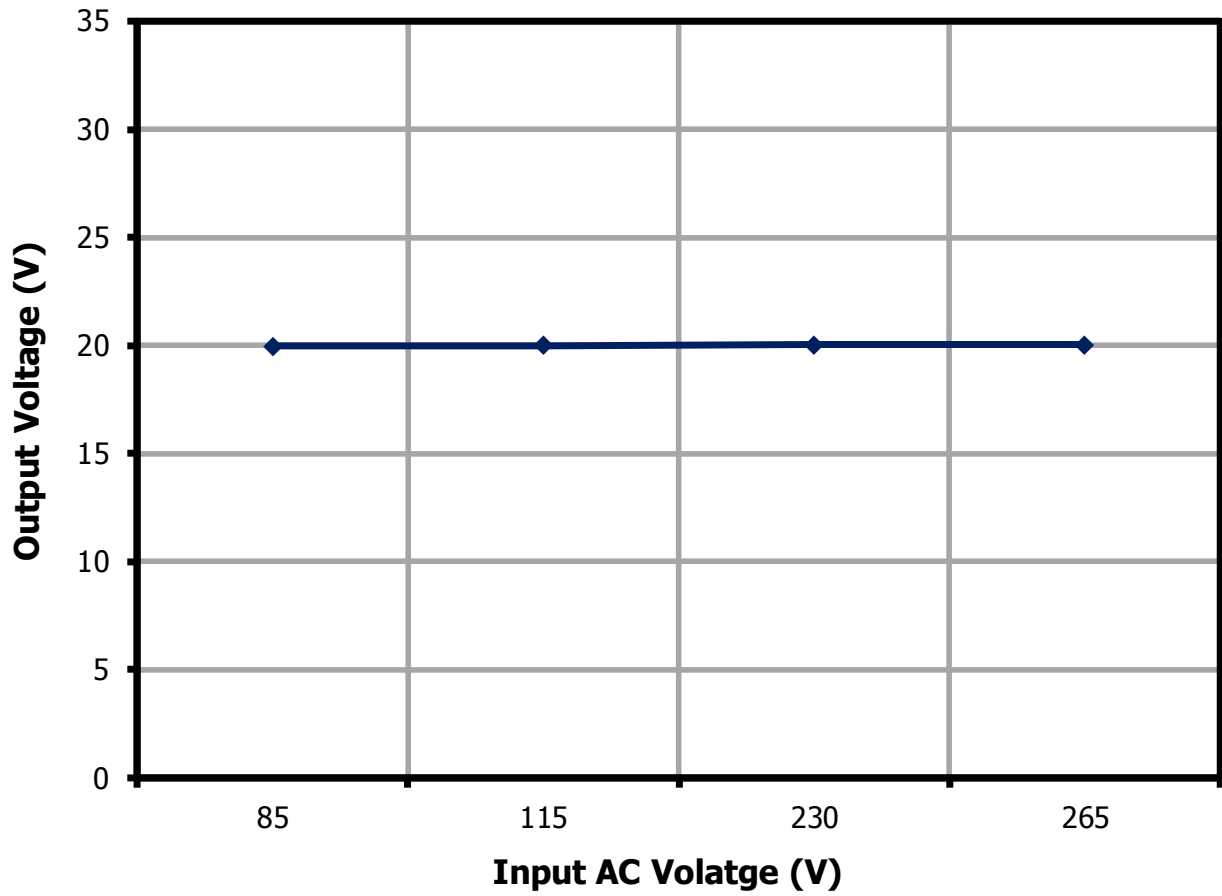


Figure 26 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

11.5.4 20.0 V Output



**Figure 27** – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.



### 11.6 Load Regulation (On Board)

#### 11.6.1 5.0 V Output

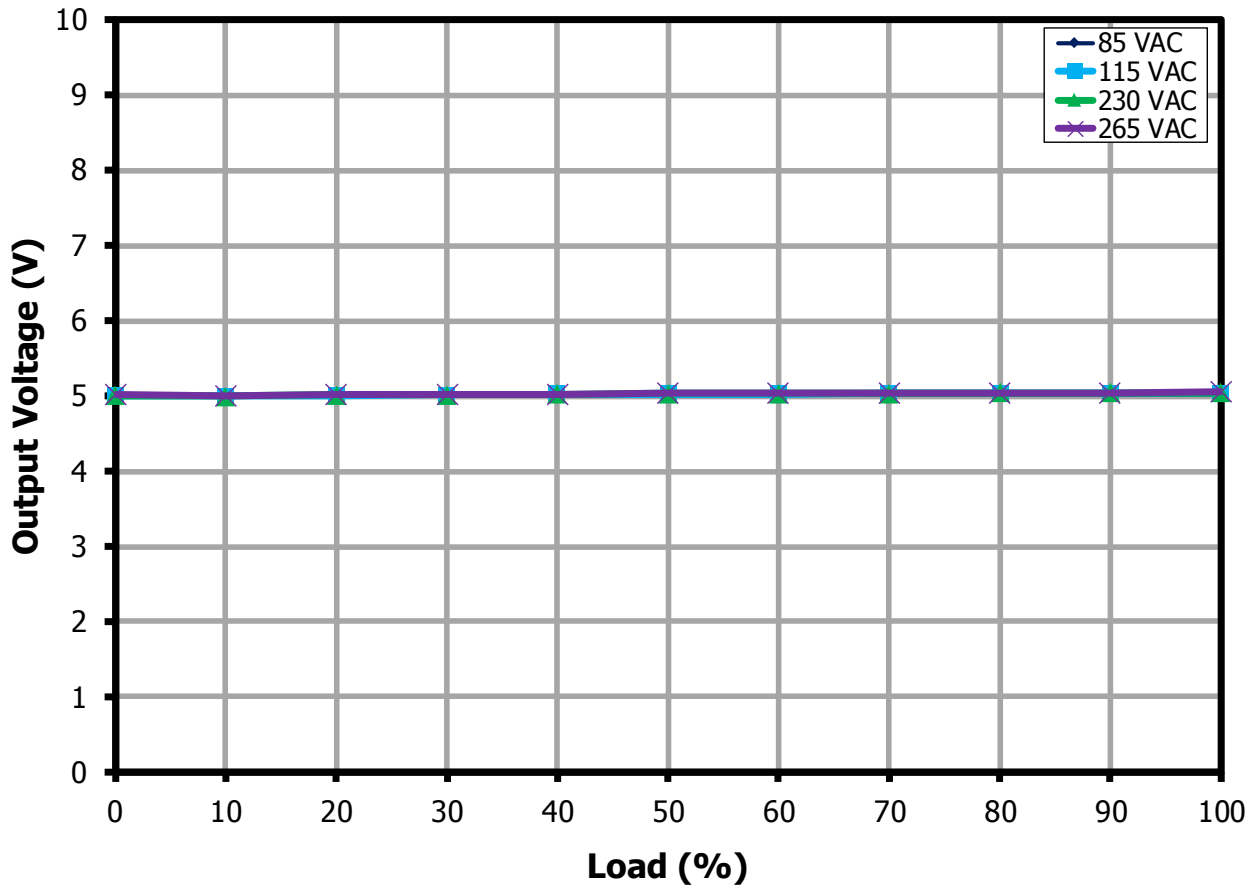


Figure 28 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

11.6.2 9.0 V Output

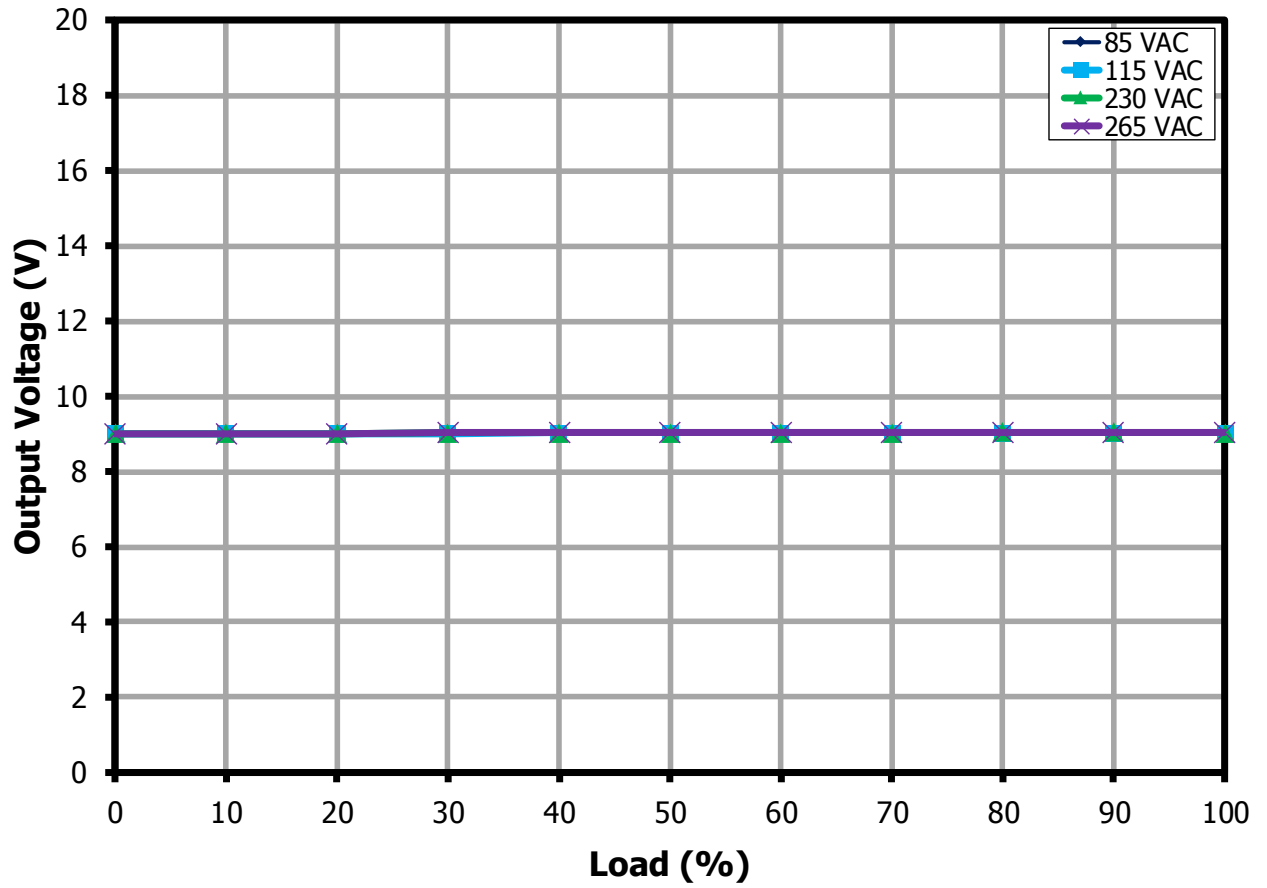
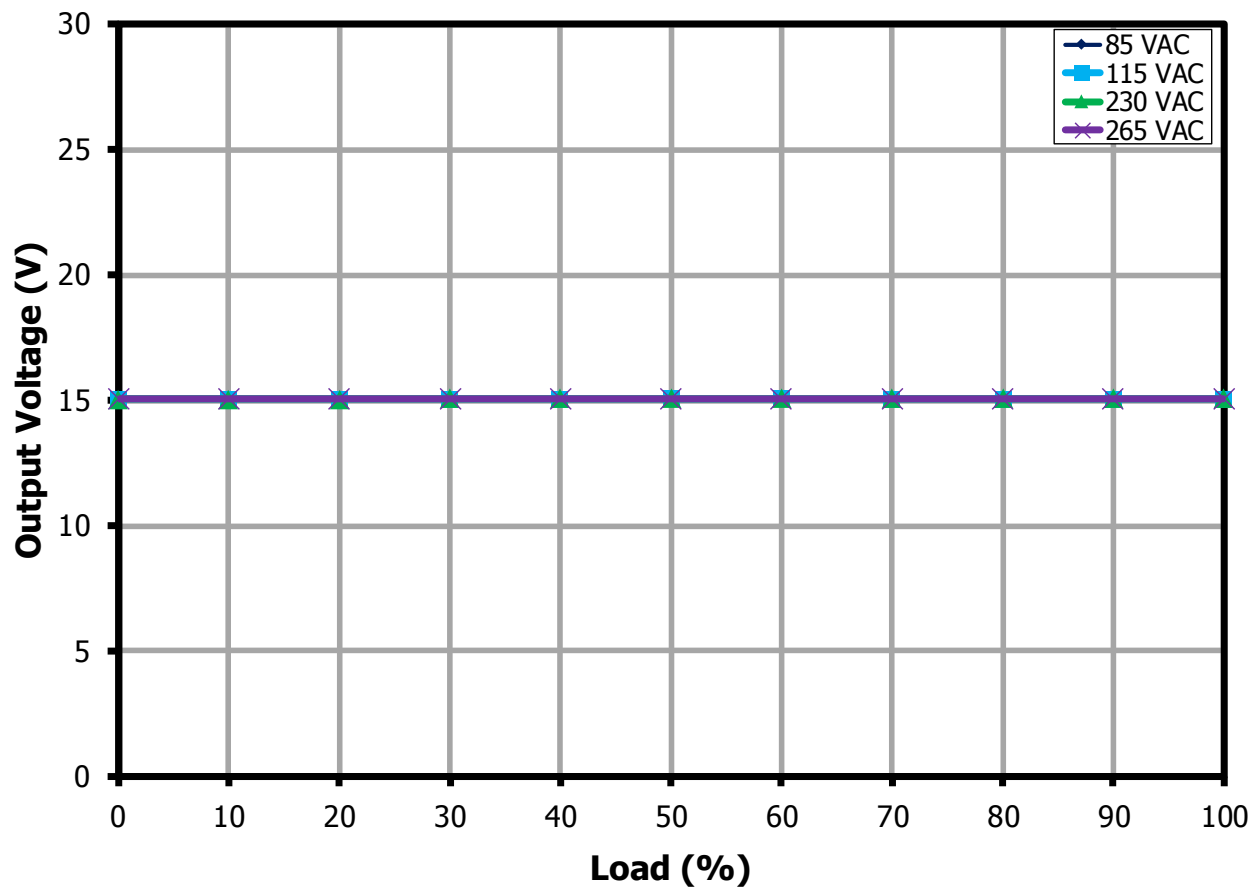


Figure 29 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.



## 11.6.3 15.0 V Output



**Figure 30** – Output Voltage vs. Output Load for 15 V Output, Room Temperature.



11.6.4 20.0 V Output

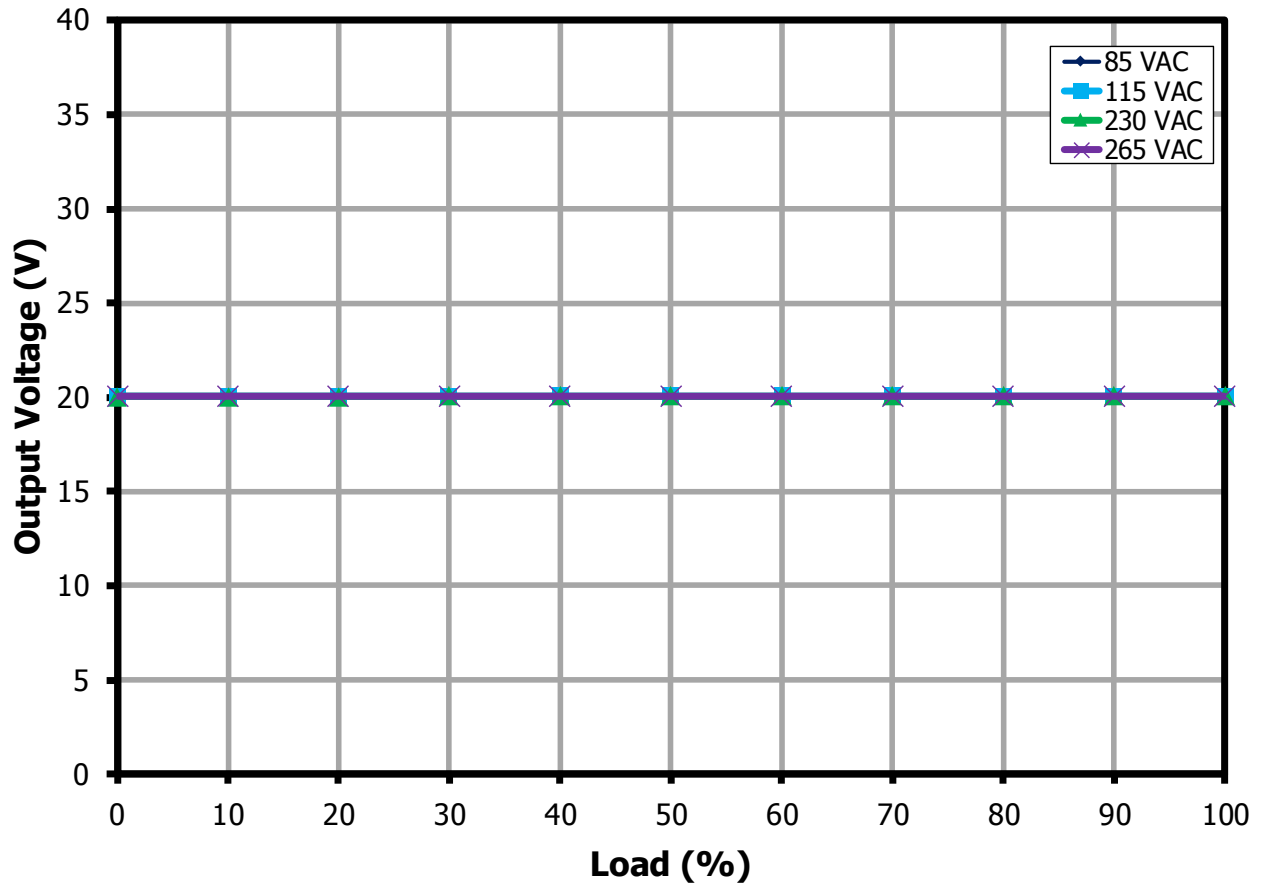


Figure 31 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

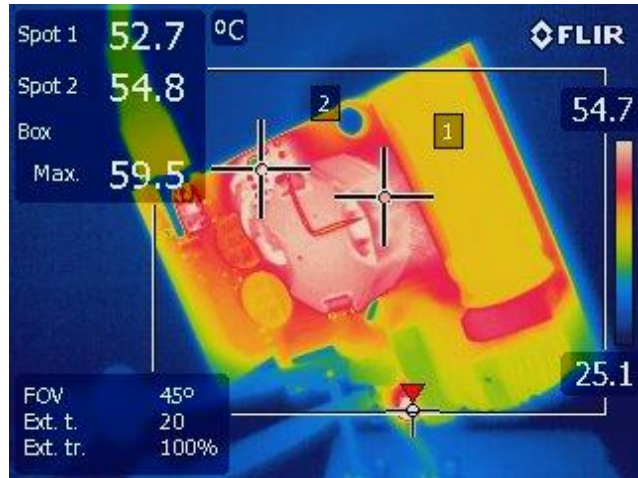


## 12 Thermal Performance in Open Case

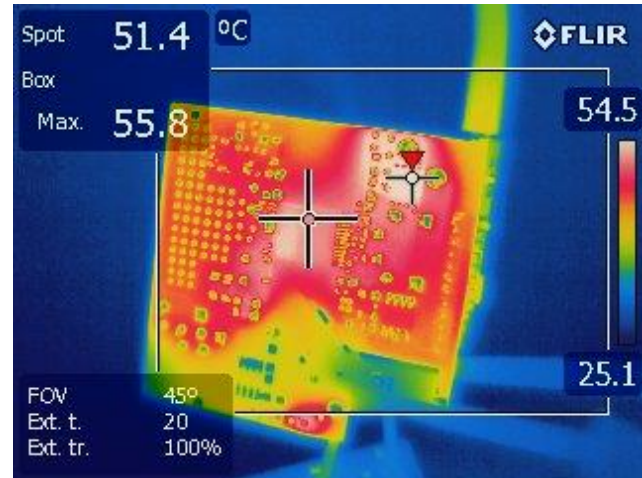
**Note:** For plastic enclosed adapters, this design requires use of a metallic heat spreader and suitable thermally conductive insulator to ensure sufficiently low temperature of the InnoSwitch-3 Pro IC and Transformer. The performance data below is for open case operation and does not use the heat spreader for cooling.

### 12.1 5 V, 3 A

#### 12.1.1 85 VAC Input

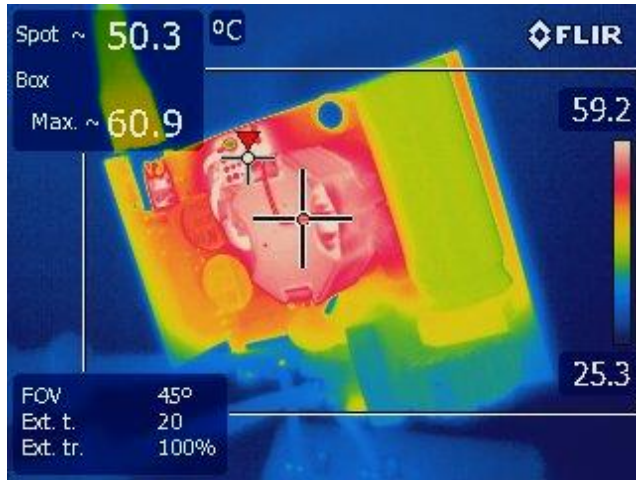


**Figure 32** – Transformer Side.  
 Ambient = 25.3 °C.  
 Thermistor = 59.5 °C.  
 Transformer = 52.7 °C.

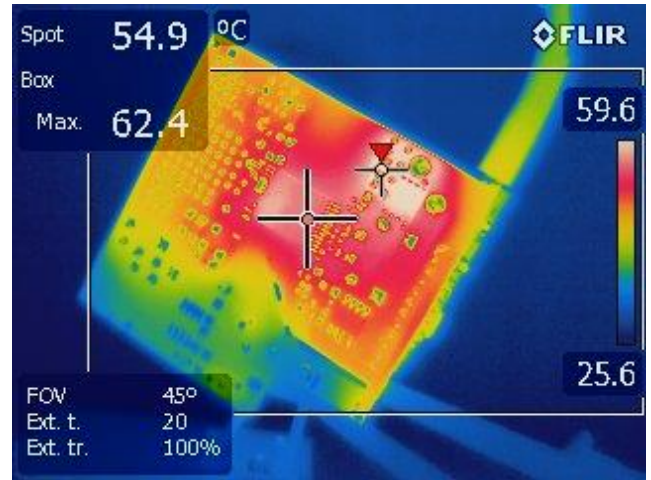


**Figure 33** – InnoSwitch3-Pro Side.  
 Ambient = 25.3 °C.  
 SR FET, Q2 = 55.8 °C.  
 InnoSwitch3-Pro = 51.4 °C.

12.1.2 265 VAC Input



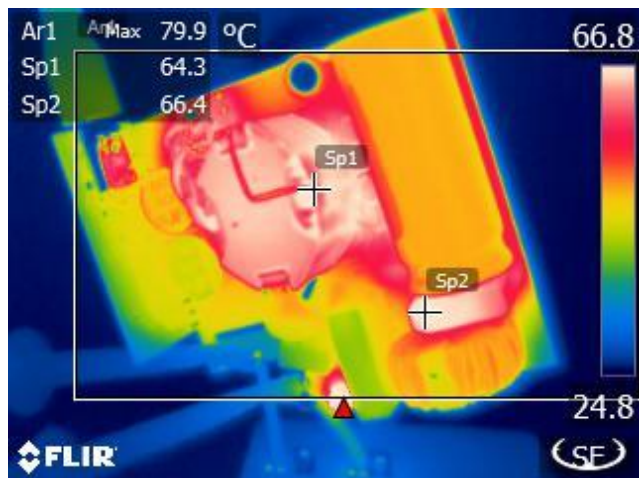
**Figure 34** – Transformer Side.  
Ambient = 25.8 °C.  
Transformer = 50.3 °C.



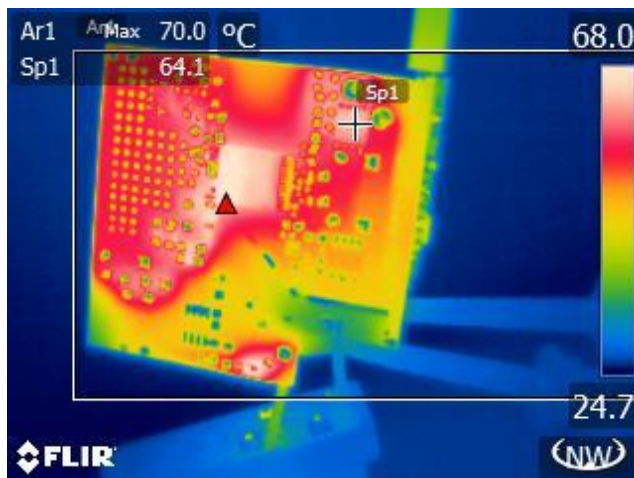
**Figure 35** – InnoSwitch3-Pro Side.  
Ambient = 25.8 °C.  
SR FET, Q2 = 62.4 °C.  
InnoSwitch3-Pro = 54.9 °C .

12.2 **9 V, 3 A**

12.2.1 85 VAC Input

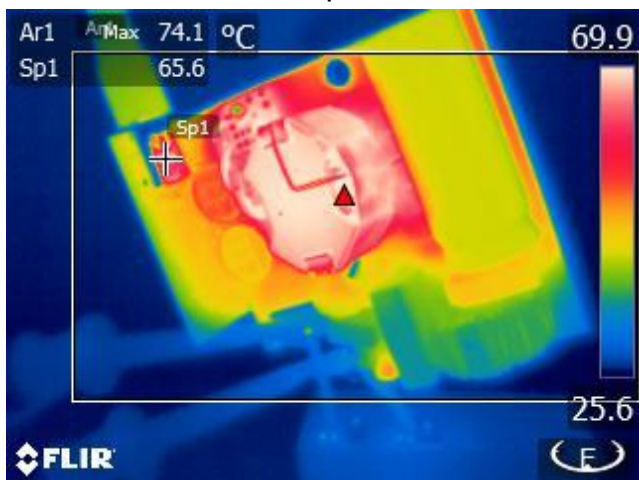


**Figure 36** – Transformer Side.  
 Ambient = 25.3 °C.  
 Thermistor, RT1 = 79.9 °C.  
 Transformer = 64.3 °C.

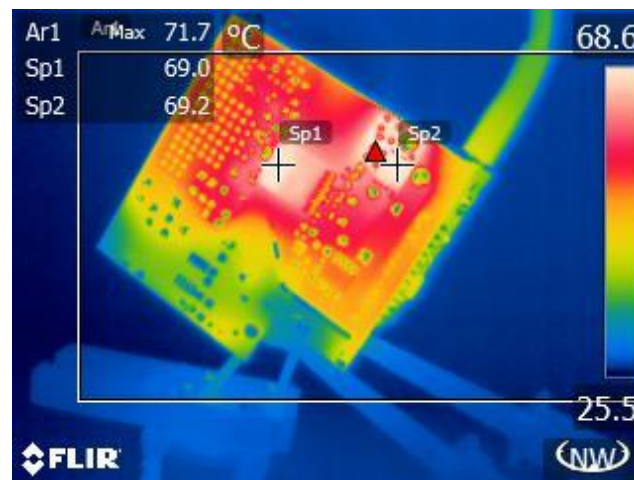


**Figure 37** – InnoSwitch3-Pro Side.  
 Ambient = 25.3 °C.  
 InnoSwitch3-Pro = 70.0 °C.  
 SR FET, Q2 = 64.1 °C.

12.2.2 265 VAC Input



**Figure 38** – Transformer Side.  
 Ambient = 25.6 °C.  
 Transformer = 74.1 °C.

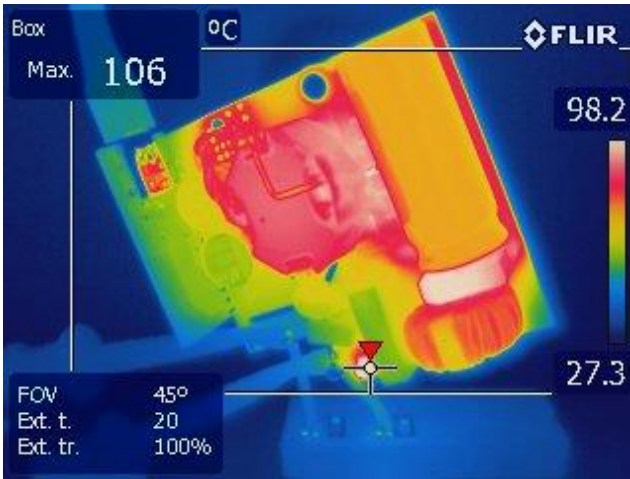


**Figure 39** – InnoSwitch3-Pro Side.  
 Ambient = 25.6 °C.  
 InnoSwitch3-Pro = 69.0 °C.  
 SR FET, Q2 = 71.7 °C.

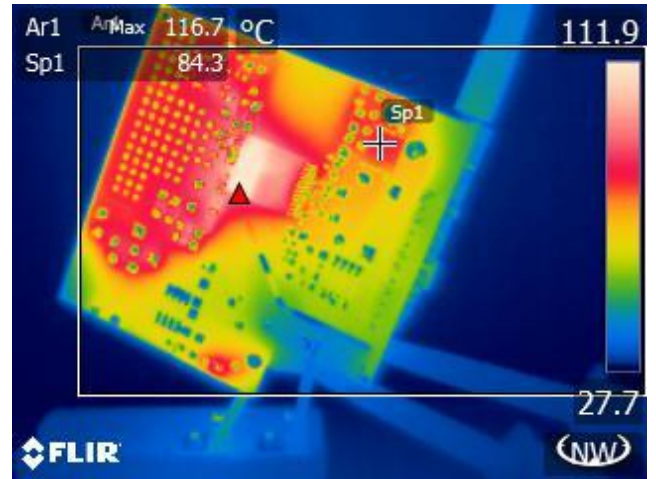


12.3 **15 V, 3 A**

12.3.1 85 VAC Input

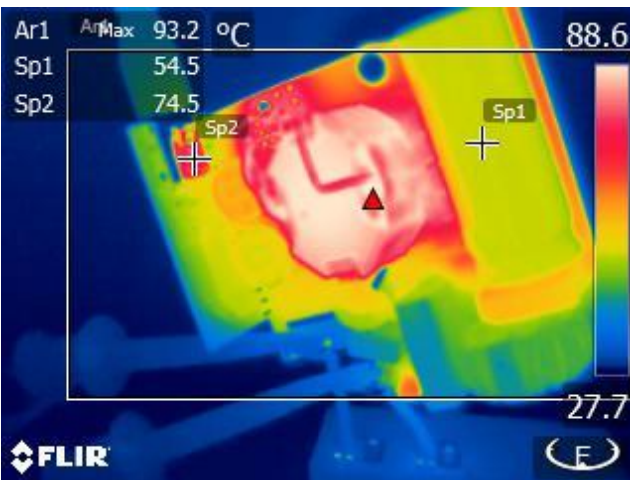


**Figure 40** – Transformer Side.  
 Ambient = 27.5 °C.  
 Thermistor, RT1 = 106.0 °C.

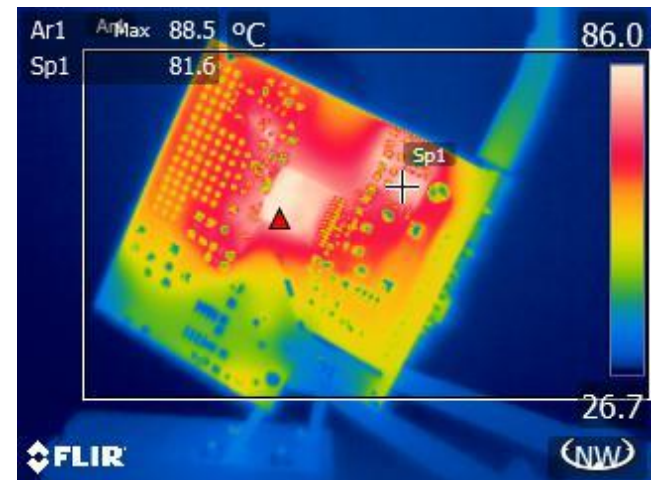


**Figure 41** – InnoSwitch3-Pro Side.  
 Ambient = 27.5°C.  
 InnoSwitch3-Pro = 116.7 °C.  
 SR FET, Q2 = 84.3 °C.

12.3.2 265 VAC Input



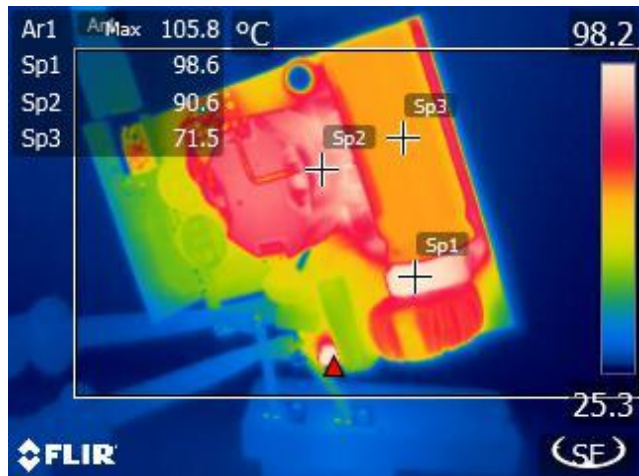
**Figure 42** – Transformer Side.  
 Ambient = 27.3 °C.  
 Transformer = 93.2 °C.



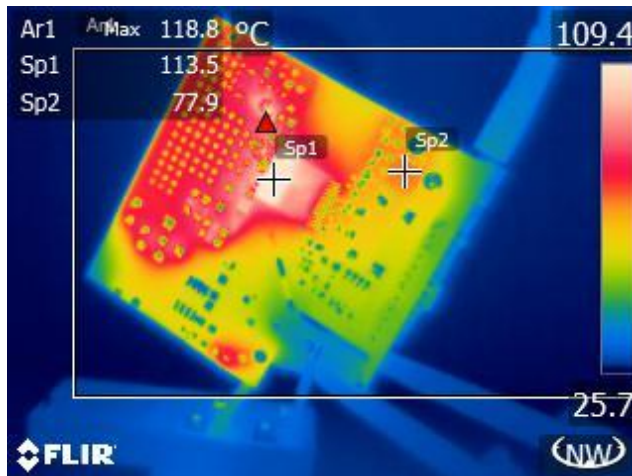
**Figure 43** – InnoSwitch3-Pro Side.  
 Ambient = 27.3 °C.  
 InnoSwitch3-Pro = 88.5 °C.  
 SR FET, Q2 = 81.6 °C.

12.4 **20 V, 2.25 A**

12.4.1 85 VAC Input

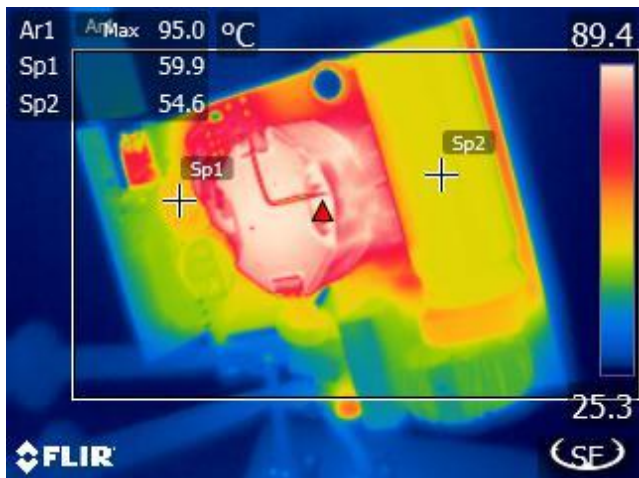


**Figure 44** – Transformer Side.  
 Ambient = 26.6 °C.  
 Thermistor, RT1 = 105.8 °C.  
 Bridge Rectifier, BR1 = 98.6 °C.

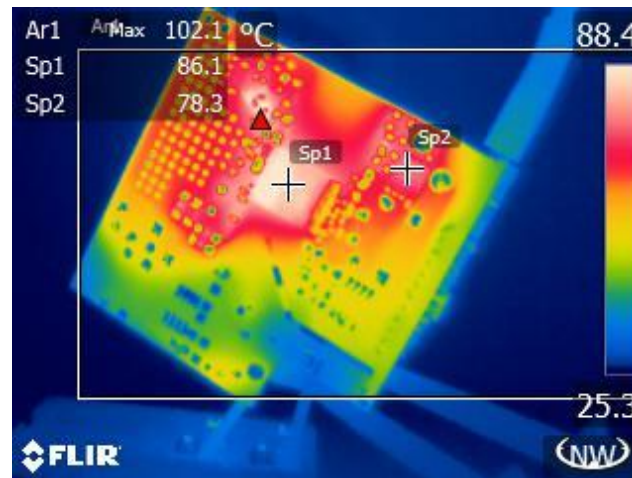


**Figure 45** – InnoSwitch3-Pro Side.  
 Ambient = 26.6 °C.  
 InnoSwitch3-Pro = 113.5 °C.  
 SR FET, Q2 = 77.9 °C.  
 BJT Transistor, Q1 = 118.8 °C.

12.4.2 265 VAC Input



**Figure 46** – Transformer Side.  
 Ambient = 26.0 °C.  
 Transformer = 95.0 °C.



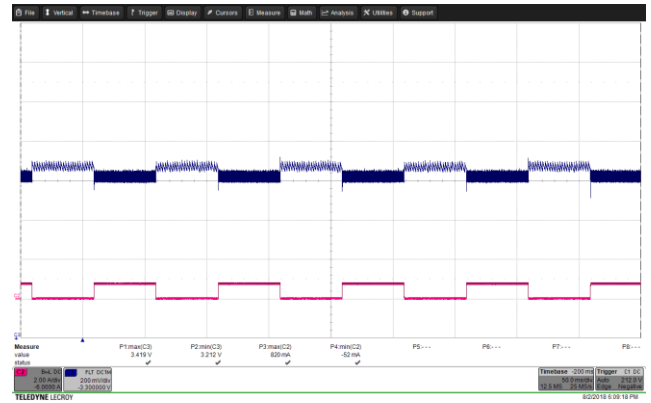
**Figure 47** – InnoSwitch3-Pro Side.  
 Ambient = 26.0 °C.  
 BJT Transistor, Q1 = 102.1 °C,  
 InnoSwitch3-Pro = 86.1 °C.  
 SR FET, Q2 = 78.3 °C.

## 13 Waveforms

### 13.1 Load Transient Response



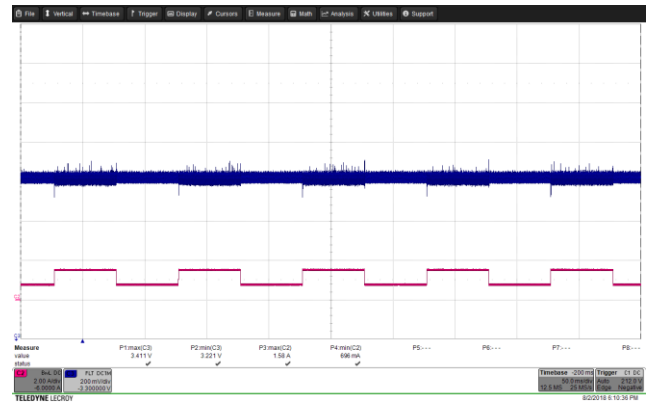
**Figure 48 – Transient Response.**  
 85 VAC, 3.3 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 3.195 V,  $V_{MAX}$ : 3.398 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 49 – Transient Response.**  
 265 VAC, 3.3 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 3.212 V,  $V_{MAX}$ : 3.419 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 50 – Transient Response.**  
 85 VAC, 3.3 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 3.199 V,  $V_{MAX}$ : 3.439 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



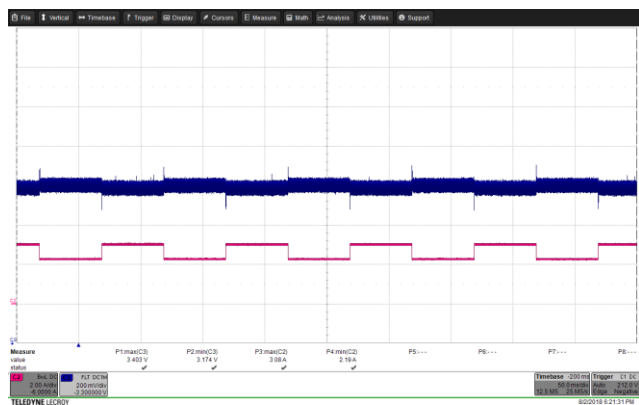
**Figure 51 – Transient Response.**  
 265 VAC, 3.3 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 3.221 V,  $V_{MAX}$ : 3.411 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



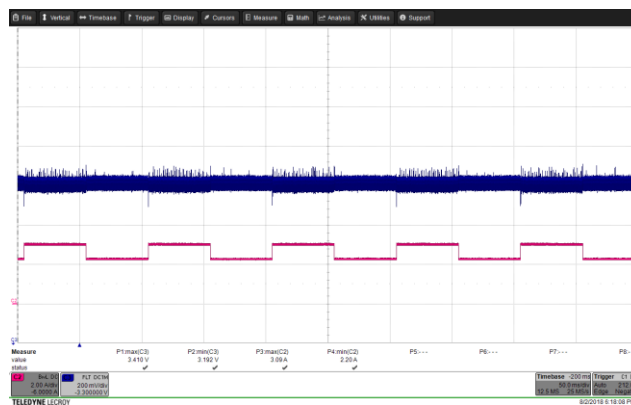
**Figure 52 – Transient Response.**  
 85 VAC, 3.3 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 3.181 V,  $V_{MAX}$ : 3.415 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 53 – Transient Response.**  
 265 VAC, 3.3 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 3.201 V,  $V_{MAX}$ : 3.420 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 54 – Transient Response.**  
 85 VAC, 3.3 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 3.174 V,  $V_{MAX}$ : 3.403 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 55 – Transient Response.**  
 265 VAC, 3.3 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 3.192 V,  $V_{MAX}$ : 3.410 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.





**Figure 56 – Transient Response.**  
 85 VAC, 5.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 4.899 V,  $V_{MAX}$ : 5.060 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



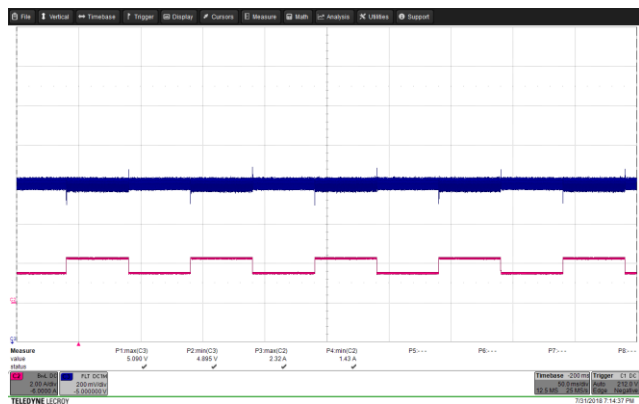
**Figure 57 – Transient Response.**  
 265 VAC, 5.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 4.941 V,  $V_{MAX}$ : 5.072 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



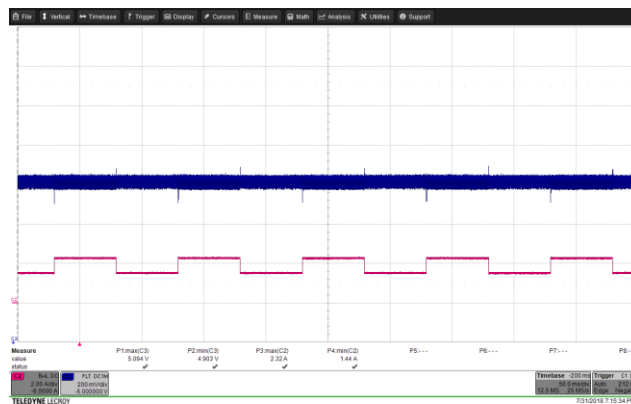
**Figure 58 – Transient Response.**  
 85 VAC, 5.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 4.900 V,  $V_{MAX}$ : 5.085 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



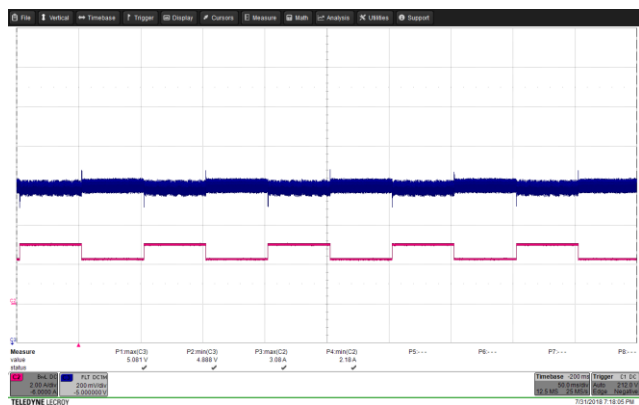
**Figure 59 – Transient Response.**  
 265 VAC, 5.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 4.961 V,  $V_{MAX}$ : 5.098 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 60 – Transient Response.**  
 85 VAC, 5.0 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 4.895 V,  $V_{MAX}$ : 5.090 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 61 – Transient Response.**  
 265 VAC, 5.0 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 4.903 V,  $V_{MAX}$ : 5.094 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 62 – Transient Response.**  
 85 VAC, 5.0 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 4.888 V,  $V_{MAX}$ : 5.081 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 63 – Transient Response.**  
 265 VAC, 5.0 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 4.908 V,  $V_{MAX}$ : 5.100 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



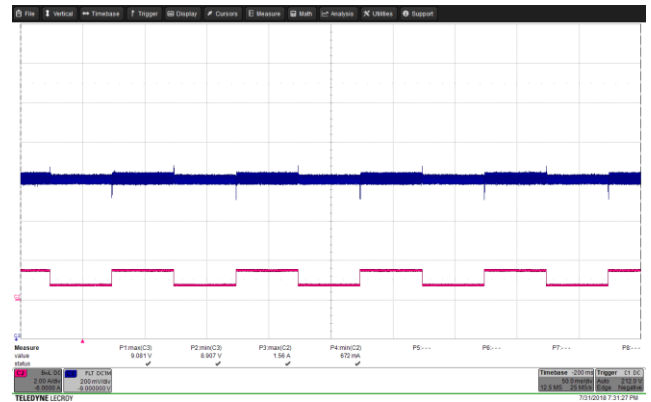
**Figure 64 – Transient Response.**  
 85 VAC, 9.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 8.888 V,  $V_{MAX}$ : 9.065 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



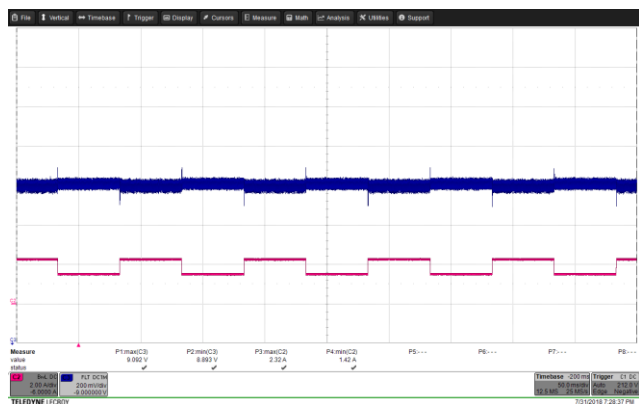
**Figure 65 – Transient Response.**  
 265 VAC, 9.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 8.899 V,  $V_{MAX}$ : 9.065 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 66 – Transient Response.**  
 85 VAC, 9.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 8.896 V,  $V_{MAX}$ : 9.089 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 67 – Transient Response.**  
 265 VAC, 9.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 8.907 V,  $V_{MAX}$ : 9.081 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



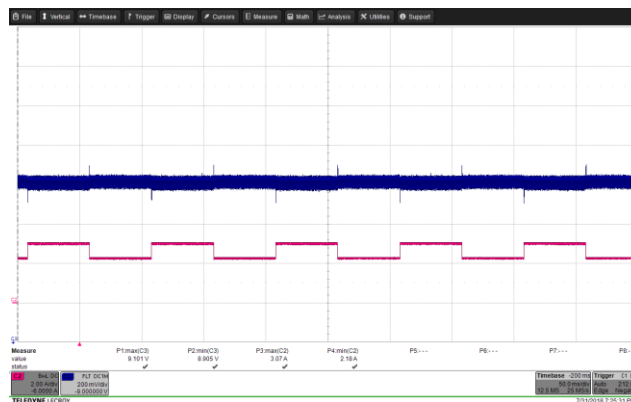
**Figure 68 – Transient Response.**  
 85 VAC, 9.0 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 8.893 V,  $V_{MAX}$ : 9.092 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 69 – Transient Response.**  
 265 VAC, 9.0 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 8.913 V,  $V_{MAX}$ : 9.103 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



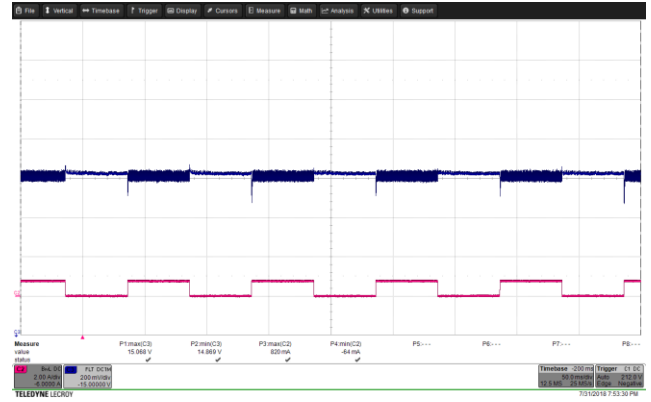
**Figure 70 – Transient Response.**  
 85 VAC, 9.0V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 8.884 V,  $V_{MAX}$ : 9.081 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 71 – Transient Response.**  
 265 VAC, 9.0 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 8.905 V,  $V_{MAX}$ : 9.101 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



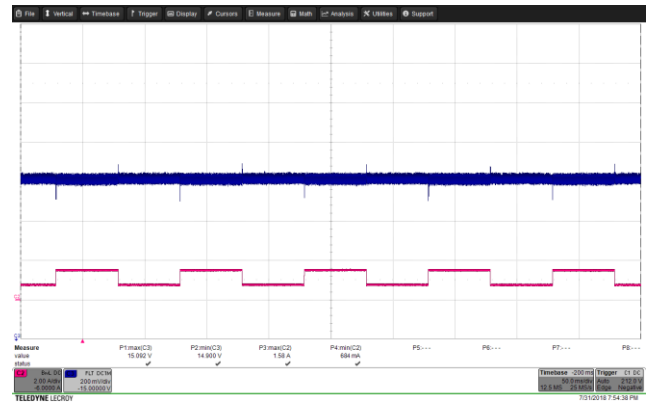
**Figure 72 – Transient Response.**  
 85 VAC, 15.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 14.867 V,  $V_{MAX}$ : 15.060 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



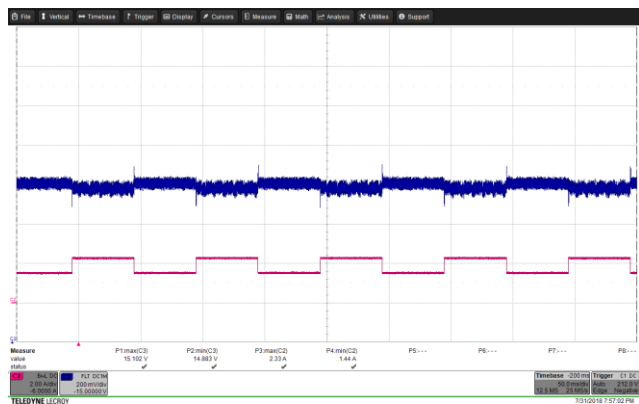
**Figure 73 – Transient Response.**  
 265 VAC, 15.0 V, 0 – 0.75 A Load Step.  
 $V_{MIN}$ : 14.869 V,  $V_{MAX}$ : 15.068 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



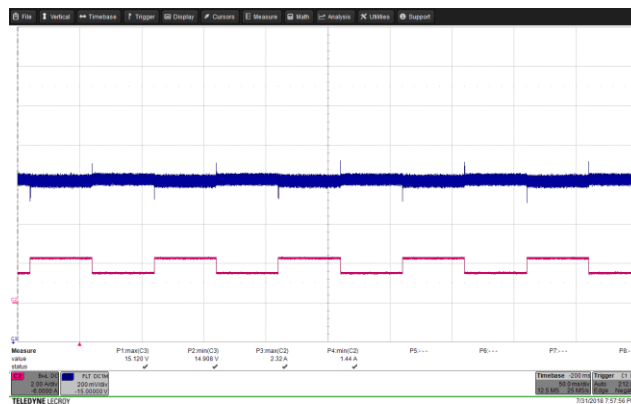
**Figure 74 – Transient Response.**  
 85 VAC, 15.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 14.885 V,  $V_{MAX}$ : 15.102 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



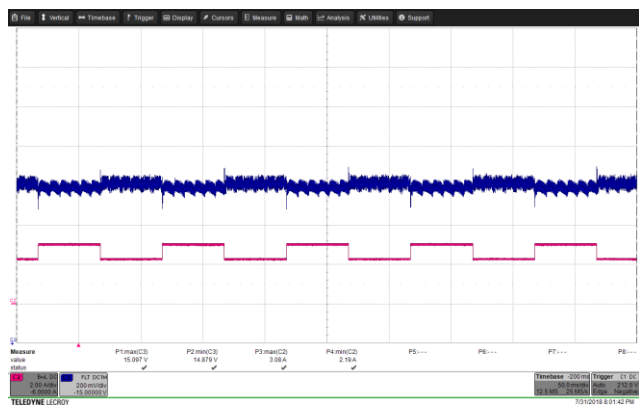
**Figure 75 – Transient Response.**  
 265 VAC, 15.0 V, 0.75 – 1.5 A Load Step.  
 $V_{MIN}$ : 14.900 V,  $V_{MAX}$ : 15.092 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 76 – Transient Response.**  
 85 VAC, 15 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 14.883 V,  $V_{MAX}$ : 15.102 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



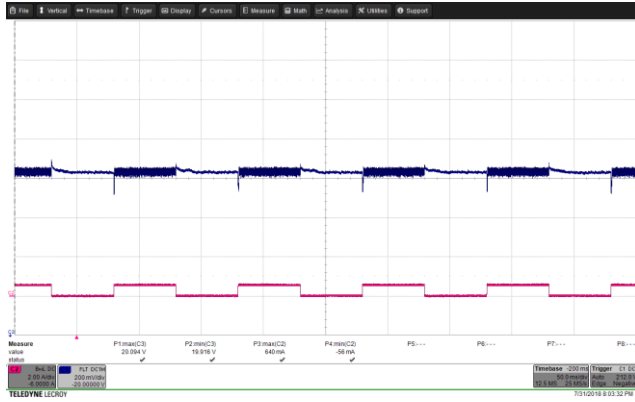
**Figure 77 – Transient Response.**  
 265 VAC, 15 V, 1.5 – 2.25 A Load Step.  
 $V_{MIN}$ : 14.908 V,  $V_{MAX}$ : 15.120 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 78 – Transient Response.**  
 85 VAC, 15 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 14.879 V,  $V_{MAX}$ : 15.097 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



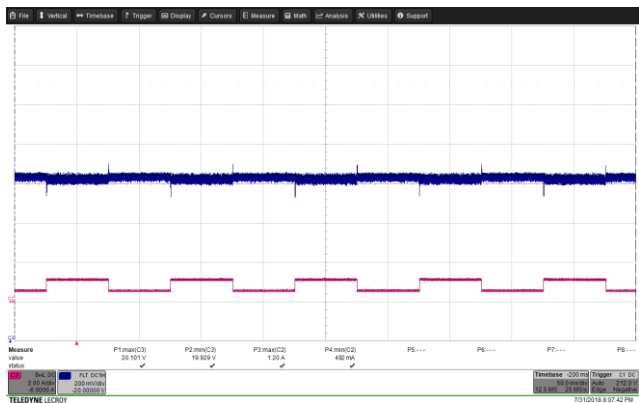
**Figure 79 – Transient Response.**  
 265 VAC, 15 V, 2.25 – 3 A Load Step.  
 $V_{MIN}$ : 14.915 V,  $V_{MAX}$ : 15.118 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



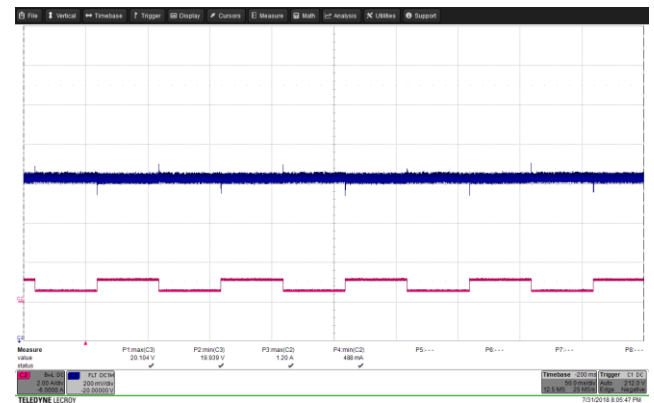
**Figure 80 – Transient Response.**  
 85 VAC, 20.0 V, 0 – 0.56 A Load Step.  
 $V_{MIN}$ : 19.916 V,  $V_{MAX}$ : 20.094 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



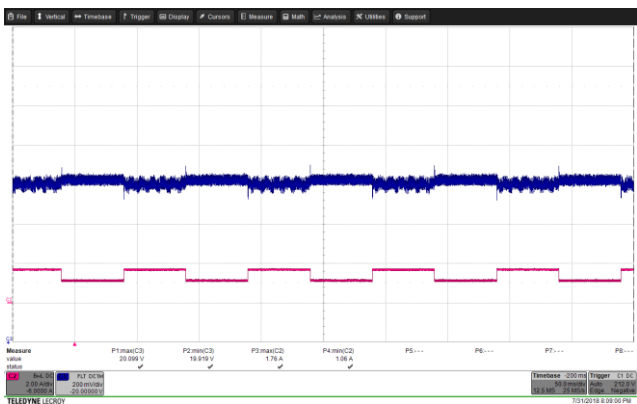
**Figure 81 – Transient Response.**  
 265 VAC, 20.0 V, 0 – 0.56 A Load Step.  
 $V_{MIN}$ : 19.924 V,  $V_{MAX}$ : 20.088 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



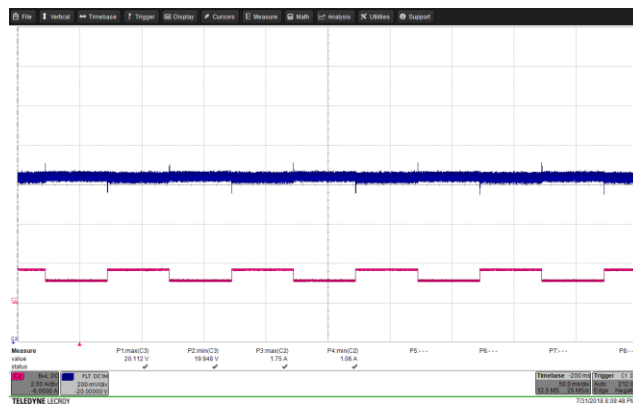
**Figure 82 – Transient Response.**  
 85 VAC, 20.0 V, 0.56 – 1.125 A Load Step.  
 $V_{MIN}$ : 19.929 V,  $V_{MAX}$ : 20.101 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



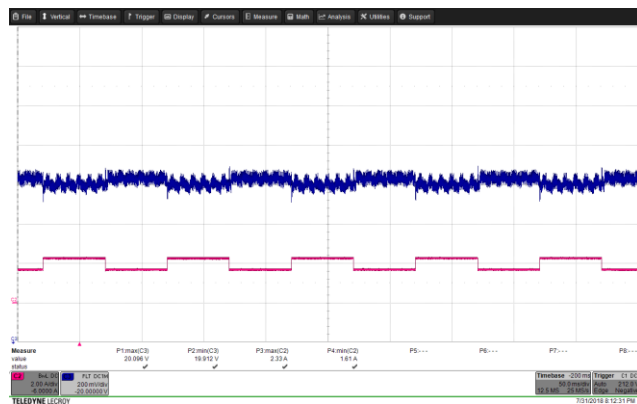
**Figure 83 – Transient Response.**  
 265 VAC, 20.0 V, 0.56 – 1.125 A Load Step.  
 $V_{MIN}$ : 19.939 V,  $V_{MAX}$ : 20.104 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



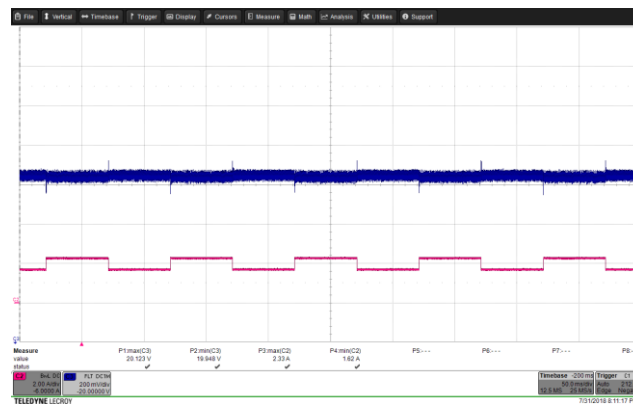
**Figure 84 – Transient Response.**  
 85 VAC, 20.0 V, 1.125 – 1.68 A Load Step.  
 $V_{MIN}$ : 19.919 V,  $V_{MAX}$ : 20.099 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 85 – Transient Response.**  
 265 VAC, 20.0 V, 1.125 – 1.68 A Load Step.  
 $V_{MIN}$ : 19.948 V,  $V_{MAX}$ : 20.112 V.  
 Upper:  $V_{OUT}$ , 0.2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.



**Figure 86 – Transient Response.**  
 85 VAC, 20.0 V, 1.68 – 2.25 A Load Step.  
 $V_{MIN}$ : 19.912 V,  $V_{MAX}$ : 20.096 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.

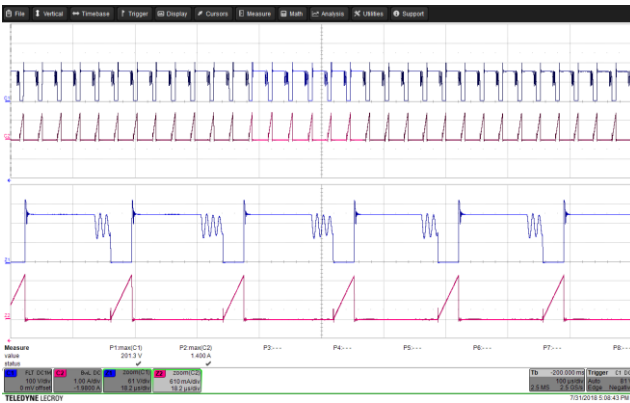


**Figure 87 – Transient Response.**  
 265 VAC, 20.0 V, 1.68 – 2.25 A Load Step.  
 $V_{MIN}$ : 19.948 V,  $V_{MAX}$ : 20.123 V.  
 Upper:  $V_{OUT}$ , .2 V / div., 50 ms / div.  
 Lower:  $I_{LOAD}$ , 2 A / div.

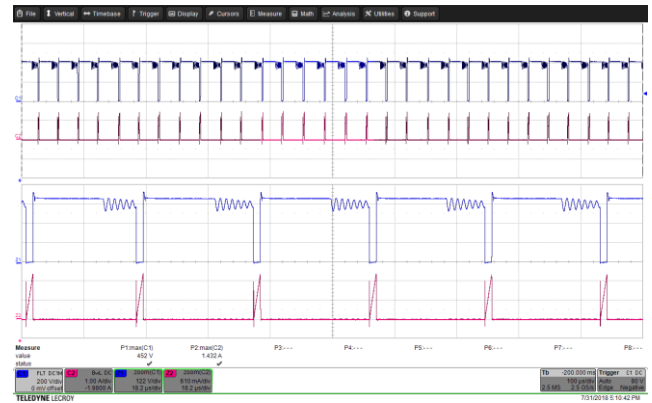


## 13.2 Switching Waveforms

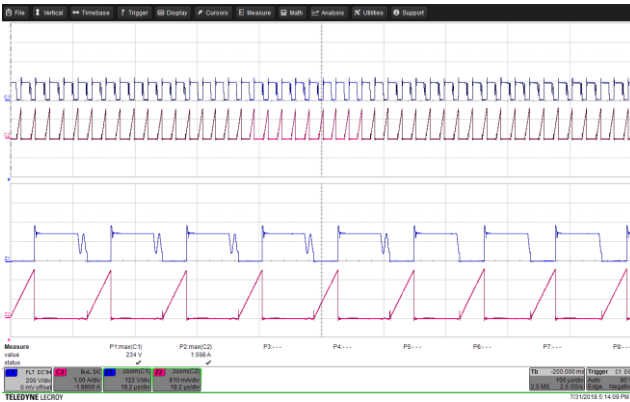
### 13.2.1 Primary Drain Voltage and Current



**Figure 88** – Drain Voltage and Current Waveforms.  
 85 VAC, 5.0 V, 3 A Load (201.3  $V_{MAX}$ ).  
 Upper:  $V_{DRAIN}$ , 100 V, 100  $\mu s$  / div.  
 Lower:  $I_{DRAIN}$ , 1 A / div.



**Figure 89** – Drain Voltage and Current Waveforms.  
 265 VAC, 5.0 V, 3 A Load (452.0  $V_{MAX}$ ).  
 Upper:  $V_{DRAIN}$ , 200 V, 100  $\mu s$  / div.  
 Lower:  $I_{DRAIN}$ , 1 A / div.

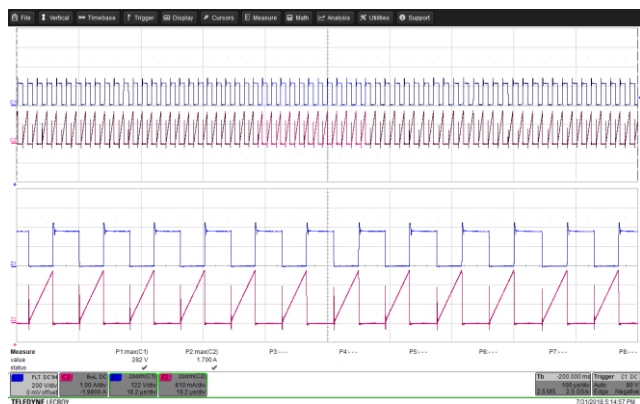


**Figure 90** – Drain Voltage and Current Waveforms.  
 85 VAC, 9.0 V, 3 A Load (234.0  $V_{MAX}$ ).  
 Upper:  $V_{DRAIN}$ , 200 V, 100  $\mu s$  / div.  
 Lower:  $I_{DRAIN}$ , 1 A / div.

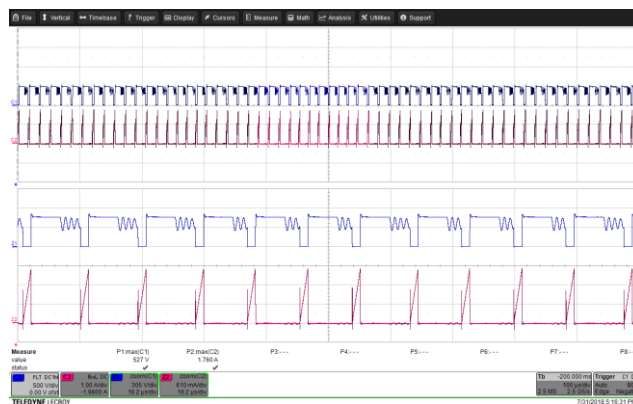


**Figure 91** – Drain Voltage and Current Waveforms.  
 265 VAC, 9 V, 3 A Load (487.0  $V_{MAX}$ ).  
 Upper:  $V_{DRAIN}$ , 200 V, 100  $\mu s$  / div.  
 Lower:  $I_{DRAIN}$ , 1 A / div.

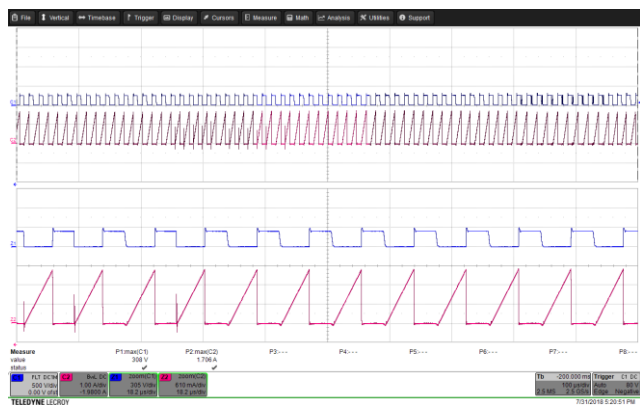




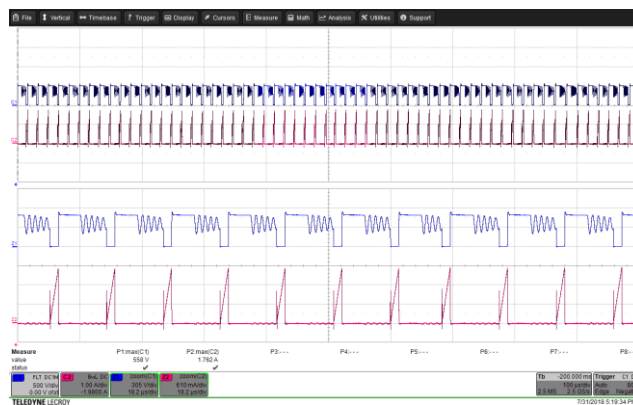
**Figure 92** – Drain Voltage and Current Waveforms.  
85 VAC, 15.0 V, 3 A Load (282.0  $V_{MAX}$ ).  
Upper:  $V_{DRAIN}$ , 200 V, 100  $\mu$ s / div.  
Lower:  $I_{DRAIN}$ , 1 A / div.



**Figure 93** – Drain Voltage and Current Waveforms.  
265 VAC, 15 V, 3 A Load (527.0  $V_{MAX}$ ).  
Upper:  $V_{DRAIN}$ , 500 V, 100  $\mu$ s / div.  
Lower:  $I_{DRAIN}$ , 1 A / div.

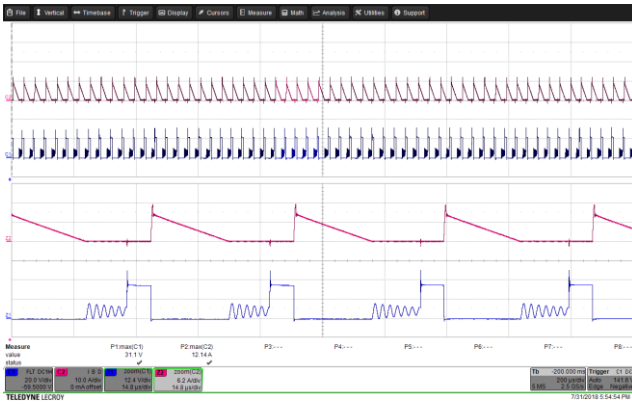


**Figure 94** – Drain Voltage and Current Waveforms.  
85 VAC, 20.0 V, 2.25 A Load (308  $V_{MAX}$ ).  
Upper:  $V_{DRAIN}$ , 500 V, 100  $\mu$ s / div.  
Lower:  $I_{DRAIN}$ , 1 A / div.

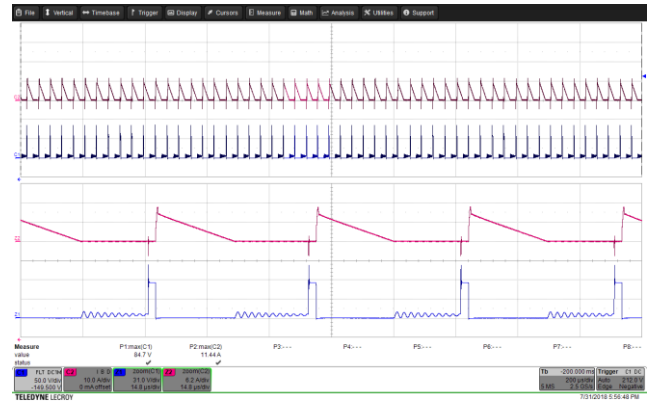


**Figure 95** – Drain Voltage and Current Waveforms.  
265 VAC, 20 V, 2.25 A Load (558.0  $V_{MAX}$ ).  
Upper:  $V_{DRAIN}$ , 500 V, 100  $\mu$ s / div.  
Lower:  $I_{DRAIN}$ , 1 A / div.

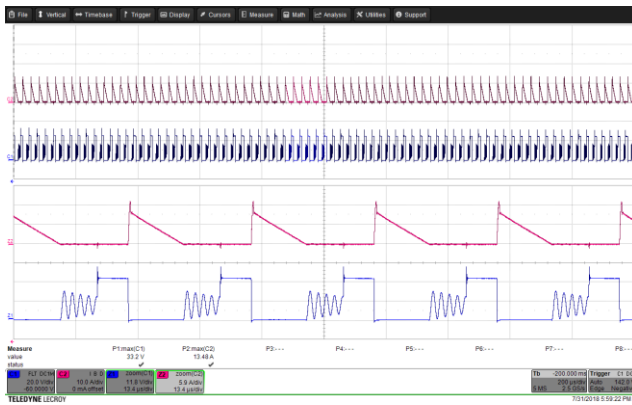
### 13.2.2 SR FET Voltage



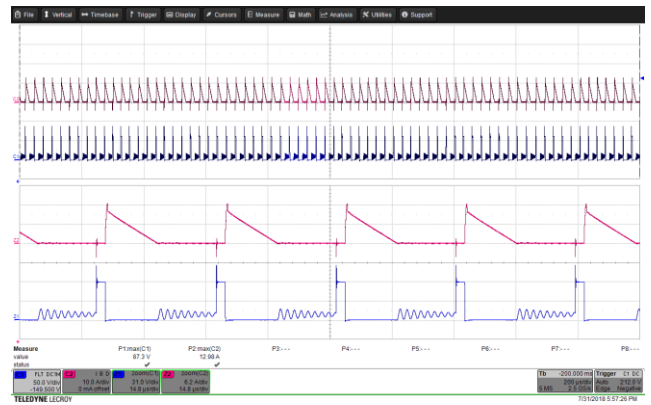
**Figure 96** – SR FET Voltage Waveforms.  
 85 VAC, 5.0 V, 3 A Load (31.1 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 20 V, 200 μs / div.



**Figure 97** – SR FET Voltage Waveforms.  
 265 VAC, 5.0 V, 3 A Load (84.7 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.

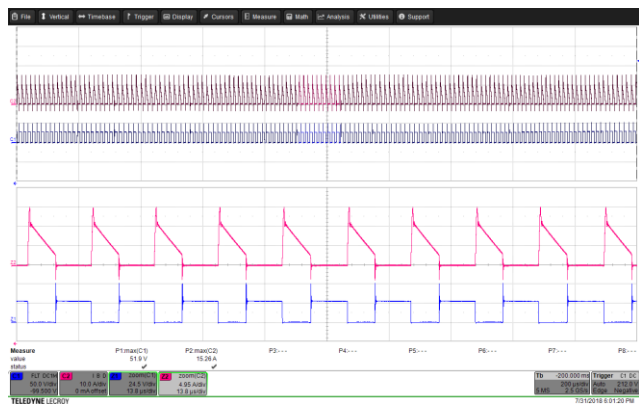


**Figure 98** – SR FET Voltage Waveforms.  
 85 VAC, 9.0 V, 3 A Load (33.2 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 20 V, 200 μs / div.

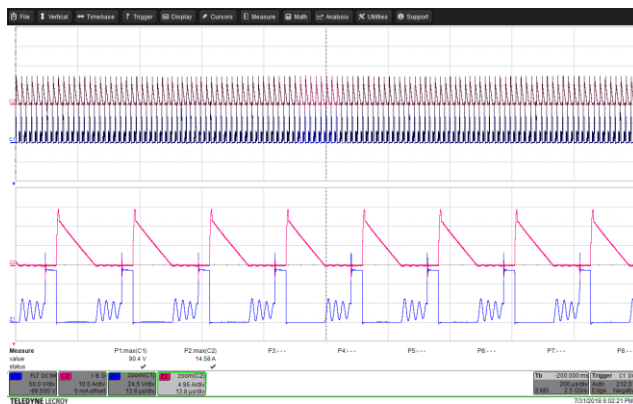


**Figure 99** – SR FET Voltage Waveforms.  
 265 VAC, 9.0 V, 3 A Load (87.3 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.

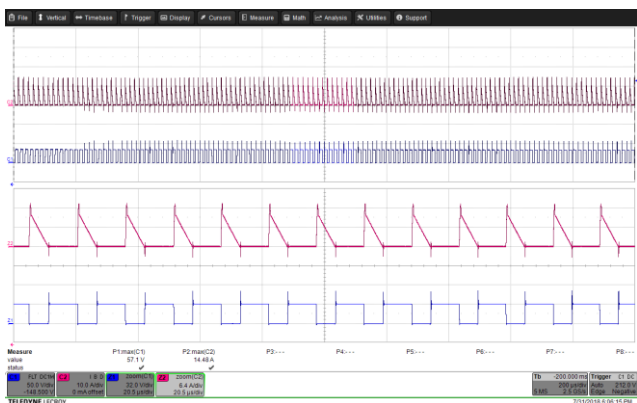




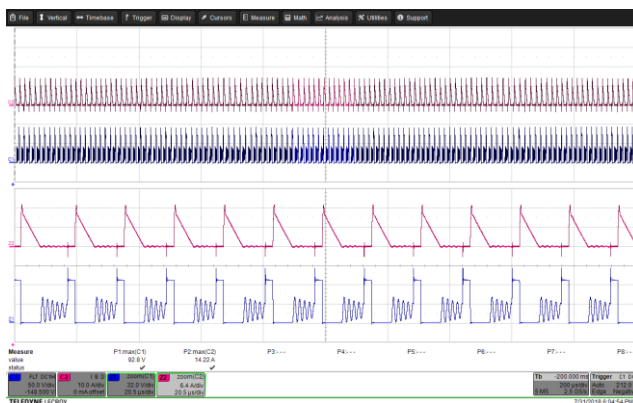
**Figure 100** – SR FET Voltage Waveforms.  
 85 VAC, 15.0 V, 3 A Load (51.9 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.



**Figure 101** – SR FET Voltage Waveforms.  
 265 VAC, 15.0 V, 3 A Load (90.4 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.

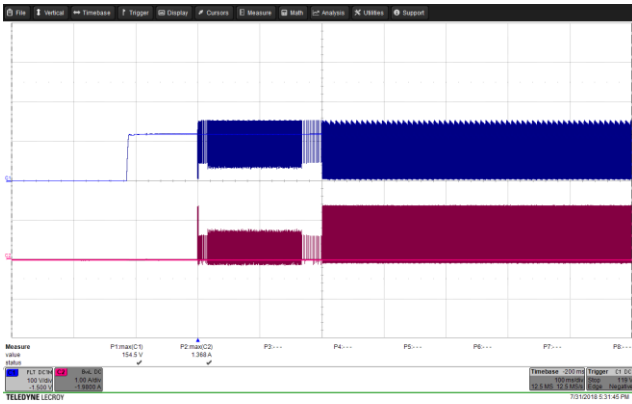


**Figure 102** – SR FET Voltage Waveforms.  
 85 VAC, 20.0 V, 2.25 A Load (57.1 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.

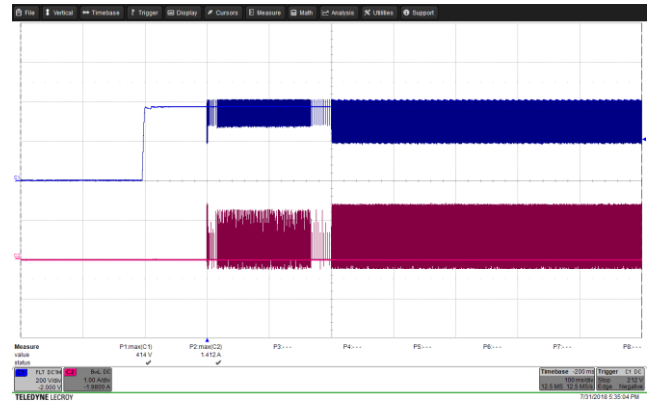


**Figure 103** – SR FET Voltage Waveforms.  
 265 VAC, 20.0 V, 2.25 A Load (92.8 V<sub>MAX</sub>).  
 Upper: I<sub>DRAIN</sub>, 10 A / div.  
 Lower: V<sub>DRAIN</sub>, 50 V, 200 μs / div.

### 13.3 Start-up



**Figure 104** – Drain Voltage and Current Waveforms.  
 85 VAC, 5.0 V, 3 A Load (154.5 V<sub>MAX</sub>).  
 Upper: V<sub>DRAIN</sub>, 100 V, 100 ms / div.  
 Lower: I<sub>DRAIN</sub>, 1 A / div.

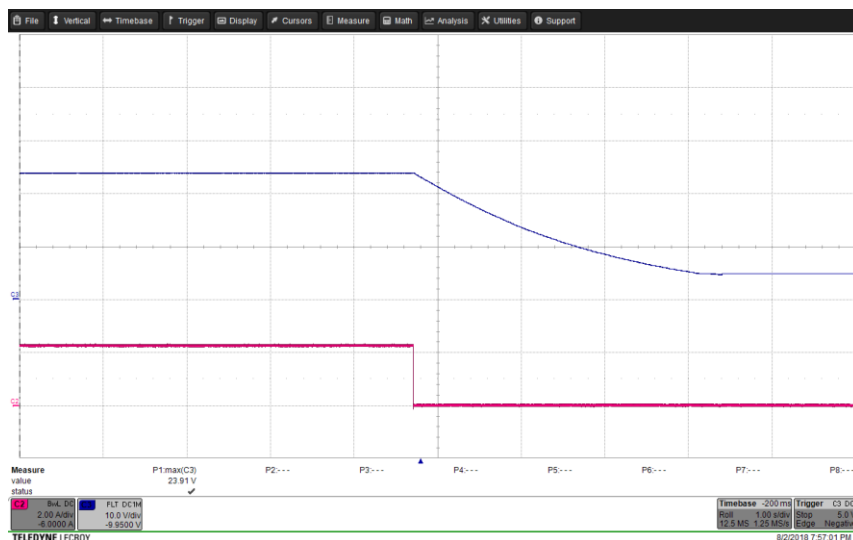


**Figure 105** – Drain Voltage and Current Waveforms.  
 265 VAC, 5.0 V, 3 A Load (414.0 V<sub>MAX</sub>).  
 Upper: V<sub>DRAIN</sub>, 200 V, 100 ms / div.  
 Lower: I<sub>DRAIN</sub>, 1 A / div.



### 13.4 *Primary Overvoltage Protection*

**Note:** To verify operation of the primary sensed output over-voltage protection feature, the daughter board was removed and an external I<sup>2</sup>C device was connected to the mother board. The output voltage was gradually increased in 20mV steps by issuing I<sup>2</sup>C commands and it was confirmed that over voltage protection operated only when the output voltage increased sufficiently above 20V. Measured over-voltage trip point for the unit tested was 23.91V.



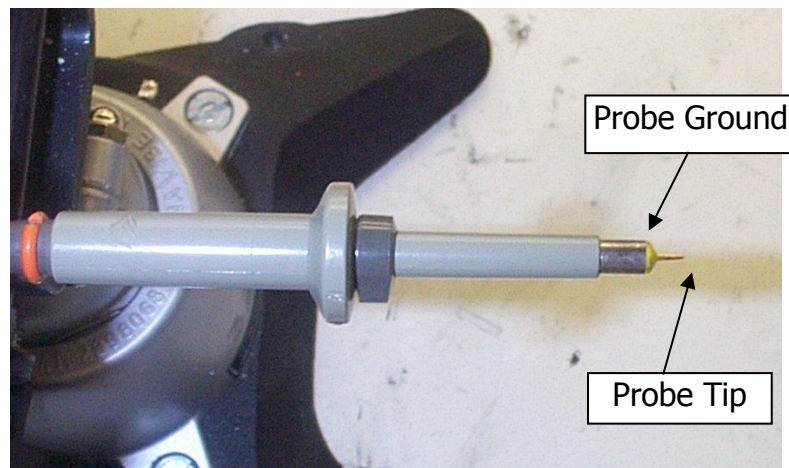
**Figure 106** – Output Voltage and Output Current Waveforms.  
85 VAC, Latch Off Occurred at 23.91 V V<sub>OUT</sub> and 2.25 A Load.  
Upper: V<sub>OUT</sub>, 10.0 V, 1 s / div.  
Lower: I<sub>OUT</sub>, 2 A / div.

## 13.5 **Output Ripple Measurements**

### 13.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1  $\mu\text{F}$ /50 V ceramic type and one (1) 47  $\mu\text{F}$ /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

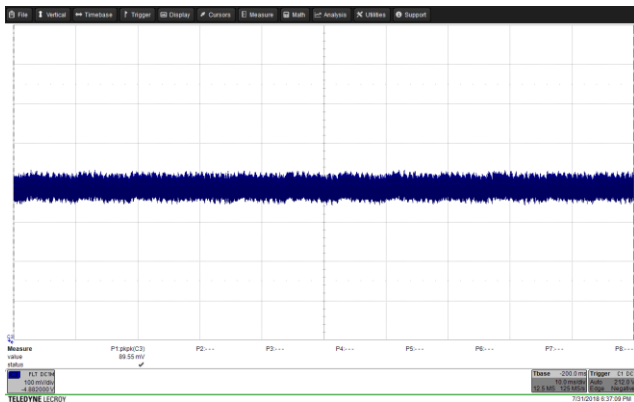


**Figure 107** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

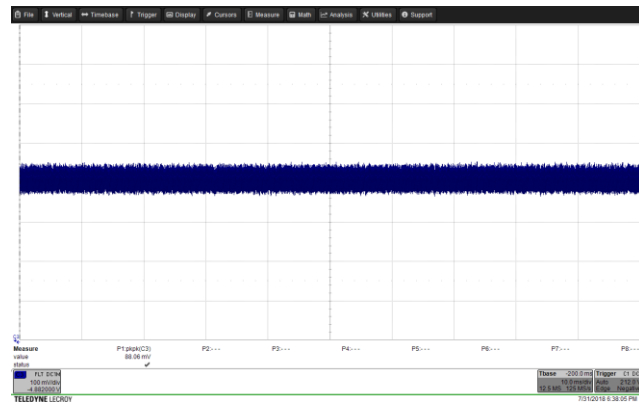


**Figure 108** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.5.1.1 5 V (End of Type-C Cable)

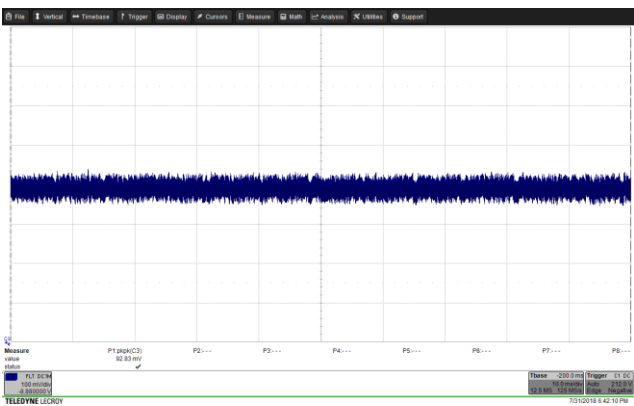


**Figure 109** – Output Ripple. PK-PK = 89.55 mV.  
85 VAC<sub>IN</sub> 5.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.

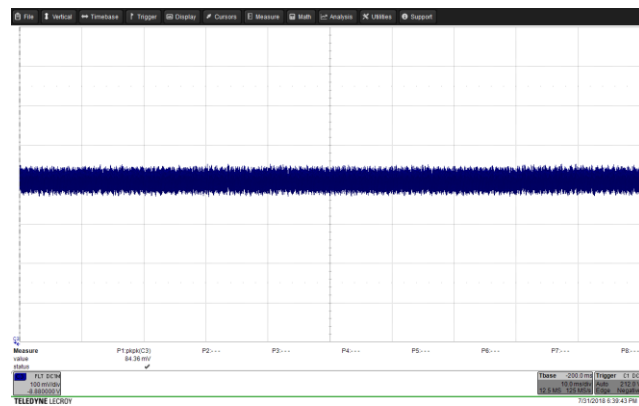


**Figure 110** – Output Ripple. PK-PK = 88.06 mV.  
265 VAC<sub>IN</sub> 5.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.

13.5.1.2 9 V (End of Type-C Cable)



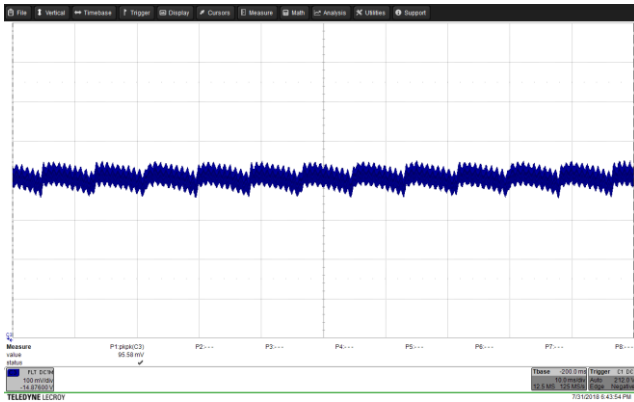
**Figure 111** – Output Ripple. PK-PK = 92.83 mV.  
85 VAC<sub>IN</sub> 9.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.



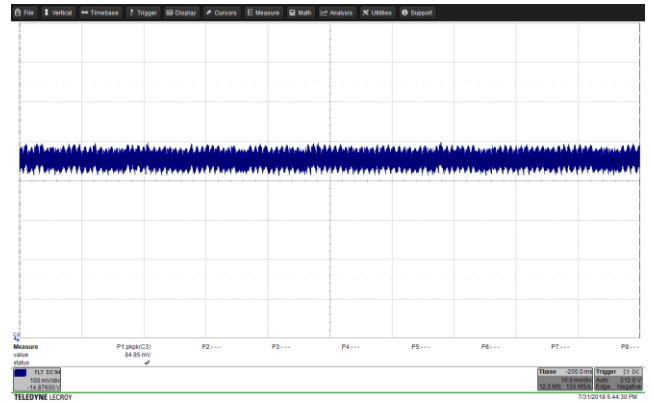
**Figure 112** – Output Ripple. PK-PK = 84.36 mV.  
265 VAC<sub>IN</sub> 9.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.



13.5.1.3 15 V (End of Type-C Cable)

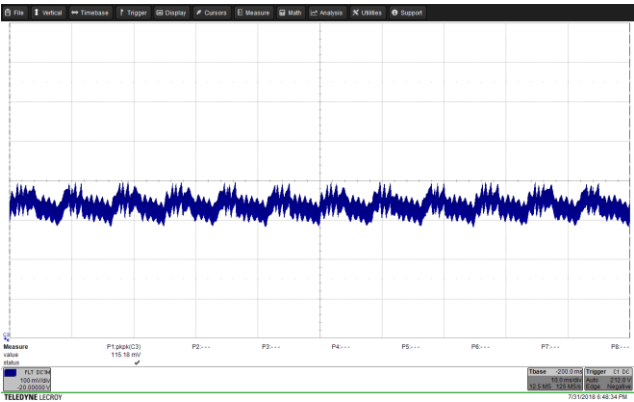


**Figure 113** – Output Ripple. PK-PK = 95.58 mV.  
85 VAC<sub>IN</sub>, 15.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.

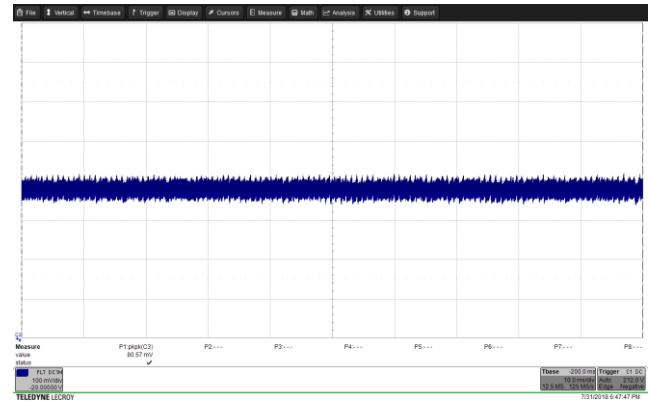


**Figure 114** – Output Ripple. PK-PK = 84.85 mV.  
265 VAC<sub>IN</sub> 15.0 V, 3 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.

13.5.1.4 20 V (End of Type-C Cable)



**Figure 115** – Output Ripple. PK-PK = 115.18 mV.  
85 VAC<sub>IN</sub>, 20.0 V, 2.25 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.



**Figure 116** – Output Ripple. PK-PK = 80.57 mV.  
265 VAC<sub>IN</sub> 20.0 V, 2.25 A Load.  
V<sub>OUT</sub>, 100 mV / div., 10 ms / div.



### 14 CV/CC Profile

Note:

- 1. Voltage is measured at the end of cable. Drop in voltage is due to cable drop
- 2. Positive slope in CC region is per the guidelines of USB PD3.0 PPS Specification

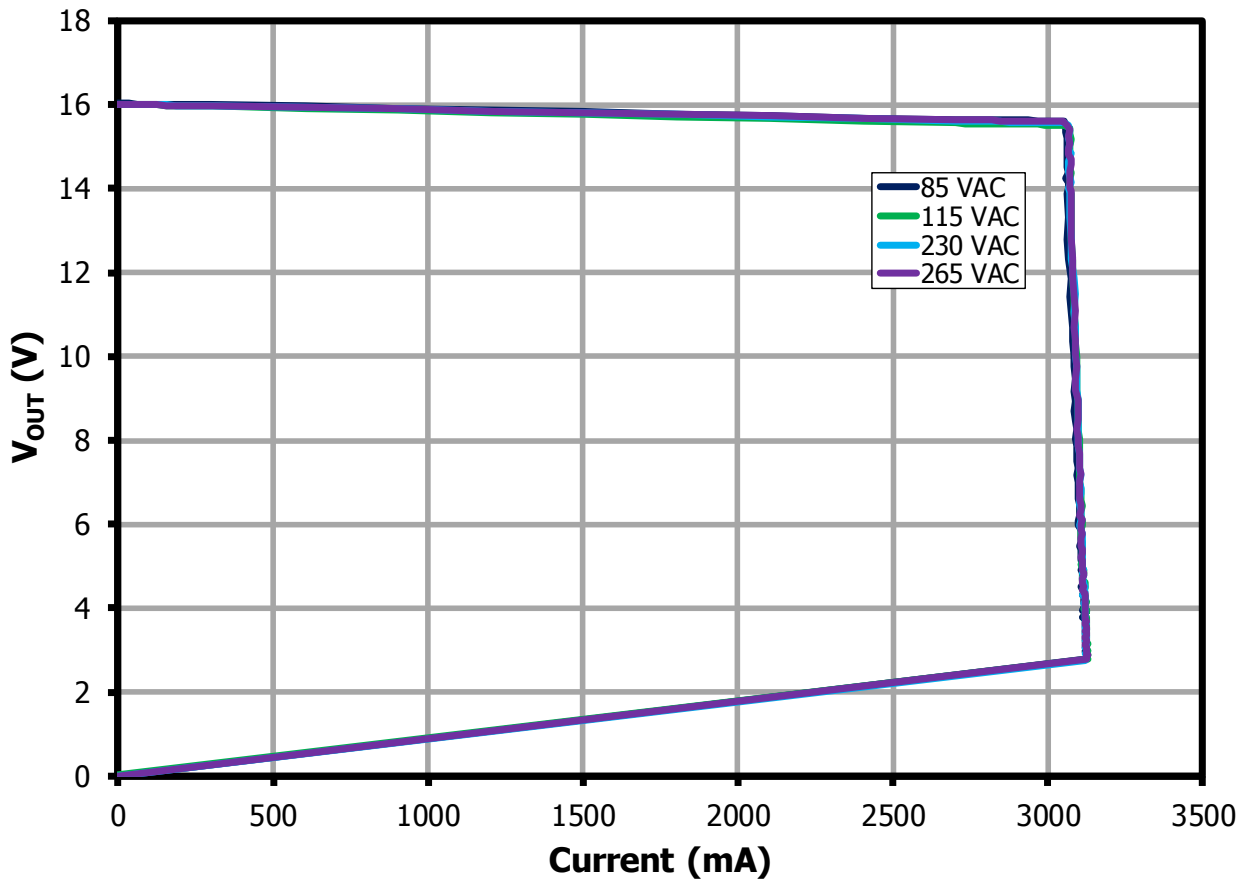
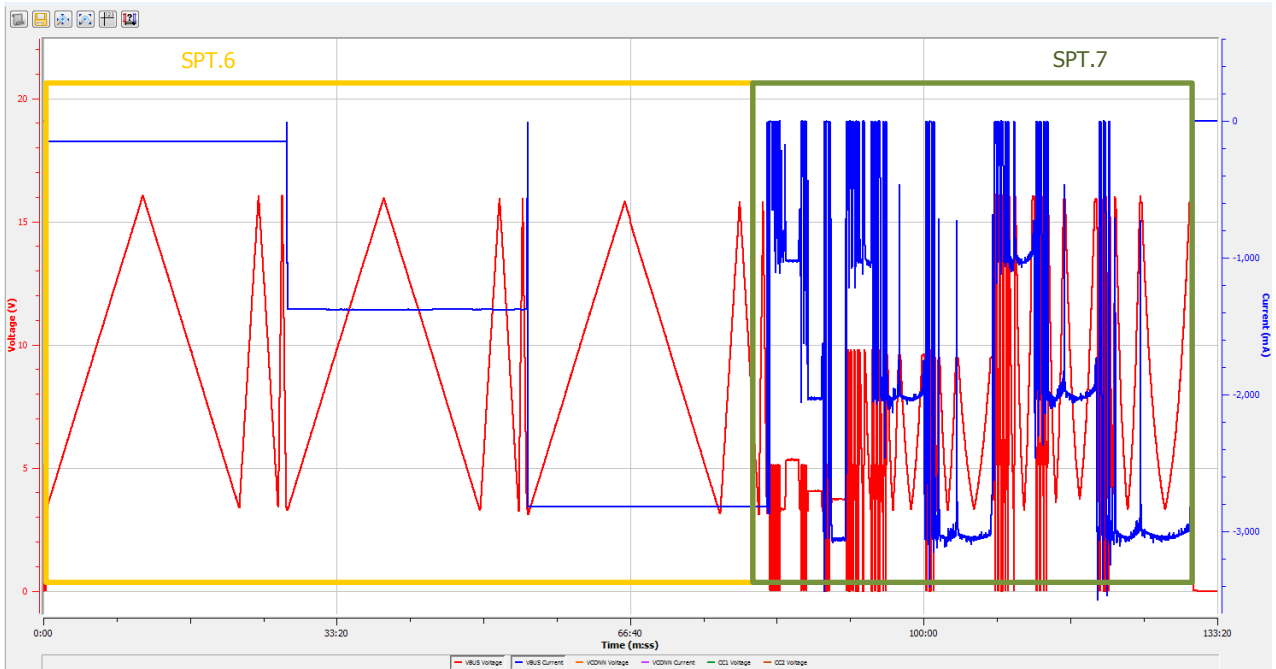


Figure 117 – CV/CC Profile with Output 16 V, 3 A.

## 15 Voltage and Current Step Test using Quadramax and Total Phase Analyzer



**Figure 118** – Plot of SPT.6 VST Test and SPT.7 CLT Test from Total Phase Analyzer.

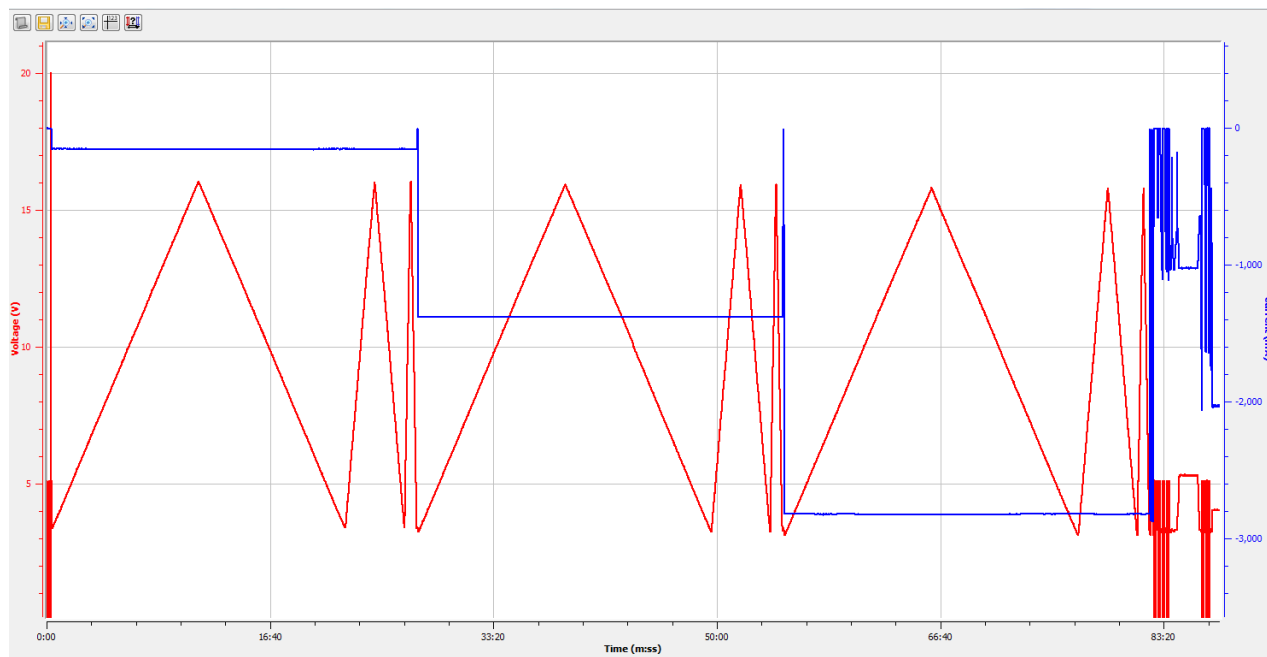


Figure 119 – Plot of SPT.6 VST Test from Total Phase Analyzer.

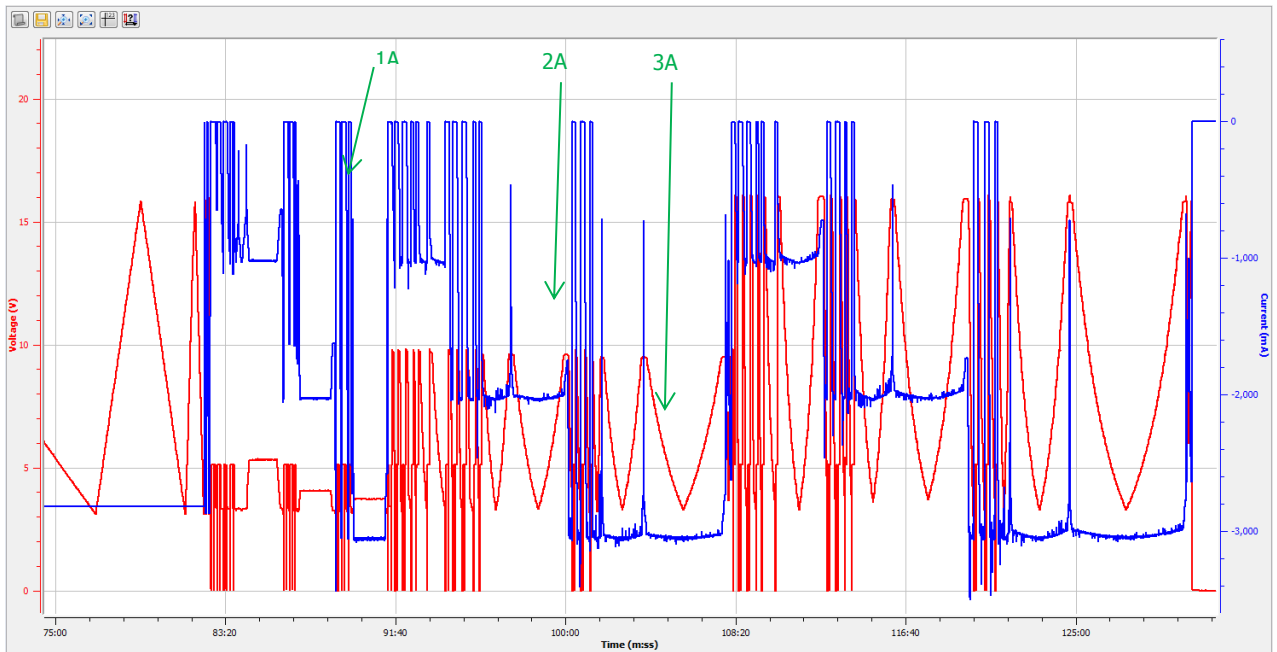


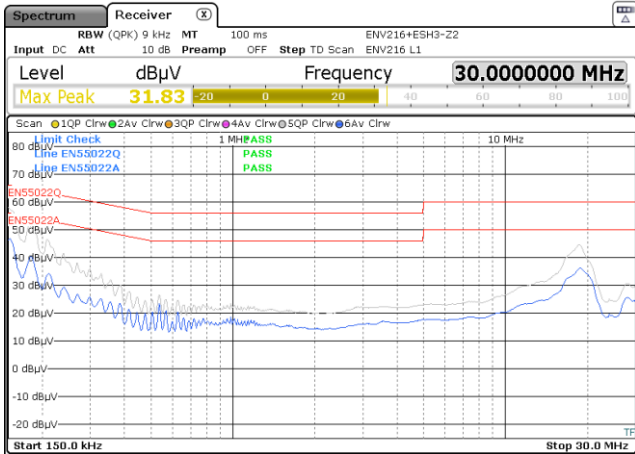
Figure 120 – Plot of SPT.7 CLT Test from Total Phase Analyzer.



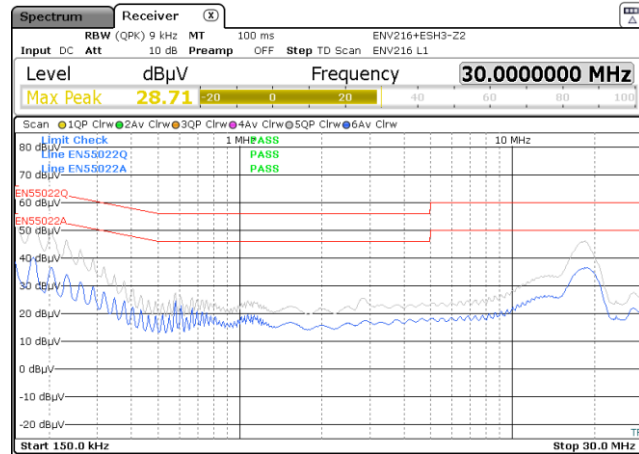
## 16 Conducted EMI

### 16.1 Output Ground Left Floating (QPK / AV)

#### 16.1.1 5 V, 3 A



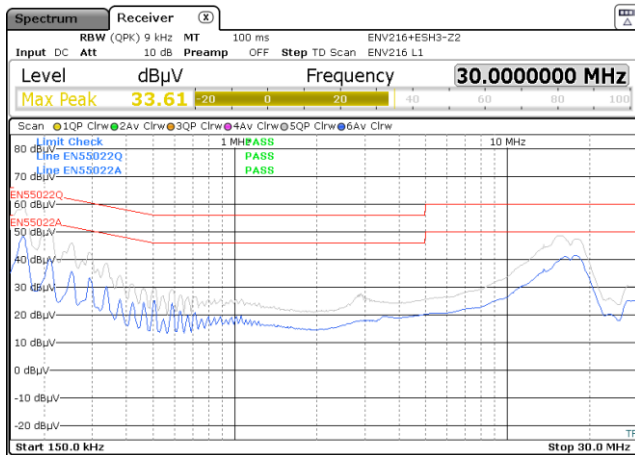
115 VAC<sub>IN</sub>.



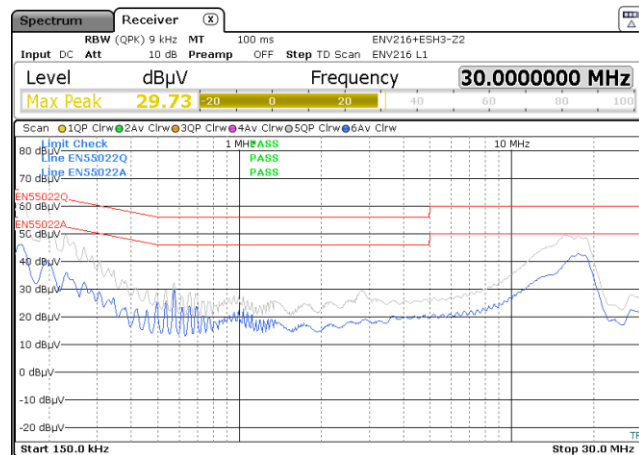
230 VAC<sub>IN</sub>.

**Figure 121** – Floating Ground EMI, 5 V / 3 A Load [Line Scan].

#### 16.1.2 9 V, 3 A



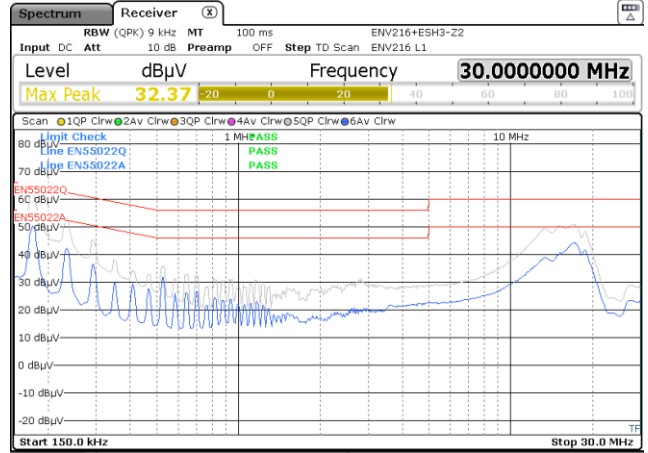
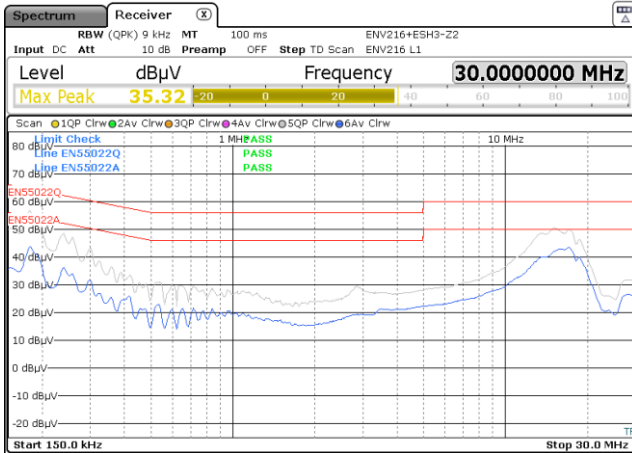
115 VAC<sub>IN</sub>.



230 VAC<sub>IN</sub>.

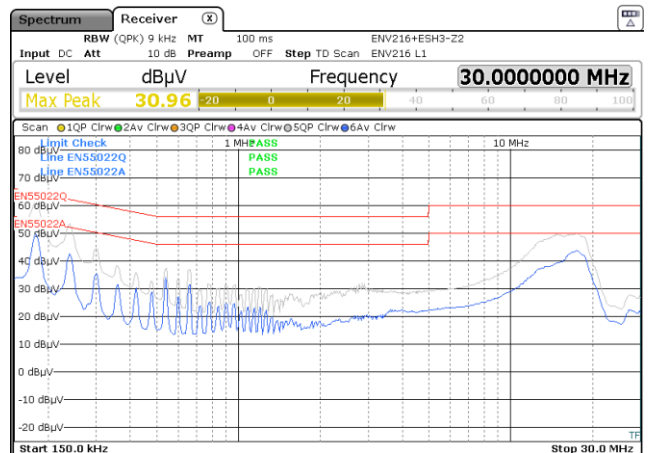
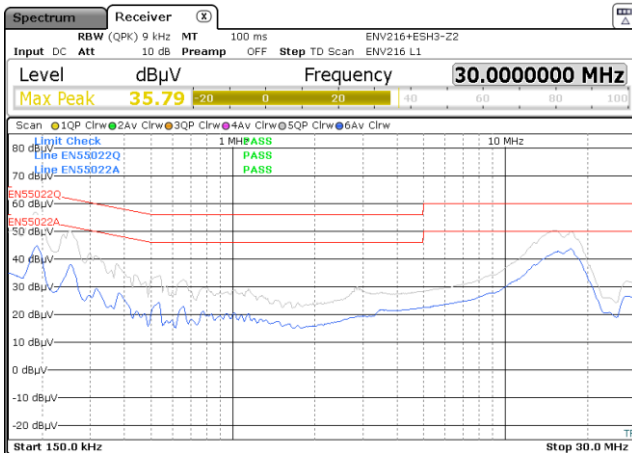
**Figure 122** – Floating Ground EMI, 9 V / 3 A Load [Line Scan].

16.1.3 15 V, 3 A



115 VAC<sub>IN</sub>. 230 VAC<sub>IN</sub>.  
**Figure 123** – Floating Ground EMI, 3 V / 3 A Load [Line Scan].

16.1.4 20 V, 2.25 A

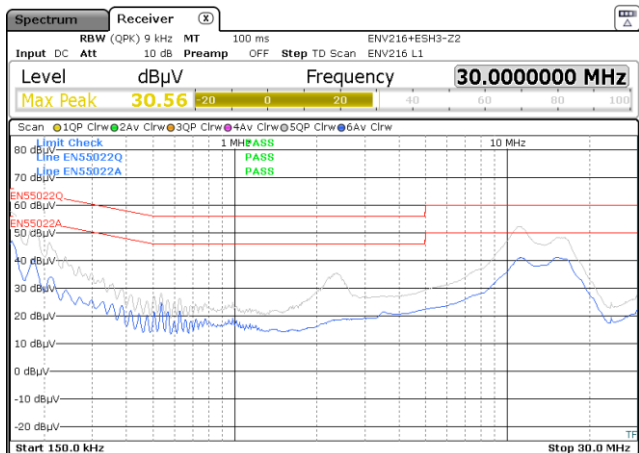


115 VAC<sub>IN</sub>. 230 VAC<sub>IN</sub>.  
**Figure 124** – Floating Ground EMI, 11 V / 2.45 A Load [Line Scan].

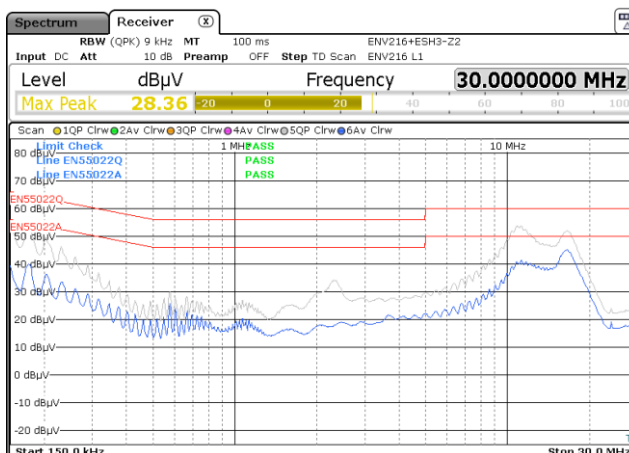


## 16.2 Output Ground Connected to Earth (QPK / AV)

### 16.2.1 5 V, 3 A



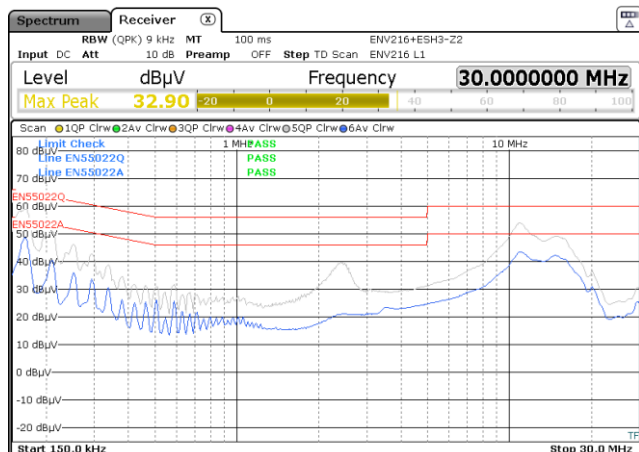
115 VAC<sub>IN</sub>.



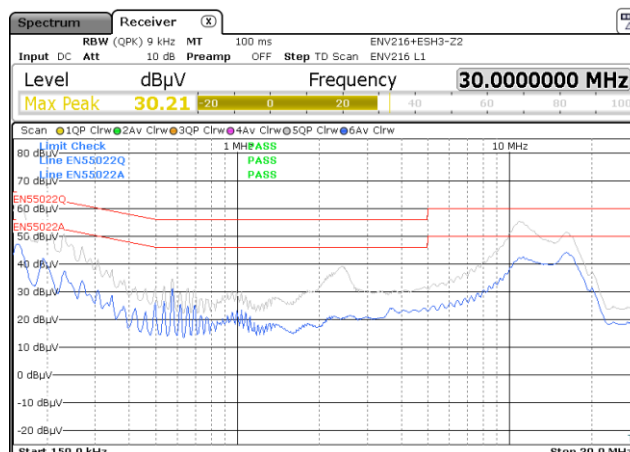
230 VAC<sub>IN</sub>.

**Figure 125** – Earth Ground EMI, 5 V / 3 A Load [Line Scan].

### 16.2.2 9 V, 3 A



115 VAC<sub>IN</sub>.

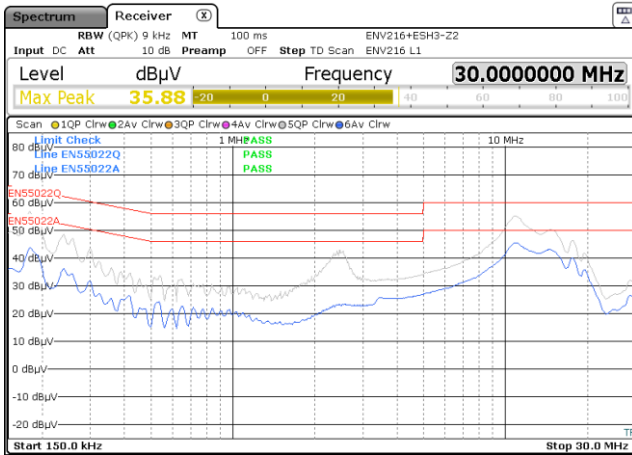


230 VAC<sub>IN</sub>.

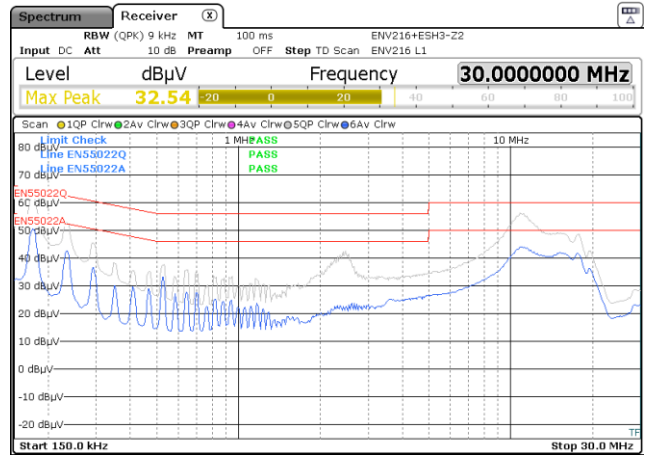
**Figure 126** – Earth Ground EMI, 9 V / 3 A Load [Line Scan].



16.2.3 15 V, 3 A



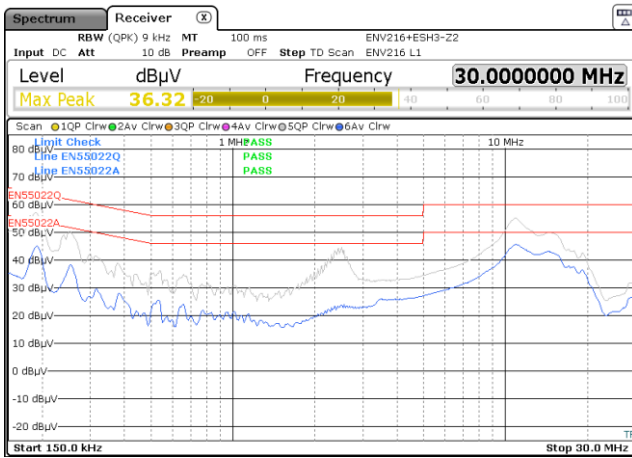
115 V<sub>AC\_IN</sub>.



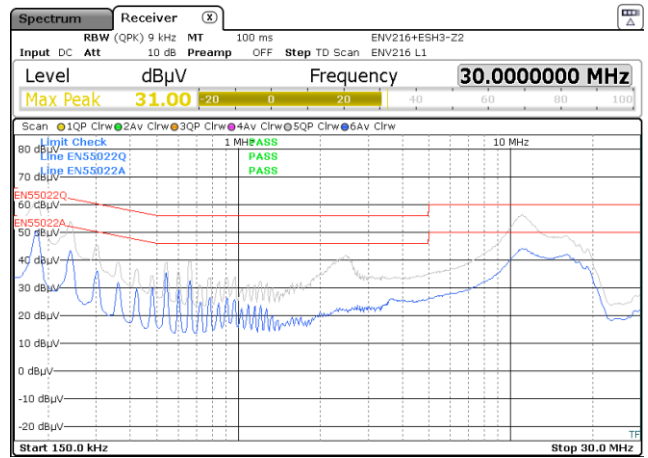
230 V<sub>AC\_IN</sub>.

Figure 127 – Earth Ground EMI, 3 V / 3 A Load [Line Scan].

16.2.4 20 V, 2.25 A



115 V<sub>AC\_IN</sub>.



230 V<sub>AC\_IN</sub>.

Figure 128 – Earth Ground EMI, 11 V / 2.45 A Load [Line Scan].



## 17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
18-Sep-18	SA	1.0	Initial Release.	Apps & Mktg
05-Oct-18	SA	1.1	Updated PCB Section.	
19-Feb-19	KM	1.2	Updated Figure 7 and BOM	



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