2SP0430V2B0C-FF1800R17IP5
SCALE-2™ Family

Gate Driver for 1700 V PrimePACK™ 3+ Power Modules
Supporting 3-level Applications
Optical I/O Interface

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for PrimePACK™ 3+ IGBT power modules with 1700 V blocking voltage
- Dual channel gate driver
- Optical I/O interface
- Secondary side power supply with reinforced insolation
- ±30 A peak output gate current
- 2 W output power per channel at maximum ambient temperature
- -40 °C to 85 °C operating ambient temperature

Protection / Safety Features

- Reinforced insulation between primary and secondary side
- Undervoltage lock-out (UVLO) protection for primary side (low voltage side) and secondary-side (high voltage side)
- Short-circuit protection
- Dynamic Advanced Active Clamping (DA^{2}C)
- Applied double sided conformal coating

Full Safety and Regulatory Compliance

- 100% production partial discharge and HIPOT test of transformer
- Clearance and creepage distances between primary and secondary sides meet requirements for reinforced isolation
- RoHS compliant

Applications

- Wind and PV power
- Traction inverter
- Industrial drives
- Other industrial applications

Description

The plug-and-play 2SP0430V2 gate driver family is optimized for operation of 1200 V and 1700 V PrimePACK™ 3+ power modules in 2-level and 3 level applications.

The gate driver features fiber optic interface and built-in DC/DC power supply with reinforced isolation. Enhanced level of protection is provided by implemented short-circuit monitoring.

Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range in IGBT off-state for up to 60 s.

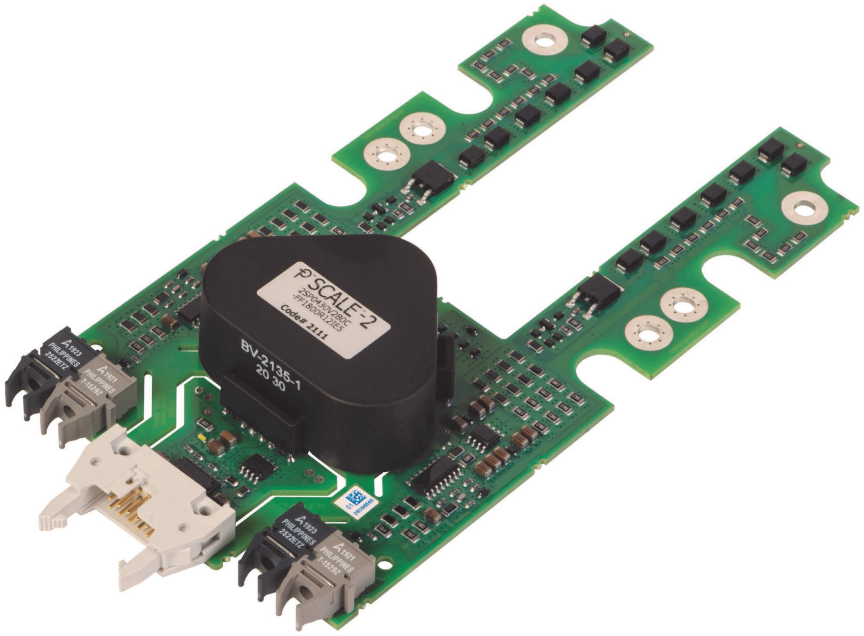

Figure 1. Board Photo.

Pin Functional Description

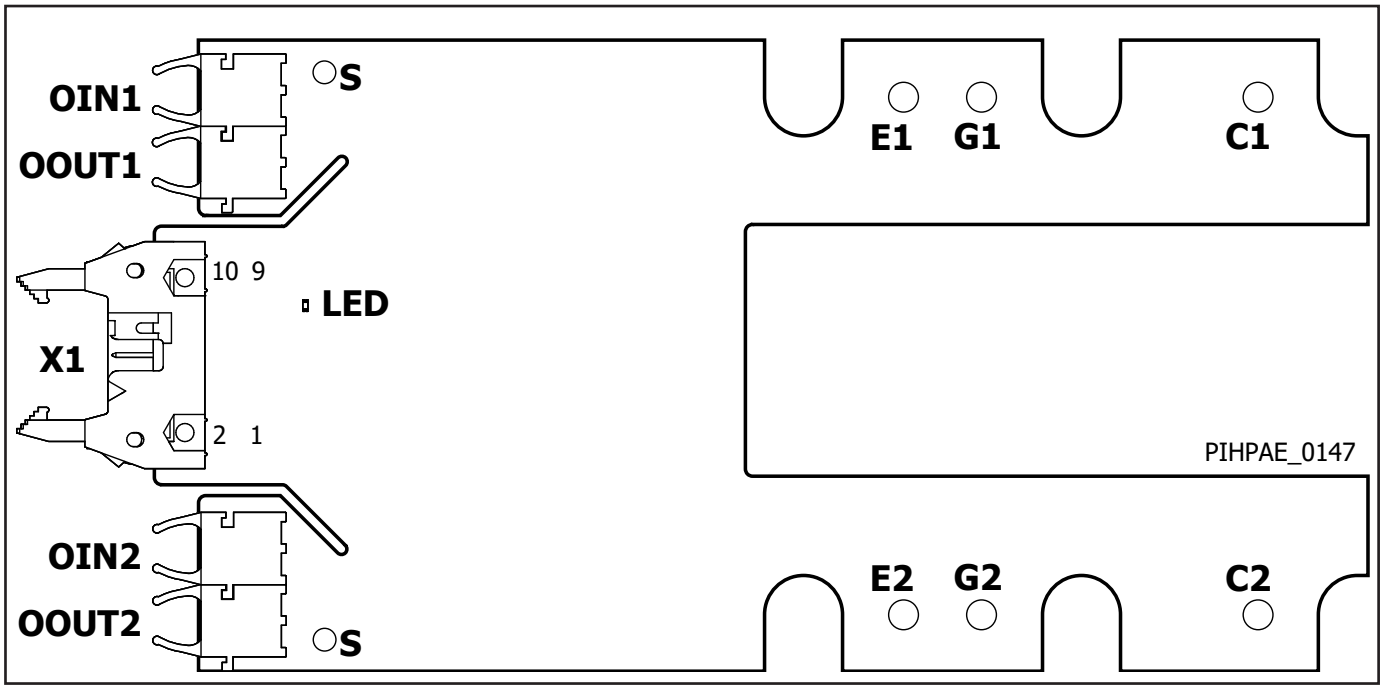

Figure 2. Pin Configuration.

Connector X1

To external power supply (N3793-5302RB from 3M, 71922-110LF from Amphenol FCI or similar).

VDC (Pin 1, 3)
These pins are the primary-side 15 V supply voltage connection for the integrated DC/DC converter. It is mandatory to use the same supply for VDC and VCC.

VCC (Pin 7, 9)
These pins are the primary-side 15 V supply voltage connection for the primary-side electronic. It is mandatory to use the same supply for VDC and VCC.

GND (Pin 2, 4, 5, 6, 8, 10)
These pins are the connection for the primary-side ground potential. All primary-side signals refer to these pins.

Optical Interface

Signal in- and output to superior controller.

OIN1
This is the optical receiver (Broadcom HFBR-2522ETZ) for the command input signal of channel 1.

OOUT1
This is the optical transmitter (Broadcom AFBR-1529Z) for the status output signal of channel 1.

OIN2
This is the optical receiver (Broadcom HFBR-2522ETZ) for the command input signal of channel 2.

OOUT2
This is the optical transmitter (Broadcom AFBR-1529Z) for the status output signal of channel 2.

Optical Indicator

LED
White optical indicator for monitoring the voltage V_{VCC}. During the absence of V_{VCC} the indicator is OFF.

Fixation Holes S

M3 holes for fixation points of stand-offs.

Functional Description

The 2SP0430V2 is a dual channel plug-and-play gate driver for PrimePACK™ 3+ power modules. The gate driver is available in different variants, which all provide reinforced isolation for all primary-side signals. The 2SP0430V2B0C for PrimePACK™ 3+ power modules features an isolation rating between primary-side and secondary-side of 9100 V_{RMS}.
As plug-and-play gate driver the 2SP0430V2 characteristics match the requirements of the individual power modules.
The operation of the channel 1 (low-side switch) and channel 2 (high-side switch) of the gate driver is independent from each other. Any dead time insertion, to avoid synchronous or overlapping switching of the driven power switches, has to be generated in the external system controller.

Note:
Synchronous or overlapping switching of top and bottom switches within a half-bridge leg may damage or destroy the driven power switche(s) and in conjunction as secondary failure the attached gate driver.

Power Supply

The 2SP0430V2 provides two power supply inputs. For both a typical supply voltage level of 15 V is required. The first input VDC supplies the integrated DC/DC converter, which generates the isolated voltage for the secondary-side gate driver channels. The positive rail of the gate driver channels has the voltage level V_{VISO} and the negative rail the voltage level V_{COM}. Both are referenced to the emitter potential at terminal E1 or E2 of the driven power semiconductor.
The second input VCC supplies the primary-side electronic of the gate driver. It is mandatory to provide the supply for VDC and VCC from the same source.

Under Voltage Monitoring

The supply voltages are closely monitored. In case of an UVLO on the secondary-side, the fault condition will be signalized on the fiber optic status signal OOUTx with a light off and the corresponding power semiconductor will be turned off.

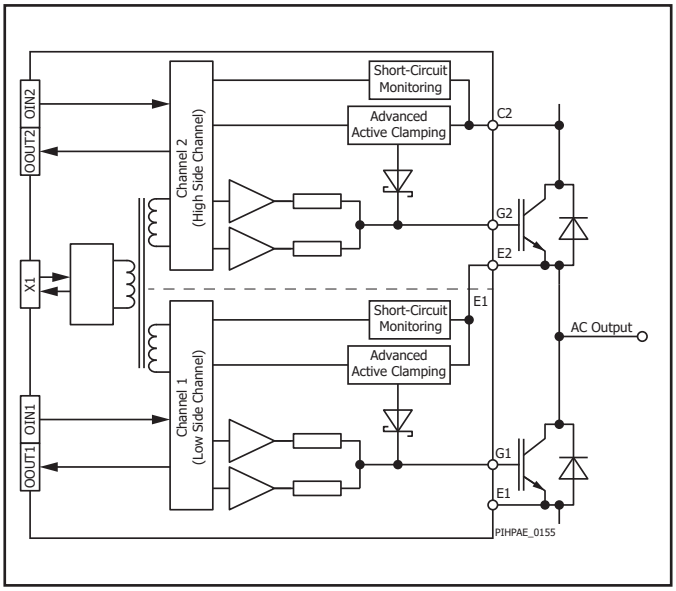

Figure 3. Functional Block Diagram.

Optical Input (OINx)

This is the edge-triggered command input signal to drive attached power semiconductor. A light signal at the input OINx will turn-on the gate of the power semiconductor. Accordingly, no light signal will turn-off the gate.
Gate driver signal is transferred from OIN to the gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

Optical Output (OOUTx)

During normal operation (i.e. the gate driver is supplied with power at nominal voltage, and there is no fault anywhere), the status feedback is given by a light on signal at the optical link. A failure condition is signaled by a light off signal.
Each edge of the control signal is acknowledged by the gate driver with a short pulse (the light is off for a period of t_{ack}). Because this can be observed by the external controller, this method allows simple and continuous monitoring of the driver and fiber-optic link. Figure 4 shows the control and response signals of a given driver in normal operation.
In case of a detected short-circuit of the driven power module the corresponding status feedback light OOUTx is set to OFF for a duration of t_{blk} after a delay of $t_{D,Fault}$ referred to the edge of the received light signal on OINx. The gate is turned off after the time $t_{P(HL),Fault}$ and blocked for t_{blk}. Figure 5 illustrates the timing of the fiber optic interface in fault (here short circuit) operating conditions.
In case of a detected under voltage lock-out condition (UVLO) on the secondary-side the corresponding status feedback light OOUTx is set to OFF as long as the UVLO condition is present. During fault condition no gate signal is transmitted to the respective gate driver channel.

Gate Voltage

2SP0430V2 possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage $V_{GE(on)}$ of the power semiconductor equals in steady state the positive supply voltage V_{VISO}.
The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no load conditions and is increasing slightly (i.e. getting less negative) with increasing load.
In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection

The gate driver uses the semiconductor desaturation effect to detect short-circuits. The desaturation is monitored by using a resistive sensing network. At turn-on the collector-emitter voltage is checked after the response time t_{res} to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(stat)}$, the driver detects a short-circuit condition. A fault signal is transmitted to optical status output OOUTx immediately. The monitored semiconductor is switched off after the delay a $t_{P(HL),Fault}$.

Gate Clamping

In the event of a short-circuit condition the gate voltage is increased due to the high dv_{CE}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{CE}/dt is driving a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to

a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor.
To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage the gate driver features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{ISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. As a result the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enables a safe turn-off of the device.

Dynamic Advanced Active Clamping (DA²C)

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the collector through transient voltage suppressor (TVS) diodes to the gate. The driver contains Power Integrations' Dynamic Advanced Active Clamping (DA²C) based on this principle:
When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping (AAC) – is mainly integrated in the secondary-side ASIC of the gate driver.
Additional TVS diodes have been added in series to the TVS diodes required to withstand the maximum DC-link voltage under non-switching operation. These TVS diodes are short-circuited during the IGBT on state as well as for about 15...20 µs after the turn-off command to guarantee efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature, illustrated in Figure 6 – together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). The time during which the voltage can be applied above the value for switching operation has to be limited to short periods (< 60 s).

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.
Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

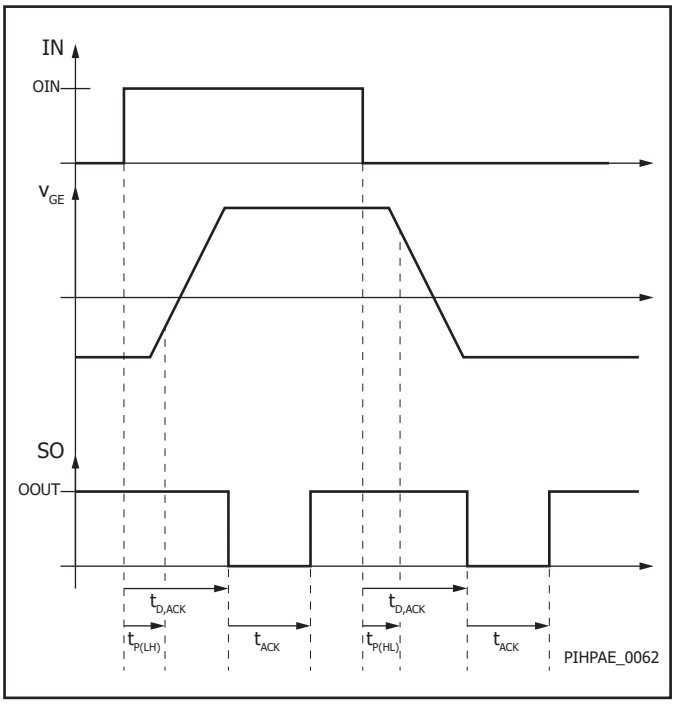

Figure 4. Fiber Optic Feedback in normal operation mode.

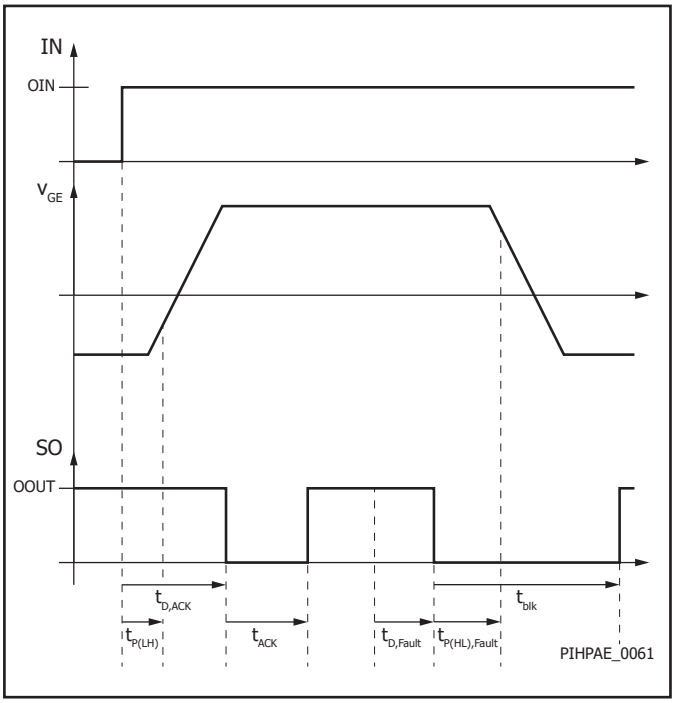

Figure 5. Fiber Optic Feedback in fault (short-circuit) operation mode.

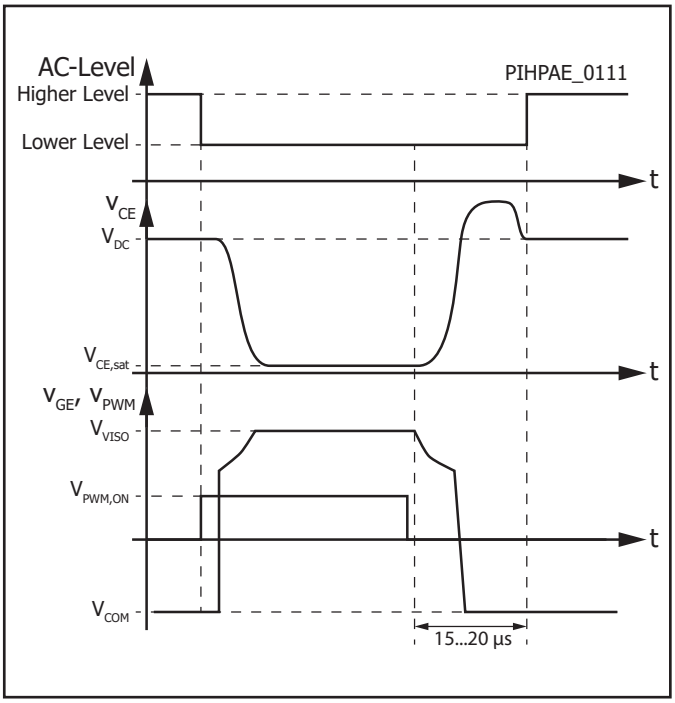

Figure 6. Dynamic Advanced Active Clamping (DA²C).

Maximum Ratings

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C	Min	Max	Units
Maximum Ratings[1]					
Primary-side supply voltage	V_{VDC}	VDC to GND	0	16	V
	V_{VCC}	VCC to GND	0	16	
Primary-side supply current	I_{VDC}			750	mA
Switching frequency	f_{SW}			10	kHz
Gate output power	P_G			2	W
Gate output current	I_G			30	A
Primary to secondary side operating voltage	$V_{op,PS}$	transient only		2050	V
		permanently applied		1500	
DC-link voltage	$V_{DC\text{-}Link}$	permanently		1250	V
		off-state only, limited to 60s		1500	
Test voltage	$V_{iso,PS}$	Primary side to secondary side, 50 Hz, 60 s		9100	V_{RMS}
	$V_{iso,SS}$	Secondary side to secondary side, 50 Hz, 60 s		6000	
Storage temperature[2]	T_{st}		-40	50	°C
Operating ambient temperature	T_A		-40	85	°C
Surface temperature[3]	T_{surf}			125	°C
Relative humidity	H_r	No condensation		93	%
Altitude of operation	A_{op}	Operation above this level requires a voltage derating to ensure proper isolation coordination.		2000	m

Recommended Operating Conditions

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{VDC}	VDC to GND	14.5	15	15.5	V
	V_{VCC}	VCC to GND	14.5	15	15.5	

Characteristics

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Units
Power Supply						
Supply current	I_{VDC}	V_{VDC} = 15 V, without load		118		mA
		V_{VDC} = 15 V, $P_G = P_{G,max}$		419		
	I_{VCC}			22		
Power supply monitoring threshold (secondary side)	$UVLO_{VISO-E}$	Clear fault (resume operation)	11.6	12.6	13.6	V
		Set fault (suspend peration)	11.0	12.0	13.0	
		Hysteresis	0.35			
	$UVLO_{COM-E}$	Clear fault (resume operation)		-5.15		V
		Set fault (suspend peration)		-4.85		
		Hysteresis		0.3		
Output voltage (secondary side)	$V_{VISO-COM}$	V_{VDC} = 15 V, without load		24.3		V
		V_{VDC} = 15 V, $P_G = P_{G,max}$		23.8		
Coupling capacitance	C_{io}	Primary-side to secondary-side		6		pF
Gate Output						
Gate turn-on voltage	$V_{GE(on)}$	V_{VDC} = 15 V, without load		15		V
		V_{VDC} = 15 V, $P_G = P_{G,max}$		15		
Gate turn-off voltage	$V_{GE(off)}$	V_{VDC} = 15 V, without load		-9.3		V
		V_{VDC} = 15 V, $P_G = P_{G,max}$		-8.8		
Turn-on gate resistor	$R_{G(on)}$			0.5875		Ω
Turn-off gate resistor	$R_{G(off)}$			5.875		Ω

Characteristics (cont.)

Parameter	Symbol	Conditions T_A = +25 °C	Min	Typ	Max	Units
Timing Characteristics						
Turn-on delay	$t_{P(LH)}$	OIN to 50% of $V_{GE(on)}$, no load attached, optical cable length 1 m		170		ns
Turn-off delay	$t_{P(HL)}$	OIN to 50% of $V_{GE(off)}$, no load attached, optical cable length 1 m		170		ns
Transmission delay of fault state	$t_{D,Fault}$	Optical cable length 1 m		70		ns
Turn-off delay after Fault	$t_{P(HL),Fault}$			120		ns
Blocking time	t_{blk}	Delay to clear fault state		10		µs
Acknowledge delay time	$t_{d(ack)}$	Optical cable length 1 m		170		ns
Acknowledge pulse width	t_{ack}	Measured on the external controller side, optical cable length 1 m	400	600	1050	ns
Short-Circuit Protection						
Static V_{CE}-monitoring threshold	$V_{CE(stat)}$			54		V
Response time	t_{res}	DC-link voltage = 1250 V		7.0		µs
		DC-link voltage = 1000 V		7.1		
		DC-link voltage = 800 V		7.4		
		DC-link voltage = 600 V		8.2		
Electrical Isolation						
Test voltage[4]	$V_{iso,PS}$	Primary side to secondary side, 50 Hz, 60 s	9100			V_{RMS}
	$V_{iso,SS}$	Secondary side to secondary side, 50 Hz, 60 s	6000			
Partial discharge extinction voltage[5]	$V_{PD,PS}$	Primary side to secondary side	3100			V_{pk}
	$V_{PD,SS}$	Secondary side to secondary side	2100			
Creepage distance	$CPG_{PS,PCB}$	Primary side to secondary side, on the PCB, material group IIIa	27			mm
	CPG_{SS}	Secondary side to secondary side, on the PCB, material group IIIa	7			
Clearance distance	CLR_{PS}	Primary side to secondary side	12.6			mm
	CLR_{SS}	Secondary side to secondary side	7			
Mechanical Characteristics						
Connection torque	$M_{Terminal}$	Terminals (Cx, Gx and Ex), M4 screw	1.8		2.1	Nm
Bending	l_{bend}	According to IPC			0.75	%

NOTES:
1. Stresses beyond those listed under maximum ratings may cause permanent damage to the device.
2. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85 °C.
3. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
4. The transformer of every production sample has undergone 100% testing at the given value for 1s.
5. Partial discharge measurement is performed on each transformer.

Reliability and EMC Qualification Items

Test Item	Test Methods and Conditions
Environmental Tests	
IEC 60068-2-6, Ed. 7.0, 2007-12	Fc (Sinusoidal Vibration): Frequency range: 5Hz - 200Hz, amplitude: 10m/s², axis: x, y, z, sweep cycles per axis: 1
IEC 60068-2-11, Ed. 3.0, 1981-01	Ka (Salt mist): Concentration 5% NaCl by weight, Duration 48h
IEC 60068-2-14, Ed. 6.0, 2009-01	Nb (Change of temperature): Temperature: -40°C, 85°C, rate of change: 5 K/min, cycles: 2
	Nb (Change of temperature): Temperature: -40°C, 125°C, rate of change: 5 K/min, cycles: 100
IEC 60068-2-27, Ed. 4.0, 2008-02	Ea (Shock): Acceleration: 150m/s², shocks per axis: 100, axis: ±x, ±y, ±z
IEC 60068-2-78, Ed. 2.0, 2012-10	Cab (Damp heat, steady state): Temperature: 40°C, humidity: 93% RH, duration: 21d
	Cab (Damp heat, steady state): Temperature: 85°C, humidity: 85% RH, duration: 21d, powered
EMC Tests	
IEC 61000-4-2, Ed.2, 2018-12	Electrostatic discharge immunity test: accessible interfaces, test level 1, class A, contact discharge with ±2kV (10 pulses each), air discharge with ±2kV (10 pulses each)
IEC 61000-4-4, Ed. 3.0, 2012-04	Electrical fast transient/burst immunity test: Primary side electrical interfaces, test level 3, class A, power ports: ±2kV, 5kHz, 300ms, Duration per test: 60s
IEC 61000-4-6, Ed. 4.0, 2013-10	Immunity to conducted disturbances, induced by radio-frequency fields: Test of accessible interfaces, test level 2, class A, voltage level: $3V_{RMS}$, 150 kHz to 80 MHz

Product Dimensions

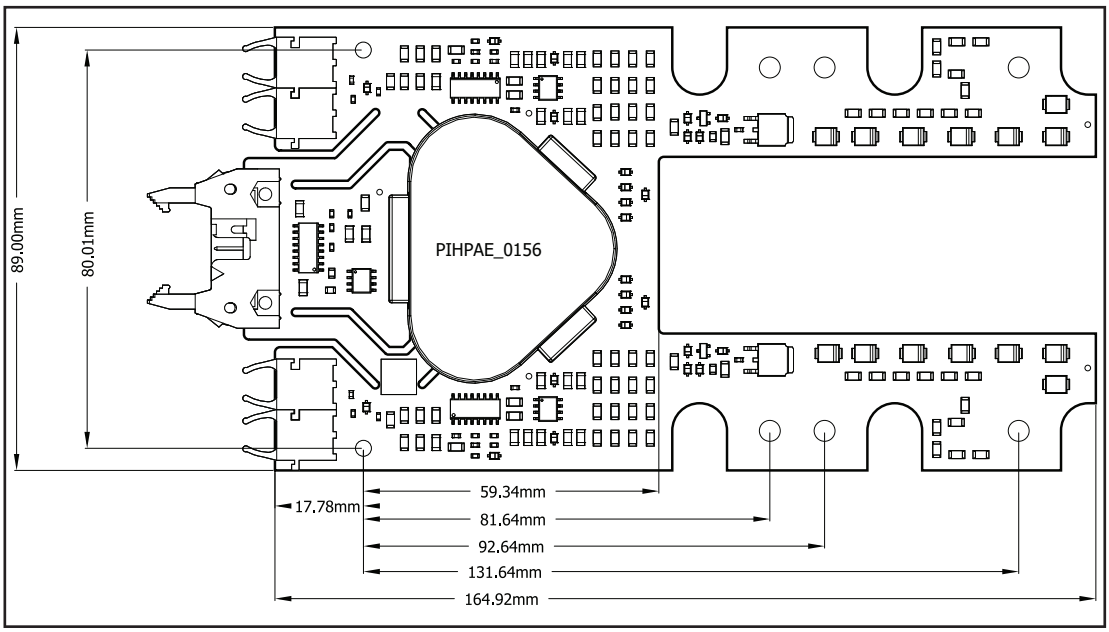

Figure 7. Top View

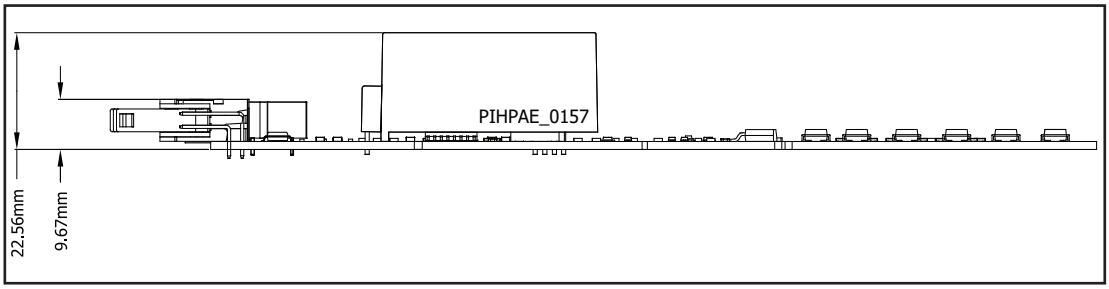

Figure 8. Side View.

Product Details

Part Number	Power Module	Voltage Class	Current Class	Package	Power Device Supplier
2SP0430V2B0C-FF1800R17IP5	FF1800R17IP5	1700 V	1800 A	PrimePACK™ 3+	Infineon

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Revision	Notes	Date
C	Final Datasheet.	11/21

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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