Application Note AN-66
LYTSwitch-3 Family

Design Guide

Introduction

The LYTSwitch™-3 family is ideal for single-stage power factor corrected constant current LED drivers for bulbs and recessed lighting up to 20 W. Each device combines a high-voltage power MOSFET, variable frequency and on-time control engine, fast start-up with soft-finish, selectable dimming curves with load shutdown at deep dimming and protection functions including instantaneous line over-voltage shutdown, output short-circuit auto-restart, output overvoltage latch-off and thermal-foldback with over-temperature-shutdown into a single package, thus greatly reducing component count. Its internal feedback controller is capable of indirect and direct output current sensing that can be set via external programming resistor, thus eliminating the need for optocoupler, especially with isolated design applications.

The integrated 725 V power MOSFET provides a large Drain voltage margin in high-line input AC applications, thus increasing reliability. A 625 V power MOSFET option is also offered to reduce cost in applications where the voltage stress on the power MOSFET is low.

Topology neutral LYTSwitch-3 operates in discontinuous conduction mode (DCM) for tight tolerance output current regulation over line input range and operating temperature, high power factor with significantly low harmonic currents via its internal control algorithm. The combination of a low-side switching topology, cooling via electronically quiet SOURCE pins, frequency jitter and DCM operation which inherently eliminates reverse current from the output diode when the power MOSFET is in OFF-state reducing high frequency noise allow the use of a simple and small input pi filter yet produces low EMI and audible noise during dimming (e.g. low input capacitance reduces THD and increases PF).

All LYTSwitch-3 ICs have a built-in TRIAC detector that discriminates accurately between leading-edge and trailing-edge type dimmers. This capability together with load monitoring circuitry regulates bleeder current during each AC line half-cycle. The controller disables the bleeder circuit completely if no dimmer is detected, significantly increasing efficiency.

Output Power Table

Product	Output Power
	85-132 VAC or 185-265 VAC
LYT33x4D	5.7 W
LYT33x5D	8.8 W
LYT33x6D	12.6 W
LYT33x8D	20.4 W

Table 1. LYTSwitch-3 Output Power Table.

Typical Circuit Configuration

The LYTSwitch-3 device family is topology neutral and can be used in any switching configuration such as buck (tapped-buck), buck-boost (tapped buck-boost), boost and flyback (isolated and non-isolated) making it broadly applicable to any design requirement regardless of LED voltage string. The high level integration of LYTSwitch-3 family enables ease of design optimization both in converter side and bleeder circuit resulting in shortened development time.

Circuit in Figures 1 and 2 show a typical low component count TRIAC dimmable LED driver using LYTSwitch-3 in Buck and Buck-Boost configuration respectively.

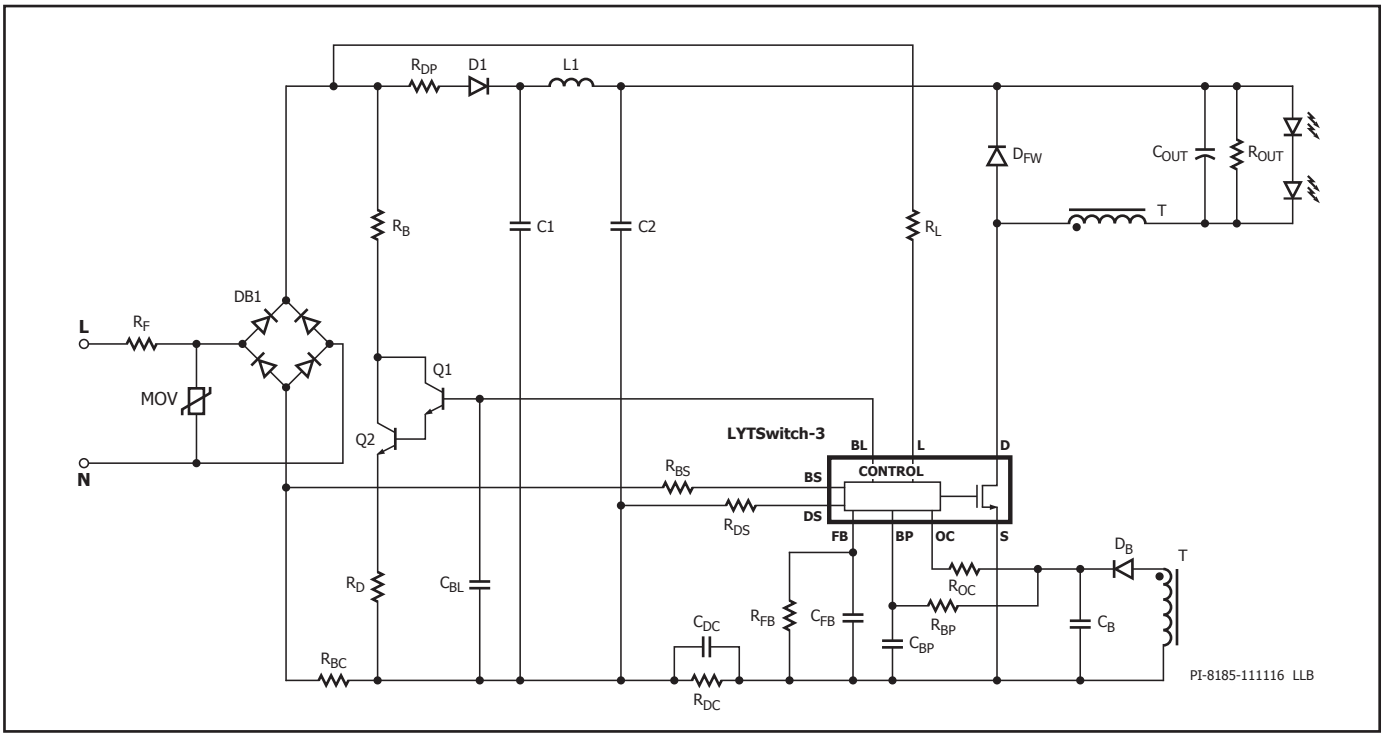

Figure 1. Low Component Count Typical Circuit Dimmable Low-Line Buck Topology with LYTSwitch-3 (30 External Components; R_{OUT} is Optional Component).

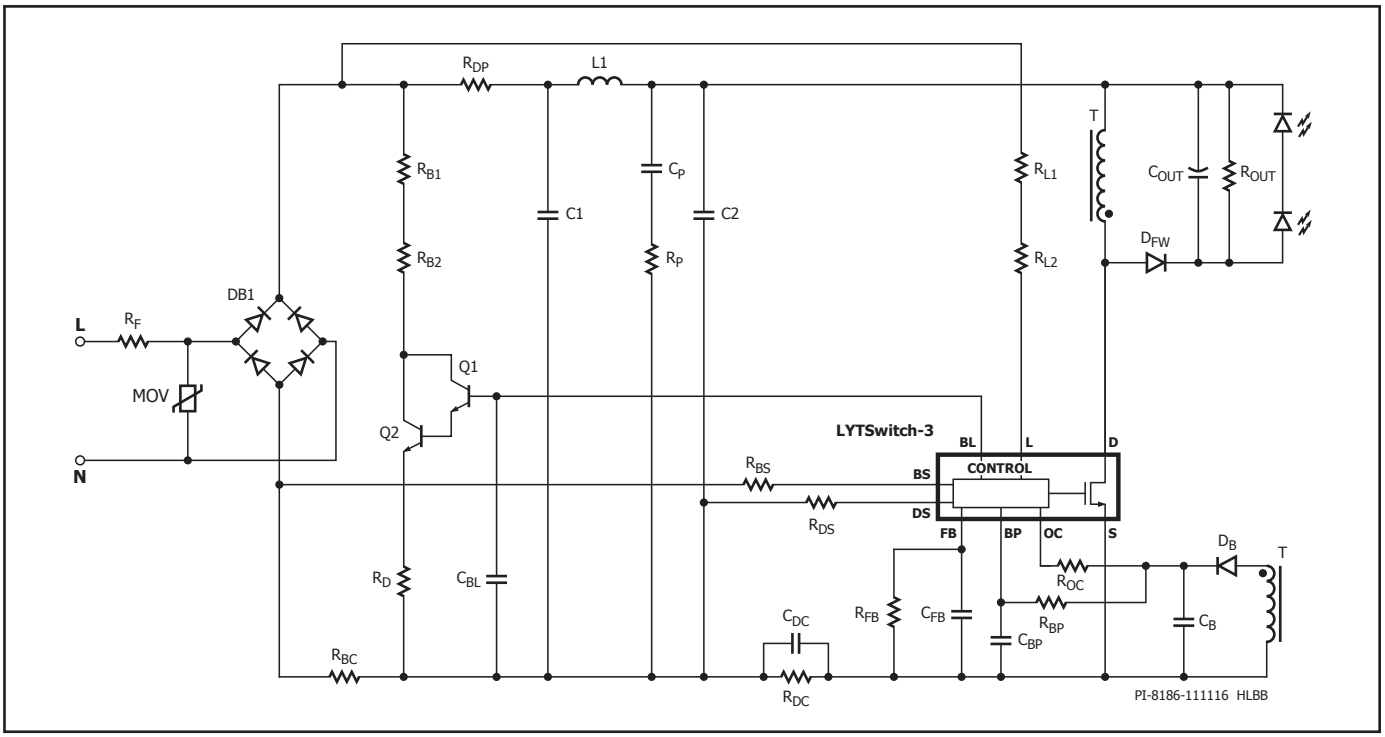

Figure 2. Low Component Count Typical Circuit Dimmable High-Line Buck-Boost Topology with LYTSwitch-3 (31 external components; R_{OUT} and R_{L1} are Optional Components).

Notice some minor differences in the bleeder circuit configuration between the low-line driver circuit – Figure 1 and the high-line driver circuit – Figure 2. Other than topology, using two resistors (R_{L1} and R_{L2}) for the LINE-SENSE pin to handle higher voltage stress if using 1/4 W resistor (one is sufficient if 1/2 W is to be used) and two bleeder resistors (R_{B1} and R_{B2}) to increase thermal handling capacity at high-line, the main difference is that a passive RC bleeder (R_P and C_P) was employed for stronger damping capability because there is much higher energy ringing can be generated at high-line when the TRIAC dimmer turns on, while the low-line design did not have the RC bleeder, the ringing energy is much less. However, it employed a blocking diode (D1) to keep the energy stored in the input filter from discharging current through the active bleeder which could consequently pull less current from the dimmer making the TRIAC turn-off prematurely, especially at low conduction angle.

Scope

This application note is intended for users designing an AC-DC LED driver using LYTSwitch-3 family devices. A simplified step-by-step instruction will guide the user in selecting key components, especially in designing the magnetics necessary to quickly jump start the design process and come up with a sound prototype design. This application note refers directly to the PIXIs design spreadsheet that is a part of the PI Expert™ design software suite (https://piexpertonline.power.com/site/login).

In this application note the user may also find product Reference Design Kits (RDK) and Design Engineering References (DER) useful. These contain a prototype board, a link to an engineering report that contains complete design information including gerber for the printed circuit-board (PCB) and test data and product samples. Further details on downloading PI Expert, RDKs and updates to this document can be found at Power Integrations' website www.power.com.

Choosing Switching Topology

The LYTSwitch-3 device family can be used in any switching topology configuration such as buck (tapped-buck), buck-boost (tapped buck-boost), boost and flyback (isolated and non-isolated) making it broadly applicable to any design requirement regardless of LED voltage string. Choosing the right topology to use can be challenging at times, however using LYTSwitch-3 the designer only needs to know is the output voltage and efficiency merit in choosing the suitable topology to use. Table 2 shows a quick selection guide.

Ouput Voltage (V)		Recommended Topology					Remark
Low-Line	High-Line	Tapped-Buck	Buck	Buck-Boost	Boost	Flyback	
< 12	< 25	✓					Limited by maximum duty of device at minimum input voltage
13 – 60	27 - 100		✓				Minimum voltage is limited by maximum on-time of device at maximum input
> 24	> 48			✓			Maximum output voltage is limited by transistor breakdown voltage
$V_{OUT} > V_{IN}$					✓		
Any Voltage						✓	
Minimum Efficiency Estimate		>80	>87	>85	>90	75-87	

Table 2. Recommended Topology Selection Guide.

Design Example

Design an 8 W TRIAC dimmable non-isolated LED driver using a LYTSwitch-3 device and having an output voltage of 72 V, output current of 115 mA, ±5% regulation tolerance with an input voltage range of 195 VAC to 265 VAC and 85% minimum efficiency. Output current should shutdown at low conduction angle to avoid light output shimmer. (Refer to DER-524 for complete report through this link https://led-driver.power.com/design-support/reference-designs/design-examples/der-524-8-w-triac-dimmable-high/)

Step-by-Step Design Procedure

For this particular specification a buck-boost topology is suitable, hence the corresponding PIXIs designer spreadsheet will be used. Visit https://piexpertonline.power.com/site/login

Step 1- Enter Application Variables

2	ENTER APPLICATION VARIABLES				Design Title
3	VACMIN		195.0	Volts RMS	Minimum AC line voltage.
4	VACNOM		230.0	Volts RMS	Nominal AC line voltage.
5	VACMAX		265.0	Volts RMS	Maximum AC line voltage.
6	FL		50	Hertz	AC line frequency.
7	VO_MIN		64.8	Volts DC	Guaranteed minimum VO that maintains output regulation.
8	VO	72.0	72.0	Volts DC	Worst case normal operating output voltage.
9	VO_OVP_MIN		85.4	Volts DC	Minimum Voltage at which output voltage protection may be activated.
10	IO	115.0	115.0	m-Amperes	Average output current specification.
11	EFFICIENCY	0.87	0.87	Dimensionless	Total power supply efficiency.
12	Z		0.50	Dimensionless	Loss allocation factor.
13	PO		8.28	Watts	Output power.

Figure 3. Application Variables Section of the PIXIs Design Spreadsheet.

Enter Input Voltage and Line Frequency: VACMIN [C3], VACNOM [C4], VACMAX [C5], FL [C6]

LYTSwitch-3 devices are intended for single range input voltages applications. Optimum electrical performance, dimmer compatibility and cost are best achieved with a single input voltage range as opposed to wide input voltage range which will require bigger components for both converter and bleeder circuits.

Enter Output Parameters: VO [C8], IO [C10], Efficiency [C11], Z [C12]

In a high power factor single-stage LED driver, the output will have significantly large low frequency ripple with twice the frequency of the input line, it is recommended to use a power meter when measuring the output power for accuracy. P_O [E13] is calculated based on the integral product of V_O [C8] and I_O [C10], which is used to choose device size.

Region	Nominal Input (VAC)	Minimum Input (VAC)	Maximum Input (VAC)	Nominal Frequency (Hz)
Japan / USA	100/115	85	132	50/60
Europe / Rest of World	230/240	195	264	50/60
Lighting in commercial buildings in USA, (208 VAC phase-to-phase)	208/277	177	308	60

Table 4. Standard Worldwide Input Line Voltages and Line Frequencies.

$$PO = \int IO_{(t)} \times VO_{(t)} dt$$

LYTSwitch-3 ICs have built-in latching output overvoltage protection (OVP). Once the current exceeds the I_{OOV} threshold via the OUTPUT COMPENSATION pin the IC will trigger a latch to disable switching thus preventing the output from rising further. Recycling the AC supply is needed to reset this protection mode from latch-off state.

The minimum voltage at which output voltage protection may be activated is calculated in cell VO_OVP_MIN [E9].

$$VO_{OVP(MIN)} = (R_{OC} \times I_{OOV} + V_{OC}) \times \frac{N_S}{N_B}$$

Where:
R_{OC} is the feedback resistor connected to OUTPUT COMPENSATION pin from the bias supply. Typical resistance value set at 100 µA I_{OC} current for nominal output voltage and output current.

$$R_{OC} = \frac{V_{BIAS} - V_{OC}}{100\ \mu A}$$

I_{OOV}: Latching overvoltage current threshold. Minimum limit - 127 µA.
V_{OC}: OUTPUT COMPENSATION pin voltage. Typical - 2.25 V.
NS: Output winding turns.
NB: Bias winding turns.

The output overvoltage is detected through the bias supply which is calculated in the PIXIs. The accuracy actual overvoltage trigger point will be dependent on the magnetic coupling between bias and output winding.

For direct output voltage sensing, NS/NB = 1. Or for PIXIs calculation, enter VBIAS [E76] = VO [C8].

Efficiency [C11], η
Use efficiency estimate in Table 2. Once the actual unit is available enter the measured efficiency for fine tuning the output current.

$$\eta = \frac{PO}{P_{IN}}$$

Loss Allocation Factor, Z [E12]
Allocation factor is the ratio of output and total loss. It is used in the efficiency of the DC-DC section of the converter for calculating the input power and drain current as seen by LYTSwitch-3 IC. Typical value is 0.5.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

Step 2 - LYTSwitch-3 Design Variables

17	**LYTSwitch-3 DESIGN VARIABLES**				
18	BREAKDOWN VOLTAGE	725	725	Volts DC	Choose between 650V and 725V.
19	GENERIC DEVICE	LYT33X5D	LYT33X5D		Chosen LYTSwitch-3 generic device.
20	ACTUAL DEVICE		LYT3325D		Chosen LYTSwitch-3 device code.
21	ILIMITMIN		1.232	Amperes	Minimum device current limit.
22	ILIMITTYP		1.325	Amperes	Typical Current Limit.
23	ILIMITMAX		1.418	Amperes	Maximum Current Limit.
24	IP_MOSFET		1.193	Amperes	Worst case peak drain current of the MOSFET.
25	TONMIN		1.208	u-seconds	Worst case minimum on-time of the MOSFET.
26	DC_MAX		0.171	Dimensionless	Worst case maximum duty cycle of the MOSFET.
27	IAVG_MOSFET		0.042	Amperes	Worst case average drain current of the MOSFET.
28	IRMS_MOSFET		0.158	Amperes	Worst case maximum RMS current of the MOSFET.
29	KDP		1.513	Dimensionless	Ratio between off-time of the MOSFET and on-time of the secondary diode.
30	VDRAIN		490.8	Volts DC	Estimated worst case drain voltage of the MOSFET.

Figure 4. LYTSwitch-3 Design Variables Section of PIXIs Design Spreadsheet.

The ACTUAL DEVICE [C20] will be automatically selected based on the output power calculated and input voltage. In the BREAKDOWN VOLTAGE [C18] cell, a 725 V part is automatically chosen for high-line input, while 650 V for low-line input. However, the user can override the default selection dependent on the requirement and choose a 650 V part, if the actual measured stress voltage on the power MOSFET is much less than 650 V and / or choose a device with smaller power MOSFET, if the thermal condition is not critical.

The corresponding data sheet current limit specifications (ILIMIT(MIN) [E21], ILIMIT(TYP) [E22], and ILIMIT(MAX) [E23]) of the selected device are displayed, which are needed for calculating other design magnetic parameters.

MOSFET Peak Current, IP_MOSFET [E24]
To ensure DCM operation, the theoretical highest operating peak current should not exceed device minimum current limit of device.

Minimum "ON" Time, TONMIN [E25]
The minimum on-time operation is based on the minimum output voltage VO_MIN [E7] to ensure tight output current regulation.

Maximum Duty Cycle, DC_MAX [E26]
The maximum operating duty cycle (DC_MAX) is based on the maximum tolerance of output voltage (assumed to be 110%) to ensure tight output current regulation.

Device MOSFET Average and RMS Currents, IAVG_MOSFET [E27], IRMS_MOSFET [E28]
MOSFET average current (IAVG_MOSFET) and RMS current (IRMS_ MOSFET) are given to estimate the conduction loss of device MOSFET.

Ripple to Peak Current Ratio, KDP [E29]
KDP > 1 is maintained up to 110° conduction angle in the dimming curve to ensure discontinuous conduction mode of operation (Figure 4).

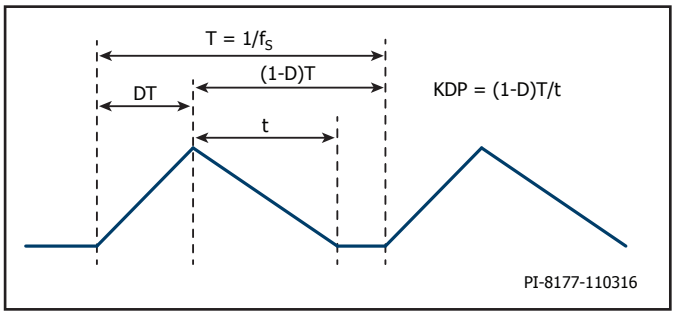

Figure 5. Inductor Current Illustration. KDP of > 1 Ensures Discontinuous Conduction Mode (DCM) of Operation.

MOSFET Drain to Source Voltage Stress, VDRAIN [E30]
Drain to Source voltage stress (VDRAIN) is calculated based on maximum input voltage and 120% of VO to account for overvoltage condition.

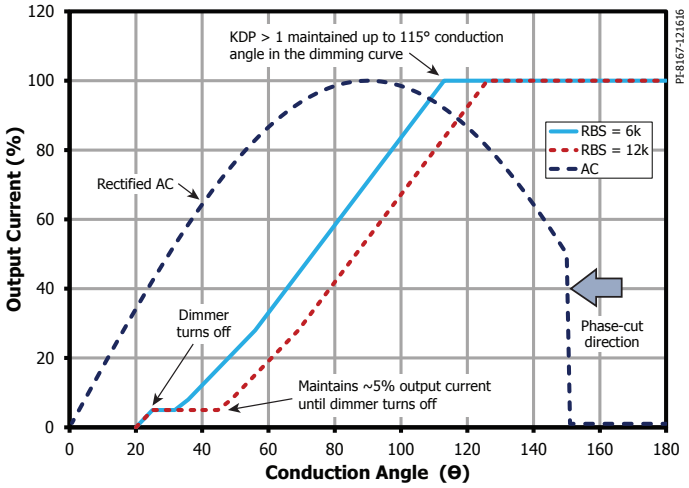

Figure 6. Graph shows Maximum Dimming Curve with RBS = 6 kΩ and Minimum Dimming Curve with RBS = 12 kΩ Dimming Curve Programming Resistor. KDP > 1 is Maintained up to the Knee of the Dimming Curve as Shown in the Graph.

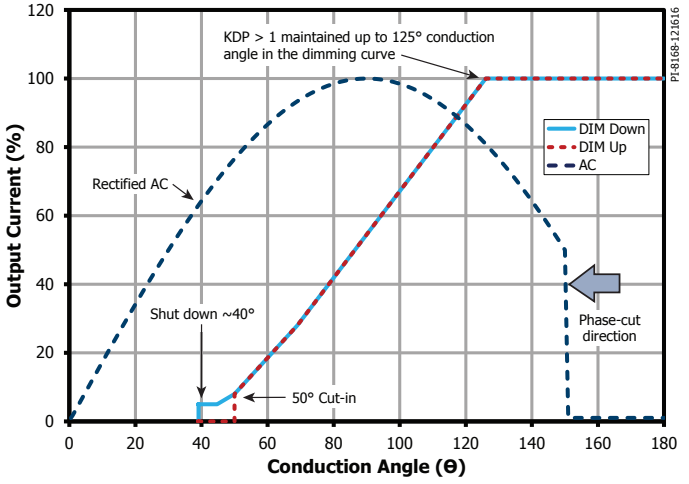

Figure 7. Minimum Dimming Curve with RBS = 12 kΩ Dimming Curve Programming Resistor with Load Shut Down (LSD).

Step 3 – Device Programming Parameters

34	DEVICE PROGRAMMING PARAMETERS				
35	RBS	24	24	k-ohms	Dimming curve programming resistor: Load shutdown using dimming curve 1.
36	RDS		6	k-ohms	Current sense programming resistor connected to the DS pin for the buck-boost converter.

Figure 8. Device Programming Parameters Input of the Design Spreadsheet.

Dimming Curve Selection RBS [C35]

LYTSwitch-3 device dimming is a closed loop function with respect to conduction angle in which dimming is achieved by adjusting the internal feedback voltage reference (VFB) of the IC in the same direction as the TRIAC conduction angle, which is measured from the input bus via a resistor to the LINE-SENSE (L) pin. As the TRIAC conduction angle decreases or increases, the FEEDBACK (FB) pin voltage (VFB) proportionally increases or decreases respectively (see Figure 10). Many dimmers available in the market have limited maximum conduction angle (e.g. < 130°) that when an incandescent or a LED bulb is connected to such dimmer, loses light output significantly. To maintain light output brightness, LYTSwitch-3 devices maintain full output current regulation up to approximately 115° conduction angle before it starts reducing output current to dim the light. The VFB is maintained at 300 mV up to 115° and reduced proportionally with 5% (~15 mV) until load shutdown if enabled, is activated or the TRIAC stops conducting due to lack of holding current (see Figures 6 and 7).

Depending on the designer's dimming preference, there are three (3) dimming curves to choose from, which can be programmed through a selection of R_{BS} resistor value shown in Table 5. The 24 kΩ R_{BS} selection has Load Shut Down (LSD) feature, in which the IC terminates the switching once conduction angle falls below 40° and remains off unless the conduction angle increases above 50º (see Figure 7). During the LSD condition the bleeder is active to keep the TRIAC dimmer conducting to minimize pop-on and dead travel. Should the TRIAC unable to maintain conducting, the bleeder would still be active to keep the input voltage from rising due to a leakage current from the dimmer, this prevents possible ghosting or fluttering of the light output while the dimmer is off. Usually the voltage leaks via the pilot lamp and / or a large internal shunt capacitor of a dimmer.

The 6 kΩ and 12 kΩ R_{BS} selections offer no-Load Shut-Down (LSD) feature, while both have extended dimming range, the 12 kΩ R_{BS} selection has the widest dimming range among the dim curves. See Figure 6.

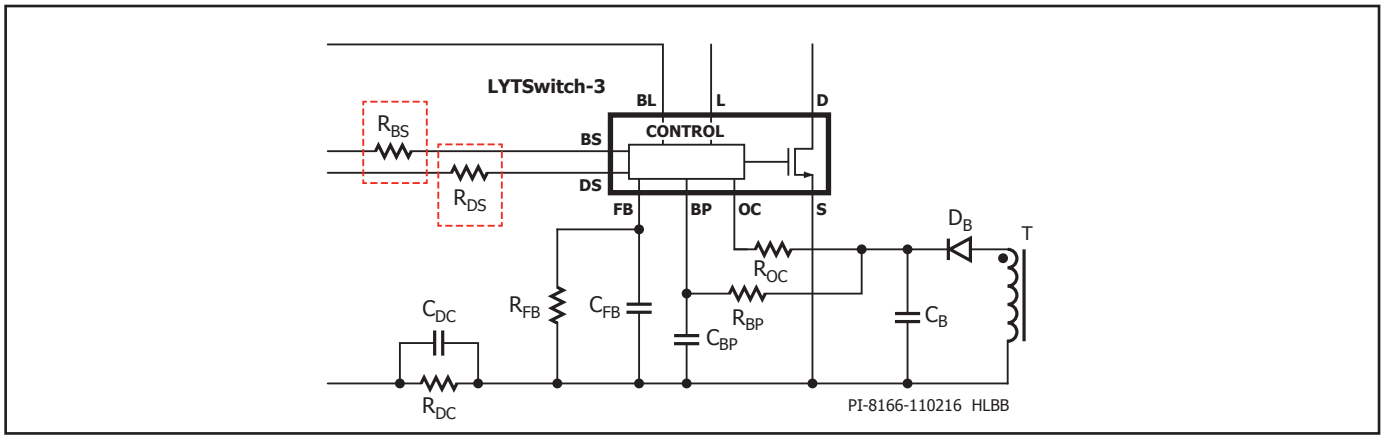

Figure 9. Schematic shows R_{BS} Dim Curve Programming Resistor and R_{DS} Topology Selection Resistor.

R_{BS} (Ω)	Dim Curve	Dimming-Start Conduction Angle	Load Shut Down (LDS)	Cut-In Conduction Angle	Remarks
6 k	Max. Dim Curve	115º	No	Dependent on Dimmer	Lowest Bleeder Dissipation
12 k	Min. Dim Curve	125º	No	Dependent on Dimmer	Highest Dim Range
24 k	Min. Dim Curve	125º	Yes	50º	Reduced Dim Range

Table 5. BLEEDER SENSE (BS) Pin Resistor Programming Table.

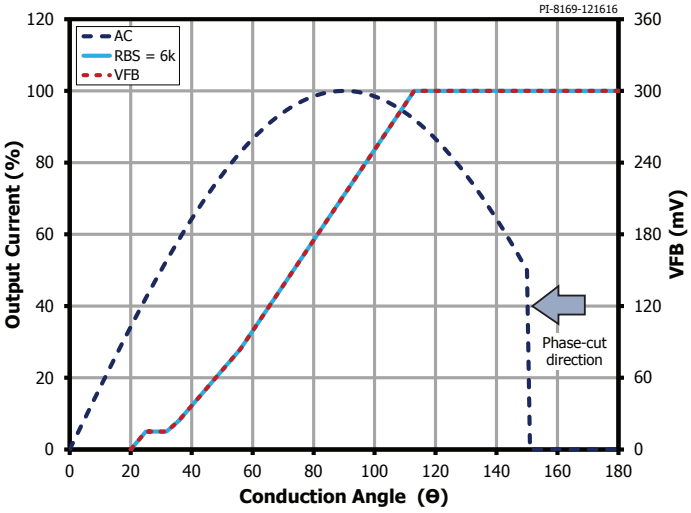

Figure 10. Dimming Curve Showing Feedback Voltage in Relation to Output Current versus Conduction Angle.

Topology Selection Resistor RDS [C36]

Resistor R_{DS} is assigned a default value per PIXIs design spreadsheet. There are two ways of sensing the output current with LYTSwitch-3 ICs to maintain good regulation that is indirect primary sense regulation (IPSR) or direct secondary sensed regulation (DSSR).

These are topology dependent and programmed through R_{DS} resistor value. With topologies where the output ground reference is not common with the input ground reference of the IC controller such as buck or isolated flyback, indirect current sensing (IPSR) is used, this will eliminate the need for a use of a complex optocoupler or a level shifter circuitry to detect the output current. The sensing is done via the R_{DC} sensing resistor where the signal is fed into the DRIVER CURRENT SENSE (DS) pin of the IC through the R_{DS} resistor. The signal is processed internally and the interpolated value is outputted to the FEEDBACK pin which is filtered by C_{FB} and R_{FB} (see Figure 11). The latter is used if the ground references are common between the input and output circuitry. With direct sensing (DSSR), the R_{DS} resistor is just simply connected to the SOURCE (S) pin and the FEEDBACK pin is used to sense directly the output current via R_{FB2} sense resistor connected in series with the load and a small low pass filter (R_{FB} and C_{FB}) is needed for the feedback signal (Figure 12).

R_{DS} (Ω)	Current Sensing	Topology
6 k	Indirect or Primary Sense Regulation (IPSR)	Buck, Buck-Boost, Isolated Flyback
12 k	Direct or Secondary Sense Regulation (DSSR)	Non-Isolated Flyback, Boost

Table 6. RDS Resistor Selection for Topology Current Sensing.

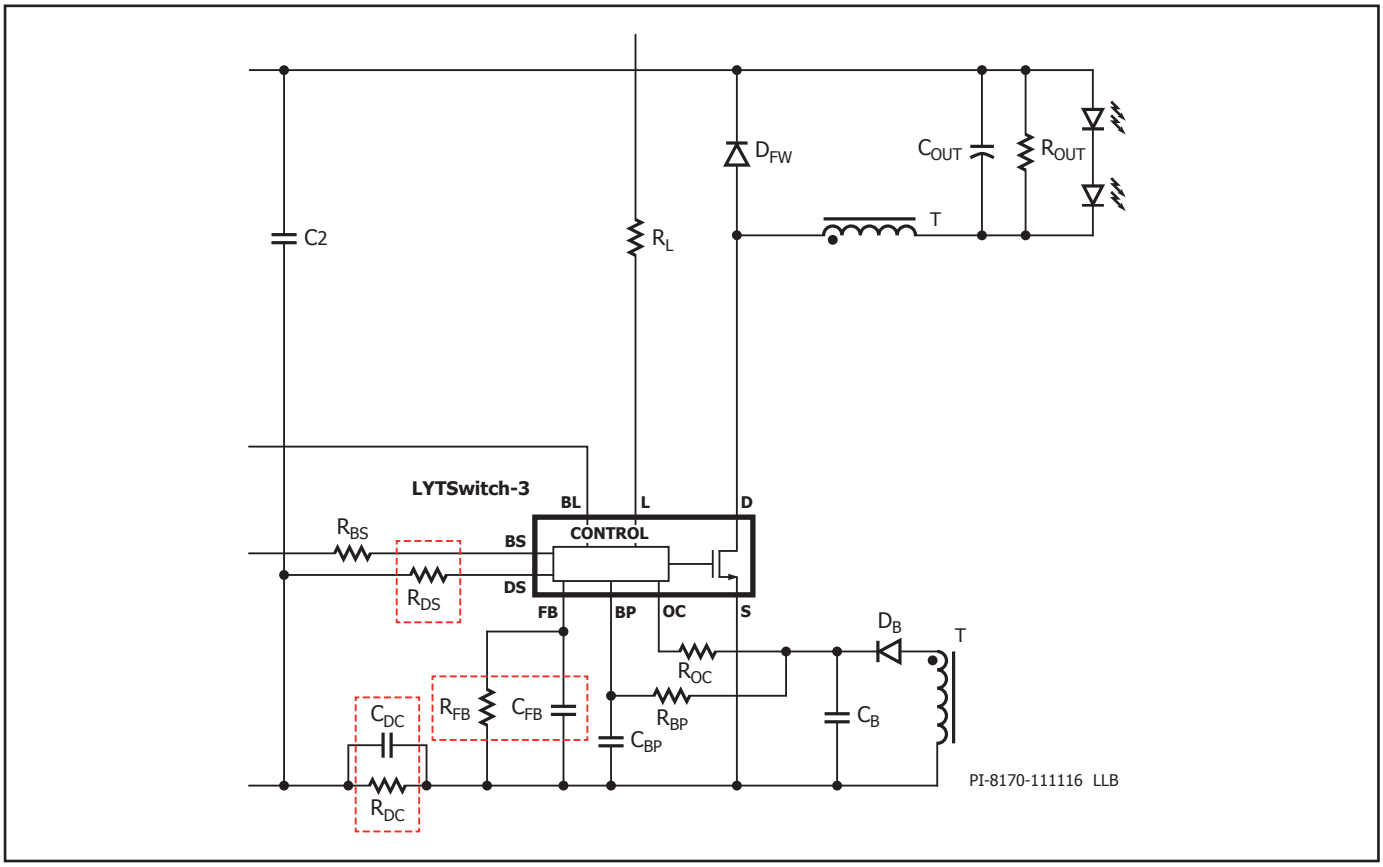

Figure 11. Schematic Shows R_{DS}, R_{DC}, R_{FB} and C_{FB} used for Indirect Sensing of Output Current with Buck Topology.

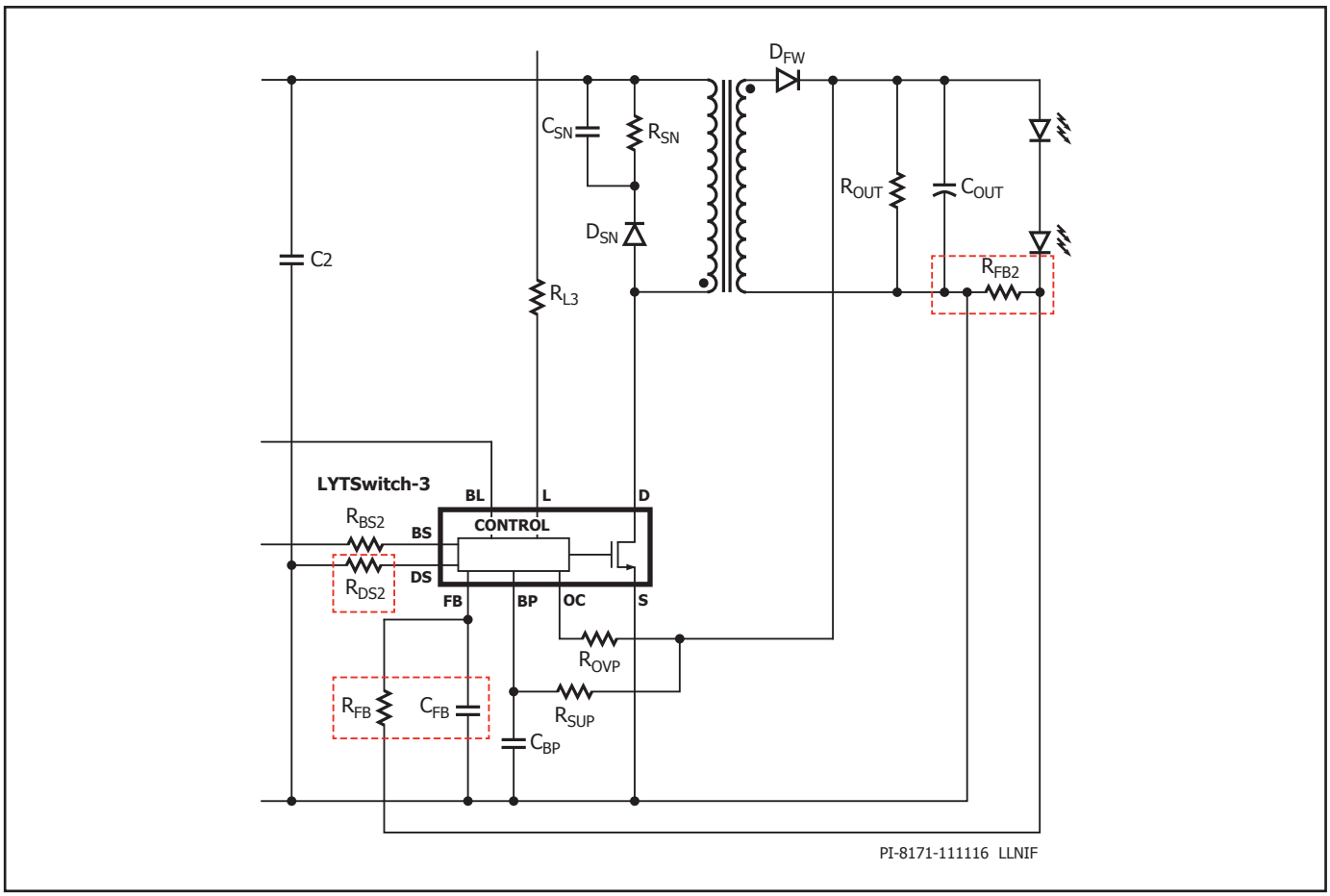

Figure 12. Schematic shows R_{DS}, R_{FB2}, R_{FB} and C_{FB} used for Direct Sensing of Output Current with Non-Isolated Flyback.

Step 4 – Enter Inductor Core and Construction Variables CORE TYPE, AE, LE, AL, VE, AW, BW

Core type selection as a default is set in Auto. The spreadsheet will automatically choose the smallest, but commonly used core suitable for the output power specified. Should the designer prefers a different type of core to use, a list of common cores can be selected from the drop down menu in cell Core Type [C41] of the PIXls spreadsheet or enter manually the parameters for the desired core to use.

Override cells can be used to enter the core and bobbin parameters onto cells AE [C42], LE [C43], AL [C44], VE [C45], AW [C46] and BW [C47]. This is useful if a preferred core is not on the list, or the specified core or bobbin information differs from that referenced by the spreadsheet.

40	ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES				
41	CORE TYPE	EE10	EE10		Core type.
42	AE		12.10	mm^2	Core effective cross sectional area.
43	LE		26.10	mm	Core effective path length.
44	AL		850	nH/T^2	Ungapped core effective inductance.
45	VE		300	mm^3	Core volume.
46	AW		12.21	mm^2	Window area of the bobbin.
47	BW		6.60	mm	Bobbin physical winding width.

Figure 13. Inductor Core and Construction Variables Input of the Design Spreadsheet.

Step 5 – Enter Transformer Design Parameters

51	TRANSFORMER DESIGN PARAMETERS				
51	Inductance parameters				
52	INDUCTANCE	420	420	u-Henrys	Typical value of inductance.
54	INDUCTOR_TOL	5	5	%	Tolerance of inductance.
55	INDUCTANCE_MIN		399	u-Henrys	Minimum value of inductance.
56	INDUCTANCE_MAX		441	u-Henrys	Maximum value of inductance.
57	N	124	124	Turns	Number of inductor turns.
58	ALG		27.32	nH/T^2	Gapped core effective inductance.
59	BM		3506	Gauss	The steady-state operating flux density is higher than 3300 Gauss. Increase the number of inductor winding turns to avoid core saturation.
60	BP		4168	Gauss	Peak flux density.
61	BAC		1753	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak).
62	LG		0.5	mm	Core gap length.
63	LAYERS_DESIRED	5	5	Dimensionless	Desired number of inductor's winding layers.
64	LAYERS_ACTUAL		5.11	Dimensionless	Actual number of inductor's winding layers.
65	AWG	31	31	AWG	Inductor's wire gauge.
66	OD_INDUCTOR_INSULATED		0.272	mm	Outer diameter of the inductor winding wire with insulation.
67	OD_INDUCTOR_BARE		0.227	mm	Outer diameter of the inductor winding wire without insulation.
68	IRMS_INDUCTOR		0.309	Amperes	Maximum RMS current flowing through the inductor's winding.
69	CMA_INDUCTOR		258	Cmils/A	Inductor winding CMA.
70	J_INDUCTOR		7.65	A/mm^2	Inductor Winding Current density.
71	PRIMARY WINDING FILL FACTOR		75%	Dimensionless	Percentage of bobbin window filled up by the inductor winding.

Figure 14. Transformer Design Parameters Section: Inductance Parameters and Bias Winding Parameters of the Design Spreadsheet.

Inductance [E53]
This is the target nominal primary inductance for the main inductor. If left blank, the spreadsheet will calculate the inductance based on the VAC_MIN [E53] to guarantee discontinuous conduction mode over the entire dimming operation. User has the flexibility to override the calculation on cell [C53] and optimized the inductance according to desired operation.

Inductor Tolerance [E54], Inductance_Min [E55] and Inductance_Max [E56]
Expected inductance production tolerance can be assigned in cell [B54]. This tolerance is used in the calculation of the worst case condition of electrical parameters for primary current and operating duty cycle.

Inductor Turns, N [E57]
This is the number of turns for the main primary winding. The spreadsheet will automatically optimize the number of turns based on estimated maximum flux density, BM [E59] and worst case AC flux density BAC [E61]. User can assign number of turns on cell [C57] for any necessary adjustment to optimize design.

Gapped Core Effective Inductance, ALG [E58]
ALG (nH/T2) is used in the production of core to set the inductance of the transformer. It is used by the transformer vendor to specify the core center leg air gap. This is the value of inductance obtained for the squared number of turns around the core.

Maximum Operating Flux Density, BM [E59]
To avoid core saturation during normal operation at maximum operating temperature, a maximum value of 3300 gauss is recommended.

Peak Flux Density, BP [E60]
A maximum 4200 gauss is recommended to avoid core saturation. Peak flux density usually occurs during start-up and/or output short-circuits conditions. The peak flux density is estimated at the maximum device current limit. It is important to verify that core saturation does not occur at maximum ambient temperature under start-up with maximum load.

AC Flux Density, BAC [E61]
This is the flux density used in estimating the core loss for a given core material and volume in steady state condition. BAC = 0.5 x BM

Core Gap Length, LG [E62]
Gap used in the transformer production to set the correct inductance based on core material permeability (AL).

Layers_Desired [D63] and Layers_Actual [D64]
Number of winding layers used to estimate the size of magnetic wire to fit in the transformer bobbin. Cell [C63] is open which can be used to optimize number layers to get desired wire parameters such as AWG, CMA and current density, these are automatically calculated when the cell input is placed.

Transformer Wire Details, OD_Diameter_Insulated [E66]
Outside wire diameter with insulation is calculated with the maximum diameter that allows the wire to fit given number of primary turns (N), bobbin width (BW) and assigned number of winding layers (L).

Inductor RMS Current, IRMS_Inductor [E68]
The RMS current can be used to estimate winding copper loss of the inductor.

The other useful magnetic parameters given in the spreadsheet are:
OD_Inductor_Bare [E66], diameter of wire without insulation.
CMA_Inductor [E67], inductor winding effective circular Mils area.
Current_Density [E68], inductor winding effective current density.
Primary Winding Fill Factor [E71], percentage of bobbin window filled up by the primary winding to estimate if there is sufficient space.

Override cells [C53], [C54], [C57], [C63] and [C65] can be used to enter desired parameters.

Step – 6 Transformer Bias Winding and Bias Components

Bias supply is necessary to supply current into the BYPASS pin to operate normally even at low conduction angle during dimming and it also provides feedback information into the OUTPUT COMPENSATION pin for regulation. The rectifier diode D_B can be any fast or ultrafast recovery type with a voltage rating above the peak inverse voltage value given in the design spreadsheet (PIVBS [E77]), typically >200 V, and current rating >200 mA. The 1N4936 and UF4004 are good examples to use. See Figure 15.

Bias Diode Voltage Drop, VD_BIAS [E74]
Typical voltage drop of 0.7 V for the bias rectifier diode. Also used in the calculation of the feedback resistor R_{OC}.

Bias Winding Turns, BIAS_TURNS [E75]
This is the number of turns of the bias winding calculated based on bias voltage chosen and output voltage.

$$N_{BIAS} = \frac{V_{BIAS}}{V_{OUT}} \times N_{PRI}$$

Bias Voltage, VBIAS [E76]
Default value is 20 V to ensure voltage supply for the bias to support the IC and the bleeder circuit during dimming operation, especially at start-up in low conduction angle. Excessive ripple is not recommended, at least 10 µF electrolytic filter capacitor (C_B) must be used and if ceramic type capacitor is used, a 22 µF value is recommended to account for huge tolerance for the said type of capacitor. Cell CBIAS [E78] displays the recommended value for capacitor C_{BP} as shown in Figure 15.

For designs which require a wider LED voltage operation, increasing the bias voltage is recommended to maintain tight regulation with lower LED voltage.

Output Rectifier Maximum Peak Inverse Voltage, PIVBS [E77]
This is maximum stress voltage across the bias diode at the maximum input voltage.

Override cells [C74] and [C76] can be used to enter desired parameters for VD_BIAS and VBIAS respectively.

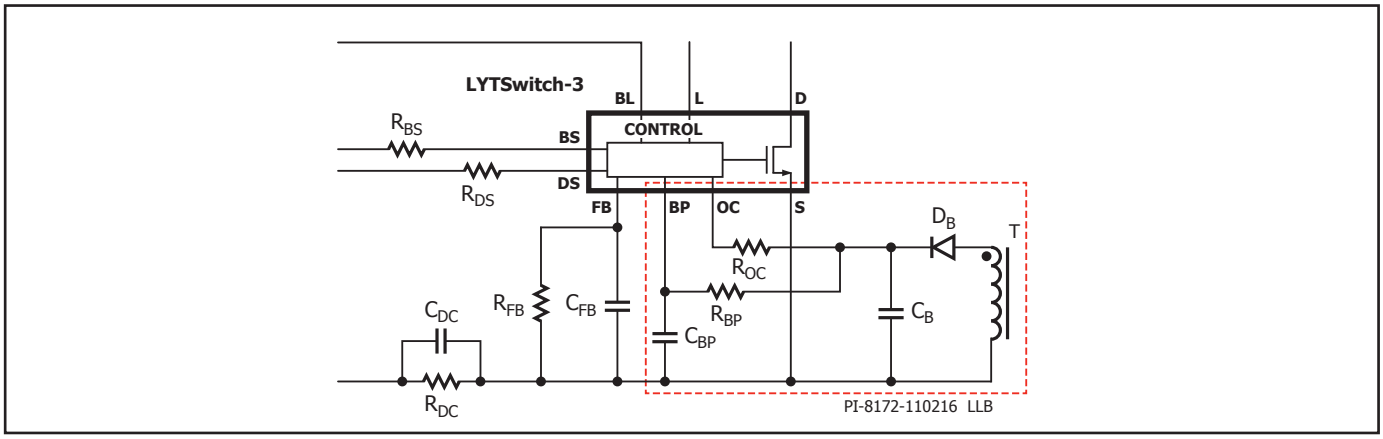

Figure 15. Schematic Shows Bias Supply Circuit of Typical LYTSwitch-3.

73	BIAS WINDING PARAMETERS				
74	VD_BIAS		0.70	Volts DC	Bias winding diode forward drop voltage.
75	BIAS TURNS		36	Turns	Number of bias winding turns.
76	VBIAS		20.0	Volts DC	Bias Voltage. Check performance at minimum VO and VACMAX.
77	PIVBS		128.8	Volts DC	Output Rectifier Maximum Peak Inverse Voltage (calculated at VACMAX)
78	CBIAS		22.0	u-Farads	Bias winding rectification capacitor.
79	RBP		14.70	k-Ohms	Bias supply resistor assuming 1mA current necessary to supply the BP pin.
80	CBP		22	u-Farads	Minimum BP pin capacitance.

Figure 16. Transformer Bias and Parts Variables of the Design Spreadsheet.

Step – 7 Secondary Output Diode Parameters

84	SECONDARY DIODE PARAMETERS				
85	VF_DIODE		0.7	Volts DC	Output diode forward voltage drop.
86	IRMS_DIODE		0.287	Amperes	Diode RMS current at LP_MIN, VACMIN and PO_MAX.
87	IP_DIODE		1.193	Amperes	Diode peak current at LP_MIN ,VACMAX and PO_MAX.
88	PIV_DIODE		506.9	Volts DC	Peak Inverse Voltage at VO_MAX on output diode.

Figure 17. Secondary Diode Parameters of the Design Spreadsheet.

Use ultrafast diode for output rectification and the recommended diode rating should 2 times of the output current, i.e. 2 × I_O < IAVG_DIODE, for higher efficiency.

Output Diode Voltage Drop, VF_DIODE [E85]
Enter the average forward voltage drop for the output diode. Use 0.7 V for a PN diode. Estimated forward power loss to this diode estimated by taking the product of I_O × VF.

Output Diode RMS Current, IRMS_DIODE [E86]
The RMS current through the diode is calculated that can be used to calculate the copper loss of the inductor.

Output Diode Peak Current, IP_DIODE [E87]
Peak current in the output diode is calculated in a worst case condition to guide the user to select the diode current rating and package size.

Peak Inverse Diode Voltage, PIV_DIODE [E88]
Use this parameter in selecting the voltage rating of the output diode. The worst case reverse peak voltage is calculated in open load condition which is the worst-case condition.

Step – 8 Feedback and Protection Parameters with Fine Tuning

This section will guide the user in selecting the external parts to be used in the design for achieving the specified output current. Leaving the section blank PIXls will recommend the initial value to be used. Once a prototype has been built, the output current can be fined tuned to the center by entering an actual measurement of the using the override cells [C93], [C95], [C98], [C99] and [C101].

Line-Sense Resistor, RL [E93]
Line sense resistor is used for line compensation for regulation, phase angle measurement in dimming, line input overvoltage detection. To achieve tight output current regulation and dimming angle measurement resistor with 1% tolerance is recommended and also it should be connected to the positive of the bridge rectifier for better sensing of the line as shown in Figures 1 and 2. It is also recommended to use 2-1206 or 2-1/4W package resistor for high line application and 1-1206 or 1-1/4W for low line application.

$$RL = 1.2 \times VACMAX \times \frac{\sqrt{2}}{ILOV+}$$

Maximum RMS Input Voltage for Line Overvoltage, OVP_LINE [E94]
The spreadsheet will calculate the equivalent RMS input voltage for OVP. The unit will enter to auto restart when the threshold is reached.

Instantaneous peak voltage during OVP is

$$V_{PK(OVP)} = \sqrt{2} \times OVP\_LINE$$

Theoretical Drain Current Sense Resistor, RDC_THEORETICAL [E95]
The ideal resistor value to be used in the drain current sensing is calculated. The voltage drop across the resistor is sensed through DRIVER SENSE pin and the recommended average voltage drop across this sense resistor is 200 mV.

92	FEEDBACK AND PROTECTION PARAMETERS WITH FINE TUNING				
93	RL	4.00	4.00	M-Ohms	Standard (E96 / 1%) L pin resistor.
94	OVP_LINE		339.4	Volts RMS	Line overvoltage based on the actual L pin resistor used.
95	RDC_THEORETICAL		4.73	Ohms	Theoretical DS pin sense resistor.
96	RDC	4.30	4.30	Ohms	Standard (E96 / 1%) DS pin sense resistor.
97	CDC		10.0	u-Farads	Standard capacitor connected in parallel with the DS pin sense resistor.
98	VBIAS_MEASURED	19.7	19.7	Volts DC	Actual bias voltage (across the bias capacitor) measured on the bench.
99	VO_MEASURED	71.3	71.3	Volts DC	Actual load voltage measured on the bench.
100	ROC		178.0	k-Ohms	Standard (E96 / 1%) OC pin resistor.
101	IO_ACTUAL	115.0	115.0	m-Amperes	Actual output current seen on the bench.
102	RFB_THEORETICAL		39.3	k-Ohms	Calculated value of RFB, using standard values for RDS, ROVP, and RL
103	RFB		39.2	k-Ohms	Standard (E96 / 1%) F pin resistor.
104	CFB		150.0	n-Farads	Standard capacitor connected to the F pin.

Figure 18. Feedback and Protection Parameters with Fine Tuning of the Design Spreadsheet.

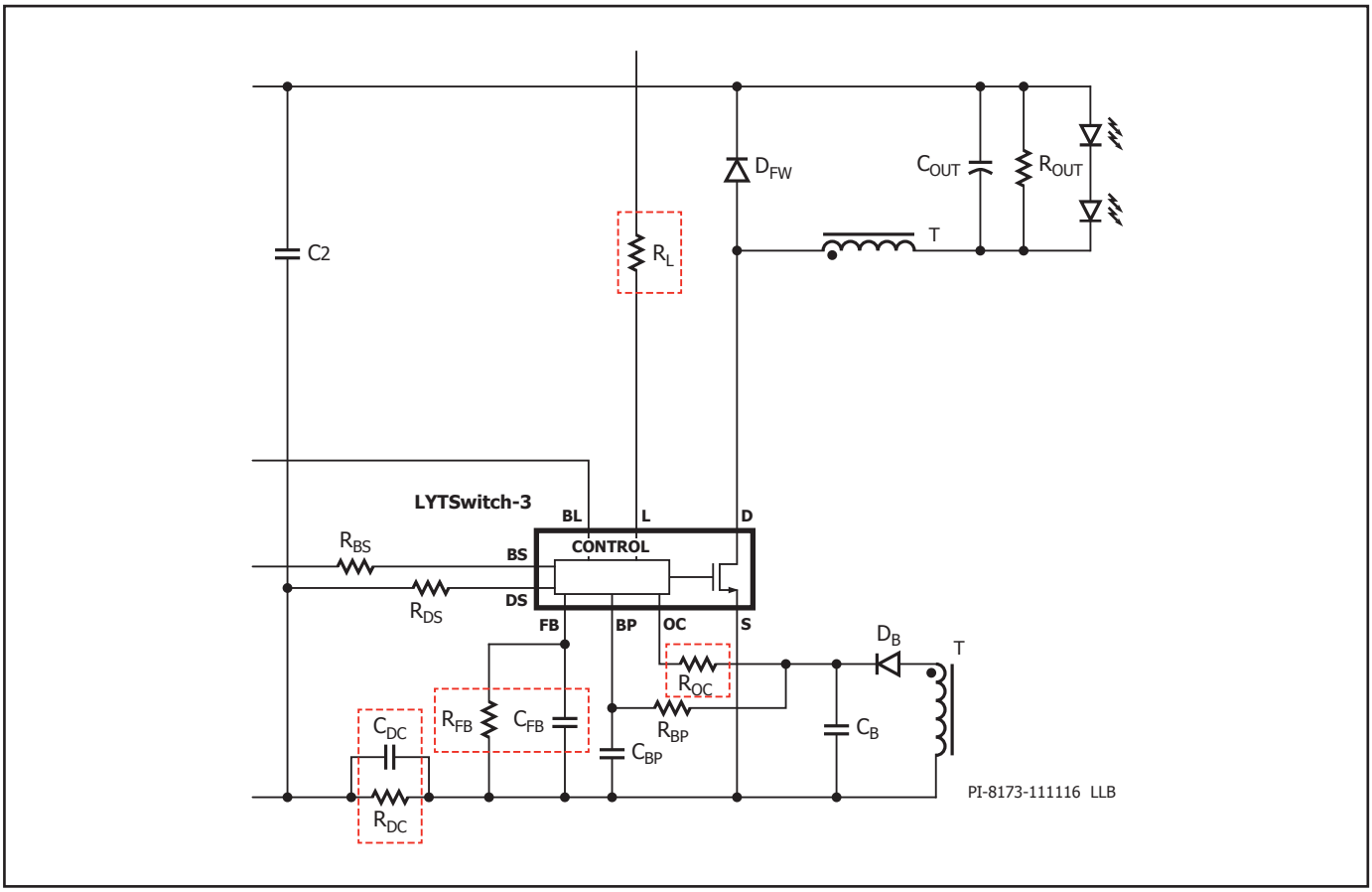

Figure 19. Schematic Shows R_L, C_{DC}, R_{DC}, R_{OC}, R_{FB} and C_{FB} used for Indirect Sensing of Output Current with Buck Topology.

Standard Drain Current Sense Resistor, RDC [E96]
This identifies standard 1% resistor value nearest to the RDC_THEORETICAL to lessen the need of paralleling anther resistor for centering the output, also saves cost and space (Figure 19).

Capacitance Across Drain Current Sense Resistor, CDC [E97]
This is the capacitor (C_{DC}) across the Drain current sense resistor (R_{DC}) that filters the switching Drain current to reduce the IRMS power dissipation across the sense resistor.

Low ESR ceramic type capacitor is recommended to use. Aluminum electrolytic capacitor due to its size, cost, relative high ESR and high capacitance tolerance is not recommended.

Actual Bias Voltage, VBIAS_MEASURED [E98]
Enter the actual bias voltage for fine tuning the output current. The actual may differ significantly from calculated due to leakage inductance of the transformer.

Actual Output Voltage, VO_MEASURED [E99]
Enter the actual output voltage with LED load for fine tuning the output current.

Output Current Compensation Resistor, ROC [E100]
Load variation, output overvoltage protection and output short-circuit is monitored through bias voltage via compensating resistor (R_{OC}).

Spreadsheet will calculate this resistance based on the actual bias voltage (VBIAS_MEASURED). A 1% tolerance resistor is recommended in this location for tight output current tolerance.

Actual Output Current, IO_ACTUAL [E101]
Enter the actual current as measured from the bench for the fine tuning of external components to center the output to a desired level.

Theoretical Feedback Resistor, RFB_THEORETICAL [E102]
Spreadsheet calculates the exact feedback resistor resistance to set the output current based on the actual output current measured.

Feedback Resistor, RFB [E103]
The spreadsheet will determine the nearest single resistance value for use in R_{FB} to avoid paralleling of components to get the desired current. But if the application requires tight output current tolerance then use the resistance calculated by RFB_THEORETICAL.

Feedback Filter Capacitance, CFB [E104]
Filter capacitance for the feedback current to average the signal to a desired voltage mean level of the FEEDBACK pin. The desired time constant can be in the range of 3 ms to 8 ms to maintain stable operation with tight current regulation.

Step - 9 Dimming Parameters

108	DIMMING PARAMETERS				
109	RDAMPER	197	197	Ohms	Damper resistor required to limit inrush current during dimming.
110	P_RDAMPER		0.568	Watts	Power dissipation of the damper resitor (RDAMPER).
111	IBLEED	31	31	m-Amperes	Target holding current for triac compatibility.
112	RBLEED	5100	5100	Ohms	Recommended maximum bleeder resistance.
113	RBLEED CASE TEMPERATURE	150	150	Degrees Celcius	Bleeder resistor case temperature.
114	PLOSS_RBLEED		4.195	Watts	Minimum power rating of the bleeder resitor at 150degC (RBLEED).
115	PBJT		0.207	Watts	Power dissiupation of the bleeder BJT.
116	RDEGENERATION		31.25	Ohms	Degeneration resistor required to limit the gain of the transistor.
117	RBC		3.9	Ohms	Programming resistor for the holding current.
118	P_RBC		0.011	Watts	Power dissipation of the programming resistor for the holding current (RBC).

Figure 20. PIXls Dimming Parameters of the Design Spreadsheet.

The schematics below in Figures 21 and 22, showing the LYTSwitch-3 active bleeder circuit for high line and low line applications respectively are recommended for high compatibility with most dimmers.

Dimming external components are calculated in this section to guide the designer the optimum holding current and component size.

Damper Resistance, RDAMPER [E109]
Damper resistor (R_{DP}) is necessary to minimize inrush current and damps the spurious ringing of the input current in a leading edge dimmer. This ringing should be minimized to prevent the input current from ringing below the holding current of a TRIAC, which can make the TRIAC to turn-off prematurely and causes flickering of the light output.

Damper Resistor Power Loss, P_RDAMPER [E110]
Damper resistor loss is estimated in a worst case condition during dimming at 90º for leading edge dimmer. It is recommended to measure the actual temperature of the resistor and verify against the manufacturer specification power de-rating guideline.

Bleeder Current, IBLEED [E111]
Setting for bleeder current (I_{BLEED}) for optimum dimming compatibility. The higher the bleeder current the better the compatibility, but higher power dissipation. It is up to the designer to optimize the design depending on the target available dimmer. Typically for 120 V rated dimmers the bleeder current (I_{BLEED}) should be set at 50 mA, while 240 V rated dimmers should be at 30 mA.

Bleeder Resistor, RBLEED [E112]
The spreadsheet will calculate the maximum resistance of the bleeder resistors (R_{B1}, R_{B2} or R_B) for optimum dimming compatibility, then selects lower resistance based on the calculated value. This value is optimized to minimize the power dissipation in the bleeder Darlington transistor (Q1 and Q2). It is recommended to measure the actual temperature of the resistor and verify against the manufacturer specification for power de-rating guideline.

Bleeder Case Temperature, RBLEED CASE TEMPERATURE [E113]
Enter the expected temperature of the bleeder resistor once operated in a given lighting enclosure. This value is used in recommending the right resistor rating at 25 ºC. It is recommended to measure the actual temperature of the resistor and verify against the manufacturer specification power de-rating guideline.

Power Rating of Bleeder Resistor, PLOSS_RBLEED [E114]
Since power rating is derated at higher temperature, the spreadsheet will calculate the equivalent rating at 25 ºC. Use this as minimum power rating value to guarantee safe operation of the unit at elevated temperature.

Power Loss in Bleeder Transistor, PBJT [E115]
The power dissipation of Darlington transistor (Q1 and Q2) is estimated by the spreadsheet. Select the transistor size base from the data sheet to determine the required package at elevated temperature.

Degeneration Resistor, RDEGENERATION [E116]
Degeneration resistor (R_D) is calculated to limit the gain of the transistor to keep the bleeder circuit stable even at high operating temperature.

Bleeder Current Sense Resistor, RBC [E117]
Compensating current or bleeder current (I_{BLEED}) through the bleeder is programmed through bleeder current sense resistor (R_{BC}). The holding current can be set using the equation;

$$R_{BC} = 120\ mV / I_{BLEED}$$

Power Loss in Bleeder Current Sense Resistor, P_RBC [E118]
The spreadsheet will calculate the estimated power loss on the bleeder resistor in non-dimming operation.

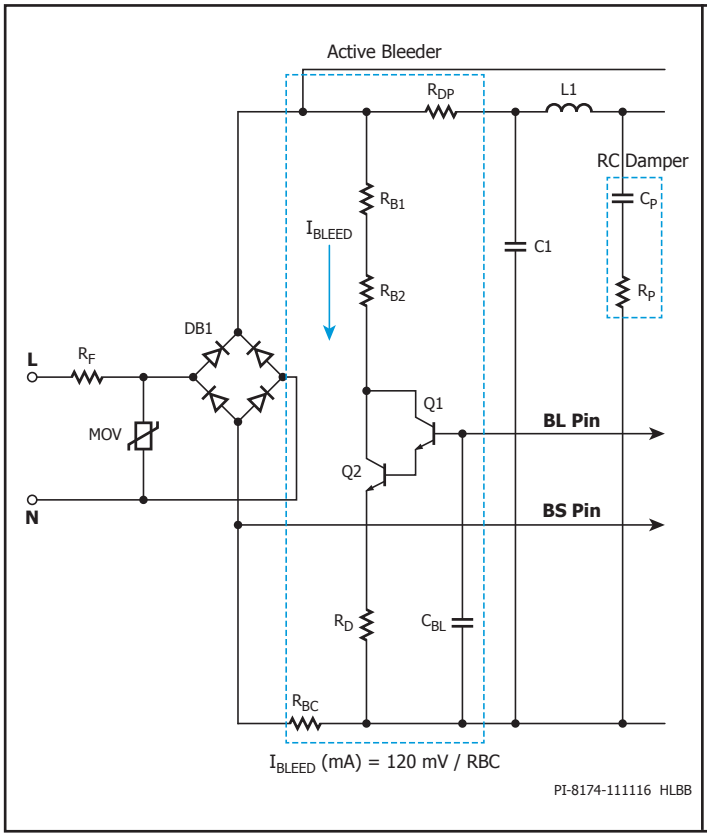

Figure 21. Recommended High-Line Active Bleeder Circuit with RC Damper C_P and R_P.

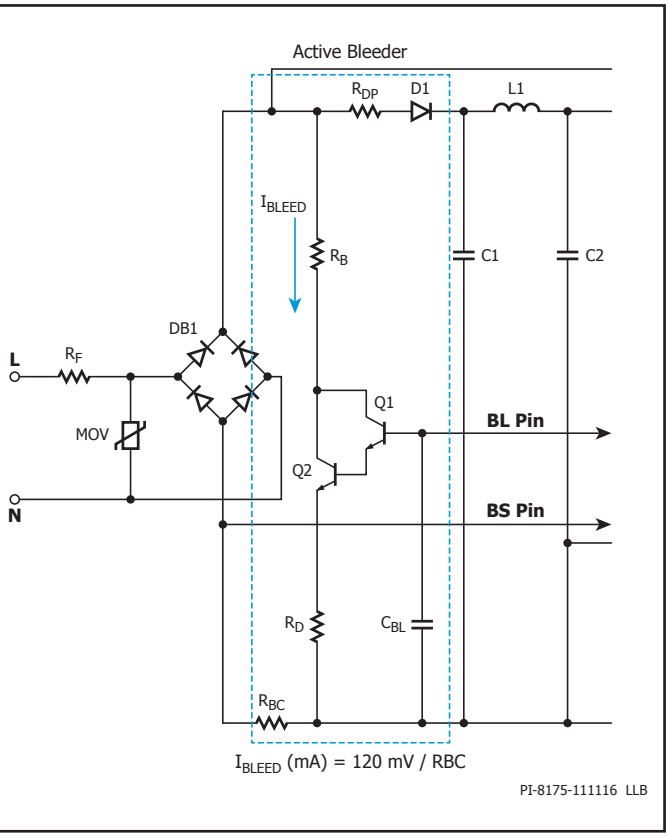

Figure 22. Recommended Low-Line Active Bleeder Circuit with Blocking Diode D1.

Phase-Cut Dimming

The biggest challenge in designing dimmable LED bulb is high compatibility with broad range of dimmer types of different power ratings. Since different types of dimmers have different minimum loading requirement, the dimmable LED bulb may manifest varying incompatibility behavior depending on the dimming conditions from light flickering or shimmering, ghosting, or huge pop-on to low dimming ratio.

There are two main types of phase-cut dimmers namely forward phase or leading edge (Figure 23) and reverse phase or trailing edge (Figure 24). Each type has its own characteristic and nuances that make it challenging for LED bulb drivers to achieve high compatibility. Many low-line dimmers especially high-power rated (i.e. >600 W) require high holding current up to 35 mA, this would make a LED bulb prone to flickering if not met. While high-line dimmers may require less than 20 mA of holding current, many have high leakage voltage (especially trailing-edge dimmers) enough to power a LED bulb momentarily which may result to fluttering, ghosting or flashing of light occasionally even when the dimmer is off. The challenge is the user may never know what type of dimmer and/or LED bulb to buy that will be compatible with each other. A LED driver using LYTSwitch-3 ICs can address this dilemma.

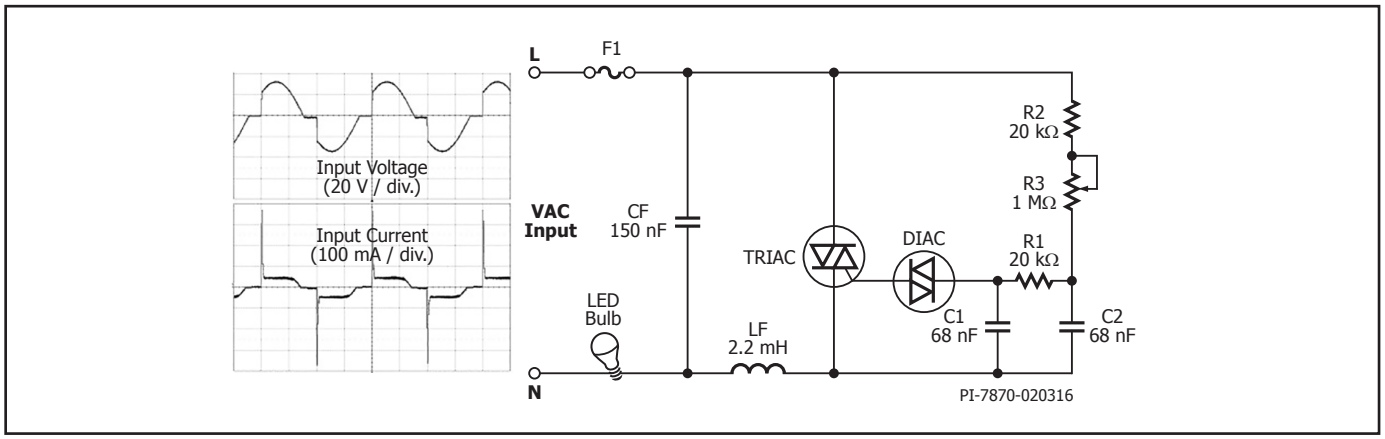

Figure 23. Typical Voltage and Current Waveform and Schematic of a Forward Phase-Cut Leading Edge Dimmer (TRIAC-Switched).

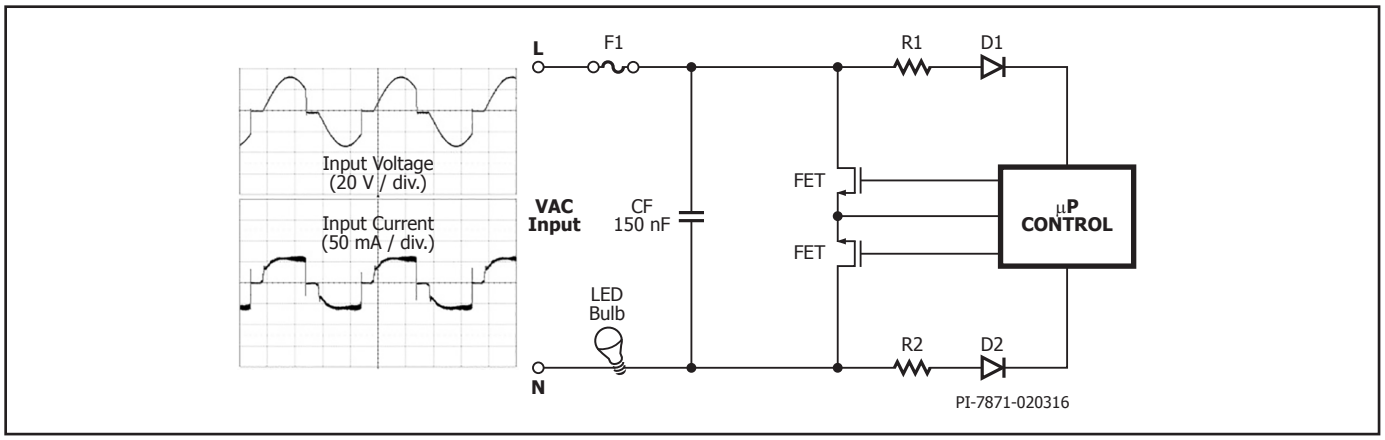

Figure 24. Typical Voltage and Current Waveforms and Schematic of a Reverse Phase-Cut Trailing Edge Dimmer (MOSFET-Switched).

Active Bleeder Circuit with LYTSwitch-3

To overcome the challenges of designing dimmable LED driver with high compatibility on any type of dimmer, all LYTSwitch-3 ICs have a built-in TRIAC detector that discriminates between leading-edge and trailing-edge type dimmers which is detected through the LINE-SENSE pin. This capability together with load monitoring circuitry via BLEEDER CURRENT SENSE pin regulates bleeder current every AC half-cycle from full to low conduction angle. In a non-dimming application where the LED driver is connected to the line directly, that is without a dimmer, the controller will detect a no TRIAC operation and disables the bleeder circuit via pulling BLEEDER CONTROL pin to ground. This will prevent additional power dissipation from the bleeder, consequently increasing system efficiency.

In Figure 25, a LYTSwitch-3 device is operating with a leading edge dimmer, the output of BLEEDER CONTROL pin drives Q1 with Q2 in emitter follower connection, a high gain active switch that pulls current from the input bus via R_B to provide latching current and maintain holding current necessary to keep the TRIAC from turning off during the entire input AC cycle. Figure 26, during the initial turn-on of the TRIAC, the BLEEDER CONTROL pin will drive bleeder transistors on for ~250 µs and pulls the necessary latching current from the bus via R_B, after which the bleeder current will be maintained if the total input current falls below the bleeder current threshold to which it was set to maintain the holding current of the TRIAC. The holding current is maintained even in low conduction angle as shown in Figure 27. The analog signal from the BLEEDER CONTROL pin of U1 drives Q1 and Q2 linearly when the input current falls below the holding current thus maintaining the current set by the resistor R_{BC}. The holding current can be set using the equation $R_{BC} = 120\ mV/I_{BLEED}$. Bleeder resistor R_B value is 5.1 kΩ with at least 2 W power rating for high-line application at 20 mA holding current and 1.2 kΩ, 2 W for low-line at 35 mA holding current. The designer is advised to take worst case operating temperature and follow the manufacturer's power de-rating guideline to size the bleeder resistor. The condition at which the bleeder resistor tends to dissipate the most power is around 90° conduction angle.

Figure 25, Capacitor C_{BL} and degenerative resistor R_D serve as stabilizing network for the bleeder transistors for stable dimming performance. R_D typical range of value is 20 - 47 Ω while C_{BL} is between 4.7 nf to 22 nf.

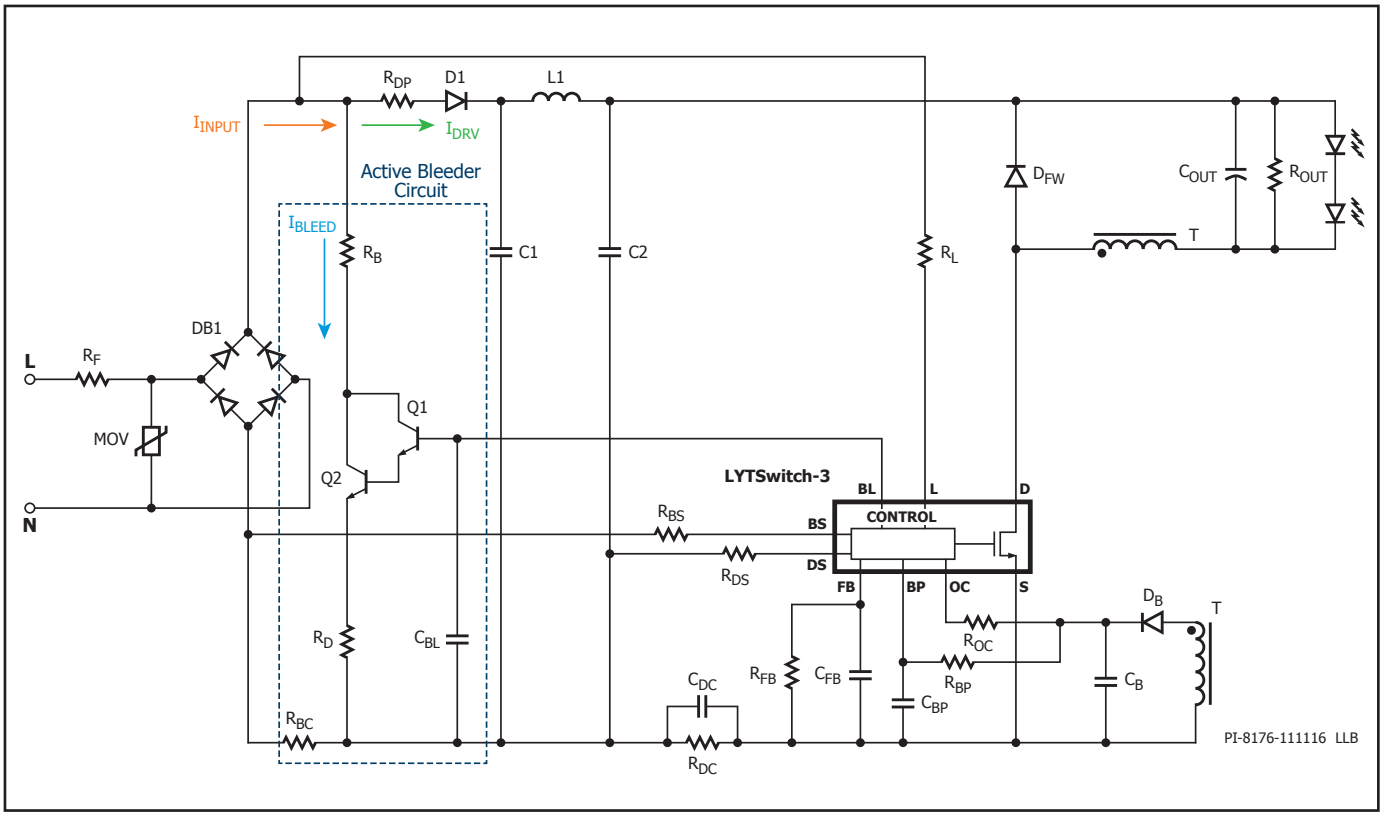

Figure 25. LYTSwitch -3 with Active Bleeder in Buck Configuration Showing Flow of Current

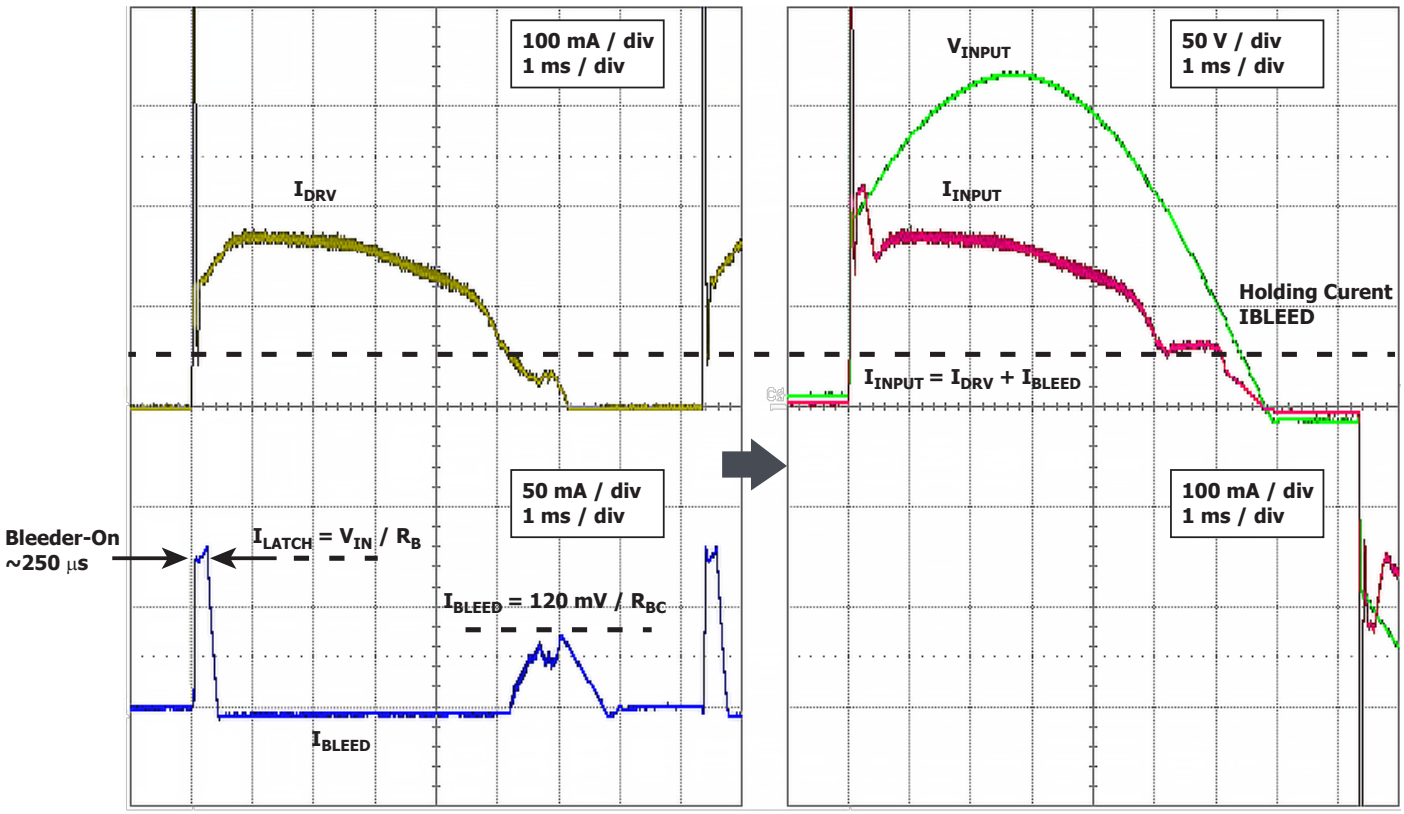

Figure 26. At 150º Forward Phase-Cut Angle Waveforms of Active Bleeder Current, Converter Current and Total Input Current.

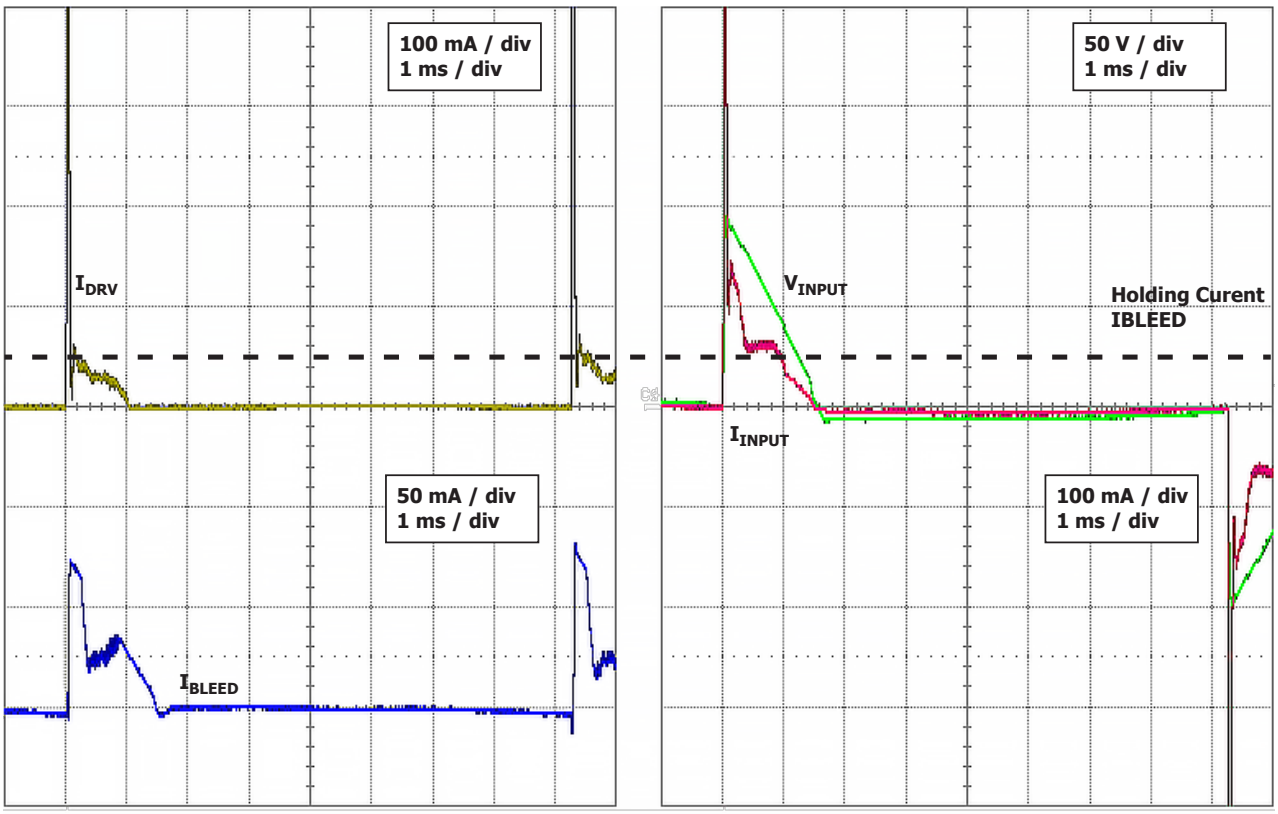

Figure 27. At 45º Forward Phase-Cut Angle Waveforms of Active Bleeder Current, Converter Current and Total Input Current.

Passive Damper

Passive RC damper is recommended for high-line application for optimum dimming compatibility. The dv/dt at high-line is much higher than low-line, which make the internal LC filter of a dimmer (Figure 28) and EMI filter of a driver more susceptible to severe ringing when the TRIAC of the dimmer turns on.

In Figure 21, capacitor C_P and resistor R_P together with fusible resistor R_F and damper R_{DP} act as dampening network to reduce the ringing of current and prevent it from falling below the TRIAC holding The value of C_P is in the range of 47 nf to 220 nf, while R_P can be between 470 Ω to 1 kΩ with 1 W rating typical for low-line input or 2 W for high-line input.

PIXls design spreadsheet for other topologies is available in Power Integrations public website (https://piexpertonline.power.com/site/login)

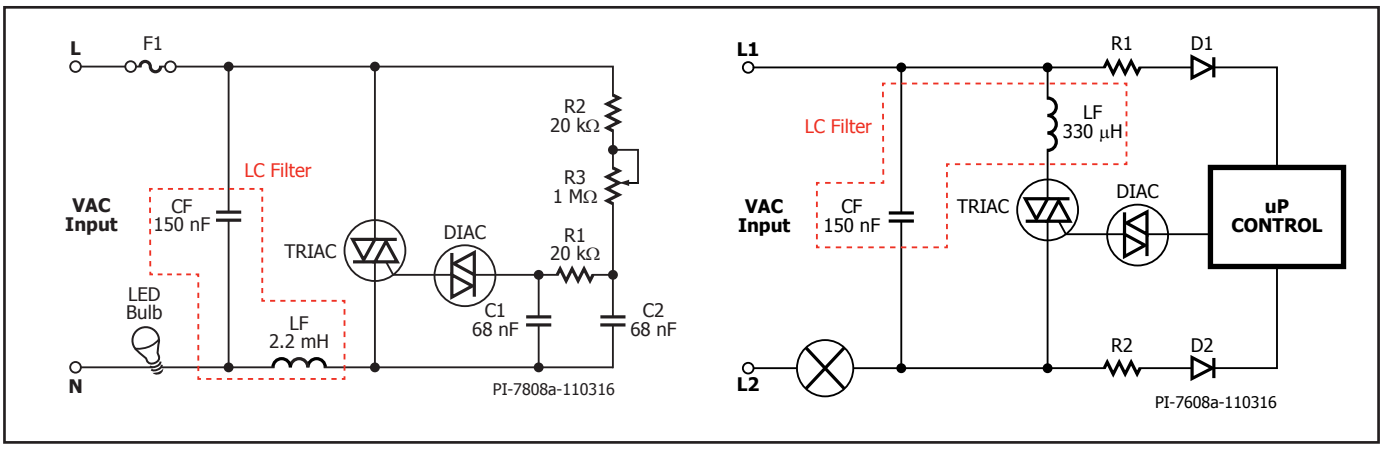

Figure 28. Typical TRIAC Dimmer Showing the LC Filter that Resonates with EMI Filter of Driver During TRIAC Turn-On.

Appendix A

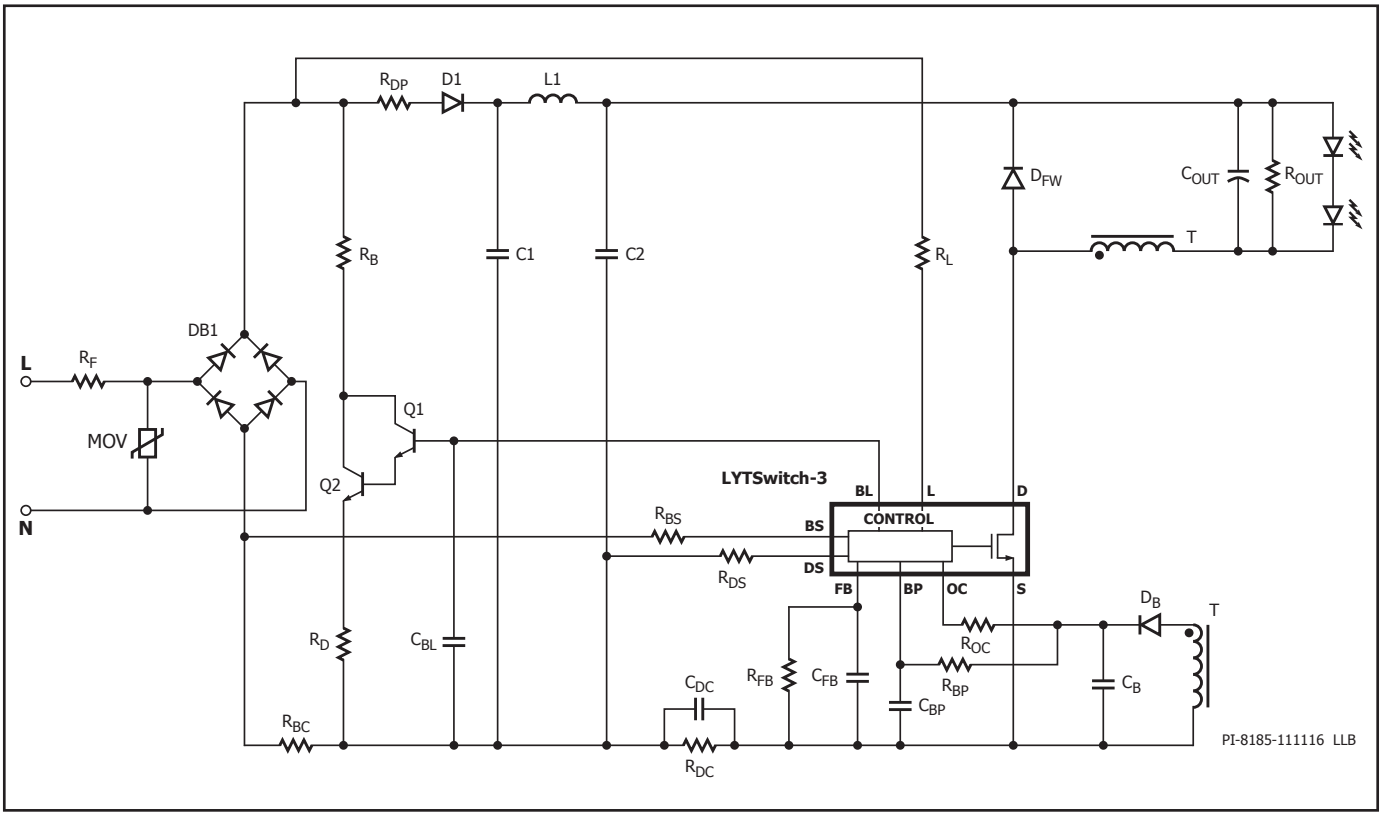

Figure 29. Typical LYTSwitch-3 Low-Line Buck Configuration.

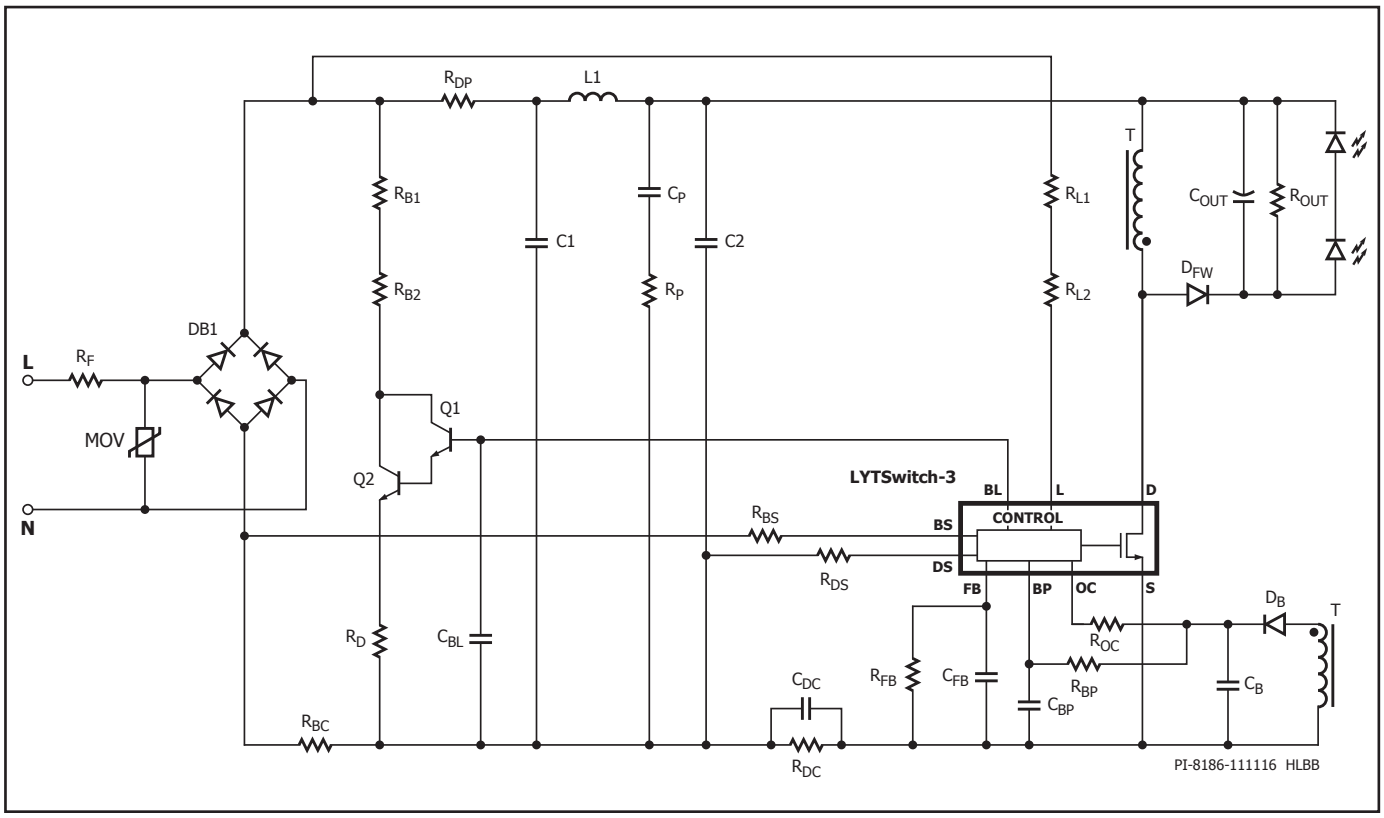

Figure 30. Typical LYTSwitch-3 High-Line Buck-Boost with RC Bleeder Configuration.

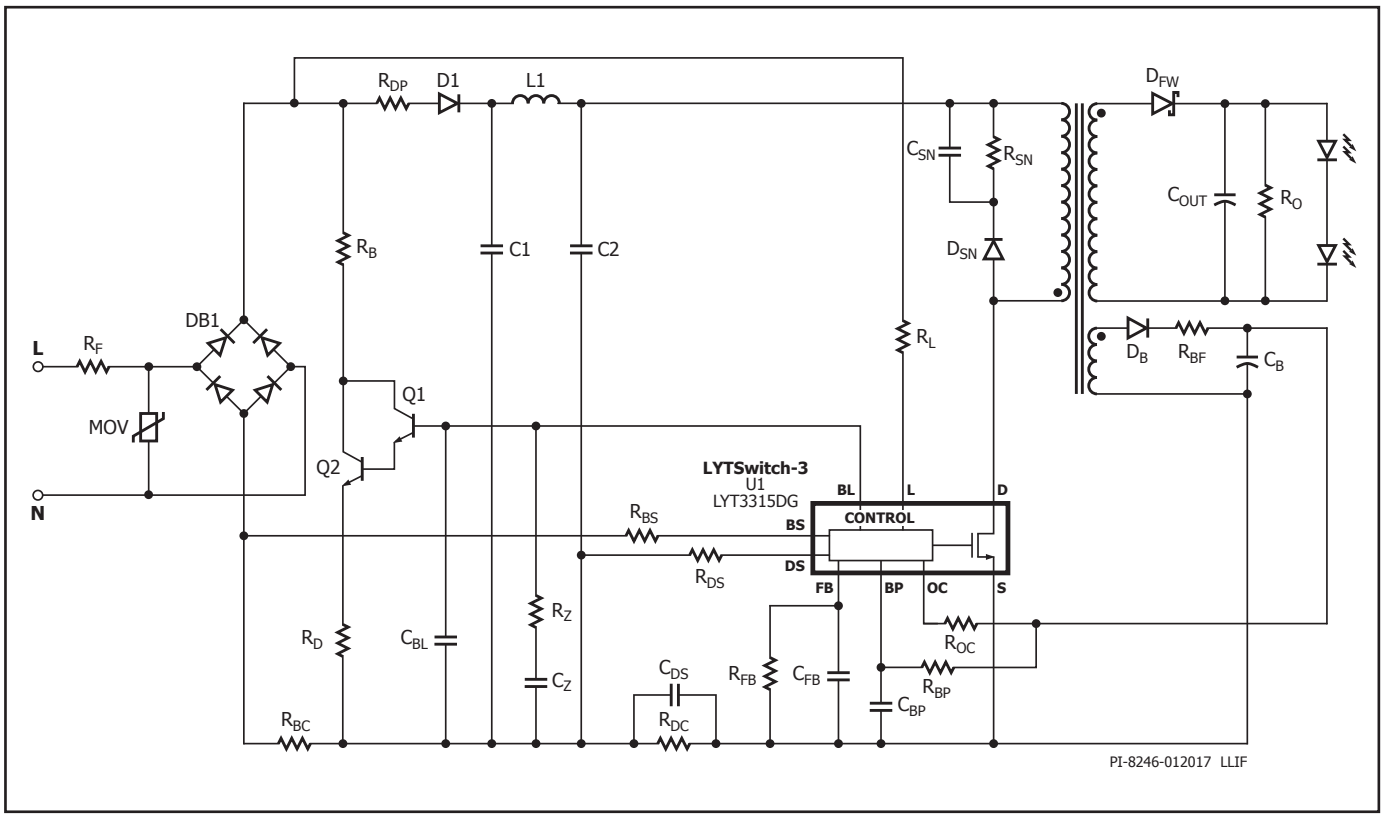

Figure 31. Typical LYTSwitch-3 Low-Line Isolated Flyback Configuration.

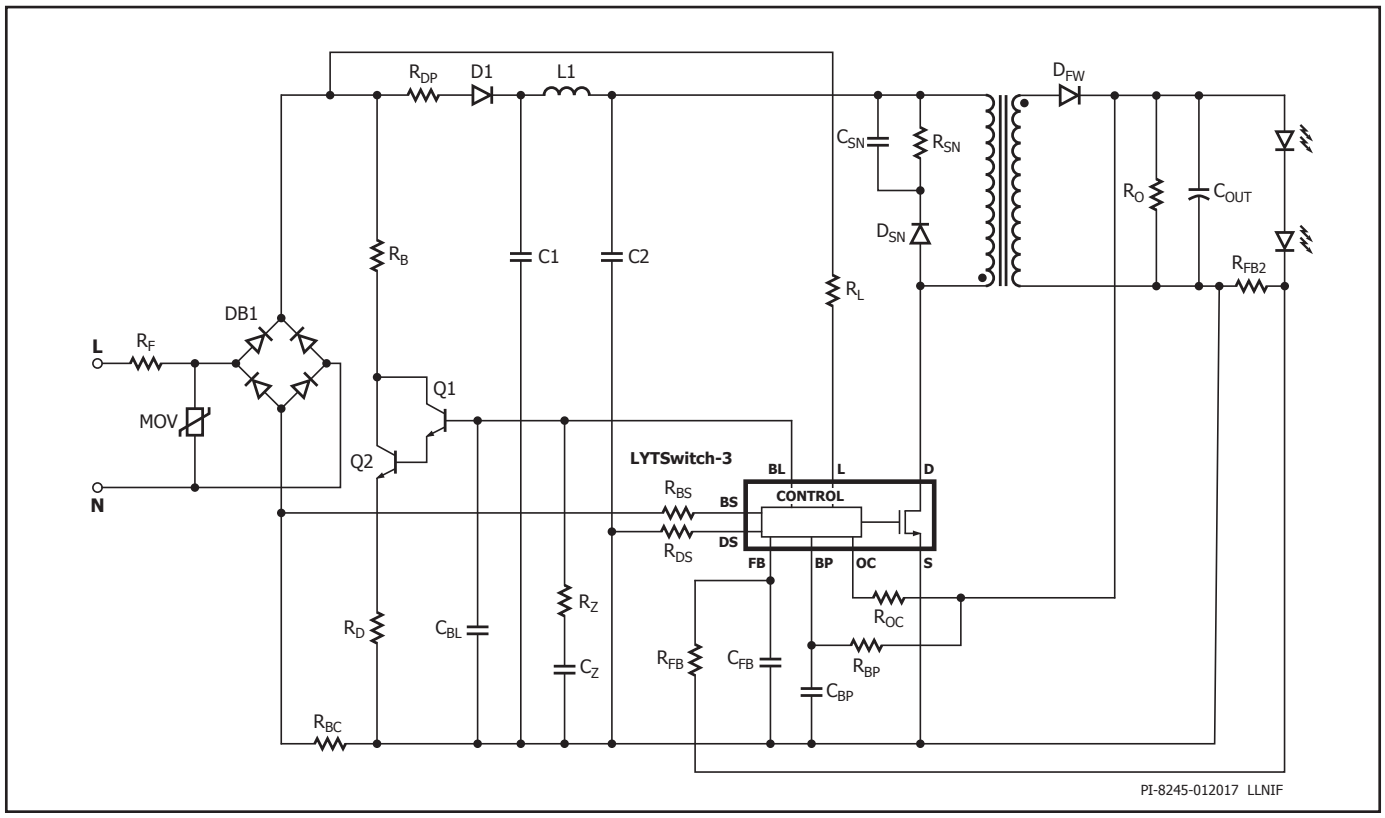

Figure 32. Typical LYTSwitch-3 Low-Line Non-Isolated Flyback with Direct Sense Regulation Configuration.

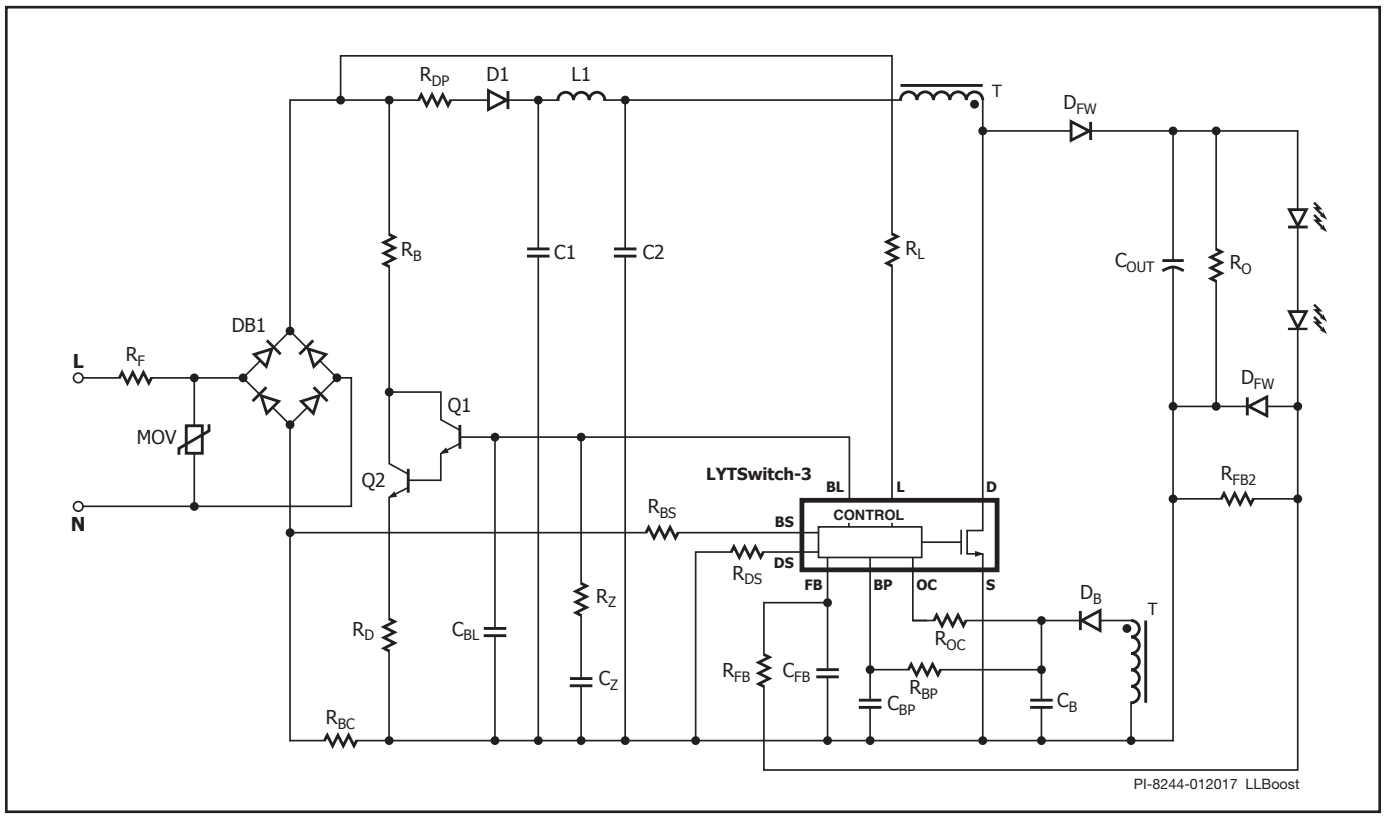

Figure 33. Typical LYTSwitch-3 Low-Line Boost with Direct Sense Regulation Configuration.

Revision	Notes	Date
A	Initial Release.	01/17

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