Application Note AN-58
LinkSwitch-HP Family

Design Guide

Introduction

The LinkSwitch™-HP family is a highly integrated monolithic switcher IC designed for off-line power supplies. Output regulation is achieved using primary-side sense regulation (PSR) that gives accurate output regulation for designs up to 90 W / 117 W. PSR eliminates secondary-side components including the optocoupler while still achieving output regulation of ±5% or better at the supply output. Other key technical performance parameters are listed in Table 1.

The controller is simple to use, utilizing a combination of variable frequency and current mode control. Loop compensation is provided by a single RC network. The input line and output overvoltage and loss of regulation sensing is all accomplished through the feedback resistor sense network which minimizes component count and eliminates the need for lossy direct high-voltage sensing. There is also the function of programming the maximum peak drain current with a single external resistor to give flexibility in both device and transformer core size selection to optimize size, cost and efficiency.

Two maximum MCM (multi-cycle-mode) off-time (related tominimum switching frequency) and MOSFET voltage rating options are available as shown in Table 2.

The maximum switching cycle off period $T_{MCM(OFF)}$ determines the minimum switching frequency and both the no-load input power performance and no-load to a high load output transient response. For lowest no-load input power 4 ms should be selected or for faster transient response 0.5 ms should be selected. The 650 V MOSFET BV_{DSS} rating offers a lower cost option in applications with less stringent de-rating requirements.

Part Number	BV_{DSS}	$T_{MCM(OFF)}$	P_{NC}
LNK677x	725 V	4 ms	<30 mW
LNK676x	650 V	4 ms	<30 mW
LNK666x	650 V	0.5 ms	<100 mW

x = Device Size (3, 4, 5, 6, 7)

Table 2. LinkSwitch-HP Device Family Options.

Power range	≤90 W (85 VAC – 265 VAC)
	≤117 W (195 VAC – 265 VAC)
Low no-load input power	<30 mW (LNK67xx devices)
	<100 mW (LNK66xx devices)
High available output power in standby	>0.75 W output for <1 W input
	>50 mW output for <0.1 W input
High full load efficiency	>86.5% (115 VAC, 12 V, 30 W)
Protection and reliability	
Output short-circuit	Auto-restart or latching
Output overload/over-current	Auto-restart or latching
Open-loop*	Auto-restart
Output overvoltage	Auto-restart or latching
Line brown-in/out (line UV)	Auto-restart
Line overvoltage	Shut down
Accurate thermal shutdown	Hysteretic or latching
Device open-circuit / adjacent pin short	Yes

*Open-loop: Open connection between the feedback winding and feedback divider network R_{FB2}, or the FEEDBACK pin to the feedback divider network R_{FB2}.

Table 1. LinkSwitch-HP Family Key Technical Performance Parameters.

Basic Circuit Configuration

The circuit shown in Figure 1 shows the basic configuration of a flyback power supply designed using LinkSwitch-HP. Because of the high level integration of LinkSwitch-HP, many power supply design challenges are resolved in the IC. Far fewer issues are left to be addressed externally, resulting in one common circuit configuration for all applications. Different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged. Advanced features like line undervoltage and overvoltage, external current limit programming, line feed-forward, and remote ON/OFF are easily implemented with a minimal number of external components, but do involve additional design considerations. For specific detail of how each of these features operates please refer to the LinkSwitch-HP data sheet.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the LinkSwitch-HP family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To simplify the task this application note refers directly to the PIXIs design spreadsheet that is part of the PI Expert™ design software suite. The basic configuration used in LinkSwitch-HP flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications used in the description throughout this application note.

In addition to this application note the reader may also find the LinkSwitch-HP Reference Design Kit (RDK) containing an engineering prototype board and device samples useful as an example of a working power supply. Further details on downloading PI Expert, obtaining a RDK and updates to this document can be found at www.powerint.com.

Quick Start

Readers willing to start immediately can use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXIs spreadsheet, other parameters will be automatically selected based on a typical design.

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} (Table 5) and line frequency f_L. Generally using a nominal line frequency of 50 Hz for a universal input design gives sufficient design margin.

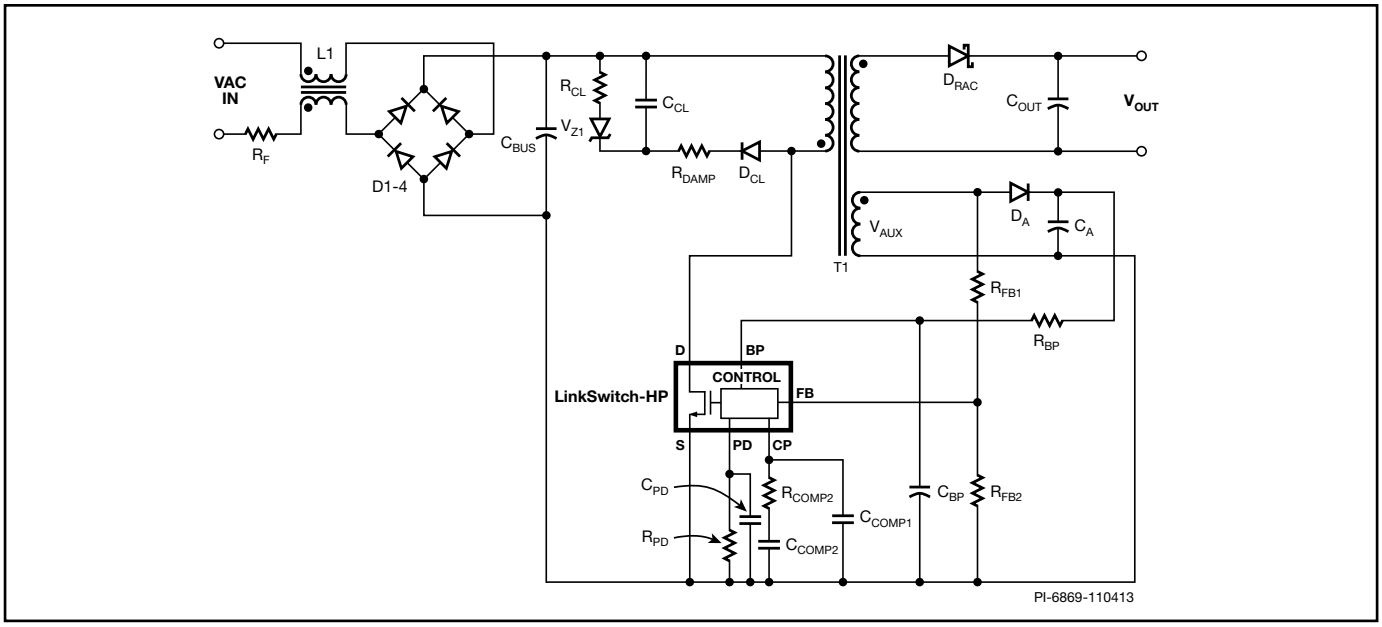


Figure 1. Typical LinkSwitch-HP Single Output Flyback Power Supply with Primary Sensed Voltage Regulation.

- Enter Nominal or Main Output Voltage V_O.
- Enter output power, P_O. If there is a peak power requirement then enter this value.
- Enter efficiency estimate, η, using Table 3 as a guide.

Input Voltage (VAC)	Output Voltage (V)	Efficiency Estimate (%)
85-265 or 85-132	3.3	77
	5	82
	≥12	86
190-265	3.3	77.5
	5	82.5
	≥12	87

Table 3. Efficiency Estimate vs. Input and Output Voltage.

Adjust the number accordingly after measuring the efficiency of the first prototype-board at maximum load and VAC_{MIN}.

- Enter loss allocation factor Z
  0.5 for typical application.
- Enter C_{IN} input capacitance
  2 µF/W ~ 3 µF/W for universal (85-265 VAC) or single (100/115 VAC) line.
  Use 1 µF/W single 230 VAC for single (185-265 VAC) line.
- Select LinkSwitch-HP from drop down list or leave as Auto. Auto selects device based on output power and line input voltage.

Select the device in the Table 4 according to output power and line input voltage.

- Enter core type (if desired) from drop down menu. A suggested core size will be selected automatically if none is entered.

Output Power Table1

Product[4]	Heat Sink	230 VAC ±15%		85-265 VAC	
		Adapter	Open Frame	Adapter	Open Frame
LNK67x3K/V	PCB-W[1]	15 W	25 W	9 W	15 W
LNK67x3K	PCB-R[2]	21 W	35 W	12 W	21 W
LNK67x3E	Metal	21 W	35 W	13 W	27 W
LNK67x4K/V	PCB-W[1]	16 W	28 W	11 W	20 W
LNK67x4K	PCB-R[2]	22 W	39 W	15 W	28 W
LNK67x4E	Metal	30 W	47 W	20 W	36 W
LNK67x5K/V	PCB-W[1]	19 W	30 W	13 W	22 W
LNK67x5K	PCB-R[2]	26 W	42 W	18 W	31 W
LNK67x5E	Metal	40 W	59[3] W	26 W	45 W
LNK67x6K/V	PCB-W[1]	21 W	34 W	15 W	26 W
LNK67x6K	PCB-R[2]	30 W	48 W	22 W	37 W
LNK67x6E	Metal	60 W	88[3] W	40 W	68[3] W
LNK67x7K/V	PCB-W[1]	25 W	41 W	19 W	30 W
LNK67x7K	PCB-R[2]	36 W	59 W	27 W	43 W
LNK67x7E	Metal	85[3] W	117[3] W	55 W	90[3] W

Table 4. Output Power Table.

Notes:
1. PCB heat sink with wave soldering.
2. PCB heat sink with IR reflow soldering (exposed pad thermally connected to PCB).
3. Maximum power specified based on proper thermal dissipation/heat sink size.
4. Packages: E: eSIP-7C, K: eSOP-12B, V: eDIP-12B. See Table 2 for all device options.

If any warnings are generated, make changes to the design by following instructions in spreadsheet column 6 (farthest to the right).

- Build transformer
- Select key components
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency, V_{MIN}).

Step-by-Step Design Procedure

Introduction

The design flow allows for design of power supplies either with or without a peak output power requirement. This is of particular relevance when using the V package with no heat sink attached, using the PCB as the heat sink. This results in a design which is thermally rather than device power capability limited. The power supply is then capable of delivering peak power for durations determined by the temperature rise of the LinkSwitch-HP and other power components in the circuit. The programmable shutdown delay feature (via the PROGRAM (PD) pin) may be used to trigger shutdown after a specified duration in applications where an output voltage droop is acceptable during peak power operation.

As average power increases, based on the measured transformer, device and output diode temperatures, it may be necessary to select a larger transformer to allow increased copper area for the windings, increase the amount of device and output diode heat sinking.

The output power table (Table 4) provides guidance for peak and continuous (average) power levels for both sealed adapters and open frame thermal conditions. For the eSIP (E) package it is assumed that an external heat sink is fitted and power delivery is limited by the device current limit. For the eDIP (V) and eSOP (K) packages, it is assumed that only the PCB is used for heat sinking and the device is thermally limited. As the current limit values are the same regardless of package the continuous values for the V and K package can be increased to those of the E package by improving heat sinking, for example placing a heat sink on the exposed pad on top of the package.

When using the design spreadsheet whenever an input cell is changed any changes in output calculations are highlighted in yellow. This is helpful in aiding understanding of the dependencies between parameters.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Select Core Size	**Auto**	EF25		
Core		EF25		Selected Core
Custom Core				Enter name of custom core is applicable
AE		0.518	cm^2	Core Effective Cross Sectional Area
LE		5.78	cm	Core Effective Path Length
AL		2000	nH/T^2	Ungapped Core Effective Inductance
BW		15.6	mm	Bobbin Physical Winding Width
M		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L		2		Number of Primary Layers
NS		10		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN		93	V	Minimum DC Input Voltage
VMAX		375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.55		Maximum Duty Cycle
IAVG		0.40	A	
IP		1.05	A	Peak Primary Current
IR		0.63	A	Primary Ripple Current
IRMS		0.56	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		670	uH	Typical Primary Inductance
LP_TOL		10	%	Primary inductance Tolerance
NP		87		Primary Winding Number of Turns
NB		8		Bias Winding Number of Turns
ALG		89	nH/T^2	Gapped Core Effective Inductance
BM		1571	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP		3422	Gauss	Peak Flux Density (BP<3700)
BAC		471	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1776		Relative Permeability of Ungapped Core
LG		0.70	mm	Gap Length (Lg > 0.1 mm)
BWE		31.2	mm	Effective Bobbin Width
OD		0.36	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.30	mm	Bare conductor diameter
AWG		29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		128	Cmils	Bare conductor effective area in circular mils
CMA		228	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

Figure 2. Highlighting Changes to Calculated Results, in this Example NS Input was Changed Resulting in Highlighted Output Changes in Yellow.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 5. Standard Worldwide Input Line Voltage Ranges.

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, $P_{O(AVE)}$, $P_{O(PEAK)}$, η, Z, V_B, t_C, C_{IN}

ENTER APPLICATION VARIABLES				Customer
VACMIN	85	V		Minimum AC Input Voltage
VACMAX	265	V		Maximum AC Input Voltage
fL	50	Hz		AC Mains Frequency
VO	12	V		Output Voltage (main)
PO	30	W		Specified Output Power
n	0.80			Efficiency Estimate
Z	0.50			Loss Allocation Factor
VB	10	V		Bias Voltage
tC	3	ms		Bridge Rectifier Conduction Time Estimate
CIN	90	uF		Input Filter Capacitor

Figure 3. Application Variable Inputs.

Line Voltage, VAC_{MIN}, VAC_{MAX}
Determine the input voltage range from Table 3. For DC input applications, for example where the supply is fed from a PFC generated DC bus, and provides a housekeeping / auxiliary supply in a larger system, enter the values for V_{MIN} and V_{MAX} directly.

Line Frequency, f_L
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimums. For most applications this gives adequate overall design margin. For absolute worst-case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz). For half-wave rectification, use $f_L/2$. The value of f_L is used to calculate the value of V_{MIN}.

DC INPUT VOLTAGE PARAMETERS			
VMIN	93	V	Minimum DC Input Voltage
VMAX	375	V	Maximum DC Input Voltage

Figure 4. DC Input Voltage Parameters.

Nominal Output Voltage, V_O (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally the main output is the output with the highest output power.

Output Power, P_O (W)
Enter the average output power of the power supply. If the power supply is a multiple output power supply, enter the sum total power of all the outputs.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under full load conditions and worst-case line (generally the lowest input voltage). Table 3 provides typical efficiency numbers for a single 5 V or 12 V output design. For multiple outputs calculate the proportion of the output power at lower voltage (<12 V) and higher voltage (≥12 V) and pick an efficiency estimate between the 5 V and 12 V numbers proportionally.

Power Supply Loss Allocation Factor, Z
This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, etc) are not processed by the power stage (transferred through the transformer) and therefore, although they reduce efficiency, the transformer design is not affected by their effect on efficiency.

Examples of primary-side losses are losses incurred in the input rectifier and EMI filter, MOSFET conduction losses and primary-side winding losses. Examples of secondary-side losses include the losses in secondary diode, secondary windings and core losses, losses associated with the primary-side clamp circuit and the bias winding. For designs that do not have a peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement, enter 0.65. This difference accounts for increased input stage losses under peak power loading when the input stage components (common mode chokes, differential inductors, thermistor, diode bridge) are sized for the average rather than the peak power.

Bias Winding Output Voltage (V_B)
Enter the voltage at the output of the bias winding output.
A starting value of 10 V is recommended. Higher voltages increase no-load input power while values below 9 V are not recommended as at light load there may be insufficient voltage to bias the controller causing higher no-load power. As the output load increases the IC switching frequency increases, causing the bias voltage to rise. This is useful as it compensates the increase in IC consumption causes by MOSFET drive increase with frequency.

Bridge Diode Conduction Time, t_C (ms)
Enter a bridge diode conduction time of 3 ms if there is no better data (from measurement) available.

Total Input Capacitance, C_{IN} (µF)
Table 6 suggests suitable multiplication factors to be used for calculating input capacitance for different AC input voltage ranges. Select the next largest standard value (or combination where two input capacitors are used). Using smaller values will result in a lower capacitor voltage and therefore higher primary RMS currents which will increases losses, device dissipation and reduce efficiency.

AC Input Voltage (VAC)	Total Input Capacitance Per Watt Output Power (µF/W) Full Wave Rectification
100/115	2-3
230	1
85-265	2-3

Table 6. Suggested Total Input Capacitance for Different Input Voltage Ranges.

Step 2 – Enter LinkSwitch-HP Variables: Device, Current Limit, V_{OR}, V_{DS}, V_D, Select the Correct LinkSwitch-HP Device

Device Selection
First, refer to LinkSwitch-HP output power table (Table 4). Then compare the continuous power to adapter column number, for enclosed designs, or compare to open-frame column number if the power-supply is open-frame design. If the column number is smaller than continuous power, then select the next larger device or choose a different device package type. Similarly, if the continuous power is close to the adapter power levels given in the power table, then it may be necessary to switch to a larger device based on the measured thermal performance of the prototype. In general, device thermals determine the maximum continuous power for adapter (enclosed) designs and device current limits for open-frame designs.

Output Power Table[1]

Product[4]	Heat Sink	230 VAC ±15%		85-265 VAC	
		Adapter	Open Frame	Adapter	Open Frame
LNK67x3K/V	PCB-W[1]	15 W	25 W	9 W	15 W
LNK67x3K	PCB-R[2]	21 W	35 W	12 W	21 W
LNK67x3E	Metal	21 W	35 W	13 W	27 W
LNK67x4K/V	PCB-W[1]	16 W	28 W	11 W	20 W
LNK67x4K	PCB-R[2]	22 W	39 W	15 W	28 W
LNK67x4E	Metal	30 W	47 W	20 W	36 W
LNK67x5K/V	PCB-W[1]	19 W	30 W	13 W	22 W
LNK67x5K	PCB-R[2]	26 W	42 W	18 W	31 W
LNK67x5E	Metal	40 W	59[3] W	26 W	45 W
LNK67x6K/V	PCB-W[1]	21 W	34 W	15 W	26 W
LNK67x6K	PCB-R[2]	30 W	48 W	22 W	37 W
LNK67x6E	Metal	60 W	88[3] W	40 W	68[3] W
LNK67x7K/V	PCB-W[1]	25 W	41 W	19 W	30 W
LNK67x7K	PCB-R[2]	36 W	59 W	27 W	43 W
LNK67x7E	Metal	85[3] W	117[3] W	55 W	90[3] W

Table 7. Output Power Table.

Notes:
1. PCB heat sink with wave soldering.
2. PCB heat sink with IR reflow soldering (exposed pad thermally connected to PCB).
3. Maximum power specified based on proper thermal dissipation/heat sink size.
4. Packages: E: eSIP-7C, K: eSOP-12B, V: eDIP-12B. See Table 2 for all device options.

ENTER LinkSwitch-HP VARIABLES					
LinkSwitch-HP	**Auto**		**LNK6766E**		Selected LinkSwitch-HP
ILIMITMIN			1.814	A	Minimum Current limit
ILIMITMAX			2.087	A	Maximum current limit
ILIMITMIN_EXT			1.814	A	External Minimum Current limit
ILIMITMAX_EXT			2.087	A	External Maximum current limit
KI	**Auto**		1.000	A	Current limit reduction factor
Rpd			124.00	k-ohm	Program delay Resistor
Cpd			33.00	nF	Program delay Capacitor
Total programmed delay			0.86	sec	Total program delay
fS			132	kHz	LinkSwitch-HP Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			124	kHz	LinkSwitch-HP Minimum Switching Frequency
fSmax			140	kHz	LinkSwitch-HP Maximum Switching Frequency
KP			0.60		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR			108.40	V	Reflected Output Voltage
Voltage Sense					
VUVON			102.11	V	Undervoltage turn on
VUVOFF			43.19	V	Undervoltage turn off
VOV			462.09	V	Overvoltage threshold
FMAX_FULL_LOAD			135.55	kHz	Maximum switching frequency at full load
FMIN_FULL_LOAD			120.06	kHz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD			3.23	us	Minimum available Diode conduction time at full load. This should be greater than 2.7 us
TSAMPLE_LIGHT_LOAD			2.52	us	Minimum available Diode conduction time at light load. This should be greater than 1.4 us
VDS			3.29	V	LinkSwitch-HP on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop

Figure 5. LinkSwitch-HP Variables Section of Design Spreadsheet.

External Current Limit Reduction Factor, KI

The user entered factor KI indicates which device current limit will be selected. There are seven discrete current limit settings between 40% and 100% (=default) in incremental steps of 10%. Each is set via the value of the external programming resistor R_{PD} (Cell [A35]) as shown in Table 8. In some countries like Korea, the 1% standard resistor value is different than the standard E96 value. To make it easy for resistor selection for the users, the adjusted external programming resistor R_{PD} provided in Table 9 that is compliant with 1% standard resistor values in Korea. This value is measured at start-up and latched internally until the IC is reset at power-down. In most cases the current limit level should be set slightly above (15%) the minimum peak current (I_P) required for power delivery. This optimizes the transformer design by limiting the peak flux density (BP) during overload and start-up when the primary and MOSFET current will reach current limit.

I_{PD} (µA)	R_{PD} (kΩ)	I_{LIMIT_NORM} (%)	I_{PD} (µA)	R_{PD} (kΩ)	I_{LIMIT_NORM} (%)
10	124	100	54	23.2	60
16	78.7	90	83	15	50
24	52.3	80	125	10	40
36	34.8	70			

Table 8. Current Limit Reduction vs. Value of R_{PD}.

I_{PD} (µA)	R_{PD} (kΩ)	I_{LIMIT_NORM} (%)	I_{PD} (µA)	R_{PD} (kΩ)	I_{LIMIT_NORM} (%)
9.5	130	100	51.6	24	60
16.5	75	90	82.7	15	50
24.3	51	80	125	10	40
37.5	33	70			

Table 9. Current limit Reduction vs. Value of R_{PD} Adjusted to be Compliant with Korea 1% Standard Resistor Value.

For higher efficiency and improved thermal performance, KI also allows the selection of a larger LinkSwitch-HP device to be used than required for power delivery by reducing KI, such that the current limit of the larger device is set to still be slightly above the calculated value for I_{PK}.

Setting the current limit significantly higher (for instance 50%) than the value of I_{PK} for power delivery can improve efficiency, especially for single AC input high-line only (190–265 VAC) designs. At high input voltages switching losses, as opposed to conduction losses, become dominant, are proportional to switching frequency. Setting the current limit 50% higher than required for power delivery reduces the device switching frequency. This is due to the control behavior of LinkSwitch-HP devices, when the primary peak current reduces to below 50% of the set current limit the switching frequency of the device reduces. (Note that the maximum output power of the power supply will be increased accordingly).

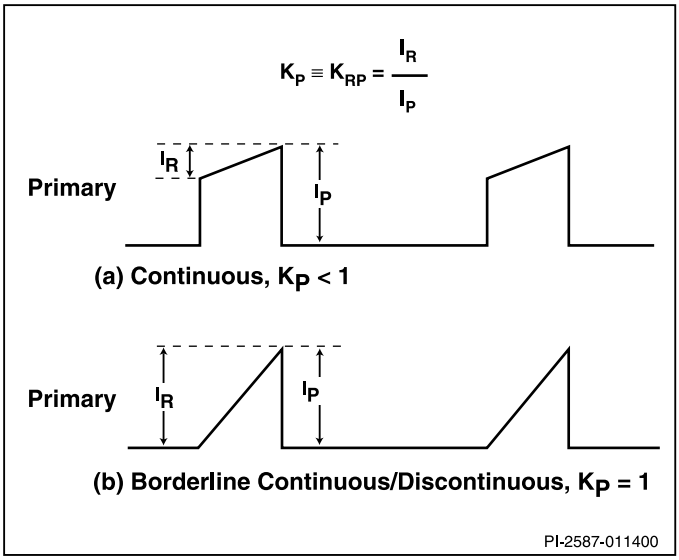


Figure 6. CCM and DCM Operation Waveform.

Switching Frequency

Typical switching frequency is 132 kHz. (Please refer to LinkSwitch-HP data sheet Figure 5 for explanation of multimode operation).

Ripple to Peak Current Ratio, K_P

K_P is the ratio of ripple to peak primary current. Generally, K_P >1 for DCM (Discontinuous Conduction Mode) operation and K_P <1 for CCM (Continuous Conduction Mode) operation and relates to the primary current waveshape.

DCM operation is not suitable for LinkSwitch-HP based designs due to the requirement that output current is still flowing in the output diode at the time point where the feedback is sampled. Hence there is a K_P restriction and it is recommended that the K_P value remains in the range of 0.5 to 0.6 for universal input voltage.

Lower K_P values leads to larger primary inductance values (L_P). This results in a higher number of turns, increasing leakage inductance and reducing allowable cross section of copper that will fit in the bobbin window. Higher K_P values mean shorter secondary diode conduction times which can approach to 1.2 µs which is the minimum sampling time requirement for the device to maintain regulation at no-load. For robust designs K_P needs to be in the recommended range. Cell D34 and D33 reports the calculated minimum secondary diode conduction time at light load/no-load and full load respectively, for a chosen K_P and V_{OR}.

Reflected Output Voltage, V_{OR} (V)

This parameter is the secondary winding voltage during diode conduction, reflected back to the primary through the turn's ratio of the transformer.

For LinkSwitch-HP based designs, the V_{OR} value is restricted by the secondary diode conduction time and maximum duty cycle. Recommended V_{OR} values are in the range of 80 V to 125 V.

For design optimization purposes, the following trade-offs should be considered:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the input capacitance value and maximizes power delivery from a given LinkSwitch-HP device.
2. Higher V_{OR} reduces the voltage stress on the output diodes, which in some cases may allow the use of a lower forward drop Schottky diode for higher efficiency.
3. Higher V_{OR} can increase leakage inductance and increase clamp losses that reduces efficiency of the power supply and degrades cross regulation in multiple output designs.
4. Higher V_{OR} increases peak and RMS current on the secondary-side, which may increase secondary-side copper and diode losses.

Optimal selection of the V_{OR} value depends on the specific application and is based on a compromise between the factors mentioned above. For lower voltage outputs (approximately 5 V or multiple output designs) a lower V_{OR} of approximately 100 V - 110 V is recommended. For higher voltage outputs (12 V and above) a higher V_{OR} of approximately 110 and 120 V is recommended.

Values below 80 V are not usually recommended. Low V_{OR} may cause excessive triggering of the MOSFET self-protection feature during start-up, especially in higher output (>12 V) designs, resulting in an output voltage rise that is not uniform.

Issue	Suggested Action	Comment
D34 (minimum diode conduction time at light load/no-load) <1.4 µs	Decrease K_P until D34 >1.4 µs	500 ns margin from 1.2 µs is desirable. Hence D34 ≥1.7 µs
D33 (minimum diode conduction time at full load) <2.7 µs	Decrease V_{OR} until D33 >2.7 µs	500 ns margin from 2.5 µs is desirable. Hence D33 ≥3.0 µs

Table 10. Suggested Actions for K_P and V_{OR} Values.

Line Sense (VUV_{ON}, VUV_{OFF})

VUV_{ON} (undervoltage turn-on) is the desired input line voltage (DC) when the LinkSwitch-HP starts switching during brown-in. This parameter is determined by the turns ratio of bias winding NB to primary winding N_P and the resistor value R_{FB1} (Figure 8) which is the top resistor of the feedback resistor divider from bias winding (also feedback sense winding). Typically 100 V is recommended value for universal input range.

By selecting the desired VUV_{ON} threshold the spreadsheet will compute the appropriate value of R_{FB1}. Only VUV_{ON} threshold is selectable. VUV_{OFF} and VOV will be positioned according to VUV_{ON} threshold selection.

Voltage Sense					
VUVON			102.11	V	Undervoltage turn on
VUVOFF			43.19	V	Undervoltage turn off
VOV			462.09	V	Overvoltage threshold

Figure 7. Line Voltage Sense Section of Design Spreadsheet.

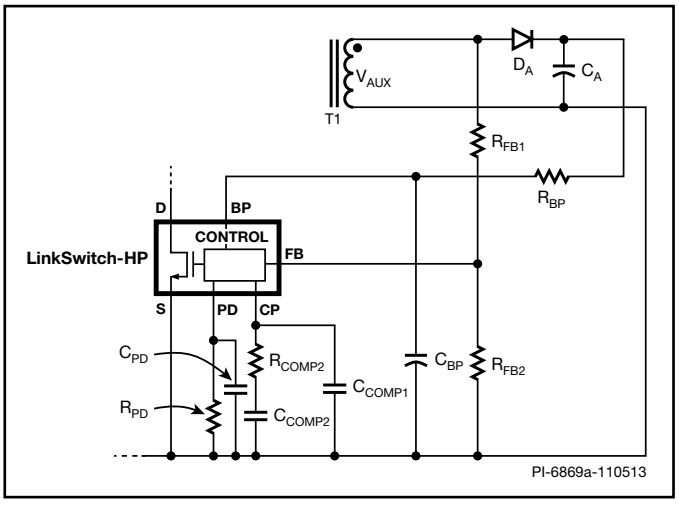


Figure 8. Typical Primary Configuration.

VUV_{OFF} (undervoltage turn-off) is the brown-out voltage threshold below which the LinkSwitch-HP stops switching. This is a fixed ratio to VUV_{ON}.

VOV (overvoltage turn-off) determines the line over voltage threshold above which the device stops switching.

Minimum Sampling Time Under Light and Heavy Load Conditions

These cells show flyback conduction time (the time period the output diode is conducting) for light and full load conditions. As shown in Figure 10 the sampling time reduces with reducing load. A warning is displayed if the conduction time is too short for either case. The typical sampling time is 1.2 µs at no-load or light load, and 2.5 µs at full load. TSAMPLE_LIGHT_LOAD is adjusted to be 1.4 µs and TSAMPLE_FULL_LOAD is adjusted to be 2.7 µs to cover the possible variable range. Please refer to Table 10 for desirable values of these parameters.

Shutdown Delay Capacitor (C_{PD})

Desired shutdown delay time (in addition to the standard 35 ms) can be programmed by selecting a delay capacitor (C_{PD}) value for a chosen current limit resistor (R_{PD}). Resistor R_{PD} is automatically selected when choosing a KI factor. The total programmed delay is

FEEDBACK SENSING SECTION					
RFB1			35.70	k-ohms	Feedback divider upper resistor
RFB2			9.09	k-ohms	Feedback divider lowerr resistor

Figure 9. Feedback Sense Resistor Values Section of Design Spreadsheet.

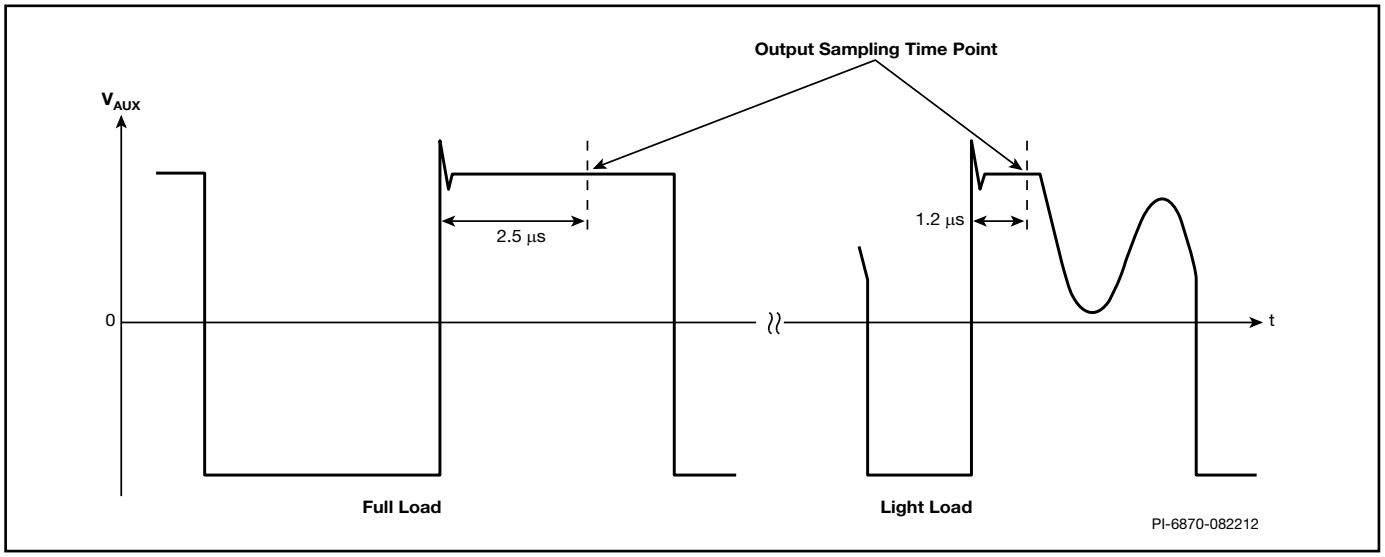


Figure 10. Sampling Time.

ENTER LinkSwitch-HP VARIABLES					
LinkSwitch-HP	**Auto**		**LNK6766E**		Selected LinkSwitch-HP
ILIMITMIN			1.814	A	Minimum Current limit
ILIMITMAX			2.087	A	Maximum current limit
ILIMITMIN_EXT			1.814	A	External Minimum Current limit
ILIMITMAX_EXT			2.087	A	External Maximum current limit
KI	**Auto**		1.000	A	Current limit reduction factor
Rpd			124.00	k-ohm	Program delay Resistor
Cpd			33.00	nF	Program delay Capacitor
Total programmed delay			0.86	sec	Total program delay

Figure 11. Shutdown Delay Section of Design Spreadsheet.

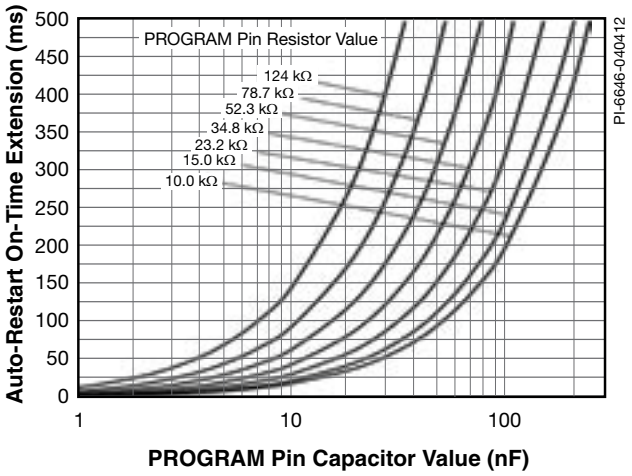


Figure 12. Shutdown Time Extension Programming.

reported in Cell [E37]. C_{PD} also works as a noise filter capacitor for the PROGRAM pin, a recommended capacitor value of 1 nF will be required to pass the surge test for 6 kV.

LinkSwitch-HP ON-State Drain to Source Voltage, V_{DS} (V)
This parameter is the average ON state voltage developed across the DRAIN and SOURCE pins of LinkSwitch-HP. By default, if the grey override cell is left empty, a value of 4 V is assumed. Use the default value if no better data is available.

Output Diode Forward Voltage Drop, V_D (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN diode if no better data is available. By default, a value of 0.5 V is assumed.

Bias Winding Diode Forward Voltage Drop, V_{DB} (V)
Enter the average forward voltage drop of the bias winding output diode. Use 0.7 V for a PN junction diode.

Feedback Resistor Network
The top resistor R_{FB1} value is already determined by the UV and OV functions described above. The spreadsheet computes the value of the bottom resistor of the feedback resistor divider R_{FB2} to scale the flyback feedback signal from the bias winding to give desired output voltage regulation.

RFB_1 is selected based on line UV turn on threshold of -250 µA (Typ) when MOSFET in ON.

$$V_{AUX} = -\frac{N_A \times (V_{BUS} - V_{DS})}{N_P}; R_{FB1} = \frac{V_{AUX}}{-250\ \mu A}$$

RFB_2 is calculated based on V_{REF} = 2.0 V and V_{AUX} when MOSFET is OFF.

$$V_{AUX} = \frac{N_A \times (V_{SEC})}{N_S}; V_{REF} = \frac{V_{AUX} \times (R_{FB2})}{(R_{FB1} + R_{FB2})}$$

PI-6945-012213

Figure 13. Formula for Calculation of R_{FB1} and R_{FB2}.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Select Core Size	**Auto**		EF25		
Core			EF25		Selected Core
Custom Core					Enter name of custom core is applicable
AE			0.518	cm^2	Core Effective Cross Sectional Area
LE			5.78	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			15.6	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of Primary Layers
NS			10		Number of Secondary Turns

Figure 14. Transformer Construction Section of Design Spreadsheet.

As defined in former section, opening the top feedback resistor R_{FB1} leads to an open-loop protection, the device enters into auto-restart mode. In case of opening the feedback resistor divider R_{FB2}, the FEEDBACK pin is connected to the bias winding through the top feedback resistor R_{FB1}, the loop is not really open in this case. The lack of the voltage divider will cause the output voltage to be much lower than the regulated output, as the device now regulates the winding voltage to be the same as the reference voltage of the trans-conductance amplifier. It may also cause the power supply to enter into a fault condition depending on the load, then the power supply will go into auto-restart or still latch depending on circuit configuration.

Step 3 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, BW, M, L, N_S

Core effective cross-sectional area, A_E (cm^2)
Core effective path length, L_E (cm).
Core ungapped effective inductance, A_L ($nH/turn^2$).
Bobbin width, BW (mm)
Tape margin width equal to half the total margin, M (mm)
Primary layers, L
Secondary turns, N_S

Core Type

Enter the core type chosen for the design.

Output Power	Triple Insulated Wire	Margin Wound
0 - 10 W	EF12.6 EE13 EF16 EE16	EI22 EE19 EI22/19/6 EEL16
10 W - 20 W	EE19 EI22 EI22/19/6 EF20	EF20 EI25 EEL19
20 W - 30 W		EI28
30 W - 50 W	EF25	EEL22
50 W - 70 W	EI28	EEL25 E30/15/7 EER28

Table 11. Suggested Core Sizes vs. Outrput Power.

The grey override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list, or the specific core or bobbin information differs from that referenced by the spreadsheet.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary but do not use triple-insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. For universal input designs, a total windings margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin. For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically, many bobbins exist for any core size and, each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

As the margin reduces the available area for the windings, the margin format described above may not be suitable for small core sizes. If after entering the margin, more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design approach using triple-insulated wire.

Primary Layers, L

Primary layers should be in the range of $1 < L < 3$, and in general it should be the lowest number that meets the primary current density limit (CMA). Values of 200 Cmils/A for designs <5 W scaling linearly to 500 Cmils/A at 200 W are typical in designs without forced air cooling. Designs with more than 3 layers are possible, but the increased leakage inductance and issues associated with the physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high. Here half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement.

Secondary Turns, NS

If the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density BM is kept below the recommended maximum of 3100 Gauss (310 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of BM limits).

Step 4 – Iterate Transformer Design and Generate Initial Design

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the output transformer design parameters can be used to either wind a prototype transformer or sent to a vendor for samples.

The Key Transformer Electrical Parameters

Primary Inductance, L_P (µH)
This is the target nominal primary inductance of the transformer.

Primary Inductance Tolerance, $L_{P\_TOLERANCE}$ (%)
This is the assumed primary inductance tolerance. A value of 10% is used by default, however if specific information is known from the transformer vendor, then this may be entered in the grey override cell.

Number of Primary Turns, N_P
Total number of primary turns. For low leakage inductance applications, a split primary construction may be used.

Gapped Core Effective Inductance, ALG (nH/N²)
Used by the transformer vendor to specify the core (gap).

Maximum Operating Flux Density, BM (Gauss)
A maximum value of 3100 Gauss (310 mT) for maximum specified output power is recommended to limit the maximum flux density under start up and output short-circuit.

Multi-cycle modulation mode (MCM) of operation used in LinkSwitch-HP can operate in the audio spectrum but avoids causing audible noise from core due to the unique patterning of on pulses as shown in Figure 15. This technique avoids producing harmonics in the 5 kHz to 20 kHz region where the core can create significant audible noise.

Ceramic capacitors that use dielectrics, such as Z5U, when used in the clamp circuit may also generate audio noise. If such is the case, try replacing them with capacitors having a different dielectric, for example a metalized film type.

Peak Flux Density, B_P (Gauss)
A maximum value of 3700 Gauss (370 mT) is recommended to limit the maximum flux density under start up and output short- circuit conditions. This calculation assumes worst-case current limit specification and inductance value. To determine, verify that core saturation does not occur at maximum ambient temperature under overload conditions just prior to loss of regulation.

Maximum Primary Wire Diameter, OD (mm)
By default, if the override cell is empty, double insulated wire is assumed and the standard wire diameter is chosen. The grey override cells can be used to enter the wire diameter directly by the user, if the wire used is different from the standard double insulated type.

The other factors automatically calculated by the spreadsheet includes:

Estimated total insulation thickness, INS (mm)
Primary wire size, DIA (mm)
Primary wire gauge, AWG
Number of primary layers, L
Estimated core center leg gap length, L_G (mm)
Number of secondary turns, N_S
Secondary wire size, DIA_S (mm)
Secondary wire gauge, AWG

In multiple output designs NSx, CMSx, AWGSx (where x is the output number) should also be used.

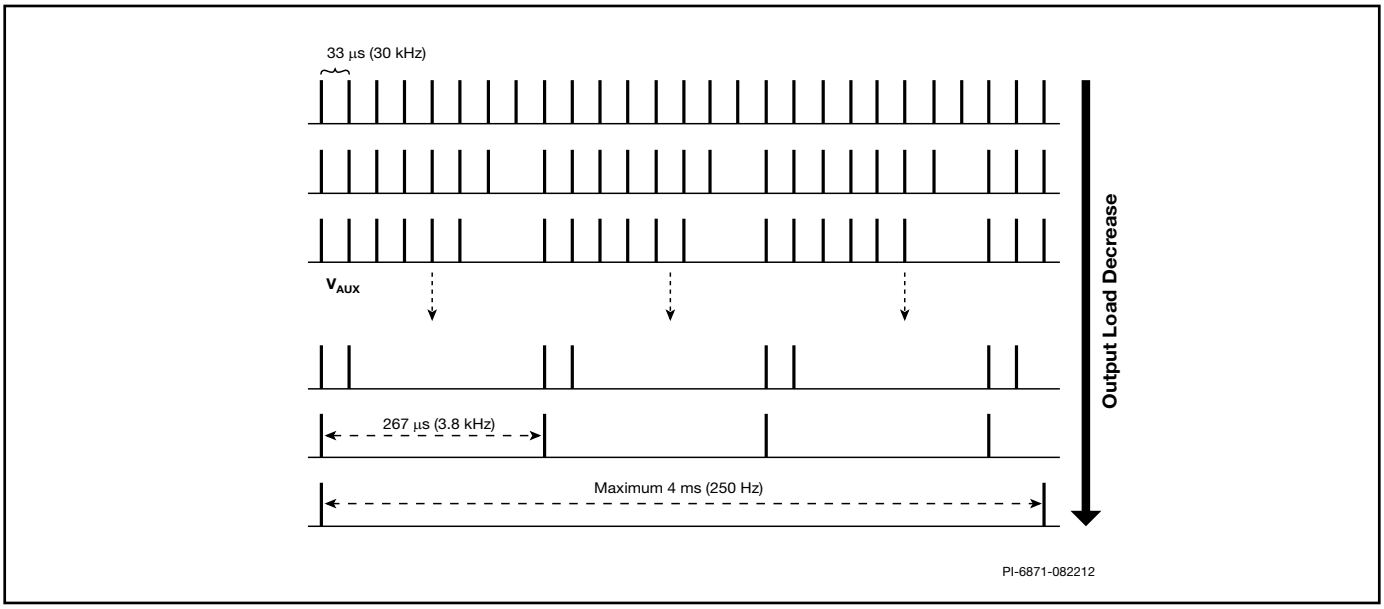


Figure 15. Light Load Switching Patterns in MCM Avoid Creating Audible Noise due to Transformer Core Magnetostriction (LNK67xx).

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_TYP			670	uH	Typical Primary Inductance
LP_TOL			10	%	Primary inductance Tolerance
NP			87		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			89	nH/T^2	Gapped Core Effective Inductance
BM			1571	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3422	Gauss	Peak Flux Density (BP<3700)
BAC			471	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1776		Relative Permeability of Ungapped Core
LG			0.70	mm	Gap Length (Lg > 0.1 mm)
BWE			31.2	mm	Effective Bobbin Width
OD			0.36	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.30	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA			228	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

Figure 16. Transformer Primary Design Parameters Section of the Design Spreadsheet.

TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			9.14	A	Peak Secondary Current
ISRMS			4.43	A	Secondary RMS Current
IO			2.50	A	Power Supply Output Current
IRIPPLE			3.66	A	Output Capacitor RMS Ripple Current
CMS			886	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.81	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.56	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.37	mm	Maximum Secondary Insulation Wall Thickness

Figure 17. Transformer Secondary Design Parameters Section of Spreadsheet – Lumped Into Single Output.

The front of spreadsheet has main output entered and total output power of design which is sufficient for a single output design. This section is where the necessary additional information is entered when designing for multiple outputs. For multiple output designs the specific output voltages and associated output currents are entered below.

Step 5 – Selection of LinkSwitch-HP External Components

Noise Decoupling

The schematic in Figure 8 shows the external components required for a typical LinkSwitch-HP power supply. It is essential that the BYPASS pin capacitor be physically located as close as possible to the BYPASS pin with very short trace length to SOURCE pin to minimize noise pick-up. Capacitor C_{COMP1}, which is normally 100 pF, should also be placed directly from the COMPENSATION pin to SOURCE pin to minimize noise pick up which will cause poor output ripple and regulation.

Compensation

A value of 100 kΩ for R_{COMP2} and 100 nF for C_{COMP2} gain setting of the control loop is advised. This gives about 21 dB gain for the transconductance error amplifier stage (feedback input to COMPENSATION pin output gain) and performs very well for most designs giving good stability and fast output transient response.

Values greater than 200 kΩ for R_{COMP2} are not recommended. Details on how this is determined are described in later section.

Bias Support

The bias capacitor C_A is typically 10 μF to 22 μF which provides adequate hold-up for the support bias into the BYPASS pin during light or no-load conditions while the operating frequency is low. The support current should be at least 550 μA into the BYPASS pin to ensure the internal current source of LinkSwitch-HP is turned off, minimizing no-load input power consumption. The bias voltage across C_A should be around 8 V or 9 V at no-load for minimum input power. The bias feed resistor R_{BP} into the BYPASS pin is typically 4 kΩ to 5 kΩ. At higher loads more bias current is required (see data sheet supply current parameter I_{BPS1}) and a good way to check if bias is sufficient is to monitor the BYPASS pin voltage from minimum to maximum load with an oscilloscope. The BYPASS pin voltage should never dip below 6.1 V over the entire output load range.

Primary Clamp

Correct clamp design is critical for correct operation of a LinkSwitch-HP design.

It is highly recommended that the Zener bleed primary clamp circuit be used (see Figure 20). A simple RCD clamp can lead to a significant increase of the no-load input power (see comparison graph in Figure 21), poor light and no-load regulation if preload is not present. A RCD clamp may also cause some oscillation at light load if the snubber components are not carefully selected.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12	V	Output Voltage
IO1			2.50	A	Output DC Current
PO1			30.00	W	Output Power
VD1			0.5	V	Output Diode Forward Voltage Drop
NS1			10.00		Output Winding Number of Turns
ISRMS1			4.432	A	Output Winding RMS Current
IRIPPLE1			3.66	A	Output Capacitor RMS Ripple Current
PIVS1			55	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1			886	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			20	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.81	mm	Minimum Bare Conductor Diameter
ODS1			1.56	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				V	Output Voltage
IO2				A	Output DC Current
PO2			0.00	W	Output Power
VD2			0.7	V	Output Diode Forward Voltage Drop
NS2			0.56		Output Winding Number of Turns
ISRMS2			0.000	A	Output Winding RMS Current
IRIPPLE2			0.00	A	Output Capacitor RMS Ripple Current
PIVS2			2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				V	Output Voltage
IO3				A	Output DC Current
PO3			0.00	W	Output Power
VD3			0.7	V	Output Diode Forward Voltage Drop
NS3			0.56		Output Winding Number of Turns
ISRMS3			0.000	A	Output Winding RMS Current
IRIPPLE3			0.00	A	Output Capacitor RMS Ripple Current
PIVS3			2	V	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			30	W	Total Power for Multi-output section
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Figure 18. Transformer Secondary Design Parameters Section of Spreadsheet – Lumped Into Single Output.

It is worth pointing out that the Zener bleed configuration is not the same as a Zener clamp. In the Zener clamp configuration, there is no resistor in series with the Zener and no parallel capacitor as shown in Figure 19. Therefore the Zener dissipates all of the power in the clamp and is subjected to peak currents close to the peak primary current. Even though the average power dissipation in the clamp is low, the pulse power dissipation in the Zener is high. This high stress and power requires the use of a transient voltage suppressor (TVS) part from the P6KE series, which should be appropriately selected with sufficient de-rating. Unlike the Zener (TVS) clamp, the Zener bleed circuit has a soft-knee which only results in a non-linear increase in the load across the clamp capacitor. This reduces the peak current in the Zener and also lowers the pulse power dissipation in the Zener, thereby ensuring low Zener stress. Typically, in the Zener bleed configuration, the peak current is limited by the series resistor to 10's of mA. The much lower stress on the Zener allows the use of low-cost 1 W components (vs. TVS types) and removes reliability concerns due to operating the Zener close to its maximum rating.

As shown in Figure 19, the power dissipation in the zener used in the Zener bleed circuit, is considerably lower than the peak power dissipated in a Zener (TVS) clamp type circuit.

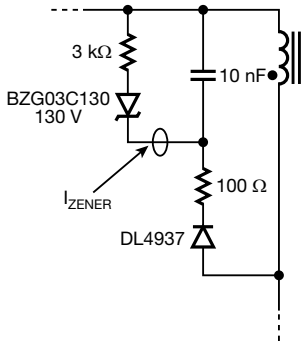
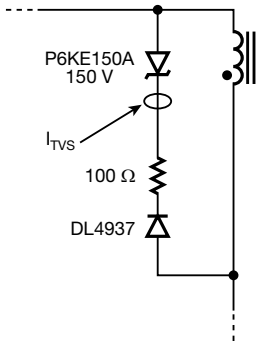
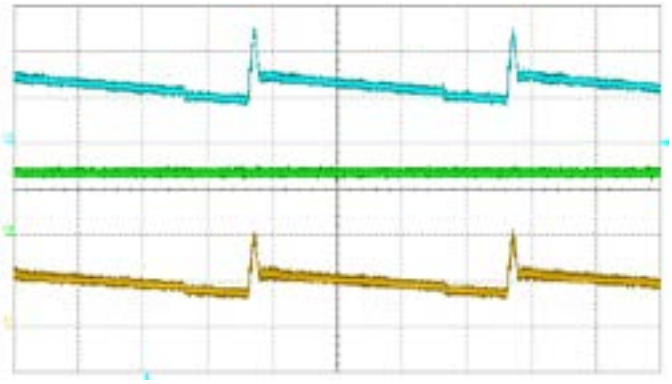
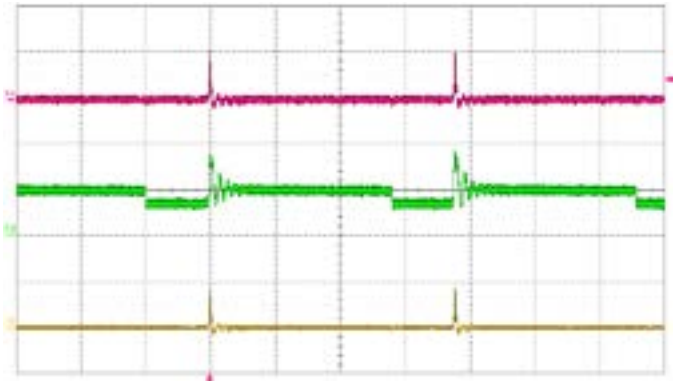
RCDZ (Zener Bleed)	Zener Clamp
 PI-7190-110113	 PI-7191-110113
	
RCDZ Clamp (300 VDC Input, 2.5 A Load). Upper: I_{ZENER}, 1 mA / div, 2 µs / div. (Waveforms measured voltage across 3 kΩ resistor) Middle: V_{ZENER}, 100 V / div, 2 µs / div Lower: Power Dissipation of Zener, 0.17 W / div. Zener: Peak Power Dissipation = 0.36 W. Zener: Mean Power Dissipation (approximately) = 165 mW.	Zener Clamp (300 VDC Input, 2.5 A Load). Upper: I_{TVS}, 500 mA / div, 2 µs / div. Middle: V_{TVS}, 100V / div, 2 µs / div. Lower: Power Dissipation of TVS, 100 W / div. TVS: Peak Power Dissipation = 97 W. TVS: Mean Power Dissipation (approximately) = 843 mW.

Figure 19. Comparison Between RCDZ and Zener Clamp.

With an RCD clamp and operation at light or no-load the voltage of C_{C1} discharges below the value of V_{OR}. When the next flyback cycle occurs, the primary clamp circuit now appears as a load, the voltage of C_{C1} must exceed the value of V_{OR} before the output diode and bias diode will conduct.

This loading effect causes the output voltage sampled via the bias winding to appear low and therefore the control loop responds and the output voltage rises above the correct value. This error may also cause bursts of pulses as the bias on C_{C1} changes erratically depending on operating frequency.

At higher load the RCD clamp allows the leakage spike amplitude to become significantly higher causing more ringing on the primary and feedback winding which may also cause oscillation due to variation in the sampled voltage. Unlike the RCD clamp, the Zener bleed circuit ensures that there is virtually no load across the clamp capacitor once the clamp capacitor is discharged to a level below the rated Zener voltage. This non-linearity provides excellent regulation from a PSR converter since it allows the bias winding and primary winding voltages to track the secondary output voltage even at light-load.

For RCDZ (Zener bleed), the value of C_{C1} is typically 1 nF for converters under 10 W and 10 nF for designs above 10 W. R_{C2} is typically 2 kΩ to 20 kΩ, adjusted such that the voltage on C_{C1} is approximately $V_{OR} \times 1.5$. The voltage rating for D_{C2} should be the next standard value above V_{OR} + 10 V.

R_{DAMP} must be high enough in value to damp out ringing – there should be no visible ringing in the drain voltage waveform beyond 1 µs from initial turn-off of the power MOSFET.

As can be seen in the regulation graph below, the RCD snubber also causes the output to rise outside of regulation limits at light load for the same preload condition. Solving this requires a heavier preload resistor which further increases no-load input power.

Finally, the RCDZ clamp shown below can be optimized to minimize ringing on the feedback winding flyback pulse. The damping resistor R_{DAMP} value has a strong effect on the amount of ringing that develops on the feedback winding as can be seen in the two cases below. Notice at the MOSFET turn-off edge how strongly the feedback winding waveform follows the primary winding qualitatively.

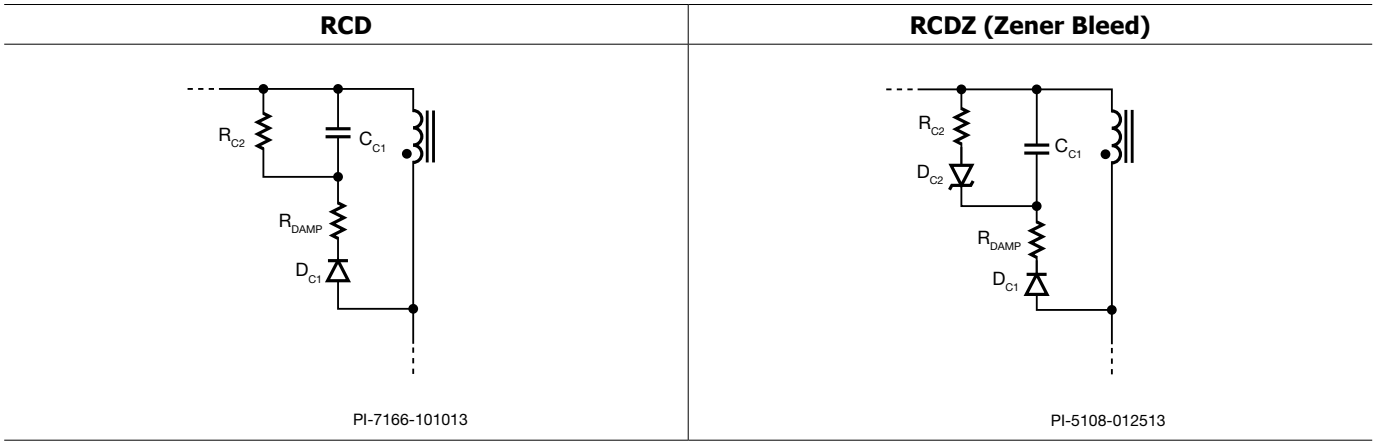


Figure 20. Primary Clamp Arrangement.

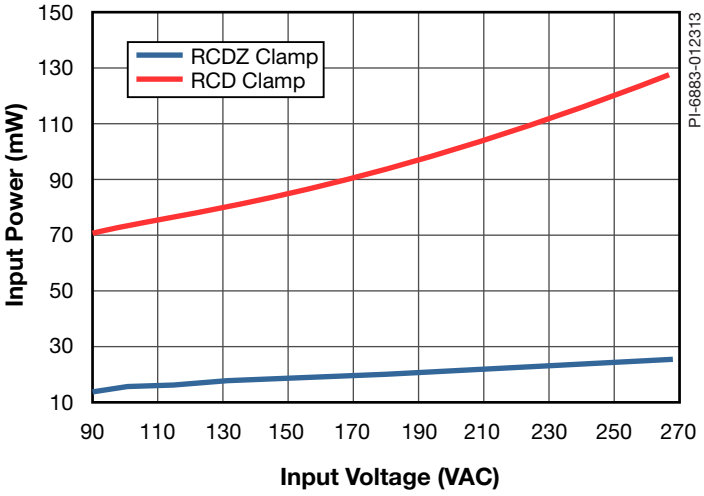


Figure 21. Comparison of No-Load Input Power for a 30 W Adapter Using RCD and RCDZ to Primary Clamp.

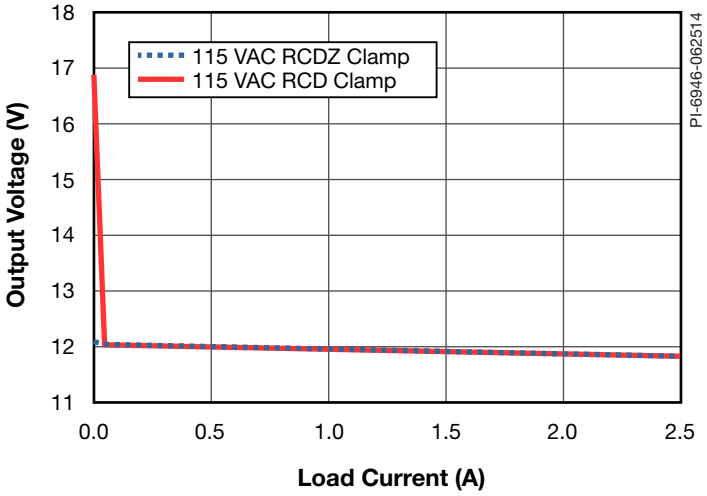


Figure 22. Comparison of Regulation for a 30 W Adapter Using RCD and RCDZ to Primary Clamp.

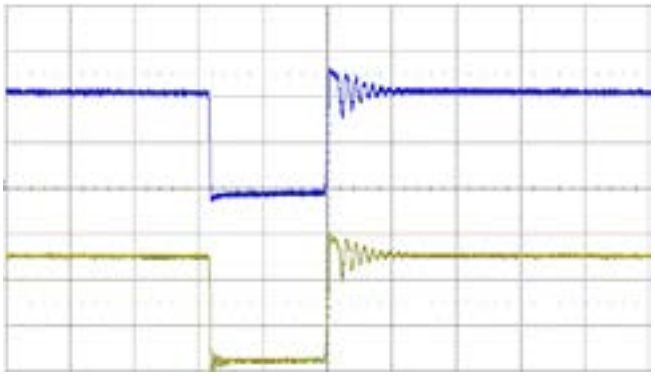
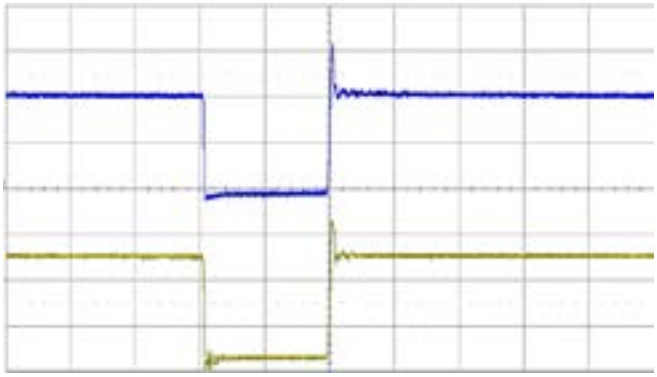
RCDZ Clamp with 20 Ω R_{DAMP}	RCDZ Clamp with 220 Ω R_{DAMP}
	
RCDZ Clamp with 20 Ω R_{DAMP}. Upper: VDS 200 V / div. Lower: Feedback Winding 20 V / div.	RCDZ Clamp with 220 Ω R_{DAMP}. Upper: VDS 200 V / div. Lower: Feedback Winding 20 V / div.

Figure 23. Comparison of Feedback Winding Ringing with Different Values of R_{DAMP}.

A simple RCD clamp circuit can also be used however satisfactory operation will require careful selection of the clamp circuit component. Specifically, clamping capacitor C_{C1}, clamping resistor R_{C2}, and damping resistor R_{DAMP} values have to be selected with care. When the RCD clamp Snubber is used, it may be necessary to place a slightly higher preload at the power supply output in order to achieve stable operation and improved load regulation. Use of higher preload could result in increased no-load power consumption. At moderate and high load, the RCD clamp allows the leakage spike amplitude to become significantly higher, so the maximum drain voltage at maximum input voltage and overload condition should be carefully checked. A minimum of 10% margin compared to the MOSFET breakdown voltage is highly recommended.

Transformer Construction

Leakage inductance and interwinding capacitance. Key recommendations – (1) $L_{LEAK}/L_{PRI} \leq 2\%$, (2) $f_{RES} \geq 200$ kHz.

1. $L_{LEAK} / L_{PRI} \leq 2\%$.
2. $F_{RES} \geq 200$ kHz.

When designing a converter with LinkSwitch-HP the ratio of leakage inductance to primary inductance should be no greater than 2%. The inter-winding capacitance should be such that the natural resonant frequency of the primary is not less than 200 kHz. Both of these parameters are easily measured by LCR meters and routinely given as part of specifications to magnetic component suppliers. For resonant frequency this can be directly measured from the frequency of the ringing seen on the drain voltage waveform.

Energy stored in the leakage inductance and inter-winding capacitance will be dissipated for every cycle and result in lower efficiency. Inter-winding capacitance will primarily affect efficiency at lighter loads. Even though LinkSwitch-HP reduces inter-winding capacitance related losses by reducing the operating frequency at lighter loads it is still important to keep this capacitance to a minimum for best efficiency and lowest no-load input power. Leakage inductance becomes dominant as a loss factor at higher output loads. Higher leakage transformer designs require more a substantial primary clamp to handle the increased power dissipation. The power MOSFET drain voltage spike at turn-off is typically higher with higher leakage transformers which may reduce maximum drain voltage margin.

Good regulation using LinkSwitch-HP also requires a low leakage low capacitance transformer design to avoid excessive ringing on the feedback winding which affects the accuracy and stability of the regulation loop as shown in figure below. The sampling delay time of the FEEDBACK pin varies linearly from 1.2 µs to 2.5 µs, for load variation from minimum to maximum load. If there is significant ringing on the feedback winding pulse within the sampling range, the potential for poor regulation and instability at certain load points is high. The voltage valleys and peaks of the feedback winding pulse from excessive ringing will cause the sampling delay to shift back and forth in an oscillatory manner in response to the apparent changing feedback voltage. If a design is unstable at particular load points it is almost certain that it is caused by ringing on the feedback winding and very rarely is it related to the loop compensation values across the COMPENSATION pin.

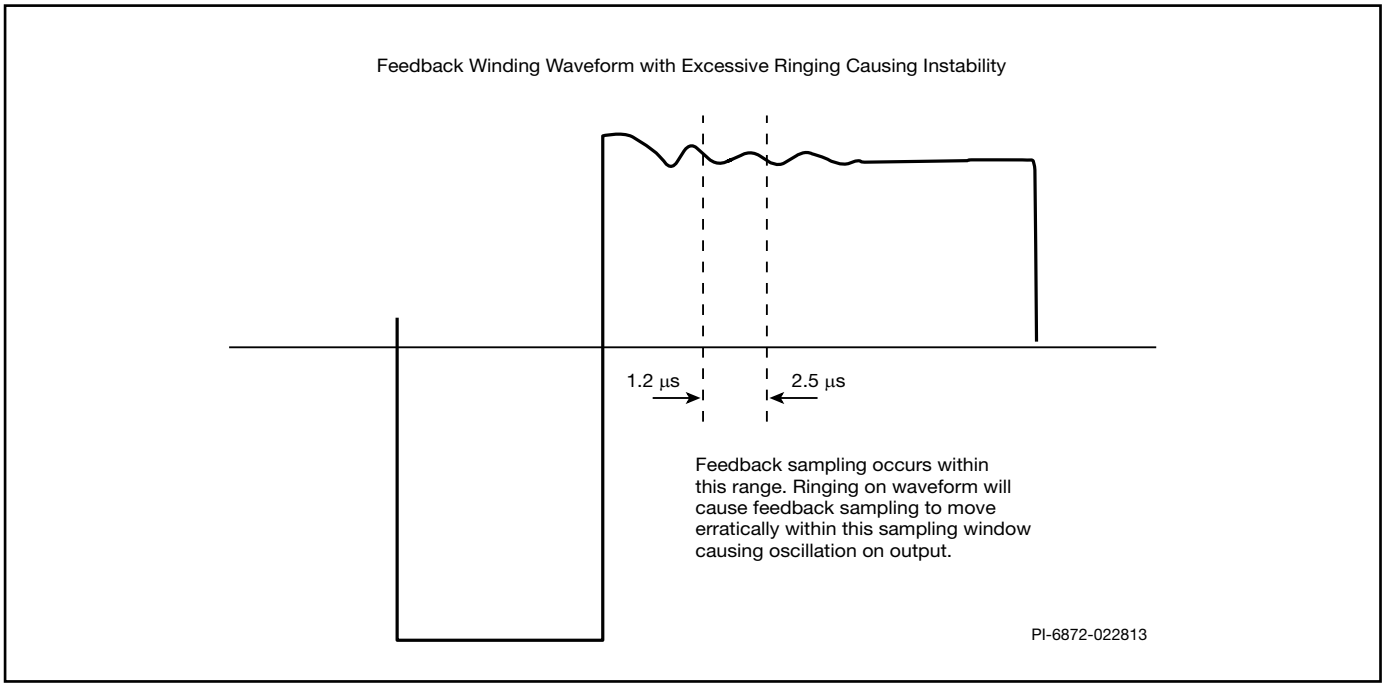


Figure 24. Ringing on Feedback (Drain) Winding May Cause Oscillation in the Output Voltage.

PIXIs will automatically optimize a transformer design to have the fewest number of turns for a given core size without violating the 3100 gauss (310 mT) maximum flux density limit. The fewest turns inherently gives the lowest leakage and inter-winding capacitance for a given winding construction.

Split primary construction is strongly recommended for designs using LinkSwitch-HP as this type construction method is well known as effective means of lowering leakage inductance (Figure 28). It also advised that the split halves of the primary be as few layers as possible. Multiple layer construction can substantially increase leakage inductance. If a particular core size forces too many layers for primary then it may be necessary to consider a core with a longer winding length or core with greater area A_E to reduce the volts/turn.

The other important consideration is the feedback winding and optimizing its coupling to the output. The feedback which often also serves as bias winding and should cover the whole allowed width of bobbin and be directly facing the first output winding layer. If the design has multiple outputs then the most critical output in terms of regulation should be the first layer on the secondary facing the feedback winding.

Feedback Winding and Regulation

As has been stated previously, it is critical that the feedback winding flyback pulse faithfully represents the output winding for best stability and regulation. This requires the transformer be as low leakage as possible and that the primary clamp circuit provides good damping.

There are a few other techniques that can be used on the winding feedback circuit itself to improve stability of feedback. One is to place a small capacitor from FEEDBACK pin to source. This capacitor works as a noise filter capacitor, it can often help light load stability issues where the leakage spike decay period is at or beyond 1 µs and can become involved with the 1.2 µs minimum load sampling time. A 10 pF or 15 pF capacitor is recommended. The allowed maximum value for this filter capacitor is 22 pF, the FEEDBACK pin voltage will need to be checked at no-load condition when using 22 pF to make sure the FEEDBACK pin voltage is flat at the sampling time of 1.2 µs. A value higher than this will start to impact light load regulation so is not advised. If the feedback winding and bias winding are the same winding, another technique to improve light load regulation is to add damping to the feedback winding itself by adding a 1 to 5 Ω series resistor.

Further investigation shows the fast recovery diode used both in primary clamping circuit and bias winding may create oscillation issue at no-load or very light load. Normally, a standard recovery diode (compared to a fast or ultrafast recovery diode) used for the bias winding rectifier diode (D_A) will help to smooth the leakage inductance ringing on the feedback winding, which will improve the stability of the power supply. Figure 25 shows the bias winding voltage and FEEDBACK pin voltage when using a fast recovery diode on bias winding, while Figure 26 shows the bias winding voltage and FEEDBACK pin voltage when using a standard diode on the bias winding.

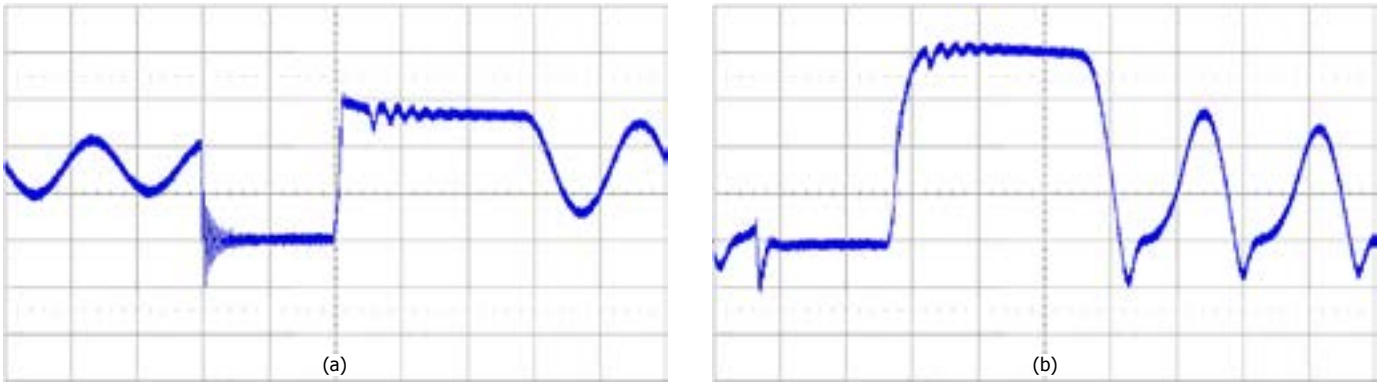


Figure 25. Bias Winding Voltage (10 V / div.) and FEEDBACK Pin Voltage (1 V / div.) with $C_{FEEDBACK\ (FILTER)}$ =10 pF, D_A = BAV21, $R_{FB(DAMP)}$ = 0 Ω.

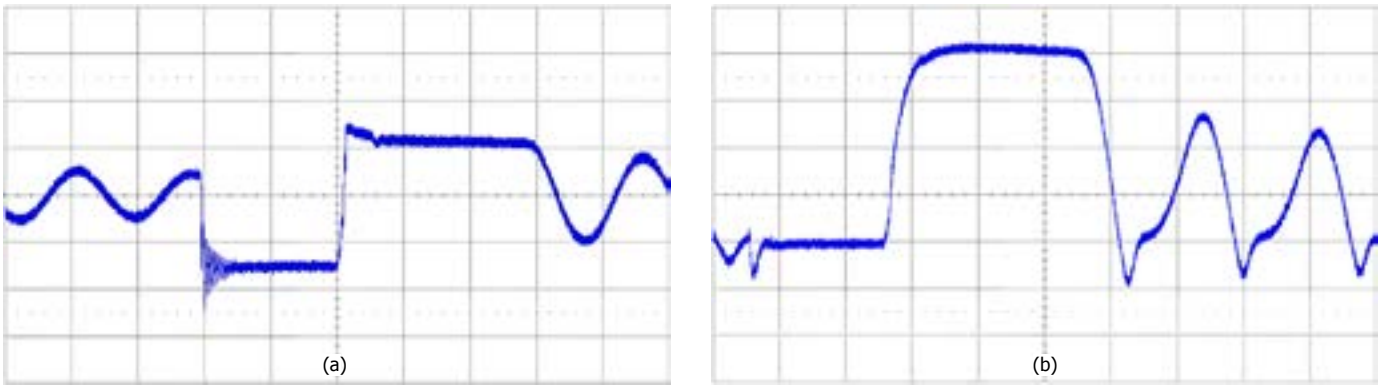


Figure 26. Bias Winding Voltage (10 V/div) and FEEDBACK Pin Voltage (1 V/div) with $C_{FEEDBACK(FILTER)}$ = 15 pF, D_A = 1N4003, $R_{FB(DAMP)}$ = 2 Ω.

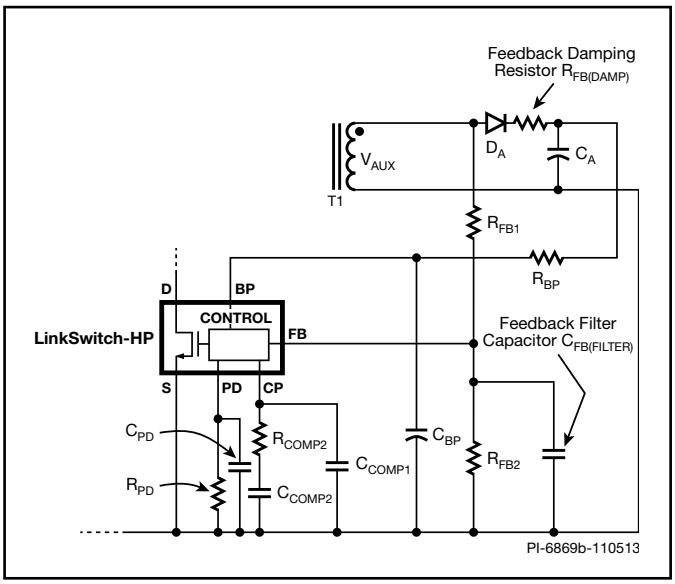


Figure 27. Recommendations for Addressing Feedback Voltage Ringing.

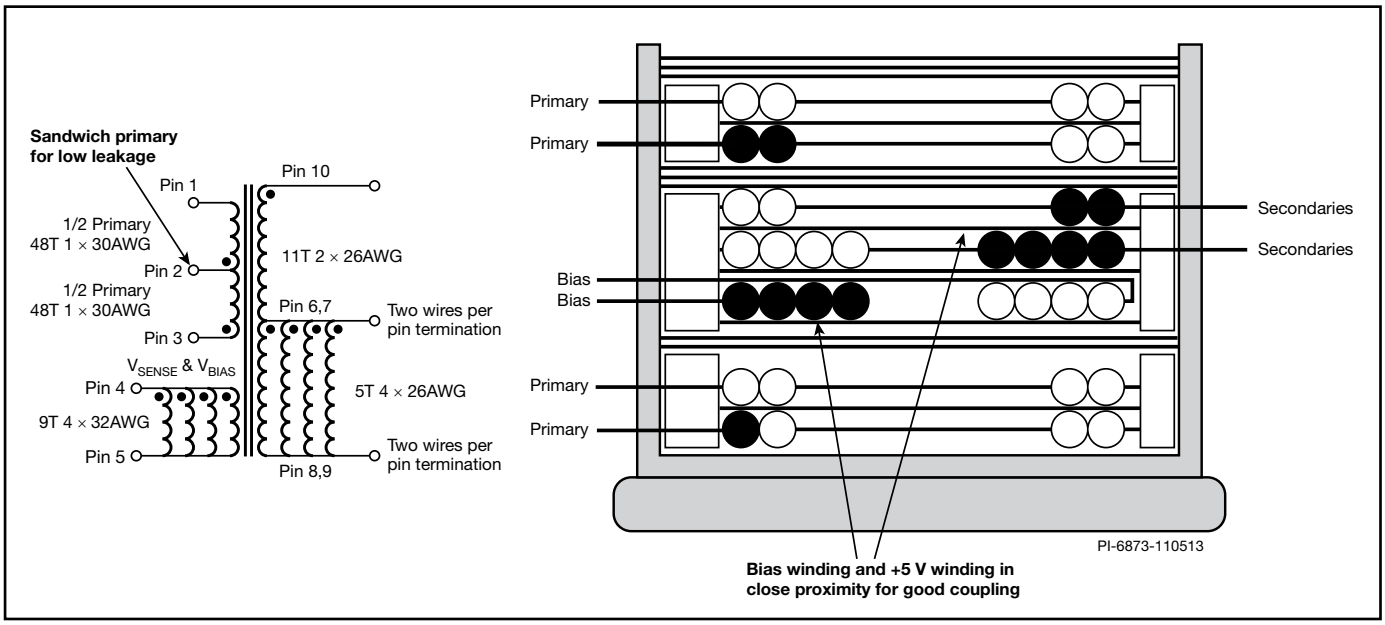


Figure 28. Recommendation for Transformer Construction: Split Primary and Bias (Feedback) Winding Next to Most Critical Secondary Point.

Load Compensation Network for Improved Load Regulation

The flyback pulse amplitude of the feedback winding will not perfectly track the output voltage over load. As the output load is increased the voltage drop increases across the output diode which reduces the actual output voltage. Increasing load will also increase the primary winding leakage spike amplitude and decay time. The leakage spike couples to the feedback winding due to close proximity to the primary winding and this will influence the amplitude of the feedback winding somewhat. Both of these parasitic elements commonly tend to cause the output to droop with load by a few percent from minimum to maximum load.

Figure 30 shows network D1, C1, R4, R3 that can be added across the winding feedback resistor divider R1 and R2 to compensate for the output droop with load. The circuit modifies the regulation set-point by adding an offset current into the FEEDBACK pin node through R3 during the flyback pulse. This offset current varies is a function of the flyback pulse duty factor ratio, D_{DCON}. D_{DCON} is the ratio of flyback conduction time (D_{CON}) to the total switching period T_{PERIOD} (Figure 29).

At light load when the operating frequency is low and the flyback pulse is short, D_{DCON} is low which causes very little voltage bias to develop across C1 (V_{C1}.) This means R3 is essentially in parallel with R1 and R4 and the regulation set-point is reduced by adding offset current into the FEEDBACK pin node.

At higher load currents when converter is operating at full switching frequency, D_{DCON} is high and V_{C1} is nearly equal to the voltage across R1 during flyback period. In this condition R3 develops very little current during flyback period and R3 has no effect on the regulation point. Therefore the regulation set point is maximum when full switching frequency has been reached.

In general, the bias on V_{C1} will change in a smooth manner between minimum and maximum load as a function of D_{DCON}. C1 is large enough to create a stable low ripple DC voltage. 100 nF is adequate for most designs. Because this compensation network works as a function of frequency the effect on regulation is restricted to the variable frequency portion of the control engine of LinkSwitch-HP.

This is typically minimum load to about 20 ~ 30% of maximum rated load. Most of the droop in regulation occurs in this load range so the performance improvement can be quite significant. Diode D1 disconnects the compensation circuit during the integrated power MOSFET on-time when the high-voltage bus voltage is indirectly sensed.

The bias developed across C1:

$$V_{C1} = (V_{FB} - 2\,V)\frac{D_{DCON}(R_3 + R_4)}{R_3 + D_{DCON}R_4}$$

So the set-point compensation current into the FEEDBACK pin node is:

$$i_{COMP} = \frac{(V_{FB} - 2\,V) - V_{C1}}{R_3}$$

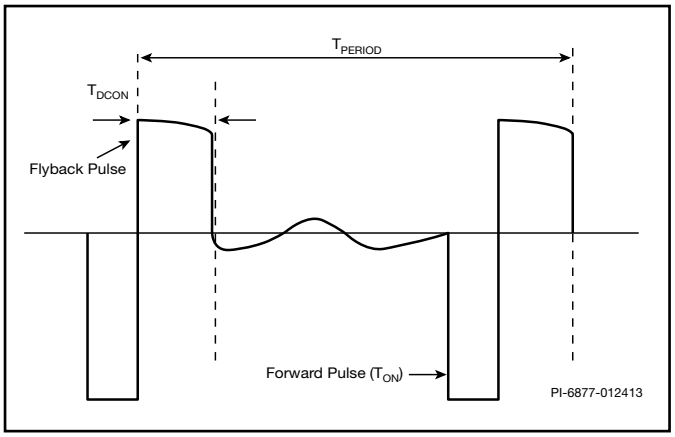


Figure 29. Feedback (Bias) Winding Voltage Waveform.

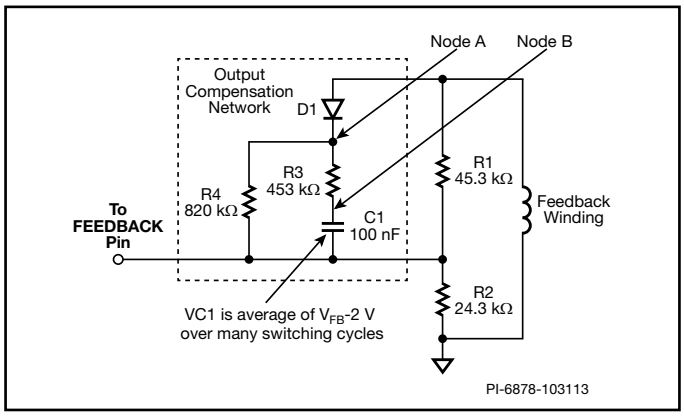


Figure 30. Optional Load Compensation Circuit.

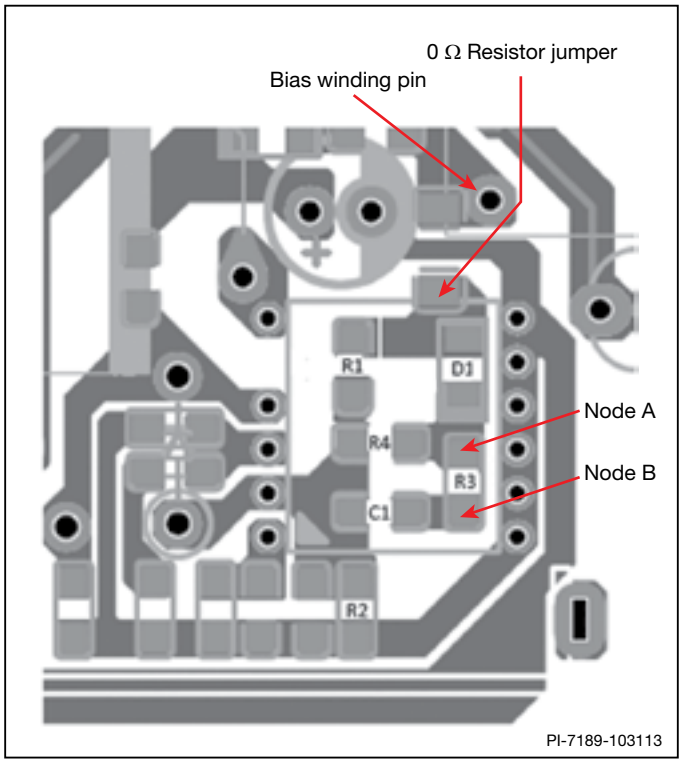


Figure 31. Layout Example of Load Compensation.

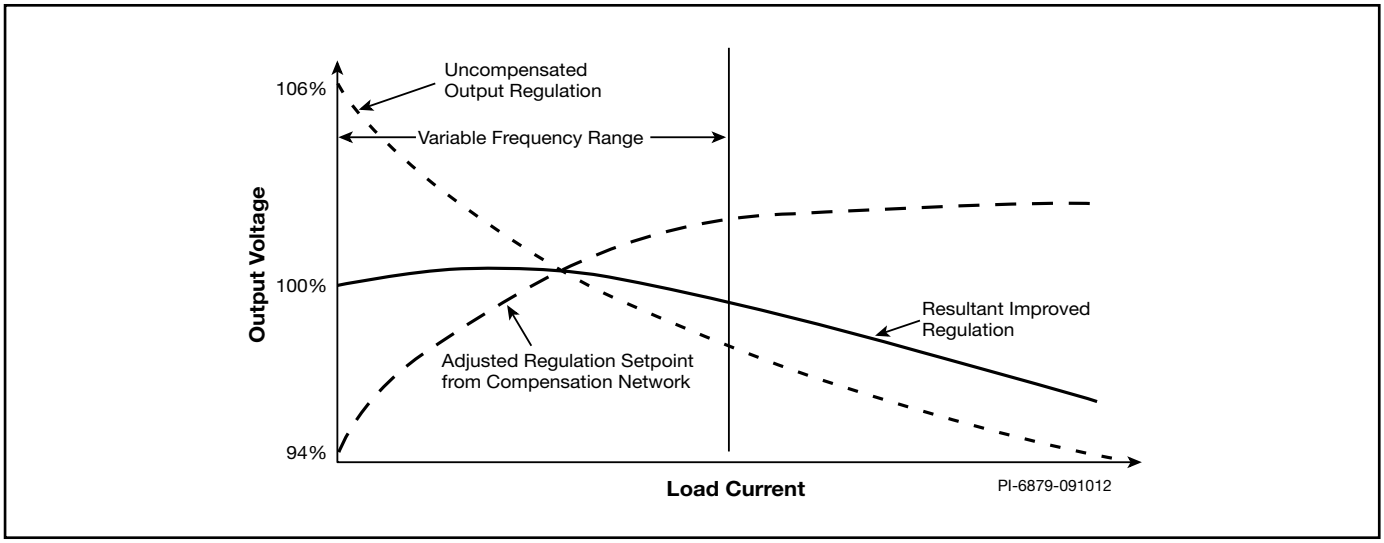


Figure 32. Effect of Compensation Circuit on Output Regulation.

Method of Selecting Optimum Values for Load Compensation Network
The first step is to design and test supply with no compensation network and plot output regulation. Measure total output voltage variation ΔV from minimum to maximum output load.

Re-center output by adjusting value of R2 such that the nominal regulation value occurs at 30% of maximum load.

Next, take the measured ΔV value from minimum to 30% load ($V_{\Delta V}$) which is needed to compute value for R3. You will also need to know the feedback winding nominal flyback amplitude which is the ratio output winding to feedback winding

$$V_{FB} = (V_O + 0.5\,V) \times \frac{N_{FB}}{N_S}$$

Compute value for load compensation resistor, R3 is:

$$R3 = \frac{R2(V_{FB} - 2V)}{V_{\Delta V}}$$

For first approximation R4 should be equal to R3 for load regulation curves where the output descends linearly with load. For output load regulation curves where the output drops at a higher rate at light load than at heavier load R4 should be higher in value than R3 with a practical limit of R4 ≤ 3 × R3. Figure 33 shows the effect of changing the ratio of R4/R3 on the linearity of the compensation as a function of D_{DCON}.

When verifying the compensation circuit at the bench, first record the load regulation with added circuit. If the output substantially rises from minimum load to 30% load then design is overcompensated. In that case compensation circuit resistor values R3 and R4 need to be increased to bring compensation more in balance. If the output droops with load in the 0 to 30% load range then R3 and R4 need to be reduced in value to add more compensation.

After optimizing for flattest possible output curve it may be necessary to re-center output by adjusting R2.

In general this method is limited to compensating a ±6% variation in regulation. Compensation beyond this range as may be required in some cable compensation specifications are beyond the capability of this circuit as there can be significant line regulation impact and also there is no active compensation in the constant frequency portion of the converter operation.

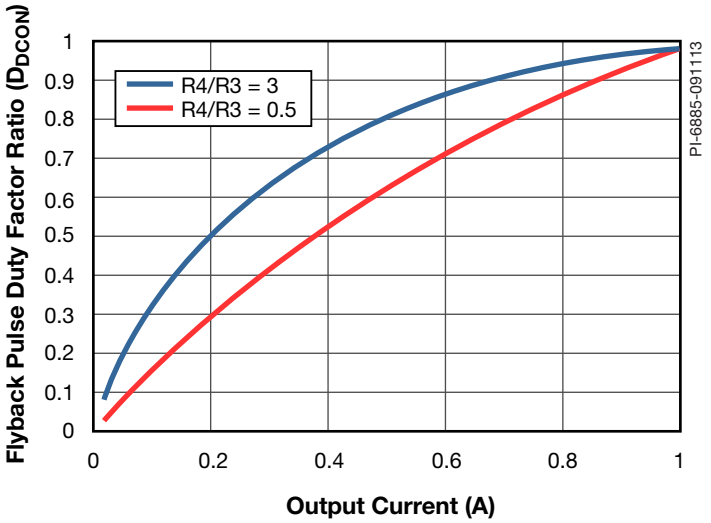


Figure 33. Adjusting Linearity of Load Compensation by Adjusting Ratio of R4/R3.

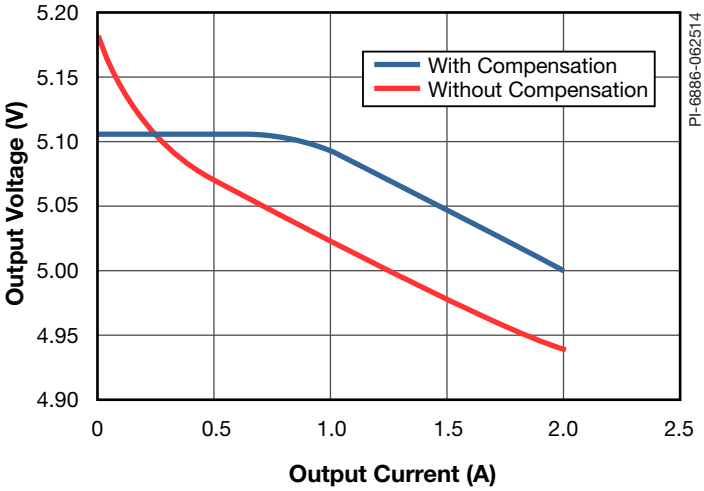


Figure 34. Example of Improved Regulation for a 5 V, 2 A Using Load Compensation Circuit.

Layout Consideration for Load Compensation Network

The node A and node B shown in Figure 30 are noise sensitive nodes, it is necessary to keep those nodes far from the bias winding node which is with high dv/dt signal. Please refer to Figure 31 for a reference design layout.

Step 6 – Select Output Rectifier Diode

For each output use the values of peak inverse voltage (V_R) and output current (I_O) provided in the design spreadsheet to select the output diodes. Table 12 shows some commonly available types.

$V_R \geq 1.25 \times PIV_S$: where PIV_S is taken from the Voltage Stress Parameters section of the spreadsheet and Transformer Secondary Design Parameters (Multiple Outputs).

$I_D \geq 2 \times I_O$: where I_D is the diode rated DC current and I_O is the average output current. Depending on the thermal rise and the duration of the peak load condition it may be necessary to increase the diode current rating once a prototype has been built. This also applies to the amount of heat sinking necessary.

Step 7 – Select Output Capacitor

Ripple Current Rating

The spreadsheet calculates the output capacitor ripple current using the average output power. Therefore the actual rating of the capacitor will depend on the peak to average power ratio of the design. In most cases this assumption will be valid as capacitor ripple rating is a thermal limitation and most peak load durations are shorter than the thermal time constant of the capacitor (<1 s). For such designs select the output capacitor(s) such that the ripple rating is greater than the calculated value, I_{RIPPLE} from the spreadsheet. However in designs with high peak to continuous (average) power and long duration peak load conditions, the capacitor rating may need to be increased based on the measured capacitor temperature rise under worst-case load and ambient temperature.

Rectified Diode	V_R (V)	I_D (A)	Package	Manufacturer
Schottky				
1N5819	40	1	Axial	General Semi
SB140	40	1	Axial	General Semi
SB160	60	1	Axial	General Semi
MBR160	60	1	Axial	IR
11DQ06	60	1.1	Axial	IR
1N5822	40	3	Axial	General Semi
SB340	40	3	Axial	General Semi
MBR340	40	3	Axial	IR
SB360	60	3	Axial	General Semi
MBR360	60	3	Axial	IR
SB540	40	5	Axial	General Semi
SB560	60	5	Axial	General Semi
MBR745	45	7.5	TO-220	General Semi IR
MBR760	60	7.5	TO-220	General Semi
MBR1045	45	10	TO-220	General Semi IR
MBR1060	60	10	TO-220	General Semi
MBR10100	100	10	TO-220	General Semi
MBR1645	45	16	TO-220	General Semi IR
MBR1660	60	16	TO-220	General Semi
MBR2045CT	45	20(2×10)	TO-220	General Semi IR
MBR2060CT		20(2×10)	TO-220	General Semi
MBR20100		20(2×10)	TO-220	General Semi IR
UFR				
UF4002	100	1	Axial	General Semi
UF4003	200	1	Axial	General Semi
MUR120	200	1	Axial	General Semi
EGP20D	200	2	Axial	General Semi
BYV27-200	200	2	Axial	General Semi IR
UF5401	100	3	Axial	General Semi
UF5402	200	3	Axial	General Semi
EGP20D	200	3	Axial	General Semi
BYV28-200	200	3.5	Axial	General Semi IR
MUR420	200	4	TO-220	General Semi
BYW29-200	200	8	TO-220	General Semi IR
BYV32-200	200	18	TO-220	General Semi IR

Table 12. List of Diodes Suitable for Use as the Output Rectifier.

In either case if a suitable individual capacitor cannot be found then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ratings.

Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This should be considered to ensure that the capacitor is not oversized.

ESR Specification

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

Voltage Rating

Select a voltage rating such that $V_{RATED} \geq 1.25 \times V_O$.

Step 8 – Select Feedback Circuit Components

The FEEDBACK pin senses the flyback pulse for each flyback cycle and stores the sampled value in an internal sample and hold stage. A transconductance feedback error amplifier compares the sampled value to an internal 2 V reference. The output response of the transconductance amplifier controls the internal modulator which controls the peak drain current and operating frequency of the converter. The output response of the error amplifier is conditioned for appropriate gain and phase margin response by an RC network from the COMPENSATION pin to ground. Typical values of compensation network which works well for the majority of applications are R_{COMP2} = 100 kΩ and C_{COMP2} = 100 nF.

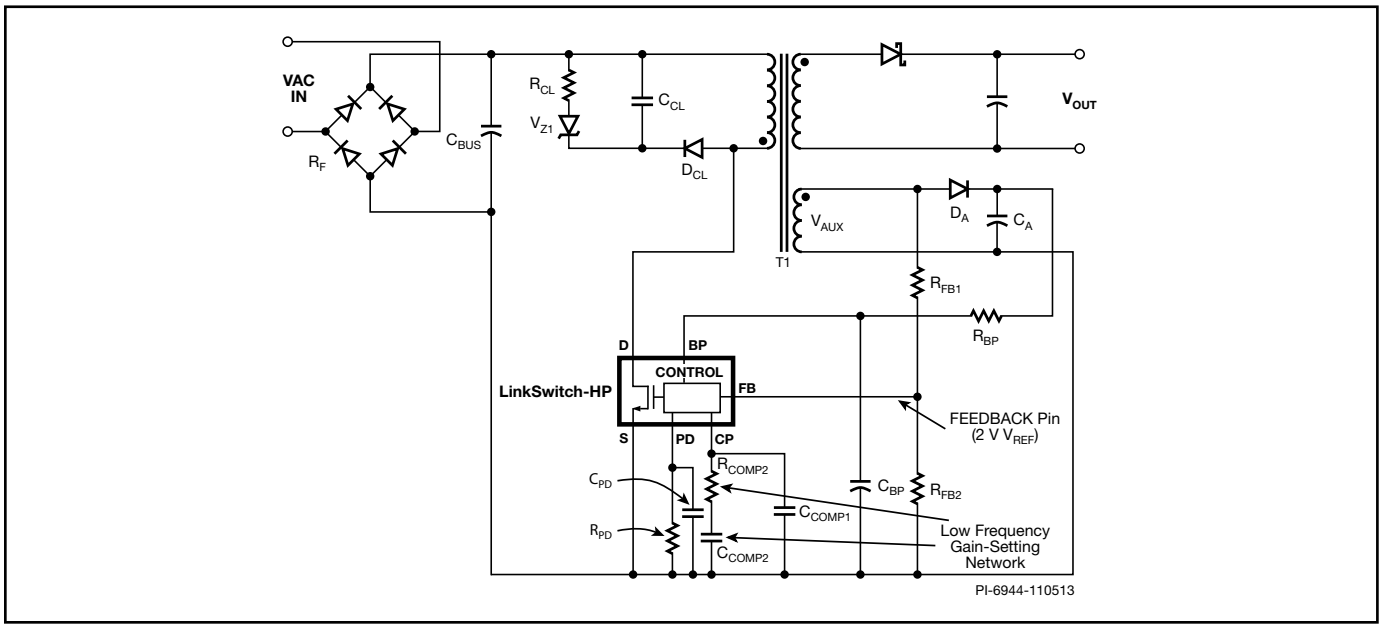


Figure 35. Loop Compensation Components.

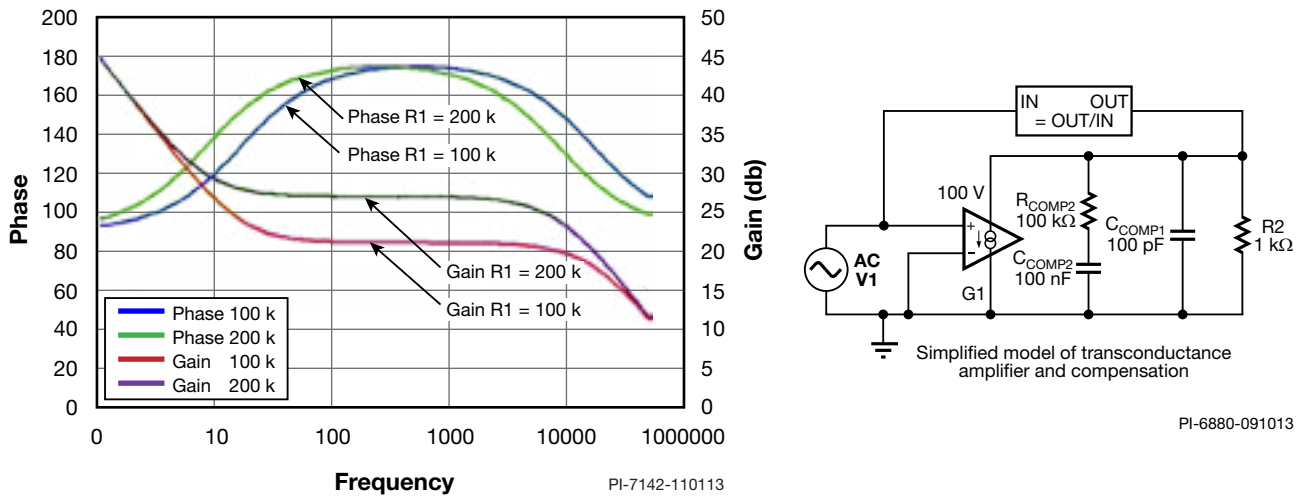


Figure 36. Internal Error Amp Model and Response.

For most designs, R_{COMP2} = 100 kΩ and C_{COMP2} = 100 nF gives very good performance. Maximum recommended value for R_{COMP2} is 200 kΩ to avoid possible noise related issues. C_{COMP} should be no less than 50 nF to avoid inadequate phase margin in low frequency region.

Compensation zero:

$$F_{COMP\_ZERO} = \frac{1}{2\pi R_{COMP2} \times C_{COMP2}}$$

Transconductance amplifier voltage gain:

$$G(dB) = 20\ Log(G_M \times R_{COMP2})$$

Transconductance amplifier voltage gain with

$$R_{COMP} = 100\ k\Omega, G(dB) = 20\ Log\left(\frac{115\ \mu A}{1\ V} \times 100\ k\Omega\right) = 21 dB$$

Loop Stability Measurement Option

Generally, using the typical values of the compensation network (R_{COMP2} = 100 kΩ, C_{COMP2} = 100 nF) will make a stable power supply design for most of the application giving good stability and fast output transient response. A loop stability measurement option does exist for getting a control loop bode plot for power supply design using LinkSwitch-HP.

As mentioned in former sections, unlike SSR (Secondary-Side Regulated) power supplies, the LinkSwitch-HP based PSR (Primary-Side Regulated) power supply controller samples the voltage of the feedback winding for each flyback cycle and stores the sampled value in an internal sample and hold stage in order to determine the output voltage. This sampling technique makes it difficult to use the conventional technique of signal injection for stability assessment by breaking the feedback loop.

A loop test box has been created that samples the winding voltage at a fixed interval of time following the turn-off of the MOSFET and provides a node suitable for conventional signal injection method. Figure 37 shows the function blocks of this loop test box, it is actually an external sample and hold circuit to convert an AC feedback winding voltage to a stable DC voltage reflecting the feedback winding voltage during flyback period.

By using this external sample and hold circuit, a conventional signal injection method can be applied to obtain the bode plot for the power supply, please refer to Figure 38. Figure 39 is a picture of the loop test box.

If you need a gain phase plot measurement for the power supply using LinkSwitch-HP, please contact the local field application engineer for support.

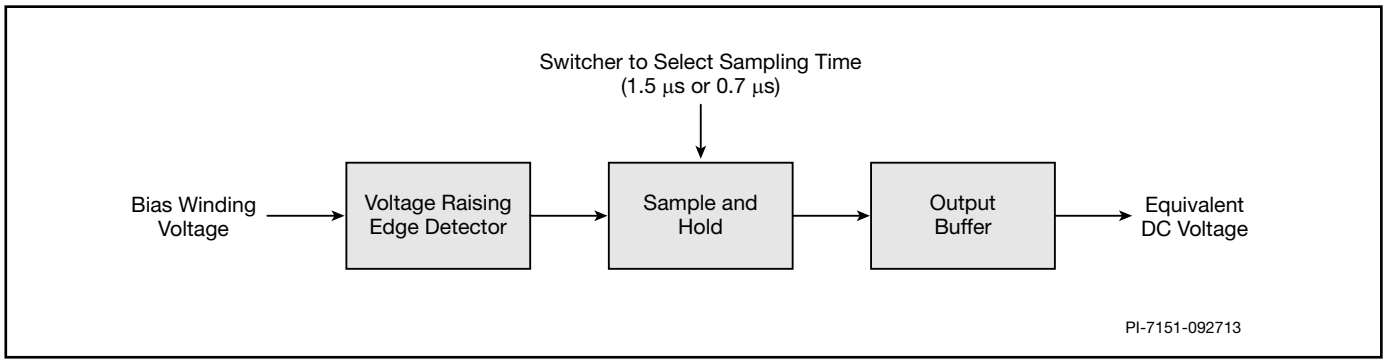


Figure 37. LinkSwitch-HP Loop Test Box Function Blocks.

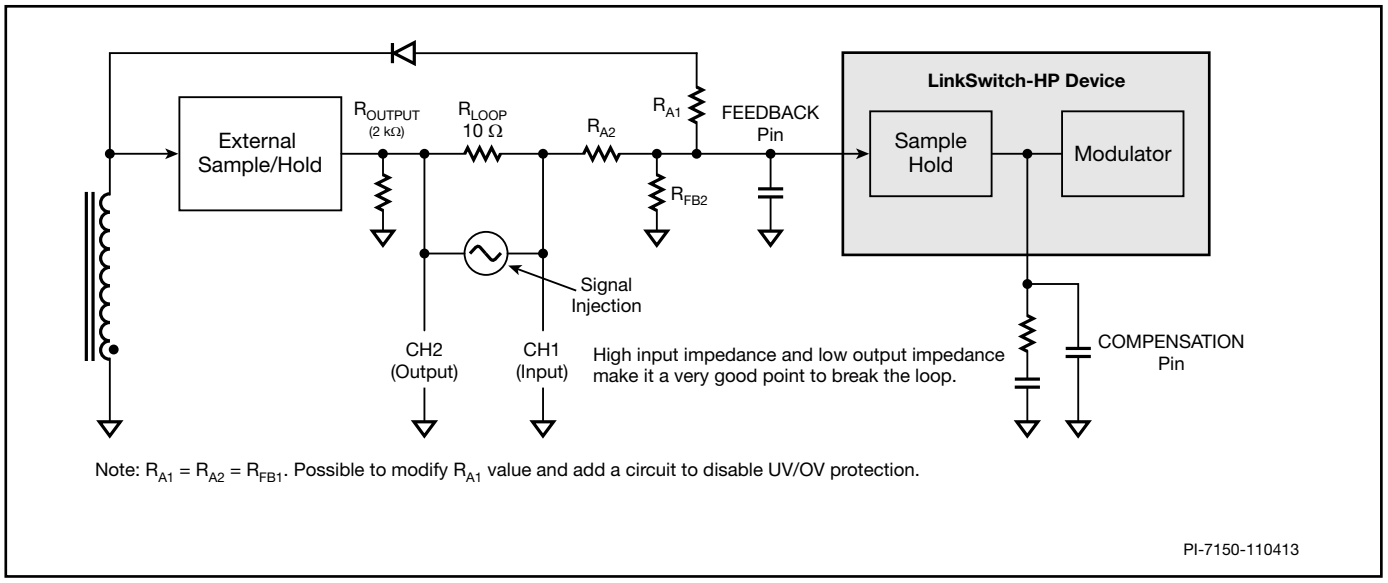


Figure 38. Loop Injection Node with Loop Test Box.

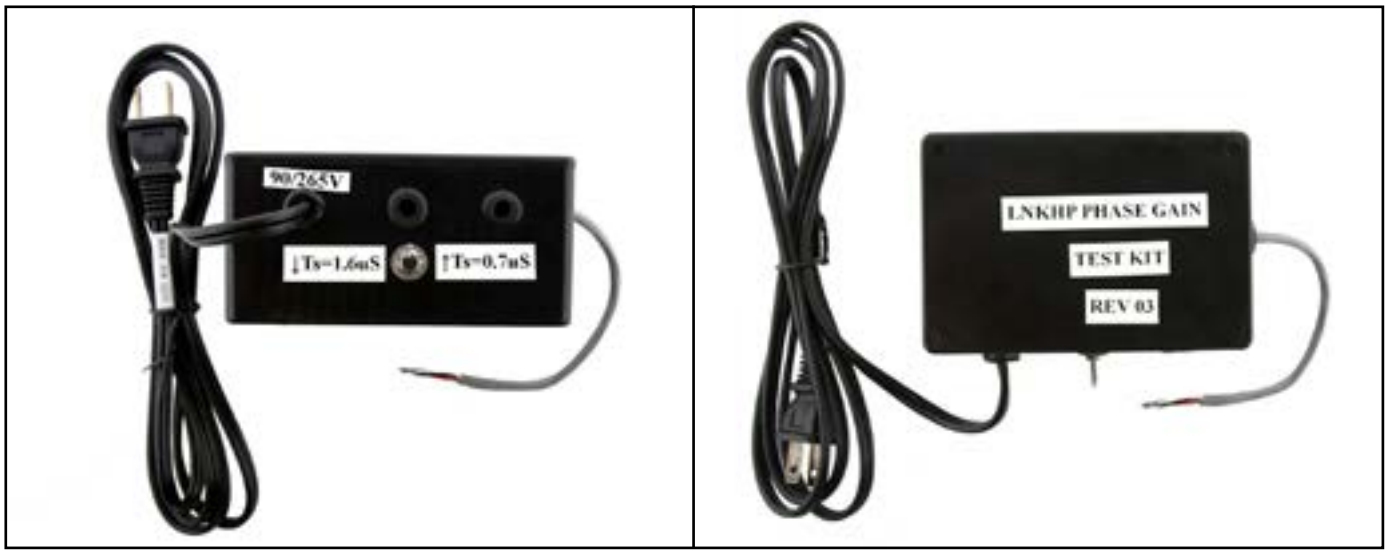


Figure 39. LinkSwitch-HP Loop Test Box.

Circuit Board Layout

LinkSwitch-HP is a highly integrated power supply solution that integrates on a single die, both, the controller and the high-voltage power MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply.

When designing a board for the LinkSwitch-HP based power supply, it is important to follow the following guidelines:

Primary-Side Connections

- Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-HP SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.
- If a heat sink is used, the mounting copper pad on PCB that receives should be electrically isolated (do not ground).
- All SOURCE pin referenced components connected to a single SOURCE pin location (star point grounding).
- Wrap the ground trace around sensitive components to act as a Farady shield. See Figure 40.
- The COMPENSATION pin 100 pF noise filter capacitor and the BYPASS pin capacitor should have the shortest possible traces to SOURCE pin.
- Keep high-voltage components such as drain switching nodes and primary clamp components as tight and far away from the sensitive pins (CP, FB, PD pins) of LinkSwitch-HP.

Y Capacitor

The preferred Y capacitor connection is close to the secondary output return pin(s) and the positive primary DC input pin of the transformer. If the Y capacitor is connected between primary and secondary RTN then the primary connection should be made via a dedicated trace from the Y capacitor to the negative input capacitor terminal. This ensures that surge current across the isolation barrier are routed away from traces connected to LinkSwitch-HP.

Secondary

To minimize leakage inductance and EMI, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

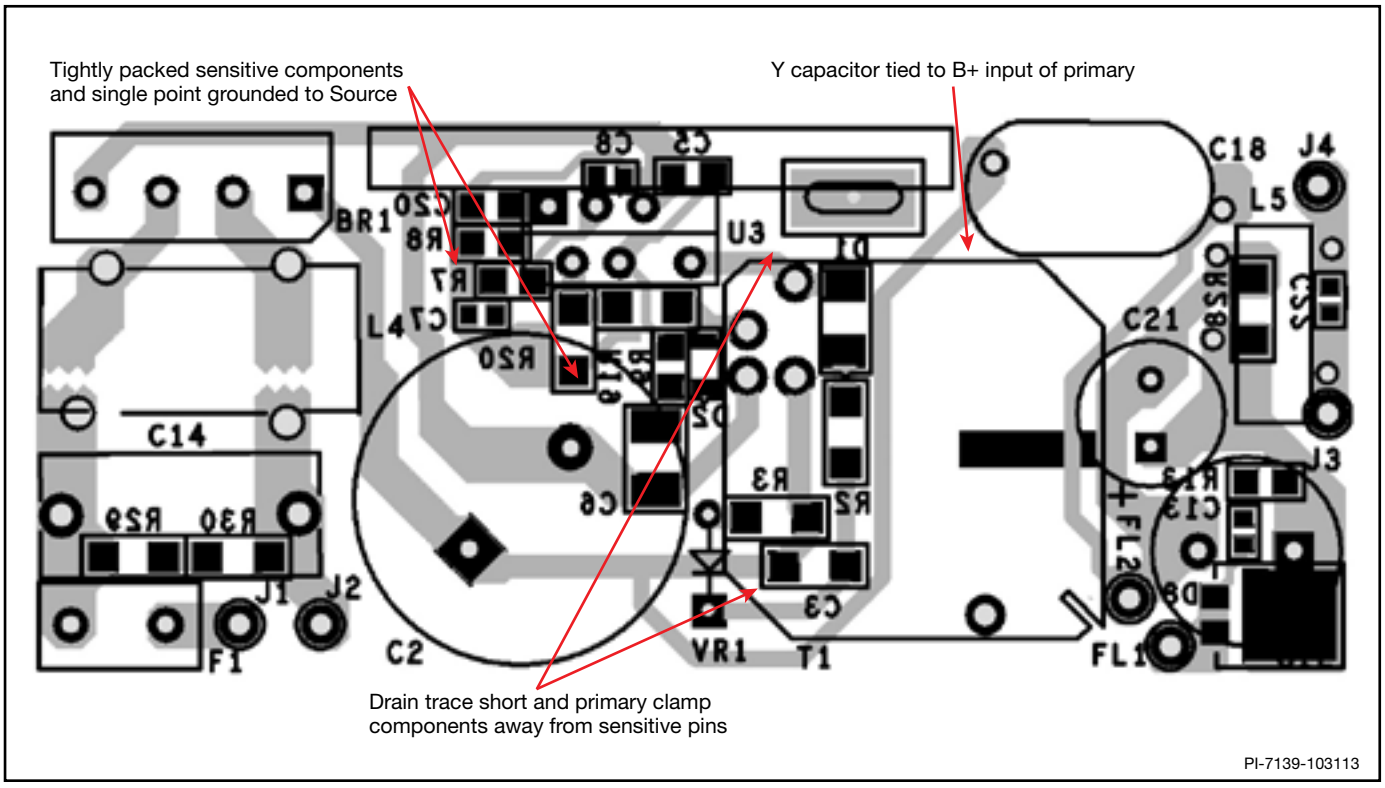


Figure 40. Layout Example of a 30 W Adapter Using eSIP Package, see Figure 47 for the Schematic.

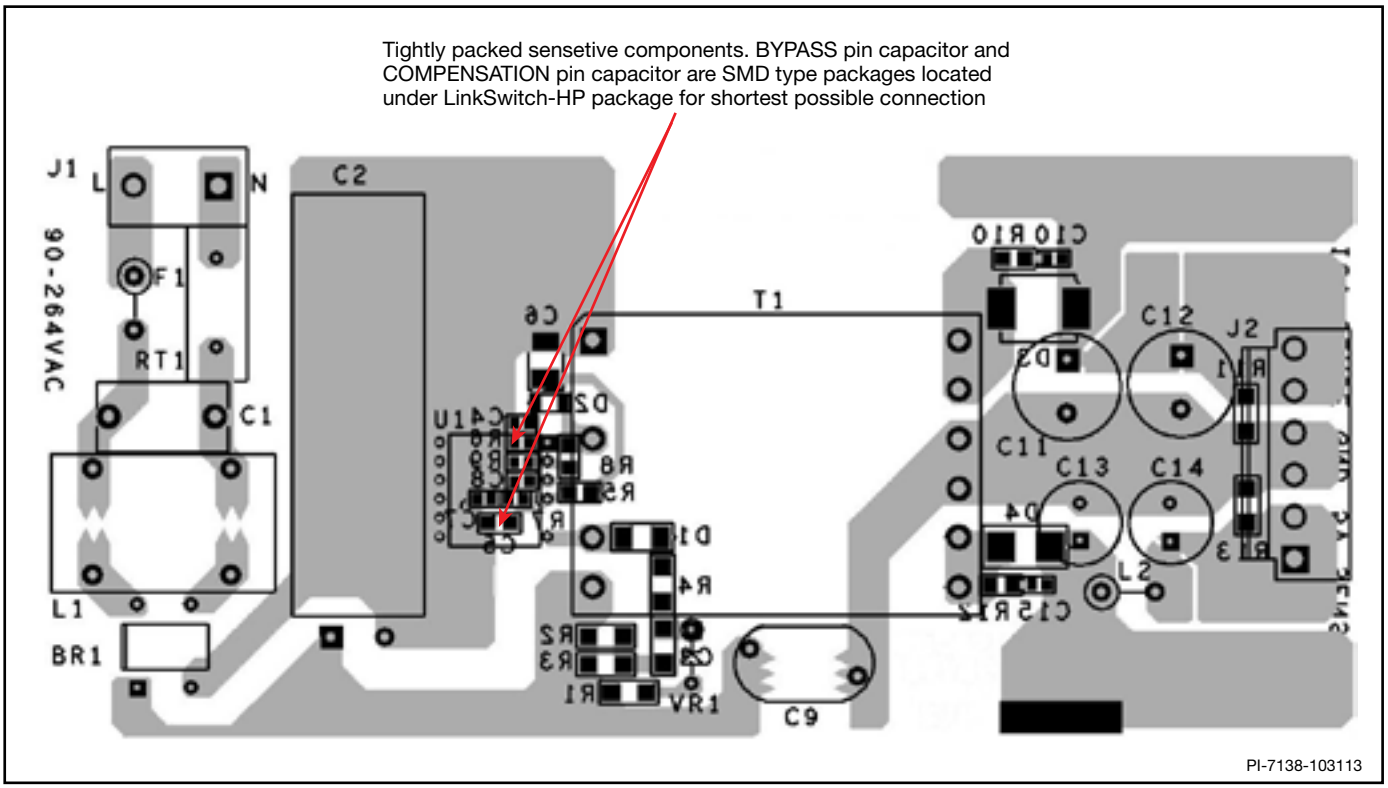


Figure 41. Layout Example of a Dual Output 17 W Open Frame Design Using eDIP Package, see Figure 48 for Schematic.

External Shutdown and Reset Options

The PROGRAM pin can be used for shutting the converter off or resetting the device after a latching event such as an OVP or over temperature fault (OTP). By externally pulling the PROGRAM pin above 3.5 V the LinkSwitch-HP will shut off and also reset any active fault latch. When the external pull-up is removed the converter begins a start-up sequence after the PROGRAM pin voltage has discharged to 0.55 V.

If during external turn-off, it is desired to retain fault latch condition, then circuit in Figure 42b can be used to turn-off converter without resetting fault latches.

The circuit in Figure 43 can be modified to serve as a fast AC reset function by adding an AC input sampling stage. When sufficient AC is present the PNP transistor is off and the inhibit is thereby removed.

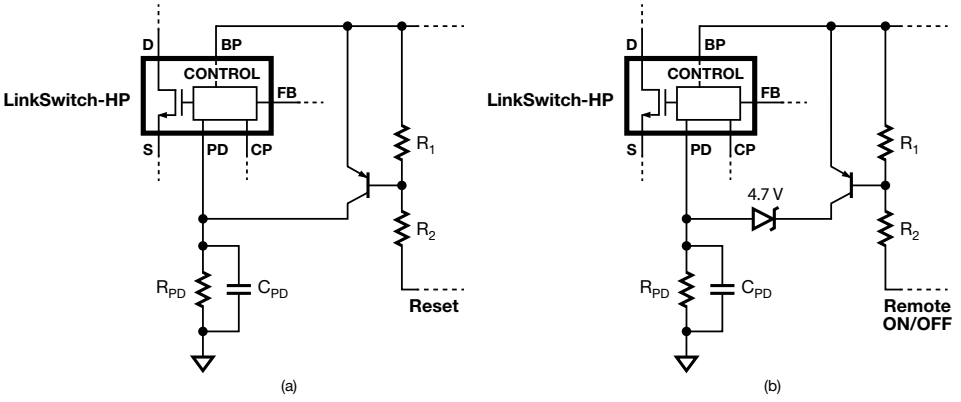


Figure 42. External Shutdown and Reset Options, (a) Reset, (b) Remote ON/OFF.

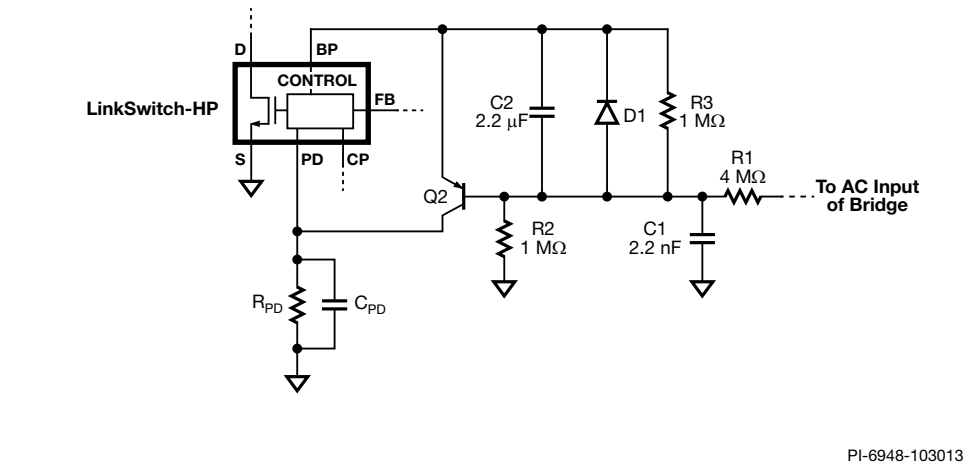


Figure 43. Fast AC Reset Configuration.

External Latch Function Option

By injecting 6.5 mA or more into the BYPASS pin the device will be commanded to latch off. Recycling AC or using reset circuit as shown in Figure 42a will reset this fault latch. The circuit shown below is typical implementation where Q1 emitter is referenced to the bias capacitor and pulling the base of Q1 low will trigger BYPASS pin latch function.

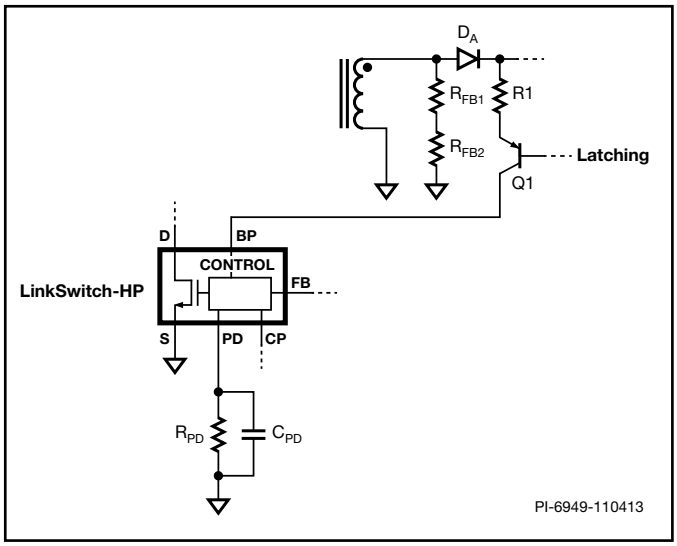


Figure 44. External Latching Shutdown Configuration.

Constant Output Power Option

To be able to droop the output voltage in case of the overload at power supply output (instead of auto-restart for OCP protection), the following circuit can be used.

The PROGRAM pin voltage will be pulled down to prevent auto- restart during the output overload situation. The output power will remain constant, while the output voltage drops with the increase of the output current. R1 and R2 resistors value will depend on the bias voltage; they can be adjusted to change the auto-restart point. Diode D1 is applied to avoid the reverse of biasing the Q1.

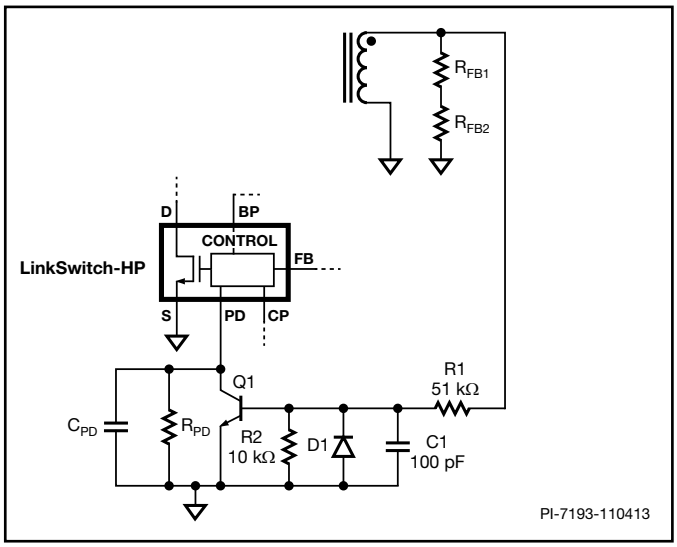


Figure 45. External Circuits for Constant Output Power Configuration.

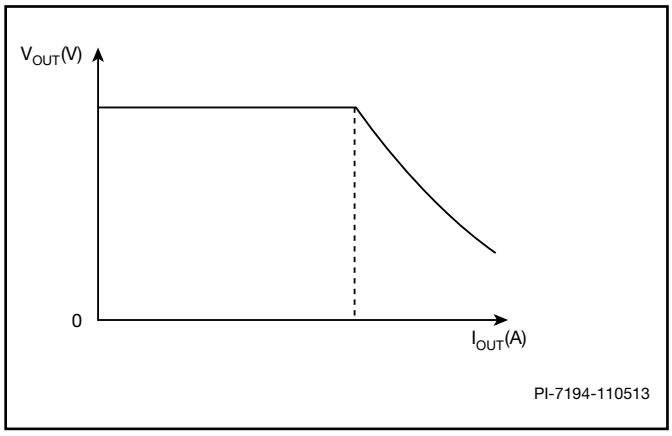


Figure 46. Power Supply Output Characteristics.

Quick Design Checklist

As with any power supply design, all LinkSwitch-HP designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 675 V for the LNK677X series and 600 V for the LNK6X6X series at highest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just before the power supply goes into auto-restart (loss of regulation).
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch-HP has a leading edge blanking time of 220 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope (see data sheet curve) for the drain current waveform at the end of the 220 ns blanking period.
3. Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for LinkSwitch-HP, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-HP, as specified in the data sheet. A maximum exposed pad temperature of 110 °C is recommended to allow for these variations. Alternatively the design margin can accounted for by connecting an external resistance in series with the DRAIN pin and attached to the same heat sink, having a resistance value that is equal to the difference between the measured $R_{DS(ON)}$ of the device under test and the worst-case maximum specification.

Appendix A – Application Examples

A High Efficiency, 30 W Universal Input Adapter

The circuit shown in Figure 47 delivers 30 W (12 V at 2.5 A) at 86% efficiency using a LNK6676E. It is a compact design due to 132 kHz operation allowing the use of an RM8 size transformer core and bobbin.

Since LinkSwitch-HP dramatically reduces the number of required external components including the total elimination of secondary sensing and feedback components, the very tight and compact layout challenges of small adapters are much easier to design.

Very low no-load input power is essential to meet today's efficiency requirement. This design is has less than 30 mW no-load input power as measured at 230 VAC.

All the standard protection functions are included in this design:

- Input and output OVP
- Input and output UV
- Tight overpower over the entire input voltage range
- Soft-start
- Short-circuit protection

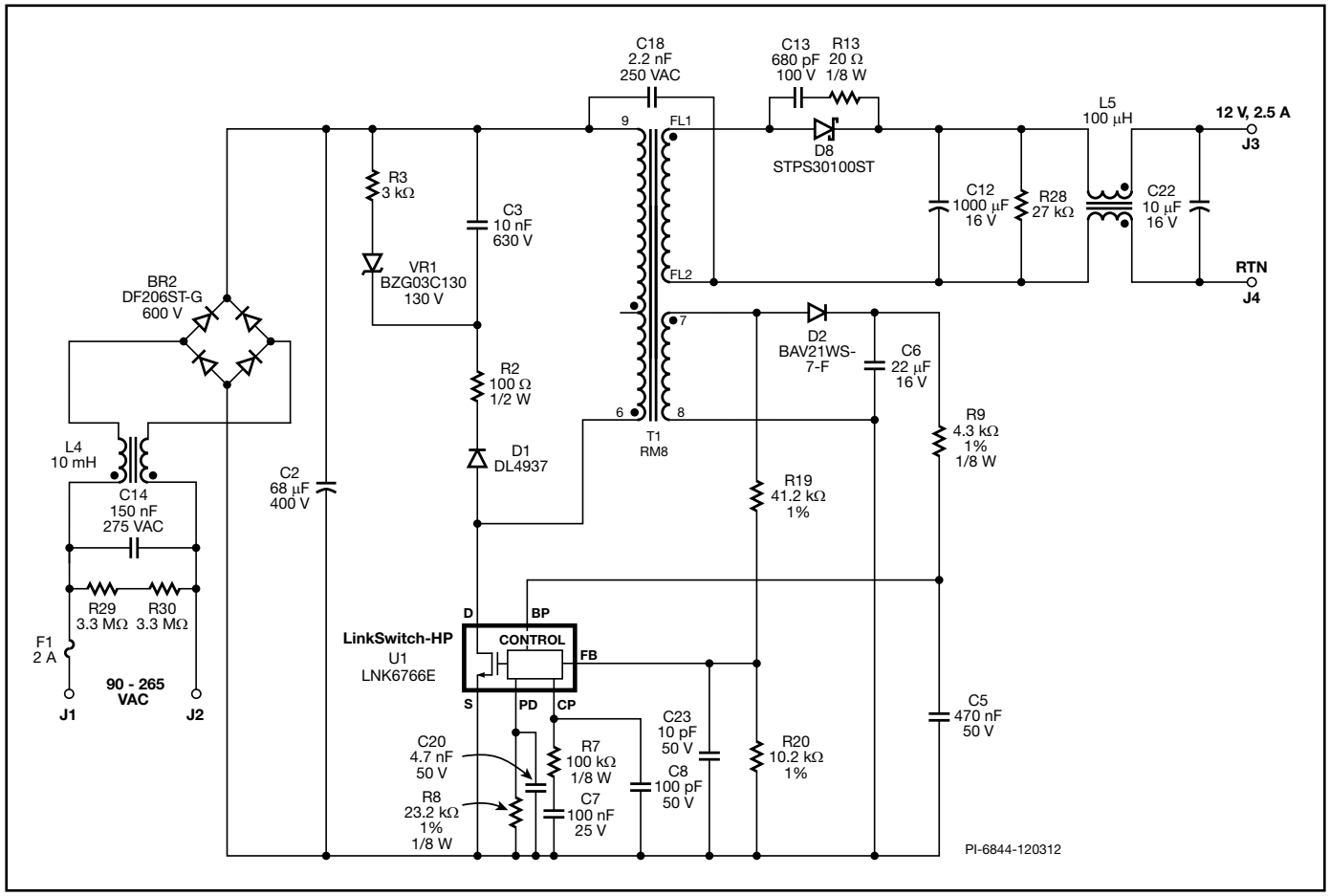


Figure 47. 30 W Universal Input Adapter.

17 W Dual Output LCD Monitor Power Supply

Figure 48 is an example of a LinkSwitch-HP used for a dual output supply with +5 V and + 18 V outputs. The +5 V output meets ±5% regulation while the 18 V output is within the limits of 16.2 V min and 26 V max over the entire line and load range. An eSOP package is used here which requires no heat sink for this design. The heat sinking is provided by the PCB copper area around the SOURCE pin connection. The transient response is excellent which allows this design to stay within transient load limits as defined by the loading conditions shown in Figure 49. There is less than 100 mW input power in standby mode which is defined as 50 mW loading of the +5 V output.

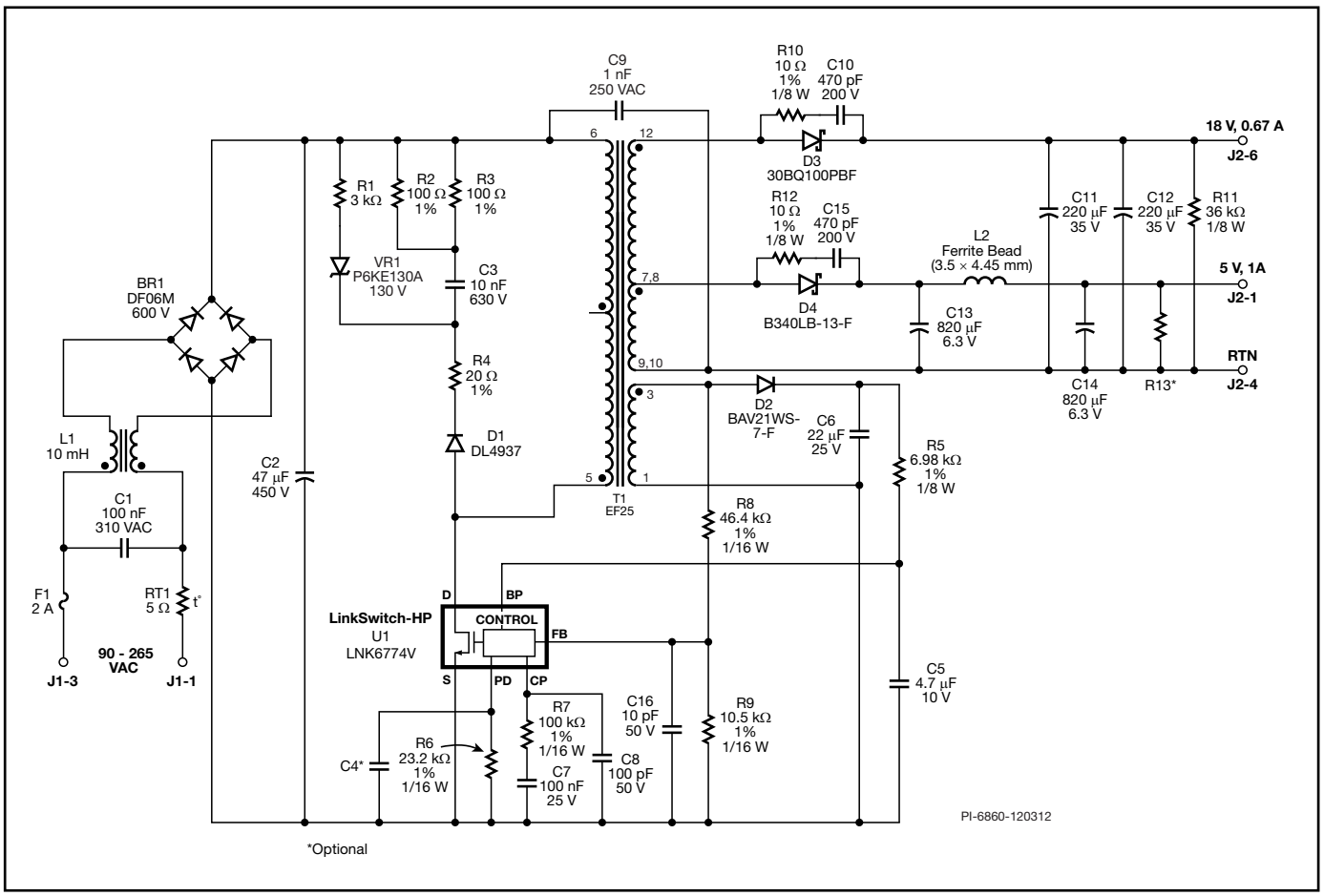


Figure 48. 17 W Dual Output Supply.

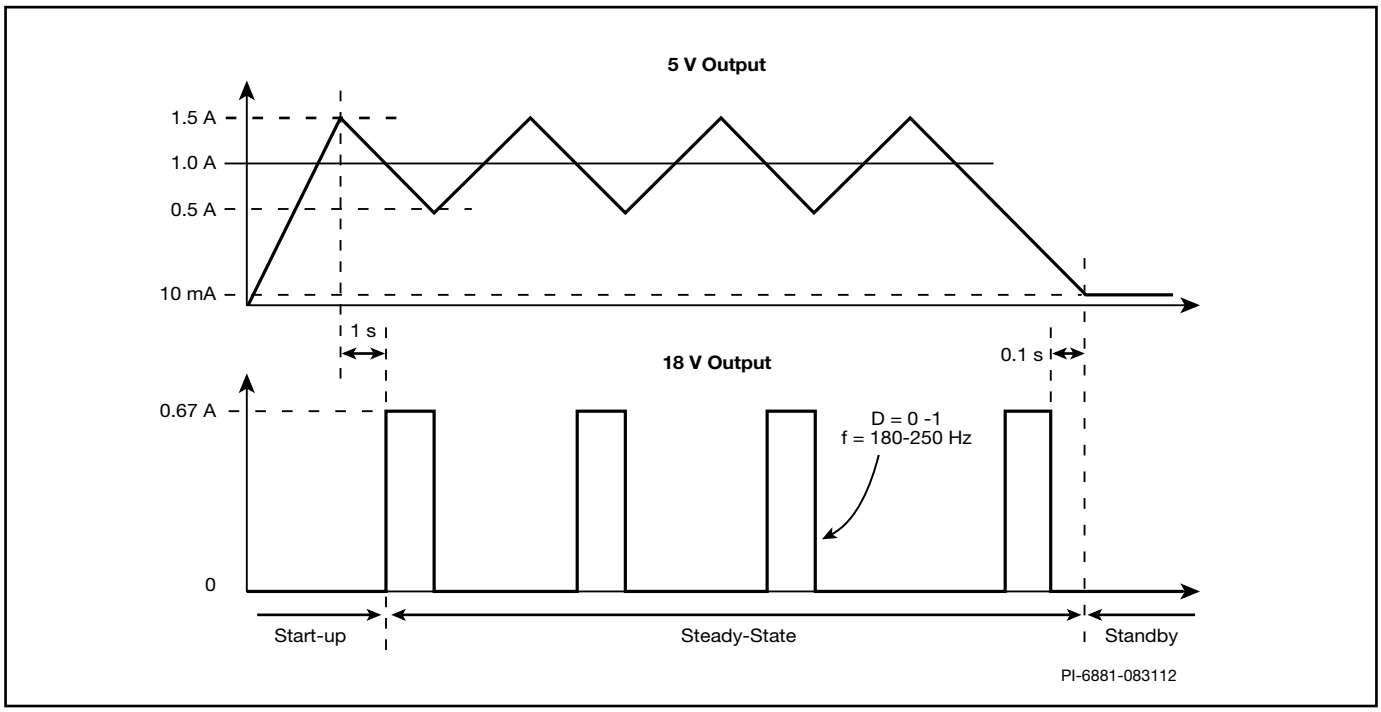


Figure 49. LCD Monitor Loading Profile.

Appendix B – Multiple Output Flyback Power Supply Design

The only difference between a multiple output flyback power supply and a single output flyback power supply of the same total output power is in the secondary-side design. Instead of delivering all power to one output as in the single output case, a multiple output flyback distributes its output power among several outputs. Therefore, the design procedure for the primary-side stays the same, while that for the secondary-side demands further considerations.

Design with Lumped Output Power

One simple way of doing multiple output flyback design is described in detail in AN-22, "Designing Multiple OutputFlyback Power Supplies with TOPSwitch". The design method starts with a single output equivalent by lumping output power of all outputs to one main output. Secondary peak current I_{SP} and RMS current I_{SRMS} are derived. Output average current I_O corresponding to the lumped power is also calculated.

Assumption for Simplification

The current waveforms in the individual output windings are determined by the impedance in each circuit, which is a function of leakage inductance, rectifier characteristics, capacitor value and most importantly, output load. Although this current waveform may not be exactly the same from output to output, it is reasonable to assume that, to the first order, all output currents have the same shape as for the single output equivalent of lumped power.

Output RMS Current vs Average Current

The output average current is always equal to the DC load current, while the RMS value is determined by current wave shape. Since the current wave shapes are assumed to be the same for all outputs, their ratio of RMS to average currents must also be identical. Therefore, with the output average current known, the RMS current for each output winding can be calculated as

$$I_{SRMS}(n) = I_O(n) \times \frac{I_{SRMS}}{I_O}$$

where $I_{SRMS}(n)$ and $I_O(n)$ are the secondary RMS current and output average current of the nth output and I_{SRMS} and I_O are the secondary RMS current and output average current for the lumped single output equivalent design.

Customization of Secondary Designs for Each Output

The turns for each secondary winding are calculated based on the respective output voltage $V_O(n)$:

$$N_S(n) = N_S \times \frac{V_O(n) + V_D(n)}{V + V_D}$$

Output rectifier maximum inverse voltage is

$$PIV_S(n) = V_{MAX} \times \frac{N_S(n)}{N_P} + V_O(n)$$

With output RMS current $I_{SRMS}(n)$, secondary number of turns $N_S(n)$ and output rectifier maximum inverse voltage $P_{IVS}(n)$ known, the secondary-side design for each output can now be carried out exactly the same way as for the single output design.

Secondary Winding Wire Size

Assumes a CMA of 200 when calculating secondary winding wire diameters. This gives the minimum wire sizes required for the RMS currents of each output using separate windings. Designers may wish to use larger size wire for better thermal performance. Other considerations such as skin effect and bobbin coverage may need to be considered too.

Feedback Winding and Regulation

With multi output power supply design, when output 1 with higher output voltage works at no-load or lighter load and output 2 with lower output voltage works at medium load, the current of output 1 winding will drop to zero before output 2 winding does due to its lighter load and higher voltage at the output [Reference 1]. After output 1 winding current reaches to zero, output 2 winding current starts to decrease. A very slight drop on the bias voltage will be caused at this point when output 1 winding current reaches to zero. The sampling delay time of the FEEDBACK pin varies linearly from 1.2 μs to 2.5 μs, minimum to maximum load. If the sampling time for feedback winding voltage is right on this point at certain load point level, then it may cause instability of the power supply. This happens when one of the outputs has no-load or lighter load while the other output is at light load or medium load.

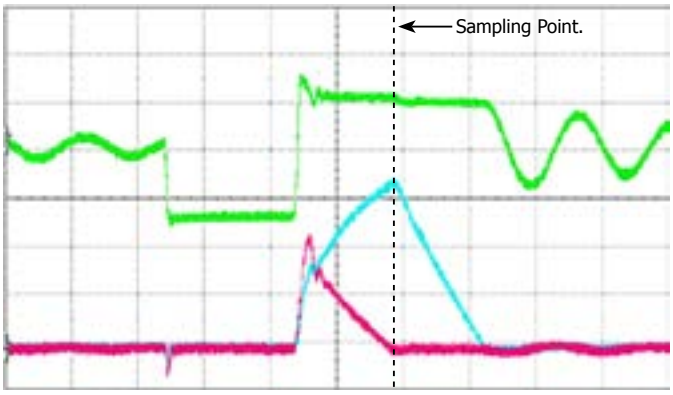


Figure 50. V_{OUT1} with Light Load, V_{OUT2} with Medium Load.
Green: Bias Winding Voltage 20 V / div., 1 μs / div.
Blue: Output 2 Diode Current 1 A / div., 1 μs / div.
Red: Output 1 Diode Current 1 A / div., 1 μs / div.

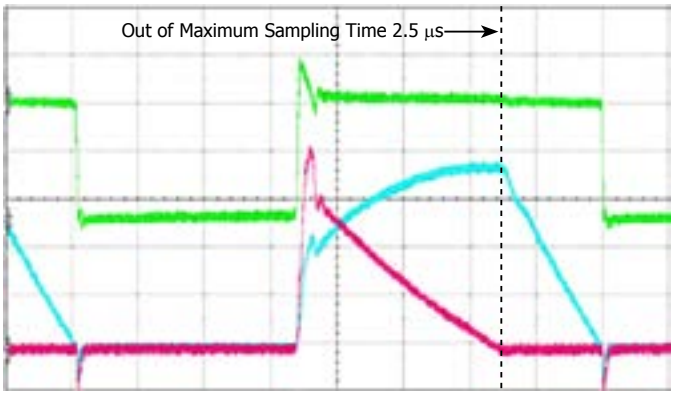


Figure 51. V_{OUT1} with Medium Load, V_{OUT2} with Heavy Load.
Green: Bias Winding Voltage 20 V / div., 1 µs / div.
Blue: Output 2 Diode Current 1 A / div., 1 µs / div.
Red: Output 1 Diode Current 1 A / div., 1 µs / div.

Generally by using all of the techniques that are mentioned in the former sections to improve the stability of feedback, even with multi output design, the instability will be barely seen. However, slightly oscillation may exist at certain loads for some specific power supply design; a bigger capacitor value of 330 pF with maximum 470 pF may be required for the noise decoupling capacitor C_{COMP1}. Decreasing the control loop gain by decreasing the compensation network R_{COMP2} value will also improve the stability, but any value less than 51 kΩ is not advised. It is important to mention that the control loop margin will need to be always verified by using load step response, output impedance check or bode plot analysis whenever any changes are made to the loop compensation circuit.

Reference

1. Cross Regulation in Flyback Converters: ANALYTIC MODEL - Chuanwen Ji and Keyue. M. Smedley, Dept. of Electrical & Computer Engineering University of California, Irvine, CA 92697, USA.

Notes

Revision	Notes	Date
A	Initial Release.	06/14
B	Updated with new PI style.	08/17

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