Design Example Report

Title	***>91% Efficient 150 W, Two Channel, Power Factor Corrected, SSL LED Driver Using LinkSwitch™-PH LNK420EG***
Specification	184 VAC – 277 VAC Input; 30 V – 36 V, 4.2 A_{TOTAL} (2.1 A per Channel) Output
Application	Street Light LED Driver
Author	Applications Engineering Department
Document Number	DER-291
Date	October 19, 2012
Revision	2.0

Summary and Features

- 150 W two-channel LED driver; 75 W each channel
- Dramatically simplifies off-line, power factor corrected, LED driver design
  - Single-stage, power factor corrected, isolated LED driver
  - Compact with extremely low component count
  - High PF >0.95 across line and load
  - High efficiency >91% across line and load
  - Low THD, <22% across line and load
  - IEC61000-3-2 CLASS C compliant with excellent margin
  - Meets IEC 61000-4-5 ring wave >2.5 kV and differential surge >2 kV withstand
  - Eliminates all control loop compensation
  - No output current sensing required
  - Frequency jittering greatly reduces EMI filter costs
  - Integrated protection and reliability features
    - Latching output open load (OVP) circuit
    - Output short-circuit protected with auto-recovery
    - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
    - No damage during brown-out or brown-in conditions

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Table of Contents

1 Introduction ... 5
2 Design Key Points ... 7
3 Power Supply Specification ... 8
4 Schematic ... 9
6 Description ... 10
6.1 Input Filtering ... 10
6.2 LinkSwitch-PH Primary ... 10
6.3 Bias Supply and Output Overvoltage Sensing ... 10
6.4 Output Feedback ... 11
6.5 Output Rectification and Filtering ... 11
7 PCB Layout ... 12
8 Bill of Materials ... 13
8.1 Electrical BOM ... 13
9 Heat Sink Assemblies ... 15
9.1 Output Diode Heat Sink ... 15
9.1.1 Output Diode Heat Sink Drawing ... 15
9.1.2 Output Diode Heat Sink Fabrication Drawing ... 16
9.1.3 Output Diode and Heat Sink Assembly Drawing ... 17
9.2 eSIP Heat Sink ... 18
9.2.1 eSIP Heat Sink Drawing ... 18
9.2.2 eSIP Heat Sink Fabrication Drawing ... 19
9.2.3 eSIP and Heat Sink Assembly Drawing ... 20
10 Transformer Specification ... 21
10.1 Electrical Diagram ... 21
10.2 Electrical Specifications ... 21
10.3 Materials ... 21
10.4 Transformer Build Diagram ... 22
10.5 Transformer Construction ... 22
10.6 Transformer Core Wrapping Process ... 23
12 Transformer Design Spreadsheet ... 25
13 Performance Data ... 28
13.1 Efficiency ... 28
13.2 Line and Load Regulation ... 29
13.3 Power Factor ... 30
13.4 A-THD ... 31
13.5 Harmonic Currents ... 32
13.5.1 30 V LED Load ... 32
13.5.2 33 V LED Load ... 33
13.5.3 36 V LED Load ... 34
13.6 Test Data ... 35
13.6.1 Test Data, 30 V LED Load ... 35
13.6.2 Test Data, 33 V LED Load ... 35
13.6.3 Test Data, 36 V LED Load ... 35
13.6.4 277 VAC 50 Hz., 30 V LED Load Harmonics Data ... 36

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13.6.5 230 VAC 50 Hz., 33 V LED Load Harmonics Data 37
13.6.6 230 VAC 50 Hz, 36 V LED Load Harmonics Data 38
14 Waveforms 39
10.1 Input Line Current 39
10.2 Drain Voltage and Current Normal Operation 40
10.3 Drain Voltage and Current Start-up Operation 40
10.4 Output Current and Output Voltage 41
10.5 Start-up Output Current and Voltage 41
10.6 Output Tracking at Power-up and Power-down 42
10.7 Open Load Test 42
10.8 Output Rectifier Peak Inverse Voltage 43
16 Power Line Transient Test 44
17 Thermal Measurements 45
18 Conducted EMI Measurements 46
18.1 Conducted EMI Test Set-up 46
18.2 Conducted EMI Test Results 47
19 Revision History 49

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a >92% efficient two channel 150 W (2 x 75 W) isolated, power factor corrected, low THD, low harmonic current content, high-efficiency LED driver designed to power a 30 V - 36 V LED string at 2.1 A from an input voltage of 184 VAC to 277 VAC.

LinkSwitch-PH cost effectively delivers a highly efficient single-stage power factor corrected LED driver with primary-side constant current control. The LinkSwitch-PH controller is optimized for LED driver applications with minimal external parts count. Control of the output current through the LED load is achieved without the use of an optocoupler.

The LinkSwitch-PH monolithically integrates the 725 V power MOSFET and controller. The controller consists of an oscillator, PWM, 6 V regulator, BYPASS (BP) pin programming functions, over-temperature protection, frequency jittering, cycle-by-cycle current limit, leading edge blanking, and charge controller for output CC (constant current) control and power factor correction.

The LinkSwitch-PH also provides a sophisticated range of protection features including auto-restart for control loop open/short faults and output short-circuit. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, conducted EMI measurements, thermal measurements, transformer documentation and typical performance characteristics.

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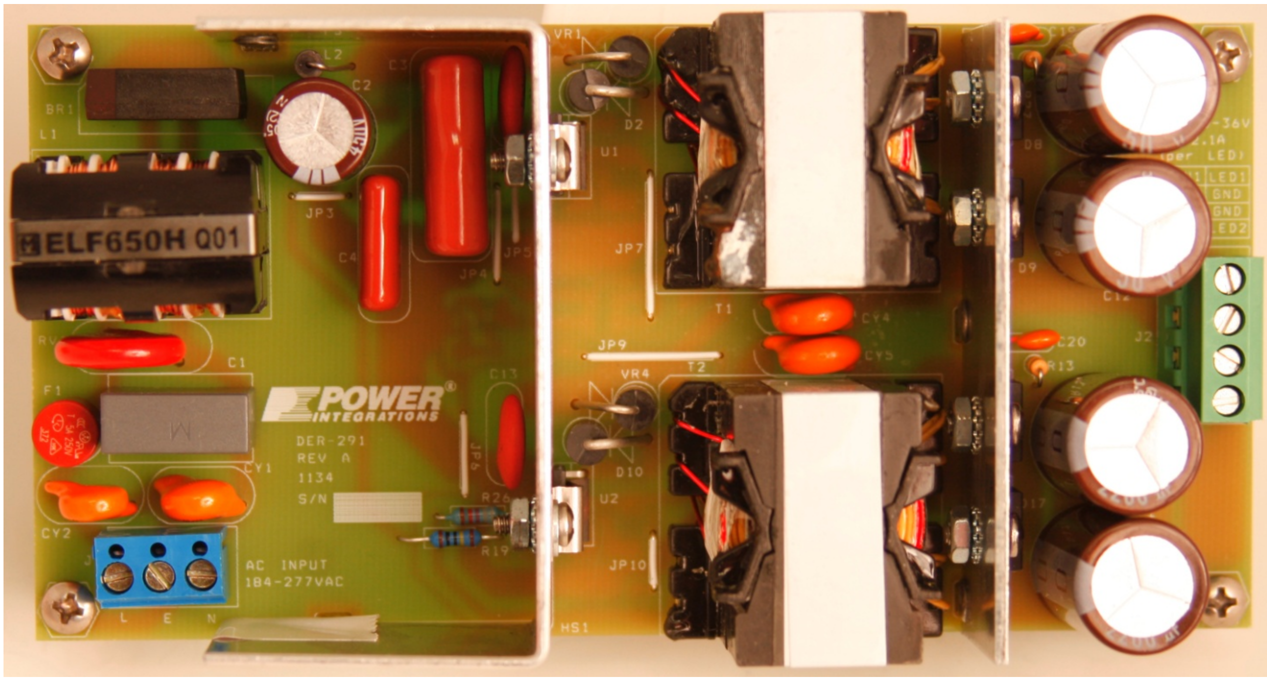

Figure 1 – Populated Circuit Board Photograph, Top (3" x 6").

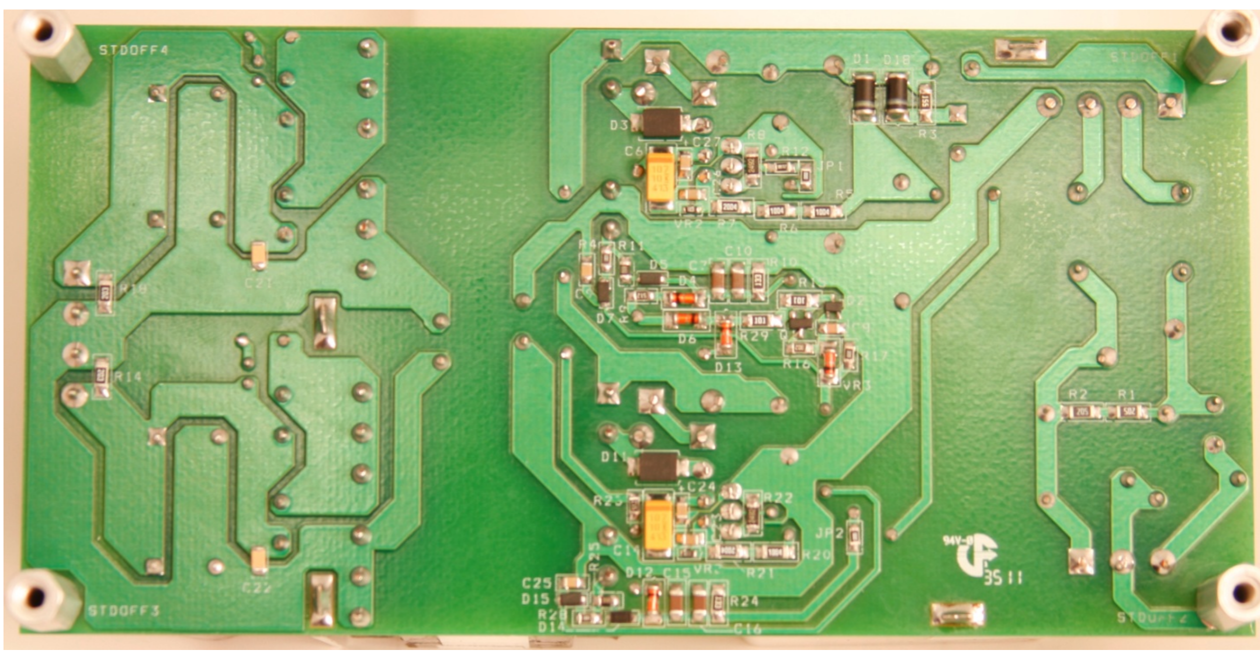

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Design Key Points

- High Efficiency
  - Used larger PQ3230 for lower copper losses, with high quality ferrite material such as PC44 or 4F4 for low core losses.
  - Employed bias supply to power LinkSwitch-PH, the device will draw less power from a low voltage bias supply than the bus supply through its internal regulator.
  - Used 2 parallel Schottky diodes for the output rectifier
  - Used Schottky diodes for drain blocking
- 2 kV Surge Withstand
  - Used small value for V pin peak detector capacitor C3 for faster overvoltage detection
  - Used passive 10 μF electrolytic capacitor C2 to absorb surge energy thus limits the peak voltage of the rectified bus voltage.
- Meets EN61000-3-2 Class C Limits
  - KP <0.65 with the use of flyback topology.
  - Minimize amount of input capacitance (such as X-capacitor)

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3 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	184		277	VAC	3 Wire – Output Floating
Frequency	f_{LINE}		50/60		Hz	
Output						
LED voltage	V_{OUT}	30	33	36	V	
LED1 Current		1.950	2.10	2.250	mA	
LED2 Current		1.950	2.10	2.250	mA	
Total Output Power						
Continuous Output Power	P_{OUT}		150		W	Total for two channels
Environmental						
Conducted EMI		Meets EN55015B				
Safety		Isolated				
Efficiency		91	92			
Harmonic Currents		Class C				IEC 61000-3-2
Power Factor		0.95				
Ambient Temperature	T_{AMB}		65		^{o}C	
Protection						
Open load latching				50	V	AC Reset <1 second

4 Schematic

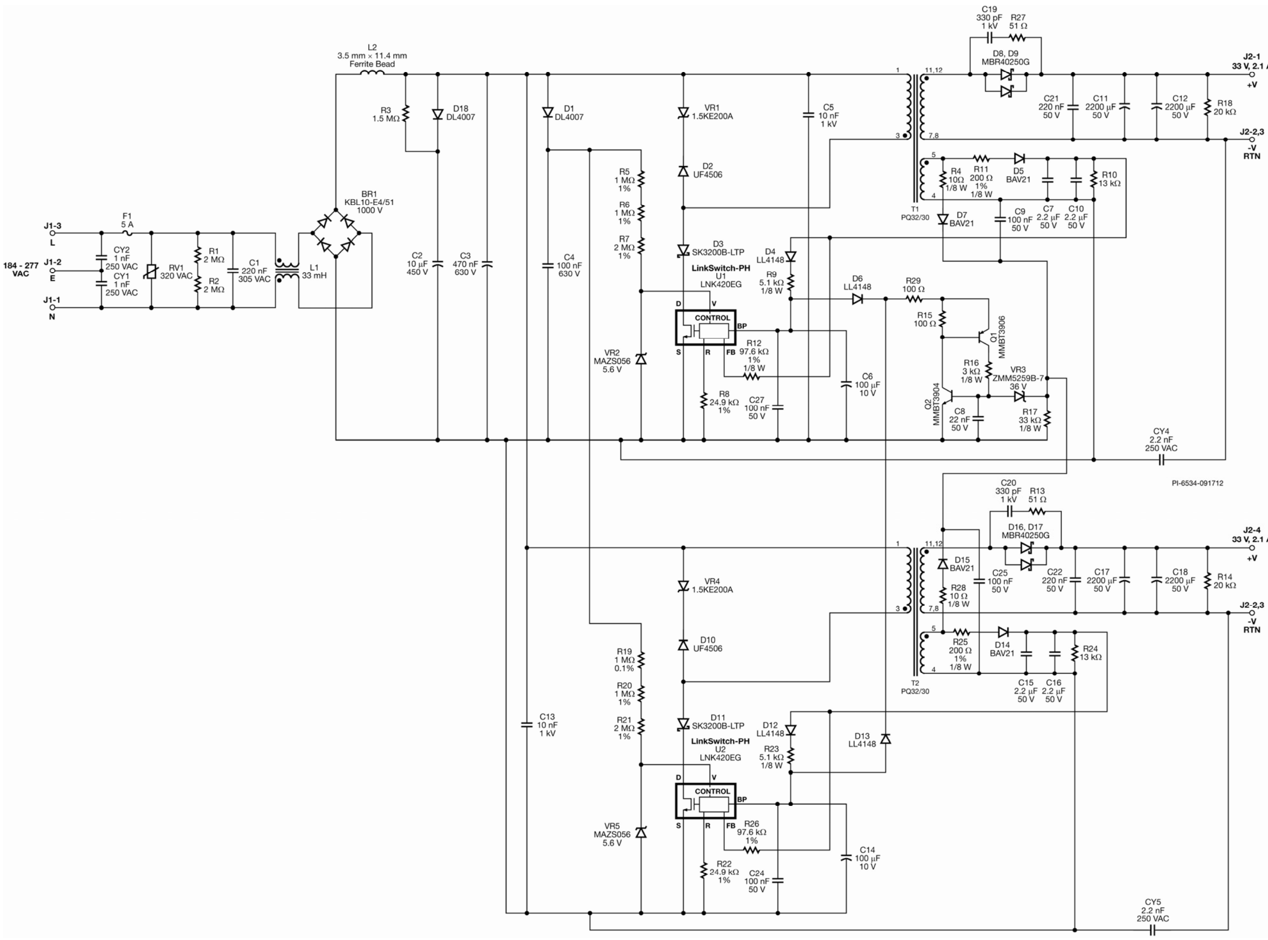

Figure 3 – Schematic.

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5 Description

The LinkSwitch-PH device is a controller and integrated 725 V MOSFET intended for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage continuous conduction mode flyback topology and provides a primary side regulated constant current output while maintaining high power factor and harmonic contents from the AC input.

5.1 Input Filtering

Fuse F1 protects the input and BR1 rectifies the AC line voltage. Inductor L1, L2, and C1 form the EMI filter and together with CY1, CY2, CY4 and CY5 (Y1 safety) capacitors allow the design to meet EN55015B conducted EMI limits. Capacitor C3 provides a low impedance path for the primary switching current, a low value of capacitance is necessary to maintain a power factor of greater than 0.9. High-voltage bypass capacitors C13 and C5 shrink the loop area of the input of each converter to reduce EMI generation.

5.2 LinkSwitch-PH Primary

Diode D1 and high-voltage capacitor C4 detects the peak AC line voltage. Capacitor C4 value was made small (100 nF) for faster detection of line over voltage especially during differential mode surge events. This voltage is converted to a current into the VOLTAGE MONITOR (V) pin via the series resistors connected to the V pin of U1 and U2. The current detected is also used by the device to set the input over/undervoltage protection thresholds. The V pin current and the FEEDBACK (FB) pin current are used internally to control the average output LED current. Non-dimming designs require 24.9 kΩ resistor on the REFERENCE (R) pin (R8, R22) and 4 MΩ resistors on the V pin. Zener diode VR2 and VR5 provides protection for the V pin during start-up.

Diodes D2, D10, VR1 and VR4 clamp the drain voltage to below the BV_{DSS} rating (725 V) of the internal power MOSFET in U1 and U2. Diode D3 and D11 are necessary to prevent reverse current from flowing through the LinkSwitch-PH device (the result of the minimal input capacitance).

To withstand a 2 kV differential line input surge, varistor RV1 and C10 (10 μF) was employed to absorb most of the energy during surge, limiting the maximum bus voltage. Diode D18 isolates C2 from the AC input during normal operation and R3 is the discharge path C2 after a surge event.

5.3 Bias Supply and Output Overvoltage Sensing

Diode D5, D14, C7, C10, C15, and C16 form the primary bias supply. This supplies the IC operating current into the BYPASS (BP) pin through D4, D12 and R9, R23 during normal operation. Resistors R11, R25 provide filtering to improve output regulation while R10, R24 acts as a minimum load.

Capacitors C6 and C14 are the supply decoupling for the LinkSwitch-PH. During start-up these are charged to ~6 V from an internal high-voltage current source tied to the device DRAIN (D) pin. Once charged the energy stored in these capacitors supplies the device until the output and bias winding voltage rise in regulation. Capacitors C24 and C27 provide local high frequency decoupling. These must be placed at the device pins of U1 and U2.

Open-load/overvoltage shutdown function is provided by the two transistors Q1 and Q2. When an overvoltage is detected through VR3, Q2 pulls down the BP pins of both U1 and U2, via D6, D13 to its BP-UVLO threshold level and will remain off until the AC input is recycled. A separate bias supply was used (R4, D7, and C9) to allow a lower value filter capacitor (C9) and therefore a shorter response time to an output OV condition.

5.4 Output Feedback

A current proportional to the output voltage from the primary bias winding is fed into the FB pin through R12 and R26. This information together with the line input voltage and the drain current are used to maintain a constant output current.

5.5 Output Rectification and Filtering

Diodes D8, D9, D16, and D17 rectify the secondary winding while capacitors C11, C12, C17, and C18 filter the output. For high efficiency two 20 A, 250 V Schottky diodes were used for each output. Resistor R18 and R14 provides a minimum load to discharge the charged left in the output capacitors when the AC is removed.

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6 PCB Layout

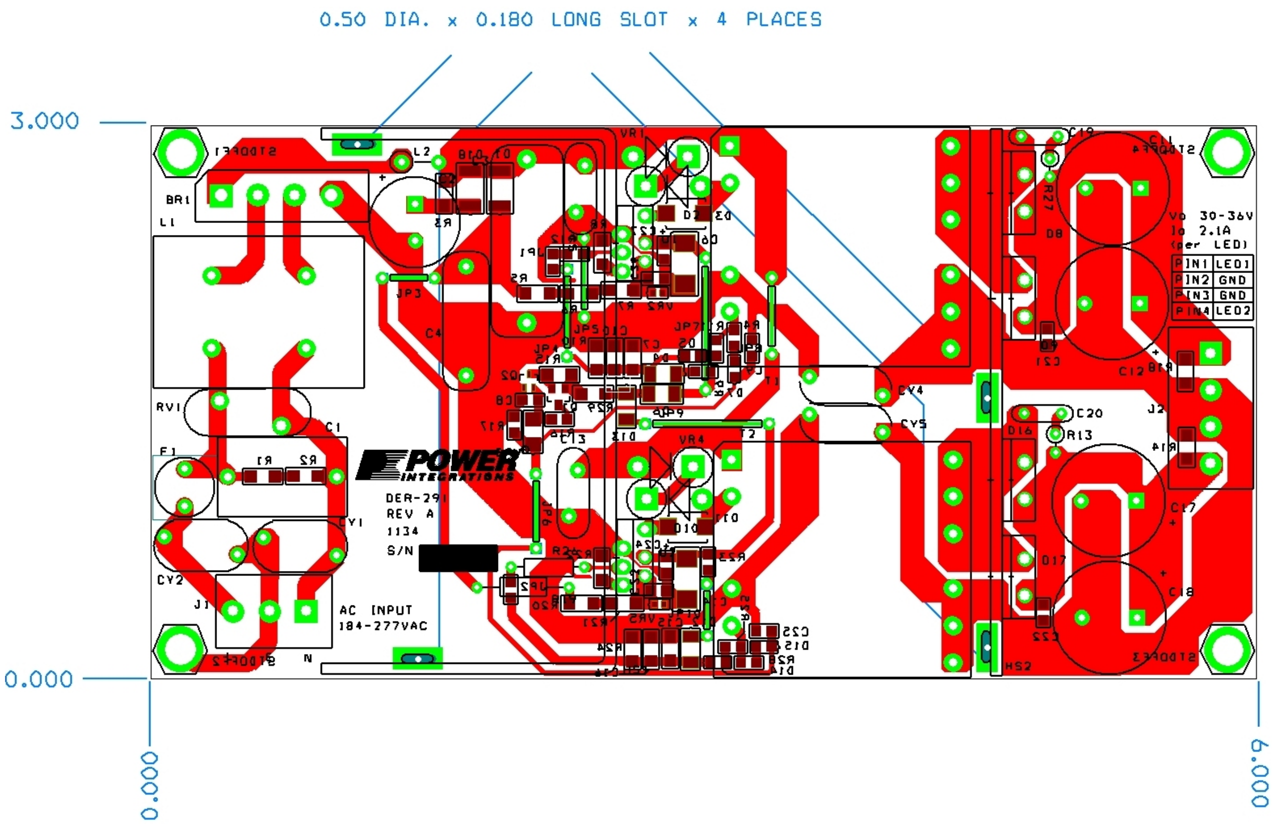

Figure 4 – Printed Circuit Layout, Top and Bottom (3” x 6”).

7 Bill of Materials

7.1 Electrical BOM

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 4 A, Bridge Rectifier	KBL10-E4/51	Vishay
2	1	C1	220 nF, 305 VAC, Film, X2	R463I322000M2M	Kemet
3	1	C2	10 μF, 450 V, Electrolytic, (12.5 x 20)	EKMG451ELL100MK20S	United Chemi-Com
4	1	C3	470 nF, 630 V, Film	ECQ-E6474KF	Panasonic
5	1	C4	100 nF, 630 V, Film	ECQ-E6104KF	Panasonic
6	2	C5 C13	10 nF, 1 kV, Disc Ceramic	562R5HKMS10	Vishay
7	2	C6 C14	100 μF, 10 V, Tant Electrolytic, C Case, SMD	T491C107K010AS	Kemet
8	4	C7 C10 C15 C16	2.2 μF, 50 V, Ceramic, Y5V, 1206	GRM31MF51H225ZA01L	Murata
9	1	C8	22 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H223K	Panasonic
10	4	C9 C24 C25 C27	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
11	4	C11 C12 C17 C18	2200 μF, 50 V, Electrolytic, Gen. Purpose, (16 x 35.5)	EKMG500ELL222MLP1S	Nippon Chemi-Con
12	2	C19 C20	330 pF, 1 kV, Disc Ceramic	562R5GAT33	Vishay
13	1	C21	220 nF, 50 V, Ceramic, X7R, 1206	ECJ-3YB1H224K	Panasonic
14	1	C22	220 nF, 50 V, Ceramic, X7R, 1206	12065C224KAT2A	AVX
15	2	CY1 CY2	1 nF, Ceramic, Y1	440LD10-R	Vishay
16	2	CY4 CY5	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
17	2	D1 D18	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
18	2	D2 D10	600 V, 3 A, Ultrafast Recovery, 75 ns, DO-201AD	UF5406-E3/54	Vishay
19	2	D3 D11	200 V, 3 A, Diode Schottky 1 A 200 V, SMB	SK3200B-LTP	Micro Commercial
20	4	D4 D6 D12 D13	75 V, 0.15 A, Fast Switching, 4 ns, MELF	LL4148-13	Diodes, Inc.
21	4	D5 D7 D14 D15	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
22	4	D8 D9 D16 D17	250 V, 40 A, Schottky, TO-220AC	MBR40250G	On Semi
23	1	F1	5 A, 250 V, Slow, TR5	37215000411	Wickman
24	1	L1	33 mH, 0.8 A, Common Mode Choke	ELF-18D650H	Panasonic
25	1	L2	3.5 mm x 11.4 mm, 144 Ohms at 100 MHz, #22 AWG hole, Ferrite Bead	2761008112	Fair-Rite
26	1	Q1	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3906LT1G	On Semi
27	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
28	2	R1 R2	2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
29	1	R3	1.5 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ155V	Panasonic
30	2	R4 R28	10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
31	3	R5 R6 R20	1.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
32	2	R7 R21	2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
33	2	R8 R22	24.9 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2492V	Panasonic
34	2	R9 R23	5.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
35	2	R10 R24	13 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ133V	Panasonic
36	2	R11 R25	200 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2000V	Panasonic
37	1	R12	97.6 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9762V	Panasonic
38	2	R13 R27	51 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-51R	Yageo
39	2	R14 R18	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
40	2	R15 R29	100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ101V	Panasonic

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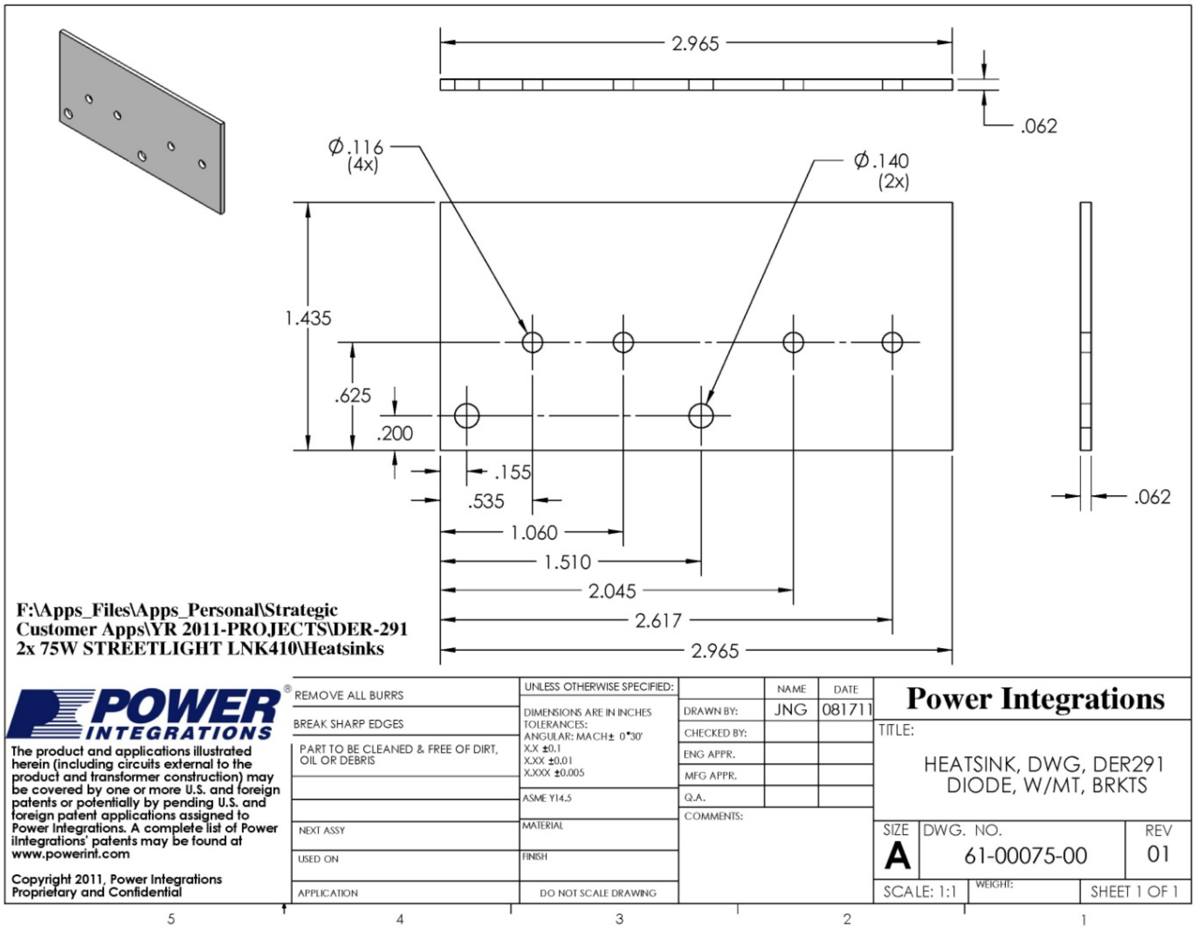
41	1	R16	3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ302V	Panasonic
42	1	R17	33 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ333V	Panasonic
43	1	R19	1 MΩ, 0.1%, 1/4 W, Metal Film	RC55Y-1M0BI	Welwyn Comp
44	1	R26	97.6 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-97K6	Yageo
45	1	RV1	320 V, 80 J, 14 mm, RADIAL	V320LA20AP	Littlefuse
46	2	U1 U2	LinkSwitch-PH, eSIP	LNK420EG	Power Integrations
47	2	VR1 VR4	200 V, 1500 W, TVS, GP-20	1.5KE200A-E3/54	Vishay
48	2	VR2 VR5	5.6 V, 5%, 150 mW, SOD-323	MAZS0560ML	Panasonic
49	1	VR3	39 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5259B-7	Diodes, Inc.

8 Heat Sink Assemblies

8.1 Output Diode Heat Sink

8.1.1 Output Diode Heat Sink Drawing



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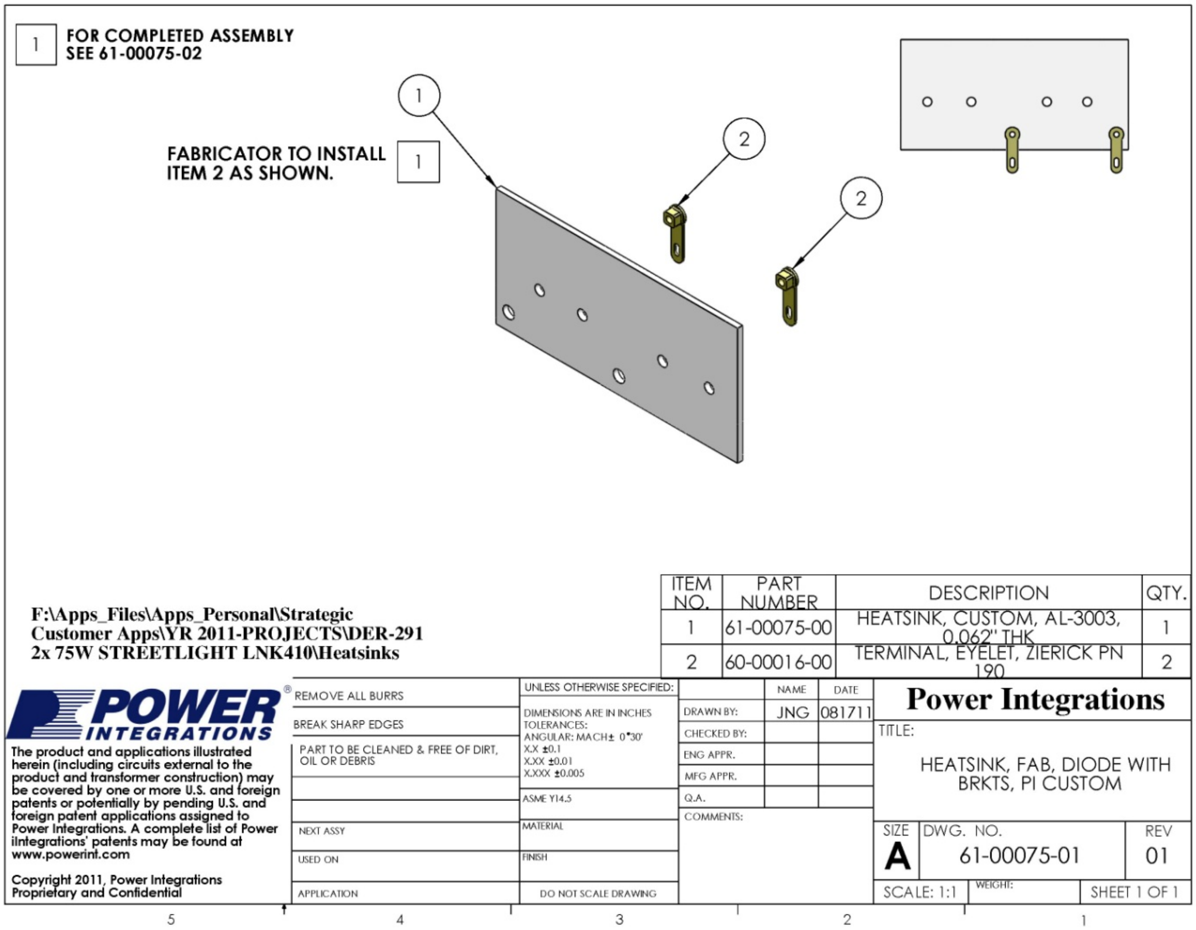
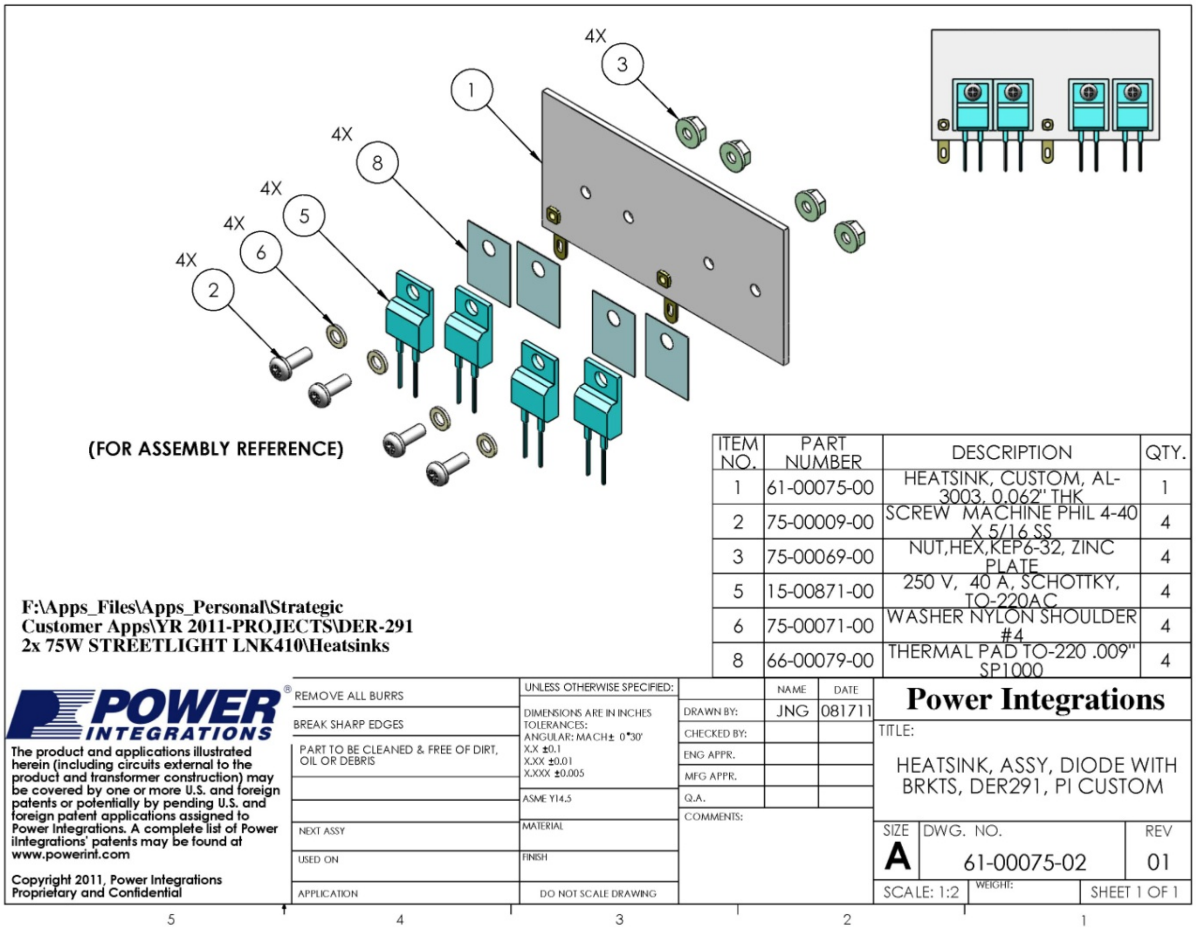
8.1.2 Output Diode Heat Sink Fabrication Drawing



8.1.3 Output Diode and Heat Sink Assembly Drawing



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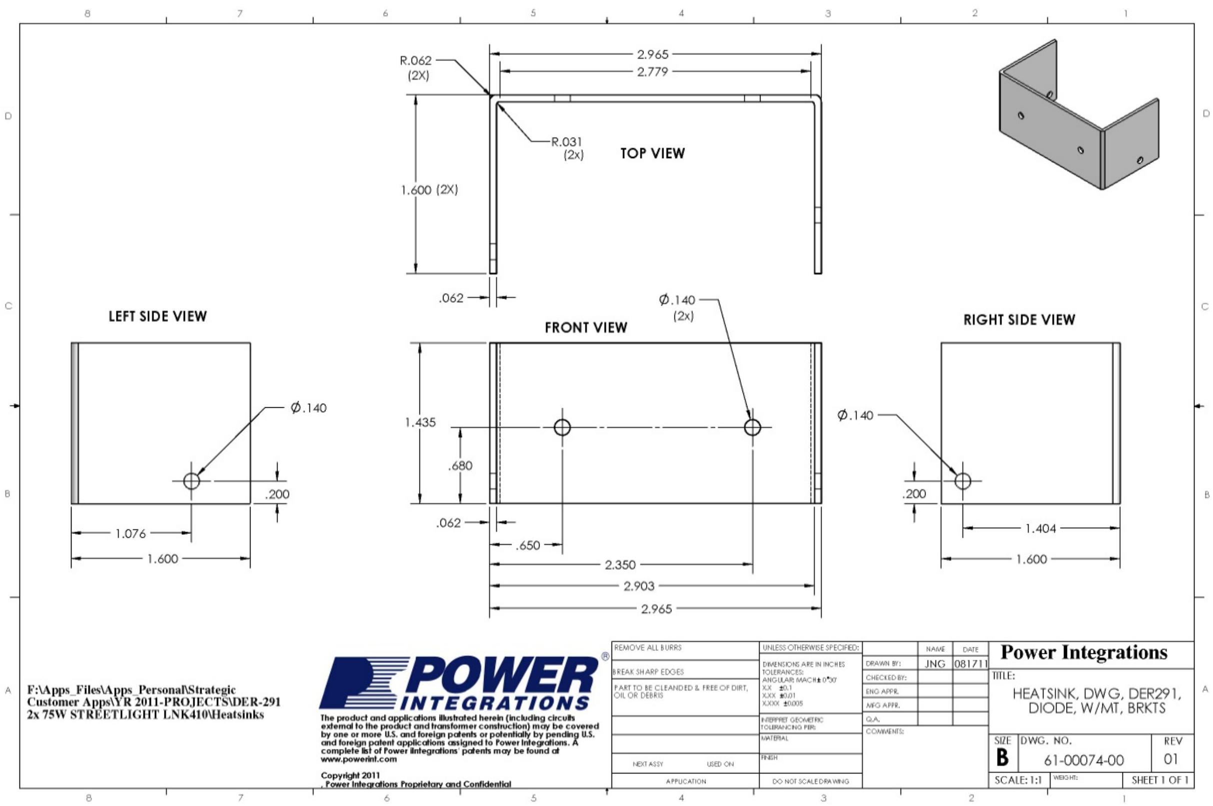
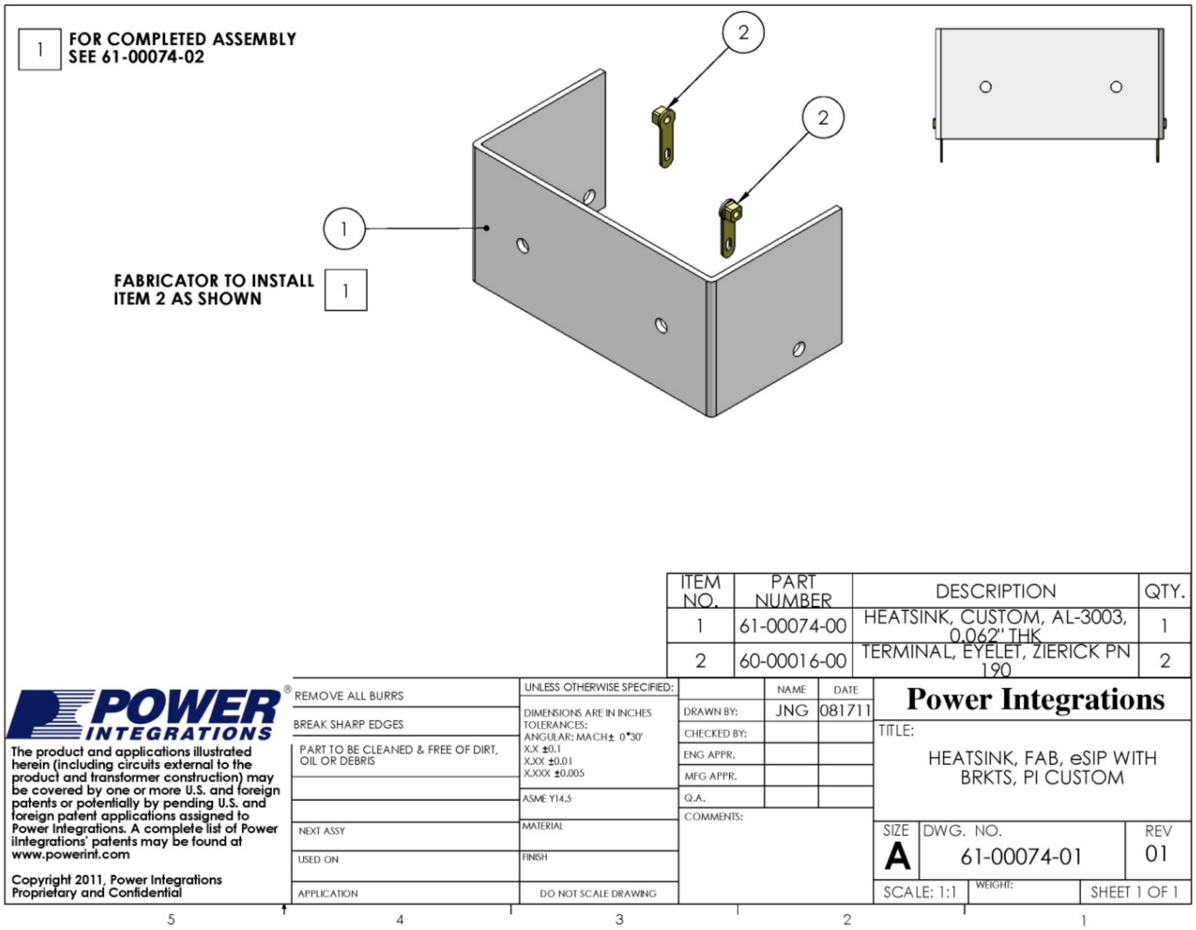
8.2 eSIP Heat Sink

8.2.1 eSIP Heat Sink Drawing



8.2.2 eSIP Heat Sink Fabrication Drawing



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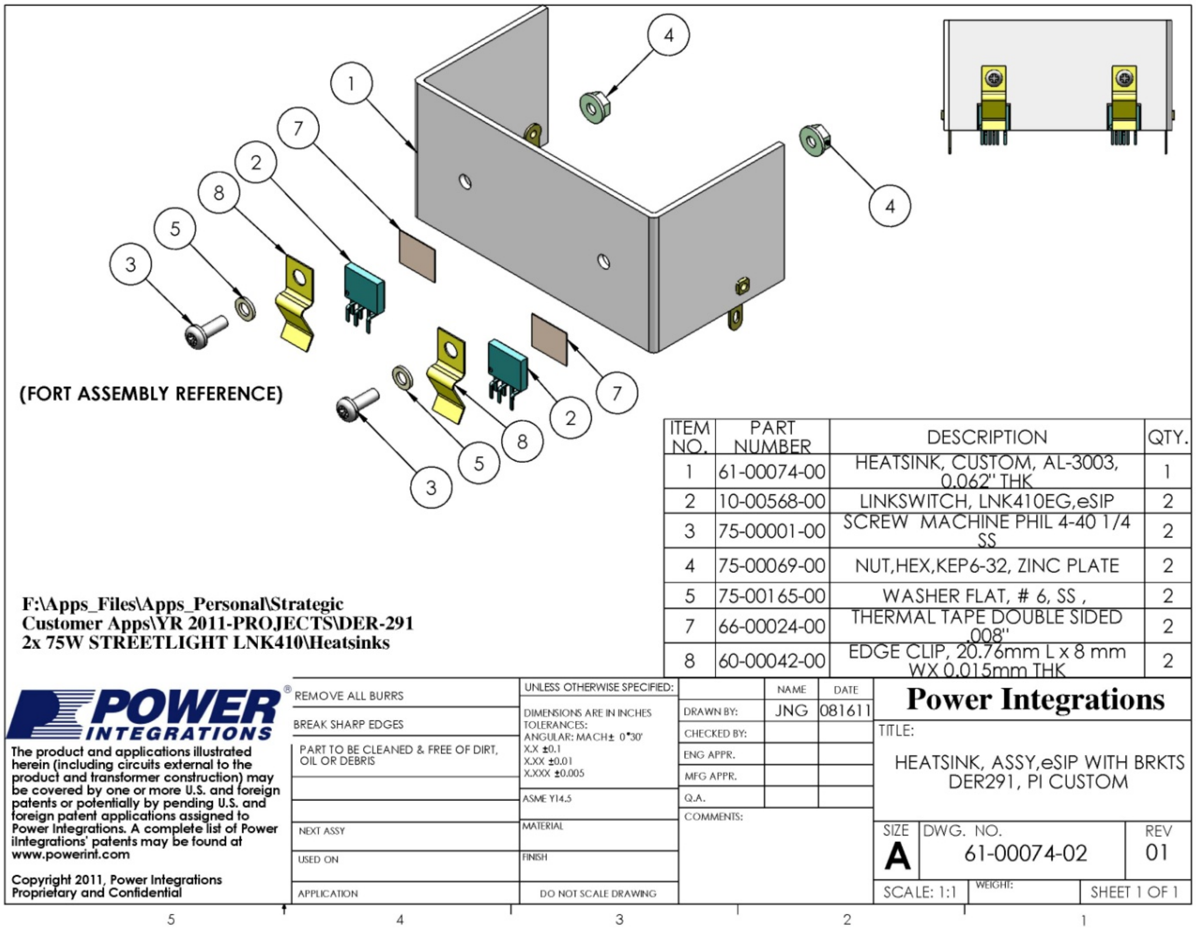
8.2.3 eSIP and Heat Sink Assembly Drawing



9 Transformer Specification

9.1 Electrical Diagram

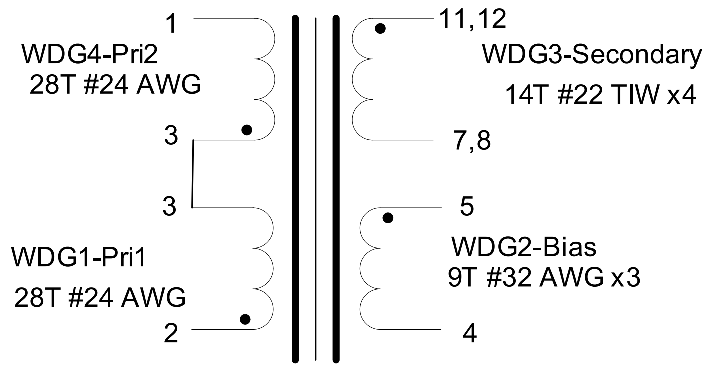


Figure 5 – Transformer Electrical Diagram.

9.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-12	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	1186 μH, +/-10%
Resonant Frequency	Pins 1-2, all other windings open	1700 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with pins 7-12 shorted, measured at 100 kHz, 0.4 V_{RMS}	7 μH (Max.)

9.3 Materials

Item	Description
[1]	Core: PC444; PQ3230.
[2]	Bobbin: RPQ3230 Vertical, 6+6 Pins.
[3]	Magnet Wire: #24 AWG.
[4]	Magnet Wire: #33 AWG.
[5]	Magnet Wire: #22 AWG Triple-insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 17.7 mm Width.
[7]	Tape: 3M 1298 Polyester Film, 36 mm Width.
[7]	Tape: 3M 1298 Polyester Film, 10 mm Width.
[8]	Varnish.

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9.4 Transformer Build Diagram

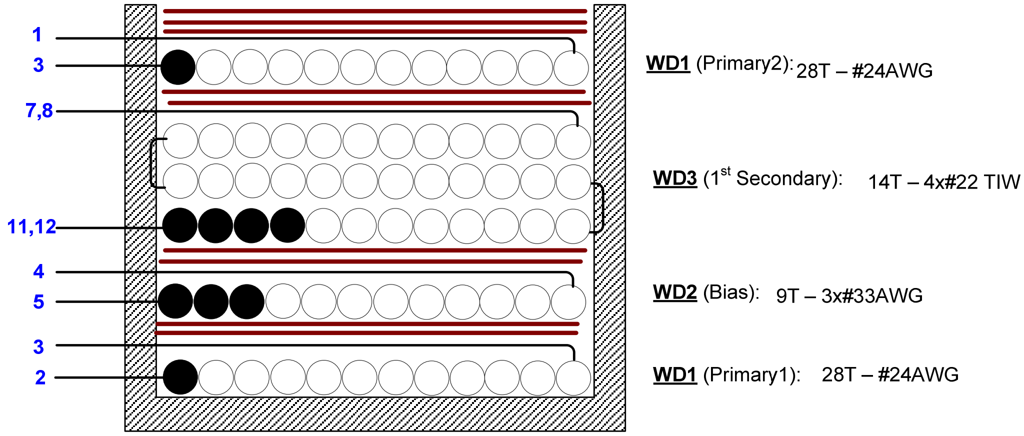
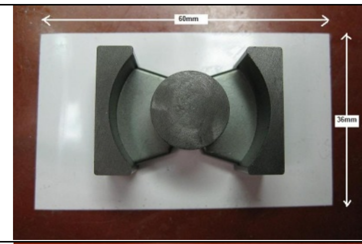
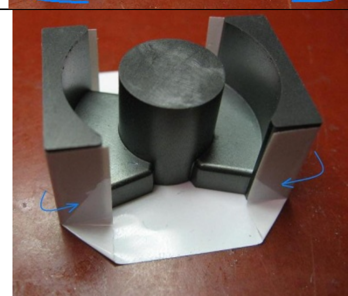
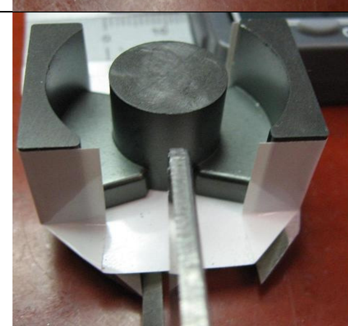
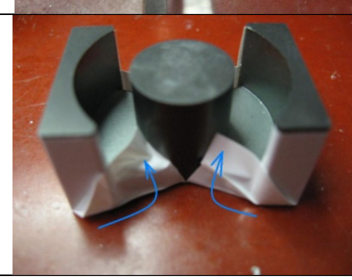


Figure 6 – Transformer Build Diagram.

9.5 Transformer Construction

Bobbin Preparation	Position the bobbin such that the pins are on the left side of the bobbin chuck. Machine rotates in forward direction.
WDG1 Primary 1	Start at pin 2; wind with firm tension 28 turns of item [3] from left to right. Finish at pin 3.
Insulation	2 layers of tape [6] for insulation.
WDG2 Bias	Start at pin 5; wind with firm tension 9 trifilar turns of item [4] from left to right. Finish at pin 4.
Insulation	2 layers of tape [6] for insulation.
WDG3 Secondary	Start at pin 11 and 12; wind with firm tension 14 quadfilar turns of item [5] in continuously in three layers. Finish at pin 7 and 8. Termination is 2 wires per pin.
Insulation	2 layers of tape [6] for insulation.
WDG4 Primary 2	Start at pin 3; wind with firm tension 28 turns of item [3] from left to right. Finish at pin 1.
Insulation	3 layers of tape [6] for insulation.
Taping	Add 1 layer of tape [7] on the bottom side of the transformer to isolate the core to secondary and primary pins. Refer to the figures below.
Assemble core	Assemble and secure the cores with 3 layers of tape [7].
Finish	Varnish transformer assembly.

9.6 Transformer Core Wrapping Process

Step 1. Position the core at the center of 60 mm X 36 mm polyester film tape [7]	
Step 2. Fold both ends of the tape into the sides of the core as shown in the illustration. Make sure that no excess tape higher than the core.	
Step 3. Fold the tape in the 4 corners of the core. Extend the folding down to the bottom of the tape until it locks.	
Step 4. Cut the center of the bottom tape on its 2 sides.	
Step 5. Fold the tape into the legs of the core as shown in the illustration. Same procedure is applied to the other side of the core.	

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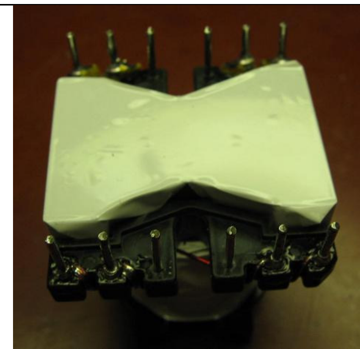
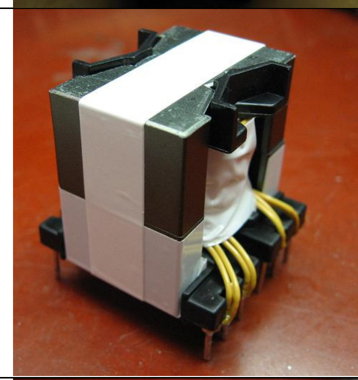
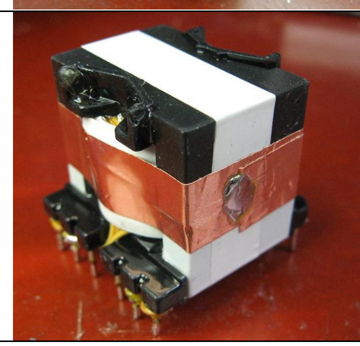
Step 6. Insert the wrapped core into the bottom side of the bobbin. Make sure that the tape is inserted between the core and the bobbin as shown in the figure.	
Step 7. Grind the top portion of the core to set the inductance as required. Assemble and fix the cores as shown in the illustration. Varnish.	
Step 8. Add 1 turn of copper shield as shown in the illustration. Solder the end of the copper shield. Varnish.	

Figure 7 – Core Wrapping Illustration.

10 Transformer Design Spreadsheet

ACDC_LinkSwitch-PH_040312; Rev.1.8; Copyright Power Integrations 2012	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_040312: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**NO**		**NO**		Select 'YES' option if dimming is required. Otherwise select 'NO'.
VACMIN	184		184	V	Minimum AC Input Voltage
VACMAX	277		277	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	33.00		33	V	Typical output voltage of LED string at full load
VO_MAX			36.30	V	Maximum expected LED string Voltage.
VO_MIN			29.70	V	Minimum expected LED string Voltage.
V_OVP			38.50	V	Over-voltage protection setpoint
IO	2.10		2.10	A	Typical full load LED current
PO			69.3	W	Output Power
n			0.8		Estimated efficiency of operation
VB			20	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK420**			Universal	115 Doubled/230V
Chosen Device		LNK420	Power Out	79W	74W
Current Limit Mode	**FULL**		FULL		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			4.90	A	Minimum current limit
ILIMITMAX			5.70	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			78.4	uA	V pin current
RV	4.00		4	M-ohms	Upper V pin resistor
RV2			1.402	M-ohms	Lower V pin resistor
IFB	180.00		180.0	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			94.4	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	0.53		0.53		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			1186	uH	Primary Inductance
VOR	133.00		133	V	Reflected Output Voltage.
Expected IO (average)		Info	1.90	A	Expected Average Output current is outside 5% tolerance band. Change IFB to 206 for better current regulation set-point
KP_VACMAX			0.65		Expected ripple current ratio at VACMAX
TON_MIN			3.84	us	Minimum on time at maximum AC input voltage
PCLAMP			0.78	W	Estimated dissipation in primary clamp
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**PQ3230**		**PQ3230**		
Bobbin		*PQ3230/ 12pins*			
AE	1.6700		1.67	cm^2	Core Effective Cross Sectional Area
LE	7.5000		7.5	cm	Core Effective Path Length
AL	4500.0		4500	nH/T^2	Ungapped Core Effective Inductance
BW	17.0		17	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to

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					Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS	14		14		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			260	V	Peak input voltage at VACMIN
VMAX			392	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.35		Minimum duty cycle at peak of VACMIN
IAVG			0.48	A	Average Primary Current
IP			2.42	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.83	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1186	uH	Primary Inductance
NP			56		Primary Winding Number of Turns
NB			9		Bias Winding Number of Turns
ALG			384	nH/T^2	Gapped Core Effective Inductance
BM			3089	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3603	Gauss	Peak Flux Density (BP<3700)
BAC			818	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
Ur			1608		Relative Permeability of Ungapped Core
LG			0.50	mm	Gap Length (Lg > 0.1 mm)
BWE			34	mm	Effective Bobbin Width
OD			0.61	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.54	mm	Bare conductor diameter
AWG			24	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			406	Cmils	Bare conductor effective area in circular mils
CMA			490	Cmils/Amp	!!! DECREASE CMA (200 < CMA < 600) Decrease L(primary layers),increase NS,smaller Core
LP_TOL	10		10		Tolerance of primary inductance
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			9.60	A	Peak Secondary Current
ISRMS			4.16	A	Secondary RMS Current
IRIPPLE			3.60	A	Output Capacitor RMS Ripple Current
CMS			833	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.81	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.21	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN			660	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			137	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			84	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			4.00	M-ohms	Upper V Pin Resistor Value
RV2			1.40	M-ohms	Lower V Pin Resistor Value

VAC1			115.0	V	Test Input Voltage Condition1
VAC2			230.0	V	Test Input Voltage Condition2
IO_VAC1			2.10	A	Measured Output Current at VAC1
IO_VAC2			2.10	A	Measured Output Current at VAC2
RV1 (new)			4.00	M-ohms	New RV1
RV2 (new)			1.40	M-ohms	New RV2
V_OV			325.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			72.4	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1	97.6		98	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+012	k-ohms	Lower FB Pin Resistor Value
VB1			18.0	V	Test Bias Voltage Condition1
VB2			22.0	V	Test Bias Voltage Condition2
IO1	2.1		2.10	A	Measured Output Current at Vb1
IO2			2.10	A	Measured Output Current at Vb2
RFB1 (new)			97.6	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

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11 Performance Data

The following data was measured using 3 sets of loads (30 V, 33 V, and 36 V). Refer to the table on Section 12.6 for the complete set of data values. All measurements were performed open frame at room temperature.

11.1 Efficiency

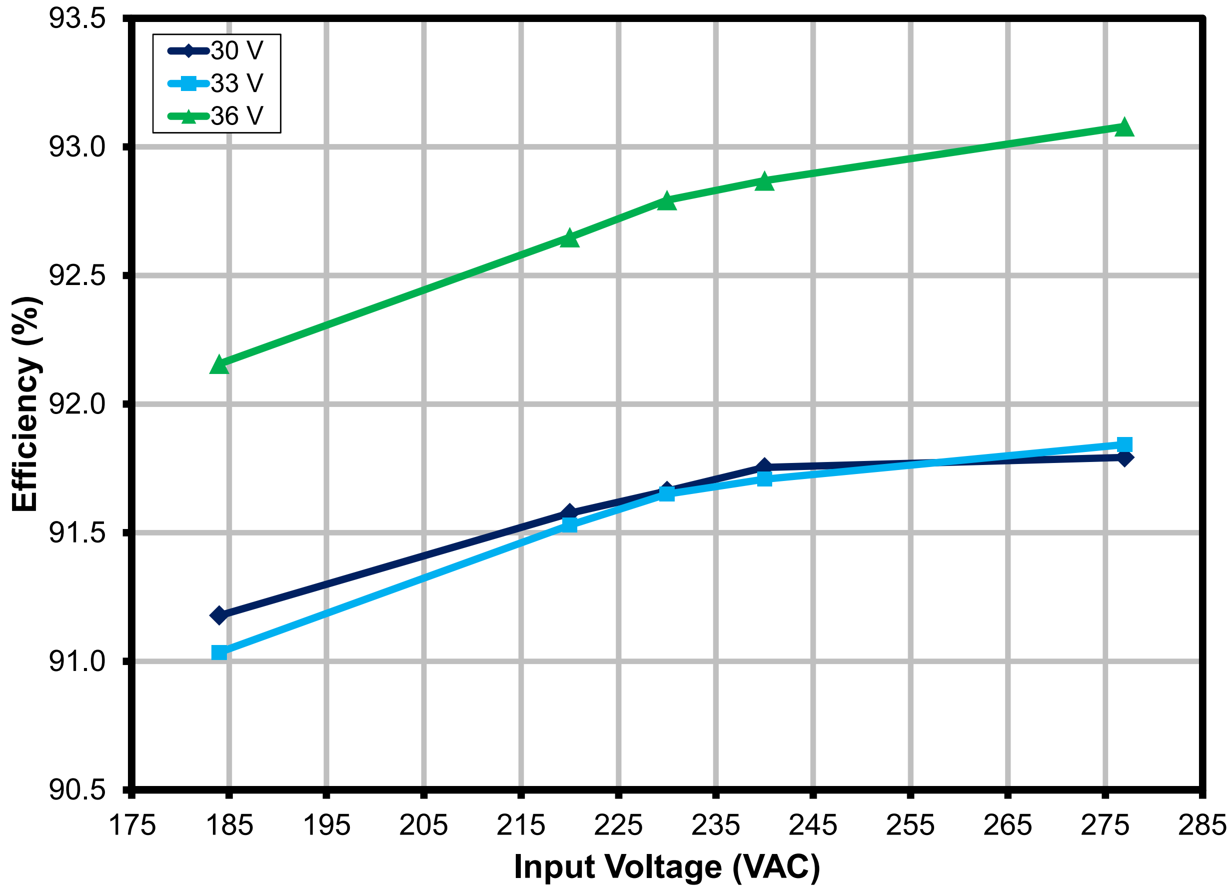

Figure 8 – Efficiency vs. Line and Load.

11.2 Line and Load Regulation

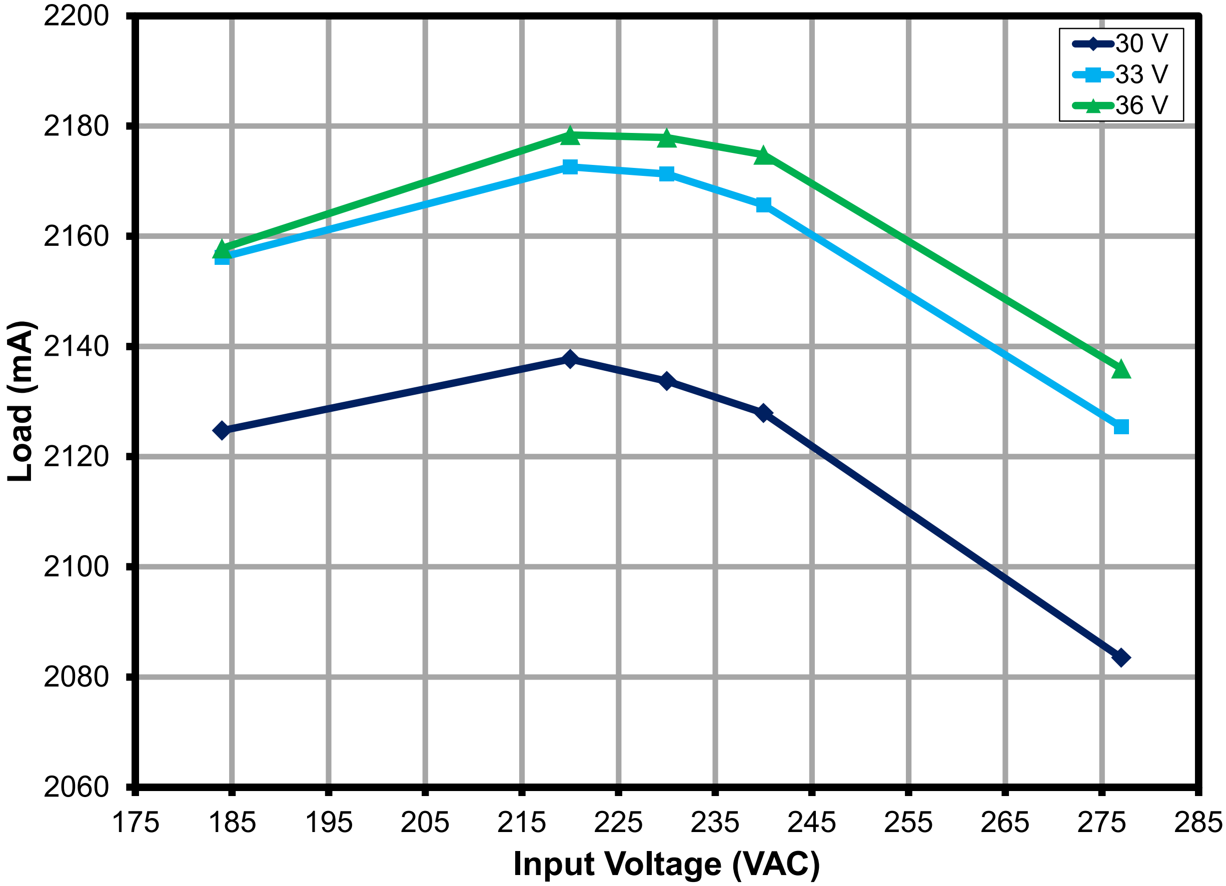

Figure 9 – Regulation vs. Line and Load.

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11.3 Power Factor

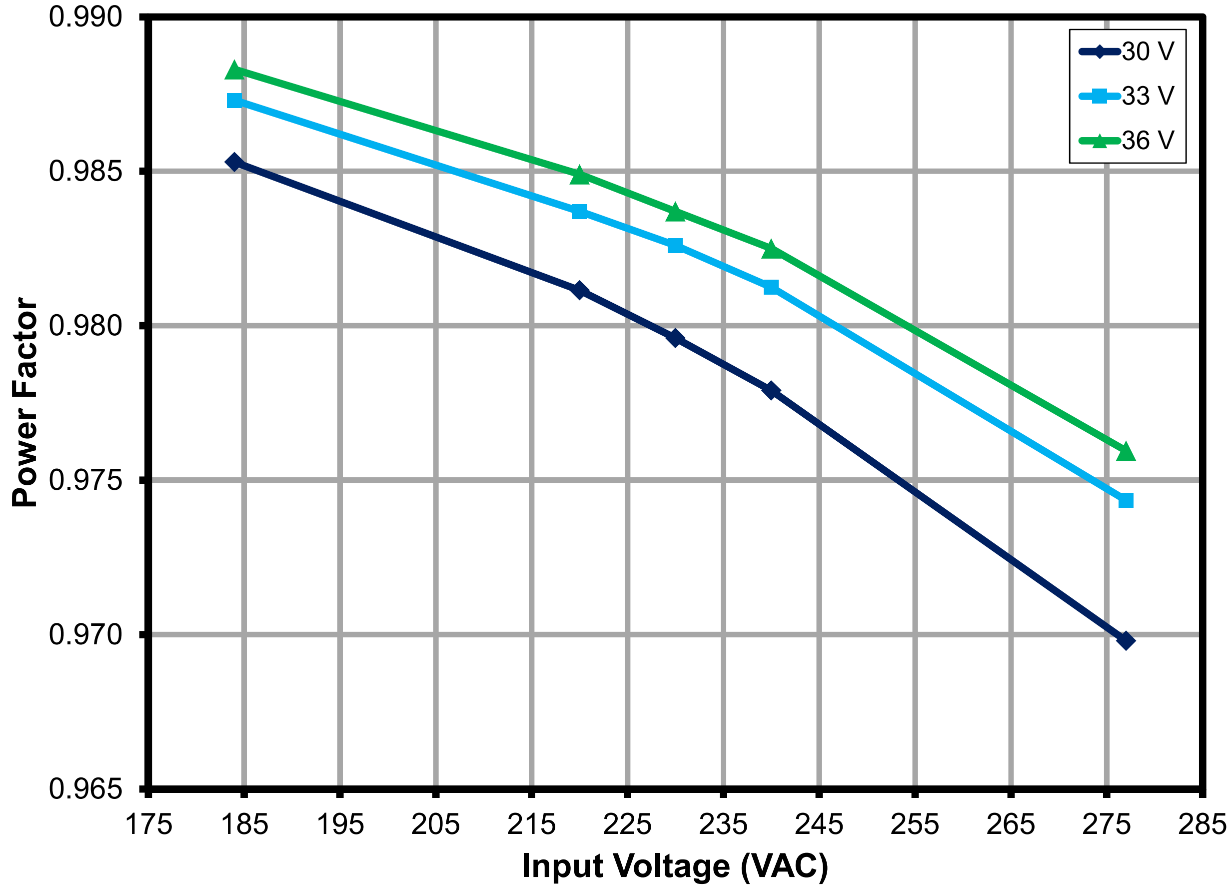

Figure 10 – Power Factor vs. Line and Load.

11.4 A-THD

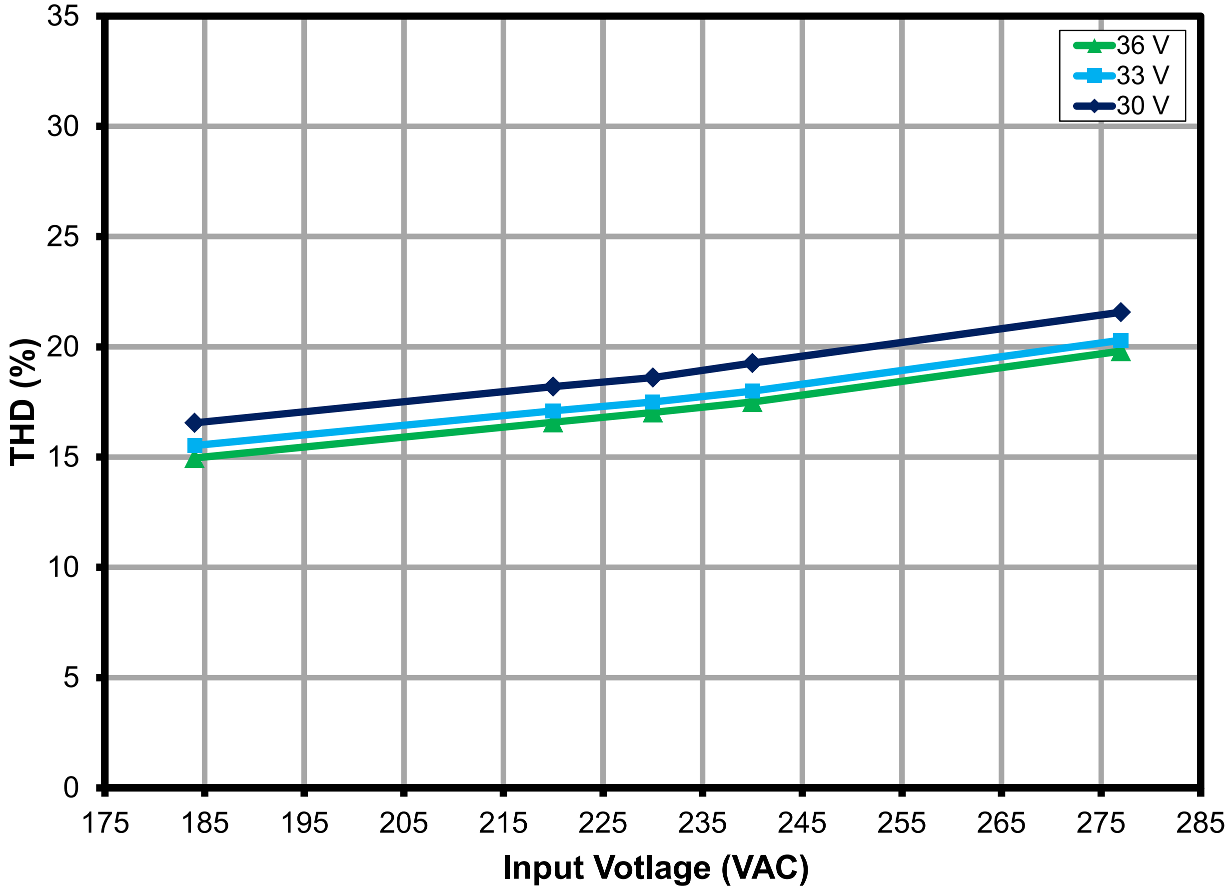

Figure 11 – A-THD vs. Line and Load.

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11.5 Harmonic Currents

11.5.1 30 V LED Load

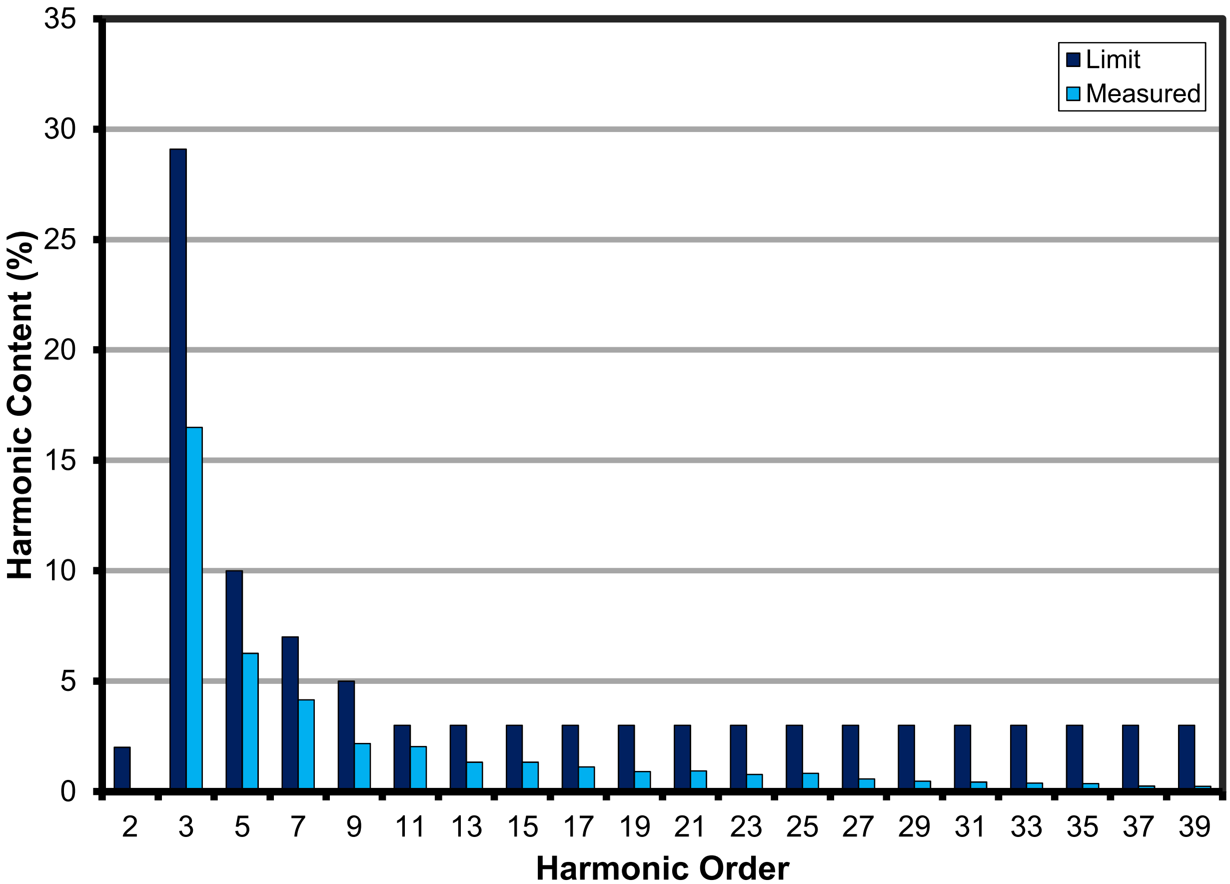

Figure 12 – Input Current Harmonics. Class C EN61000-3-2.

11.5.2 33 V LED Load

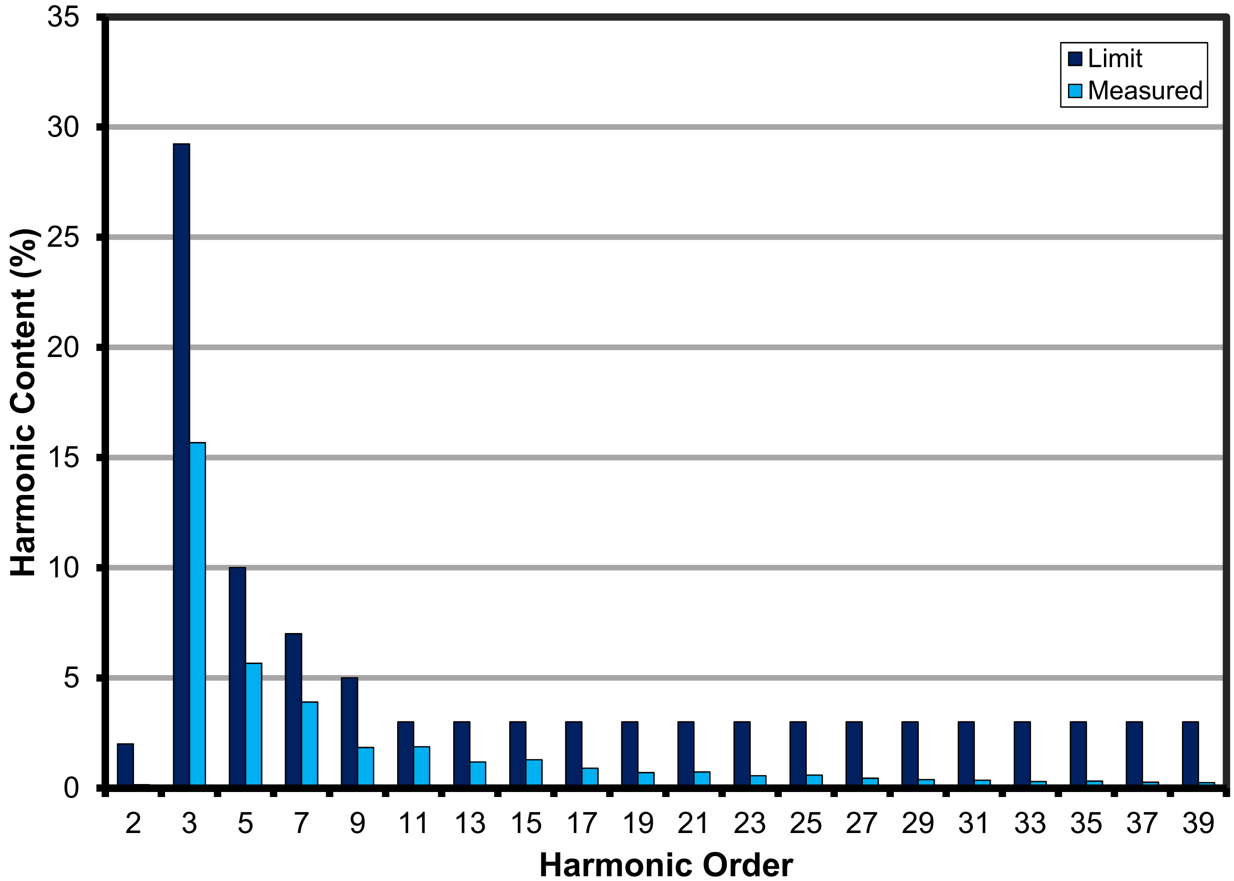

Figure 13 – Input Current Harmonics. Class C EN61000-3-2.

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11.5.3 36 V LED Load

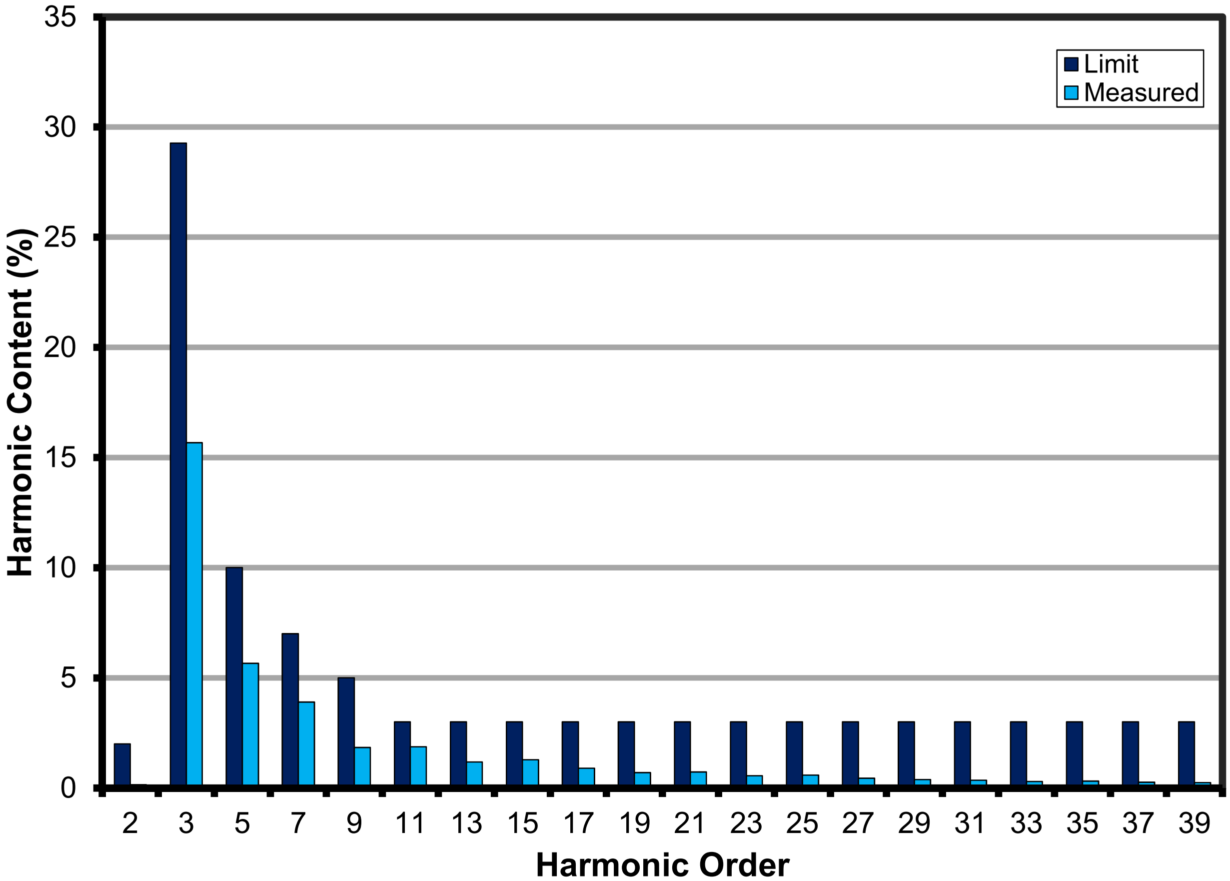

Figure 14 – Input Current Harmonics. Class C EN61000-3-2.

11.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient, and 50 Hz line frequency

11.6.1 Test Data, 30 V LED Load

Input		Input Measurement					Load Measurement CH1			Load Measurement CH2			Calculation	
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	$P_{TOTAL(CAL)}$ (W)	Efficiency (%)
184	50	184.66	742.70	135.13	0.985	16.56	29.56	2124.70	62.95	28.91	2087.90	60.51	123.46	91.18
220	50	220.83	623.30	135.05	0.981	18.20	29.47	2137.70	63.14	28.86	2099.60	60.75	123.88	91.58
230	50	230.93	594.45	134.47	0.980	18.61	29.39	2133.70	62.84	28.82	2097.10	60.58	123.42	91.66
240	50	240.97	567.80	133.80	0.978	19.26	29.33	2127.90	62.54	28.78	2092.40	60.36	122.90	91.75
277	50	278.19	484.35	130.68	0.970	21.57	29.24	2083.50	61.04	28.71	2051.40	59.03	120.07	91.79

11.6.2 Test Data, 33 V LED Load

Input		Input Measurement					Load Measurement CH1			Load Measurement CH2			Calculation	
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	$P_{TOTAL(CAL)}$ (W)	Efficiency (%)
184	50	184.63	861.55	157.05	0.987	15.52	33.32	2156.20	71.97	33.36	2120.60	70.86	142.84	91.04
220	50	220.91	723.05	157.13	0.984	17.10	33.31	2172.60	72.48	33.32	2135.20	71.26	143.75	91.53
230	50	230.90	690.20	156.59	0.983	17.50	33.28	2171.30	72.38	33.27	2133.50	71.10	143.48	91.65
240	50	240.99	659.25	155.90	0.981	17.99	33.25	2165.70	72.13	33.23	2128.10	70.83	142.96	91.71
277	50	278.27	562.10	152.42	0.974	20.30	33.18	2125.40	70.62	33.15	2089.20	69.37	139.99	91.84

11.6.3 Test Data, 36 V LED Load

Input		Input Measurement					Load Measurement CH1			Load Measurement CH2			Calculation	
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	$P_{TOTAL(CAL)}$ (W)	Efficiency (%)
184	50	184.70	915.95	167.19	0.988	14.96	36.02	2157.80	77.84	35.87	2125.50	76.35	154.187	92.16
220	50	220.92	767.10	166.90	0.985	16.59	35.82	2178.40	78.14	35.70	2143.60	76.65	154.787	92.65
230	50	230.97	730.15	165.90	0.984	17.03	35.65	2177.90	77.75	35.55	2143.20	76.30	154.054	92.79
240	50	241.06	696.30	164.91	0.983	17.50	35.51	2174.80	77.35	35.44	2138.20	75.88	153.233	92.87
277	50	278.34	592.65	160.99	0.976	19.81	35.36	2136.00	75.64	35.30	2101.30	74.27	149.914	93.08

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11.6.4 277 VAC 50 Hz, 30 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
277	50.00	483.90	130.5400	0.9698	21.59

nth Order	mA Content	% Content	Limit >25 W	Remarks
1	556.00			
2	0.50	0.09%	2.00%	Pass
3	91.70	16.49%	29.09%	Pass
5	34.80	6.26%	10.00%	Pass
7	23.10	4.15%	7.00%	Pass
9	12.10	2.18%	5.00%	Pass
11	11.30	2.03%	3.00%	Pass
13	7.40	1.33%	3.00%	Pass
15	7.40	1.33%	3.00%	Pass
17	6.20	1.12%	3.00%	Pass
19	5.00	0.90%	3.00%	Pass
21	5.20	0.94%	3.00%	Pass
23	4.30	0.77%	3.00%	Pass
25	4.60	0.83%	3.00%	Pass
27	3.20	0.58%	3.00%	Pass
29	2.60	0.47%	3.00%	Pass
31	2.40	0.43%	3.00%	Pass
33	2.10	0.38%	3.00%	Pass
35	2.00	0.36%	3.00%	Pass
37	1.40	0.25%	3.00%	Pass
39	1.30	0.23%	3.00%	Pass
41	1.60	0.29%		
43	1.20	0.22%		
45	2.80	0.50%		
47	17.00	3.06%		
49	16.50	2.97%		

11.6.5 230 VAC 50 Hz, 33 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
277	50.00	562.10	152.4200	0.9744	20.32

nth Order	mA Content	% Content	Limit >25 W	Remarks
1	648.50			
2	1.00	0.15%	2.00%	Pass
3	101.60	15.67%	29.23%	Pass
5	36.70	5.66%	10.00%	Pass
7	25.30	3.90%	7.00%	Pass
9	11.90	1.84%	5.00%	Pass
11	12.10	1.87%	3.00%	Pass
13	7.70	1.19%	3.00%	Pass
15	8.30	1.28%	3.00%	Pass
17	5.80	0.89%	3.00%	Pass
19	4.50	0.69%	3.00%	Pass
21	4.70	0.72%	3.00%	Pass
23	3.60	0.56%	3.00%	Pass
25	3.80	0.59%	3.00%	Pass
27	2.90	0.45%	3.00%	Pass
29	2.50	0.39%	3.00%	Pass
31	2.30	0.35%	3.00%	Pass
33	1.90	0.29%	3.00%	Pass
35	2.00	0.31%	3.00%	Pass
37	1.70	0.26%	3.00%	Pass
39	1.60	0.25%	3.00%	Pass
41	1.50	0.23%		
43	1.70	0.26%		
45	3.70	0.57%		
47	17.70	2.73%		
49	16.00	2.47%		

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11.6.6 230 VAC 50 Hz, 36 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
277	50.00	592.90	161.0600	0.9759	19.83

nth Order	mA Content	% Content	Limit >25 W	Remarks
1	684.70			
2	0.80	0.12%	2.00%	Pass
3	104.80	15.31%	29.28%	Pass
5	37.30	5.45%	10.00%	Pass
7	26.00	3.80%	7.00%	Pass
9	12.20	1.78%	5.00%	Pass
11	12.20	1.78%	3.00%	Pass
13	11.50	1.68%	3.00%	Pass
15	6.00	0.88%	3.00%	Pass
17	6.00	0.88%	3.00%	Pass
19	4.20	0.61%	3.00%	Pass
21	4.70	0.69%	3.00%	Pass
23	3.80	0.55%	3.00%	Pass
25	3.80	0.55%	3.00%	Pass
27	3.00	0.44%	3.00%	Pass
29	2.70	0.39%	3.00%	Pass
31	2.40	0.35%	3.00%	Pass
33	2.20	0.32%	3.00%	Pass
35	2.00	0.29%	3.00%	Pass
37	1.90	0.28%	3.00%	Pass
39	1.70	0.25%	3.00%	Pass
41	1.80	0.26%		
43	1.50	0.22%		
45	3.80	0.55%		
47	16.90	2.47%		
49	17.40	2.54%		

12 Waveforms

12.1 Input Line Current

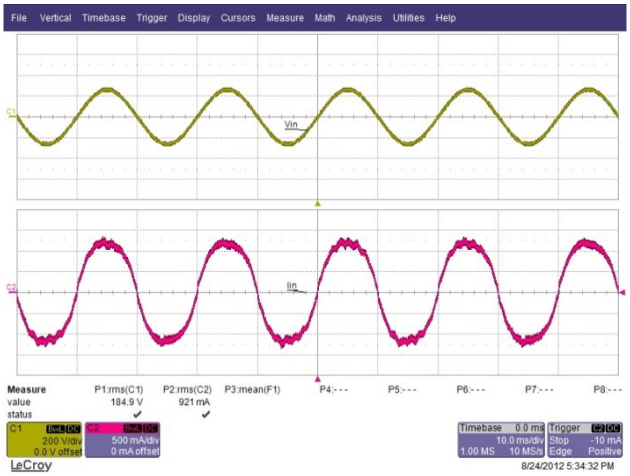

Figure 15 – 184 VAC 50 Hz, Full Load.
Upper: V_{IN}, 200 V
Lower: I_{IN}, 0.5 A / div.,10 ms / div.

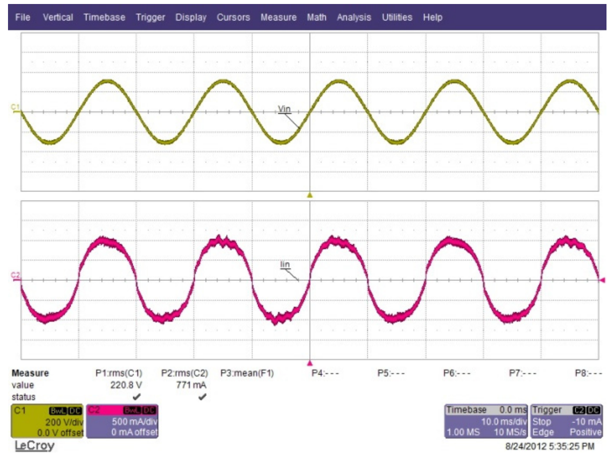

Figure 16 – 220 VAC 50 Hz, Full Load.
Upper: V_{IN}, 200 V
Lower: I_{IN}, 0.5 A / div.,10 ms / div.

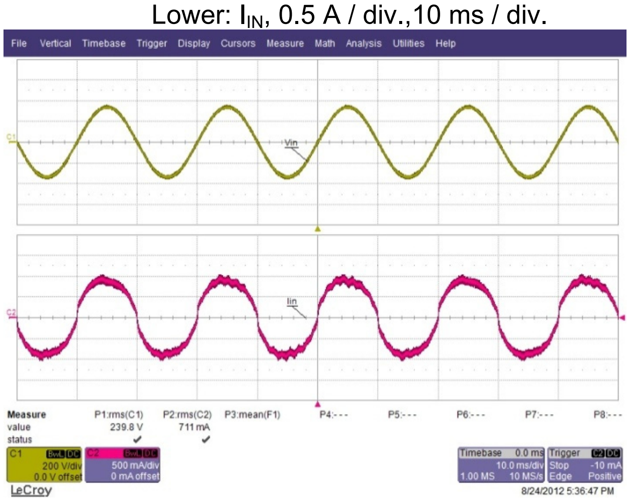

Figure 17 – 240 VAC 50 Hz, Full Load.
Upper: V_{IN}, 200 V
Lower: I_{IN}, 0.5 A / div.,10 ms / div.

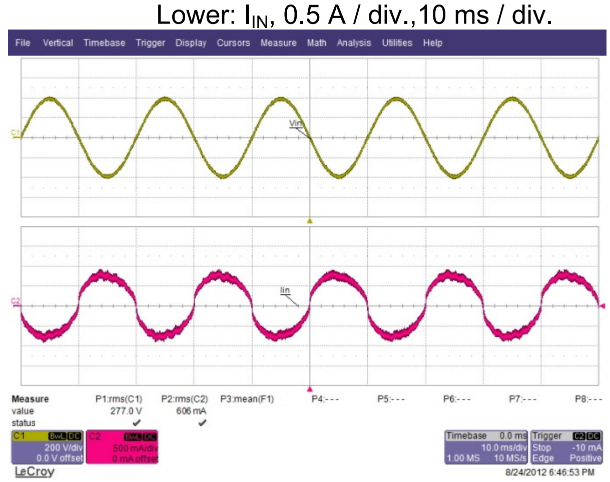

Figure 18 – 277 VAC 50 Hz, Full Load.
Upper: V_{IN}, 200 V
Lower: I_{IN}, 0.5 A / div.,10 ms / div.

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12.2 Drain Voltage and Current Normal Operation

Figure 19 – 184 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

Figure 20 – 277 VAC 50 Hz, Full Load.
Upper: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

12.3 Drain Voltage and Current Start-up Operation

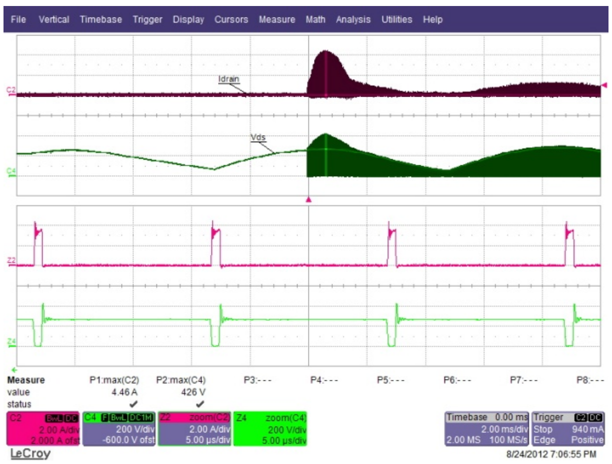

Figure 21 – 184 VAC 50 Hz., Full Load Start-up.
Upper: I_{DRAIN}, 2 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

Figure 22 – 277 VAC 50 Hz., Full Load Start-up.
Upper: I_{DRAIN}, 2 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

12.4 Output Current and Output Voltage

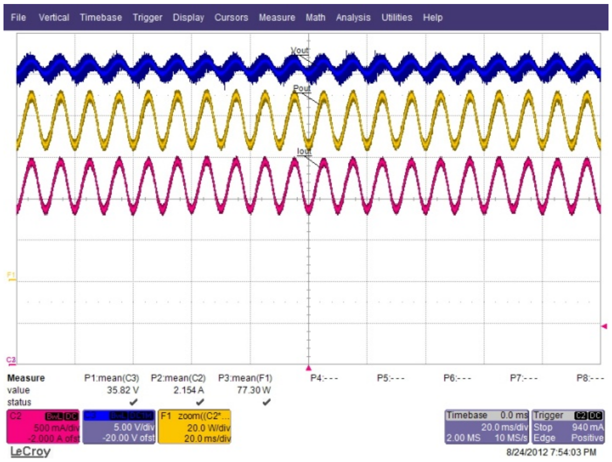

Figure 23 – 184 VAC 50 Hz., Max Load.
Upper: V_{OUT}, 5V / div.
Middle: P_{OUT}, 20W / div.
Lower: I_{OUT}, 500 mA / div.

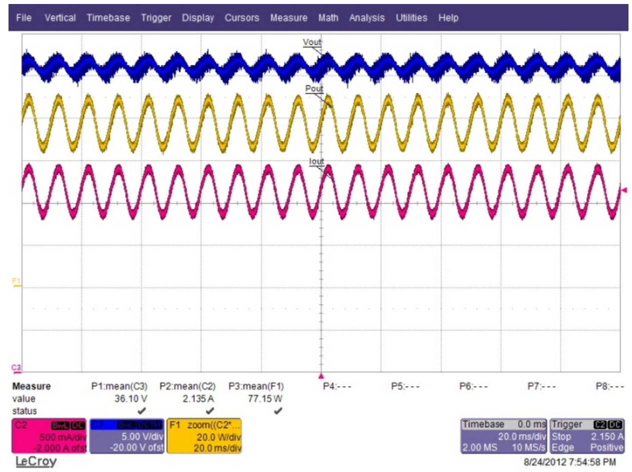

Figure 24 – 277 VAC 50 Hz., Max Load.
Upper: V_{OUT}, 5V / div.
Middle: P_{OUT}, 20W / div.
Lower: I_{OUT}, 500 mA / div.

12.5 Start-up Output Current and Voltage

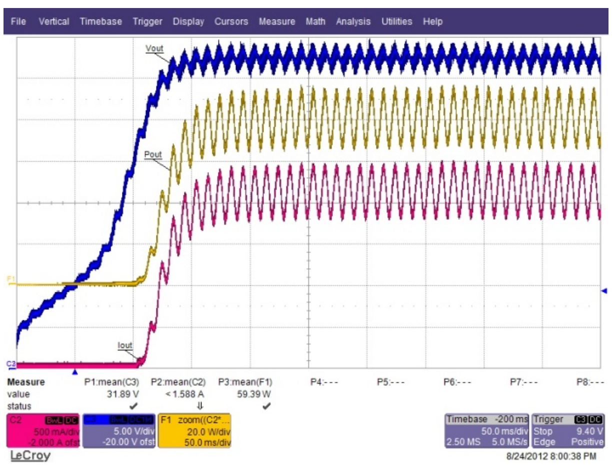

Figure 25 – 184 VAC 50 Hz, Output Rise.
Upper: V_{OUT}, 5V / div.
Middle: P_{OUT}, 20W / div.
Lower: I_{OUT}, 500 mA / div.

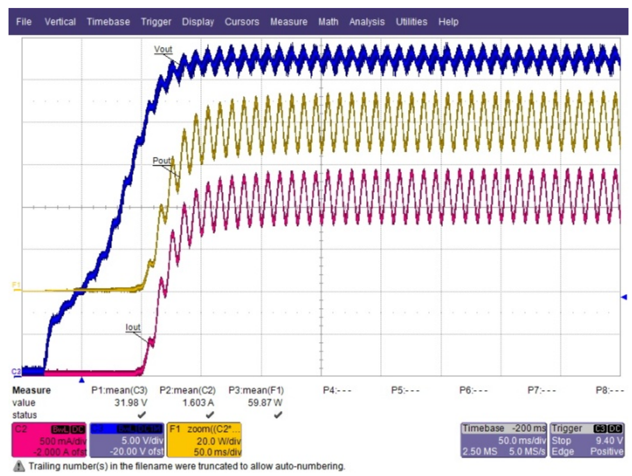

Figure 26 – 277 VAC 50 Hz, Output Rise.
Upper: V_{OUT}, 5V / div.
Middle: P_{OUT}, 20W / div.
Lower: I_{OUT}, 500 mA / div.

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12.6 Output Tracking at Power-up and Power-down

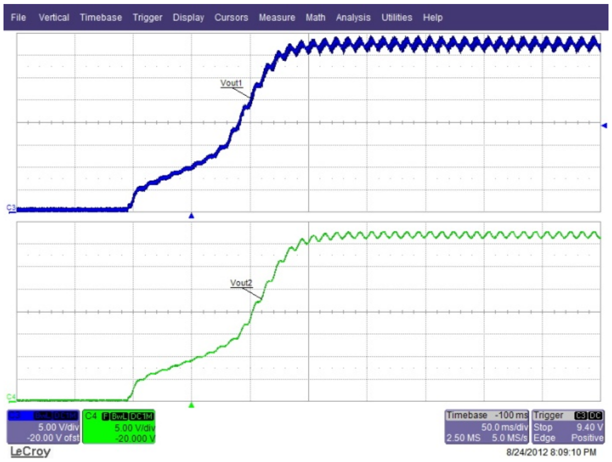

Figure 27 – 184 VAC 50 Hz, Power-up.
Upper: $V_{OUT-LED1}$, 5 V / div.
Lower: $V_{OUT-LED2}$, 5 V / div., 50ms / div.

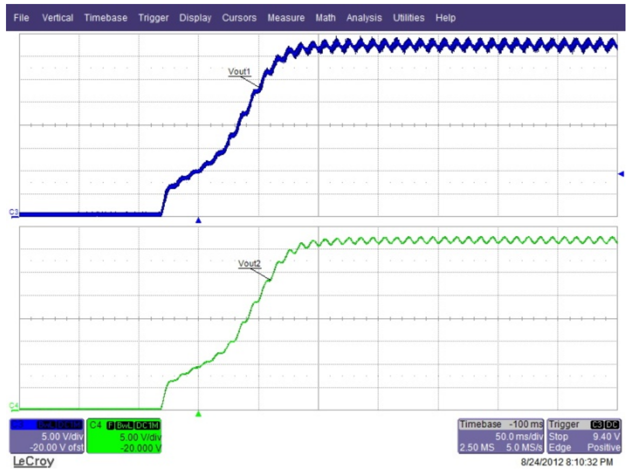

Figure 28 – 277 VAC 50 Hz, Power-down.
Upper: $V_{OUT-LED1}$, 5 V / div.
Lower: $V_{OUT-LED2}$, 5 V / div., 50ms / div.

12.7 Open Load Test

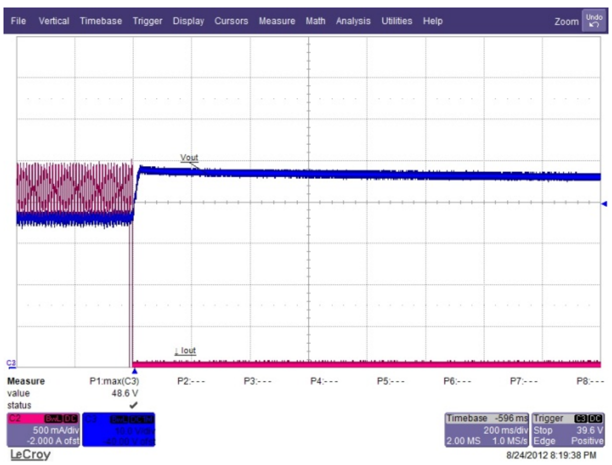

Figure 29 – 277 VAC 50 Hz, Output 1 Open.
Upper: $V_{OUT-LED1}$, 10 V / div.
Lower: $I_{OUT-LED1}$, 500 mA, 200 ms / div.

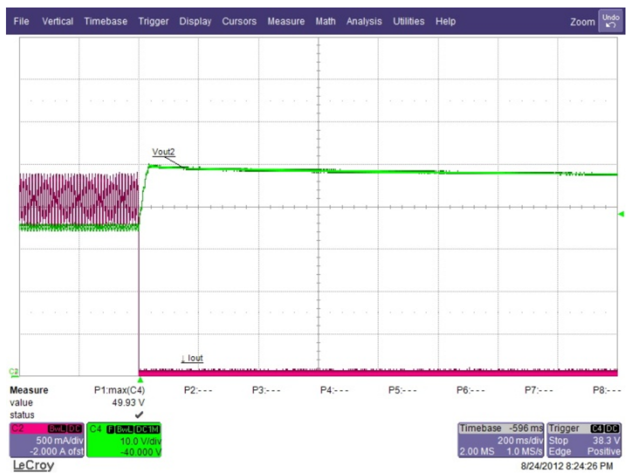

Figure 30 – 277 VAC 50 Hz, Output 2 Open.
Upper: $V_{OUT-LED1}$, 10 V / div.
Lower: $I_{OUT-LED1}$, 500 mA, 200 ms / div.

12.8 Output Rectifier Peak Inverse Voltage

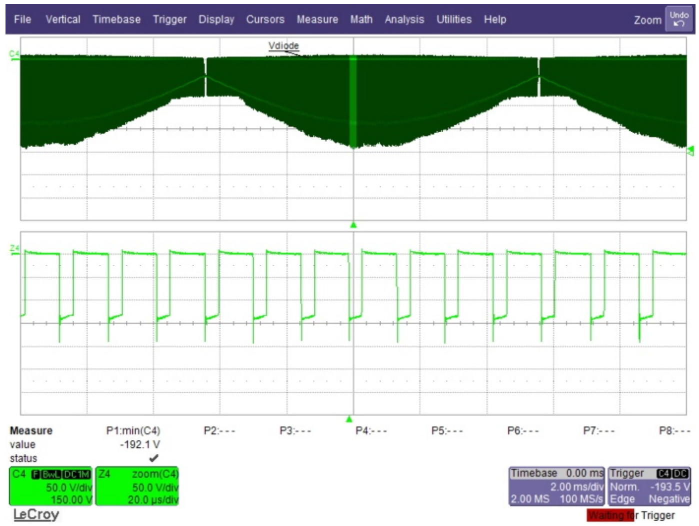

Figure 31 – 277 VAC 50 Hz, Output Short.
Lower: V_{PIV}, 50 V, 5 ms / div.

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13 Power Line Transient Test

The unit was subjected to ±2500 V, 100 kHz ring wave and ±2000 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2000	230	L1, L2	0	Surge (2Ω)	Pass
-2000	230	L1, L2	90	Surge (2Ω)	Pass
+2000	230	L1, L2	0	Surge (2Ω)	Pass
-2000	230	L1, L2	90	Surge (2Ω)	Pass

14 Thermal Measurements

Thermal performance was measured inside an enclosure with two 36 V LED loads with no airflow. The thermocouple was attached to the body of the components. Temperature stabilized after 2 hour.

DESCRIPTION	184 VAC / 50 Hz. (ºC)	230 VAC / 50 Hz. (ºC)	277 VAC / 50 Hz. (ºC)
Ambient Temperature	65	65	65
Input Bridge (BR1)	110.5	103.5	95.5
Transformer (T1)	78.6	81.3	82.6
Transformer (T2)	77.3	79.6	81.9
LNK-PH (U1)	119.7	116.3	114.2
LNK-PH (U2)	120.5	117.9	115.5
Output Diode (D17)	99.9	98.5	98
Output Diode (D9)	99.6	99.9	99.5
Output Diode (D16)	97.3	97.8	97.3
Output Diode (D8)	99.1	99	98.3
TVS (VR1)	110.9	105.2	102.7
TVS (VR4)	112.3	107.6	104
Block Diode (D3)	114.6	108.9	105.5
Block Diode (D11)	116.6	111.3	106.6

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15 Conducted EMI Measurements

15.1 Conducted EMI Test Set-up

The UUT is placed on a ground plane as shown below together with the LED load.

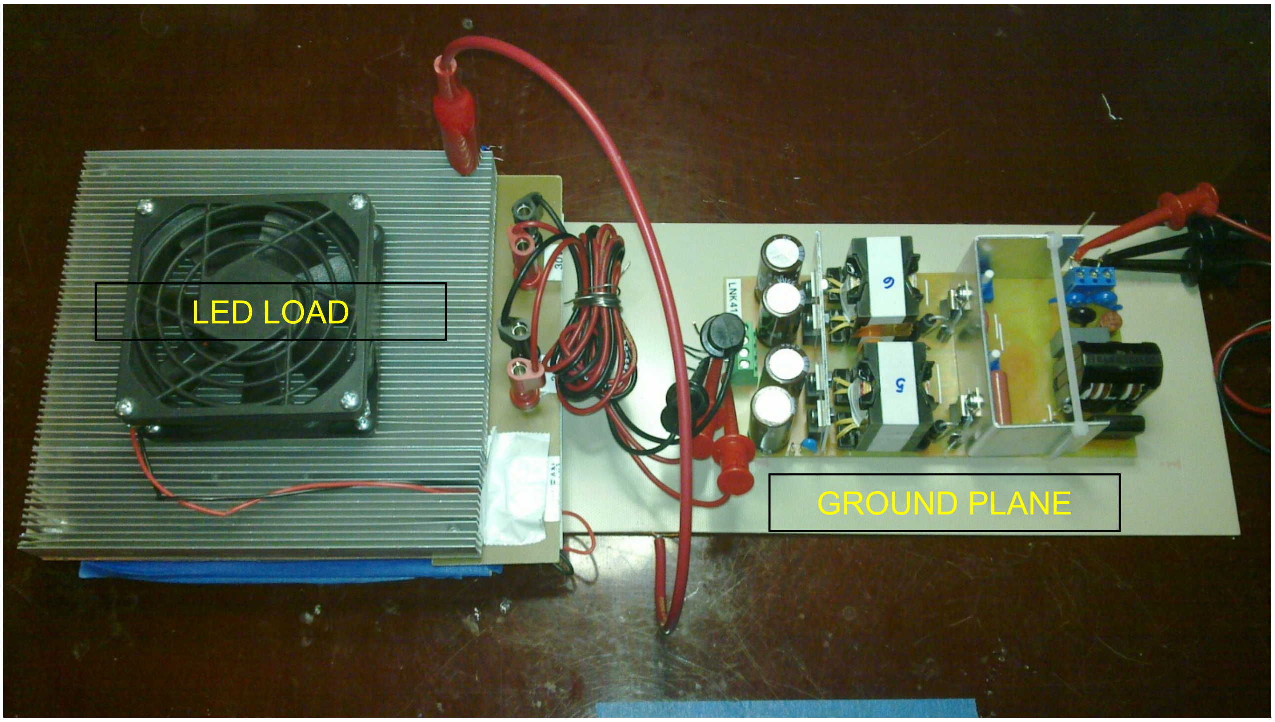

Figure 32 – EMI Measurement Set-up.

15.2 Conducted EMI Test Results

Figure 33 – 30 V LED Load, 230 VAC, 60 Hz, and EN55015 Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	64.5467705779 kHz	38.64	N gnd	
2	Average	67.8393045788 kHz	40.85	N gnd	
2	Average	126.977840157 kHz	48.68	L1 gnd	
2	Average	130.825395691 kHz	50.77	L1 gnd	
2	Average	133.454986145 kHz	55.87	N gnd	
2	Average	137.49880568 kHz	53.71	N gnd	
1	Quasi Peak	164.052790903 kHz	47.12	N gnd	-18.12
2	Average	165.693318812 kHz	40.45	L1 gnd	-14.71
2	Average	196.231331718 kHz	48.41	L1 gnd	-5.35
1	Quasi Peak	198.193645035 kHz	56.59	L1 gnd	-7.09
1	Quasi Peak	264.49018761 kHz	48.32	L1 gnd	-12.96
2	Average	264.49018761 kHz	39.23	L1 gnd	-12.05
1	Quasi Peak	332.507282579 kHz	45.25	L1 gnd	-14.13
1	Quasi Peak	397.727746704 kHz	40.49	L1 gnd	-17.40
1	Quasi Peak	598.084042089 kHz	39.43	L1 gnd	-16.56
1	Quasi Peak	7.71534368894 MHz	40.79	L1 gnd	-19.21
1	Quasi Peak	20.6619488204 MHz	52.62	N gnd	-7.37
2	Average	20.6619488204 MHz	44.60	N gnd	-5.39
1	Quasi Peak	28.9799739049 MHz	46.37	N gnd	-13.62

Figure 34 – Scan Summary at 30 V LED Load, 230 VAC, 60 Hz, and EN55015 Limits.

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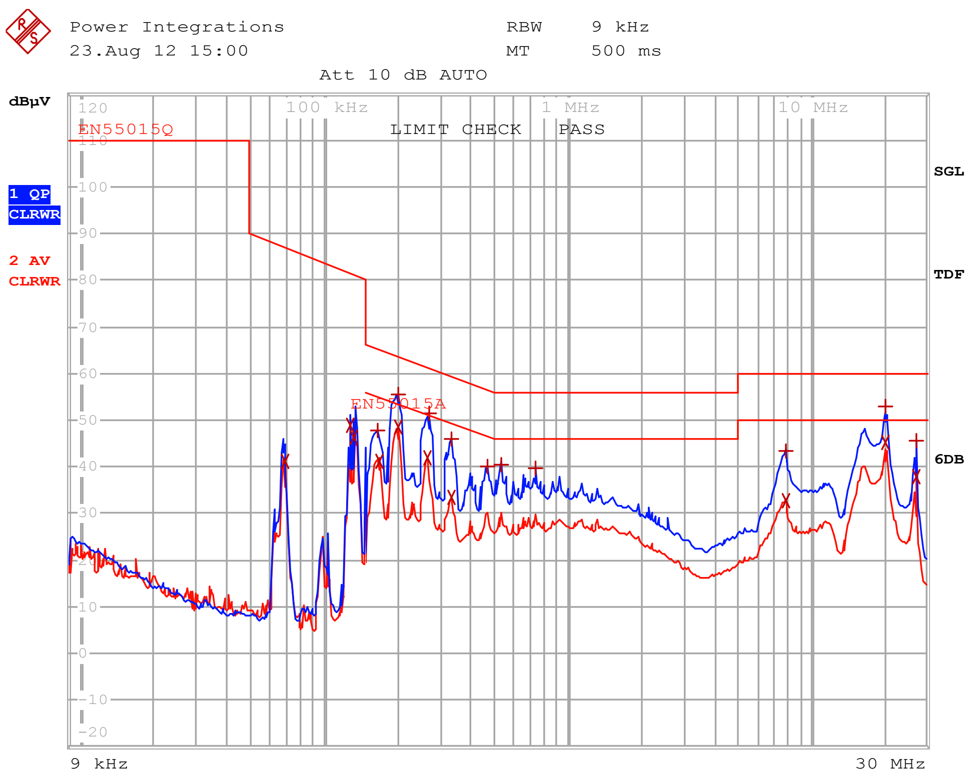

Figure 35 – Line Conducted EMI, 36 V LED Load, 230 VAC, 60 Hz, and EN55015 Limits

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	68.5176976246 kHz	41.29	L1 gnd	
2	Average	126.977840157 kHz	48.93	N gnd	
2	Average	132.133649648 kHz	46.48	N gnd	
1	Quasi Peak	164.052790903 kHz	47.91	L1 gnd	-17.34
2	Average	167.350252 kHz	41.25	L1 gnd	-13.83
1	Quasi Peak	200.175581485 kHz	55.59	N gnd	-8.00
2	Average	200.175581485 kHz	48.52	L1 gnd	-5.07
2	Average	264.49018761 kHz	41.74	L1 gnd	-9.54
1	Quasi Peak	267.135089486 kHz	51.30	L1 gnd	-9.90
1	Quasi Peak	332.507282579 kHz	46.06	L1 gnd	-13.32
2	Average	332.507282579 kHz	33.55	L1 gnd	-15.83
1	Quasi Peak	466.367062279 kHz	40.20	L1 gnd	-16.37
1	Quasi Peak	530.769219795 kHz	40.56	L1 gnd	-15.43
1	Quasi Peak	729.776191209 kHz	39.79	L1 gnd	-16.20
1	Quasi Peak	7.79249712583 MHz	43.47	L1 gnd	-16.52
2	Average	7.79249712583 MHz	32.54	L1 gnd	-17.45
1	Quasi Peak	20.2548268017 MHz	52.99	N gnd	-7.00
2	Average	20.2548268017 MHz	45.25	N gnd	-4.74
1	Quasi Peak	26.7625196891 MHz	45.70	N gnd	-14.29
2	Average	26.7625196891 MHz	37.87	N gnd	-12.12

Figure 36 – Scan Summary at 36 V LED Load, 230 VAC, 60 Hz, and EN55015 Limits.

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Nov-11	ME	1.0	Initial Release	Apps & Mktg
19-Oct-12	JDC	2.0	Updated Test Results for LNK420EG	Apps & Mktg

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