Application Note AN-72
InnoSwitch3 Family

Design Guide

Introduction

InnoSwitch™3 devices combine a high-voltage power MOSFET / PowiGaN switch, with both primary-side and secondary-side controllers, an innovative high-speed magneto-coupling communications technology and a synchronous rectification driver into one isolated, safety-rated device. The incorporation of Fluxlink™, which transmits information safely and reliably across the isolation barrier, eliminates the need for an optocoupler – used in the feedback loop of conventional power conversion circuits. This reduces component count and eliminates the lifetime and reliability limitations inherent in opto feedback devices. The InnoSwitch3 integrated circuits feature a variable frequency, variable peak-current control scheme which together with quasi-resonant switching and synchronous rectification ensure very high conversion efficiency across the load range. The family can be used to create power supplies up to 100 W output, including CV/CC chargers that easily meet average-power-supply-efficiency requirements and offers very low no load input power and outstanding standby performance. Power Integrations' EcoSmart™ technology used in InnoSwitch3 ICs enables designs that consume as little as 15 mW of no-load power and makes the family ideal for applications that must meet energy efficiency standards such as the United States Department of Energy DoE 6, California Energy Commission (CEC) and European Code of Conduct.

The primary-side flyback controller in InnoSwitch3 can seamlessly transition between DCM, QR and CCM switching. The primary controller consists of start-up circuitry, a frequency jitter oscillator, a receiver circuit that is magnetically coupled to the secondary side, a current limit controller, audible noise reduction engine, overvoltage detection circuitry, lossless input line sensing circuit, over-temperature protection and a 650 V or 725 V power MOSFET / 750 V PowiGan.

The InnoSwitch3 secondary controller consists of a transmitter circuit that is magnetically coupled to the primary-side, a constant voltage (CV) and constant current (CC) control circuit, synchronous-rectifier-MOSFET driver, QR mode circuit, and a host of integrated protection features including output overvoltage, overload, power limit, and hysteretic thermal overload protection.

At start-up the primary controller is limited to a maximum switching frequency of 25 kHz and 70% of the maximum programmed current limit. An auto-restart function limits power dissipation in the switching MOSFET / PowiGaN, transformer, and output SR MOFET during overload, short-circuit or open-loop fault conditions.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a flyback power supply designed using InnoSwitch3. Different output power levels may require different values for some circuit components, but the general circuit configuration remains similar. Advanced features such as line overvoltage and undervoltage protection, primary or secondary sensed output overvoltage protection and constant current limit programming are implemented using very few passive components.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step by step design approach described later, and can use the following information to quickly design the transformer and select the components for a first prototype. For this approach, only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet line numbers are provided in square brackets [line reference].

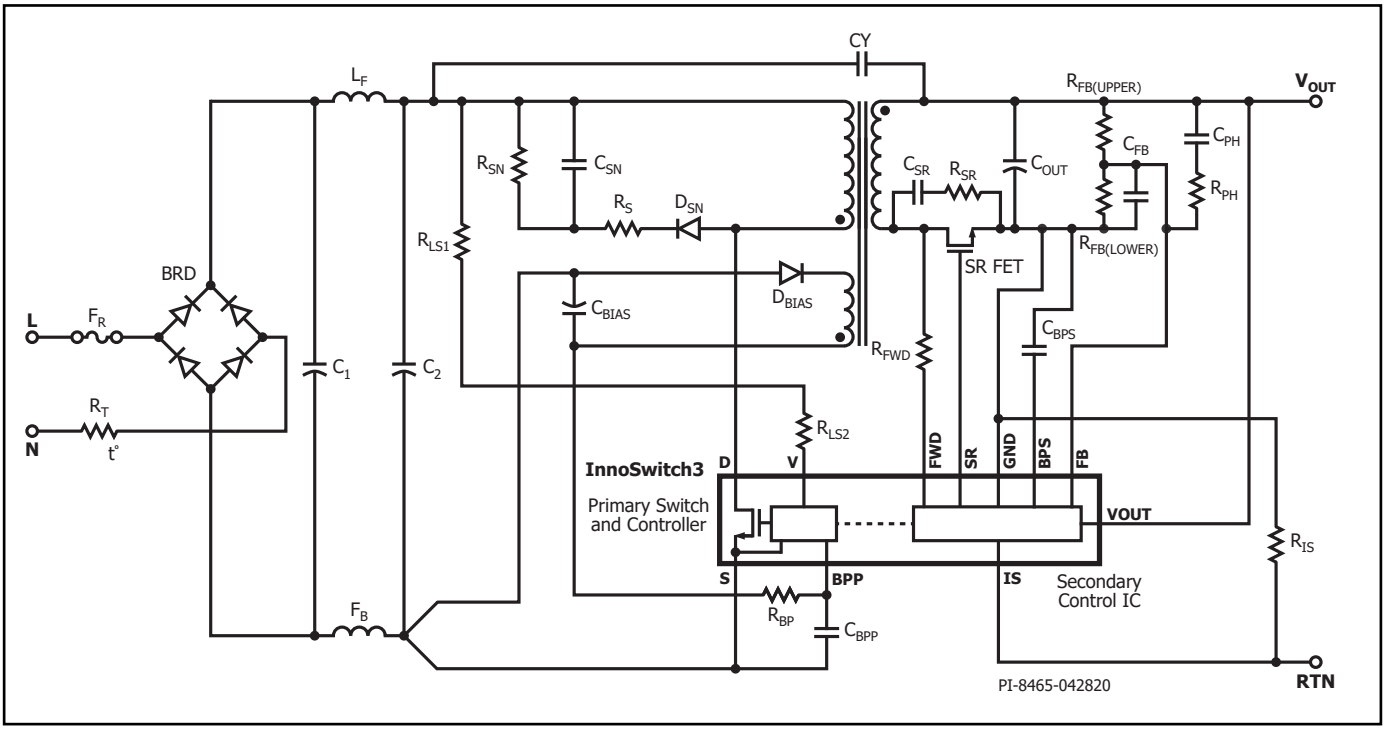


Figure 1. Typical Adapter Power Supply Schematic using InnoSwitch3 with Line Undervoltage Lockout, Line Overvoltage Shutdown, Constant Output Current Limit and Quasi-Resonant Synchronous MOSFET Rectifier and Integrated Output Overvoltage Protection.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply or charger using the InnoSwitch3 family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To help simplify the task, this application note refers directly to the PIXls designer spreadsheet that is part of the PI Expert™ design software suite available online (https://piexpertonline.power.com/site/login). The basic configuration used in InnoSwitch3 flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identification used in the description throughout this application note.

In addition to this application note, there is the InnoSwitch3 reference design kit (RDK) containing an engineering prototype board as well as device samples that provides an example of a working power supply. Further details on downloading PI Expert, obtaining an RDK and updates to this document can be found at www.power.com.

- Enter AC input voltage range and line frequency, VAC_MIN [B3], VAC_MAX [B4], LINEFREQ [B6]
- Enter input capacitance, CAP_INPUT [B7]
  - 3 µF / W for universal (85-265 VAC) or single (100/115 VAC) line. A more aggressive value of 2 µF / W can be used for many charger designs that do not need to meet hold up time requirement
  - Use 1 µF/W for 230 VAC or for single (185-265 VAC) line. If this cell is left blank then the capacitance value for a VMIN of 70 V (universal input) or 150 V (single 230 VAC) is calculated. Often this will lead to an optimal input filter capacitance value
- Enter nominal output voltage, VOUT [B8]
- Enter desired cable drop compensation, PERCENT_CDC [B9]
  - "0%" for no cable compensation
  - "1% - 6%" for featured H-code trim
- Enter continuous output current, IOUT [B10]
- Enter efficiency estimate, EFFICIENCY [B12]
  - 0.83 for universal input voltage (85-265 VAC) or single 100/115 VAC (85-132 VAC) and 0.85 for a single 230 VAC (185-265 VAC) design. Adjust the number accordingly after measuring the efficiency of the first prototype-board at max load and VACMIN

- Select power supply enclosure, ENCLOSURE [B14]
- Select current limit mode, ILIMIT_MODE [B19]
  - Two current limit configurations are available, STANDARD or INCREASED
- Select InnoSwitch3 from drop-down list or enter directly [B20]
  - Select the device from Table 1 according to output power, input voltage and application
    - InnoSwitch3-CE for CV/CC flyback application
    - InnoSwitch3-EP for CV/CC flyback application with 725 V MOSFET
- Enter desired maximum switching frequency at full load, FSWITCHING_MAX [B34]
- Enter desired reflected output voltage, VOR [B35]
- Enter core type (if desired), CORE [B63] from drop down menu
  - Suggested core size will be selected automatically if none is entered [B63]
  - For custom core, enter CORE CODE [B64], and core parameters from [B65] to [B72]
- Enter secondary number of turns [B88]

If any warnings are generated, make changes to the design by following instructions in spreadsheet column D.

- Build transformer as suggested in "Transformer Construction" tab
- Select key components
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency, V_{MIN}). Note that the initial efficiency estimate is very conservative.

Output Power Table

Product[3]	230 VAC ± 15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
INN3162C	10 W	12 W	10 W	10 W
INN3163C	12 W	15 W	12 W	12 W
INN3164C	20 W	25 W	15 W	20 W
INN3165C	25 W	30 W	22 W	25 W
INN3166C	35 W	40 W	27 W	36 W
INN3167C	45 W	50 W	40 W	45 W
INN3168C	55 W	65 W	50 W	55 W

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Minimum peak power capability.
3. Package: InSOP-24D.

Output Power Table

Product[3]	230 VAC ± 15%		85-265 VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
INN3264C/3274C	20 W	25 W	15 W	20 W
INN3265C/3275C	25 W	30 W	22 W	25 W
INN3266C/3276C	35 W	40 W	27 W	36 W
INN3277C	40 W	45 W	36 W	40 W
INN3267C	45 W	50 W	40 W	45 W
INN3268C	55 W	55 W	50 W	55 W
INN3278C	70 W	75 W	55 W	65 W
INN3279C	80 W	85 W	65 W	75 W
INN3270C	90 W	100 W	75 W	85 W

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 40 °C ambient. (package temperature <125 °C).
2. Minimum peak power capability.
3. Package: InSOP-24D.
4. INN326x – 650 V MOSFET, INN3274-77 – 725 V MOSFET, INN3278 / INN3279 / INN3270 – 750 V PowiGaN switch.

Output Power Table

Product[3]	230 VAC ± 15%	85-265 VAC
	Peak or Open Frame[1,2]	Peak or Open Frame[1,2]
INN3672C	12 W	10 W
INN3673C	15 W	12 W
INN3674C	25 W	20 W
INN3675C	30 W	25 W
INN3676C	40 W	36 W
INN3677C	45 W	40 W
Product[3]	750 V PowiGaN Switch	
	230 VAC ± 15%	85-265 VAC
	Peak or Open Frame[1,2]	Peak or Open Frame[1,2]
INN3678C	75 W	65 W
INN3679C	85 W	75 W
INN3670C	100 W	85 W
Product[3]	900 V MOSFET	
	230 VAC ± 15%	85-265 VAC
	Peak or Open Frame[1,2]	Peak or Open Frame[1,2]
INN3692C	12 W	10 W
INN3694C	25 W	20 W
INN3696C	35 W	30 W

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Minimum peak power capability.
3. Package: InSOP-24D.

Table 1. Output Power Tables of InnoSwitch3-CE, CP and EP.

Step-by-Step Design Procedure

This design procedure uses the PI Expert design software (available from Power Integrations), which automatically performs the key calculations required for an InnoSwitch3 flyback power supply design. PI Expert allows designers to avoid the typical highly iterative design process. Look-up tables and empirical design guidelines are provided in this procedure where appropriate to simplify the design task.

Iterate the design to eliminate warnings. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Once all warnings have been cleared, the output transformer design parameters can be used to create a prototype transformer.

Step 1 – Application Variables

Enter: VIN_MIN, VIN_MAX, LINEFREQ, CAP_INPUT, VOUT, PERCENT_CDC, IOUT, EFFICIENCY, FACTOR_Z, and ENCLOSURE

Minimum and Maximum Input Voltage, V_MIN, V_MAX (VAC)
Determine the input voltage range from Table 2 for a particular regional requirement.

Line Frequency, LINEFREQ (Hz)
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst-case or based on the product specification reduce these numbers by 6% (47 Hz or 56 Hz).

Total Input Capacitance, CAP_INPUT (µF)
Enter total input capacitance using Table 3 for guidance.

2	APPLICATION VARIABLES					Design Title
3	VIN_MIN	**85**		85	V	Minimum AC input voltage
4	VIN_MAX	**265**		265	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT			40.0	uF	Input capacitor
8	VOUT	**5.00**		5.00	V	Output voltage at the board
9	PERCENT_CDC	**0%**		0%		Percentage (of output voltage) cable drop compensation desired at full load
10	IOUT	**4.00**		4.00	A	Output current
11	POUT			20.00	W	Output power
12	EFFICIENCY	**0.89**		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	**ADAPTER**		ADAPTER		Power supply enclosure

Figure 2. Application Variable Section of InnoSwitch3-CE Design Spreadsheet with Gray Override Cells.

Region	Nominal Input Voltage (VAC)	Minimum Input Voltage (VAC)	Maximum Input Voltage (VAC)	Nominal Line Frequency (Hz)
Japan	100	85	132	50 / 60
United States, Canada	120	90	132	60
Australia, China, European Union Countries, India, Korea, Malaysia, Russia	230	185	265	50
Indonesia, Thailand, Vietnam	220	185	265	50
Rest of Europe, Asia, Africa, Americas and rest of the world	115, 120, 127	90	155	50 / 60
	220, 230	185	265	50 / 60
	240	185	265	50

Visit: https://en.wikipedia.org/wiki/Mains_electricity_by_country

Table 2. Standard Worldwide Input Line Voltage Ranges and Line Frequencies.

	Total Input Capacitance per Watt of Output Power (µF/W)	Total Input Capacitance per Watt of Output Power (µF/W)
AC Input Voltage (VAC)	Full Wave Rectification	
	Adapter with hold-up time requirement	Open Frame or Charger/Adapter without hold-up time requirement
100 / 115	3	2
230	1	1
85-265	3	2

Table 3. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, VMIN > 70 V.

Nominal Output Voltage, VOUT (V)
Enter the nominal output voltage of the main output at full load. Usually the main output is the output from which feedback is derived.

Cable Compensation, PERCENT_CDC (%)
Select the appropriate cable compensation depending on the choice of cable for the design. If this power supply is not supplied with a cable, use the default 0%. (For InnoSwitch3-EP, this feature is not available)

Power Supply Output Current, IOUT (A)
This is the maximum continuous load current of the power supply.

Output Power, POUT (W)
This is a calculated value and will be automatically adjusted based on cable compensation selected.

Power Supply Efficiency, EFFICIENCY (η)
Enter the estimated efficiency of the complete power supply measured from the input and output terminals under peak load conditions and worst-case line (generally lowest input voltage). The table below can be used as a reference. Once a prototype has been constructed then the measured efficiency should be entered and further transformer iteration(s) can be performed if required.

Power Supply Loss Allocation Factor, FACTOR_ Z
This factor describes the apportioning of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency to determine the actual power that must be delivered by the power stage. For example losses in the input stage (EMI filter, rectification etc) are not processed by the power stage (transferred through the transformer) and therefore although they reduce efficiency the transformer design is not effected.

$$Z = \frac{\text{Secondary Losses}}{\text{Total Losses}}$$

For designs that do not have a peak power requirement, a value of 0.5 is recommended. For designs with a peak power requirement enter 0.65. The higher number indicates larger secondary side losses.

Enclosure
Power device selection will also be dependent on the application environment. For an open frame application where the operating ambient temperature is lower than in an enclosed adapter, the PIXIs will suggest a smaller device for the same output power.

Efficiency is also a function of output power, low power designs are most likely around 84% to 85% efficient, whereas with a synchronous rectifier (SR) the efficiency would reach 90% typically.

Nominal Output Voltage (VOUT)	Typical Low-Line Range		Typical Universal Range		Typical High-Line Range	
	85 VAC - 132 VAC		85 VAC - 265 VAC		185 VAC - 265 VAC	
	Schottky Diode Rectifier	Synchronous Rectifier	Schottky Diode Rectifier	Synchronous Rectifier	Schottky Diode Rectifier	Synchronous Rectifier
5	0.84	0.87	0.84	0.88	0.87	0.89
12	0.86	0.90	0.86	0.90	0.88	0.90

Table 4. Efficiency Estimate Without Output Cable .

Step 2 – Primary Controller Selection

Enter: Device Current Limit mode, ILIMIT and Generic Device Code, DEVICE_GENERIC

18	PRIMARY CONTROLLER SELECTION					
19	ILIMIT_MODE	**STANDARD**		STANDARD		Device current limit mode
20	DEVICE_GENERIC	**Auto**		INN31X5		Generic device code
21	DEVICE_CODE			INN3165C		Actual device code
22	POUT_MAX			22	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			3.47	Ω	Primary MOSFET on time drain resistance at 100 degC
24	ILIMIT_MIN			0.88	A	Minimum current limit of the primary MOSFET
25	ILIMIT_TYP			0.95	A	Typical current limit of the primary MOSFET
26	ILIMIT_MAX			1.02	A	Maximum current limit of the primary MOSFET
27	VDRAIN_BREAKDOWN			650	V	Device breakdown voltage
28	VDRAIN_ON_MOSFET			0.87	V	Primary MOSFET on time drain voltage
29	VDRAIN_OFF_MOSFET			508.4	V	Peak drain voltage on the primary MOSFET during turn-off

Figure 3. Primary Controller Selection of InnoSwitch3-CE Design Spreadsheet with Current Limit Mode Selection.

Generic Device Code, DEVICE_GENERIC
The default option is automatically selected based on input voltage range, maximum output power and application (i.e. adapter or open frame).

For manual selection of device size, refer to the InnoSwitch3 power table in the data sheet and select a device based on the peak output power. Then compare the continuous power to adapter column numbers in the power table, (if the power supply is of fully enclosed type), or compare to the open-frame column (if the power supply is an open-frame design). If the continuous power exceeds the value given in the power table (Table 1), then the next larger device should be selected. Similarly, if the continuous power is close to the maximum adapter power given in the power table, it may be necessary to switch to a larger device based on the measured thermal performance of the prototype.

Device Current Limit Mode, ILIMIT_MODE
For designs where thermals are not as challenging (such as open frame applications) and lowest cost is a critical requirement, ILIMIT MODE allows the choice of an INCREASED current limit mode, this will set the peak current of the device equivalent to the next bigger device's current limit and allow higher output power. By default, ILIMIT is set to STANDARD.

On-Time Drain Voltage, VDRAIN_ON_MOSFET (V)
This parameter is calculated based on RDSON_100DEG and primary RMS current.

Drain Peak Voltage, VDRAIN_OFF_MOSFET (V)
This parameter is the assumed Drain voltage seen by the device during off-time. The calculation assumes 10% minimum margin from the breakdown voltage rating of the internal MOSFET and gives a warning if this is exceeded.

$VDRAIN < (VIN\_MAX * 1.414) + VOR + VLK_{PRI} - (BV_{DSS} \times 10\%)$.

VLK_{PRI} is the voltage induced by the leakage inductance of the transformer when MOSFET turns off.

Other electrical parameters are displayed based from the data sheet, **RDSON_100DEG, ILIMIT_MIN, ILIMIT_TYP, ILIMIT_MAX, VDRAIN_BREAKDOWN.**

Step 3 – Worst-Case Electrical Parameters

Enter: FSWITCHING_MAX, VOR and LPRIMARY_TOL, or VMIN

33	WORST CASE ELECTRICAL PARAMETERS					
34	FSWITCHING_MAX	80000		80000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR			65.0	V	Seconday voltage reflected to the primary when the primary MOSFET turns off
36	VMIN			85.95	V	Valley of the rectified minimum AC input voltage at full power
37	KP			0.66		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			CCM		Mode of operation
39	DUTYCYCLE			0.433		Primary MOSFET duty cycle
40	TIME_ON			7.46	us	Primary MOSFET on-time
41	TIME_OFF			7.09	us	Primary MOSFET off-time
42	LPRIMARY_MIN			805.6	uH	Minimum primary inductance
43	LPRIMARY_TYP			830.5	uH	Typical primary inductance
44	LPRIMARY_TOL	3.0		3.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			855.4	uH	Maximum primary inductance
46						
47	PRIMARY CURRENT					
48	IPEAK_PRIMARY			0.95	A	Primary MOSFET peak currrent
49	IPEDESTAL_PRIMARY			0.30	A	Primary MOSFET current pedestal
50	IAVG_PRIMARY			0.25	A	Primary MOSFET average current
51	IRIPPLE_PRIMARY			0.76	A	Primary MOSFET ripple current
52	IRMS_PRIMARY			0.41	A	Primary MOSFET RMS current
53						
54	SECONDARY CURRENT					
55	IPEAK_SECONDARY			12.24	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			3.79	A	Secondary winding current pedestal
57	IRMS_SECONDARY			6.44	A	Secondary winding RMS current

Figure 4. Worst-Case Electrical Parameters Section of InnoSwitch3-CE Design Spreadsheet with Gray Override Cells.

Switching Frequency, FSWITCHING_MAX (Hz)

This parameter is the switching frequency at full load at minimum rectified AC input voltage. The maximum switching frequency of InnoSwitch3 in normal operation is 100 kHz, and the typical overload detection frequency of is 110 kHz. In normal operating condition, the switching frequency at full load should not be close to the overload detection frequency.

The programmable switching frequency range is 25 to 95 kHz, but it should be continued that the average frequency accounting for primary inductance and peak current tolerances does not result in average frequency higher than 110 kHz as this will trigger auto-restart due to overload. Pushing frequency higher to reduce transformer size is advisable, but Table 5 provides the suggested frequency based on the size of the internal high-voltage MOSFET, and represents the best compromise to balance overall device losses (i.e. conduction and switching losses).

InnoSwitch3 Family	Maximum Switching Frequency
INN3264C/3274C	85 - 90 kHz
INN3265C/3275C	80 kHz
INN3266C/3276C	75 kHz
INN3277C	70 kHz
INN3267C	65 kHz
PowiGaN device INN3278	70 kHz
PowiGaN device INN3279	65 kHz
PowiGaN device INN3270	60 kHz

Table 5. Suggested Maximum Switching Frequency.

Reflected Output Voltage, VOR (V)

This parameter is the secondary winding voltage during the diode / Synchronous Rectifier MOSFET (SR FET) conduction-time reflected back to the primary through the turns ratio of the transformer. Table 6 provides suggested values of VOR. VOR can be adjusted to achieve a design that does not violate design rules for the transformer and SR FET while simultaneously achieving sufficiently low Drain-Source voltage of the primary side MOSFET. VOR can be adjusted as necessary to ensure that no warnings in the spreadsheet are triggered. For design optimization purposes, the following factors should be considered,

- Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery from a given.

- Higher VOR reduces the voltage stress on the output diodes and SR FETs, which in some cases may allow a lower voltage rating for higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary-side which may increase secondary side copper, diode and SR FET losses thereby reducing efficiency.

It should be noted that there are exceptions to this guidance especially for very high output currents where the VOR should be reduced to obtain highest efficiency. Higher output voltages (above 15 V) should employ a higher VOR to maintain acceptable peak inverse voltage (PIV) across the output SR FET.

Optimal selection of the VOR value depends on the specific application and is based on a compromise between the factors mentioned above.

Output Voltage	Suggested VOR Value	Suggested Range
5 V	55 V	45 V - 60 V
9 V	85 V	80 V - 90 V
12 V - 20 V	110 V	100 V - 120 V

Table 6. Suggested VOR Values for Power MOSFET Devices.

Mode of Operation, K_P

K_P is a measure of how discontinuous or continuous the mode of switching is. $K_P > 1$ is said to be in discontinuous operation (DCM), while $K_P < 1$ denotes continuous operation (CCM).

Ripple to Peak Current Ratio, K_P

Below 1 (indicating continuous conduction mode), K_P is the ratio of ripple to peak primary current (Figure 5).

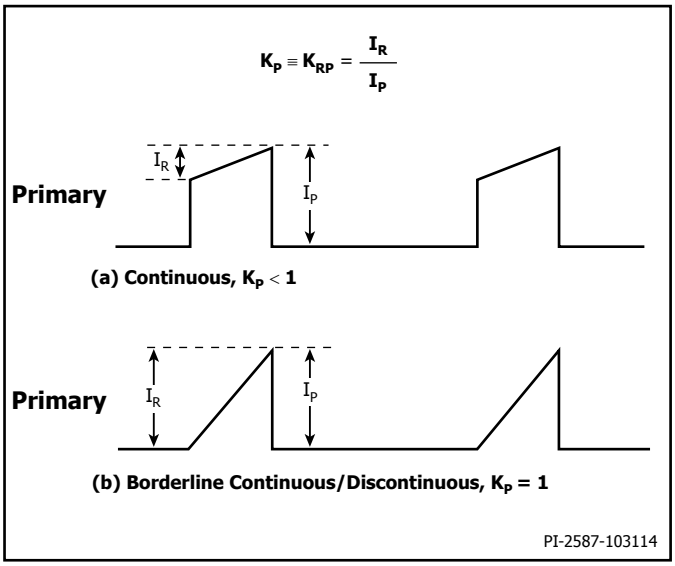


Figure 5. Continuous Mode Current Waveform, $K_P \leq 1$.

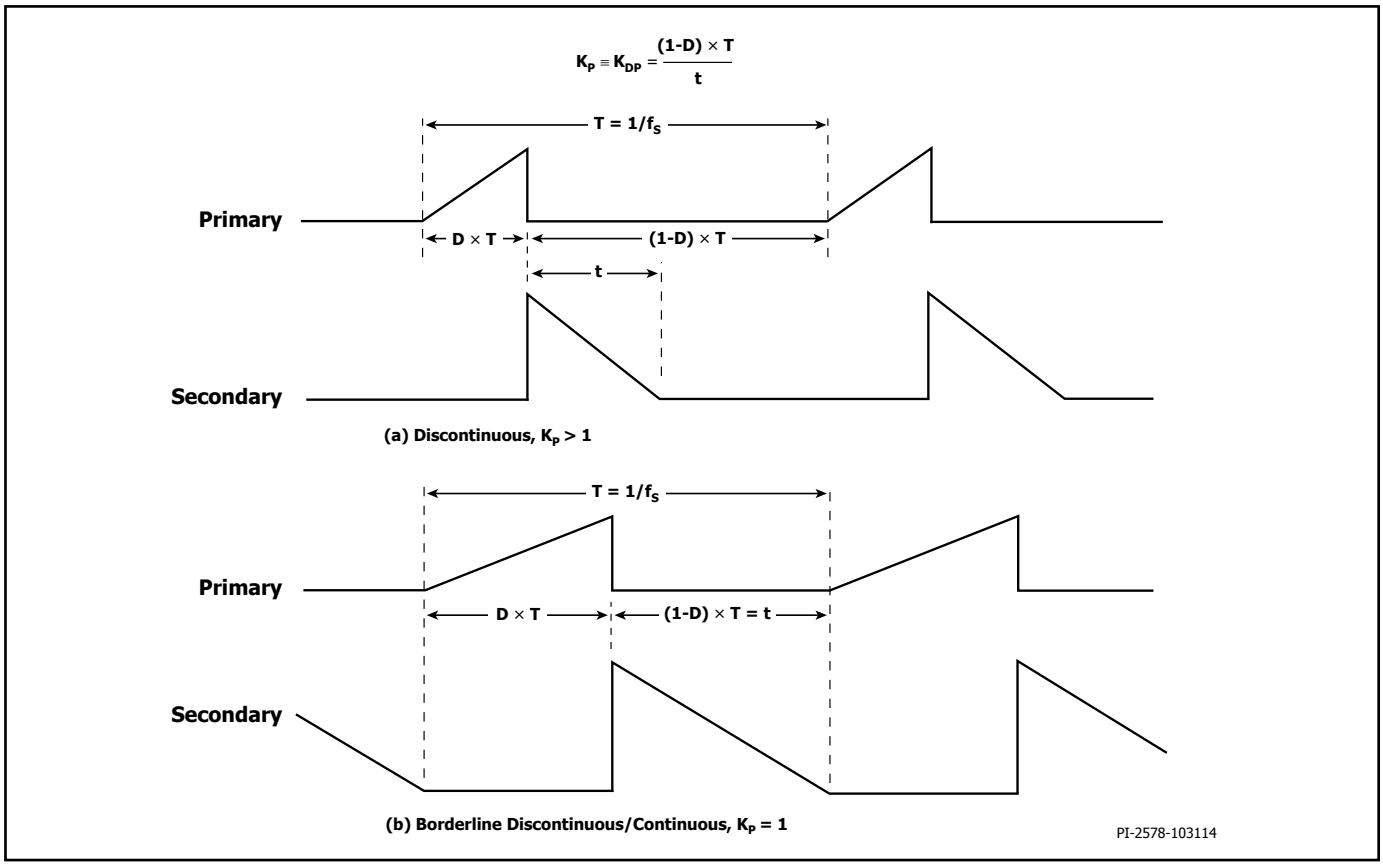


Figure 6. Discontinuous Mode Current Waveform, $K_P \geq 1$.

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

Above a value of 1, indicating discontinuous conduction mode, K_P is the ratio of primary MOSFET off time to the secondary SR_FET conduction time.

$$K_P \equiv K_{DP} = \frac{(1 - D) \times T}{t}$$
$$= \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

The value of K_P should be in the range of $0.5 < K_P < 6$. Guidance is given in the comments cell if the value of K_P is outside this range.

Experience has shown that a K_P value between 0.8 and 1 will result in higher efficiency by ensuring DCM or critical mode operation (CRM) which is desirable for most charger designs.

The spreadsheet will calculate the values of peak primary current, primary RMS current, primary ripple current, primary average current, and the maximum duty cycle for the design based on the selection of the these parameters.

Typical Primary Inductance, LPRIMARY_TYP (µH)
This is the typical transformer primary inductance target.

Primary Inductance Tolerance, LPRIMARY_TOL (%)
This parameter is the assumed primary inductance tolerance. A value of 7% is used by default, however if specific information is provided from the transformer vendor, then this may be entered in the grey override cell. A value of 7% helps to reduce unit-to-unit variation and is easy to meet for most magnetics vendors. A value of 3% will help improve production tolerance further but will be more challenging to vendors.

The other important electrical parameters are automatically calculated by the spreadsheet. These can used to appropriately select the other components in the circuit, such as input fuse (F_R) and EMI filter (L_F), bridge rectifiers (B_{RD}), output rectifiers (SR_{FET}) and capacitors (C_{OUT}), as described in Figure 1.

PRIMARY CURRENT
IPEAK_PRIMARY – Peak primary current
IPEDESTAL_PRIMARY – Primary MOSFET current pedestal in CCM mode
IAVG_PRIMARY – Primary MOSFET average current
IRIPPLE_PRIMARY – Primary MOSFET ripple current
IRMS_PRIMARY – Primary MOSFET RMS current

SECONDARY CURRENT
IPEAK_SECONDARY – Peak secondary current
IPEDESTAL_SECONDARY – Secondary winding current pedestal
IRMS_SECONDARY – Secondary winding RMS current

Minimum Rectified Input Voltage, VMIN
Valley of the rectified minimum AC input voltage at full power is calculated based on input capacitance (CAP_INPUT).

Step 4 – Transformer Construction Parameters

Enter: CORE, AE, LE, AL, VE, BOBBIN, AW, BW, MARGIN
Choose Core and Bobbin based on maximum output power.

61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	**CORE SELECTION**					
63	CORE	**RM6**	Info	RM6		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
64	CORE CODE			PC95RM06Z		Core code
65	AE			37.00	mm^2	Core cross sectional area
66	LE			29.20	mm	Core magnetic path length
67	AL			2150	nH/turns^2	Ungapped core effective inductance
68	VE			1090.0	mm^3	Core volume
69	BOBBIN			B-RM06-V		Bobbin
70	AW			15.52	mm^2	Window area of the bobbin
71	BW			6.20	mm	Bobbin width
72	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
73						
74	**PRIMARY WINDING**					
75	NPRIMARY			77		Primary turns
76	BPEAK			3125	Gauss	Peak flux density
77	BMAX			2844	Gauss	Maximum flux density
78	BAC			933	Gauss	AC flux density
79	ALG			140	nH/turns^2	Typical gapped core effective inductance
80	LG			0.310	mm	Core gap length
81	LAYERS_PRIMARY	**4**		4		Number of primary layers
82	AWG_PRIMARY			30	AWG	Primary winding wire AWG
83	OD_PRIMARY_INSULATED			0.303	mm	Primary winding wire outer diameter with insulation
84	OD_PRIMARY_BARE			0.255	mm	Primary winding wire outer diameter without insulation
85	CMA_PRIMARY			248	Cmil/A	Primary winding wire CMA
86						
87	**SECONDARY WINDING**					
88	NSECONDARY	**6**		6		Secondary turns
89	AWG_SECONDARY			19	AWG	Secondary winding wire AWG
90	OD_SECONDARY_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation
91	OD_SECONDARY_BARE			0.912	mm	Secondary winding wire outer diameter without insulation
92	CMA_SECONDARY			216	Cmil/A	Secondary winding wire CMA
93						
94	**BIAS WINDING**					
95	NBIAS			15		Bias turns

Figure 7. Transformer Core and Construction Variables Section of InnoSwitch3 PIXLs Spreadsheet.

Core Type, CORE
By default, if the core type cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous (average) output power specified. Different core types and sizes from the drop-down list are available to choose from if a user-preferred core is not available, the grey override cells (AE, LE, AL, VE, AW & BW) can be used to enter the core and bobbin parameters directly from the manufacturer's data sheet.

Output Power at 75 kHz	Core and Bobbin Table								
	Core						Bobbin		
	Core	Code	AE (mm^2)	LE (mm)	AL (nH/T^2)	VE (mm^3)	Code	AW (mm^2)	BW (mm)
0 W – 10 W	EE10	PC47EE10-Z	12.1	26.1	850	300	B-EE10-H	12.21	6.60
0 W – 10 W	EE13	PC47EE13-Z	17.1	30.2	1130	517	B-EE13-H	18.43	7.60
0 W – 10 W	EE16	PC47EE16-Z	19.2	35.0	1140	795	B-EE16-H	14.76	8.50
0 W – 10 W	EE19	PC47EE19-Z	23.0	39.4	1250	954	B-EE19-H	29.04	8.80
10 W – 20 W	EE22	PC47EE22-Z	41.0	39.4	1610	1620	B-EE22-H	19.44	8.45
10 W – 20 W	EE25	PC47EE25-Z	41.0	47.0	2140	1962	B-EE25-H	62.40	11.60
20 W – 50 W	EE30	PC47EE30-Z	111.0	58.0	4690	6290	B-EE30-H		13.20
0 W – 10 W	RM5	PC95RM05Z	24.8	23.2	2000	574	B-RM05-V		4.90
10 W – 20 W	RM6	PC95RM06Z	37.0	29.2	2150	1090	B-RM06-V		6.20
20 W – 30 W	RM8	PC95RM08Z	64.0	38.0	5290	2430	B-RM08-V	30.00	8.80
30 W – 50 W	RM10	PC95RM10Z	96.6	44.6	4050	4310	B-RM10-V		10.00
45 W – 65 W	EQ25	EQ25-3C96	100	41.4	4400	4145	EQ25-15.5A-4P-TH-J-12	34.83	8.1
50 W – 70 W	PQ26/20	PC95PQ26/20Z-12	119	46.3	7470	5490	BPQ26/20-1112CPFR	30.7	9.2

Table 7. Commonly Available Cores and Power Levels at Which These Cores Can be used for Typical Designs.

Safety Margin, MARGIN (mm)
For designs that require safety isolation between primary and secondary, but are not using triple insulated wire the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical; however if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin was only present on one side of the bobbin. For designs using triple insulated wire it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically several bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required.

Margin reduces the available area for the windings, marginated construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero margin approach using triple insulated wire.

Primary Turns, NPRIMARY
This is the number of turns for the main winding of the transformer calculated based on VOR and Secondary Turns.

Peak Flux Density, BPEAK (Gauss)
A maximum value of 3800 gauss is recommended to limit the peak flux density at max current limit and 132 kHz operation. Under an output-shorted condition the output voltage is low and little reset of the transformer occurs during the MOSFET off-time. This allows the transformer flux density to "staircase" beyond the normal operating level. A value of 3800 gauss at the max current limit of the selected device together with the built in protection features of InnoSwitch3 provides sufficient margin to prevent core saturation under output short-circuit conditions.

Maximum Flux Density, BMAX (Gauss)
The low frequency operation resulting from a light load condition can generate audible frequency components within the transformer, especially if a long core is used. To limit audible noise generation, the transformer should be designed such that the maximum core flux density is below 3000 gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. A careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

AC Flux Density, BAC (Gauss)
The BAC value can be used for calculating core loss.

Gapped Core Effective Inductance, ALG: (nH/N^2)
Used to specify the CORE GAP [LG].

Primary Layers, LAYERS_PRIMARY
By default, if the override cell is empty, a value of 3 is assumed. Primary layers should be in the range of $1 \leq L \leq 3$, and in general it should meet the current capacity guideline of 200 – 500 circular mils/ampere for designs without forced air cooling. Primary winding wire gauge AWG_PRIMARY is calculated in cell [E82]. Values above 3 layers are possible but the increased leakage inductance and physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high. In this approach half of the primary winding is placed on either side of the secondary (and bias) windings in a sandwich arrangement.

Primary Winding Wire Guage, AWG_PRIMARY (AWG)
By default, if the override cell is empty, double insulated wire is assumed and a standard wire diameter is chosen. The grey override cells can be used to enter the wire gauge directly by the user, or if the wire used is different from the standard double insulated type.

Secondary Turns, NSECONDARY
By default, if the grey override cell is left blank, the minimum number of secondary turns is calculated such that the peak operating flux density B_{PEAK} is kept below the recommended maximum of 3800 gauss (380 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired.

Bias Turns, NBIAS
Determined based on VBIAS set voltage or secondary turns.

The other transformer parameters that are automatically calculated by the spreadsheet include:

OD_PRIMARY_INSULATED (mm), Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE (mm), Outer diameter without insulation
CMA_PRIMARY (Cmil/A), Winding CMA
OD_SECONDARY_INSULATED (mm), Secondary winding wire outer diameter with insulation
OD_ SECONDARY _BARE (mm), Outer diameter without insulation
CMA_ SECONDARY (Cmil/A), Winding CMA

Step 5 – Primary Components Selection

Enter: BROWN-IN VOLTAGE, VBIAS, VF_BIAS

Brown-Out Actual
During brown-out, the power supply will inhibit switching when the brown-out threshold current falls below the IUV- threshold.

Line Overvoltage, OVERVOLTAGE_LINE
This is the input AC voltage at which the power supply will instantaneously stop switching once the overvoltage threshold (I_{OV+}) is exceeded, switching will be re-enabled when switching the line overvoltage hysteresis ($I_{OV(H)}$) level is reached. Line OV voltage is approximately equal to $I_{OV+} \times$ (RLS1 + RLS2) / 1.414.

Rectified Bias Voltage, VBIAS
A default value of 12 V is assumed. The voltage may be set to different values (for example for applications when the bias winding output is also used as a non-isolated primary-side auxiliary output). Higher voltages typically increase no-load input power. Values below 10 V are not recommended since at light load there may be insufficient voltage to supply current to the PRIMARY BYPASS pin which will increase no-load input power. A 22 μF, 50 V low ESR electrolytic capacitor is recommended for the bias winding rectification filter capacitor, CBIAS. A low ESR electrolytic capacitor improves no-load input power.

BPP Pin Capacitor, CBPP
The capacitance value is determined by the ILIMIT_MODE required. 0.47 μF for standard or 4.7 μF for increased current limit. Although electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. A ceramic X7R (or better) type capacitor rated to at least 25 V is recommended.

99	**PRIMARY COMPONENTS SELECTION**					
100	**Line undervoltage**					
101	BROWN-IN REQURED	**74.0**		74.0	V	Required AC RMS line voltage brown-in threshold
102	RLS			3.74	MΩ	Connect two 1.87 MOhm resistors to the V-pin for the required UV/OV threshold
103	BROWN-IN ACTUAL			75.0	V	Actual AC RMS brown-in threshold
104	BROWN-OUT ACTUAL			67.8	V	Actual AC RMS brown-out threshold
105						
106	**Line overvoltage**					
107	OVERVOLTAGE_LINE			312.5	V	Actual AC RMS line over-voltage threshold
108						
109	**Bias diode**					
110	VBIAS			12.0	V	Rectified bias voltage
111	VF_BIAS			0.70	V	Bias winding diode forward drop
112	VREVERSE_BIASDIODE			84.73	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
113	CBIAS			22	uF	Bias winding rectification capacitor
114	CBPP			0.47	uF	BPP pin capacitor

Figure 8. Primary Components Section of InnoSwitch3 PIXls Spreadsheet.

Required Line Undervoltage Brown-in, BROWN-IN REQUIRED
This is the input AC voltage at which the power supply will turn on (once the brown-in threshold (IUV+) is exceeded). The typical value is 20% below minimum AC input voltage (VIN_MIN). The brown-in voltage can be changed to a specific voltage required on cell [C101].

Line Undervoltage / Overvoltage Sense Resistor, RLS
PIXls will calculate the resistance value based on the brown-in voltage. Shown as RLS1 + RLS2 on Figure 13, they are typically connected after the bridge rectifier. Typical total value for RLS1 + RLS2 is 3.8 MΩ. RLS is approximately equal to $V_{BROWN-IN} \times 1.414 / I_{UV+}$.

Bias Diode Forward Drop, VF_BIAS
A default value of 0.7 V is used though this can be changed to match the type of diode used for rectifying the bias winding.

Step 6 – Secondary Components

Enter: RFB_UPPER

118	SECONDARY COMPONENTS					
119	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
120	RFB_LOWER			34.00	kΩ	Lower feedback resistor
121	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor

Figure 9. Secondary Components Section of InnoSwitch3 PIXLs Spreadsheet.

125	MULTIPLE OUTPUT PARAMETERS					
126	**OUTPUT 1**					
127	VOUT1			5.00	V	Output 1 voltage
128	IOUT1			4.00	A	Output 1 current
129	POUT1			20.00	W	Output 1 power
130	IRMS_SECONDARY1			5.95	A	Root mean squared value of the secondary current for output 1
131	IRIPPLE_CAP_OUTPUT1			4.41	A	Current ripple on the secondary waveform for output 1
132	AWG_SECONDARY1			19	AWG	Wire size for output 1
133	OD_SECONDARY1_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation for output 1
134	OD_SECONDARY1_BARE			0.912	mm	Secondary winding wire outer diameter without insulation for output 1
135	CM_SECONDARY1			1191	Cmils	Bare conductor effective area in circular mils for output 1
136	NSECONDARY1			6		Number of turns for output 1
137	VREVERSE_RECTIFIER1			34.09	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
138	SRFET1	Auto		AON6266		SRFET selection for output 1
139	VF_SRFET1			0.076	V	SRFET on-time drain voltage for output 1
140	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
141	RDSON_SRFET1			19.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

Figure 10. Secondary Components Section of InnoSwitch3 PIXls Spreadsheet.

Upper Feedback Resistor, RFB_UPPER
The RFB_UPPER resistor value is calculated based on VOUT and the nominal internal reference voltage of the IC (1.265 V).

Upper Feedback Resistor, RFB_LOWER
The RFB_LOWER resistor is calculated based on VOUT and the 1.265 V internal reference voltage. The value will change if the specified value is used for the RFB_UPPER resistor.

Lower Feedback Resistor Decoupling Capacitor, CFB_LOWER
A 330 pF surface mount ceramic X7R type capacitor (or better) is recommended as this can be placed close to the pins of the FEEDBACK and GROUND pins of the IC.

Step 7 – Multiple Output Parameters

This section allows the user to design up to three secondary outputs (excluding bias supply) and choose a suitable MOSFET size for synchronous rectification. The spreadsheet will provide a warning should the total power of the multiple outputs exceed the power described in the **POUT** cell.

For single output design, cells **VOUT1**, **IOUT1** and **POUT1** will be the main output parameters entered in section 1.

Each output provides a selection of synchronous rectifier MOSFETs **(SRFET)** in the drop down menu, (see Table 10). Based on the SR FET chosen the on-state forward voltage, **VF_SRFET (V)**, breakdown voltage, **VBREAKDOWN_SRFET (V)**, and on-time drain resistance, **RDSON_SRFET (mΩ)** will be displayed in the spreadsheet.

The spreadsheet also calculates the critical electrical parameters for each secondary output:

RMS Current of the Secondary Output, RMS_SECONDARY (A)
– Used to size the secondary winding wire.
Current Ripple on Secondary, IRIPPLE_CAP_OUTPUT (A)
– Used to size the output filter capacitor.
–**Number of Turns for Output, NSECONDARY**
– Calculated turns for each output.

Additional information for the magnetic wire are also given, **AWG_ SECONDARY (AWG), OD_SECONDARY_INSULATED (mm) and OD_SECONDARY_BARE (mm).**

143	**OUTPUT 2**					
144	VOUT2			0.00	V	Output 2 voltage
145	IOUT2			0.00	A	Output 2 current
146	POUT2			0.00	W	Output 2 power
147	IRMS_SECONDARY2			0.00	A	Root mean squared value of the secondary current for output 2
148	IRIPPLE_CAP_OUTPUT2			0.00	A	Current ripple on the secondary waveform for output 2
149	AWG_SECONDARY2			0	AWG	Wire size for output 2
150	OD_SECONDARY2_INSULATED			0.000	mm	Secondary winding wire outer diameter with insulation for output 2
151	OD_SECONDARY2_BARE			0.000	mm	Secondary winding wire outer diameter without insulation for output 2
152	CM_SECONDARY2			0	Cmils	Bare conductor effective area in circular mils for output 2
153	NSECONDARY2			0		Number of turns for output 2
154	VREVERSE_RECTIFIER2			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
155	SRFET2	**Auto**		NA		SRFET selection for output 2
156	VF_SRFET2			NA	V	SRFET on-time drain voltage for output 2
157	VBREAKDOWN_SRFET2			NA	V	SRFET breakdown voltage for output 2
158	RDSON_SRFET2			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
159						
160	**OUTPUT 3**					
161	VOUT3			0.00	V	Output 3 voltage
162	IOUT3			0.00	A	Output 3 current
163	POUT3			0.00	W	Output 3 power
164	IRMS_SECONDARY3			0.00	A	Root mean squared value of the secondary current for output 3
165	IRIPPLE_CAP_OUTPUT3			0.00	A	Current ripple on the secondary waveform for output 3
166	AWG_SECONDARY3			0	AWG	Wire size for output 3
167	OD_SECONDARY3_INSULATED			0.000	mm	Secondary winding wire outer diameter with insulation for output 3
168	OD_SECONDARY3_BARE			0.000	mm	Secondary winding wire outer diameter without insulation for output 3
169	CM_SECONDARY3			0	Cmils	Bare conductor effective area in circular mils for output 3
170	NSECONDARY3			0		Number of turns for output 3
171	VREVERSE_RECTIFIER3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
172	SRFET3	**Auto**		NA		SRFET selection for output 3
173	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
174	VBREAKDOWN_SRFET3			NA	V	SRFET breakdown voltage for output 3
175	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3
176						
177	PO_TOTAL			20.00	W	Total power of all outputs
178	NEGATIVE OUTPUT	**N/A**		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Figure 11. Continuation of Multiple Output Parameters Section of InnoSwitch3 PIXIs Spreadsheet.

Step 8 – Tolerance Analysis

This is a useful part of the InnoSwitch3 PIXIs designer spreadsheet that provides the user with switching parameters such as switching frequency **(FSWITCHING)** for corner limits of device current limit **CORNER_ILIMIT** and primary inductance of transformer **CORNER_LPRIMARY**.

182	**TOLERANCE ANALYSIS**					
183	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
184	CORNER_ILIMIT	**TYP**		0.95	A	Current limit corner to be evaluated
185	CORNER_LPRIMARY	**TYP**		830.5	uH	Primary inductance corner to be evaluated
186	MODE_OPERATION			CCM		Mode of operation
187	KP			0.728		Measure of continuous/discontinuous mode of operation
188	FSWITCHING			67267	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
189	DUTYCYCLE			0.433		Steady state duty cycle
190	TIME_ON			6.44	us	Primary MOSFET on-time
191	TIME_OFF			8.43	us	Primary MOSFET off-time
192	IPEAK_PRIMARY			0.91	A	Primary MOSFET peak currrent
193	IPEDESTAL_PRIMARY			0.25	A	Primary MOSFET current pedestal
194	IAVERAGE_PRIMARY			0.25	A	Primary MOSFET average current
195	IRIPPLE_PRIMARY			0.66	A	Primary MOSFET ripple current
196	IRMS_PRIMARY			0.40	A	Primary MOSFET RMS current
197	CMA_PRIMARY			252	Cmil/A	Primary winding wire CMA
198	BPEAK			2835	Gauss	Peak fux density
199	BMAX			2641	Gauss	Maximum flux density

Figure 12. Tolerance Analysis Section of InnoSwitch3 PIXIs Spreadsheet.

Step 9 – Critical External Components Selection

The schematic in Figure 13 shows the key external components required for a practical single output InnoSwitch3 design. Component selection criteria is as follows:

Secondary Bypass Pin Capacitor (C_{BPS})
This capacitor works as a supply decoupling capacitor for the secondary-side controller. A surface-mount, 2.2 µF, 25 V, multi-layer ceramic capacitor is recommended for satisfactory operation of the IC. The SECONDARY BYPASS Pin voltage needs to reach 4.4 V before the output voltage reaches its target voltage. A significantly higher

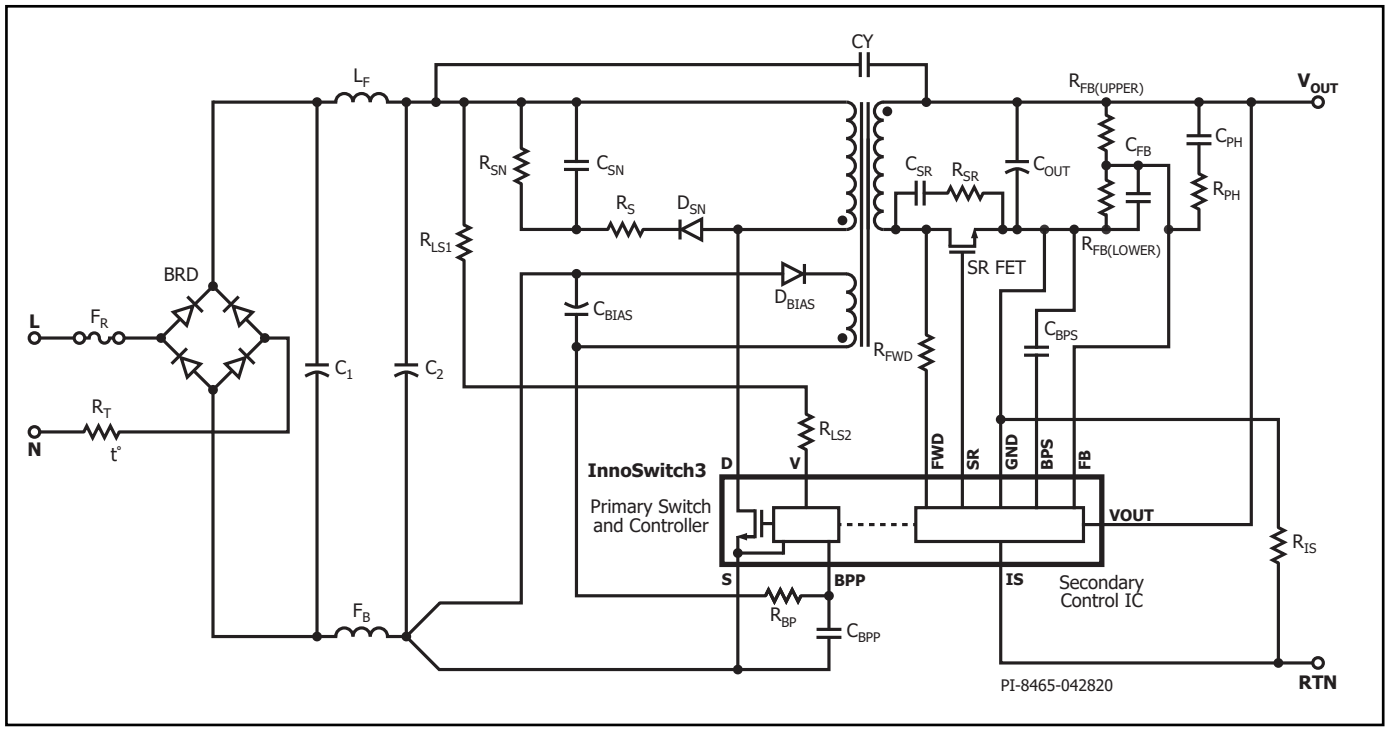


Figure 13. Typical InnoSwitch3 Flyback Power Supply.

Primary Bypass Pin Capacitor (C_{BPP})
This capacitor works as a supply decoupling capacitor for the internal primary-side controller and determines current limit for the internal MOSFET. For a 4.7 µF or 0.47 µF capacitor select either increased or standard current limit respectively. All though electrolytic capacitors can be used, surface mount multi-layer ceramic capacitors are often preferred for use with double sided boards as they enable the capacitor to be placed close to the IC. A surface mount multi-layer ceramic X7R capacitor rated for 25 V is recommended.

To ensure correct current limit it is recommended that either only 0.47 µF / 4.7 µF capacitors be used. In addition, the BPP capacitor tolerance should be equal or better than indicated below taking into account the ambient temperature range of the target application. The minimum and maximum acceptable capacitor tolerance values are set by IC characterization (Table 8).

Nominal PRIMARY BYPASS Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	+100%

Table 8. BYPASS Pin Capacitor Tolerance Values.

BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF will cause unpredictable operation. The capacitor must be located adjacent to the IC pins. The 25 V rating is necessary to guarantee sufficient capacitance in operation (the capacitance of ceramic capacitors drops with applied voltage). 10 V rated capacitors are not recommended for this reason. For best results capacitors with X5R or X7R dielectrics should be used.

FORWARD Pin Resistor (R_{FWD})
The FORWARD pin is connected to the Drain terminal of the synchronous rectifier MOSFET (SR FET). This pin is used to sense the drain voltage of the SR FET and allows precise turn-ON and turn-OFF control. This pin is also used to charge the BPS (SECONDARY BYPASS pin) capacitor when output voltage is lower than the BPS voltage. A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current and works for wide range of output voltages.
A higher or lower resistor value should not be used as it can affect device operation and effect synchronous rectification timing.

Care should be taken to ensure that the voltage on the FORWARD pin never exceeds its absolute maximum voltage. If in any design, the FORWARD pin voltage exceeds the FORWARD pin absolute maximum voltage, the IC will be damaged.

FEEDBACK Pin Divider Network (RFB_{UPPER}, RFB_{LOWER})
A suitable resistor voltage divider should be connected from the output of the power supply to the FEEDBACK pin of the InnoSwitch3 IC such that for the desired output voltage, the voltage on the FEEDBACK pin is 1.265 V. It is recommended that a decoupling capacitor (C_{FB}) of 330 pF be connected from the FEEDBACK pin to the GROUND pin. This will serve as a decoupling capacitor for the FEEDBACK pin to prevent switching noise from affecting operation of the IC.

Primary Clamp Network Across Primary Winding (D_{SN}, R_S, R_{SN}, and C_{SN})
See Figure 13. An R2CD clamp is the most commonly used clamp in low power supplies. For higher power designs, a Zener clamp or the R2CD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 90% of BV_{DSS} under worst-case conditions (maximum input voltage, maximum overload power or output short- circuit). In Figure 13, the clamp diode, D_{SN} must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of less than 500 ns. The use of standard recovery glass passivated diodes allows recovery of some of the clamp energy in each switching cycle and helps improve average efficiency. The diode conducts momentarily each time the MOSFET inside InnoSwitch3 turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{SN}. Resistor R_S, which is in the series path, offers damping preventing excessive ringing due to resonance between the leakage reactance and the clamp capacitor C_{SN}. Resistor R_{SN} bleeds-off energy stored inside the capacitor C_{SN}. Power supplies using different InnoSwitch3 devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor C_{SN}, and resistors R_{SN} and R_S must therefore be optimized for each design. As a general rule it is advisable to minimize the value of capacitor C_{SN} and maximize the value of resistors R_{SN} and R_S, while still meeting the 90% BV_{DSS} limit at highest input voltage and full load. The value of R_S should be large enough to damp the ringing in the required time, but must not be so large as to cause the drain voltage to exceed 90% of BV_{DSS}. A ceramic capacitor that uses a dielectric such as Z5U when used in clamp circuit for C_{SN} may generate audible noise, so a polyester film type should be used.

As a guide the following equations can be used to calculate R2CD component values;

$$R_{SN} = \left[\frac{V_C^2}{\frac{1}{2} L_{IK} \times I_{PK}^2 \times \frac{V_C \times F_S}{(V_C - V_{OR})}} \right] \quad ; \text{Eq. (1)}$$

$$C_S = \frac{V_C}{RSN\ 1 \times F_S \times dV_{CSN}} \quad ; \text{Eq. (2)}$$

$$R_S = \left(\frac{L_{IK}}{C_{SN}} \right)^{\frac{1}{2}} \quad ; \text{Eq. (3)}$$

Where;

V_C: Voltage across clamp circuit
I_{PK}: Peak switching current
F_S: Switching frequency
L_{IK}: Leakage inductance
V_{OR}: Reflected output voltage
dV_{CSN}: The maximum ripple voltage across clamp capacitor (10%)

For example;

If V_C = 205 V, F_S= 100 kHz, I_{PK} = 1 A, V_{OR} = 100, L_{IK} = 5 µH and dV_{SN} = 20 V

Applying the equations above,

R_{RSN} = 92.4 kΩ, C_S = 1.08 nF and R_S = 68 Ω

Common Primary Clamp Configurations

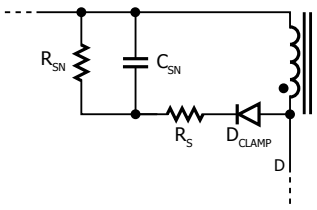
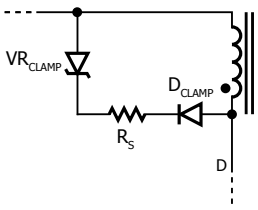
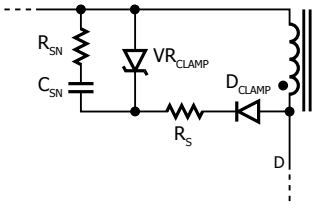
R2CD	Zener	R2CD + Zener
		
PI-8502-041818	PI-8504-041818	PI-8503-041818

Figure 14. Recommended Primary Clamp Components.

Primary Clamp Circuit			
Benefits	**R2CD**	**Zener**	**R2CD + Zener**
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 9. Benefits of Primary Clamp Circuits.

External Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BP})

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage interface node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor. In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3 to be powered externally through a bias winding, decreasing the no-load consumption to less than 15 mW in a 5 V output design.

12 V is the recommended bias voltage. Higher voltage will increase no-load input power. Ultrafast diodes are recommended for the bias winding rectifier to reduce no-load power consumption.

A 22 µF, 50 V low ESR electrolytic aluminum capacitor is recommended for the bias supply filter, C_{BIAS}. A Low ESR electrolytic capacitor will reduce no-load input power. Use of ceramic surface mount capacitor is not recommended as they cause audible noise due to piezoelectric effect in its mechanical structure.

To have the minimum no-load input power and high full load power efficiency, Resistor R_{BP} should be selected such that the current through this resistor is higher than the PRIMARY BYPASS pin current.

The PRIMARY BYPASS pin supply current at normal operating frequency can be calculated as shown in the following equation;

$$I_{SSW} = \frac{F_{SW}}{132\ kHz} \times (I_{S2} - I_{S1}) + I_{S1}$$

Where;

I_{SSW}: PRIMARY BYPASS pin supply current at operating switching frequency

F_{SW}: Operating switching frequency (kHz)

I_{S1}: PRIMARY BYPASS pin supply current at no switching (refer to data sheet)

I_{S2}: PRIMARY BYPASS pin supply current at 132 kHz (refer to data sheet)

The BPP voltage is internally clamped to 5.3 V when bias current is higher than PRIMARY BYPASS pin supply current. If BPP voltage is ~5.0 V, then this indicates that the current through R_{BP} is less than the PRIMARY BYPASS pin supply current and charge current is being drawn from the DRAIN pin to keep the PRIMARY BYPASS pin above 5.0 V except during start-up.

To determine maximum value of R_{BP};

$$R_{BP} = [V_{BIAS\,(NO\,-\,LOAD)} - V_{BPP}] / I_{SSW;}\ V_{BPP} = 5.3V$$

Output Synchronous Rectifier MOSFET (SR FET)

InnoSwitch3 features a built-in synchronous rectifier (SR) driver that enables the use of low-cost low voltage MOSFETs for synchronous rectification and increases system efficiency. Since the SR driver is referenced to the output GND, the SR FET is placed in the return line. GND is the typical threshold that ensures the SR FET will turn off ($V_{SR(TH)}$) at the end of the flyback conduction time. There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET in order to avoid current shoot through. During SR FET conduction the energy stored in the inductor is transferred to the load, the current will continue to drop until the voltage drops across the $R_{DS(ON)}$ of the SR FET drops to 0 V, at this point the SYNCHRONOUS RECTIFIER pin will pull the gate low to instantaneously turn off the SR FET. Minimal current will flow through the SR FET body diode during the remainder of the flyback time (see Figure 15). Putting a schottky diode across the SR FET may further increase efficiency by 0.1% – 0.2% depending on the design and SR FET used. In continuous conduction mode (CCM), the SR FET is turned off when a feedback pulse is sent to the primary to demand a switching cycle, providing excellent synchronous operation, free of any cross conduction between the SR FET and primary MOSFET.

The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A SR FET with a high threshold voltage is therefore not suitable. SR FETs with a gate voltage threshold voltage range ($V_{G(TH)}$) of 1.5 V to 2.5 V are recommended.

Since the termination of the ON-time of the SR FET is based on when the Drain-Source voltage of the MOSFET reaches to 0 V during the conduction cycle using an SR MOSFET with ultra-low $R_{DS(ON)}$ (< 5 mΩ) may result to early termination of the SR FET drive signal. This will cause secondary current to conduct instead through its body diode, which has a higher voltage drop compared to the SR FET's $R_{DS(ON)}$ which will slightly reduce system efficiency (see Figure 16).

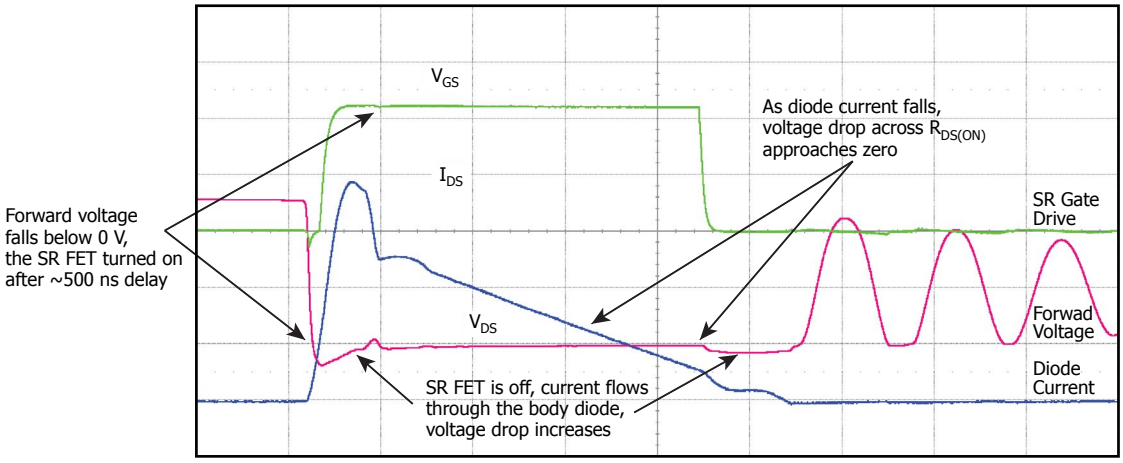


Figure 15. SR FET Turn-ON and Turn-OFF Events During DCM Operation.

An SR FET with 18 mΩ $R_{DS(ON)}$ is appropriate for a 5 V, 2 A output, and a SR FET with 8 mΩ $R_{DS(ON)}$ is suitable for designs rated with a 12 V, 3 A output.

The recommended optimum SR FET Drain-to Source On resistance ($R_{(DS)ON}$) can be estimated as follows,

Lets assume;

1. SR FET needs to conduct for 90% of the secondary conduction time.
2. $R_{D(SON)}$ at 100 °C is 50% higher than $R_{D(SON)}$ at 25 °C.

$$R_{D(SON)} \text{ at } 100\ °C = R_{D(SON)} \text{ at } 25\ °C \times 1.5$$

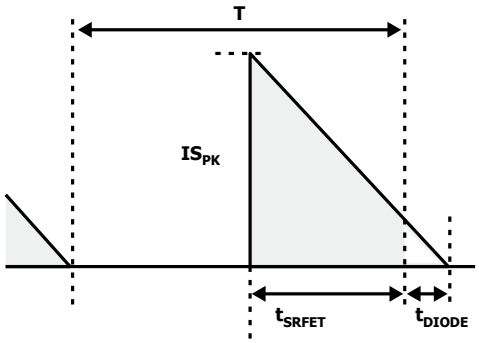
Since

$$\bullet\ \frac{N_P}{N_S} = \frac{V_{OR}}{V_O} \quad (1)$$

$$\bullet\ I_{SP} = I_P \times \frac{N_P}{N_S} \quad (2)$$

To make SR FET conduct 90% of the secondary conduction time, the voltage across FET will be equal to SR pin Voltage threshold (2.5 mV) when the secondary current, I_S, drops to 10% of its peak current level (I_{SP})

$$2.5\ mV = 10\% \times I_{SP} \times R_{D(SON)} \text{ at } 100\ °C$$



The optimum $R_{D(SON)}$ at 25 °C will be,

$$R_{D(SON)} @\ 25\ °C \approx \frac{2.5\ mV}{10\% \times 1.5 \times I_{SP}} = \frac{0.016 \times V_O}{I_P \times V_{OR}}$$

The recommended optimum SR FET Drain-to-Source on-resistance ($R_{DS(ON)}$) is approximately,

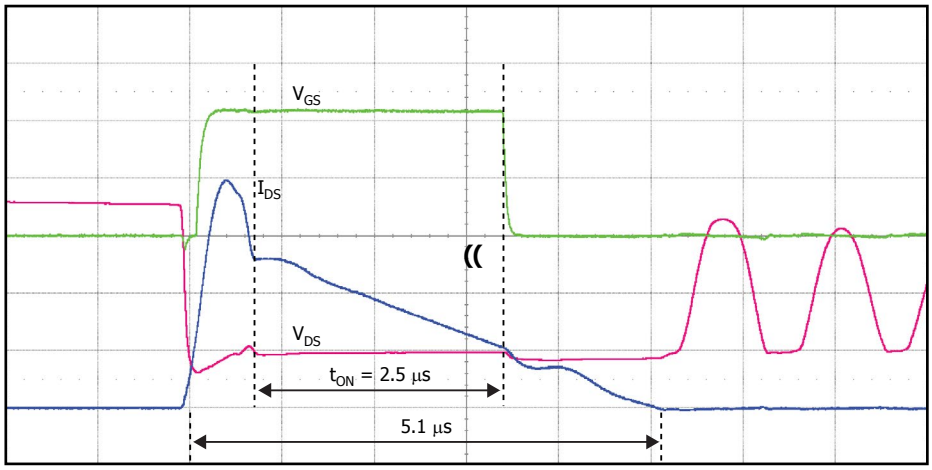
$$R_{DS(ON)} \approx \frac{0.016 \times V_O}{I_P \times VOR}$$

Some SR FETs, suitable for synchronous rectification and which meet the criteria described in this section is shown in Table 10.

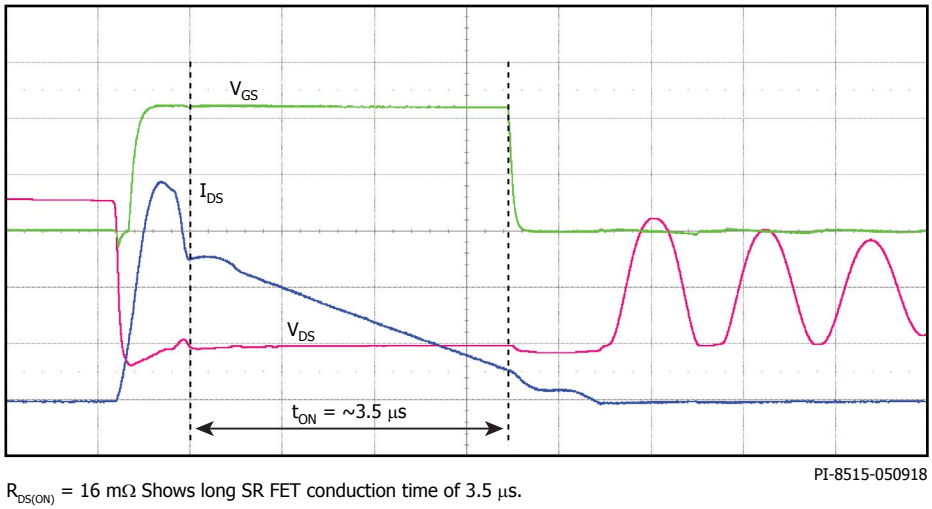
The voltage rating of the SR FET should be at least 1.3 times the expected peak inverse voltage (PIV). The peak inverse voltage is the applied maximum input DC bus voltage multiplied by the primary to secondary turns ratio of the transformer. The spreadsheet provides this estimate on line 137 as VREVERSE_RECTIFIER1. This voltage should still be measured to confirm sufficient margin for the BV_{DSS} of the SR FET and the antiparallel diode (if used).

The SR FET provides significant efficiency improvement without a cost penalty due to the reduced prices of low voltage MOSFETs. It is permissible to use a Schottky or fast-recovery diode for output rectification, by shorting gate drive SYNCHRONOUS RECTIFIER pin to ground. This may be preferred for high-voltage output.

The DC current rating of MOSFET needs to be >2 higher than the average output current. Depending on the temperature rise and the duration of a peak load condition, it may be necessary to increase the SR FET current rating and heat dissipation area once the prototype has been built.



$R_{DS(ON)}$ = 7.5 mΩ Shows short SR FET conduction time of 2.5 µs.



$R_{DS(ON)}$ = 16 mΩ Shows long SR FET conduction time of 3.5 µs.

Figure 16. Effect of $R_{DS(ON)}$ on SR FET Conduction Time.

Part	PIV	I_{DRAIN}	$V_{GS(TH)}$	$V_{GS(TH)}$	CISS	CRSS	CRSS/ CISS	R_G	$R_{DS(ON)}$	T_{RR}	Package	Manufacturer
			Max	Min								
	(V)	(A)	(V)	(V)	(pF)	(pF)	(%)	(Ω)	(mΩ)	(ns)		
AO4260	60	18.0	2.4	1.3	4940	32.0	0.65	0.9	6.3	22	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AO4264	60	12.0	2.5	1.4	2007	12.5	0.62	1.2	13.5	15	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AON6244	60	85.0	2.5	1.5	3838	14.5	0.38	1.0	6.2	17	8-PowerSMD, Flat Leads	Alpha & Omega
AON6266	60	30.0	2.5	1.5	1340	10.0	0.75	1.5	19.0	17	8-PowerSMD, Flat Leads	Alpha & Omega
AON7246	60	34.5	2.5	1.5	1340	10.0	0.75	1.5	19.0	15	8-PowerVDFN	Alpha & Omega
AO4294	100	11.5	2.4	1.4	2420	11.0	0.45	0.6	15.5	25	8-SOIC (0.154", 3.90 mm Width)	Alpha & Omega
AON7292	100	23.0	2.6	1.6	1170	8.0	0.68	0.7	32.0	24	8-WDFN Exposed Pad	Alpha & Omega
AO4292	100	8	2.7	1.6	1190	7	0.59	3	33	20	SOIC-8	Alpha & Omega
AO4294	100	11.5	2.4	1.4	2420	11	0.45	3	15.5	25	SOIC-8	Alpha & Omega
AO4296	100	13.5	2.3	1.3	3130	12.5	0.40	3	10.6	28	SOIC-8	Alpha & Omega
AOD294A	100	55	2.5	1.5	2305	11.5	0.50	3	15.5	30	TO-252	Alpha & Omega
AOD296A	100	70	2.3	1.3	3130	12.5	0.40	3	10.6	30	TO-252	Alpha & Omega
AOD2910	100	31	2.7	1.6	1190	7	0.59	3	33	30	TO-252	Alpha & Omega
AOD2916	100	25	2.7	1.6	870	3.5	0.40	3	43.5	20	TO-252	Alpha & Omega
AON6220	100	48	2.3	1.3	4525	22.5	0.50	1.1	7.4	32	DFN5X6	Alpha & Omega
AOD2544	150	23.0	2.7	1.7	675	4.0	0.59	2.9	66.0	37	TO-252 DPAK	Alpha & Omega
AON7254	150	17.0	2.7	1.7	675	4.0	0.59	2.9	66.0	37	8-WDFN Exposed Pad	Alpha & Omega

Table 10. List of MOSFETs Suitable for Synchronous Rectification.

At the instance of voltage reversal at the winding due to primary MOSFET turn-ON, the interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor of 10 Ω to 47 Ω may be used (higher resistance values will lead to a noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

When the primary MOSFET turns on, a fast rising voltage is transferred to the secondary via the transformer across the drain-source of the SR FET. This high dv/dt combined with high ratio of C_{GD} to CISS MOSFET capacitances will induce gate-source voltage on the SR FET. If the induced gate voltage exceeds the minimum gate threshold voltage, $V_{GS(TH)}$, then it will turn-on the SR FET causing cross-conduction possibly leading to catastrophic failure. The recommended C_{GD} (CRSS), is less than 35 pF, and the ratio of CRSS to CISS to be less than 2%.

Another important parameter in the selection of SR FET is the reverse recovery time (T_{RR}) of its body diode. The reverse recovery characteristics of the SR FET's body diode can influence the level of voltage stress on the drain when the primary MOSFET switches on. As shown in Figure 17, the SR FET with a slow body diode (> 40 ns T_{RR}) has twice the voltage stress compared to the one with a fast body diode. The recommended maximum reverse recovery time (T_{RR}) of the body diode is less than 40 ns.

Output Filter Capacitance (C_{OUT})

The current ripple rating of the output capacitor(s) should be greater than the calculated value in the spreadsheet, IRIPPLE_CAP_OUTPUT1. However in designs with high peak to continuous (average) power and for those with long duration peak load conditions, the capacitor rating may need to be increased. Selection in this one should be based on the measured capacitor temperature rise under worst-case load and ambient temperature conditions. The spread- sheet calculates the output capacitor ripple current using the average

output power. The actual rating of the capacitor will therefore depend on the peak-to-average power ratio of the design. In most cases, this assumption will be valid as capacitor ripple rating is a thermal limitation and most peak load durations are shorter than the thermal time constant of the capacitor (typically < 1 s).

In either case, if a suitable capacitor cannot be found then two or more capacitors may be used in parallel to achieve a combined ripple current rating equal to the sum of the individual capacitor ripple ratings. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from its data sheet maximum. This is to ensure that the capacitor is not oversized.

The use of aluminum-polymer solid capacitors has gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters. Typically, 200 µF to 300 µF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is allowable output ripple. Ensure that only capacitors with a voltage rating higher than the highest output voltage plus suitable margin are used.

The switching ripple voltage is equal to the peak secondary current multiplied by the ESR of the output capacitor. It is therefore important to select low ESR capacitor types to reduce the ripple voltage. In general, selecting a high ripple current rated capacitor results in an acceptable value of ESR.

The voltage rating of the capacitor should be at least 1.2 times the output voltage (VOUT).

Output Current Sense Resistor (R_{IS})

For constant current (CC) output operation, the external current sense resistor R_{IS} should be connected between the IS pin and secondary GROUND pin of the IC. If constant current (CC) regulation is not required, the IS pin should be connected directly to the GROUND pin of the IC.

The voltage generated across the resistor is compared to an internal current limit voltage threshold ($I_{SV(TH)}$) of approximately 35 mV.

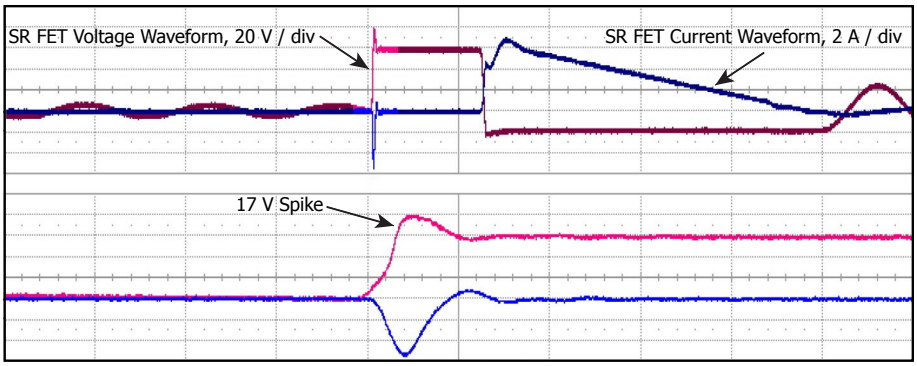
The external current sense resistor R_{IS} can be estimated by using;

$$R_{IS} = I_{SV(TH)}/I_{OUT(CC)}$$

The voltage developed across the resistor is connected to an internal reference $V_{SV(TH)}$ (35 mV), the R_{IS} resistor must be placed close to IS and GROUND pins with short traces in order to prevent ground impedance noise instability in constant current operation.

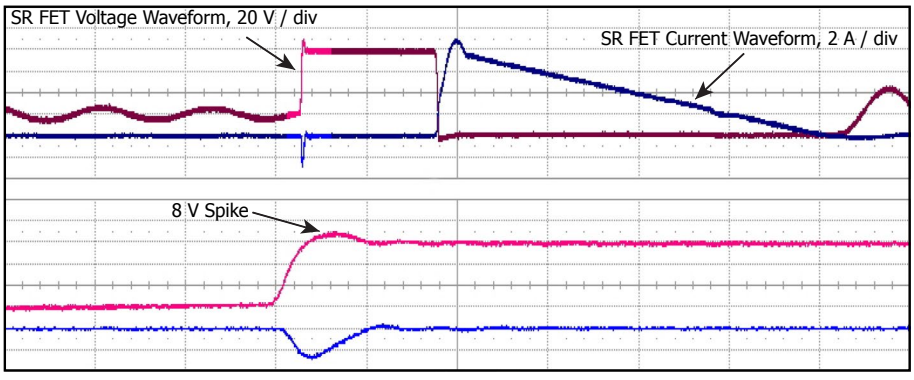
Output Post Filter Components (L_{PF}, C_{PF})

If necessary a post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 µH – 3.3 µH with a current rating above the peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥ 1.25 × V_{OUT}. If a post filter is used then the output voltage sense resistor should be connected before the post filter inductor.



PI-8517-100118

SR FET with slow body diode, showing high-voltage spike, 17 V.



PI-8518-100118

SR FET with fast body diode, significantly low voltage spike, 8 V.

Figure 17. Effect of Body Diode Reverse Recovery Time on V_{DS}.

Key Applications Design Considerations

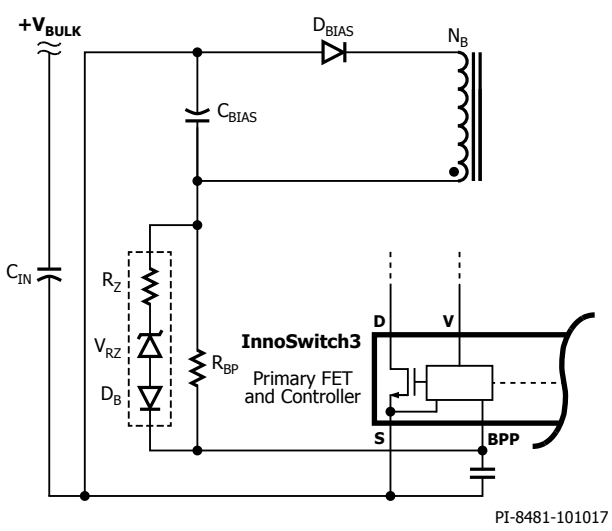
Output Power Table

The output power table in the data sheet (Table 1) represents the maximum practical continuous output power that can be obtained under the following conditions:

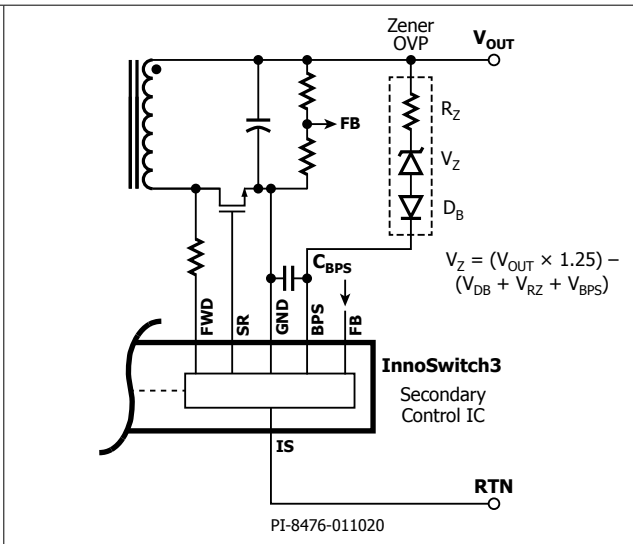
3. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input (or 115 VAC with a voltage-doubler). Input capacitor voltage should be sized to meet these criteria for AC input designs.
4. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >84% increasing to >89% for the largest device and are quite conservative.
5. Transformer primary inductance tolerance of ±10%.
6. Reflected output voltage (V_{OR}) is set to maintain K_P = 0.8 at minimum input voltage for universal line and K_P = 1 for high-line designs.
7. Maximum conduction loss for adapters is limited to 0.6 W, 0.8 W for open frame designs.
8. Increased current limit is selected for peak and open frame power designs and standard current limit for adapter designs.
9. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
10. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters is assured.
11. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.5 is used. This prevents the initial current limit (I_{INT}) from being exceeded at MOSFET turn-ON.
12. It is unique feature in InnoSwitch3 that a designer can set the operating switching frequency between 25 kHz to 95 kHz depending on the transformer design. One of the ways to effectively lower device temperature is to design the transformer to operate at low switching frequency, a good starting point is 60 kHz for larger device such as size 8, but for smaller device such size 2, 80 kHz is appropriate.

Primary-Side Overvoltage Protection

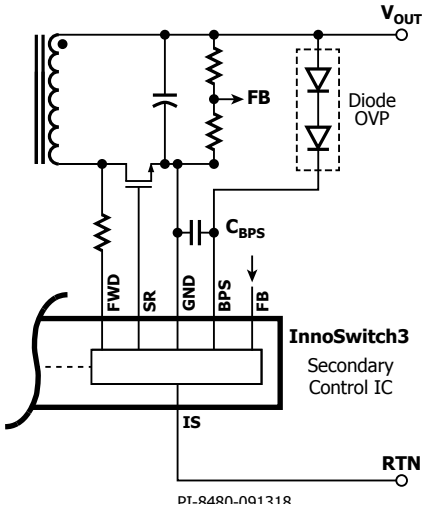
Primary-side output overvoltage protection provided by the InnoSwitch3 IC uses an internal latch that is triggered by a threshold current of I_{SD} flowing into the PRIMARY BYPASS pin. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as



a. Primary-side OVP with high current pushed into BPP via Zener V_{RZ}.



b. Secondary-side OVP with high current pushed into BPS via Zener V_Z and resistor R_Z.



c. Secondary-side OVP with high current pushed into BPS via two diodes (for 5 V output only).

Figure 18. Output Overvoltage Protection Circuits.

close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

Primary sensed OVP can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin (see Figure 18-a). The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) dependent on the coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. Ideally this measurement should be made at the lowest input voltage and with full output load. This measured voltage should be used to select the components required to provided primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be used. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode should be used. The blocking diode prevents any reverse current charging the bias capacitor during start-up. Finally, the value of the series resistor set such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage event.

Secondary-Side Overvoltage Protection

Secondary-side output overvoltage protection is provided by the InnoSwitch3 IC. It is activated when an internal auto-restart is triggered when a current exceeding the $I_{BPS(SD)}$ threshold is fed into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage rating shall be the difference between 1.25 V_{OUT} and 4.4 V SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor, in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin (see Figure 18-b).

An OVP for a 5 V output can be implemented by two-diodes in series (shown in Figure 18-c). The filter capacitor should be rated for 6.3 V.

Recommendations for Circuit Board Layout

Single-Point Grounding

Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. See Figures 19 and 20.

Bypass Capacitors

The PRIMARY BYPASS (C_{BPP}), SECONDARY BYPASS (C_{BPS}) decoupling capacitors must be located directly adjacent to the PRIMARY BYPASS-SOURCE, SECONDARY BYPASS-GROUND and FEEDBACK-GROUND (C_{FB}) pins respectively and connections should be routed via short traces.

Signal Components

External components R_{LS}, R_{BP}, $R_{FB(UPPER)}$, $R_{FB(LOWER)}$ and R_{IS} which are used for monitoring feedback information must be placed as close as possible to the IC pin with short traces.

Critical Loop Area

Circuits where high dv/dt or di/dt occurs should be kept as small as possible. The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

No loop area should be placed inside another loop (see Figure 21). This will minimize cross-talk between circuits.

Primary Clamp Circuit

A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop between the clamp components, the transformer and the IC.

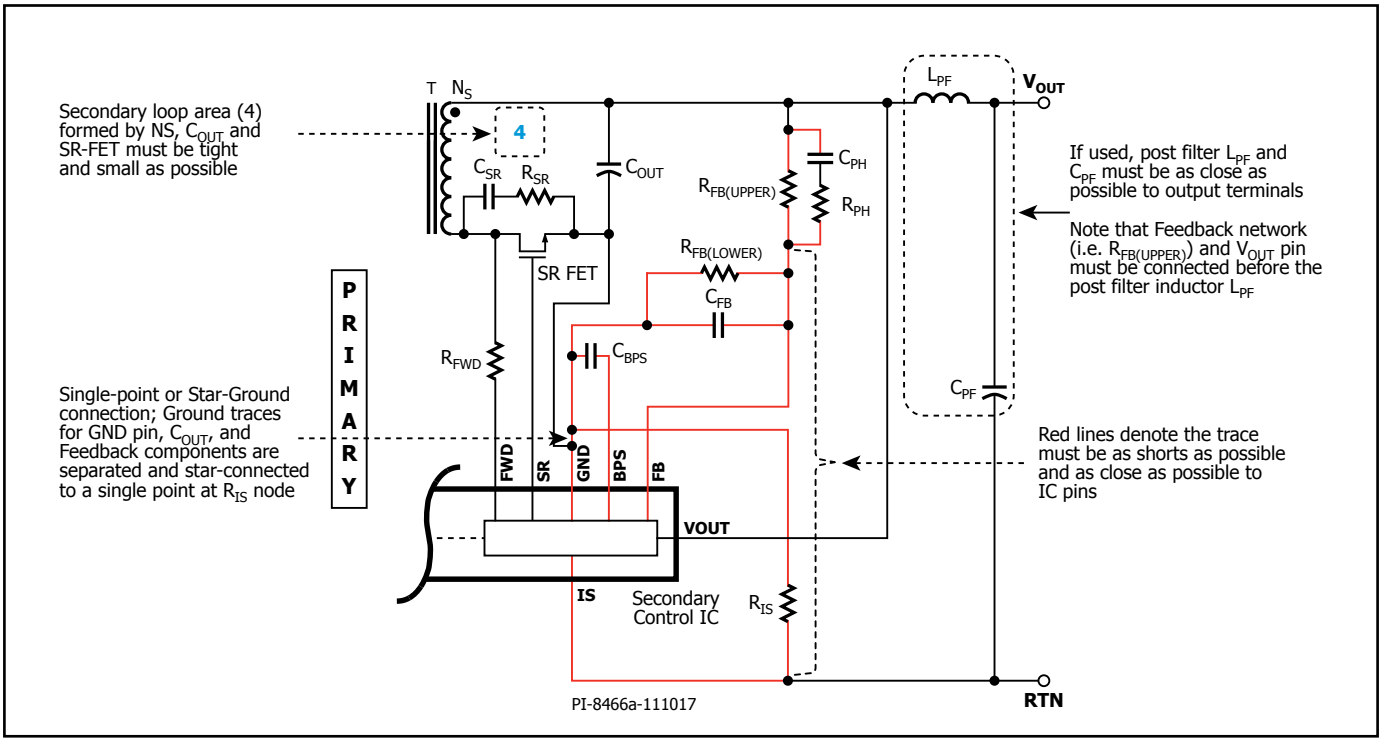


Figure 19. Typical Schematic of InnoSwitch3 Primary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding.

Y Capacitor

The placement of the Y capacitor should be directly from the primary input filter capacitor positive terminal to the output positive or return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the IC. Note that if an input pi EMI filter C1, L_F, C2 is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR MOSFET

For best performance, the area of the loop connecting the secondary winding, the output SR MOSFET, and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the terminals of the SR MOSFET for heat sinking. The distance between SR FET source and InnoSwitch3 GROUND pin needs to be short. To prevent negative current flowing through the primary MOSFET.

ESD Immunity

Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD or hi-pot isolation requirements. The spark gap is best placed between output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration a 6.4 mm (5.5 mm is acceptable – dependent on customer requirement) spark gap is more than sufficient to meet the creepage and clearance requirements of most applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input. See layout example Figure 21.

A spark gap across the common-mode-choke or inductor helps provide low impedance path for a high energy discharge due to ESD or a common-mode surge.

Drain Node

The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin, and the trace width and length in this circuit should be minimized.

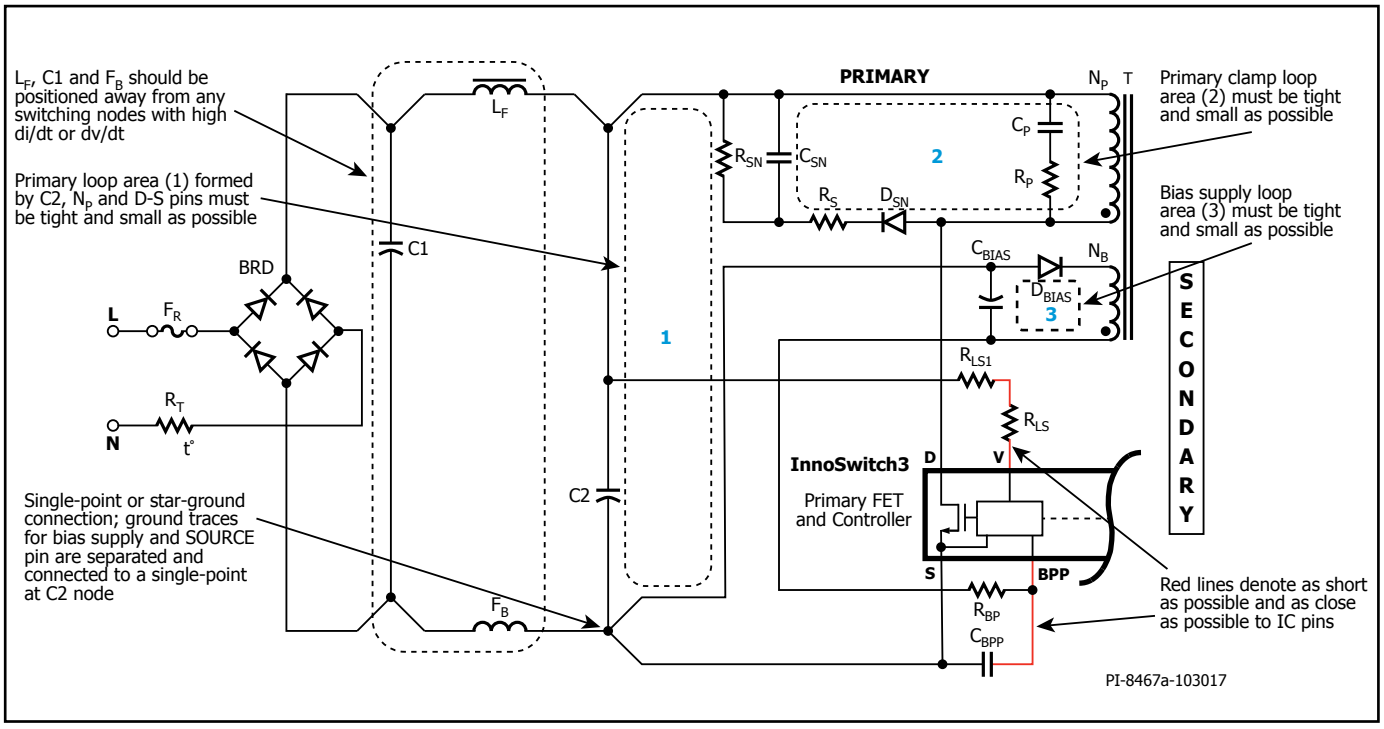
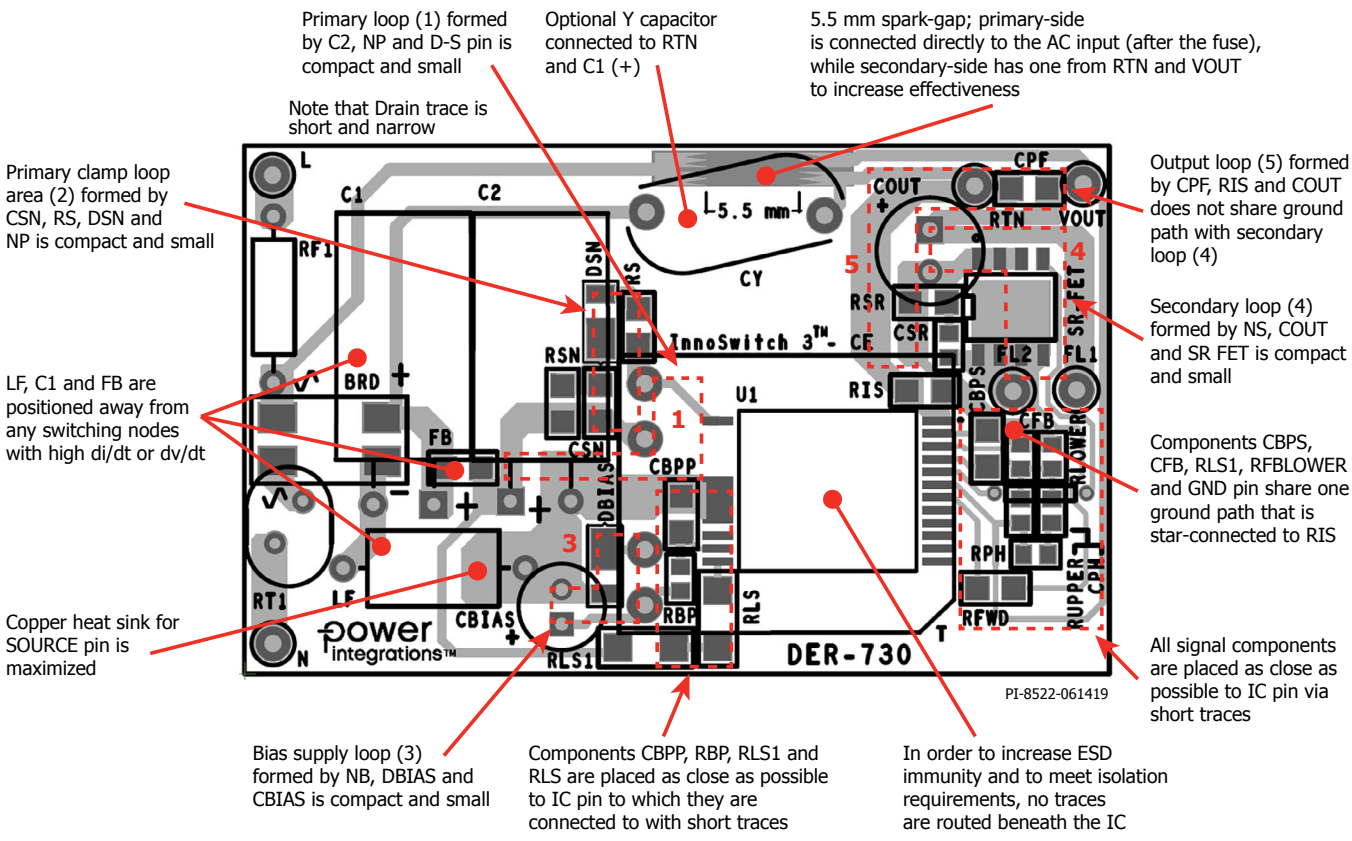


Figure 20. Typical Schematic of InnoSwitch3 Secondary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding. Optional Post Filter LC included.

Layout Example



Special Notes

- All loops are separated; no loop is inside a loop. This will avoid ground impedance noise coupling.
- Keep trace surface area and length of high dv/dt nodes such as Drain, as small and short as possible to minimize RFI generation.
- No (quiet) signal trace such as Y capacitor and feedback return should be routed near to or across noisy nodes (high dv/dt or di/dt) such as Drain, underneath transformer belly, switching-side of any winding or output rectifier diode. This avoids capacitive or magnetic noise coupling.
- No signal trace should share path with traces having an AC switching current such as the output capacitors. Connection must be star-connected to capacitor pad in order to avoid ground impedance coupled noise.

Figure 21. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location in Reference to Figures 19 and 20.

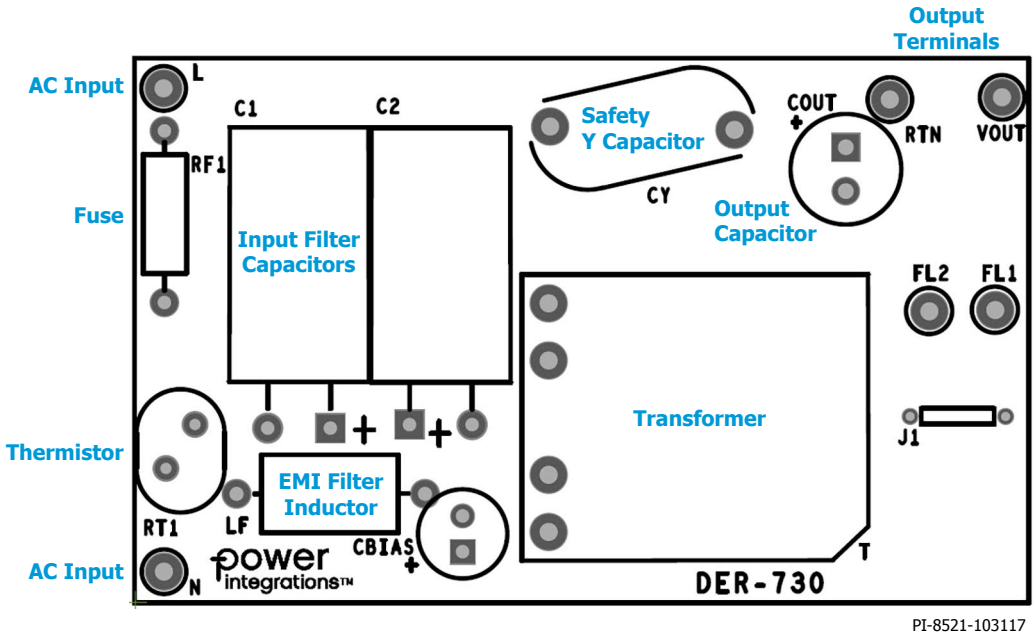


Figure 22. TOP Side – Layout Example Showing Through-Hole Components.

Design Considerations When Using PowiGaN Devices (INN3x78C, INN3x79C and INN3x70C)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 23.

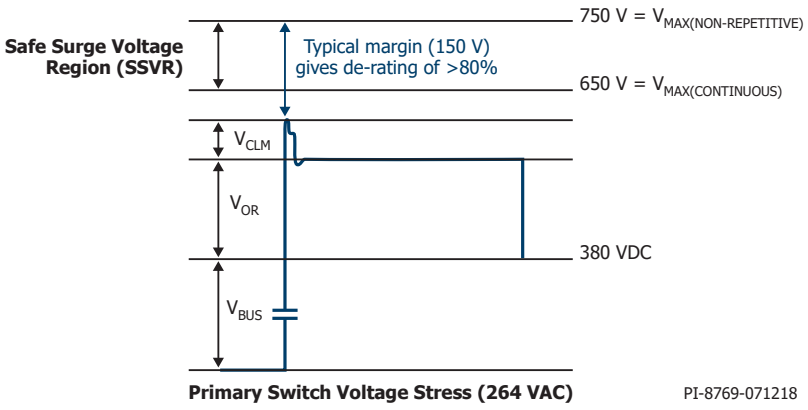


Figure 23. Peak Drain Voltage for 264 VAC Input Voltage.

VOR is the reflected output voltage across the primary winding when the secondary is conducting. VBUS is the DC voltage connected to one end of the transformer primary winding.

In addition to VBUS+VOR, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch.

VCLM in Figure 20 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of VBUS, VOR and VCLM.

VOR and the clamp voltage VCLM should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage (VOR) to maintain KP = 0.8 at minimum input voltage for universal input and KP ≥ 1 for high-line-only conditions.

Consider the following for design optimization:

1. Higher VOR allows increased power delivery at VMIN, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN INN3678C, INN3679C and INN3670C device.
2. Higher VOR reduces the voltage stress on the output diodes and SR FETs.
3. Higher VOR increases leakage inductance which reduces power
4. Higher VOR increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents the VOR should be reduced to get highest efficiency. For output voltages above 15 V, VOR should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier.

VOR choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of VOR for optimal performance:

Output Voltage	Optimal Range for VOR
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 150
24 V	135 - 180

Effect of Surge Voltage on R_{DSON} of the Device (INN3x78C, INN3x79C and INN3x70C)

R_{DSON} of the device increases when subjected to repetitive surge over 650V on the drain, however the device R_{DSON} recovers to nominal value over time.

Figure 24 shows the effect of repetitive surge on R_{DSON} of the device.

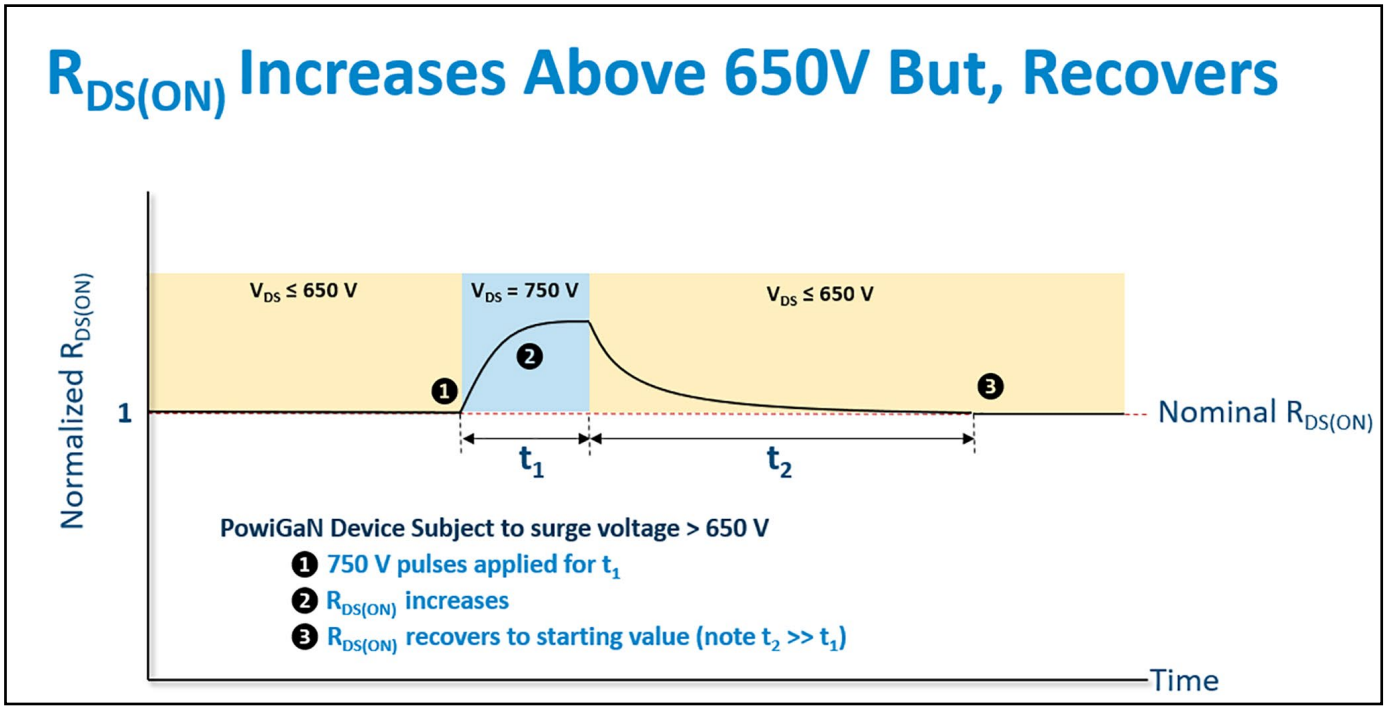


Figure 24. Effect of Surge Voltage on R_{DSON} of the Device.

Where as

T1	T2	R_{DSON} Increase
100s	20 Hr	5%

Recommended Position of InSOP-24D Package with Respect to Transformer

The PCB underneath the transformer and InSOP-24D must be rigid. If a large size transformer core is used on the board with thin PCB, (<1.5 mm), it is recommended that the transformer be away from the InSOP package. Cutting a slot in the PCB that runs near to or underneath the InSOP package is generally not recommended as this weakens the PCB. In the case of a long PCB, it is recommended that mechanical support or post be placed in the middle of the board or near the InSOP package.

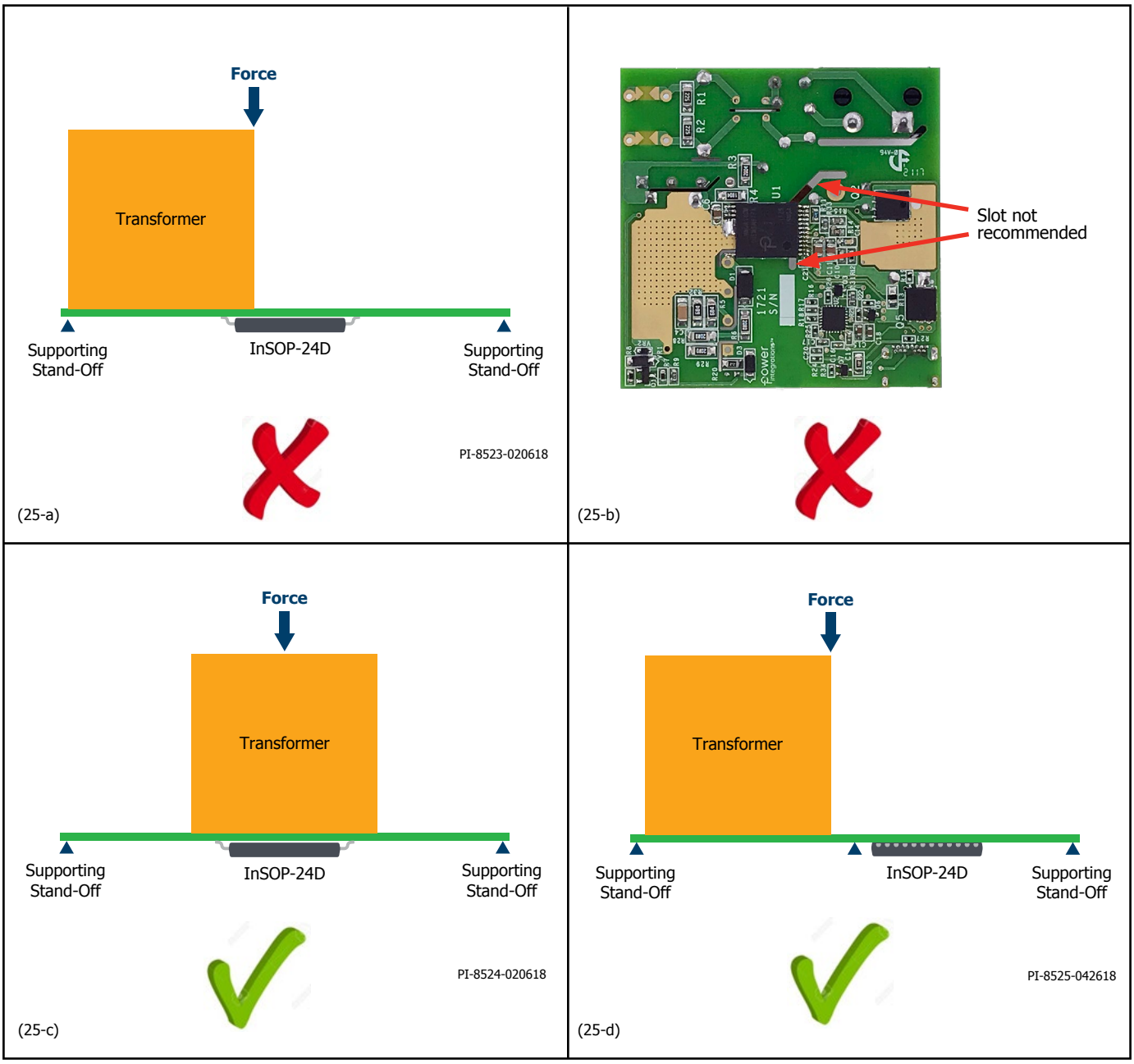


Figure 25. Recommended Position of InSOP-24D Package Shown with Check Mark.

Recommendations to Reduce No-load Consumption

The InnoSwitch3 IC will start in self-powered mode, drawing energy from the BYPASS pin capacitor that is charged from an internal current source. A bias winding is required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3 IC has started switching. A bias winding supply to the PRIMARY BYPASS pin enables power supplies with no-load power consumption of less than 15 mW. Resistor R_{BP} shown in Figure 13 should be adjusted to achieve the lowest no-load input power.

Other areas that may help reduce no-load consumption further are;

1. Low value of primary clamp capacitor, C_{SN}.
2. Schottky or ultrafast diode for bias supply rectifier, D_{BIAS}.
3. Low ESR capacitor for bias supply filter capacitor, C_{BIAS}.
4. Low value SR FET RC snubber capacitor, C_{SR}.
5. Tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter winding capacitance.

Recommendations for Reducing EMI

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area. (See Figures 19 and 20)
2. A small capacitor parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor (2 – 47 Ω) in series with the bias winding helps reduce radiated EMI.
4. A small resistor and ceramic capacitor (< 22 pf) in series across primary shown in Figure 20 and/or across secondary winding (< 100 pf) may help reduce conducted and/or radiated EMI. However if value is large, then no-load consumption will increase.
5. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common-mode noise. However, the same performance can be achieved by use of shield windings in the transformer. Shield windings can also be used in conjunction with common mode filter inductors at the input to reduce conducted and radiated EMI.
6. Adjusting SR MOSFET RC snubber component values can help reduce high frequency radiated and conducted EMI.
7. A pi filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI. A ferrite bead as shown in Figure 20 can be added to further improve EMI margin at minimal cost.
8. A resistor across the differential inductors reduces their Q factor which can reduce EMI above 10 MHz. However low frequency EMI below 5 MHz may increase slightly.
9. A 1 μF ceramic capacitor connected at the output of the power supply may help to reduce radiated EMI.
10. A slow diode (i.e. 250 ns < t_{RR} < 500 ns) as the bias rectifier (D_{BIAS}) is generally good for reducing conducted EMI > 20 MHz and radiated EMI
    > 30 MHz.

Recommendations for Increased ESD Immunity

1. Sufficient clearance should be maintained (> 8 mm) between the primary-side and secondary-side circuits (especially underneath InSOP package and transformer).
    a. It is not recommended to place spark gap near or across InSOP package.
2. Use two spark gaps connected to secondary terminals (output return and positive) and one of the AC inputs after the fuse (see Figure 21). In this configuration at least 5.4 mm gap is often sufficient to meet creepage and clearance requirements of applicable safety standards.
    a. For applications with a USB connector, float the PCB pads connected to the legs of the connector.
3. Use a spark gap across common-mode choke or inductor to provide a low impedance path for any high energy discharge build up due to ESD or common mode surge.
4. Use a Y capacitor connected from either positive or negative output terminals to the input bulk capacitor's positive terminal or to the AC input after the fuse.
5. Employ good layout practices and follow the PCB layout recommendations in the application note.
6. Apply multi-layer tape between bias and secondary windings, and also between secondary and primary windings.

Thermal Management Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without causing EMI problems. Similarly for the output SR MOSFET, maximize the PCB area connected to the pins on the package through which heat is dissipated.

Sufficient copper area should be provided on the board to keep the IC temperature safely below absolute maximum limits. It is recommended that the copper area to which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 90 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage (at nominal ambient). Further de-rating can be applied as required.

Heat Spreader

For stringent thermal requirements, position the IC adjacent to the transformer as shown in Figure 25-d. This will reduce heat transfer to the IC from the transformer. For enclosed high power applications such as laptop adaptor or similar applications with high ambient environment, using the PCB as a heat sink may not be enough for the IC to operate within specified operating temperature, therefore a metal heat spreader may be necessary to keep the IC cool. Unless a ceramic material is used for the heat sink, care must be taken to maximize the safety limit. A heat spreader is formed by combination of a heat spreader material (Copper or Aluminum), a 0.4 mm mylar pad (for reinforced isolation) and a thermally conductive pad for better heat transfer between the IC and the spreader.

Figure 26 shows the basic idea how to implement the attachment of a heat spreader to an InSOP-24D package while maintaining creepage between primary-side and secondary-side pins of InnoSwitch3 IC.

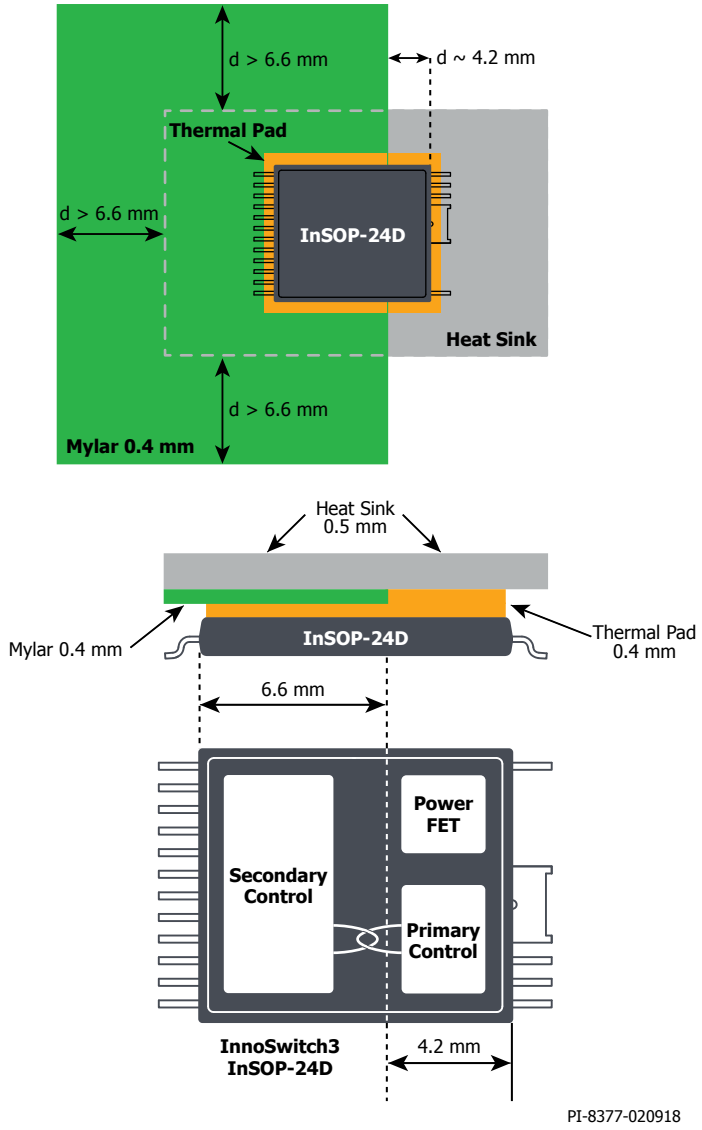


Figure 26. Simplified Diagram of Heat Spreader Attachment to an InSOP-24D Package.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3 designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage

Verify that V_{DS} of InnoSwitch3 and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current

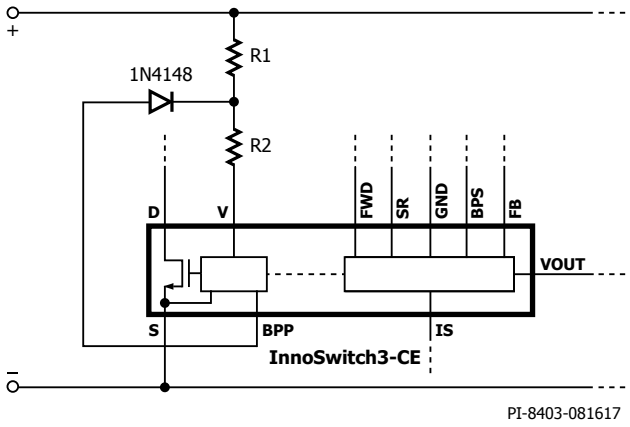
At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review Drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum Drain current for the primary MOSFET should be below the specified absolute maximum ratings.

Thermal Check

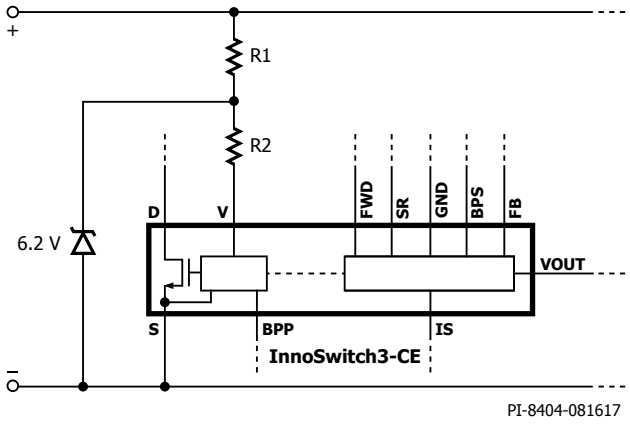
At specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for InnoSwitch3 IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of MOSFET $R_{DS(ON)}$. At low-line, maximum power, a maximum InnoSwitch3 SOURCE pin temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

Simple Circuit Ideas

Line OV Only
Diode biased from BPP and provides constant current into the VOLTAGE pin via R2 above I_{UV} threshold, thus disabling UV function of the IC.



Line UV Only
Zener clamps the voltage on R1-R2 node and provides constant voltage above I_{UV} thresholds, thus disabling OV function of the IC.



Fast AC Reset for IC with OV Latch Function
Diode allows VOLTAGE pin to monitor line voltage for OV/UV detection. A capacitor is sized to filter the line ripple. C_S must be small to allow the VOLTAGE pin to discharge fast enough to go below the I_{UV-} threshold in order to reset the latch.

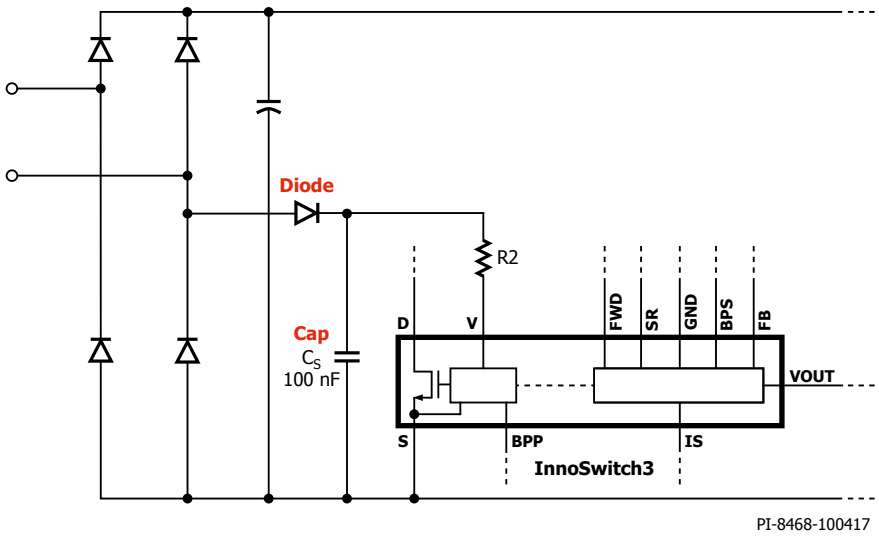
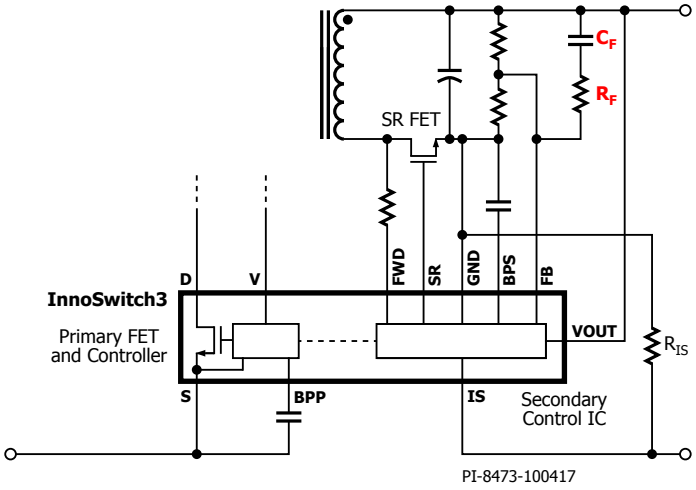
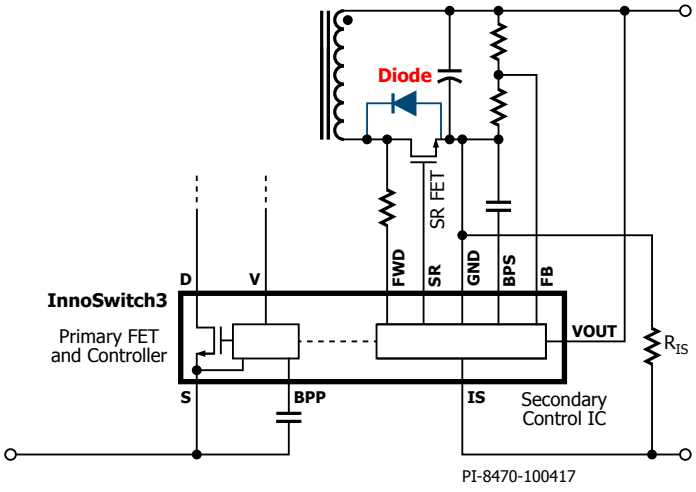


Figure 27. Circuit Ideas to Enhance Design.

RC Network Across RFB_{UPPER}
In some applications where low output ripple voltage is required, it is necessary to speed up the feedback sensing by adding an RC phase-boost network circuit in parallel with upper feedback resistor. A good starting value is 1 nF and 1 kΩ.



Diode Across SR FET
Putting a Schottky diode across the SR FET may further increase efficiency by 0.1 to 0.2% depending on the input and the SR FET used.



Capacitor Across OUTPUT VOLTAGE-GROUND Pins
Putting a small ceramic capacitor (up to 10 μF) from OUTPUT VOLTAGE to GROUND pins can reduce output ripple

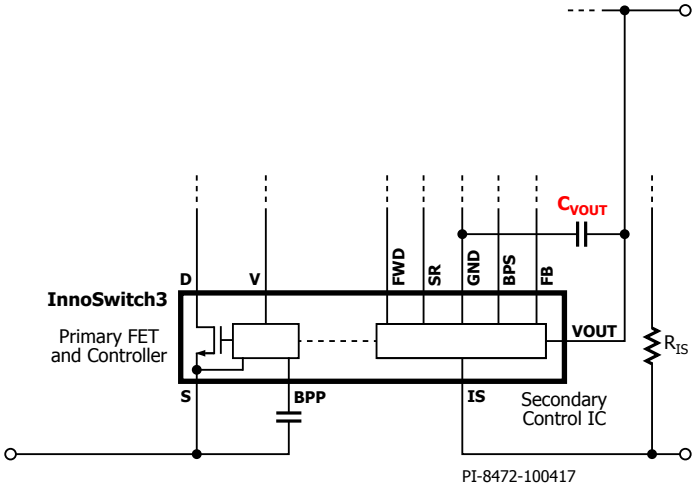
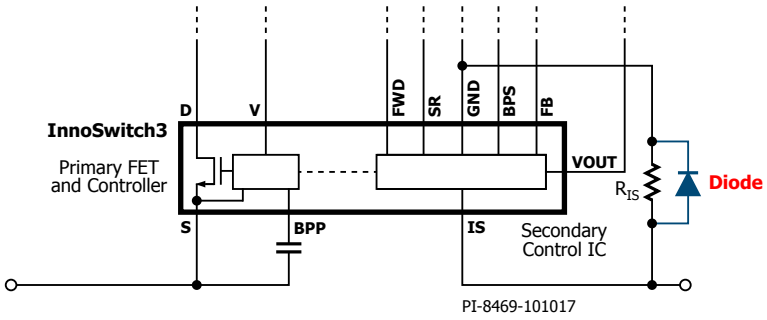
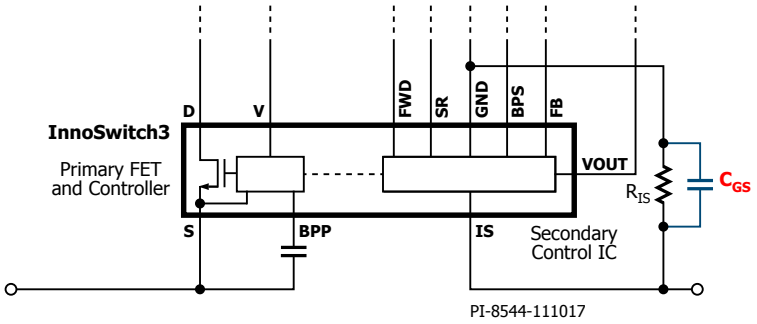


Figure 27 (cont.). Circuit Ideas to Enhance Design.

Diode Across Current Sense R_{IS}
A diode (Schottky or ultrafast) positioned across the current sense resistor (R_{IS}) acts as a bypass for very high surge of current and voltage during short-circuit which could potentially damage R_{IS}. This is more likely for designs with high output voltage and high output filter capacitance.



Capacitor Across Current Sense R_{IS}
Putting a capacitor (10 - 100 nF) across IS and GND pins when R_{IS} is placed somewhat away from the IC will reduce pulse grouping (bunching) in CC operation.



Enable/Disable Circuit
Use two switches, Q1 (PNP) and Q2 (NPN), to control the current flowing into V pin to Enable/Disable circuit with logic level signal.

Logic High – Disable: V pin current = $(V_{BPP} / (R1//R2)) > I_{OV+}$
Logic Low – Enable: V pin current = $I_{UV+} < (V_{BPP} / R1) < I_{OV+}$

Note: InnoSwitch needs to be turned on first before receiving Logic High signal due to Innoswitch's own start-up sequence.

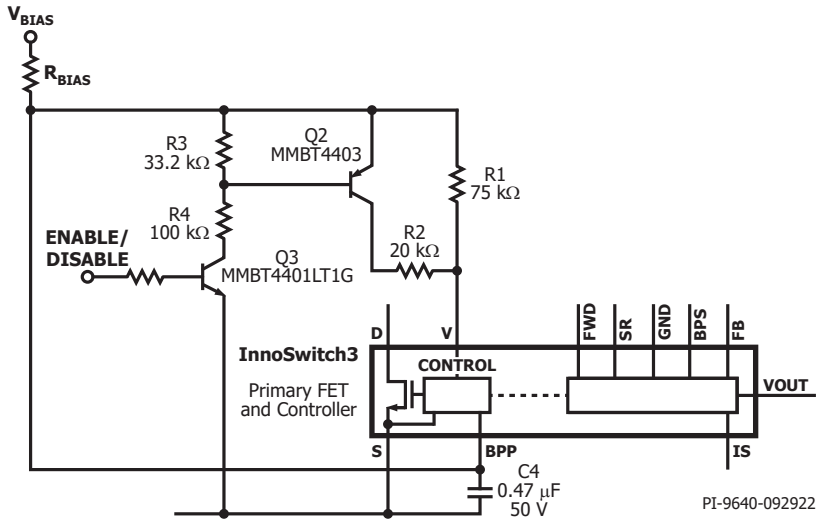


Figure 27 (cont.). Circuit Ideas to Enhance Design.

Application Examples

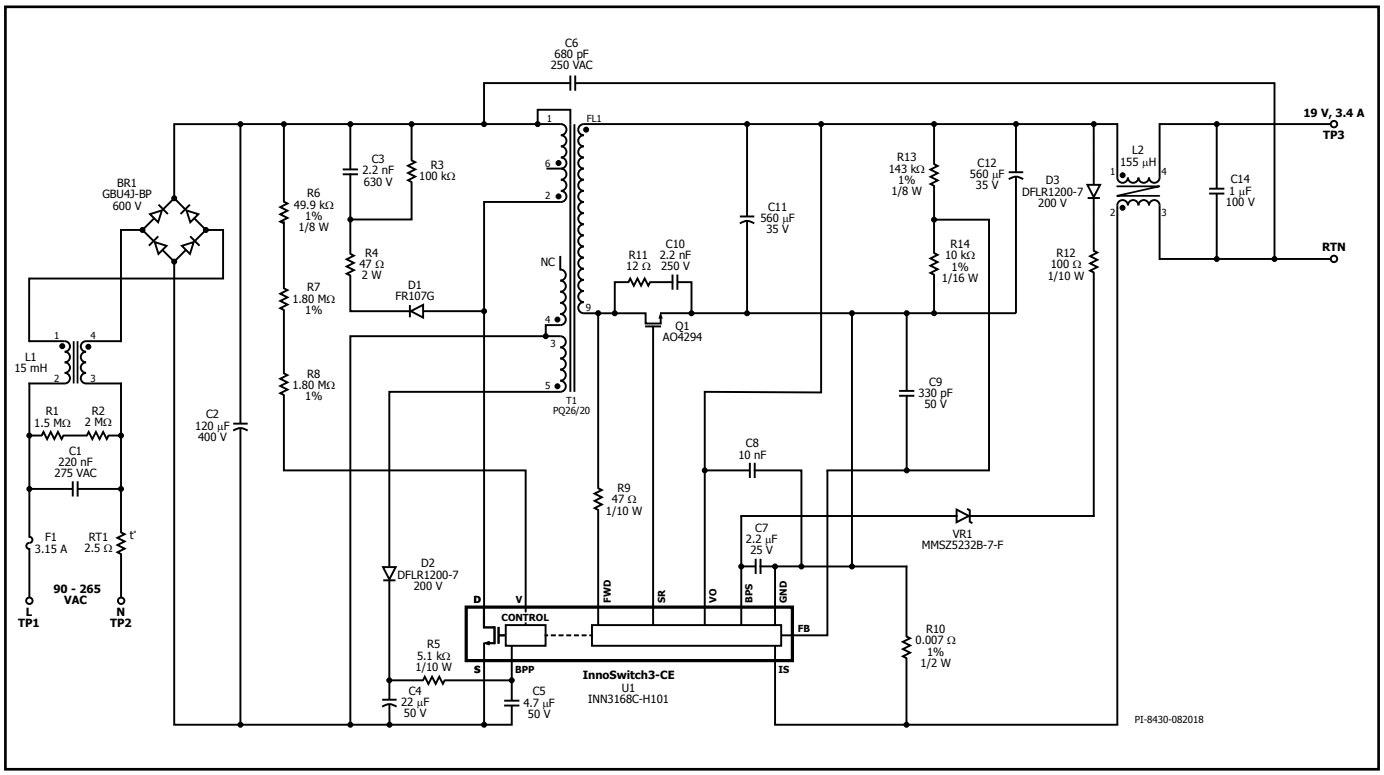


Figure 28. Schematic of DER-535 65 W, 19 V Power Supply using INN3168C.

A High Efficiency, 65 W Universal Input Power Supply (InnoSwitch3-CE)

The circuit shown in Figure 28 delivers 65 W (19 V at 3.4 A) at higher than 90% average efficiency from 90 VAC to 265 VAC input using INN3168C.

The bleeding resistors, R1 and R2, are used to discharge the stored energy in C1 to meet safety requirement. The input capacitor C2 is sufficient to maintain full output power delivery at 90 VAC input, and Resistors R6, R7, and R8 provide line voltage sensing. At approximately 100 V DC, the current through these resistors exceeds the line undervoltage threshold, which enables U1. At approximately 420 V DC, the current through these resistors exceeds the line overvoltage threshold, disabling U1. A low cost RCD clamp formed by D1, R3, R4, and C3 limits the peak drain voltage due to the interaction of transformer leakage reactance with output trace inductance.

The secondary-side of the INN3168C provides output voltage and output current sensing, and provides drive to a synchronous rectification MOSFET. Output rectification for the 19 V output is provided by SR FET Q1. Very low ESR capacitors, C11 and C12, provide filtering. RC snubber network comprising R11 and C10 for Q1 damps high frequency ringing across the SR FET, which results from leakage of the transformer windings and the secondary trace. Capacitor C8 protects U1 from ESD. Adding a small SMD ceramic capacitor between the OUTPUT VOLTAGE pin and the GROUND pin improves ESD and surge protection. The OVP sensing Zener diode, VR1, provides secondary-side output over voltage protection via R12. Output common mode choke L2 reduces high frequency common mode noise and protects U1 from common mode surge.

A heat spreader is required to keep the InnoSwitch3 device below 110 °C when operating under full load, low-line, while at maximum ambient temperature.

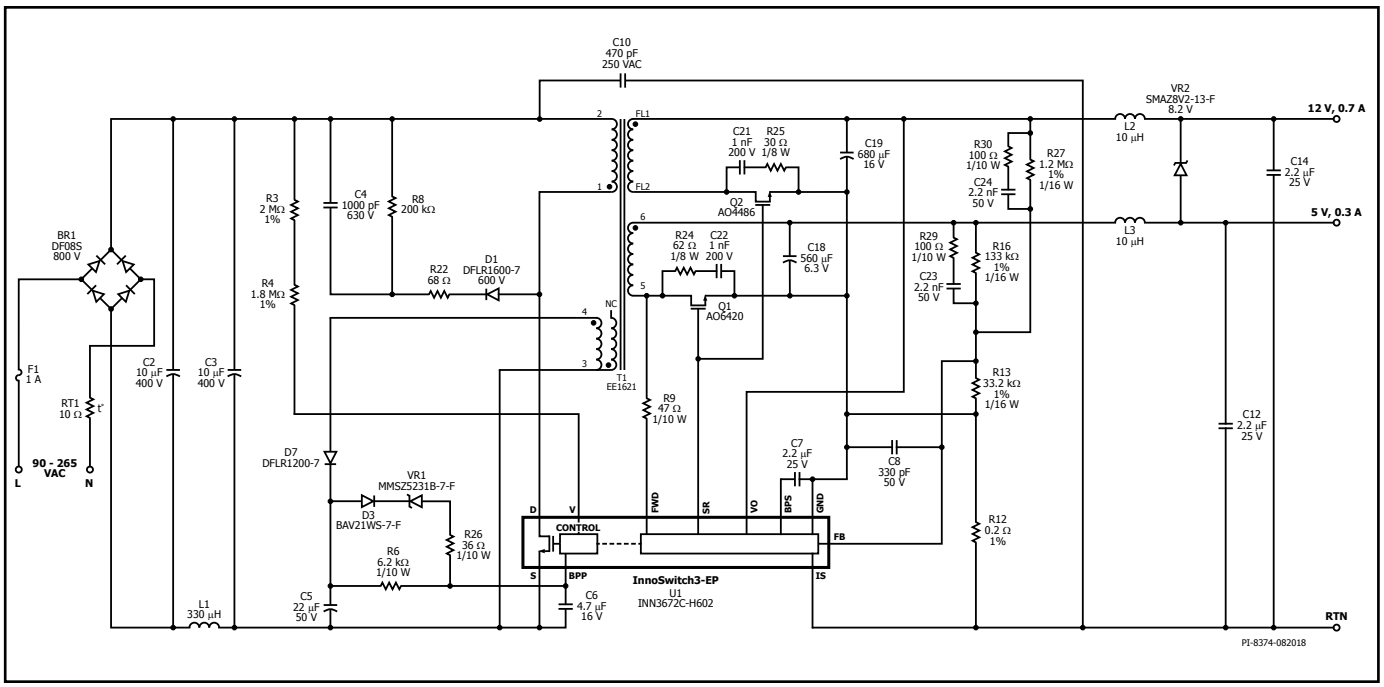


Figure 29. Schematic DER-611, 5 V, 0.3 A and 12 V, 0.7 A for HVAC (Heating, Ventilation and Air-Conditioning) Application.

A High Efficiency, 10 W, Dual Output – Universal Input Power Supply (InnoSwitch3-EP)

The circuit in Figure 29 delivers 10 W output power from 90 VAC to 265 VAC input. Higher than 84% efficiency at 90 VAC input at full load is achieved (using INN3672C from the InnoSwitch3-EP family), and provides accurate cross regulation between two outputs with two SR FETs.

Primary-side overvoltage protection is obtained using Zener diode VR1. In the event of overvoltage occurred on any output, the increased voltage at the output of the bias winding causes the Zener diode VR1 to conduct and triggers the OVP latch in the primary-side controller of the InnoSwitch3-EP IC.

Output rectification of the 5 V output is provided by SR FET Q1, and output rectification of the 12 V output is provided by SR FET Q2. The timing of Q1 and Q2 turn-on is controlled by the 5 V winding voltage sensed via R9 and the FORWARD pin of the IC. Resistor R16, R27 and R13 form a voltage divider network that senses the output voltage from both outputs to provide better cross-regulation. The feedback current ratio between 12 V and 5 V outputs is 1:3 to provide better regulation on the 5 V output and good cross regulation. Feedback compensation networks comprising capacitors C23 and C24 reduce output ripple voltage. Capacitor C8 provides decoupling to prevent high frequency noise interfering with power supply operation. Zener diode VR2 improves the cross regulation when the 5 V output only is fully loaded when no-load is present on the 12 V output.

Revision	Notes	Date
A	Initial release.	10/18
B	Updated caption text in Figure 21.	06/19
C	Updated equation in Figure 18b.	01/20
D	Added PowiGaN information.	05/20
E	Updated page 19 equations.	07/22
F	Added new Enable/Disable Circuit on page 34.	09/22

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