compared to the voltage-mode design that overshoots quite a bit. If we now zoom in on the output voltage for the current-mode design, we can see a negative answer: this is typical of current mode. If we injected more compensation ramp, the current-mode undershoot would increase until it became similar to that of the voltage mode. It would be an overcompensated design.

We can see through this example the good behavior of the k factor with current-mode supplies, mainly first-order systems in the low-frequency portion (before subharmonic poles). In some cases, designers might prefer to manually place the poles and zeros after the crossover frequency has been chosen. This is possible with the type 2 amplifier, and the derivation has been documented in App. 3C. You mainly select your pole and zero locations and calculate the resistor R_2 to generate the right gain at f_c.

3.6.10 The Current-Mode Model and Transient Steps

The current-mode model, in its CCM, DCM, or autotoggling versions, puts a rather heavy burden on the SPICE numerical solver. As a result, simulations can sometimes fail to properly converge when the step occurs in transient runs. The ac analysis does not usually show any problem since the operating point is calculated before the simulation starts. But in transient, some particular modes can lead to trouble. Here is a quick guide to get rid of the convergence issues in transient:

- This is one drawback of the current-mode autotoggling model: if during the transient you transition between the two modes, CCM or DCM, then the resonating capacitor connection or disconnection can lead to convergence issues. The best thing is to then put a star at the beginning of the SPICE code that describes the capacitor expression in the PWMCM subcircuit, as suggested below:

```
* C1 c p C=V(mode) > 0.1 ? {4/((L)*(6.28*Fs)^2)} : 1p ; IsSpice
* XC1 c p mode varicap                              ; PSpice
```

- Increase the transient iteration limit which is the number of trials before a data point is rejected. By default, *ITL4* = 100. Increasing to 300 to 500 helps to solve "Time step too small" errors.
- Relax the relative tolerance *RELTOL* to 0.01.
- If it still fails, relax the absolute current and voltage error tolerance, respectively, *ABSTOL* and *VNTOL*. Values such as 1 μ for *ABSTOL* and 1 m for *VNTOL* usually help a lot.
- Increase *GMIN* to 1 nS or 10 nS. *GMIN* is the minimum conductance in each branch. It helps convergence in deep nonlinear circuits by linearly routing some current out of the nonlinear element.

3.7 FEEDBACK WITH THE TL431

Showing compensation circuits around an op amp is an interesting thing, but the industrial design world differs in reality. The TL431 presence in feedback systems is overwhelming, and few designs still use a true operational amplifier. Why? Because the TL431 already includes a stable and precise reference voltage with an error amplifier. Even if its open-loop gain cannot compete against a true op amp, it is good enough for the vast majority of product definitions. What exactly is a TL431? Figure 3-35a shows the internal arrangement of the device. You can observe a reference voltage of 2.5 V biasing an operational amplifier inverting input.

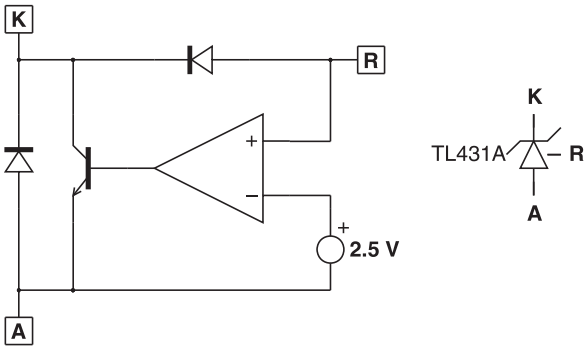

FIGURE 3-35a The internal schematic of the TL431 featuring a 2.5 V reference voltage.

The output drives a bipolar transistor, actually making the TL431 a shunt regulator: when the voltage on the reference pin (R) is below 2.5 V, the transistor remains open, and the TL431 is transparent to the circuit. As soon as the voltage exceeds the reference, the transistor starts to conduct and a current circulates inside the device. If an optocoupler LED appears in series with the cathode, it becomes possible to build an opto-isolated feedback system. Figure 3-35b shows how most of today's power supplies implement a TL431: here, in a typical flyback converter.

The TL431 also exists in different precision versions, depending on what you are looking for. In some cases where you need output voltages below 2.5 V, the TLV431 might be a good choice. The latter also features a smaller minimum biasing current compared to the TL431. It can be a good advantage in low-standby-power designs. The following array compares all versions.

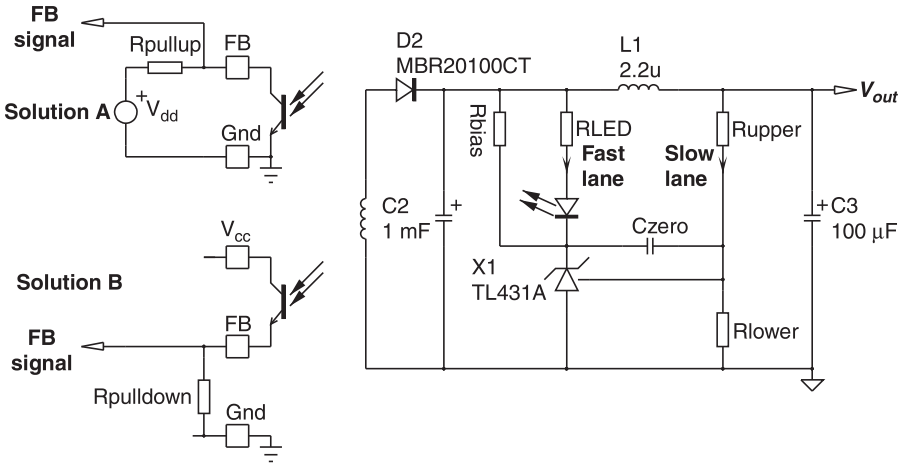

FIGURE 3-35b A TL431 monitors a portion of the output voltage and activates an optocoupler LED to transmit the feedback information to the nonisolated primary side.

Reference	V_{ref}	$I_{bias,min}$	Precision	Max. voltage	Max. current
TL431I	2.495 V	1 mA	± 2% @ 25 °C	36 V	100 mA
TL431A	2.495 V	1 mA	± 1% @ 25 °C	36 V	100 mA
TL431B	2.495 V	1 mA	± 0.4% @25 °C	36 V	100 mA
TLV431A	1.24 V	100 µA	± 1% @25 °C	1 V	20 mA
TLV431B	1.24 V	100 µA	± 0.5% @25 °C	1 V	20 mA

Appendix 3B describes the SPICE models of a behavioral TL431, which we extensively used in all the book examples. This model can work on *IsSpice* or *PSpice* and has proved to properly reflect reality.

In Fig. 3-35b, the resistive network $R_{upper}-R_{lower}$ senses the output voltage and biases the TL431 reference pin. When the output is above the reference, the TL431 reduces its cathode voltage and increases the LED current. This, in turn, reduces the feedback set point, and the converter delivers less power. On the contrary, when the output is below the target, the TL431 almost leaves the cathode open and stops pumping current into the LED. As a result, the primary feedback allows for more output power, pushing the converter to increase the output voltage until the TL431 detects the target is reached. The converter can accept two different optocoupler configurations, described as solutions A and B:

- *Solution A*: This is a common emitter configuration as found on popular controllers such as ON Semiconductor's NCP1200 series. Bringing the FB pin down reduces the peak current in this current-mode controller. This solution also exists on UC384X-based designs where the collector can directly drive the output of the internal op amp.
- *Solution B*: In this common collector configuration, the emitter pulls high the FB pin to reduce the duty cycle or the peak current set point. This option usually requires an inverting amplifier inside the controller.

As you can see in Fig. 3-35b, the LED branch is called the "fast lane" whereas the divider network is tagged "slow lane." The slow lane uses the internal op amp to drive the TL431 output transistor and fixes the dc operating point via the resistive network divider $R_{upper} - R_{lower}$. Thanks to the presence of the capacitor C_{zero}, it is possible to introduce an origin pole and thus roll off the gain as a standard type 1 amplifier would do. Alas! Above a certain frequency range, because C_{zero} has completely rolled off the gain, the shunt regulator no longer behaves as a controlled zener diode. The internal op amp still fixes the dc bias point but no longer ac controls the shunt regulator as its gain has gone to a low value via the impedance of C_{zero}. The sketch thus simplifies to Fig. 3-36 (with solution A, for instance) where the TL431 becomes a simple zener diode. For the small-signal study, we can replace this diode by a fixed voltage in series with its internal impedance, the LED undergoing the same translation. However, as the sum of these dynamic resistors remains small compared to R_{LED}, we can easily neglect them in the final calculation.

From Kirchhoff's law,

$$V_{FB}(s) = -I_1 R_{pullup}\text{CTR} \tag{3-53}$$

where CTR represents the optocoupler current transfer ratio, a gain linking the quantity of photons collected by the transistor base and the collector current they engender: $I_c = I_1\text{CTR}$. Considering constant the LED voltage drop and the zener voltage, their derivative terms are zero in the small-signal analysis, therefore:

$$I_1 = \frac{V_{out}(s)}{R_{LED}} \tag{3-54}$$

Substituting Eq. (3-54) into Eq. (3-53) gives

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup}}{R_{LED}}\text{CTR} \tag{3-55}$$

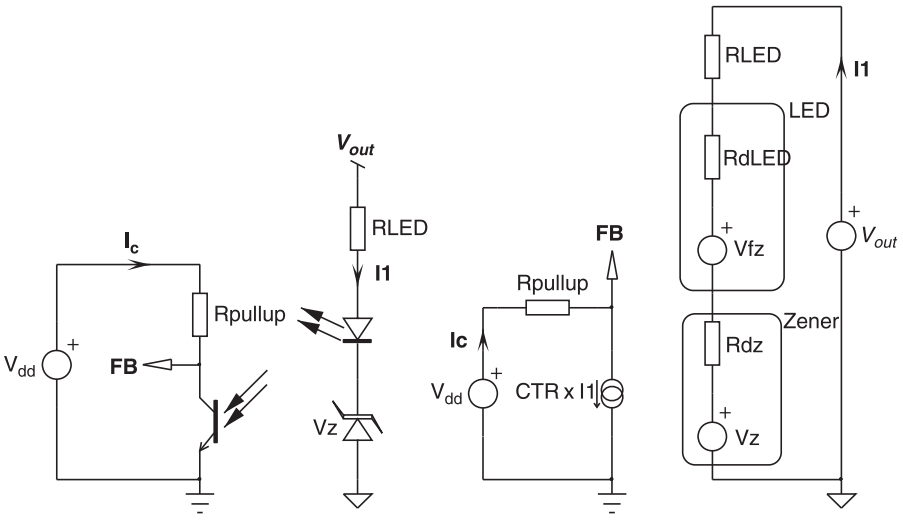

FIGURE 3-36 The small-signal model includes various dynamic resistors, but they are of low value compared to the series resistor R_{LED}.

This equation describes the "fast lane" gain that you simply cannot roll off. It also sheds light on the selection of R_{LED}: it obviously cannot be made solely on bias current considerations as it affects the loop gain. Bias current will rely on the resistor R_{bias} whose current does not cross the optocoupler LED and thus does not play a role in the gain definition. For Fig. 3-35b solution B, the result is almost similar to the Eq. (3-55) result, except that there is no phase reversal as with the common collector structure.

Once the operating principle is understood, the final TL431 representation makes more sense, as Fig. 3-37 shows. You can see the standard op amp having a capacitor C_{zero} but followed by an adder network representative of the fast lane. Note in Fig. 3-35b that the LED

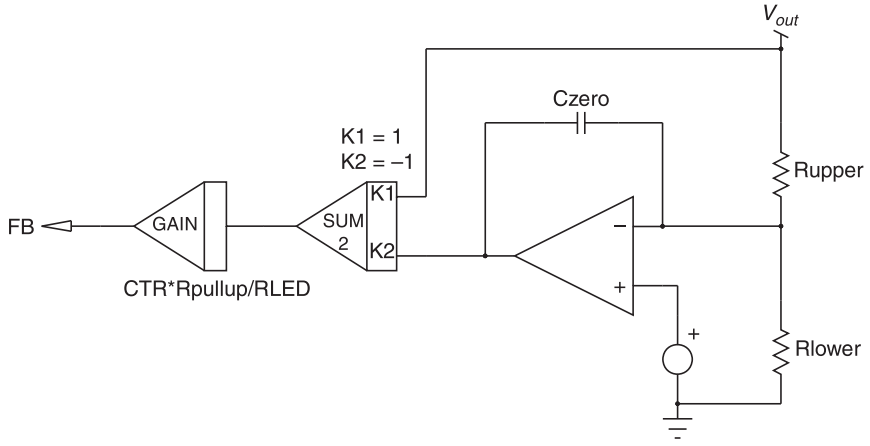

FIGURE 3-37 From this sketch, the fast lane can easily be identified.

connects *before* the secondary *LC* filter. This is done to avoid offering gain at high frequency when the *LC* network starts to resonate. This configuration is typical of flyback converters featuring high-frequency noise reduction via an *LC* filter. Make sure the resonant frequency of this filter is placed at least 10 times above the selected crossover frequency to avoid any interaction.

As it is placed, C_{zero} capacitor looks as if it introduces an origin pole. However, if we derive the transfer function of this complete feedback chain, we get the following results:

$$V_{FB}(s) = \left(V_{out}(s) \frac{1}{sR_{upper}C_{zero}} + V_{out}(s) \right) \frac{R_{pullup}}{R_{LED}} \text{CTR} \tag{3-56}$$

Rearranging the equation gives

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\left(\frac{1}{sR_{upper}C_{zero}} + 1 \right) \frac{R_{pullup}}{R_{LED}} \text{CTR} = -\left(\frac{sR_{upper}C_{zero} + 1}{sR_{upper}C_{zero}} \right) \frac{R_{pullup}}{R_{LED}} \text{CTR} \tag{3-57}$$

Equation (3-57) reveals the presence of an origin pole, f_{po} (as suspected . . .) plus a zero, f_z, introduced by the fast lane configuration. Unfortunately, if we want a type 2 amplifier, which is the most common type, we need a pole f_p somewhere. How can we obtain it? Simply by placing a capacitor from the output node to ground (Fig. 3-38a and b). If we update Eq. (3-57) with the presence of this pole, we obtain the final equation ruling the TL431 network as presented by Fig. 3-35b:

$$G(s) = \frac{V_{FB}(s)}{V_{out}(s)} = -\left(\frac{sR_{upper}C_{zero} + 1}{sR_{upper}C_{zero}} \right) \left(\frac{1}{1 + sR_{pullup}C_{pole}} \right) \frac{R_{pullup}}{R_{LED}} \text{CTR} \tag{3-58}$$

As usual, we can evaluate poles and the zero positions through the following definitions:

$$f_{po} = \frac{1}{2\pi R_{upper}C_{zero}} \tag{3-59}$$

$$f_z = \frac{1}{2\pi R_{upper}C_{zero}} \tag{3-60a}$$

$$f_p = \frac{1}{2\pi R_{pullup}C_{pole}} \tag{3-60b}$$

$$G = \frac{R_{pullup}}{R_{LED}} \text{CTR} \tag{3-61}$$

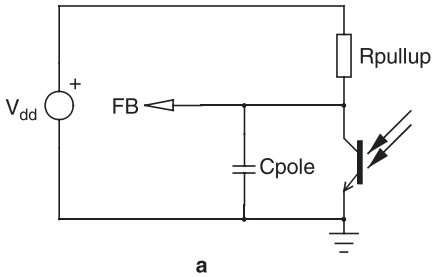

FIGURE 3-38a A simple capacitor placed between the feedback pin and ground introduces a pole.

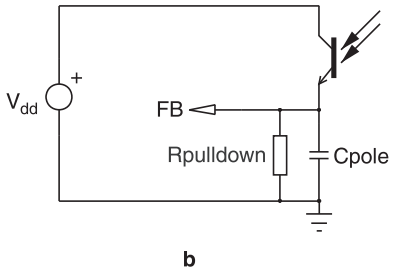

FIGURE 3-38b The same applies to a common collector configuration.