200mA Low Power Consumption CMOS LDO Regulator

DSZ6821.0E; 1/07

CLZ6821/22

General Description

The CLZ6821 is a positive LDO regulator designed on patent pending CMOS circuit technologies. The device attains high ripple rejection ratio and superior line and load transient response in spite of only 6uA current consumption. The output voltage is presetable to the voltages in the range from 1.5V to 4.5V in 0.1V increments by means of laser trimming process. The CLZ6821 consists of a voltage reference, an error amplifier, an output trimming resistor network, a short circuit protection and over-current protector, a phase compensation and a chip enable circuit. A low ESR capacitor such as ceramic capacitor is acceptable. An internal low-on-resistance PMOS pass transistor provides low dropout output voltage. The ultra low current consumption and the chip enable (CLZ6821 only) interface ensure long battery life.

It quickly goes into fast response mode with a large load current therefore it can react to fast and asynchronous DRAM refresh operation under low quiescent current mode without any external control signal.

Package

CLZ6821 : SOT-23-5, SC-70-5

CLZ6822 : SOT-23-3

Features

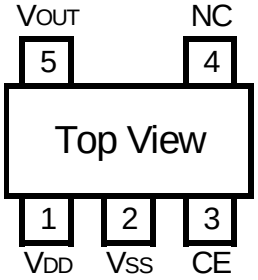
- **Low power consumption ··· 6μA (light load less than 3mA), 45μA (50mA load)**
- **Low standby current ····· 50nA**
- **Fast load transient response 40mV drop (V_{OUT} =2.8V, I_{OUT} =0.1~50mA, C_O =4.7μF)**
- **Output voltage ····· 1.5V~4.5V**
- **Output current ··· 200mA (V_{DD} =V_{OUT} +1.0V)**
- **Output voltage accuracy ····· ±2.0%**
- **Low drop out voltage ··· 0.25V (V_{OUT}=2.8V, V_{DD}=3.8V, I_{OUT} =200mA)**
- **Ripple Rejection ····· 70dB at 1kHz**
- **Over current limiter ····· 350mA**
- **Short-circuit current ····· 20mA**
- **Low ESR capacitor ····· C=0.47-10μF, ESR=0.1mΩ-10Ω**

Applications

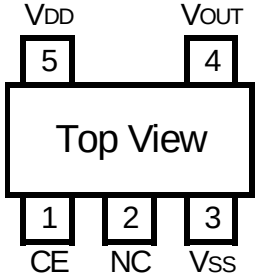
- **Personal communication equipment**
- **Camera, Video, Game**
- **Personal AV equipment**
- **Home electronic appliance**
- **Battery-powered equipment**

Pin Configuration

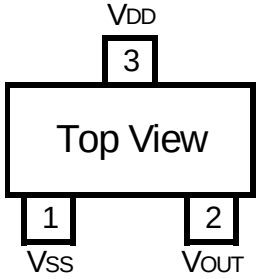
CLZ6821
SOT-23-5/ SC-70-5



CLZ6821
SC-70-5 (R)



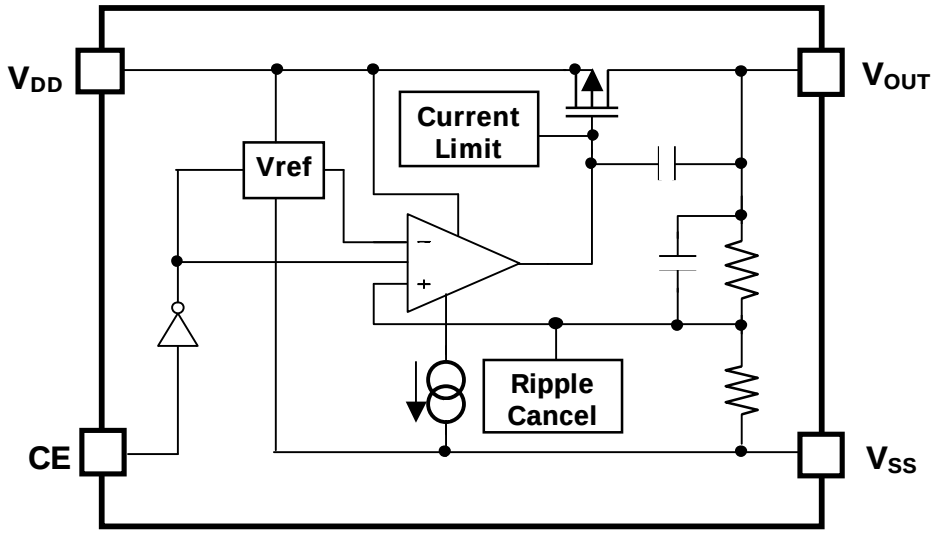
CLZ6822
SOT-23-3



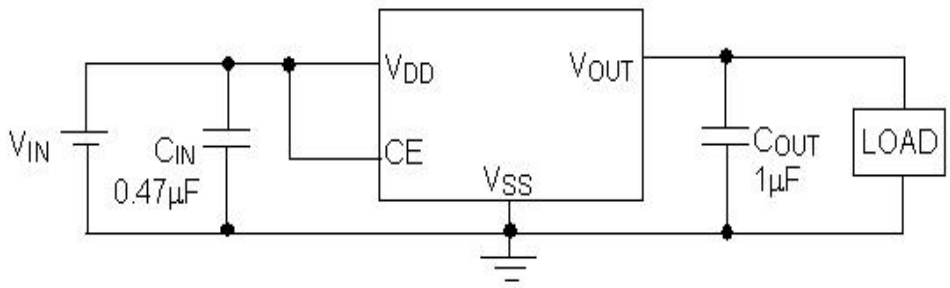
Pin Description

Pin Number			Name	Description
SOT-23-5 / SC-70-5	SC-70-5 (R)	SOT-23-3		
1	5	3	V_{DD}	Unregulated input power
2	3	1	V_{SS}	Ground
3	1		CE	Enable/ Shutdown (Input), CMOS compatible. Logic high = enable; logic low = shutdown. Do not leave open
4	2		NC	No connection
5	4	2	V_{OUT}	Regulated output power

Block Diagram



Typical Application



Ordering Information

CLZ6821 - X X X X X X

- T : Tape & Reel
  U : Tube
- Package Type
  B : SOT-23-5
  F : SC-70-5
  FA : SC-70-5 (R)
- Operating Temperature Range
  M : -40 to +85°C with Green Package
- Output Voltage
  15 : 1.5V
  :
  33 : 3.3V

CLZ6822 - X X X X X X

- T : Tape & Reel
  U : Tube
- Package Type
  A : SOT-23-3
- Operating Temperature Range
  M : -40 to +85°C with Green Package
- Output Voltage
  15 : 1.5V
  :
  33 : 3.3V

Marking

SOT-23-3 : 8 6 1 X X

- Output Voltage
  15 : 1.5V
  :
  33 : 3.3V

SOT-23-5 : 8 6 1 X X

- Output Voltage
  15 : 1.5V
  :
  33 : 3.3V

SC-70-5 : 8 6 X

- Output Voltage
  E : 1.5V
  F : 1.8V
  G : 2.5V
  H : 2.8V
  J : 3.3V
- 86 : SC-70-5
  86 : SC-70-5 (R)

Absolute Maximum Ratings

Supply Voltage (V_{DD}) 6V
Output Current (I_{OUT}) 300mA
CE input voltage ..... VDD+0.3V
Ambient Temperature Range (T_A) ... -40°C to 85°C
Storage temperature .....-55°C to +125°C

Thermal Information

Thermal Resistance (θ_{JA})
SOT-23 ..... 250°C/W
SC-70-5 ..... 333°C/W
Junction Temperature Range .....-40°C to +125°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V, T_A = 25°C, C_{IN} = C_{out} = 1μF/ Ceramic , unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{DD}				5.5	V
Output Voltage (Note 1)	V_{OUT}	I_{OUT} =50mA	-2		+2	%
Output Current	I_{OUT}	V_{DD} =V_{OUT} +1.0V	200			mA
Current Limit	I_{LIM}	V_{DD} =V_{OUT} +1.0V, V_{CE} =V_{DD}		300		mA
Dropout Voltage	V_{DO}	1.5≦V_{OUT}≦1.8, I_{OUT} =200mA		500	650	mV
		1.8<V_{OUT}≦2.4, I_{OUT} =200mA		350	500	mV
		2.4<V_{OUT}≦3.5, I_{OUT} =200mA		250	400	mV
		3.5<V_{OUT}≦4.5, I_{OUT} =200mA		200	300	mV
Ground Current	I_{SS1}	V_{DD} =V_{CE} =V_{OUT} +1.0V, I_{OUT} =0mA, V_{OUT} =2.8V		6	9	μA
	I_{SS2}	V_{DD} =V_{CE} =V_{OUT} +1.0V, I_{OUT} =50mA, V_{OUT} =1.8V		45	60	μA
	I_{SS0}	V_{DD} =V_{OUT} +1.0V, V_{CE} =V_{SS}			50	nA
Short-circuit Current	I_{SHORT}	V_{DD} =V_{OUT} +1.0V, V_{CE} =V_{DD}, RL=0		20		mA
Line Regulation	V_{LNR}	I_{OUT} =100mA, V_{OUT}+0.5V≦V_{DD}≦5.5V		0.05	0.2	%/V
Load Regulation	V_{LDR}	V_{DD} =V_{OUT} +1.0V, 1mA≦I_{OUT}≦200mA			40	mV
V_{OUT} Temp. Coefficient		V_{DD} =V_{OUT} +1.0V, I_{OUT} =50mA, -40°C≦T_A≦85°C		±100		ppm/°C
Ripple rejection	PSRR	V_{DD} =V_{OUT} +1.0V, I_{OUT} =50mA, f=1kHz, Ripple 0.2Vp-p		70		dB
Short-circuit current	I_{SHORT}	V_{DD} =V_{OUT} +1.0V, V_{CE} =V_{DD}, RL=0		20		mA
Input Transient Response	V_{ITR}	(Note 2)			0.05	V
Load Transient Response	V_{OTR}	V_{OUT} =2.8V, V_{DD} =3.8V, C =4.7μF, I_{OUT} =0.1↔50mA, tr =0.5μS		0.02	0.035	V
		V_{OUT} =2.8V, V_{DD} =3.8V, C =4.7μF, I_{OUT} =0.1↔150mA, tr =0.5μS		0.05	0.1	V
CLZ6821 Only						
CE Transient Response		(Note 3)		200		μsec
CE"H"Level Input Voltage	V_{CEH}	V_{DD} =V_{OUT} +1.0V	1.1		V_{DD}	V
CE"L"Level Input Voltage	V_{CEL}	V_{DD} =V_{OUT} +1.0V			0.25	V
CE"H"Level Input Current	I_{CEH}	V_{DD} =V_{OUT} +1.0V, no pull-down		0.5		μA
CE"L"Level Input Current	I_{CEL}	V_{DD} =V_{OUT} +1.0V		0.01		μA

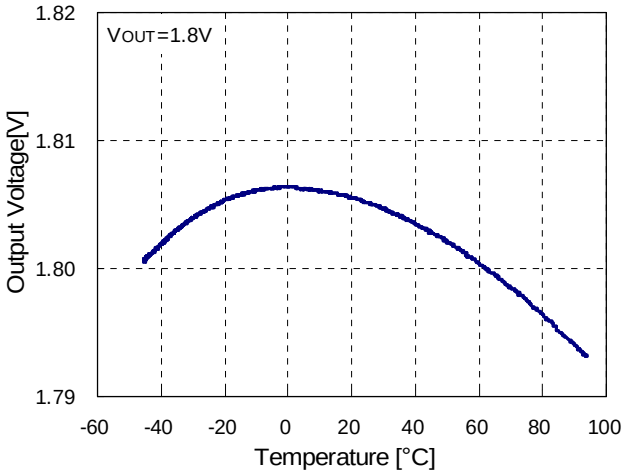
Note 1: V_{OUT}: Actual output voltage; $V_{OUT(S)}$: specified output voltage

Note 2: The output voltage changes when input voltage is changed from V_{OUT} +1.0V to V_{OUT} +2.0V or from V_{OUT} +2.0V to V_{OUT} +1.0V. Output current I_{OUT} =50mA

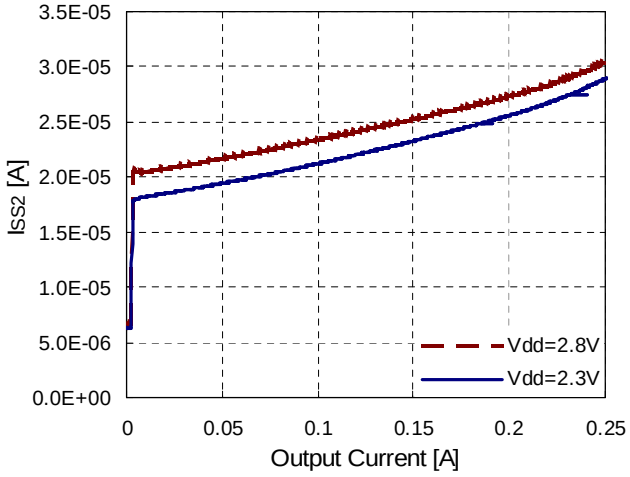
Note 3: The transient time from V_{CE} =1.1V to V_{OUT} =0.98×$V_{OUT(S)}$ when V_{CE} is from 0V to $V_{OUT(S)}$ +1.0V for 5μsec or the transient time from V_{CE} =0.25V to V_{OUT} =0.1×$V_{OUT(S)}$ when V_{CE} is from $V_{OUT(S)}$ +1.0V to 0V for 5μsec. Output current I_{OUT} =50mA

Typical Performance Characteristics

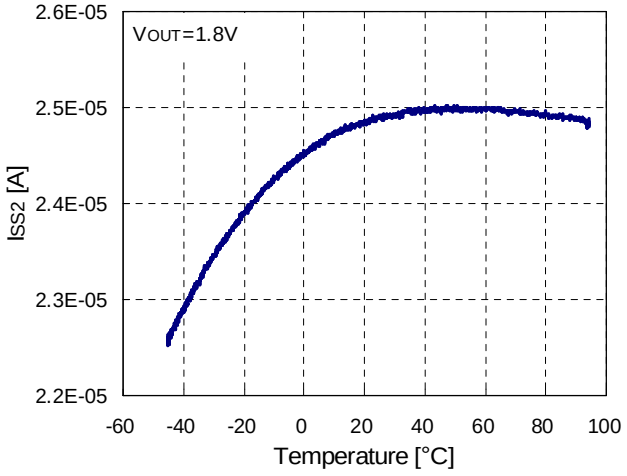
Output Voltage vs. Temperature



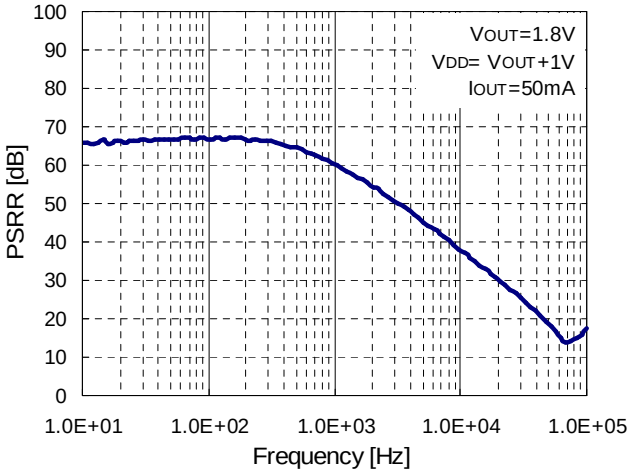
Ground Current vs. Output Current



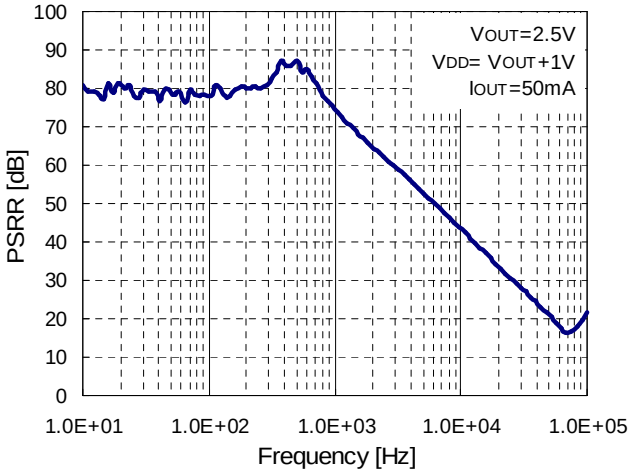
Ground Current vs. Temperature



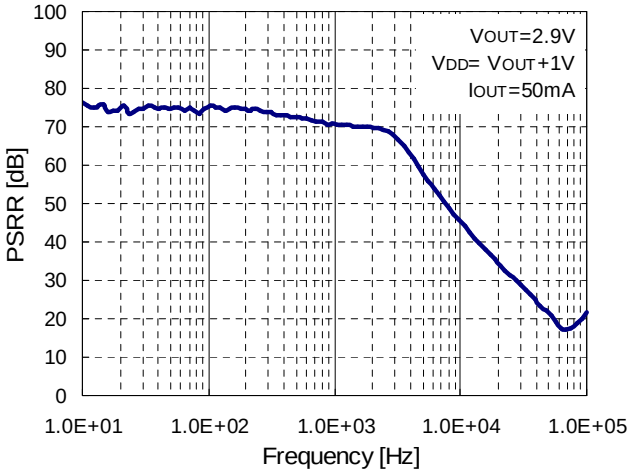
PSRR



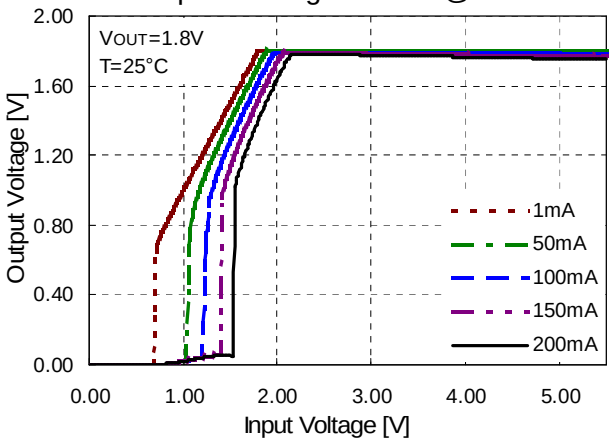
PSRR



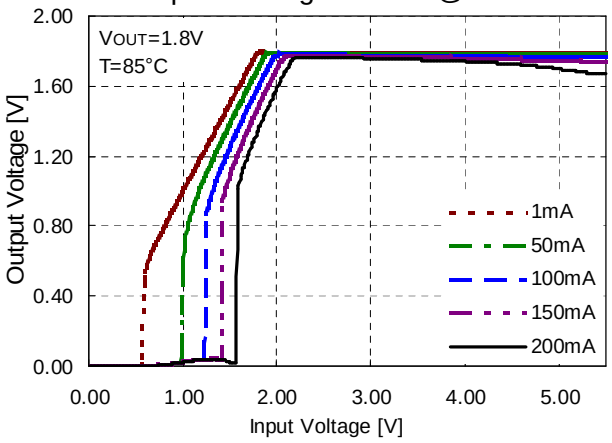
PSRR



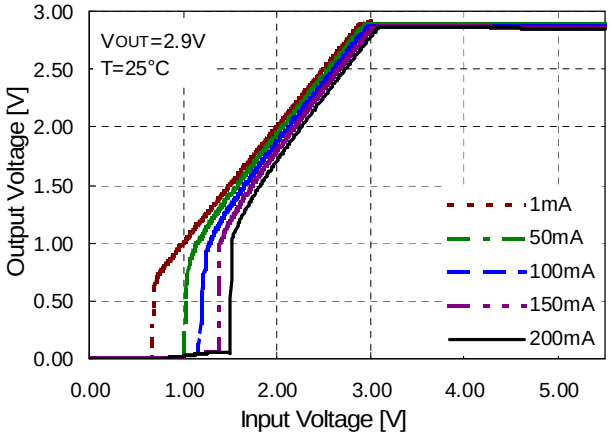
Output Voltage vs. Input Voltage
Dropout Voltage=360mV@200mA



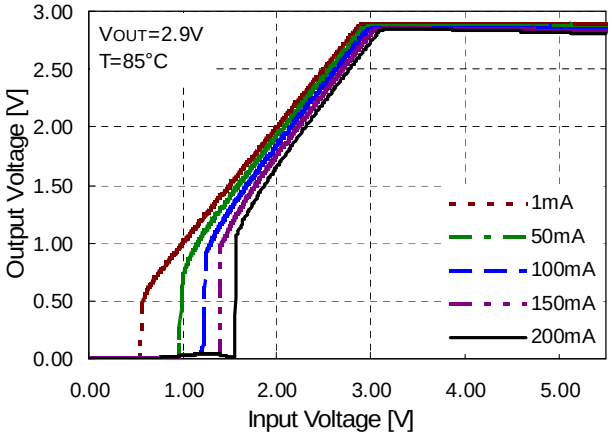
Output Voltage vs. Input Voltage
Dropout Voltage=410mV@200mA



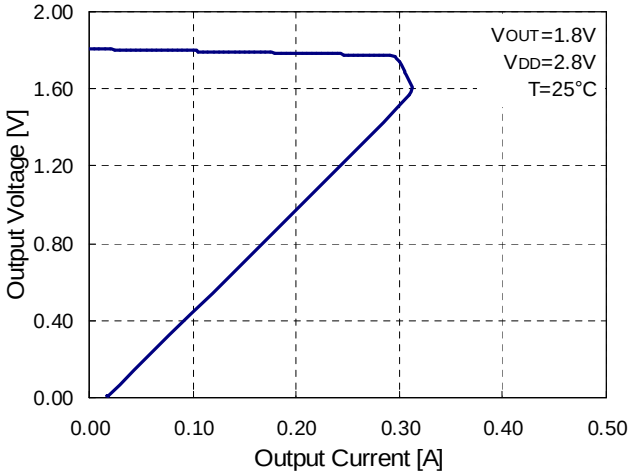
Output Voltage vs. Input Voltage
Dropout Voltage=225mV@200mA



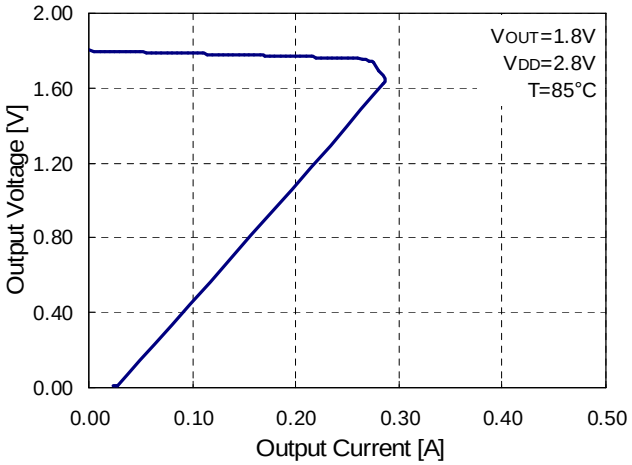
Output Voltage vs. Input Voltage
Dropout Voltage=263mV@200mA



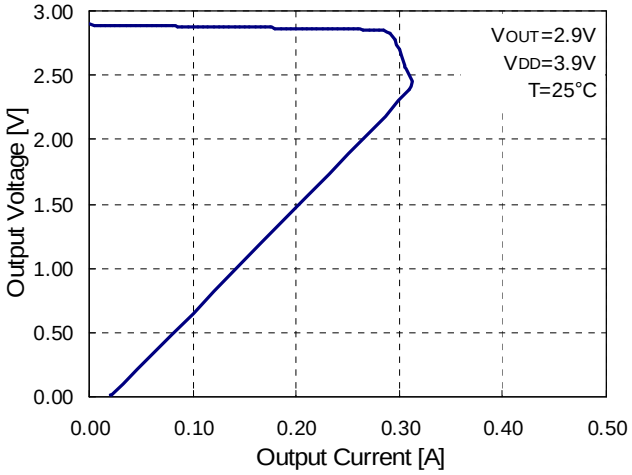
Output Voltage vs. Output Current



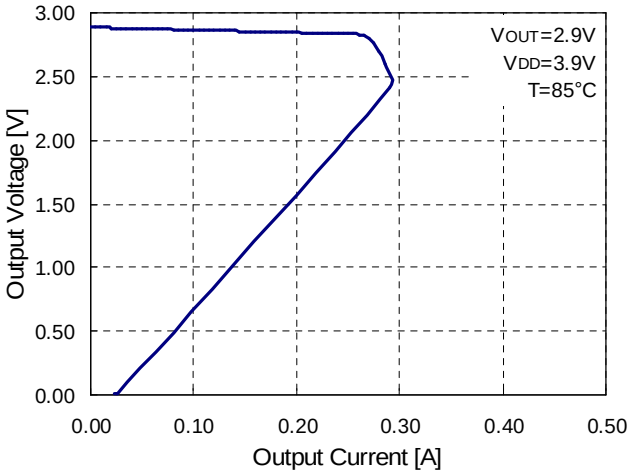
Output Voltage vs. Output Current



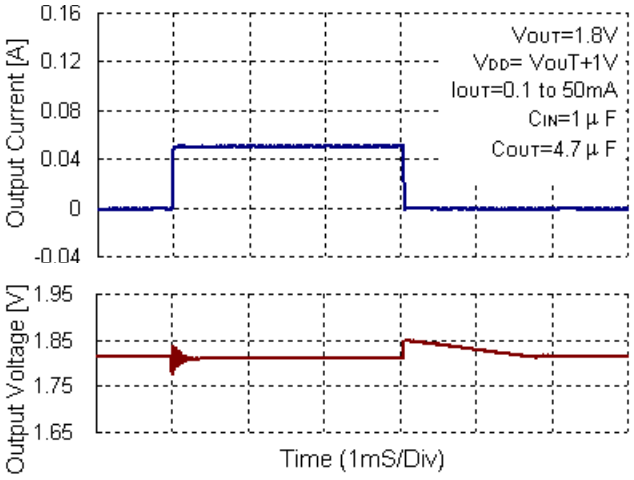
Output Voltage vs. Output Current



Output Voltage vs. Output Current



Load Transient



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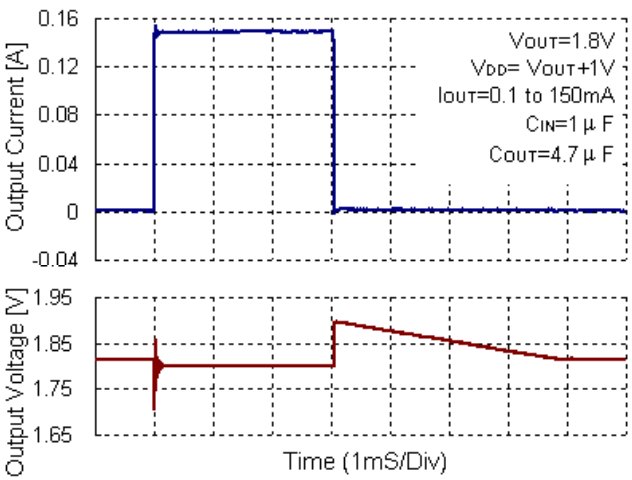

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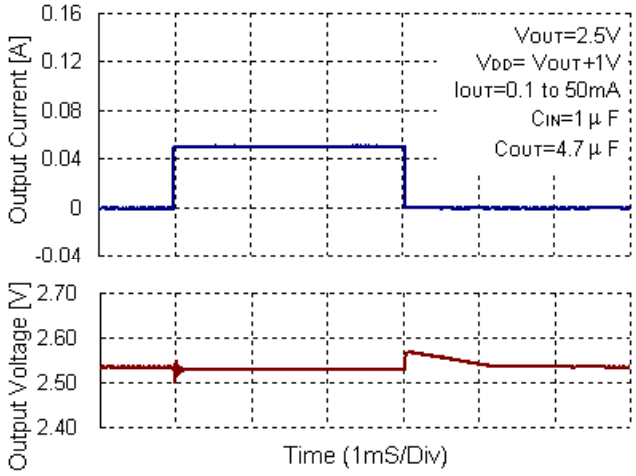

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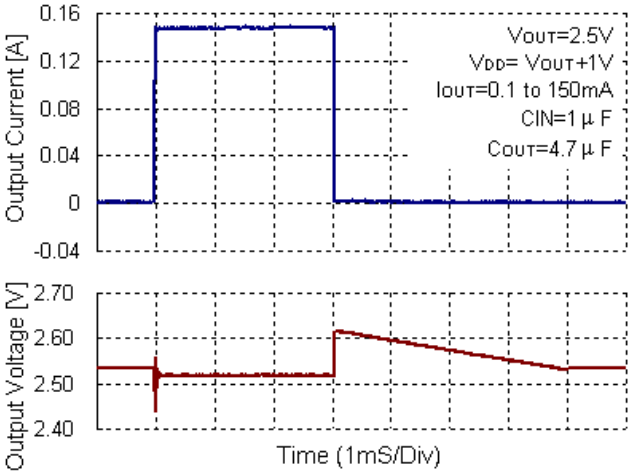

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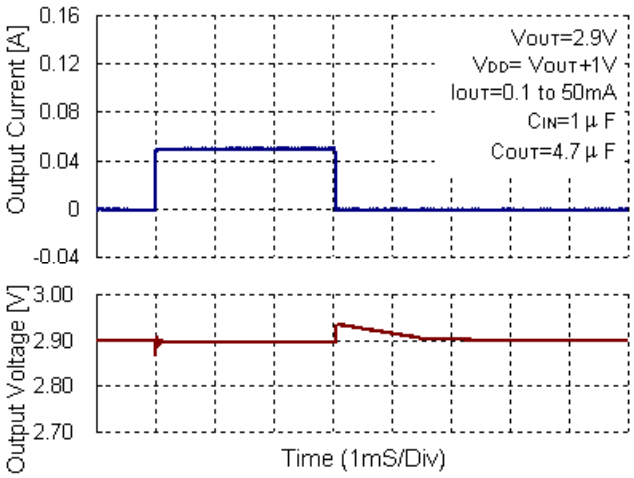
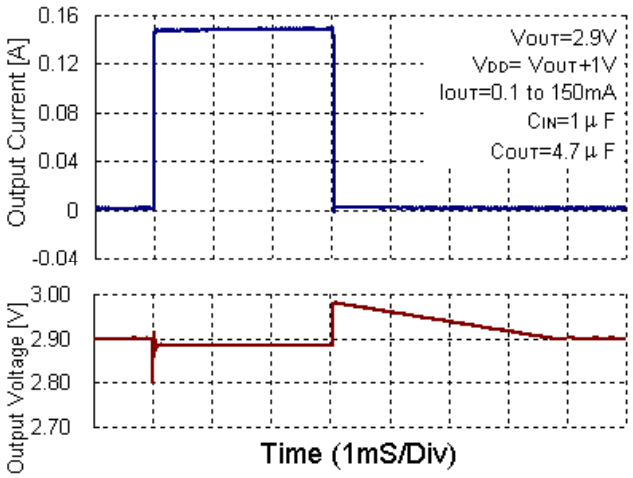
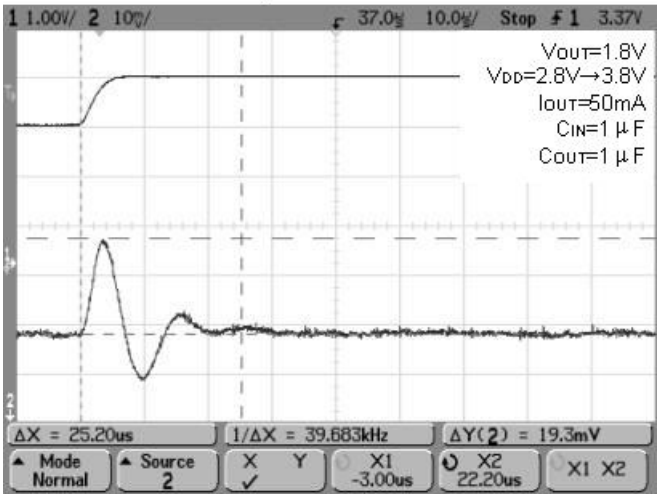


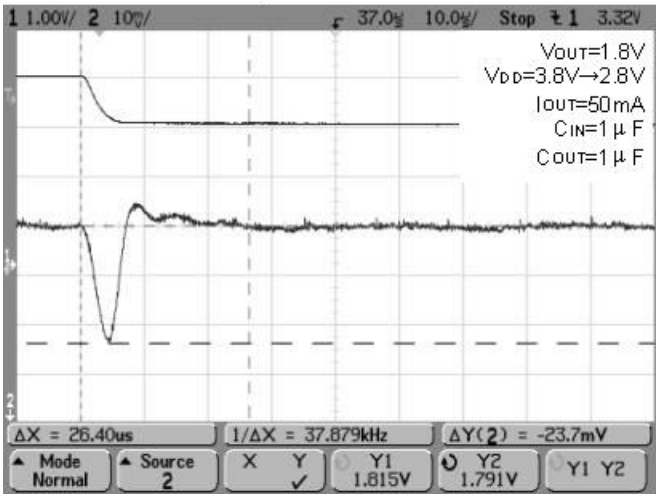
Load Transient



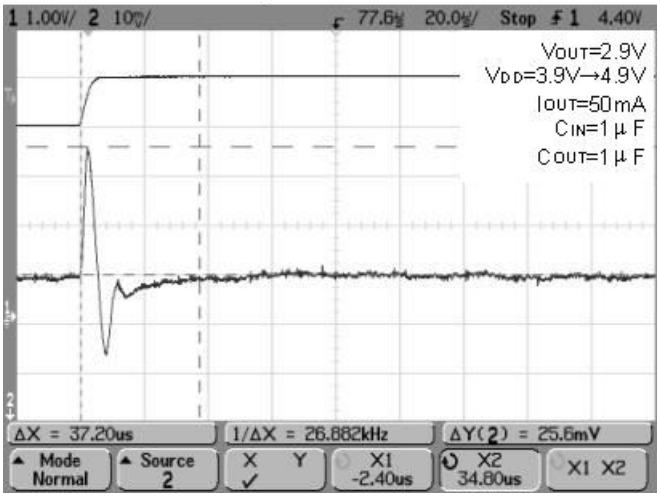
Input Transient



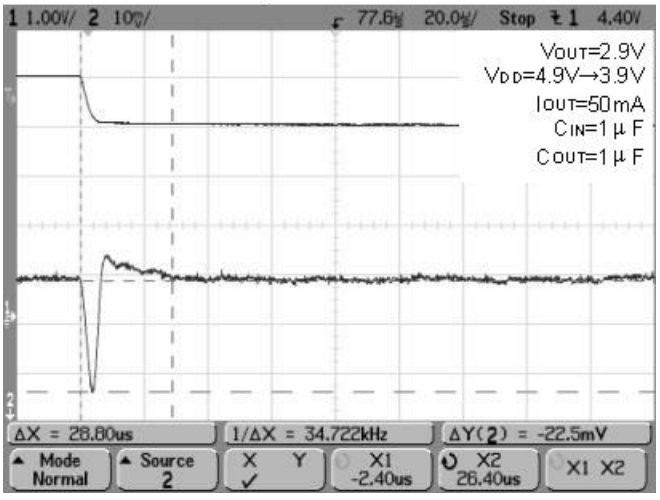
Input Transient



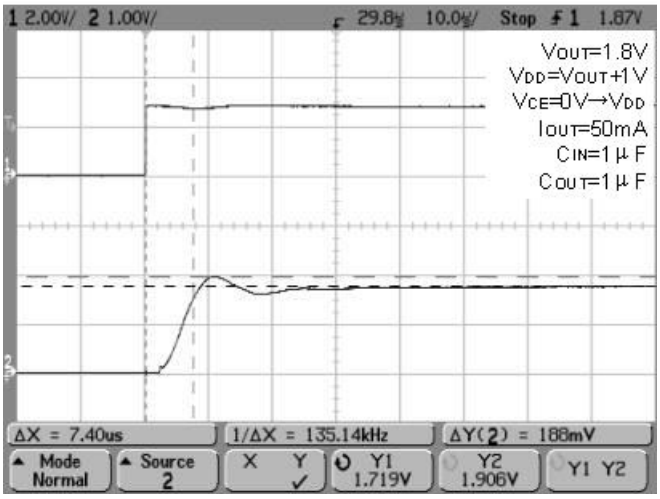
Input Transient



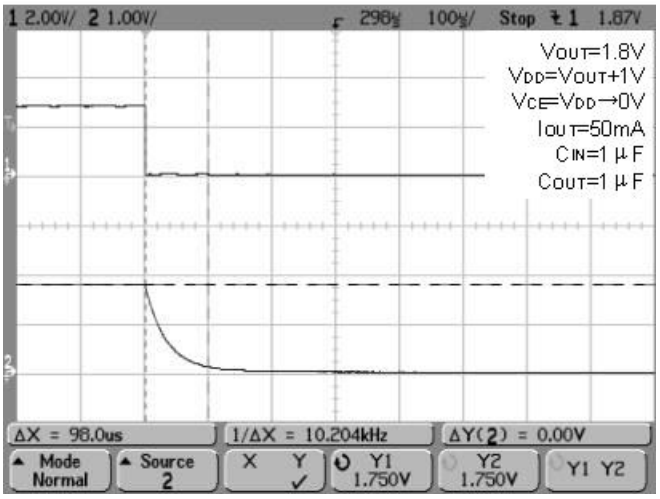
Input Transient



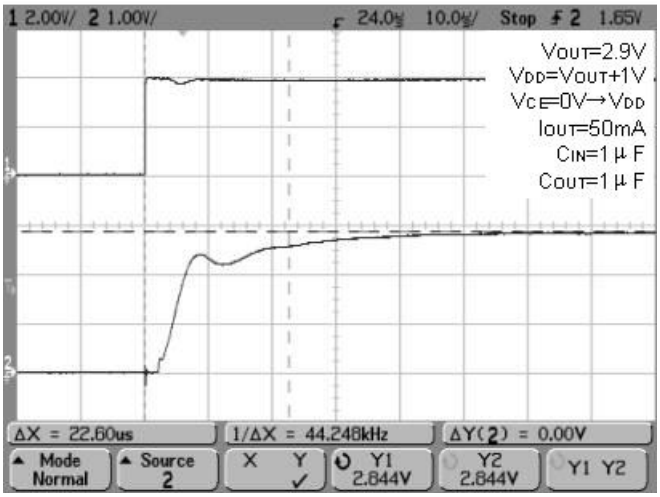
CE Pin Transient



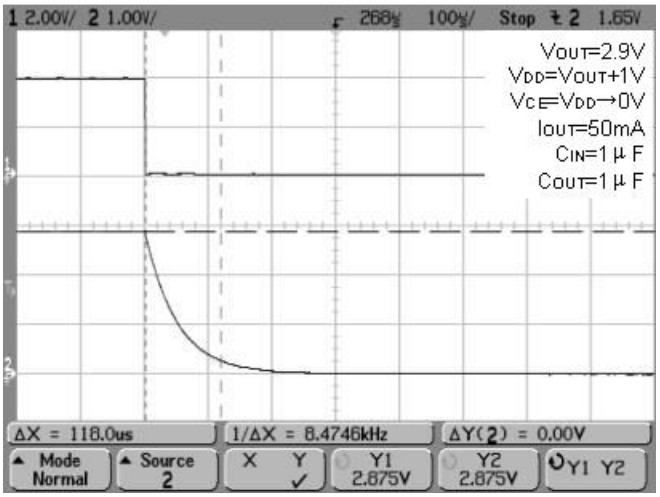
CE Pin Transient



CE Pin Transient



CE Pin Transient



Applications Information

Enable/Shutdown

The enable inputs allow for logic control of output voltage. The enable input is active high, requiring at least 1.1V for guaranteed operation. Forcing the enable pin low disables the output. The enable input is CMOS logic and cannot be left floating.

Input Capacitor

A 1μF capacitor is required from the input pin to ground to provide stability for this high performance device. Low ESR ceramic capacitors provide optimal performance at minimum of space. Additional high-frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high frequency noise and are good practice in any RF based circuit.

Output capacitor

The design requires 1μF or greater on the output to maintain stability. The design is optimized for use with low ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation.

X7R/X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

Thermal Considerations

The CLZ6821/22 is designed to provide 200mA of continuous current in a very small package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

$$P_D\ (max) = (T_J\ (max) - T_A) / \theta_{JA}$$

T_J (max) is the maximum junction temperature of the die, 125°C, and T_A is the ambient operating temperature. θ_{JA} is layout dependent; the junction-to-ambient thermal resistance for the CLZ6821/22 is 250°C/W for SOT-23 with minimum footprint in PCB layout.

The actual power dissipation of the regulator circuit can be determined using the equation:

$$P_D = (V_{DD} - V_{OUT}) \times I_{OUT}$$

Substituting PD(max) for PD and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, when operating the CLZ6821/22 at 50°C with a minimum footprint layout, the maximum input voltage for a set output current can be determined as follows:

$$P_D\ (max) = (125°C - 50°C) / 250°C/W = 300mW$$

The maximum power dissipation must not be exceeded for proper operation. Using the output voltage of 3.0V and an output current of 150mA, the maximum input voltage can be determined. Because this device is CMOS and the ground current is typically 100μA over the load range, the power dissipation contributed by the ground current is < 1% and can be ignored for this calculation.

$300mW = (V_{IN} - 3.0V) \times 150mA$

$300mW = V_{IN} \times 150mA - 450mW$

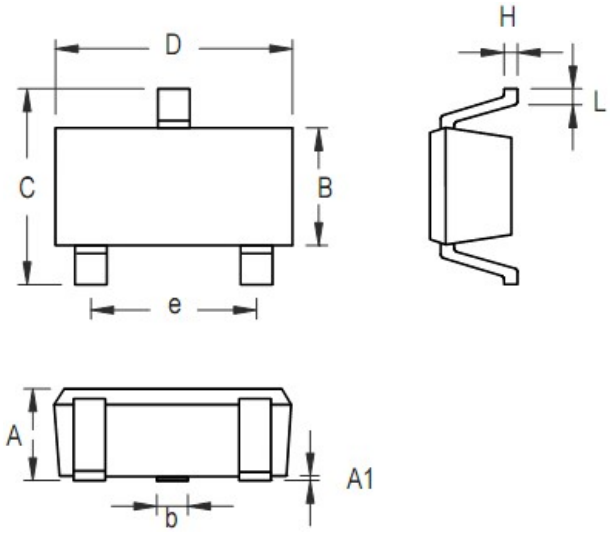
$750mW = V_{IN} \times 150mA$

$V_{IN}\ (max) = 5.0V$

Therefore, a 3.0V application at 150mA of output current can accept a maximum input voltage of 5.0V in a SOT-23 package.

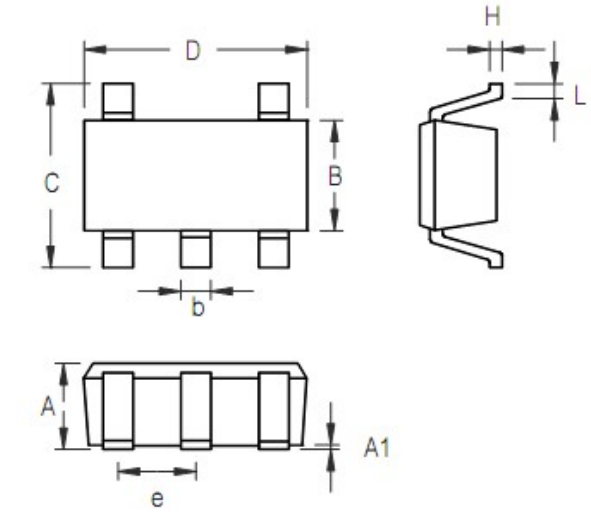
Package Information

SOT-23-3



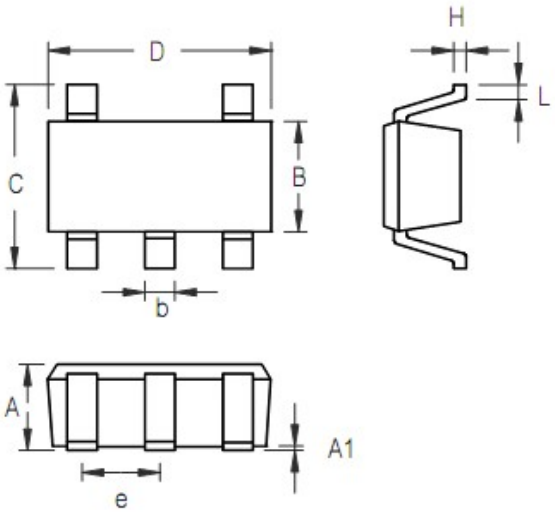
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	1.00	0.028	0.039
A1	0.00	0.10	0.000	0.004
B	1.40	1.80	0.055	0.071
b	0.30	0.51	0.012	0.020
C	2.59	3.00	0.102	0.118
D	2.69	3.10	0.106	0.122
e	1.90 BSC		0.075 BSC	
H	0.08	0.25	0.003	0.010
L	0.30	0.61	0.014	0.024

SOT-23-5



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.35	0.041	0.053
A1	0.05	0.15	0.002	0.006
B	1.50	1.70	0.059	0.067
b	0.30	0.50	0.012	0.020
C	2.60	3.00	0.102	0.118
D	2.80	3.00	0.110	0.118
e	0.95 BSC		0.037 BSC	
H	0.08	0.22	0.003	0.009
L	0.35	0.60	0.014	0.024

SC-70-5



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
B	1.15	1.35	0.045	0.053
b	0.15	0.30	0.006	0.012
C	1.80	2.40	0.071	0.094
D	1.80	2.20	0.071	0.087
e	0.65 BSC		0.026 BSC	
H	0.08	0.22	0.003	0.009
L	0.26	0.46	0.010	0.018