# TinySwitch-5 Family

Integrated Off-Line Switcher with EcoSmart Technology for Highly Efficient Power Supplies

## Product Highlights

### Highly Integrated, Compact Footprint
- Robust 725 V silicon MOSFET provides excellent surge withstand
- Switching frequency up to 150 kHz minimizes transformer size

### EcoSmart™ – Energy Efficient
- Up to 92% efficient, flat across load range
- Less than 30 mW no-load power at 230 VAC including line sense
- Up to 210 mW output power for 300 mW input (230 VAC)
- Lossless primary current sensing

### Reduced Part Count, Design Flexibility
- Frequency jitter reduces EMI filter size
- Integrated soft-start minimizes start-up stress
- Adjustable switching frequency

### Extensive Protection
- Auto-restart limits power delivery to <3% during output short circuit faults
- Output short-circuit, overload and overvoltage protection
- Line undervoltage (UV) detection prevents turn-off glitching
  - Simple, fast AC reset
- Line overvoltage (OV) shutdown
- Accurate thermal shutdown with large hysteresis (OTP)

### Typical Applications
- Auxiliary, standby and bias power supplies for appliances, and consumer products
- Utility meter, smart grid and industrial power supplies

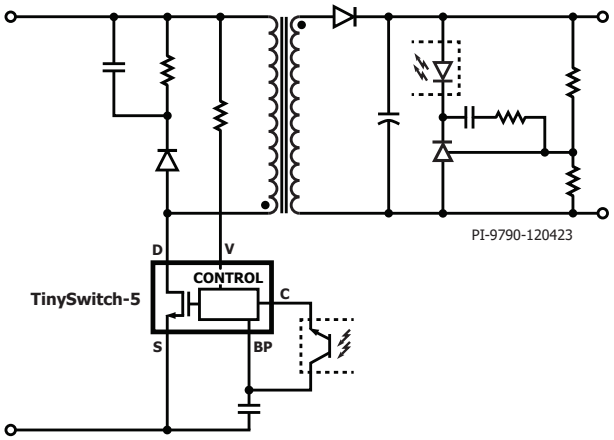



Figure 1. Typical Flyback Application.

| Product Type | Output Power (W) | | |
|---|---|---|---|
| | 400 VDC | 230 VAC | 85-265 VAC |
| eSOP-12 (K) | 25 - 75 | 22 - 70 | 15 - 45 |
| eDIP-12 (V) | 25 - 75 | 22 - 70 | 15 - 45 |
| eSIP-7 (E) | 120 - 190 | 105 - 175 | 70 -120 |

Table 1. Power Range by Package Type.

**eSOP™-12 Package (K Suffix)**
- Low profile surface mount package ultra-slim designs
- Supports wave or reflow soldering
- PCB cooling via SOURCE pin and exposed pad for low EMI

**eDIP™-12 Package (V Suffix)**
- Low profile horizontal orientation for ultra-slim designs
- Suitable for Top heatsink and reflow
- Thermal impedance equivalent to a TO-220 package

**eSIP™-7 Package (E Suffix)**
- Vertical orientation for minimum PCB footprint
- Simple heatsink mounting using clip
- Thermal impedance equivalent to TO-220 package
- Provides extended power range

Figure 2. Packages.

## Output Power Table[1]

| Product[3] | PCB Copper Area[1] | | | Product[3] | Metal Heatsink[1] | | |
|---|---|---|---|---|---|---|---|
| | 400 VDC | 230 VAC ±15% | 85-265 VAC | | 400 VDC | 230 VAC ±15% | 85-265 VAC |
| | **Peak or Open Frame[2,3]** | **Peak or Open Frame[2,3]** | **Peak or Open Frame[2,3]** | | **Peak or Open Frame[2,3]** | **Peak or Open Frame[2,3]** | **Peak or Open Frame[2,3]** |
| **TNY5071K** | 25 W | 22 W | 15 W | **TNY5071V** | 25 W | 22 W | 15 W |
| **TNY5072K** | 35 W | 32 W | 20 W | **TNY5072V** | 35 W | 32 W | 20 W |
| **TNY5073K** | 50 W | 45 W | 30 W | **TNY5073V** | 50 W | 45 W | 30 W |
| **TNY5074K** | 60 W | 55 W | 35 W | **TNY5074V** | 60 W | 55 W | 35 W |
| **TNY5075K** | 75 W | 70 W | 45 W | **TNY5075V** | 75 W | 70 W | 45 W |
| | | | | **TNY5075E** | 120 W | 105 W | 70 W |
| | | | | **TNY5076E** | 150 W | 140 W | 95 W |
| | | | | **TNY5077E** | 190 W | 175 W | 120 W |

Table 2. Output Power Table.

Notes:

1. The power table 2 represents the maximum practical continuous output power based on the following assumptions:
   a. 12 V output.
   b. Schottky output diode.
   c. 130 V reflected voltage ($V_{OR}$) and 85% efficiency.
   d. A 100 VDC minimum DC bus voltage for 85-265 VAC and 300 VDC bus voltage for 230 VAC.
   e. Sufficient heatsinking to keep device temperature ≤110 °C.
   f. Power levels shown for the V package device assume 19.4 cm 2 of 610 g/m 2 copper heatsink area.
   g. Open frame design operating in a +50 °C ambient temperature.
2. Minimum peak power capability.
3. Packages: E: eSIP-7C, V: eDIP-12B, K: eSOP-12B.

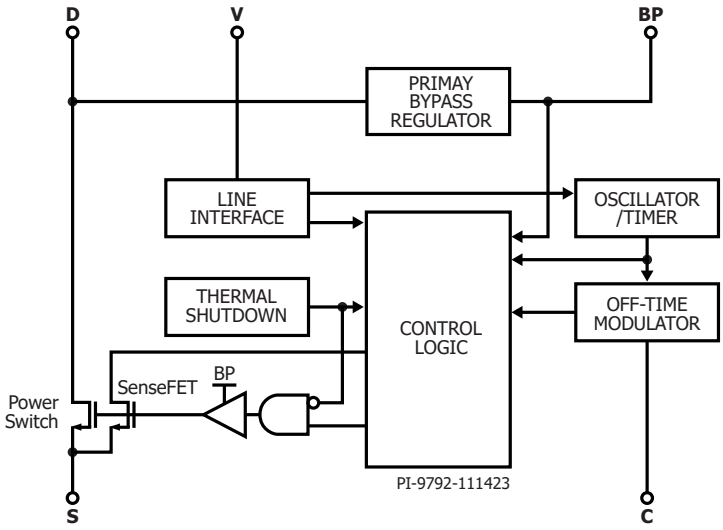



Figure 3. Functional Block Diagram.

## Pin Functional Description

**DRAIN (D) Pin**
Power switch drain connection.

**SOURCE (S) Pin**
These pin(s) are the power switch source connection. Also ground reference for BYPASS pin.

**BYPASS (BP) Pin**
The connection point for an external bypass capacitor for the controller supply.

**VOLTAGE MONITOR (V) Pin**
Pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

**CONTROL (C) Pin**
Feedback control current input pin.

**SIGNAL GROUND (SG) Pin**
SG pin must be connected to Source.

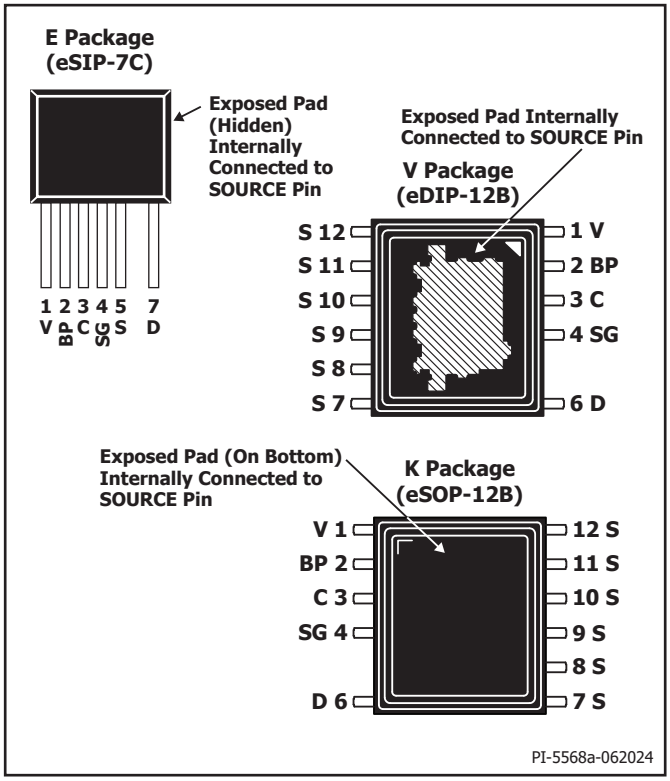



Figure 4. Pin Configuration (Top View).

## TinySwitch-5 Functional Description

The TinySwitch™-5 IC is an integrated switched mode power supply IC that monitors an analog feedback current at the Control input which is then used to modulate the variable frequency variable current control algorithm.

The TinySwitch-5 flyback controller can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The controller consists of a frequency jitter oscillator, a current limit controller, 5 V regulator on the BYPASS pin, BYPASS undervoltage and overvoltage detection circuit, an input line sensing circuit, over-temperature protection, leading edge blanking, and a silicon MOSFET power switch.

**BYPASS Pin Regulator**

The BYPASS pin has an internal regulator that charges the BYPASS pin capacitor to $V_{BP}$ by drawing current from the DRAIN pin whenever the power switch is off. The BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the BYPASS pin capacitor.

In addition, a shunt regulator clamps the BYPASS pin voltage to $V_{SHUNT}$ when current is provided to the BYPASS pin through an external resistor. This allows the TinySwitch-5 IC to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

**Bypass Undervoltage Threshold**

The BYPASS pin undervoltage circuitry disables the power switch when the BYPASS pin voltage drops below ~4.5 V ($V_{BP}$ – $V_{BP(H)}$) in steady-state operation. Once the BYPASS pin voltage falls below this threshold, it must rise to $V_{BP}$ to re-enable turn-on of the power switch.

**Bypass Output Overvoltage Function**

The BYPASS pin has an auto-restart OV protection feature. A Zener diode in parallel with the resistor in series with the BYPASS pin capacitor is typically used to detect an overvoltage on the bias winding and activate the protection mechanism. In the event that the current into the BYPASS pin exceeds $I_{SD}$, the device will disable switching.

**Over-Temperature Protection**

The thermal shutdown circuitry senses the power switch temperature. The threshold is set to $T_{SD}$ with a hysteretic response.

Hysteresis response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

**Off-Time Modulator**

The off-time modulator converts an analog feedback current to off-time duration, which is proportional to the feedback current. This algorithm produces longer off-time as the output load reduces.

At the end, of the off-time cycle, the off-time modulator initiates the on-cycle request to turn-on the integrated power switch.

**Current Limit Operation**

The current limit threshold is proportional to the time between the termination of the previous switching cycle (power switch turns off) and the next switching request.
This characteristic produces a current limit that increases as the switching frequency (load) increases as shown in Figure 5.

At high load, switching cycles have a maximum current that approaches 100% $I_{LIM}$. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

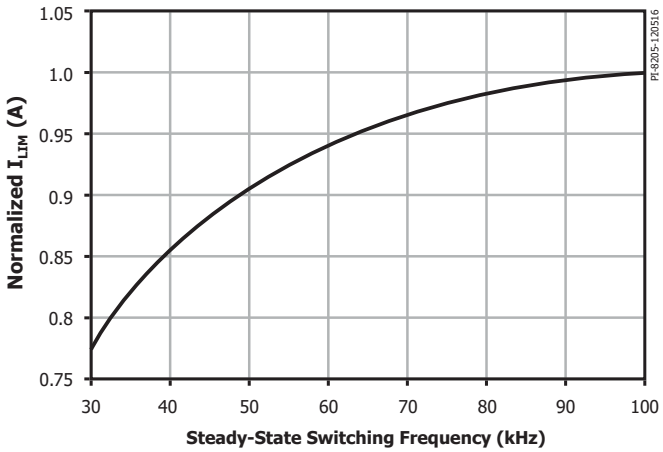



Figure 5. Normalized Current Limit vs Frequency.

**Jitter**

The normalized current limit is modulated between 100% and 94.5% at a modulation frequency of $f_M$.

**SOA Protection**

After two consecutive cycles where the 110% $I_{LIM}$ (100% $I_{LIM}$ is $I_{LIM}$ at 100 kHz) is reached between $t_{LEB}$ and $t_{SOA}$, the controller will interrupt switching for approximately ~20 µs, which is equivalent to approximately 3 cycles at maximum 150 kHz switching frequency. This provides sufficient time for the transformer to reset when delivering power to large capacitive loads without extending the start-up time.

**Input Line Voltage Monitoring**

The VOLTAGE MONITOR (V) pin is used for input undervoltage and overvoltage sensing and protection.

An 8 MΩ resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier along with suitable diode rectification for fast AC reset) and the VOLTAGE MONITOR pin to enable this functionality. This function can be disabled by shorting the VOLTAGE MONITOR pin to the SOURCE pin.

At power-up, after the bypass (BP) capacitor is charged and the $I_{LIM}$ state is set, and (prior to switching) the state of the VOLTAGE MONITOR pin current is checked to confirm that it is above the brown-in ($I_{UV+}$) and below the overvoltage shutdown thresholds ($I_{OV+}$).

In normal operation, if the VOLTAGE MONITOR pin current falls below the brown-out threshold ($I_{UV-}$) and remains below brown-out for longer than $t_{UV-}$, switching is interrupted. Once the VOLTAGE MONITOR pin current is above the brown-in threshold (IUV+), the controller initiates a soft start.

During normal operation, if the VOLTAGE MONITOR pin current increases above the overvoltage threshold ($I_{OV+}$) for longer than $t_{OV+}$, switching is interrupted. Switching will intiate a soft start once the VOLTAGE MONITOR pin current falls below ($I_{OV-}$).

**Maximum On-Time Extension**

On-time extension keeps the cycle on until current limit is reached. If current limit is not reached by $t_{ONEXT(MAX)}$ = 15 µs, the controller terminates the switching cycle.

This feature reduces the minimum input voltage required to maintain regulation, extending hold-up time and minimizing the size of the bulk capacitor required.

**Maximum Switching Frequency**

The maximum switching frequency of the controller is $f_{OSC}$.

**Minimum Off-Time**

The off-time modulator initiates a cycle request to turn ON the integrated power MOSFET switch. The maximum frequency of off-time modulator requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This ensures that there is sufficient reset time after the integrated switch conduction time for the transformer to deliver energy to the load.

**Maximum Duty Cycle**

The power MOSFET is turned off when the current ramps up to the current limit or when the $t_{ONEXT(MAX)}$ limit is reached.

The controller monitors the power MOSFET on-time $t_{MOSFET(ON)}$ and measures the timer $t_{DC(MAX)} = DC_{MAX}/f_{OSC}$ from when the MOSFET turns on. If:

$t_{MOSFET(ON)} \geq t_{DC(MAX)}$, the off-time modulation starts after the MOSFET is turned off.

$t_{MOSFET(ON)} < t_{DC(MAX)}$, the off-time modulation starts after $t_{DC(MAX)}$ timer ends.

**Frequency Soft-Start**

At start-up, the controller linearly ramps the switching frequency up from $f_{SW(STARTUP)}$ over the $t_{SOFT}$ time period.

If the control pin current $I_C$ rises above the $I_{C(TH)}$ threshold within the $t_{SOFT}$ time period, the frequency ramp is immediately aborted and the controller is permitted to go full frequency. This allows the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved.

In the event of a short-circuit or overload at start-up, the controller moves into auto-restart (AR) mode if the control current $I_C$ does not rise above the $I_{C(TH)}$ threshold before the expiration of the $t_{AR}$ time.

## Application Examples

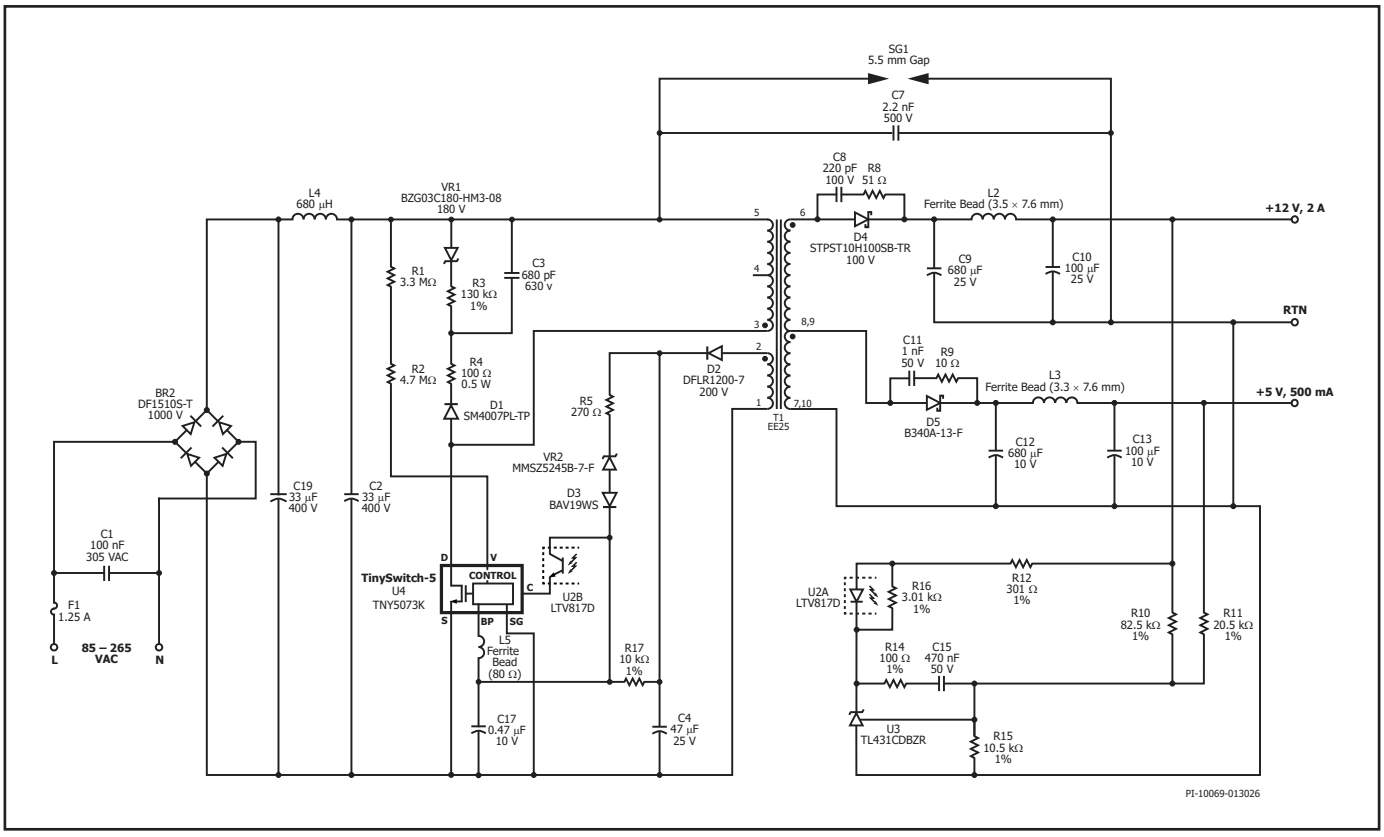



Figure 6. Schematic of RDR-1016 26.5 W, Dual Output Power Supply, 12 V / 2 A and 5 V / 500 mA using TNY5073K.

### A High Efficiency, 27 W Dual Output Power Supply (TinySwitch-5)

The circuit shown in Figure 6 delivers 27 W (12 V at 2 A and 5 V a 500 mA) from 85 VAC to 265 VAC input using TNY5073K.

The supply features line undervoltage lockout, line overvoltage protection, primary sensed output overvoltage auto-restart protection, output short-circuit protection, high 115 VAC full load efficiency (>86%), high 230 VAC full load efficiency (>87%), high average efficiency (>85.5%) and low no-load input power consumption (<50 mW at 230 VAC). Output regulation is accomplished using an optocoupler and a shunt regulator (TL431) feedback.

The input fuse F1 provides protection against excess input current resulting from catastrophic failure of any components in the power supply. The bridge rectifier BR2 rectifies the AC input supply. Capacitors C2 and C19 filter the rectified AC input, and together with inductor L4, form a pi-filter to attenuate differential mode EMI. The X capacitor C1 also helps to reduce differential mode EMI. The Y capacitor C7, connected between the power supply output and input, and reduces common mode EMI. Additionally, the TinySwitch-5 frequency jitter feature reduces EMI. One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the power switch inside the TinySwitch-5 IC (U4).

Line undervoltage and overvoltage thresholds are determined by the current supplied by resistors R1 and R2 to the V pin.

A RCDZ clamp, consisting of diode D1, resistors R3 and R4, capacitor C3, and Zener VR1, limits the peak drain voltage of U4 at the moment the switch inside U4 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The TinySwitch-5 IC is self-starting, using an internal high-voltage current source to charge the primary BYPASS pin capacitor (C17) when AC is first applied. An optional ferrite bead (L5) was used to increase noise immunity. During normal operation, the IC primary controller is powered from a bias winding on the transformer T1. Output of this bias winding is rectified by diode D2 and filtered by capacitor C4. Resistor R17 limits the current being supplied to the TinySwitch-5 IC (U4). Resistor R17 feeds current into the BP pin, inhibiting the internal high-voltage current source that normally maintains the BP pin capacitor voltage (C17) during the internal MOSFET off-time. This design reduces no-load consumption to less than 50 mW at 230 VAC.

Primary sensed OVP can be achieved by connecting a series combination of a Zener diode (VR2), a current limiting resistor (R5), and a blocking diode (D3) from the bias voltage supply to the BYPASS pin. In the event of overvoltage on any output, the increased voltage at the output of the bias winding causes the Zener diode (VR2) to conduct, increasing current into the BP pin. Once the current exceeds current threshold ($I_{SD}$), the TinySwitch-5 will stop switching, and auto-restart will occur until $V_{OUT}$ is within regulation.

Output rectification for the 12 V output is provided by the secondary rectifier diode D4, while the 5V output rectification is accomplished by

secondary rectifier diode D5. An RC snubber network, consisting of R8 and C8 for D4 and R9 and C11 for D5, damps high frequency ringing across the secondary rectifier diodes, which results from leakage inductance in the transformer windings and the secondary trace capacitance.

Very low ESR capacitors, C9 and C12, provide filtering for their respective outputs. Ferrite beads L2 and L3, along with output capacitors C10 and C13, form a low-pass filter that helps reduce output ripple for both 12 V and 5 V outputs.

In the feedback circuit, the output voltages are sensed via the resistor divider R10, R11, and R15. These voltages are regulated to achieve 2.495 V on the TL431 REF pin. The feedback current ratio between the 12 V and 5 V outputs is approximately 1:1, ensuring better output regulation and good cross-regulation. As the cathode voltage changes, the current through the optocoupler LED and transistor within U2 changes. R12, R14 and C15 provide stable operation, while resistor R16 ensures minimum bias to U3. The bias winding voltage was tuned to approximately 10 V at no-load, high line to reduce no-load input power.

Typically, the feedback current into the CONTROL pin at high-line is around 250 μA. This current is sourced from both the bias winding (voltage across C4) and directly from the output, representing a load on the power supply's output. To minimize dissipation from the bias winding under no-load conditions, the number of bias winding turns and the value of C4 were adjusted to achieve a minimum voltage of approximately 10 V across C4. This is the minimum required to keep the optocoupler biased and the output in regulation.

To further minimize dissipation in the secondary-side feedback circuit, a high CTR (300-600%) optocoupler was used. This reduces the secondary-side opto-LED current from around 250 μA to less than 90 μA, thereby reducing the effective load on the output. Additionally, the standard 2.5 V TL431 voltage reference can be replaced with the 1.24 V LMV431, reducing the supply current requirement of this component from 1 mA to 100 μA.

A heat spreader in the form of a PCB copper plane is required to keep the TinySwitch-5 and secondary rectifier diode device below 110 °C when operating.

## Key Application Design Considerations

**Power Table**

The output power table in the data sheet (Table 2) represents the maximum practical continuous output power that can be obtained under the following conditions:

1. The minimum DC input voltage is 85 V or higher for 85 VAC input, and 220 V or higher for 230 VAC input. The input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on input voltage range. Universal input voltage or low line input assumes efficiency >85% increasing to >89% for a high line input. The assumed efficiency is based on the lowest voltage of the input range.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain $K_p$ > 0.4 at a minimum input voltage to provide the maximum power. At high line nominal, it recommended to designed $K_p$ between 1 and 1.1 to increase efficiency.
5. Use low forward voltage drop ($V_F$) Schottky diode for efficiency improvements.
6. The part is board-mounted with SOURCE pins soldered to a sufficient area of copper and/or a heatsink to maintain the device temperature at or below 110 °C at the required highest ambient temperature.
7. An ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters is assumed.
8. A unique feature of TinySwitch-5 IC is that a designer can set the operating switching frequency between 25 kHz to 142 kHz depending on the transformer design. One effective way to lower U4 temperature is to design the transformer to operate at a lower switching frequency, with a good starting point being 66 kHz. If a smaller size transformer is needed, the operating switching frequency can be increased to 130 kHz.

**Overvoltage Protection**

The output overvoltage protection provided by TinySwitch-5 uses an internal protection that is triggered by a threshold current ($I_{SD}$) into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor forms an external filter, providing noise immunity and preventing inadvertent triggering. To ensure the bypass capacitor is effective as a high-frequency filter, it should be placed as close as possible to the SGND and BYPASS pins of the device.

The primary sensed output OVP function can be achieved by connecting a series combination of a Zener diode (VR2), a resistor (R5), and a blocking diode (D3) from the rectified and filtered bias winding voltage supply to the BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended to measure the rectified bias winding voltage, at the lowest input voltage and highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP.

A Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered should be selected. A forward voltage drop of 1 V can be assumed for the blocking diode, and a small signal standard recovery diode is recommended. The blocking diode prevents any reverse current from discharging the bias capacitor during start-up. Finally, the value of the series resistor should be calculated to ensure that a current higher than $I_{SD}$ flows into the PRIMARY BYPASS pin during an output overvoltage event.

**Reducing No-load Consumption.**

The TinySwitch-5 IC starts in self-powered mode, drawing energy from the BYPASS pin capacitor, which is charged from an internal current source. Once the TinySwitch-5 IC begins switching, a bias winding is required to provide supply current to the BYPASS pin. This bias winding supply enables power supplies to achieve low no-load power consumption. The value of resistor $R_{BIAS}$ should be adjusted to achieve the lowest no-load input power.

Additional techniques to further reduce no-load consumption include:

1. Using a low value primary clamp capacitor ($C_{PRI\_SNUB}$).
2. Employing a Schottky or ultrafast diode for the bias supply rectifier ($D_{BIAS}$).
3. Employing high Current Transfer Ratio optocoupler with a CTR of 300-600% (OPTO)
4. Selecting a low ESR capacitor for the bias supply filter capacitor ($C_{BIAS}$).
5. Selecting low ESR for input bulk capacitor ($C_{BULK}$) and output filter capacitor ($C_{OUT}$).
6. Utilizing a low value secondary rectifier diode RC snubber capacitor ($C_{SEC\_SNUB}$).
7. Applying tape between primary winding layers and multi-layer tapes between primary and secondary windings to reduce inter-winding capacitance.

## Component Selection

Figure 7 shows the key external components required for a practical single output TinySwitch-5 design.

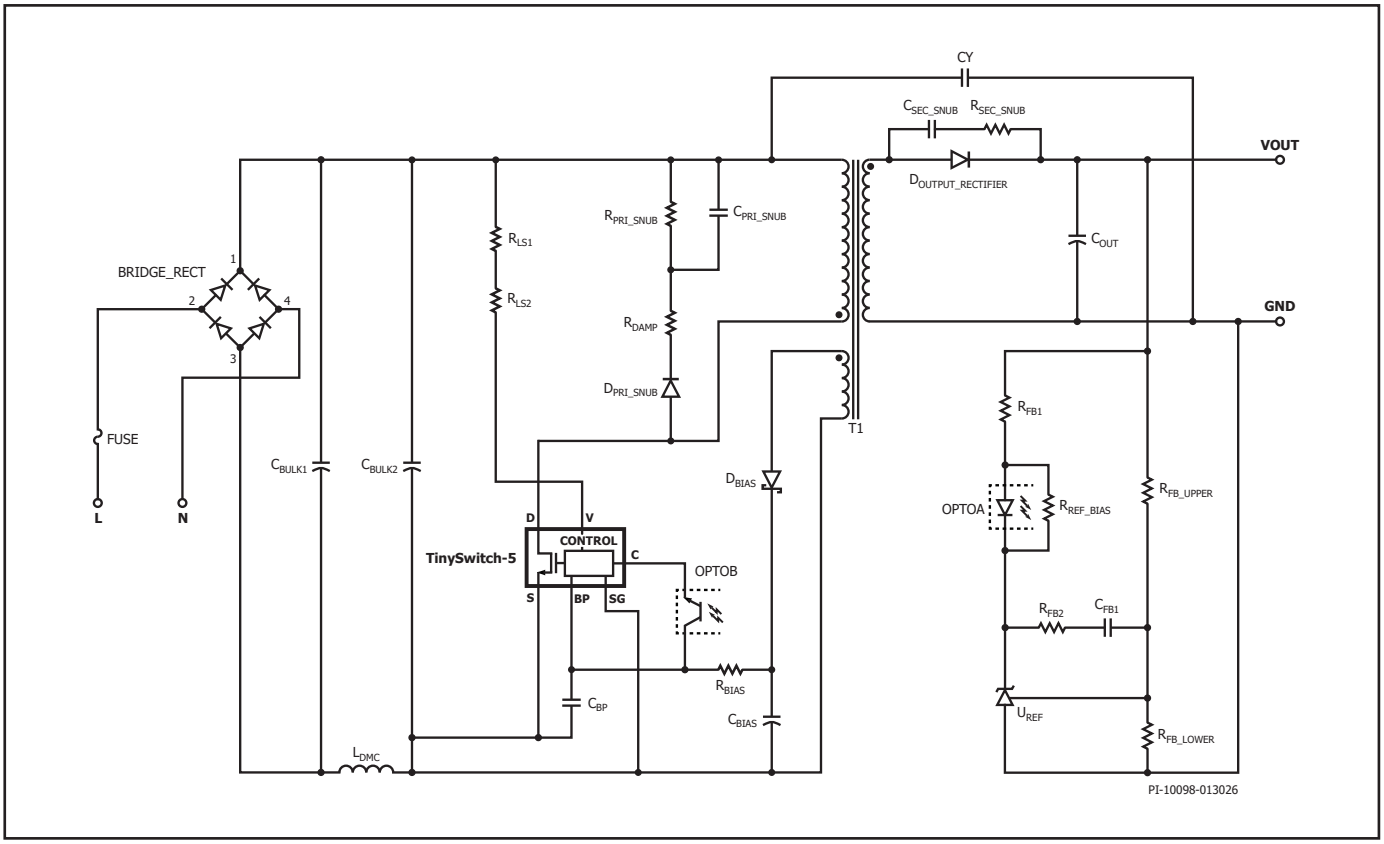



Figure 7. Typical TinySwitch-5 Flyback Power Supply Single-output design.

### BYPASS Pin Capacitor ($C_{BP}$)

A capacitor connected from the BYPASS pin (BP) of the TinySwitch-5 IC to SGND provides decoupling for the primary controller. A 0.47 µF capacitor may be used. While electrolytic capacitors are an option, surface mount multi-layer ceramic capacitors are often preferred for double-sided boards as they can be placed close to the IC. Their small size also makes them ideal for compact power supplies. At least 10 V, 0805 or larger size X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met. Note that ceramic capacitor type designations, such as X7R and X5R, can vary in voltage coefficients across different manufacturers or product families. It is advisable to review capacitor data sheets to ensure the selected capacitor does not experience more than a 20% drop in capacitance at 5 V. Avoid using Y5U or Z5U / 0603 rated MLCCs, as they have poor voltage and temperature coefficient characteristics.

### V Pin Line Sense Resistors ($R_{LS1}$ and $R_{LS2}$)

Resistors connected from the V pin to the DC bus enable input voltage sensing for line undervoltage and overvoltage protection. For a typical universal input application, a total resistor value of 8 MΩ is recommended. For high line input, it is advisable to use two 0.25 W SMD 1206 resistors or leaded resistors in series, each with a value of 4 MΩ.

Connecting the V pin to SOURCE disables the line sensing function. It is not recommended to leave the V pin floating.

### Primary Clamp ($D_{PRI\_SNUB}$, $R_{DAMP}$, $R_{PRI\_SNUB}$, $C_{PRI\_SNUB}$)

Refer to Figure 7. An RRCD clamp is a commonly used clamp in low-power power supplies. For higher power designs, a Zener clamp or RRCD + Zener clamp can be used to increase efficiency. It is advisable to limit the peak drain voltage to 90% of the device absolute DRAIN voltage rating under worst-case conditions (maximum input voltage, maximum overload power or output short-circuit).

The clamp diode ($D_{PRI\_SNUB}$) must be a standard recovery glass-passivated type or a fast recovery diode with a reverse recovery time of less than 500 ns. Using standard recovery glass passivated diodes allows recovery of some of the clamped energy in each switching cycle, improving light-load and average efficiency. The diode conducts momentarily each time the MOSFET inside TinySwitch-5 turns off, transferring the stored energy from the leakage reactance and the clamp capacitor $C_{PRI\_SNUB}$ to the output

Resistor $R_{DAMP}$, in the series path, provides damping preventing excessive ringing due to resonance between the leakage inductance and the MOSFET switch output capacitance $C_{OSS}$. Resistor $R_{PRI\_SNUB}$ bleeds-off energy stored in the capacitor $C_{PRI\_SNUB}$. Power supplies using different TinySwitch-5 devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor $C_{PRI\_SNUB}$ and resistor $R_{PRI\_SNUB}$ and $R_{DAMP}$ must therefore be optimized for each design.

As a general rule it is advisable to minimize the value of capacitor $C_{PRI\_SNUB}$ and maximize the value for $R_{PRI\_SNUB}$ and $R_{DAMP}$, while ensuring the MOSFET DRAIN voltage remains below 90% of its absolute maximum limit at the highest input voltage and maximum load. The value of $R_{DAMP}$ should be large enough to damp the ringing within the required time. However, as the value of $R_{DAMP}$ increases the DRAIN peak voltage and its power dissipation also increase. Therefore, care must be taken to keep the DRAIN voltage below 90% of its maximum absolute limit. The recommended range for $R_{DAMP}$ is 47 Ω to 100 Ω. While the recommended range for $R_{PRI\_SNUB}$ is 100 kΩ to 470 kΩ.

Using a disc ceramic capacitor with dielectric such as Z5U in the clamp circuit for $C_{PRI\_SNUB}$ may generate audible noise, therefore a polyester film type or a ceramic capacitor with X7R as a dielectric, 1 kV rating, 1206 size is commonly used. The recommended range for $C_{PRI\_SNUB}$ is 470 pF to 1 nF.

### Bias Winding and External Bias Supply Circuit ($D_{BIAS}$, $C_{BIAS}$, $R_{BIAS}$)

The internal primary bypass regulator connected from the DRAIN pin to the BYPASS pin of the TinySwitch-5 IC charges the capacitor $C_{BP}$ connected to the BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can supply at least 1.5 mA of current to the BYPASS pin and C pin.

A bias voltage of 12 V is recommended at full load. Higher voltage will increase no-load input power. To reduce no-load consumption and improve standby input efficiency, ultrafast or Schottky diodes are recommended for the bias winding rectifier. The turns ratio for the bias winding should be selected such that 10 V is developed across the bias winding at the lowest rated output voltage of the power supply under the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to slightly higher than $I_{S1}$ of 258 μA to achieve the lowest no-load power consumption when operating the power supply at 230 VAC input. This can be achieved by fine tuning the value of $R_{BIAS}$ resistor. A glass-passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes, which can lead to higher radiated EMI.

An aluminum low ESR electrolytic capacitor of at least 47 μF and 25 V rating is recommended for the bias filter capacitor $C_{BIAS}$. A 47 μF low ESR electrolytic capacitor will help to improve the no-load input power and standby input power efficiency. The use of ceramic surface mount capacitors is not recommended, as they can cause audible noise due to the piezoelectric effect in their mechanical structure.

To achieve minimum no-load input power and high full load efficiency, the resistor $R_{BIAS}$ should be selected such that the current through this resistor is higher than the required BYPASS pin current.

### Secondary Output Rectifier Diode ($D_{OUTPUT\_RECTIFIER}$)

The output diode is selected based on peak inverse voltage, output current, and thermal conditions in the application, including heatsinking and air circulation. The higher $DC_{MAX}$ of the TinySwitch-5 IC, combined with an appropriate transformer turns ratio, allows the use of an 80 V Schottky diode for higher efficiency at output voltages up to 15 V.

Considerations for selecting an output rectifier diode:

- Ensure the reverse voltage rating ($V_R$) is at least 1.25 times the peak inverse voltage (PIV).
- Select a diode with a current rating ($I_D$) that is at least twice the output current ($I_{OUT}$).

### Output Filter Capacitance ($C_{OUT}$)

A low ESR electrolytic capacitors is one of the key requirements in smoothing output ripple voltage. Other parameters to be considered are the RMS ripple current rating, DC working voltage and ESR. The actual capacitance value is of less importance.

Considerations for Selection of Output Capacitor:

- Ensure the capacitor ripple is specified @ 105 ºC, 100 kHz must be larger than the expected ripple current ($IS_{RIPPLE}$).
- Use a low ESR (Equivalent Series Resistance) electrolytic capacitor to minimize output switching ripple voltage, which is calculated using $V_{RIPPLE} = IS_{RIPPLE}$ x ESR.
- Select a capacitor with a voltage rating such that the rated voltage is at least 1.25 times the output voltage ($V_{OUT}$).

### Output Post Filter Components ($L_{PF}$ and $C_{PF}$):

A post filter ($L_{PF}$ and $C_{PF}$) can be added to reduce high frequency switching noise and ripple.

Considerations for Adding a Post Filter:

- The inductor ($L_{PF}$) should have an inductance value in the range of 1 μH to 3.3 μH and a current rating that exceeds the peak output current.
- The capacitor ($C_{PF}$) should have a capacitance value in the range of 100 μF to 330 μF and a voltage rating that is at least 1.25 times the output voltage ($V_{OUT}$).
- If a post filter is used, ensure that the output voltage sense resistor and optocoupler are connected before the post filter inductor. See Figure 9.

## Recommendations for Circuit Board Layout

For this section refer to Figures 8 to 12

**Single-Point Grounding**
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. The $C_{BIAS}$ ground should have a dedicated trace that is star-connected to the input filter capacitor ground pin.

**Bypass Capacitors**
The BYPASS pin decoupling capacitor ($C_{BP}$) must be located directly adjacent to the BYPASS and SOURCE pins. Ensure the connections should be routed via short traces.

**Critical Loop Area**
Circuits with high dv/dt or di/dt should be kept as small as possible. Minimize the area of the primary loop that connects the input filter capacitor, transformer primary, and IC. Similarly, reduce the area of the loop connecting the secondary winding, output rectifier diode, and output filter capacitor.

Ensure that no loop area is placed inside another loop to minimize crosstalk between circuits.

**Drain Node**
The drain switching node is the dominant noise generator. Therefore, components connected to the drain node should be placed close to the IC and away from sensitive primary control circuits. The clamp circuit components should be physically located away from the BYPASS pin, and the trace width and length in this circuit should be minimized.

**Power Trace Routing**
Current will flow through the path of least resistance. Even if the trace is connected to the capacitors, there is a possibility that the current may bypass them, rendering the capacitors ineffective. For effective filtering and noise immunity, it is recommended that power signal traces be star-connected to the capacitor's pads.

**Primary Clamp Circuit**
A clamp is used to limit the peak voltage on the DRAIN pin during turn-off. This can be achieved by using an R2CD or R2CDZ clamp across the primary winding. To reduce EMI, minimize the loop area between the clamp components, the transformer, and the IC.

**Y Capacitor**
The Y capacitor should be placed directly from the positive terminal of the primary input filter capacitor to the output positive or return terminal of the transformer secondary. This placement will route high-magnitude common mode surge currents away from the IC.

If an input pi EMI filter ($C_{BULK1}$, $L_{DMC}$, $C_{BULK2}$) is used, the inductor should be placed between the negative terminals of the input filter capacitors.

**ESD Immunity**
Sufficient clearance should be maintained between the primary-side and secondary-side circuits to ensure compliance with ESD and hi-pot isolation requirements. The spark gap should be placed between the output return and/or positive terminals and one of the AC inputs (after the fuse). In this configuration, a 6.4 mm spark gap (5.5 mm is acceptable, depending on customer requirements) is sufficient to meet the creepage and clearance requirements of most safety standards for a universal input power supply. For effective ESD immunity, the spark gap spacing should be the closest distance between the primary and secondary sections.

A spark gap across the common-mode choke or inductor provides a low impedance path for high-energy discharges due to ESD or common-mode surges.

**Secondary Rectifier Diode**
For optimal performance, the loop area connecting the secondary winding, secondary rectifier diode, and output filter capacitor should be minimized. When using SMD diodes, ensure sufficient copper area at the terminals of the secondary rectifier diode for heat dissipation. A heatsink may be required for the secondary diode.

**Thermal Considerations**
The SOURCE pin is internally connected to the IC lead frame and serves as the main path for heat removal in V and K packages. Therefore, the SOURCE pin should be connected to a copper area underneath the IC, functioning as both a single-point ground and a heatsink. Since this area is connected to the quiet source node, it can be maximized for effective heat dissipation without causing EMI issues. K packages feature an exposed pad at the bottom of the IC, which should be soldered to the SOURCE copper heatsink to further reduce the IC temperature.

For E packages, the exposed pad at the back of the IC is used to attach a heatsink. A heatsink is necessary to ensure the IC operates safely below the absolute maximum junction temperature limit.

Sufficient copper area or a heatsink should be provided on the board to maintain the IC temperature safely below absolute maximum limits. It is recommended that the copper area or heatsink keeps the IC temperature below 110°C when operating the power supply at full rated load, the lowest rated input AC supply voltage, and system's maximum operating ambient temperature. Further de-rating can be applied as needed.

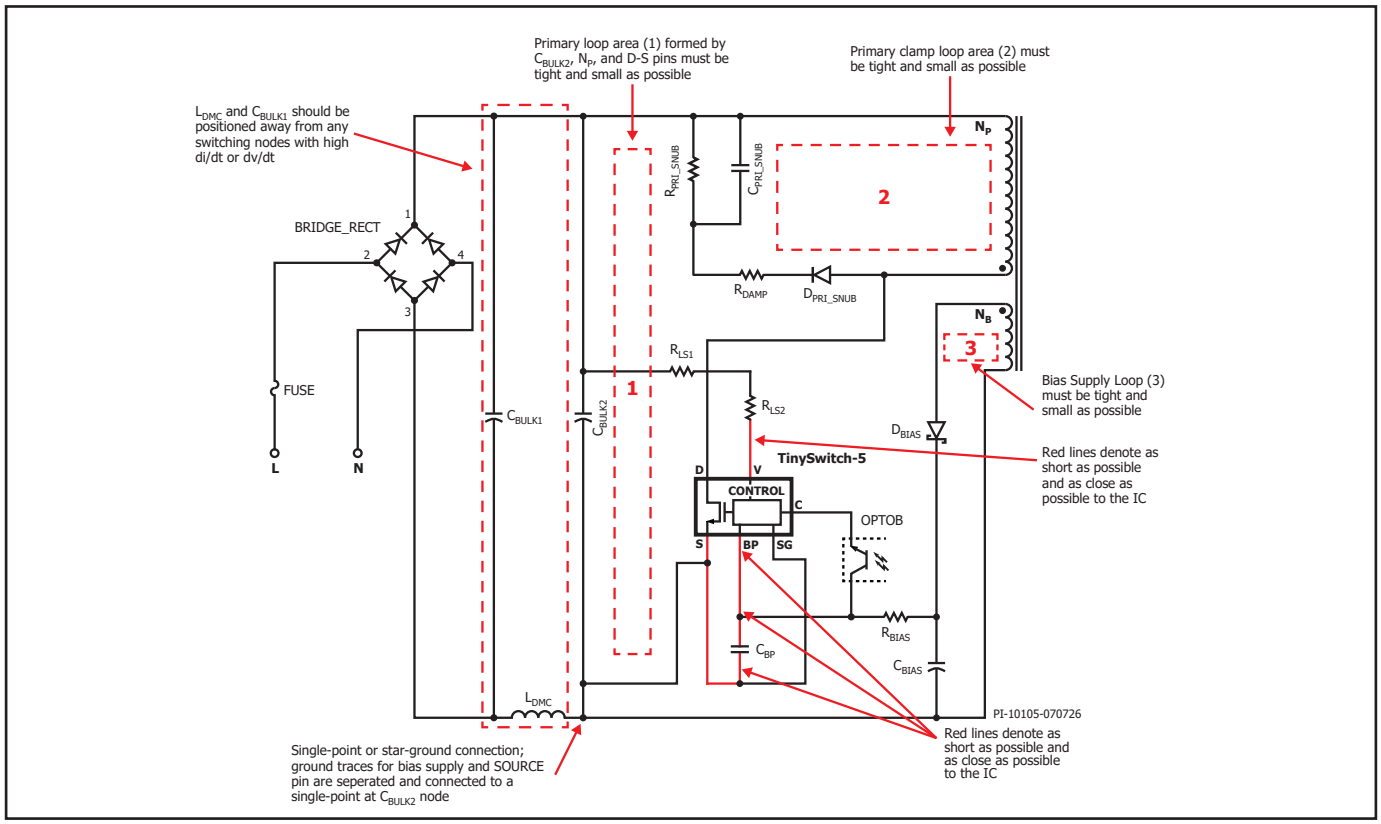



Figure 8. Typical Schematic of TinySwitch-5 Primary-Side Showing Critical Loops Areas, Critical Component Traces, and Single-Point or Star Grounding.

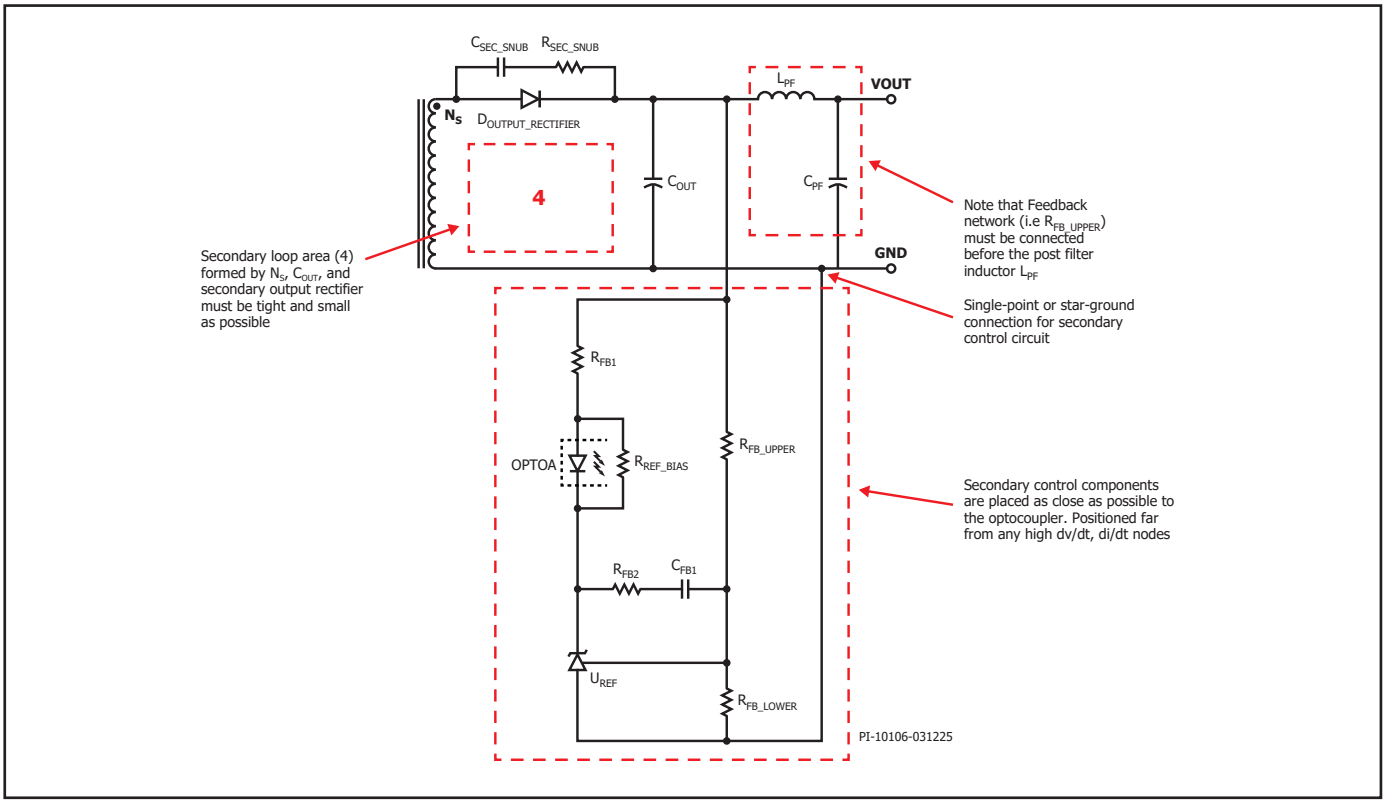



Figure 9. Typical Schematic of TinySwitch-5 Secondary-Side Showing Critical Loops Areas, Critical Component Traces and Single-Point or Star Grounding. Optional Post Filter LC included.

## Layout Example

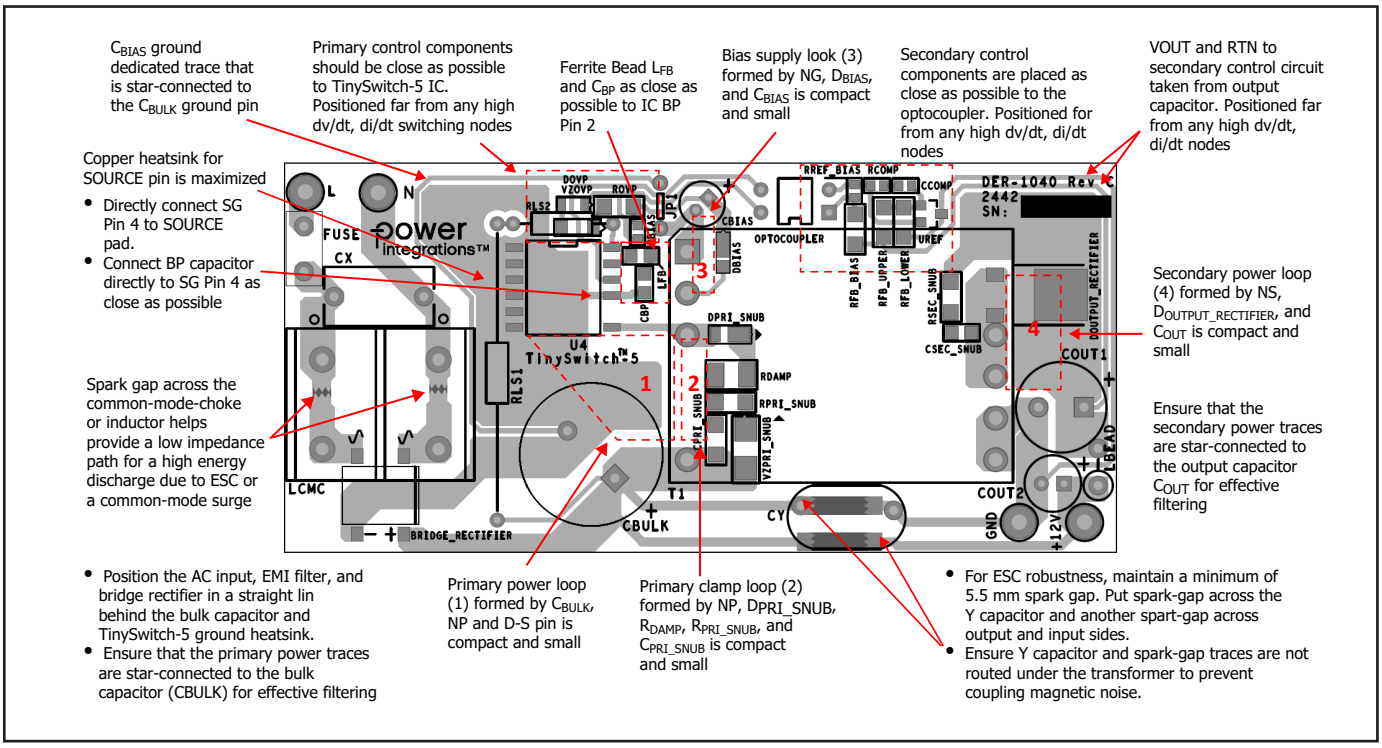



Figure 10. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 K-package.

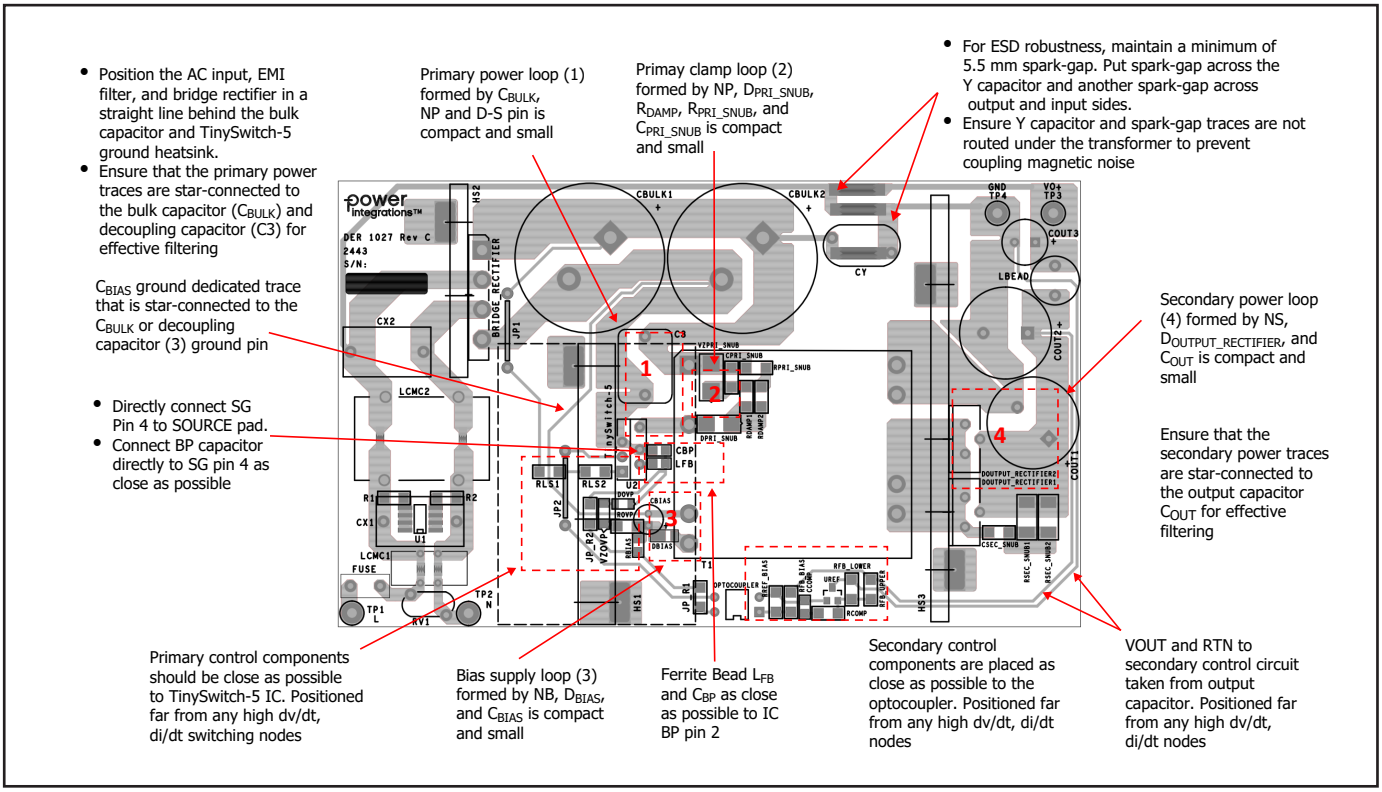



Figure 11. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 E-package.

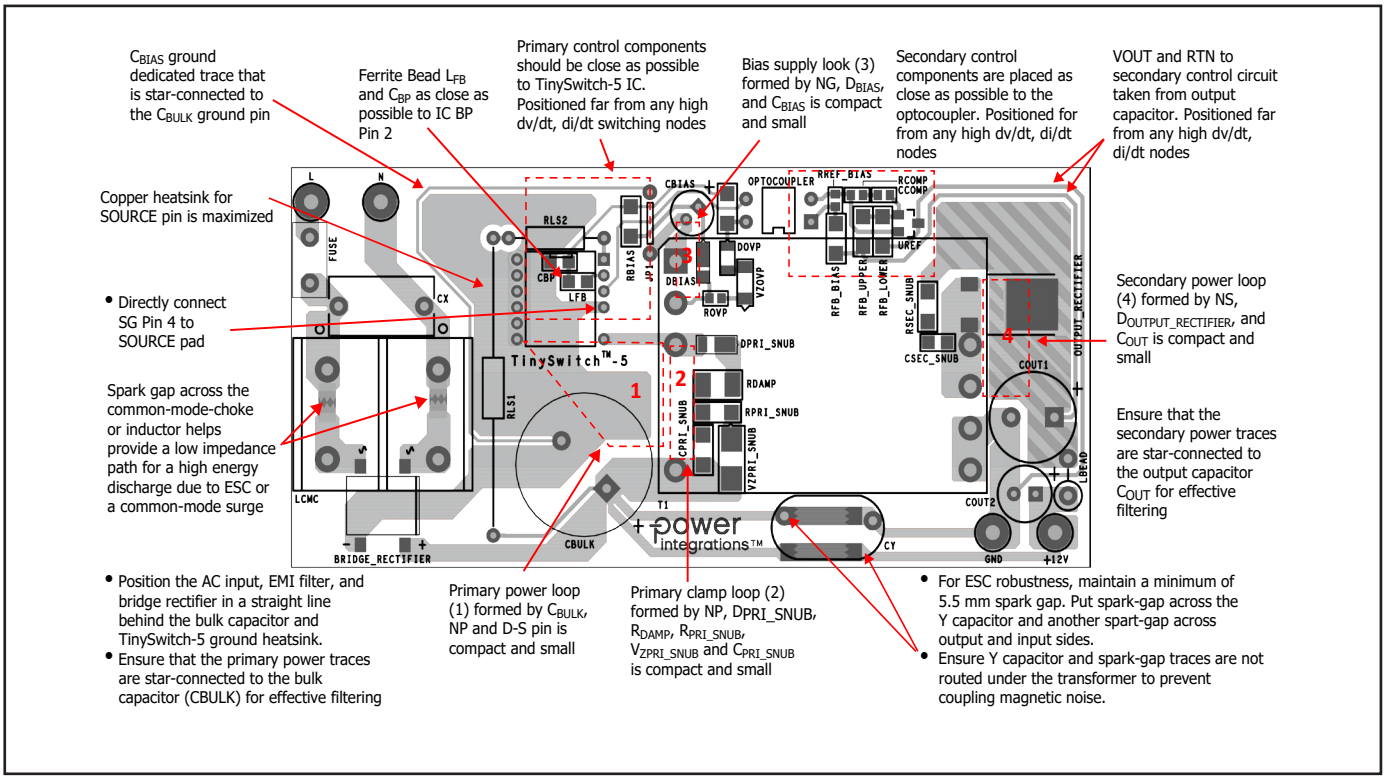



Figure 12. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt or di/dt, Component Placement and Spark-Gap Location for TinySwitch-5 V-Package.

**Special Notes on PCB Layout**

- Ensure all loops are separated, with no loop inside another loop, to avoid ground impedance noise coupling.
- Minimize the surface area and length of high dv/dt nodes, such as the Drain, to reduce RFI (Radio Frequency Interference) generation.
- Avoid routing quiet signal traces, such as those for Y capacitors and feedback returns, near or across noisy nodes (high dv/dt or di/dt), such as the Drain, underneath the transformer belly, the switching side of any winding, or the output rectifier diode. This helps prevent capacitive or magnetic noise coupling.

## Recommendation for EMI Reduction

1. Ensure appropriate component placement and minimize loop areas of the primary and secondary power circuits to reduce radiated and conducted EMI. Aim for a compact loop area.
2. Adding a small capacitor in parallel with the clamp diode on the primary side can help reduce radiated EMI.
3. A resistor in series with the bias winding can help reduce radiated EMI.
4. Common mode chokes (CMC) are often required at the power supply input to attenuate common mode noise. Alternatively, shield windings on the transformer can achieve similar performance. Shield windings can also be used with common mode filter inductors at the input to improve conducted and radiated EMI margins.
5. Adjusting the RC snubber component values of the secondary rectifier diode can help reduce high frequency radiated and conducted EMI.
6. Use a pi-filter comprising differential inductors and capacitors in the input rectifier circuit to reduce low-frequency differential EMI.
7. Connecting a 1 µF ceramic capacitor at the power supply output helps reduce radiated EMI.

## Recommendation for Transformer Design

The transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the bulk capacitor used. It is recommended to use at least 2 µF/W to maintain the DC bus voltage above 90 V, though 3 µF/W provides the typical margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

**Reflected Output Voltage, VOR (V)**

This parameter represents the secondary winding voltage during the diode conduction time, reflected to the primary through the transformer's turns ratio. The default value is 130 V, but VOR can be adjusted to achieve a design that adheres to design rules. For design optimization, consider the following factors:

- Higher VOR allows increased power delivery at VMIN, minimizing the value of the input capacitor and maximizing power delivery.
- Higher VOR reduces voltage stress on the output diodes, potentially allowing for a lower voltage rating and higher efficiency.
- Higher VOR increases leakage inductance which reduces power supply efficiency.
- Higher VOR increases peak and RMS current on the secondary side, potentially increasing secondary side copper and diode losses, thereby reducing efficiency.

It should be noted that there are exceptions to this guidance, especially for very high output currents where the VOR should be reduced to achieve the highest efficiency. For higher output voltages (above 15 V), a higher VOR should be employed to maintain an acceptable peak inverse voltage (PIV) across the output diode.

Optimal selection of the VOR value depends on the specific application and involves a compromise between the factors mentioned above.

**Ripple to Peak Current Ratio ($K_P$)**

A $K_P$ below 1 indicates continuous-conduction mode, where $K_P$ is the ratio of ripple current to peak primary current (Figure 13).

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$

A $K_P$ value higher than 1 indicates discontinuous conduction mode. In this case, $K_P$ is the ratio of primary switch off-time to secondary diode conduction time.

$$K_P \equiv K_{DP} = \frac{(1 - D) \times T}{t} = \frac{VOR \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

It is recommended to use a $K_P$ close to 0.9 at the minimum expected DC bus voltage for most TinySwitch-5 designs. A $K_P$ value of less than 1 results in higher transformer efficiency by lowering the primary RMS current but leads to higher switching losses in the primary-side switch, resulting in a higher TinySwitch-5 IC temperature.

The PIXIs spreadsheet can be used to effectively optimize the selection of $K_P$, the inductance of the primary winding, the transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

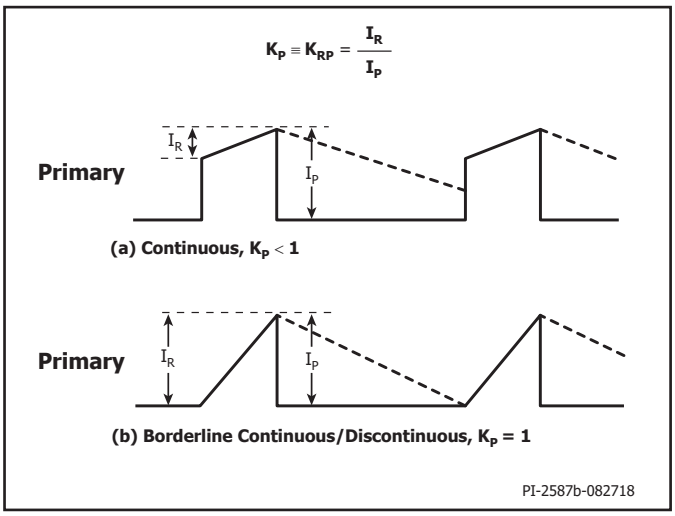



Figure 13. Continuous Conduction Mode Current Waveform, $K_P < 1$.

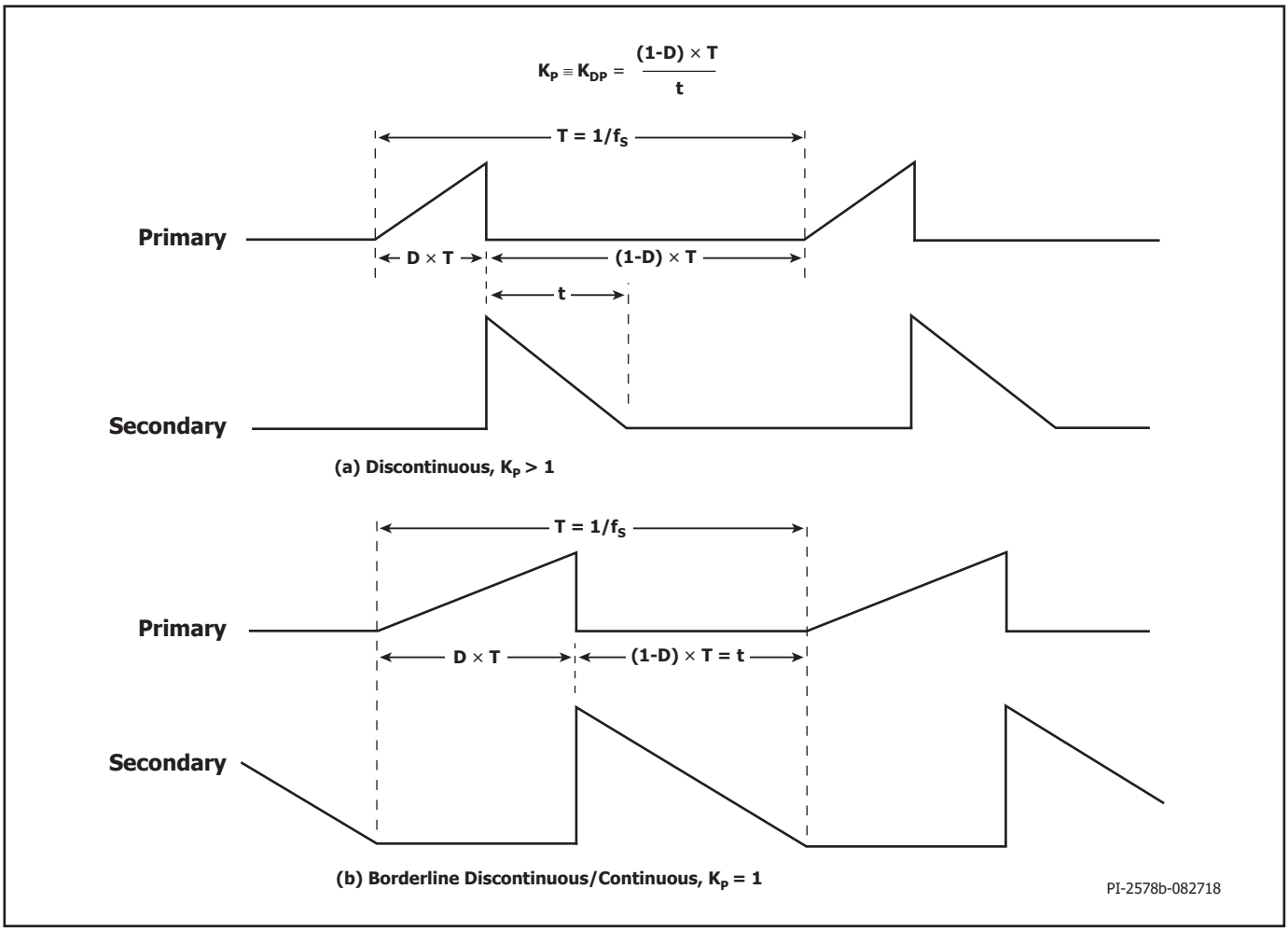



Figure 14. Discontinuous Conduction Mode Current Waveform, $K_P > 1$.

**Maximum Flux Density, $B_M$ (Gauss)**
A maximum value of 3800 gauss at the peak device current limit is recommended to limit the peak flux density during start-up and under output short-circuit conditions. Under these conditions, the output voltage is low, and there is minimal reset of the transformer during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device, combined with the built-in protection features of the TinySwitch-5 IC, provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions

**Transformer Primary Inductance, $L_P$**
Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

**Core Type**
The choice of a suitable core depends on the physical constraints of the power supply enclosure. It is recommended to use only low-loss cores to minimize thermal challenges.

**Safety Margin, MARGIN (mm)**
For designs that require safety isolation between primary and secondary but are not using triple insulated wire the width of the safety margin to be used on each side of the bobbin should be entered here. Typically for universal (85 – 265 VAC) input designs a total margin of 6.2 mm is required, and a value of 3.1 mm should be entered into the spreadsheet. For vertical bobbins, the margin may not be symmetrical; however, if a total margin of 6.2 mm is required then 3.1 mm would still be entered even if the physical margin were only present on one side of the bobbin. For designs using triple insulated wire it may still be necessary to enter a small margin to meet the required safety creepage distances. Typically, several bobbins exist for each core size, and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required.

Margin reduces the available area for the windings, marginated construction may not be suitable for small core sizes. If after entering the margin more than 3 primary layers are required, it is suggested that either a larger core be selected or that the design is switched to a zero-margin approach using triple insulated wire.

**Primary Layers, L**
Primary layers should be in the range of 1 to 3, with the lowest number that meets the primary current density limit (CMA) being preferred. A value of ≥200 Circular-mils/Amp can be used as a starting point for most designs, though higher values may be required due to thermal constraints. Designs with more than three layers are possible, but increased leakage inductance and the physical fit of the windings should be considered.

A split primary construction may be beneficial for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. However, this arrangement can be disadvantageous for low power designs as it typically increases common mode noise and adds cost to the input filtering.

## Quick Design Checklist

As with any power supply, the operation of all TinySwitch-5 designs should be verified on-the-bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

**Maximum Drain Voltage**
Verify that $V_{DS}$ of TinySwitch-5 and reverse voltage of the secondary rectifier diode do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

**Maximum Drain Current**
At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review Drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading-edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB\ (MIN)}$. Under all conditions, the maximum Drain current for the primary MOSFET should be below the specified absolute maximum ratings.

**Thermal Check**
At the specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for the TinySwitch-5 IC, transformer, bridge rectifier, secondary rectifier Diode, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of MOSFET $R_{DS(ON)}$. At low-line, maximum power, a maximum TinySwitch-5 IC temperature of 110 °C is recommended to allow for $R_{DS(ON)}$ variation.

**Design Support**
Up-to-date information on design support can be found at the Power Integrations website: www.power.com

## Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: TNY5071-TNY5077 ..... -0.3 V to 725 V
DRAIN Pin Peak Current: TNY5071 ..... 1.9 A[3]
TNY5072 ..... 3 A[3]
TNY5073 ..... 4.2 A[3]
TNY5074 ..... 6 A[3]
TNY5075 ..... 9 A[3]
TNY5076 ..... 12 A[3]
TNY5077 ..... 14 A[3]
BP Pin Voltage ..... -0.3 to 6 V
BP Pin Current ..... 100 mA
V Pin Voltage ..... -0.3 V to 6 V
C Pin Voltage ..... -0.3 V to 6 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Maximum Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and secondary GROUND, $T_A$ = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 15 about maximum allowable voltage and current combinations.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for up to 5 seconds.

## Thermal Resistance

Thermal Resistance: E Package
($\theta_{JA}$) ..... 105 °C/W[1]
($\theta_{JC}$) ..... 2 °C/W[2]
V Package
($\theta_{JA}$) ..... 68 °C/W[3], 58 °C/W[4]
($\theta_{JC}$) ..... 2 °C/W[2]
K Package
($\theta_{JA}$) ..... 45 °C/W[3], 38 °C/W[4]
($\theta_{JC}$) ..... 2 °C/W[2]

Notes:
1. Free standing with no heatsink.
2. Measured at the back surface of tab.
3. Soldered (including exposed pad for K package) to typical application PCB with a heatsinking area of 0.36 sq. in. (232 mm$^2$), 2 oz. (610 g/m$^2$) copper clad.
4. Soldered (including exposed pad for K package) to typical application PCB with a heatsinking area of 1 sq. in. (645 mm$^2$), 2 oz. (610 g/m$^2$) copper clad.

| Parameter | Symbol | Conditions<br>SOURCE = 0 V<br>$T_J$ = -40 °C to 125 °C<br>(Unless Otherwise Specified) | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Control Functions** | | | | | | | |
| **Start-Up Off-Time** | $T_{OFF(STARTUP)}$ | $T_J$ = 25 °C | | | 30 | 45 | µs |
| **Maximum Operating Frequency** | $f_{OSC}$ | $T_J$ = 25 °C | | 139 | 150 | | kHz |
| **Jitter Modulation Frequency** | $f_M$ | $T_J$ = 25 °C<br>$f_{SW}$ = 150 kHz | | | 0.22 | | kHz |
| **Maximum Duty Cycle** | $DC_{MAX}$ | $T_J$ = 25 °C | | 59 | 66 | | % |
| **Maximum On-Time Extension** | $T_{ONEXT(MAX)}$ | $T_J$ = 25 °C | | 12.5 | 15 | | µs |
| **Minimum Off-Time** | $T_{OFF(MIN)}$ | $T_J$ = 25 °C | | 1.32 | 2.2 | 2.7 | µs |
| **Soft-Start Time** | $T_{SOFT}$ | $T_J$ = 25 °C | | | 6.26 | | ms |
| **CONTROL Current No Switching** | $I_{C(NOSWITCHING)}$ | $T_J$ = 25 °C | | | 300 | 450 | µA |
| **C Pin Voltage** | $V_C$ | $T_J$ = 25 °C, $I_C$ = 300 µA | | | 2.04 | 2.2 | V |
| **Control Current Auto-Restart and End Soft-Start Threshold** | $I_{C(TH)}$ | $T_J$ = 25 °C | | 5 | 14 | 25 | µA |
| **BP Supply Current** | $I_{S1}$ | $V_{BP}$ = $V_{BP}$ + 0.1 V<br>(Switch not Switching)<br>Exclude $I_{C (NOSWITCHING)}$<br>$T_J$ = 25 °C | | | 258 | 310 | µA |
| | $I_{S2}$ | $V_{BP}$ = $V_{BP}$ + 0.1 V<br>(Switch Switching at 150 kHz)<br>$T_J$ = 25 °C | TNY5071 | | 0.5 | 0.61 | mA |
| | | | TNY5072 | | 0.55 | 0.67 | |
| | | | TNY5073 | | 0.64 | 0.78 | |
| | | | TNY5074 | | 0.73 | 0.88 | |
| | | | TNY5075 | | 0.96 | 1.16 | |
| | | | TNY5076 | | 1.07 | 1.29 | |
| | | | TNY5077 | | 1.37 | 1.65 | |
| **BP Pin Charge Current** | $I_{CH1}$ | $V_{BP}$ = 0 V, $T_J$ = 25 °C | | -1.74 | -1.44 | -1.19 | mA |
| | $I_{CH2}$ | $V_{BP}$ = 4 V, $T_J$ = 25 °C | | -7.3 | -4.60 | -2.27 | |
| **BP Pin Voltage** | $V_{BP}$ | $T_J$ = 25 °C | | 4.75 | 4.95 | 5.15 | V |
| **BP Pin Voltage Hysteresis** | $V_{BP(H)}$ | $T_J$ = 25 °C | | 0.33 | 0.47 | 0.61 | V |
| **BP Shunt Voltage** | $V_{SHUNT}$ | $I_{BP}$ = 2 mA<br>$T_J$ = 25 °C | | 5.15 | 5.40 | 5.65 | V |
| **BP Power-Up Reset Threshold Voltage** | $V_{BP(RESET)}$ | $T_J$ = 25 °C | | 2.8 | 3.30 | 3.8 | V |
| **V Pin Brown-In Threshold** | $I_{UV+}$ | $T_J$ = 25 °C | | 10.9 | 12.2 | 13.3 | µA |

| Parameter | Symbol | Conditions<br>SOURCE = 0 V<br>$T_J$ = -40 °C to 125 °C<br>(Unless Otherwise Specified) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Control Functions (cont.)** | | | | | | |
| **V Pin Brown-Out Threshold** | $I_{UV-}$ | $T_J$ = 25 °C | 9.2 | 10.3 | 11.4 | µA |
| **Brown-Out Delay Time** | $t_{UV-}$ | $T_J$ = 25 °C | | 36 | | ms |
| **V Pin Line Overvoltage Threshold** | $I_{OV+}$ | $T_J$ = 25 °C | 53.2 | 55.8 | 58.6 | µA |
| **V Pin Line Overvoltage Hysteresis** | $I_{OV(H)}$ | $T_J$ = 25 °C | | 3.9 | | µA |
| **V Pin Line Overvoltage Recovery Threshold** | $I_{OV-}$ | $T_J$ = 25 °C | 49 | | | µA |
| **Line Fault Protection** | | | | | | |
| **VOLTAGE Pin Line Overvoltage Deglitch Filter** | $t_{OV+}$ | $T_J$ = 25 °C<br>See Note B | | 3 | | µs |
| **V Pin Voltage** | $V_V$ | $T_J$ = 25 °C<br>$I_V$ = 45 µA | 2.2 | 2.6 | 3.0 | V |

| Parameter | Symbol | Conditions<br>SOURCE = 0 V<br>$T_J$ = -40 °C to 125 °C<br>(Unless Otherwise Specified) | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Circuit Protection** | | | | | | | |
| **Standard Current Limit (BP) Capacitor 0.47 µF See Note C** | $I_{LIMIT}$ (Switch Switching at 150 KHz) | di/dt = 76 mA/µs<br>$T_J$ = 25 °C | TNY5071K | 348 | 375 | 402 | mA |
| | | | TNY5071V | 348 | 375 | 402 | |
| | | di/dt = 120 mA/µs<br>$T_J$ = 25 °C | TNY5072K | 544 | 585 | 626 | |
| | | | TNY5072V | 544 | 585 | 626 | |
| | | di/dt = 176 mA/µs<br>$T_J$ = 25 °C | TNY5073K | 757 | 815 | 873 | |
| | | | TNY5073V | 757 | 815 | 873 | |
| | | di/dt = 205 mA/µs<br>$T_J$ = 25 °C | TNY5074K | 892 | 960 | 1028 | |
| | | | TNY5074V | 892 | 960 | 1028 | |
| | | di/dt = 259 mA/µs<br>$T_J$ = 25 °C | TNY5075K | 1125 | 1210 | 1295 | |
| | | | TNY5075V | 1125 | 1210 | 1295 | |
| | | di/dt = 410 mA/µs<br>$T_J$ = 25 °C | TNY5075E | 1794 | 1930 | 2066 | |
| | | di/dt = 619 mA/µs<br>$T_J$ = 25 °C | TNY5076E | 2323 | 2500 | 2677 | |
| | | di/dt = 690 mA/µs<br>$T_J$ = 25 °C | TNY5077E | 3013 | 3240 | 3467 | |

| Parameter | Symbol | Conditions<br>SOURCE = 0 V<br>$T_J$ = -40 °C to 125 °C<br>(Unless Otherwise Specified) | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Circuit Protection (cont.)** | | | | | | | |
| **BYPASS Pin Fault Shut-Down Threshold Current** | $I_{SD}$ | $T_J$ = 25 °C | | 3.5 | 7 | 11 | mA |
| **Auto-Restart On-Time** | $t_{AR}$ | $T_J$ = 25 °C | | | 63 | | ms |
| **Auto-Restart Off-Time** | $t_{AR(OFF)}$ | $T_J$ = 25 °C | | | 1.2 | | sec |
| **Short Auto-Restart Off-Time** | $t_{AR(OFF)SH}$ | $T_J$ = 25 °C<br>See Note B | | | 0.2 | | sec |
| **Output** | | | | | | | |
| **ON-State Resistance** | $R_{DS(ON)}$ | TNY5071K/V<br>$I_D$ = 225 mA | $T_J$ = 25 °C | | 9.14 | 10.53 | Ω |
| | | | $T_J$ = 100 °C | | 13.75 | 15.84 | |
| | | TNY5072K/V<br>$I_D$ = 351 mA | $T_J$ = 25 °C | | 5.94 | 6.85 | |
| | | | $T_J$ = 100 °C | | 8.75 | 10.10 | |
| | | TNY5073K/V<br>$I_D$ = 489 mA | $T_J$ = 25 °C | | 4.23 | 4.88 | |
| | | | $T_J$ = 100 °C | | 7.12 | 8.21 | |
| | | TNY5074K/V<br>$I_D$ = 576 mA | $T_J$ = 25 °C | | 2.93 | 3.38 | |
| | | | $T_J$ = 100 °C | | 4.35 | 5.02 | |
| | | TNY5075K/V<br>$I_D$ = 726 mA | $T_J$ = 25 °C | | 1.80 | 2.08 | |
| | | | $T_J$ = 100 °C | | 2.60 | 3.01 | |
| | | TNY5075E<br>$I_D$ = 1158 mA | $T_J$ = 25 °C | | 1.91 | 2.21 | |
| | | | $T_J$ = 100 °C | | 2.90 | 3.35 | |
| | | TNY5076E<br>$I_D$ = 1500 mA | $T_J$ = 25 °C | | 1.70 | 1.97 | |
| | | | $T_J$ = 100 °C | | 2.60 | 3.00 | |
| | | TNY5077E<br>$I_D$ = 1944 mA | $T_J$ = 25 °C | | 1.16 | 1.34 | |
| | | | $T_J$ = 100 °C | | 1.75 | 2.02 | |
| **OFF-State Drain Leakage Current** | $I_{DSS1}$ | $V_{BP} = V_{BP} + 0.1$ V<br>$V_{DS}$ = 80% Peak Drain Voltage<br>$T_J$ = 125 °C | | | | 200 | µA |
| | $I_{DSS2}$ | $V_{BP} = V_{BP} + 0.1$ V<br>$V_{DS}$ = 325 V<br>$T_J$ = 25 °C | | | 15 | | µA |
| **Drain Supply Voltage** | | See Note B | | 30 | | | V |
| **Thermal Shutdown** | $T_{SD}$ | See Note A | | 135 | 142 | 150 | ºC |
| **Thermal Shutdown Hysteresis** | $T_{SD(H)}$ | See Note A | | | 70 | | ºC |

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF capacitors are used. In addition, the BP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The operation of the device with the minimum and maximum capacitor values shown are guaranteed by characterization.

| Nominal BP Pin Capacitor Value | BP Capacitor Minimum | Value Tolerance Maximum |
|---|---|---|
| 0.47 µF | -60% | +100% |

Recommended to use at least a 10 V / 0805 / X7R SMD MLCC capacitor.

## Typical Performance Curves

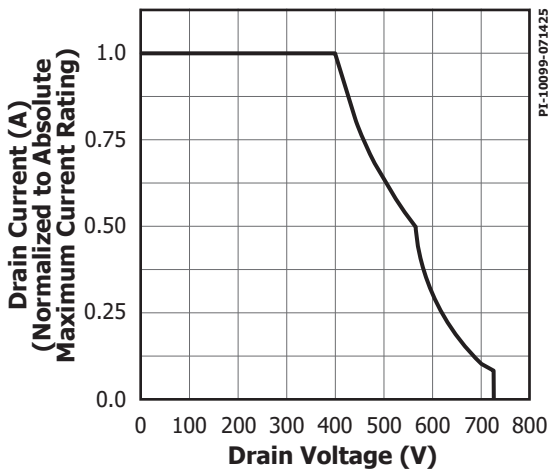



Figure 15. Maximum Allowable Drain Current vs. Drain Voltage.

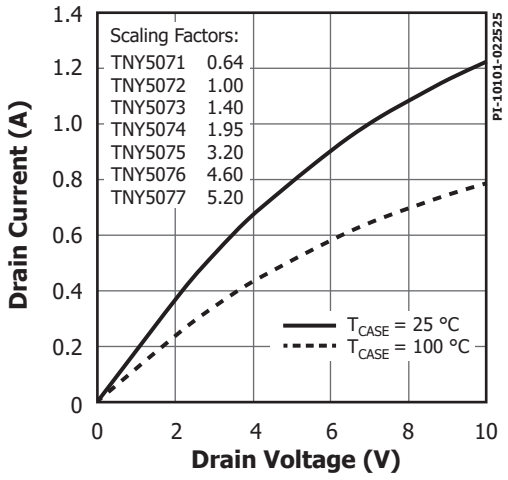



Figure 16. Output Characteristics.

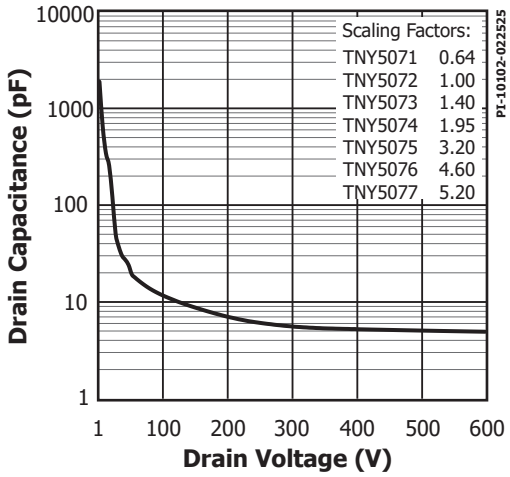



Figure 17. $C_{OSS}$ vs. Drain Voltage.

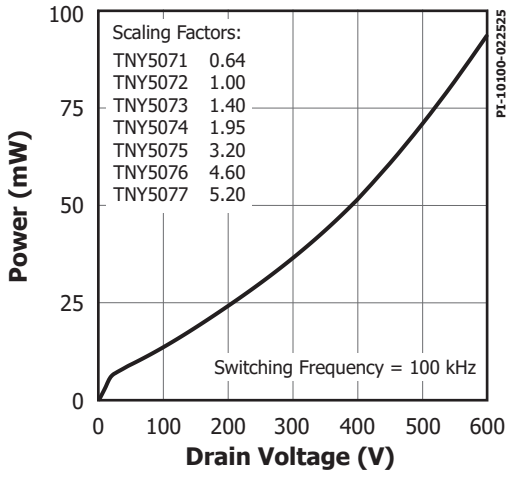
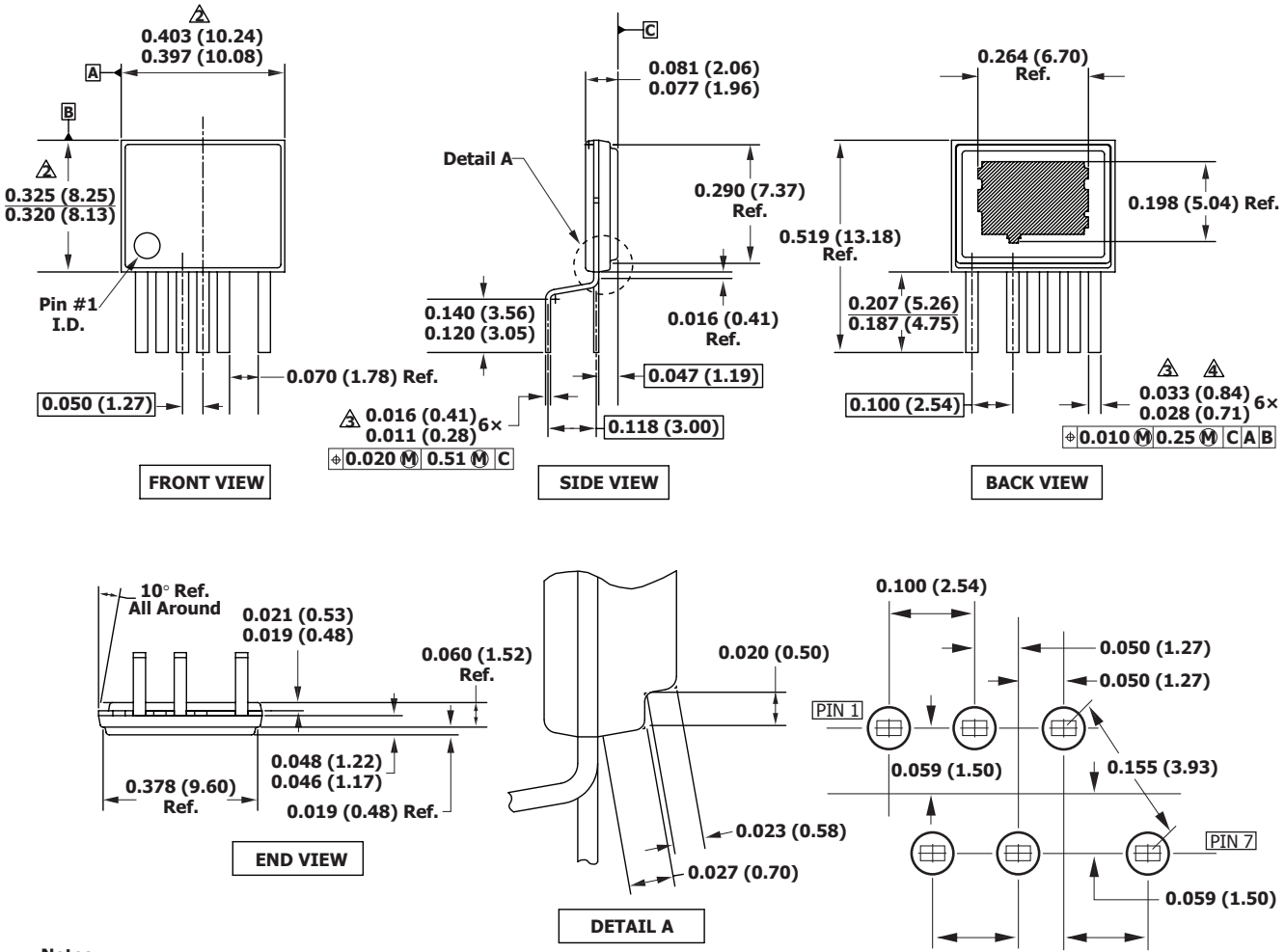



Figure 18. Drain Capacitance Power.

# eSIP-7C (E Package)

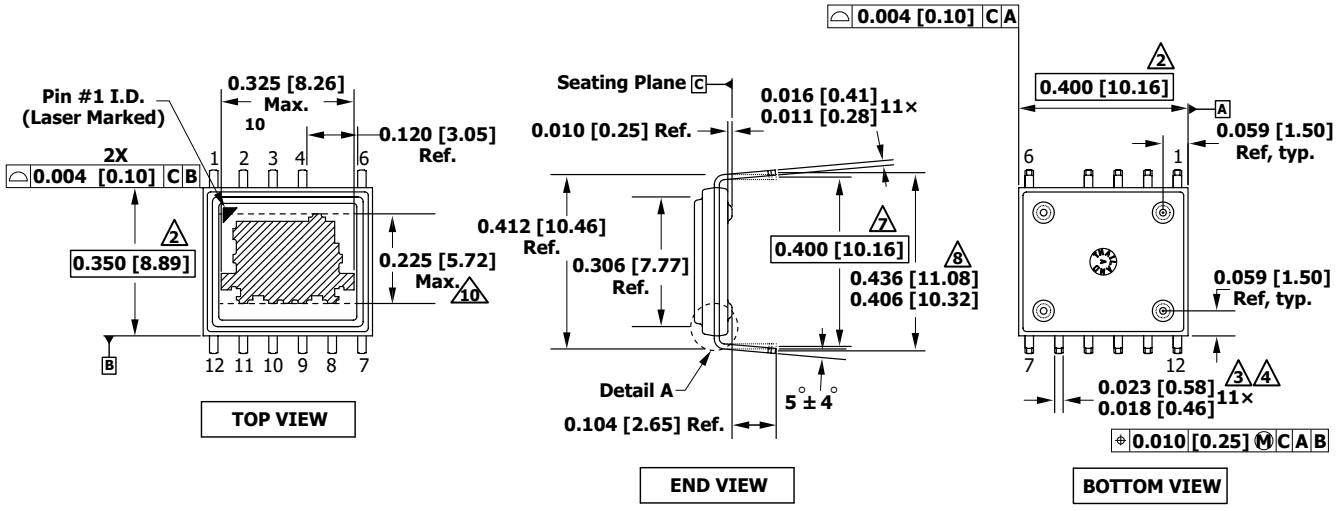


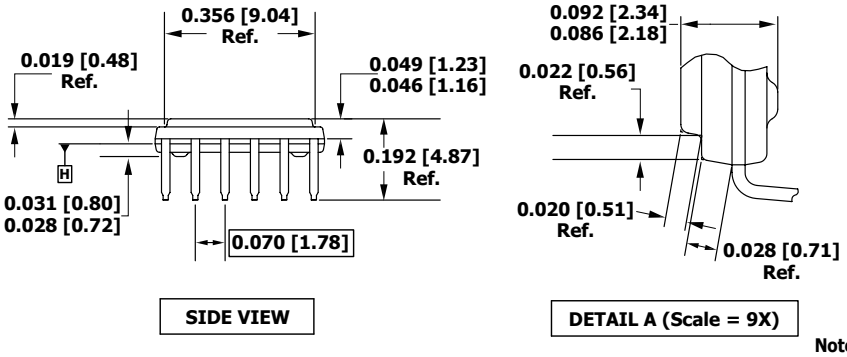

**Notes:**

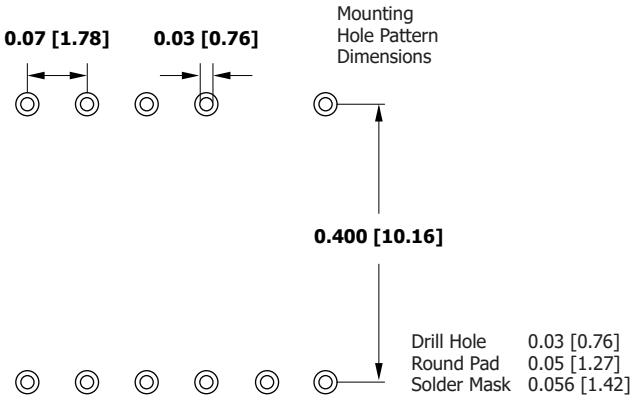
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-020515

# eDIP-12B (V Package)



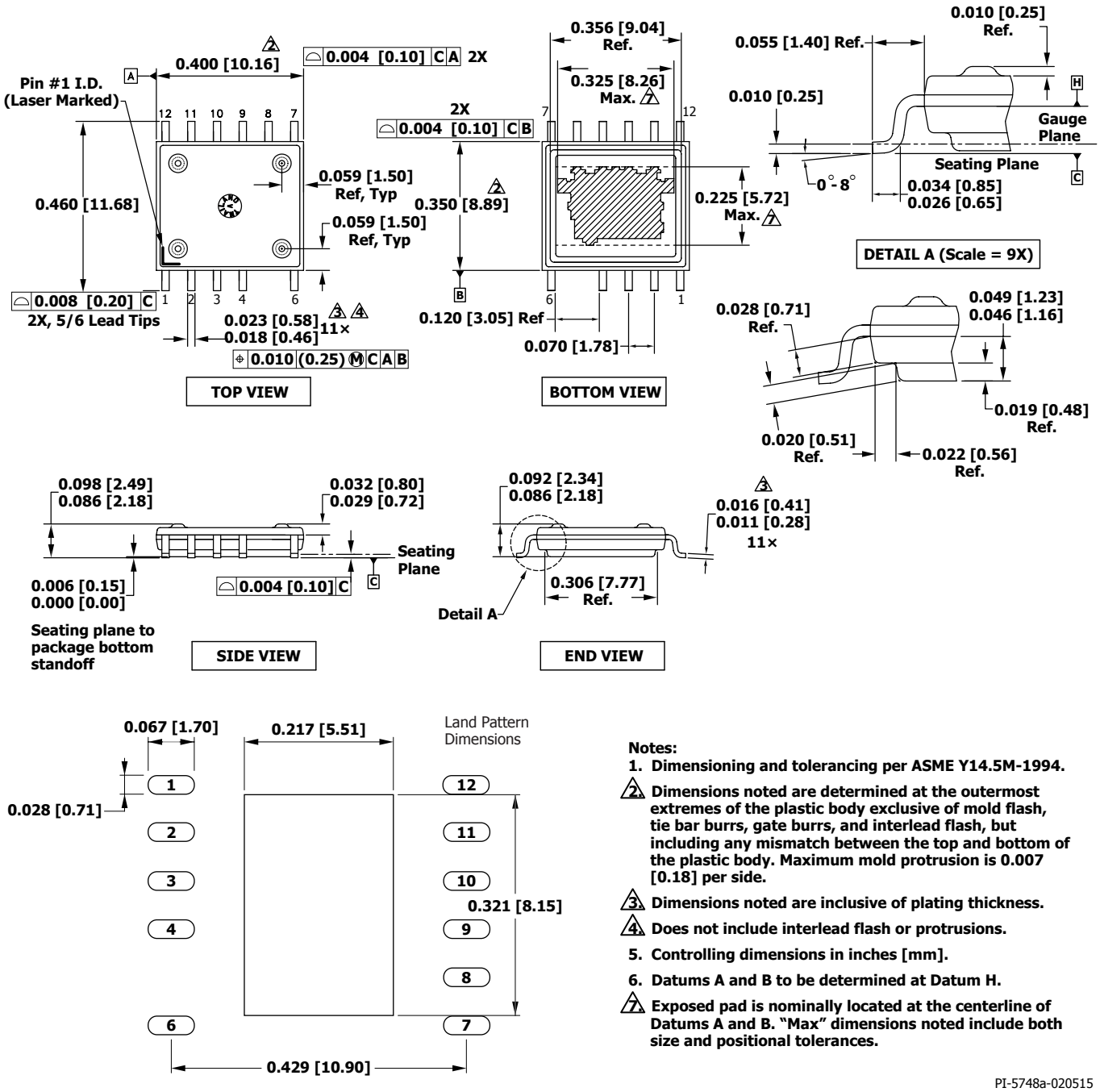




**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outer-most extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Measured with the leads constrained to be perpendicular to Datum C.
8. Measured with the leads unconstrained.
9. Lead numbering per JEDEC SPP-012.
10. Exposed pad is nominally located at the center-line of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5556a-021715

# eSOP-12B (K Package)





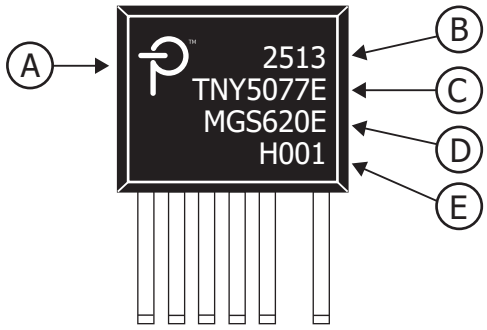


**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5748a-020515

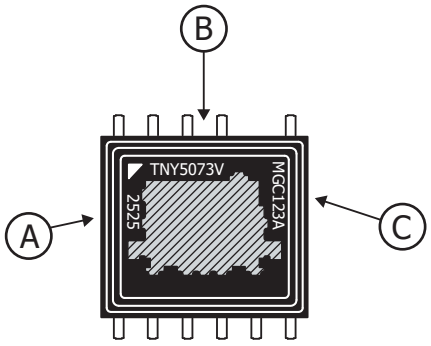
## eSIP-7C PLASTIC PACKAGE MARKING




A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification
D. Lot Identification Code
E. Optional H-Code

PI-10210-071425

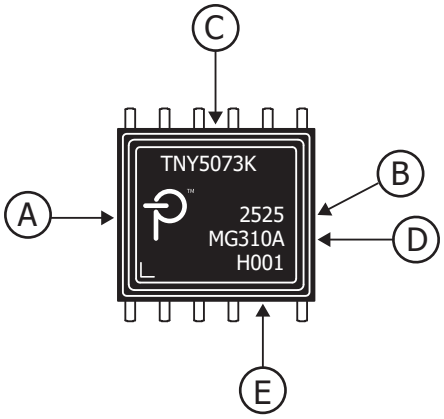
## eDIP-12B (V) PLASTIC PACKAGE MARKING




A. Assembly Date Code (last two digits of year followed by 2-digit work week)
B. Product Identification (Part #/Package Type [V = eDIP-12])
C. Lot Identification Code

PI-10146-071825

## eSOP-12B (K) Plastic Package Marking




A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type [K = eSOP-12])
D. Lot Identification Code
E. Optional H-Code

PI-10144-042925

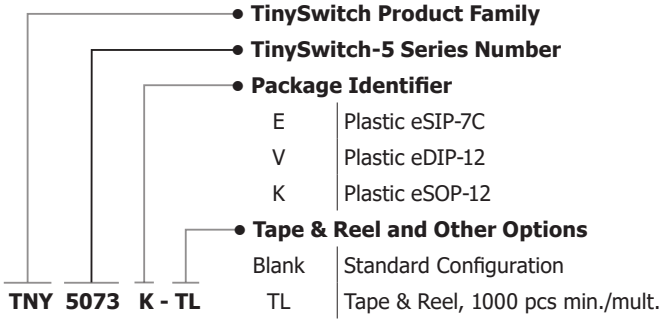
## MSL Table

| Part Number | MSL Rating |
|---|---|
| TNY50XXK | 3 |
| TNY50XXV | N/A |
| TNY50XXE | N/A |

## ESD and Latch-Up Table

| Test | Conditions | Results |
|---|---|---|
| Latch-up at 125 °C | JESD78D | > ±200 mA or > 1.5 × $V_{MAX}$ on all pins |
| Human Body Model ESD | ANSI/ESDA/JEDEC JS-001-2014 | > ±2000 V on all pins |
| Charge Device Model ESD | ANSI/ESDA/JEDEC JS-002-2014 | > ±500 V on all pins |

## Part Ordering Information



| Revision | Notes | Date |
|---|---|---|
| A | Preliminary release. | 12/23 |
| B | Page formatting corrections, text changes on pages 4, 5 and parameter table updates on pages 8 and 10. | 06/24 |
| C | Introduction release. | 12/24 |
| D | Added Applications Example and Typical Performance Curves. | 03/25 |
| E | Define limits on all electrical parameters. | 07/25 |
| F | Removed all ILIM selection as per PCN-25481. | 12/25 |
| G | In electrical table, updated BP Pin Voltage Hysteresis values | 07/26 |

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