Title	**750 W (~1 HP) Three-Phase High Voltage Motor Drive Inverter Using BridgeSwitch™-2 BRD2469WB and LinkSwitch™-TN2 LNK3205D in FOC Operation**
Specification	340 VDC Input, 750 W Continuous Three-Phase Inverter Output Power, 3.0 A_{RMS} Continuous Motor Phase Current
Application	High-Voltage Brushless DC (BLDC) Motor Drive
Author	Applications Engineering Department
Document No.	RDR-975
Date	September 3, 2025
Revision	A

Summary and Features

- BridgeSwitch-2 high-voltage half-bridge motor driver
- Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- No heat sink
- High-side and low-side cycle-by-cycle current limit
- Optional latching low-side current limit
- Configurable latching or hysteretic over-temperature protection
- High-voltage bus monitor for overvoltage protection (OVP)
- Error flagging through the Error Flag (EF) pin or FAULT bus on the MCU interface
- Supports any microcontroller (MCU) for sensorless field-oriented control (FOC) through the signal interface
- Instantaneous phase current output through the IPH pin of each BridgeSwitch-2 device
- +3.3 V supply available through the interface

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Important Note:

During operation, the reference design board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

1 Introduction

This document presents a 750 W, three-phase inverter designed for high-voltage brushless DC (BLDC) motor applications, utilizing three BridgeSwitch™-2 BRD2469WB devices, achieving 97.6% efficiency with a peak of 98.5%. It details both the device and system-level performance, as well as the fault protection capabilities provided by the highly integrated BridgeSwitch-2 half-bridge motor driver IC. A high-voltage buck converter, implemented with minimal component count using the LinkSwitch™-TN2 LNK3205D device, supplies the required external bias for the BRD2469WB components. An optional current sense amplifier is also included to support applications requiring shunt resistor-based current feedback.

This document also provides the inverter specifications, schematic diagram, bill of materials (BOM), printed circuit board (PCB) layout, performance metrics, and an overview of the test setup and procedure. The waveforms and performance data are obtained using a sensorless field-oriented control (FOC) method based on the Space Vector Modulation (SVM) technique, commonly referred to as three-phase modulation. This control is implemented via the MotorXpert™ Suite, using the BRD2469WB's instantaneous phase current (IPH) data for current feedback.

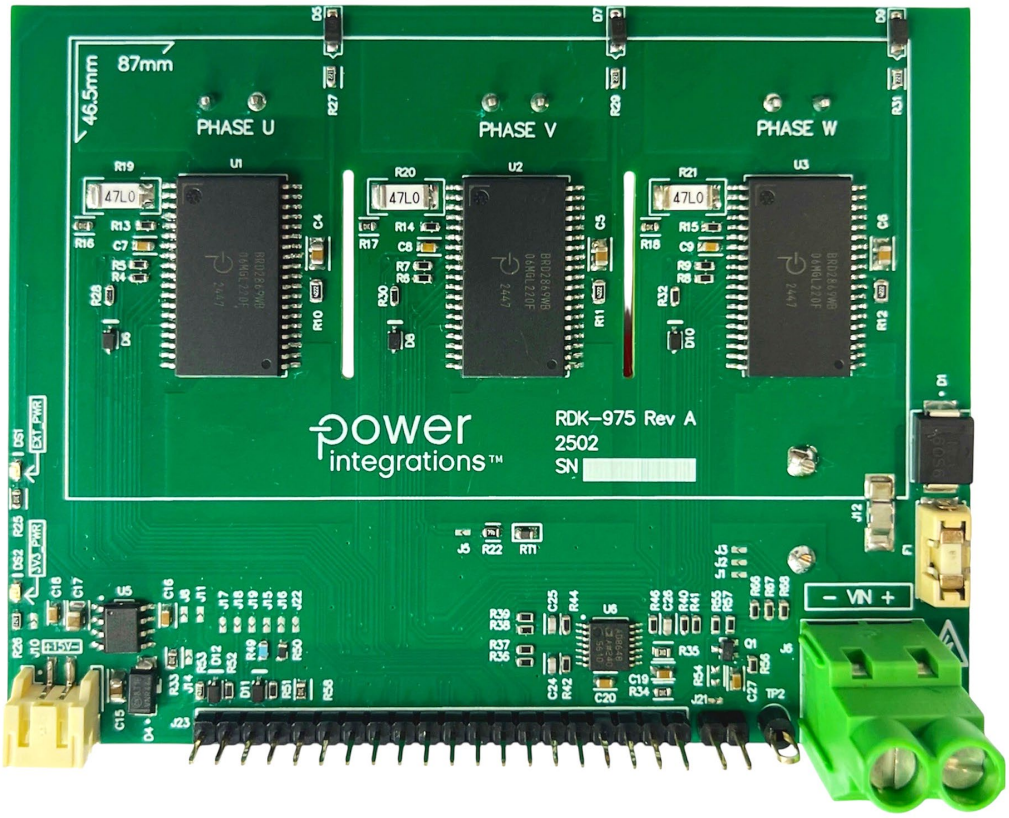

Figure 1 – Populated Circuit Board Top View.

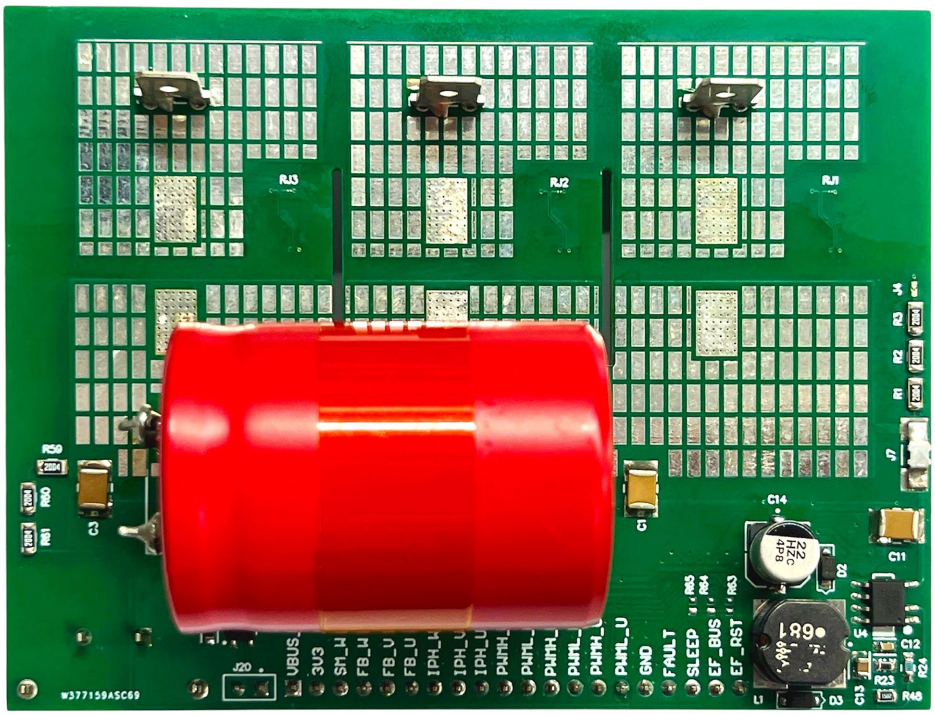

Figure 2 – Populated Circuit Board Bottom View.

2 Inverter Specification

The following table presents the electrical specifications and performance results of the three-phase inverter design.

Description	Symbol	Min	Typ	Max	Unit	Comment
Input						
Input Voltage	V_{IN}	270	340	365	V	Two-wire DC Input
Rated Input Current(1)	$I_{IN, RATED}$		1.74		A	Rated Input DC Current
Max. Input Current(2)	$I_{IN, MAX}$		2.28		A	Max. Input DC Current
Rated Input Power(1)	$P_{IN, RATED}$		591		W	Rated Inverter Input Power
Max. Input Power(2)	$P_{IN, MAX}$		774		W	Max. Inverter Input Power
Output						
Rated Output Power(1)	$P_{OUT, RATED}$		580		W	Rated Inverter Output Power
Max. Output Power(2)	$P_{OUT, MAX}$		756		W	Max. Inverter Output Power
Rated Inverter Efficiency(1)	η_{RATED}		98.2		%	At the rated loading condition
Max. Inverter Efficiency(2)	η_{MAX}		97.6		%	At the maximum loading condition
Rated Inverter Output Current (RMS)(1)	$I_{MOT(RMS), RATED}$		2.26		A	Rated RMS Current Per Phase
Max. Inverter Output Current (RMS)(2)	$I_{MOT(RMS), MAX}$		2.91		A	Max. RMS Current Per Phase
PWM Carrier Frequency(3)	f_{PWM}		10.0		kHz	Three-Phase FOC Modulation
Motor Speed	ω		3000		RPM	
Environmental						
Rated Ambient Temperature(1)	$T_{AMB, RATED}$		23.5		°C	Closed case. No airflow. Free Convection.
Max. Ambient Temperature(2)	$T_{AMB, MAX}$		27.5		°C	
Rated Device Case Temperature(1)	$T_{PACKAGE, RATED}$		89.3		°C	
Max. Device Case Temperature(2)	$T_{PACKAGE, MAX}$		132		°C	
System Level Monitoring						
DC Bus Sensing						Reported through the Error Flag (EF) Pin
OV Threshold	V_{OV}		362		V	
Over Current (OCP) Threshold(4)	I_{OCP}		7.00		A_{PK}	XL/XH = 42.2 kΩ

Notes:
1. At 2.26 A_{RMS} operating at 3000 RPM, resulting in an inverter output power of 580 W.
2. At 2.91 A_{RMS} to achieve the 750 W inverter output power at 3000 RPM.
3. 20 kHz is the maximum recommended PWM frequency.
4. This can be manually configured by adjusting the XL/XH resistor value. For BRD2469WB, the maximum current protection level is 7.00 A using an XL/XH resistance of 42.2 kΩ.

Table 1 – Inverter Specification.

3 Schematic

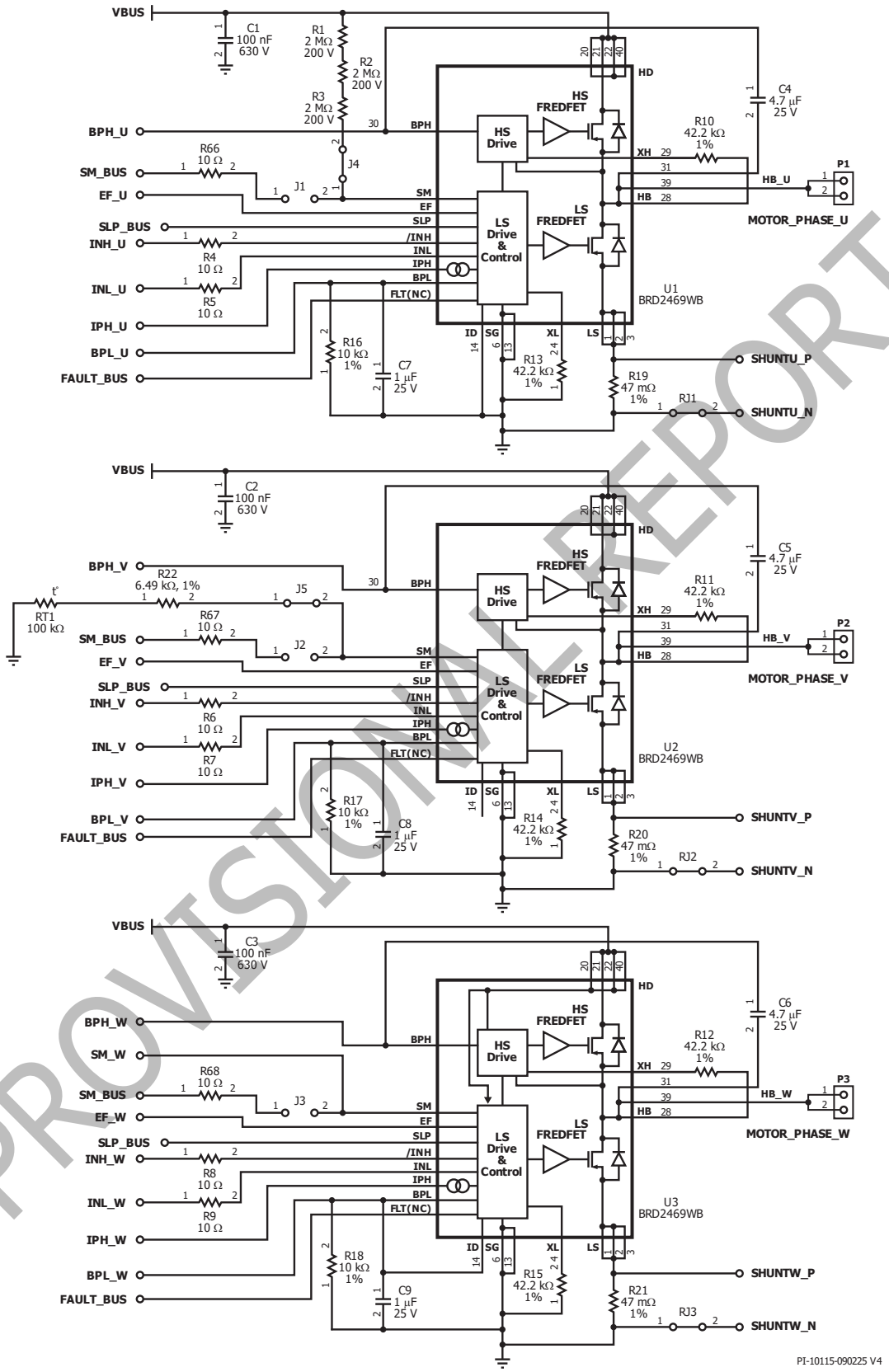

Figure 3 – Inverter Section.

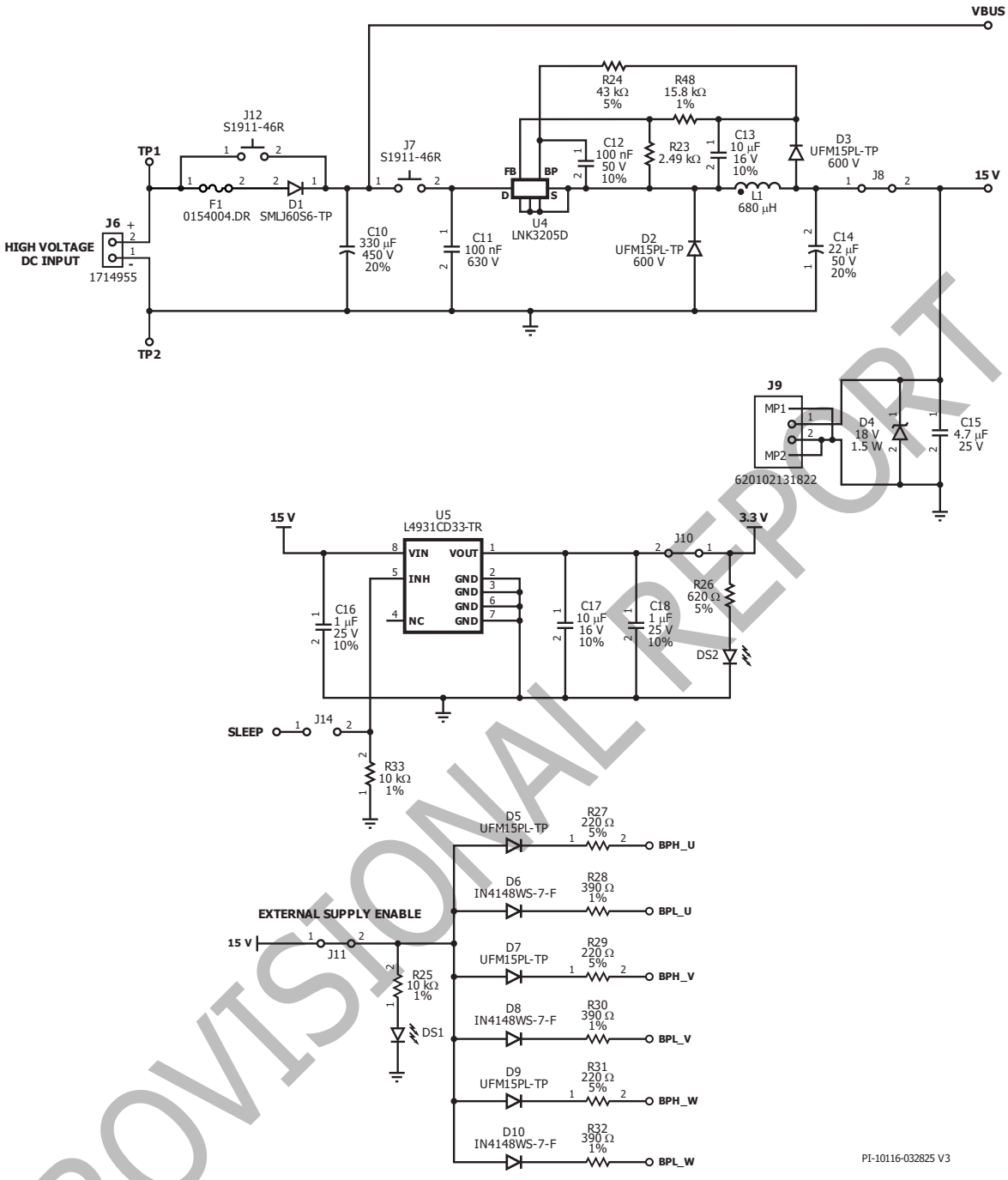

Figure 4 – Auxiliary Supply Section.

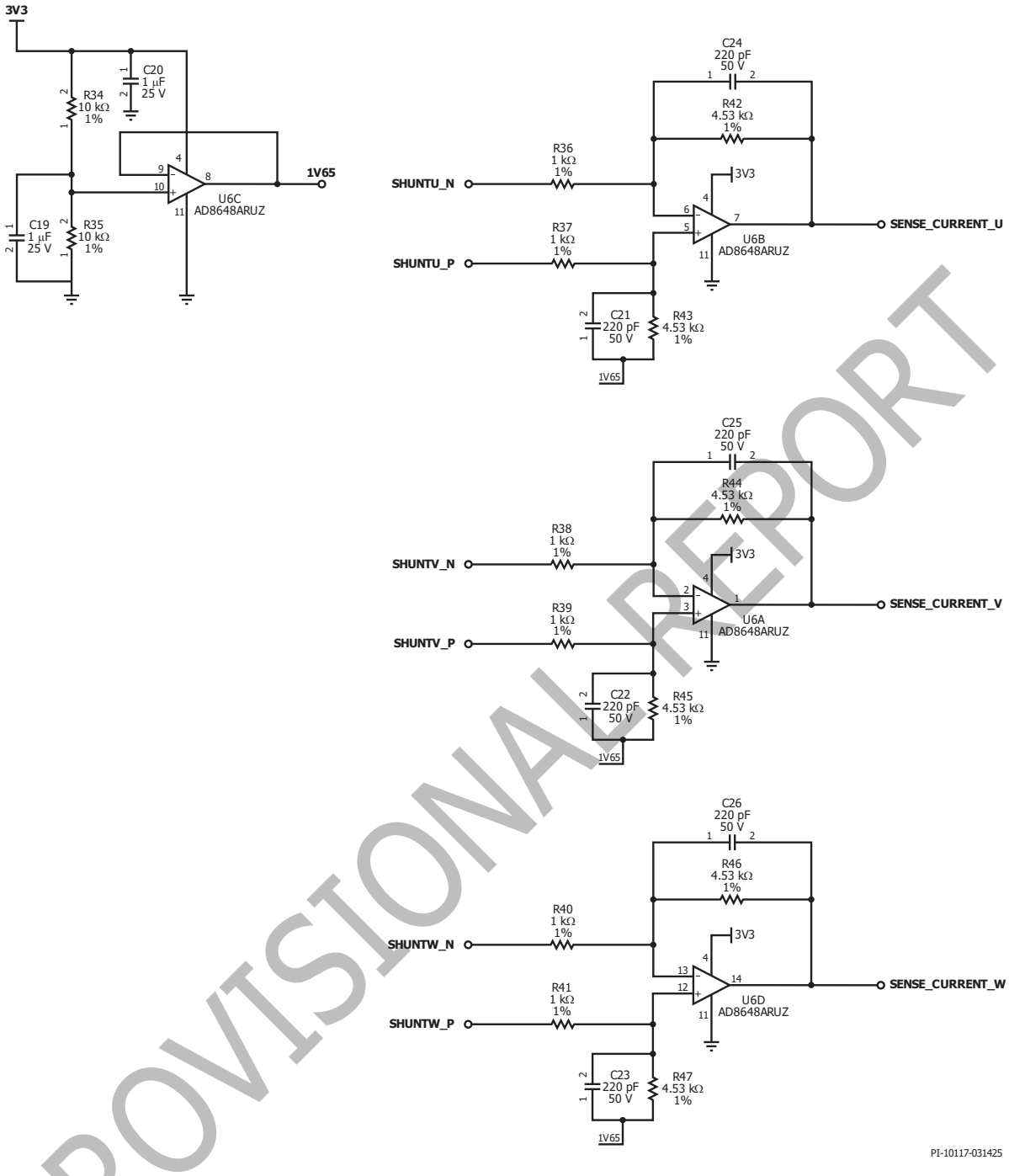

Figure 5 – Current Feedback Section.

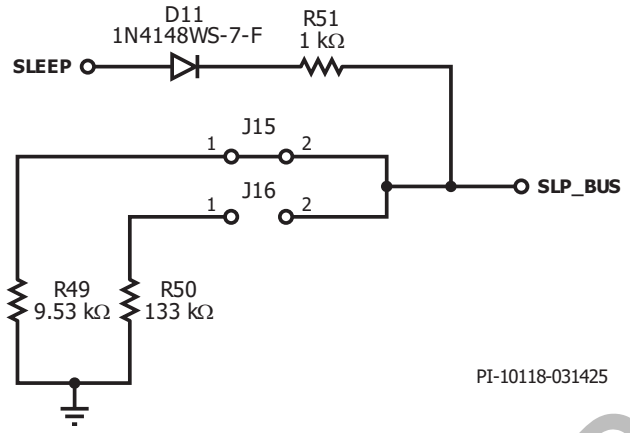

Figure 6 – Sleep Mode and Programming.

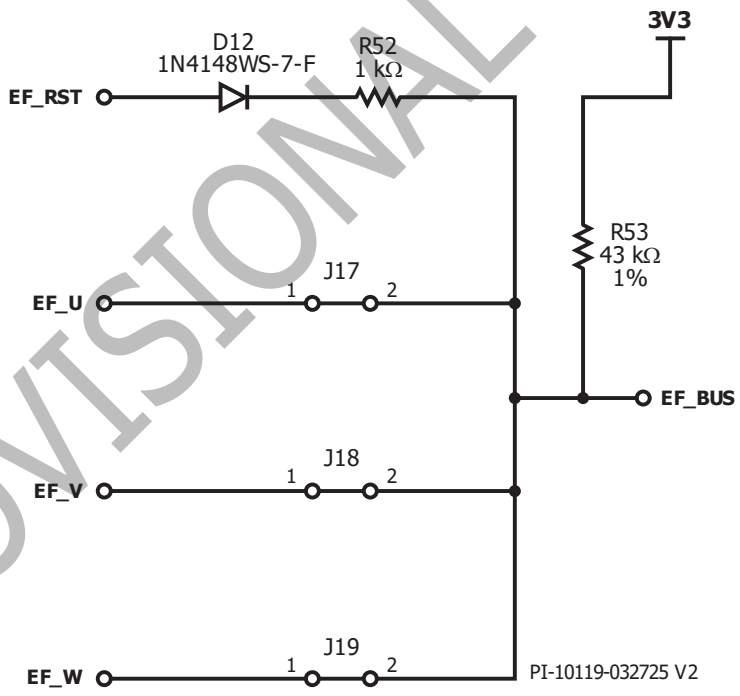

Figure 7 – Error Flag Circuit.

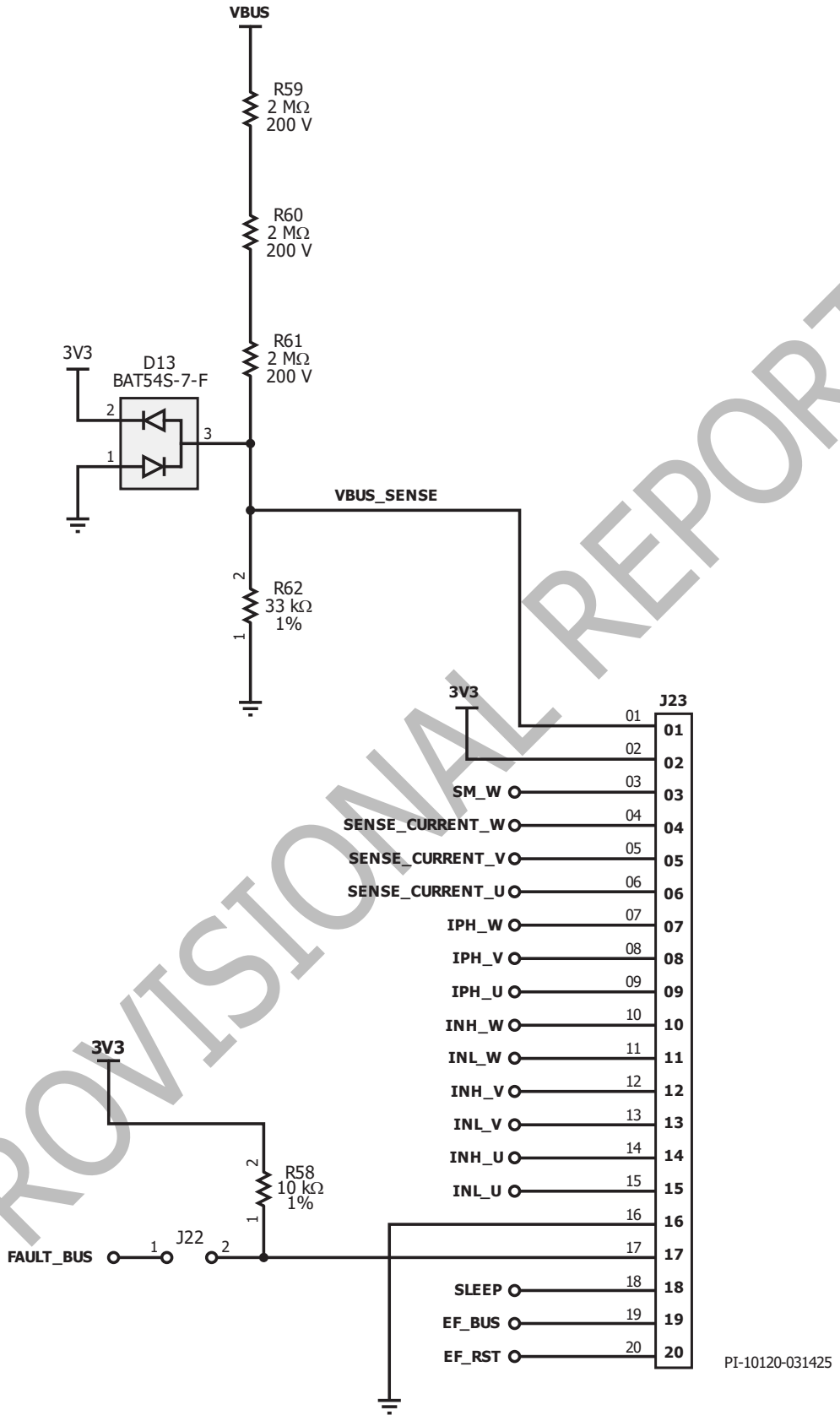

Figure 8 – Microcontroller (MCU) Interface.

4 Circuit Description

This reference design features a three-phase inverter that utilizes three BridgeSwitch-2 BRD2469WB components to drive a high-voltage, three-phase, brushless DC motor. Each BridgeSwitch-2 component integrates two 600 V, N-channel power FREDFETs along with their respective gate drivers into a compact surface-mount package. The power FREDFET incorporates an ultra-soft, fast-recovery diode that is ideally suited for use in inverter drives. A LinkSwitch-TN2 LNK3205D device configured as a high-voltage buck converter supplies the necessary 15 V bias power for the BRD2469WB component. The 3.3 V linear regulator steps down the 15 V external supply voltage to supply power to both the external MCU and the current sensing amplifier circuit.

Each BridgeSwitch-2 device incorporates various fault protection features, such as cycle-by-cycle overcurrent protection (OCP) for both low-side and high-side FREDFETs, overtemperature protection (OTP), and overvoltage protection (OVP). The BridgeSwitch-2 also features the new error flag (EF) pin, which inhibits the device from switching when pulled down by an external microcontroller, and upon encountering any of the following destructive fault conditions: overvoltage (OV), overtemperature (OT), and sixteen consecutive low-side overcurrent (OC) events, when configured in latching mode.

4.1 Inverter Section

The BRD2469WB devices U1, U2, and U3 form the three-phase inverter. The output of the inverter connects to the three-phase BLDC motor through connectors P1, P2, and P3. In the PCB layout, the motor connectors are directly connected to the HB pad (Pin 39) of each BRD2469WB device, but not to the HB pins (Pins 28 and 31). The HB pad and pin are internally connected in the device, allowing more creepage and clearance headroom in the PCB layout.

4.2 Power Section

The power section consists of four main blocks: the input stage, the 15 V auxiliary supply, the 3.3 V low-dropout (LDO) regulator, and the external bias circuitry for each BRD2469WB device.

4.2.1 Input Section

The input section comprises the DC input connector (J6), input diode (D1), input fuse (F1), bypass jumper (J12), and bulk capacitor (C10). Diode D1 provides reverse-polarity protection for the DC input, while fuse F1 safeguards against overcurrent conditions. Capacitor C10 serves as the main bulk capacitance for the entire inverter. Jumper J12 remains open during normal operation and is shorted during efficiency measurements to bypass the fuse and diode. For stable high-voltage DC input applications, a 330 μF capacitor at C10 is sufficient, whereas AC input applications require a minimum of 750 μF. In this reference design, a high-voltage DC supply is used.

4.2.2 15 V Auxiliary Supply

The LNK3205D device (U4), configured as a buck converter, generates the 15 V external bias from the high-voltage DC bus input. Jumper J8 connects the buck converter output to the 15 V DC rail. Alternatively, jumper J9 allows the bias voltage to be supplied externally,

with J7 and J8 left open to disable the buck converter and disconnect its output from the external source. For inverter efficiency measurements, using an external 15 V supply is recommended to isolate inverter performance from overall system efficiency.

For detailed information on the LNK3205D, refer to the datasheet: https://ac-dc.power.com/design-support/product-documents/data-sheets/linkswitch-tn2-data-sheet/

4.2.3 3.3 V LDO

The 3.3 V low-dropout regulator (U5) powers both the external microcontroller (MCU) and the optional current amplifier circuit for shunt-based current feedback applications. Jumper J10, shorted by default, connects the LDO output to the 3.3 V rail. Alternatively, Pin 2 of connector J23 allows the 3.3 V rail to be supplied externally via the MCU interface. If done so, J10 should remain open. LED DS2 provides a visual indication of the 3.3 V rail status.

4.2.4 BridgeSwitch-2 External Supply Biasing

A 15 V external supply is required for the BRD2469WB low-side and high-side drivers. Resistors R27, R28, R29, R30, R31, and R32 limit the current to approximately 2.5 mA into the gate driver supply pins (BPL and BPH). Diodes D5, D7, and D9 serve as high-voltage bootstrap diodes for the high-side gate drivers, while diodes D6, D8, and D10, which are used to isolate the BPL pins, are optional and may be shorted if not required. Capacitors C4, C5, C6, C7, C8, and C9 provide local decoupling for both the low-side and high-side gate driver supplies.

4.3 PWM Input

The input PWM signals INL_U, INH_U, INL_V, INH_V, INL_W, and INH_W control the switching states of the integrated high-side and low-side power FREDFETs. These signals are generated by the system microcontroller at the desired switching frequency. Resistors R4, R5, R6, R7, R8, and R9 act as PWM input filters before routing the signals to the INL and /INH pins of each BRD2469WB device.

4.4 Cycle-by-Cycle Current Limit

Resistors R10, R11, R12, R13, R14, and R15 define the cycle-by-cycle current limit for the integrated low-side and high-side power FREDFETs. With a resistance value of 42.2 kΩ, the current limit is set to 100% of the default overcurrent threshold (7.0 A for the BRD2469WB). For the low-side FREDFET, the cycle-by-cycle overcurrent protection response is selected by configuring the SLP resistor: either 9.53 kΩ by shorting J15, or ≥1 MΩ by keeping both J15 and J16 open. The high-side FREDFET OCP response is fixed to cycle-by-cycle operation by default and is not influenced by the SLP resistor value.

4.5 Latching Current Limit

Setting the SLP programming resistor to 133 kΩ by shorting J16 enables latching current limit protection for the low-side power FREDFET. In this mode, the low-side FREDFET latches off after sixteen consecutive overcurrent events. The Error Flag pin is then driven low to inhibit switching and is only released after either a power cycle or an EF reset command from the MCU. The high-side FREDFET OCP response remains fixed to cycle-by-cycle operation by default and is unaffected by the SLP resistor setting.

4.6 Overvoltage (OV) Protection

The SM pin of BridgeSwitch-2 device U1 is configured to monitor the DC bus voltage via resistors R1, R2, and R3. A total resistance of 6 MΩ sets the overvoltage protection threshold to 362 VDC. When this threshold is exceeded, the EF bus inhibits FREDFET switching on all BridgeSwitch-2 devices after an 80 μs delay. Switching is automatically re-enabled once the bus voltage falls below the hysteresis threshold of approximately 338 VDC, at which point the EF bus is released.

4.7 Error Flag

The Error Flag (EF) pin is an open-drain pin that facilitates fault communication with the microcontroller. It requires a minimum pull-up resistance of 43 kΩ for compatibility with both 3.3 V and 5 V MCUs and is typically connected to other EF pins to form the EF bus.

Under latching fault conditions, such as latching overcurrent or overtemperature faults, the EF pin is driven low to inhibit FREDFET switching. It remains latched until cleared by either a power cycle or an EF reset command via D12 and R52. For hysteretic protection events, such as overvoltage or hysteretic overtemperature, the EF pin is automatically released once safe operating conditions are re-established.

4.8 FAULT Bus

Using the alternate BridgeSwitch-2 product variant (BRD2269) enables the FAULT bus functionality. Shorting jumper J22 pulls the FAULT bus up to the LDO supply, activating it. In this case, jumpers J17, J18, and J19 must be opened to isolate the EF pins from the EF bus.

The FAULT bus reports internal and system status changes via pin 17 of the MCU interface (J23). For detailed information on FAULT status communication, refer to the BridgeSwitch-2 datasheet.

4.9 Device ID

The ID pin allows a specific BridgeSwitch-2 device to inform the system microcontroller of its physical location when the FAULT bus functionality is used. This identification is configured by the ID pin connection.

In this reference design, U1, connected to the SG pin, has a device ID of 80 μs, U2, left floating, has a device ID of 60 μs, and U3, shorted to the BPL pin, has a device ID of 40 μs. In this configuration, U1, with the longest device ID (80 μs), is prioritized during simultaneous fault reporting.

4.10 System Undervoltage Status Updates

Resistors R1, R2, and R3 allow monitoring of the high-voltage DC bus through current detection to the SM pin. During undervoltage events, the FAULT bus sends out messages to the microcontroller at four distinct voltage levels. At a total SM resistance of 6 MΩ, the following levels are set:

Undervoltage (UV) FAULT	DC Bus Level R1 + R2 + R3 = 6 MΩ
UV100	212 V
UV85	182 V
UV70	152 V
UV55	122 V

Table 2 – UV Thresholds.

4.11 External Temperature Monitoring

When using the FAULT bus functionality, the SM pin can also be configured for external temperature monitoring. This is achieved by shorting J5, which connects thermistor RT1 and resistor R22 to the SM pin of device U2. RT1 should be an NTC-type thermistor, while R22 is selected such that the product of the equivalent resistance of RT1 at the desired temperature threshold and R22, multiplied by 100 μA, yields approximately 1.17 V. During operation, U2 reports a system thermal fault via the FAULT bus when this threshold is reached.

4.12 IPH Feedback

This reference design utilizes the IPH signals as current feedback for Field-Oriented Control implementation via MotorXpert. The IPH pin functions as a current source that outputs the instantaneous low-side FREDFET current, scaled according to the device's gain. Resistors R16, R17, and R18 convert the IPH current signal into a corresponding voltage signal, which is fed directly to the microcontroller for current feedback.

For the BRD2469WB, the IPH gain is 30 μA/A, resulting in a 30 μA IPH output for a 1 A low-side FREDFET current. Using a 10 kΩ IPH resistor converts this current into a 300 mV voltage signal, suitable as input to the microcontroller's ADC pin.

4.13 Current Sense Amplifier

This reference design includes on-board op-amp amplifier circuits for a traditional shunt resistor current feedback method. Op-amps U6A, U6B, and U6D act as current sense amplifiers, converting voltage drops across shunt resistors R19, R20, and R21 into voltage signals suitable for the microcontroller ADC inputs. Op-amp U6C generates a 1.65 VDC offset from the 3.3 VDC supply, shifting the current signals into the positive range for ADC compatibility.

The shunt resistors are sized to produce a maximum of ±0.33 V across the LS-to-SG pins at the device's overcurrent protection threshold of 7.0 A. With a differential gain of 4.53, the amplifier circuits output a 1.5 V peak signal centered at 1.65 VDC.

4.14 Microcontroller (MCU) Interface

Connector J23 provides the interface between the BridgeSwitch-2 three-phase inverter board and an external microcontroller.
Table 3 lists the MCU interface pin assignments.

Pin Name	Pin Type	Pin Description
EF_RST	Input	Error Flag reset signal. Momentarily pulling this pin high re-enables device switching after a latching fault.
EF_BUS	Open-drain, I/O	Error Flag state monitoring. Pulling this low inhibits FREDFET switching for BridgeSwitch-2 devices with EF functionality.
SLEEP	Input	Pulling this pin high enables SLEEP mode on BridgeSwitch-2 devices with the self-supply feature (not used in this design).
FAULT_BUS	Open-drain, I/O	FAULT bus monitoring for BridgeSwitch-2 devices. The MCU can pull this low for 160 μs to request status updates, or for 320 μs to re-enable switching after a latching fault.
GND	MCU Ground	Microcontroller ground reference.
INL_U	Input	Phase U (U1) low-side FREDFET PWM control signal.
INH_U	Input	Phase U (U1) high-side FREDFET PWM control signal.
INL_V	Input	Phase V (U2) low-side FREDFET PWM control signal.
INH_V	Input	Phase V (U2) high-side FREDFET PWM control signal.
INL_W	Input	Phase W (U3) low-side FREDFET PWM control signal.
INH_W	Input	Phase W (U3) high-side FREDFET PWM control signal.
IPH_U	Output	Phase U (U1) IPH output.
IPH_V	Output	Phase V (U2) IPH output.
IPH_W	Output	Phase W (U3) IPH output.
SENSE_CURRENT_U	Output	Phase U (U1) R_{SHUNT} voltage amplifier output.
SENSE_CURRENT_V	Output	Phase V (U2) R_{SHUNT} voltage amplifier output.
SENSE_CURRENT_W	Output	Phase W (U3) R_{SHUNT} voltage amplifier output.
SM_W	Input	Optional SM pin input for Phase W (U3).
3V3	Power Input	3.3 V microcontroller supply input.
VBUS_SENSE	Output	Voltage divider output for high-voltage DC bus sensing (scale-down factor: 0.0055).

Table 3 – MCU Interface Pinout Description.

5 Printed Circuit Board Layout

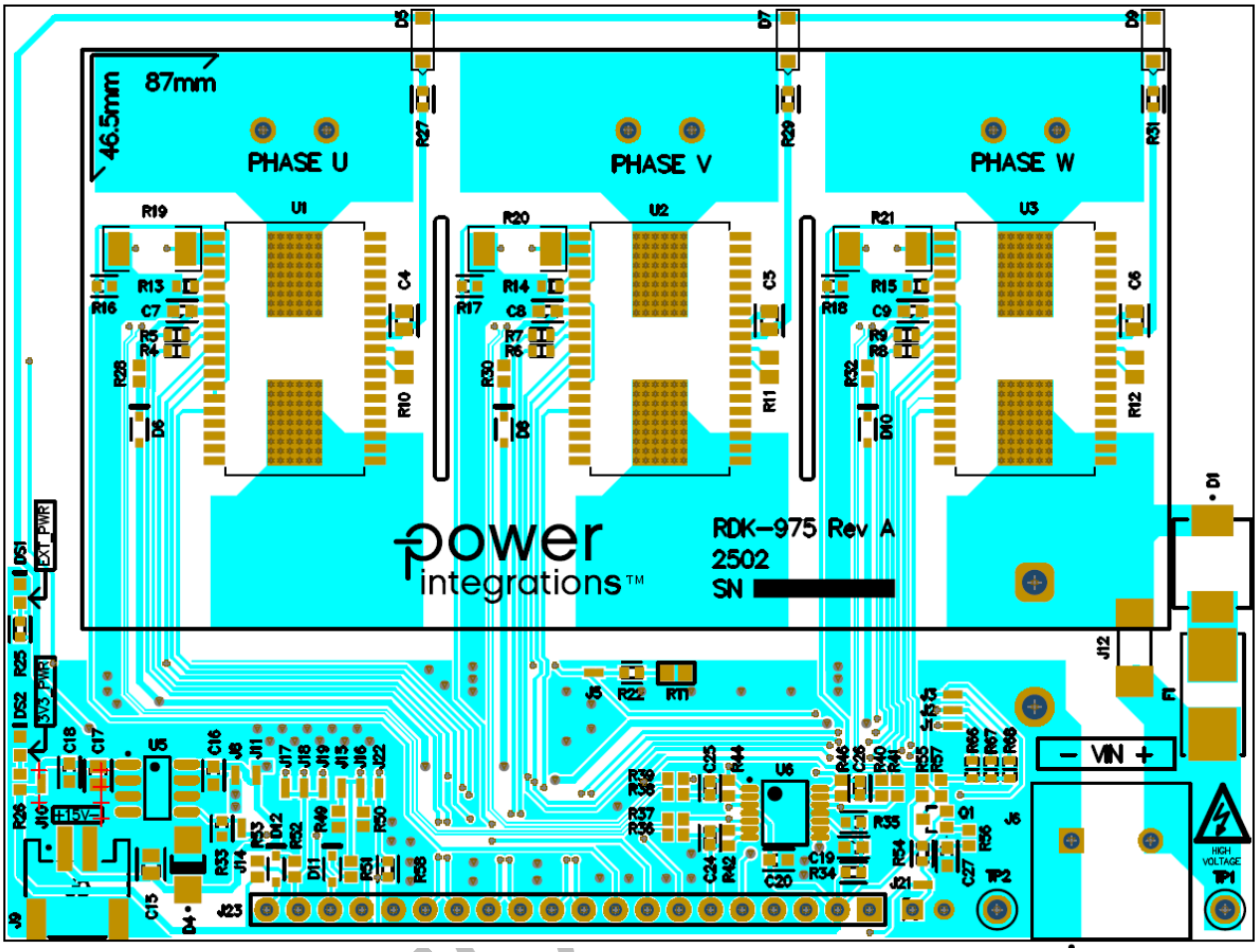

Figure 9 – Printed Circuit Board Layout Top View.

Notes:

1. The overall PCB dimension is 100 mm x 75 mm (L x W).
2. The inverter PCB dimension is 87 mm x 46.5 mm (L x W) – outlined by the black rectangle.
3. PCB Specifications:
   - Board thickness: 2 mm
   - Board material: FR4
   - Copper weight: 2 oz
   - No. of layers: 2

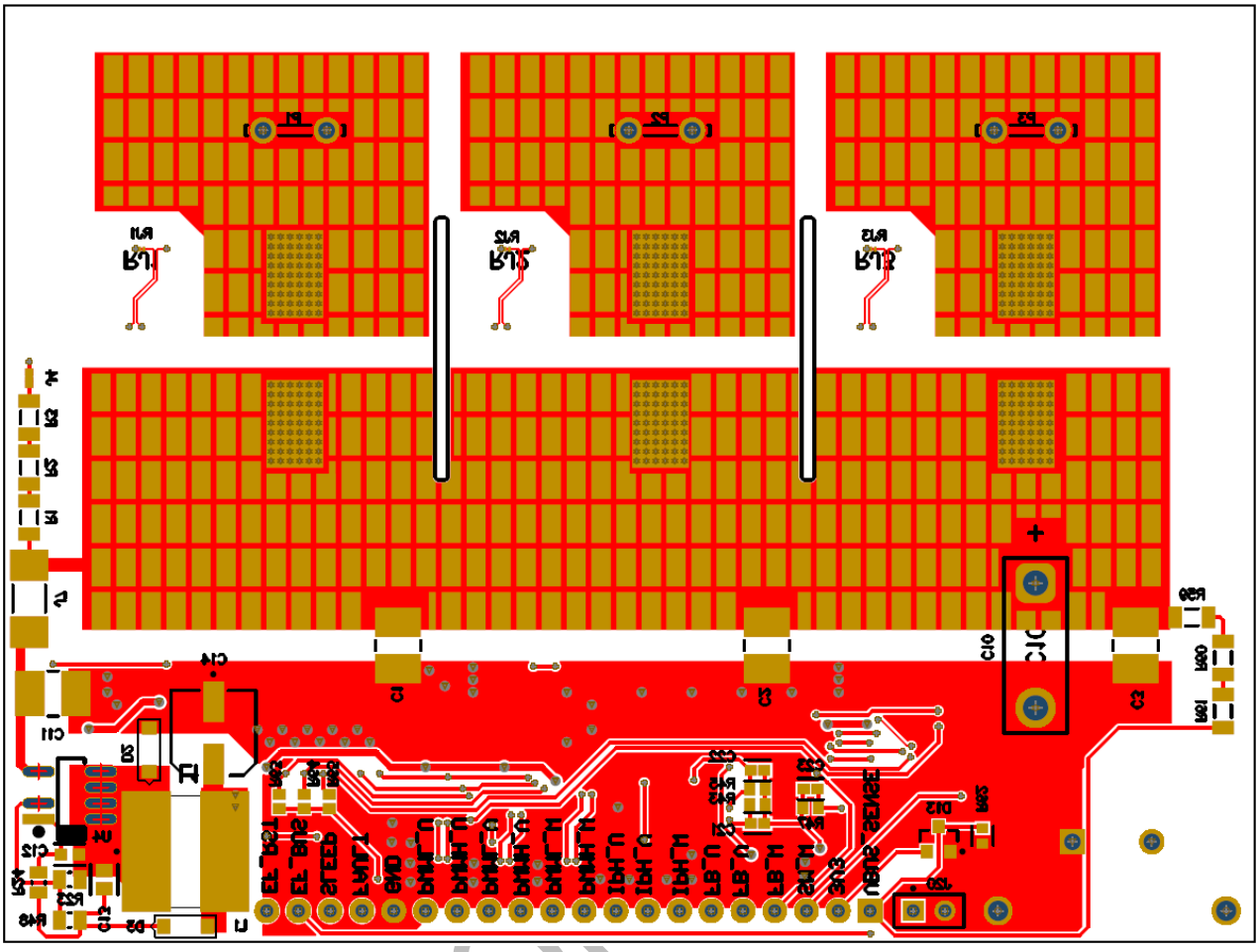

Figure 10 – Printed Circuit Board Layout Bottom View.

6 Bill of Materials

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	4	C1, C2, C3, C11	0.1 μF, 630 V, Ceramic, X7R, 1812	GRM43DR72J104KW01K	Murata Electronics
2	4	C4, C5, C6, C15	4.7 μF, 25 V, Ceramic, X7R, 0805	CL21B475KAFNNNE	Samsung
3	8	C7, C8, C9, C16, C18, C19, C20, C27	1 μF, 25 V, Ceramic, X7R, 0603	GCM188R71E105KA64D	Murata Electronics
4	1	C10	330 μF, 20%, 450 V, Aluminum, TH	861221485017	Würth Elektronik
5	1	C12	0.1 μF, 50 V, Ceramic, X7R, 0603	CL10B104KB8NNND	Samsung
6	2	C13, C17	10 μF, 16 V, Ceramic, X7R, 0805	CL21B106KOQNNNE	Samsung
7	1	C14	22 μF, 20%, 50 V, Aluminum Hybrid, SMD	EEH-ZC1H220P	Panasonic
8	6	C21, C22, C23, C24, C25, C26	220 pF, 50 V, Ceramic, C0G, 0603	C1608C0G1H221J080AA	TDK Corporation
9	1	D1	600 V, 6 A, Standard, DO-214AB	SMLJ60S6-TP	Micro Commercial
10	5	D2, D3, D5, D7, D9	600 V, 1 A, Standard, SOD-123FL	UFM15PL-TP	Micro Commercial
11	1	D4	18 V, 1.5 W, Zener, SMA	SZ1SMA5931BT3G	onsemi
12	5	D6, D8, D10, D11, D12	75 V, 150 mA, Standard, SOD-323	1N4148WS-7-F	Diodes Incorporated
13	1	D13	30 V, 200 mA, Schottky, SOT-23	BAT54S-7-F	Diodes Incorporated
14	2	DS1, DS2	Red, LED, Chip SMD	LTST-C190KRKT	Lite-On Inc.
15	1	F1	4 A, 125 VAC/VDC, 2-SMD	0154004.DR	Littelfuse Inc.
16	16	J1, J2, J3, J4, J5, J8, J10, J11, J14, J15, J16, J17, J18, J19, J21, J22	PCB Jumper	JUMPER	
17	1	J6	2P, 6.35 mm, Terminal Block, Side Ent.	1714955	Phoenix Contact
18	2	J7, J12	Tin Jumper, SMD	S1911-46R	Harwin Inc.
19	1	J9	2 pos, 2 mm pitch, Header, SMD R/A	620102131822	Würth Elektronik
20	1	J20	2 pos, 2.54 mm, Header, Vertical	M20-9990245	Harwin Inc.
21	1	J23	20 pos, 2.54 mm, Header, Vertical	PH1-20-UA	Adam Tech
22	1	L1	680 μH, 360 mA, 2.25 Ω, SMD	744776268	Würth Elektronik
23	3	P1, P2, P3	0.250”, Quick Connect Tab	1287-ST	Keystone Electronics
24	1	Q1	40 V, 0.2 A, PNP Transistor, SC70-3	MMBT3906WT1G	onsemi
25	6	R1, R2, R3, R59, R60, R61	RES, 2 MΩ, 1%, 1/4 W, 1206	ERJ-8ENF2004V	Panasonic
26	9	R4, R5, R6, R7, R8, R9, R66, R67, R68	RES, 10 Ω, 1%, 1/10 W, 0603	ERJ-3EKF10R0V	Panasonic
27	3	R10, R11, R12	RES, 42.2 kΩ, 1%, 1/8 W, 0805	ERJ-6ENF4222V	Panasonic
28	3	R13, R14, R15	RES, 42.2 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF4222V	Panasonic
29	8	R16, R17, R18, R25, R33, R34, R35, R58	RES, 10 kΩ, 1%, 1/10 W, 0603	CRGCQ0603F10K	TE Connectivity
30	3	R19, R20, R21	RES, 47 mΩ, 1%, 3/4 W, 2010	UR73D2HTTE47L0F	KOA Speer Electronics
31	1	R22	RES, 6.49 kΩ, 1%, 1/10 W, 0603	CRCW06036K49FKEA	Vishay Dale
32	1	R23	RES, 2.49 kΩ, 1%, 1/4 W, 0805	RK73H2ATTD2491F	KOA Speer Electronics
33	1	R24	RES, 43 kΩ, 5%, 1/8 W, 0805	RC0805JR-0743KL	YAGEO
34	1	R26	RES, 620 Ω, 5%, 1/10 W, 0603	ERJ-3GEYJ621V	Panasonic
35	3	R27, R29, R31	RES, 220 Ω, 5%, 1/10 W, 0603	ERJ-3GEYJ221V	Panasonic
36	3	R28, R30, R32	RES, 390 Ω, 1%, 1/10 W, 0603	ERJ-3EKF3900V	Panasonic

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
37	9	R36, R37, R38, R39, R40, R41, R51, R52, R56	RES, 1 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF1001V	Panasonic
38	6	R42, R43, R44, R45, R46, R47	RES, 4.53 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF4531V	Panasonic
39	1	R48	RES, 15.8 kΩ, 1%, 1/4 W, 0805	RK73H2ATTD1582F	KOA Speer Electronics
40	1	R49	RES, 9.53 kΩ, 1%, 1/10 W, 0603	RK73H1JTTD9531F	KOA Speer Electronics
41	1	R50	RES, 133 kΩ, 1%, 1/10 W, 0603	CRCW0603133KFKEA	Vishay Dale
42	1	R53	RES, 43 kΩ, 1%, 1/10 W, 0603	RK73H1JTTD4302F	KOA Speer Electronics
43	2	R55, R57	RES, 8.2 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF8201V	Panasonic
44	1	R62	RES, 33 kΩ, 1%, 1/10 W, 0603	CRCW060333K0FKEA	Vishay Dale
45	1	RT1	100 kΩ, 4330 K, NTC Thermistor, 0603	ERT-J1VS104JA	Panasonic
46	1	TP1	Test Point, Red, Thru-hole Mount	5010	Keystone Electronics
47	1	TP2	Test Point, Black, Thru-hole Mount	5011	Keystone Electronics
48	3	U1, U2, U3	BridgeSwitch-2, Max. BLDC Motor Current 7 A (DC), InSOP-L38C	BRD2469WB	Power Integrations
49	1	U4	LinkSwitch-TN2, SO-8C	LNK3205D	Power Integrations
50	1	U5	IC, REG, LDO, 3.3 V, 250 mA, 8-SOIC	L4931CD33-TR	STMicroelectronics
51	1	U6	IC, GP Op-Amp, Quad Circuit, 14-TSSOP	AD8648ARUZ	Analog Devices Inc.

Table 4 – Bill of Materials.

7 Performance Data

This section presents the waveforms and performance data of the RDK-975 BRD2469WB inverter. Unless otherwise noted in a specific subsection, all measurements were taken under the default test conditions listed in Table 5.

Parameter	Value	Remarks
Input Voltage (DC)	340 VDC	Supplied by a stable high-voltage DC source.
Motor Control Algorithm	Sensorless FOC with IPH Current Reconstruction	Configured via MotorXpert Suite 3.0
PWM Switching Frequency	10.0 kHz	-
Startup Control Scheme	I/F Control	-
FOC Control Loop Frequency	10.0 kHz	-
Motor Speed	3000 RPM	Steady-state operation
Phase Current (Light Load)	550 mA_{RMS}	-
Phase Current (Full Load)	2.20 A_{RMS}	Rated phase current of the BRD2469WB
Current Feedback	IPH	Shunt resistors R19, R20, and R21 shorted
Ambient Temperature	23.0 °C	-
SLP Pull-down Resistor	133 kΩ	Configuration: • J15 Open (9.53 kΩ) • J16 Shorted (133 kΩ)
Fault Response	-	• Latching LS OCP • Latching OTP

Table 5 – Default Test Conditions.

7.1 Start-Up Operation

7.1.1 Start-Up Waveforms

A 340 VDC bus voltage is applied with a 50 V/ms slew rate, producing the start-up waveforms shown below. The plots display the 15 V rail voltage, low-side bypass pin voltage, and high-side bypass pin voltage, following the recommended start-up sequence outlined in Section 8.2 of the Appendix.

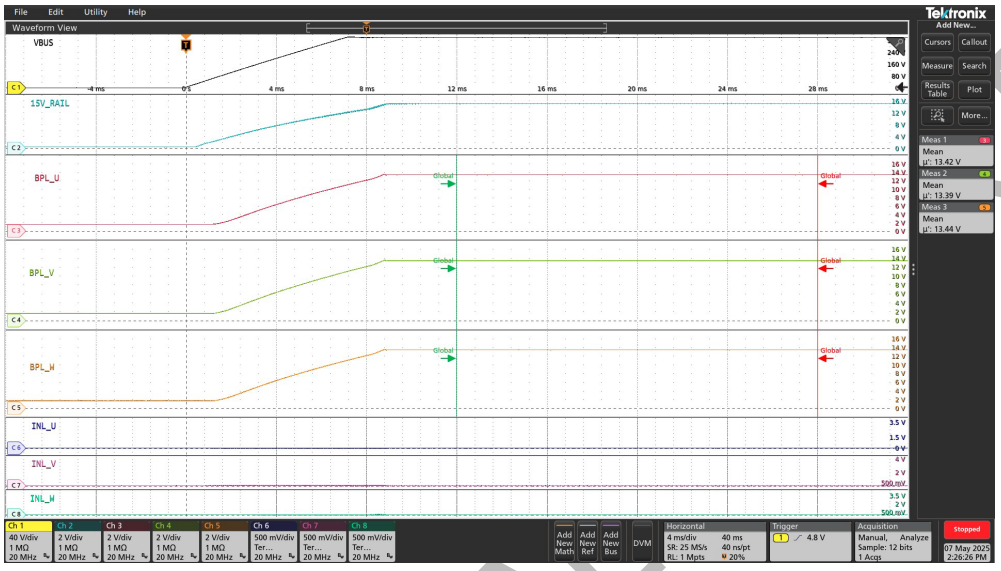

Figure 11 – 15 V Rail and BPL-to-SG Voltages at Start-up.

CH1: V_{BUS}, 40 V/div
CH2: V_{15V_RAIL}, 2 V/div
CH3: V_{BPL_U}, 2 V/div
CH4: V_{BPL_V}, 2 V/div
CH5: V_{BPL_W}, 2 V/div
CH6: V_{INL_U}, 0.5 V/div
CH7: V_{INL_V}, 0.5 V/div
CH8: V_{INL_W}, 0.5 V/div
Time Scale: 4 ms/div

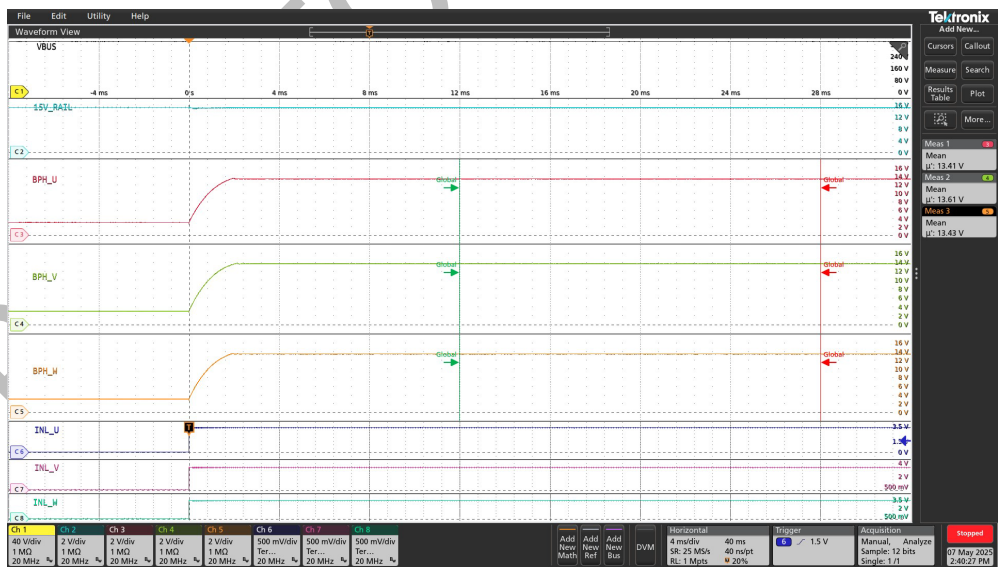

Figure 12 – BPH-to-HB Voltages at Start-up.

CH1: V_{BUS}, 40 V/div
CH2: V_{15V_RAIL}, 2 V/div
CH3: V_{BPH_U}, 2 V/div
CH4: V_{BPH_V}, 2 V/div
CH5: V_{BPH_W}, 2 V/div
CH6: V_{INL_U}, 0.5 V/div
CH7: V_{INL_V}, 0.5 V/div
CH8: V_{INL_W}, 0.5 V/div
Time Scale: 4 ms/div

7.1.2 Motor Start-Up Waveforms

The following waveforms illustrate the motor start-up behavior under light-load (550 mA_{RMS}) and full-load (2.2 A_{RMS}) conditions.

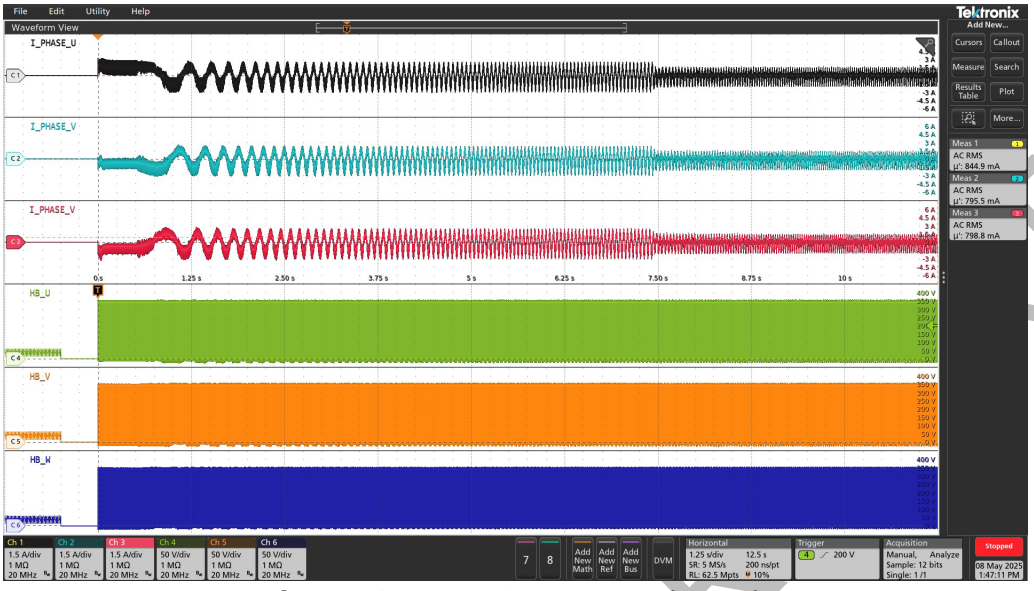

Figure 13 – Motor Start-up at Light Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1.25 s/div

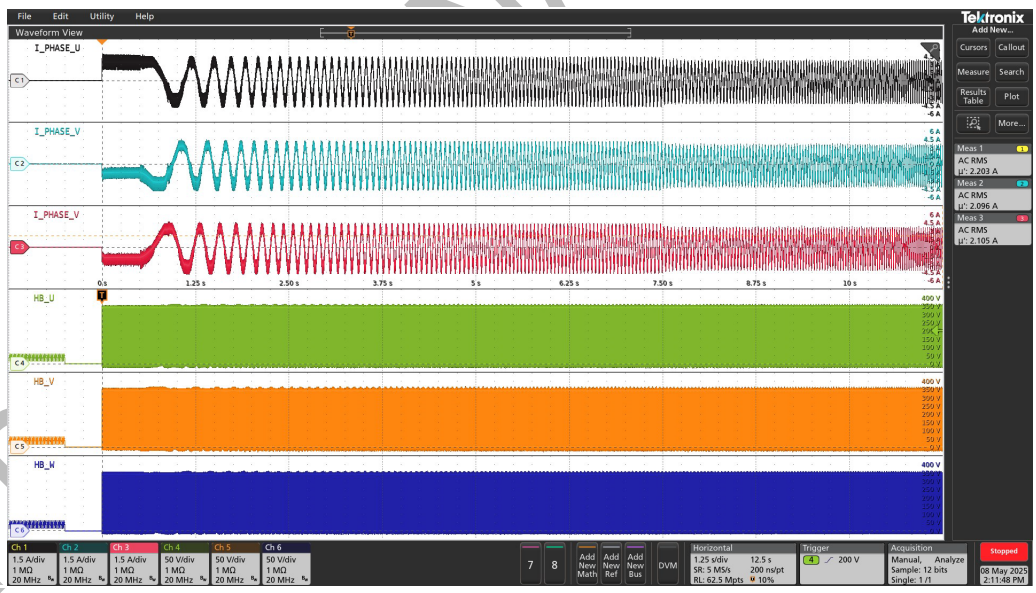

Figure 14 – Motor Start-up at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1.25 s/div

7.2 Steady-State Operation

7.2.1 Phase Voltages and Motor Phase Currents at Steady-State

The following waveforms present the phase voltage (low-side V_{DS}) and motor phase currents during operation at light load (550 mA_{RMS}) and full load (2.2 A_{RMS}).

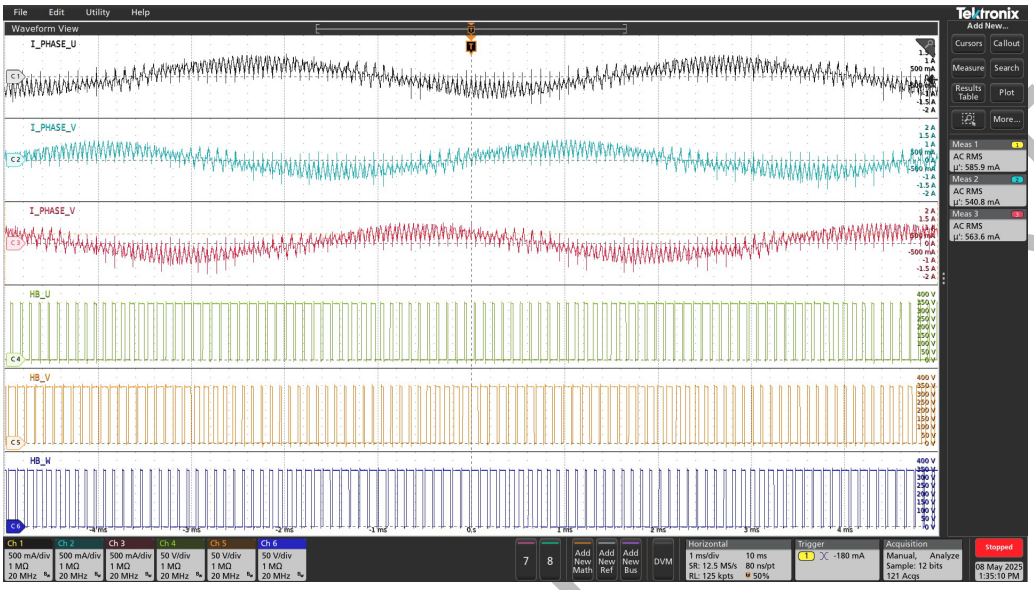

Figure 15 – Steady State Phase Voltages and Phase Currents at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1 ms/div

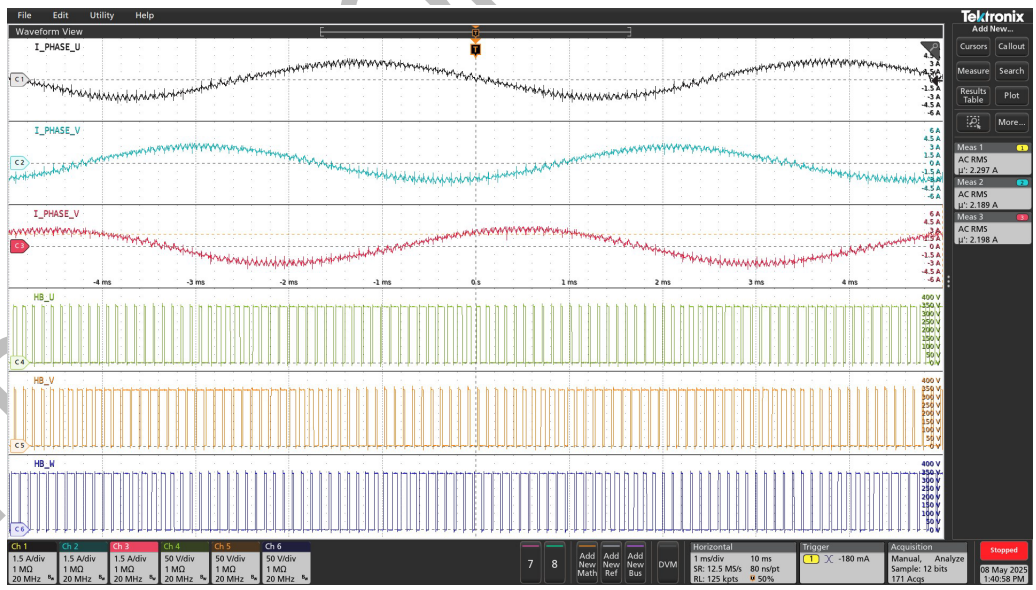

Figure 16 – Steady State Phase Voltages and Phase Currents at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1 ms/div

7.2.2 Low-Side Drain-to-Source Voltage Slew Rate at Steady State

The following waveforms show the voltage slew rate at the turn-on and turn-off transitions of the low-side FREDFET. Measurements were taken at light load and full load conditions, captured at both the positive and negative peaks of the phase current.

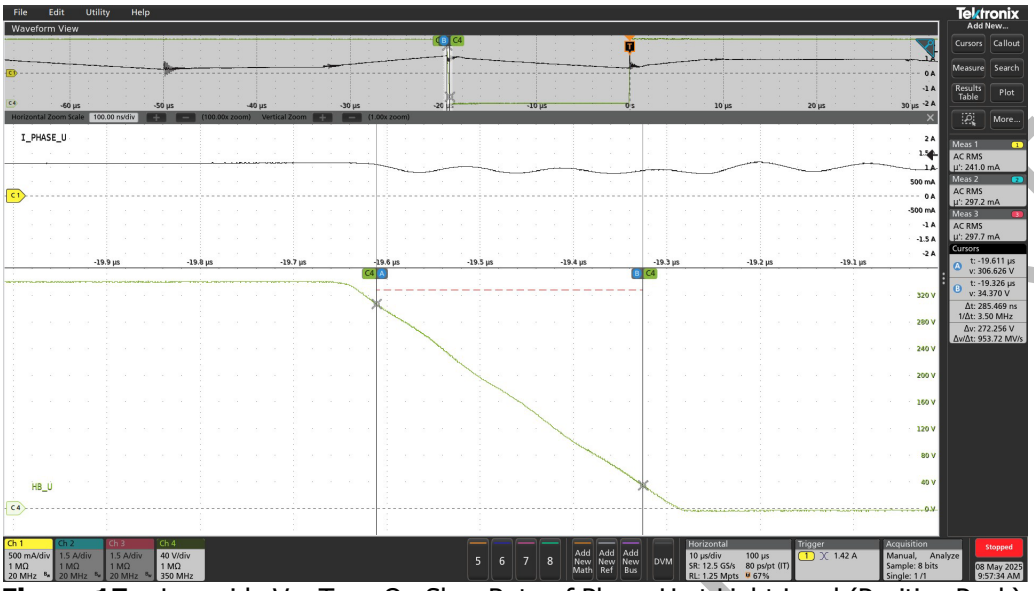

Figure 17 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Light Load (Positive Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 0.95 V/µs

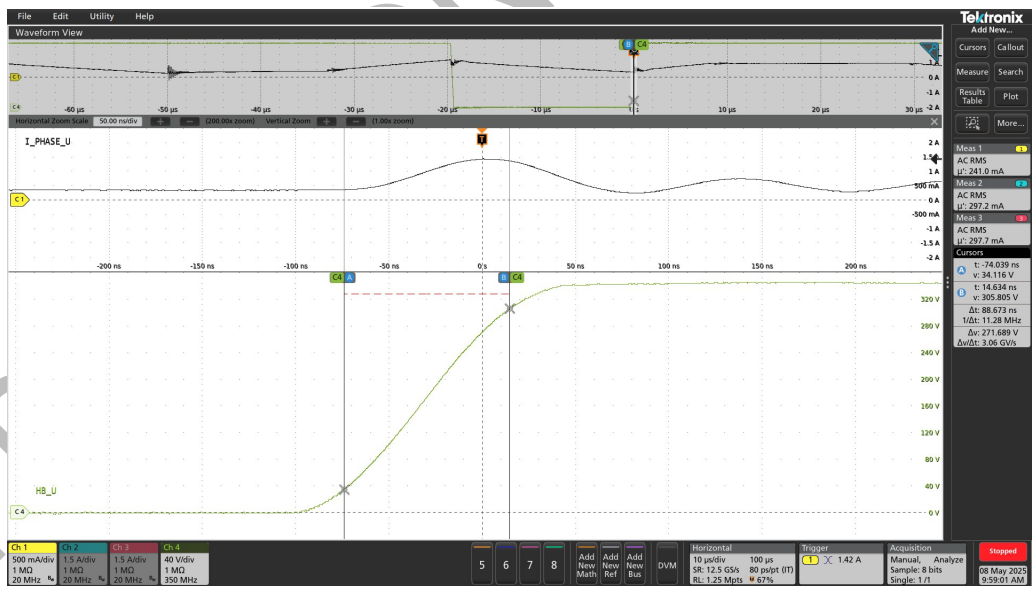

Figure 18 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Light Load (Positive Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.06 V/µs

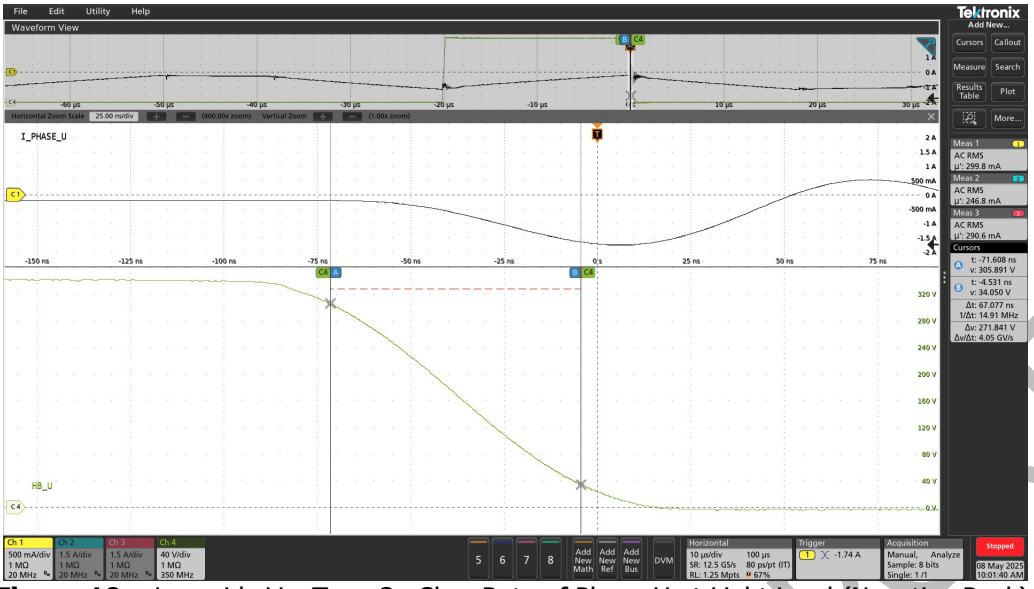

Figure 19 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Light Load (Negative Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 4.05 V/µs

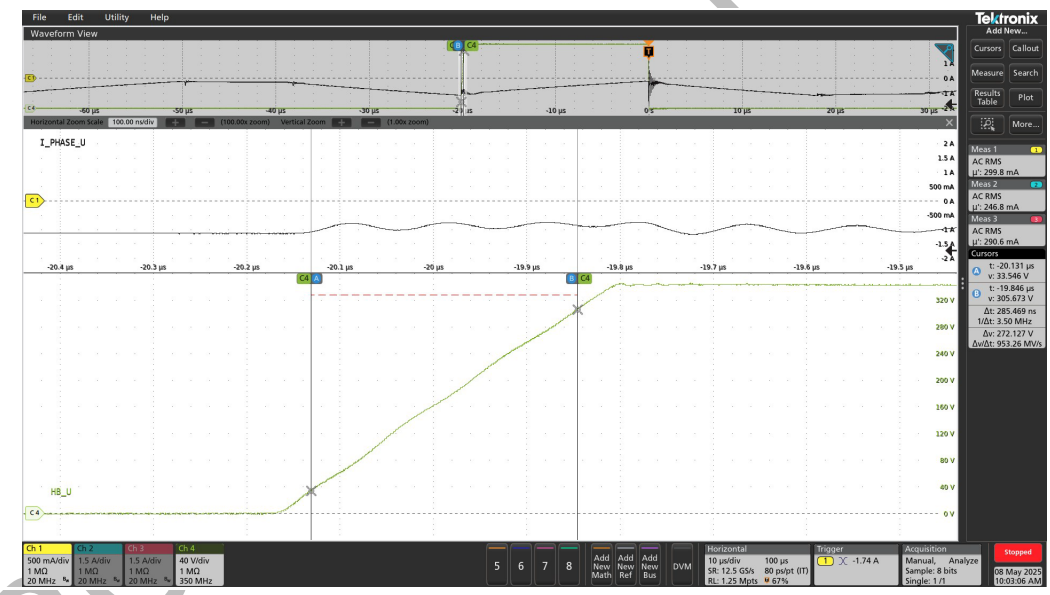

Figure 20 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Light Load (Negative Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 0.95 V/µs

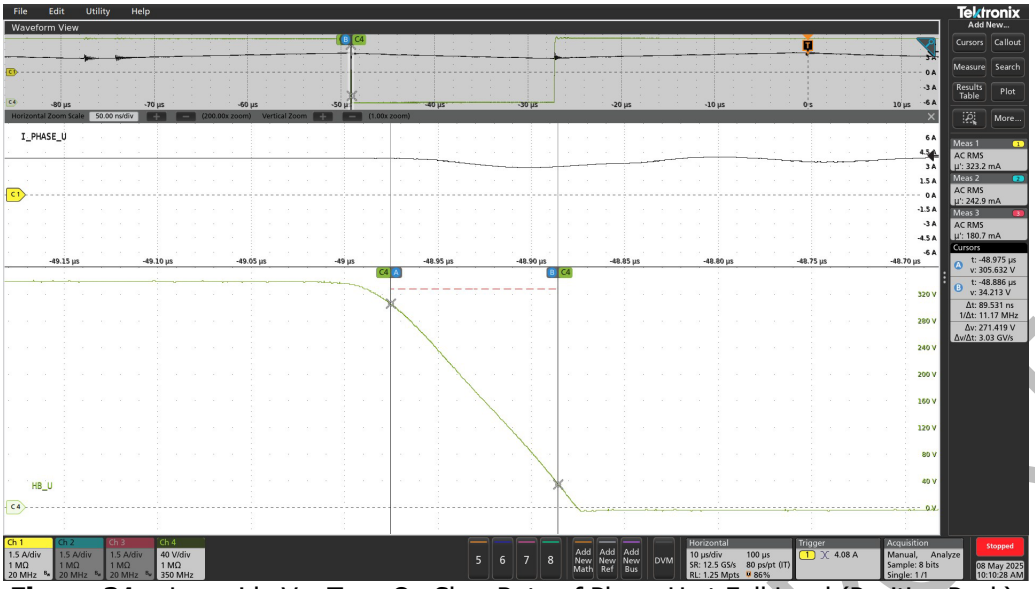

Figure 21 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Full Load (Positive Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.03 V/µs

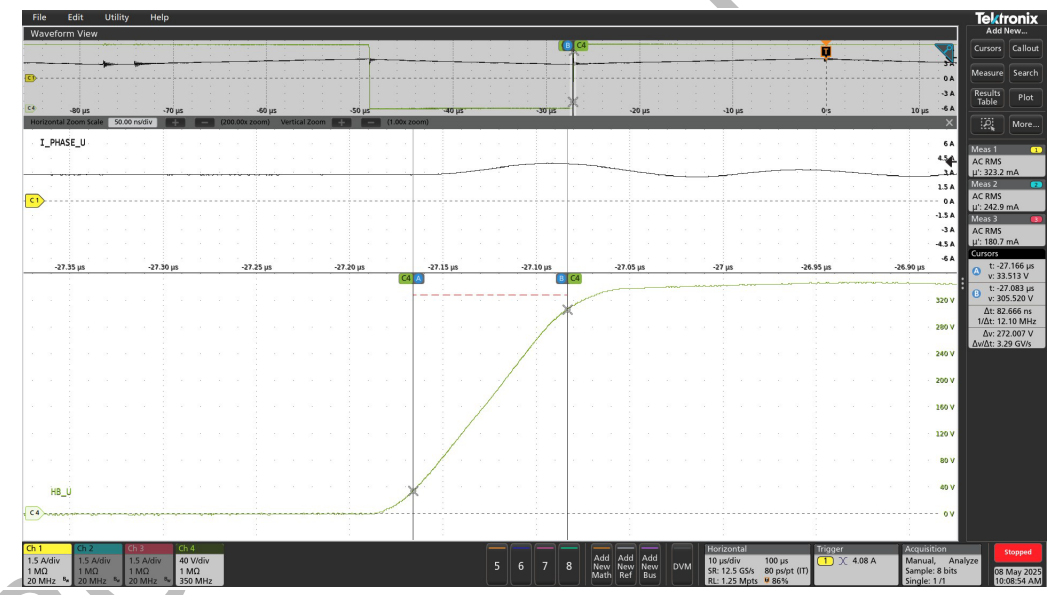

Figure 22 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Full Load (Positive Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.29 V/µs

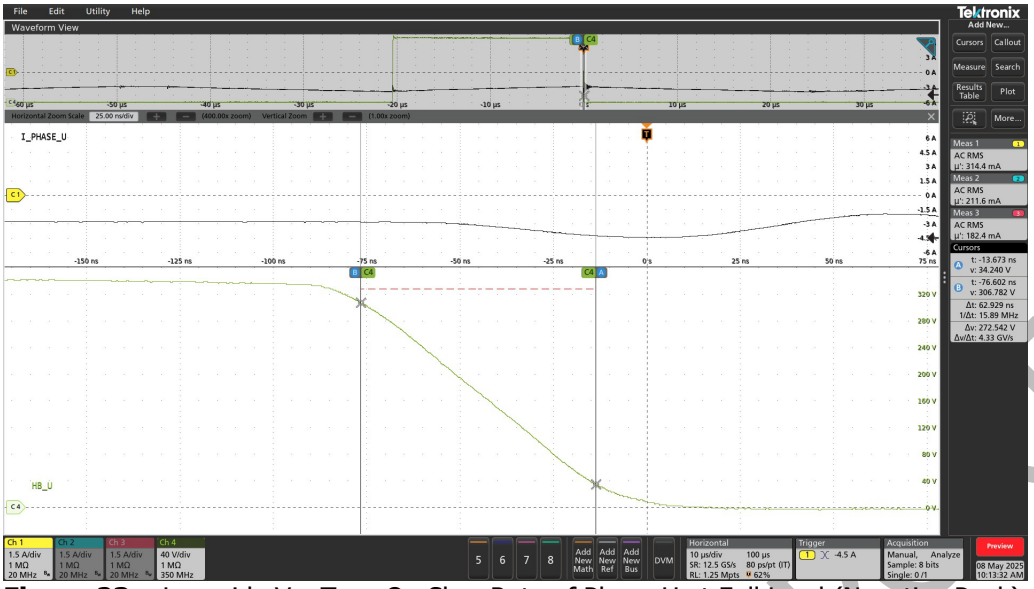

Figure 23 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Full Load (Negative Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 4.33 V/µs

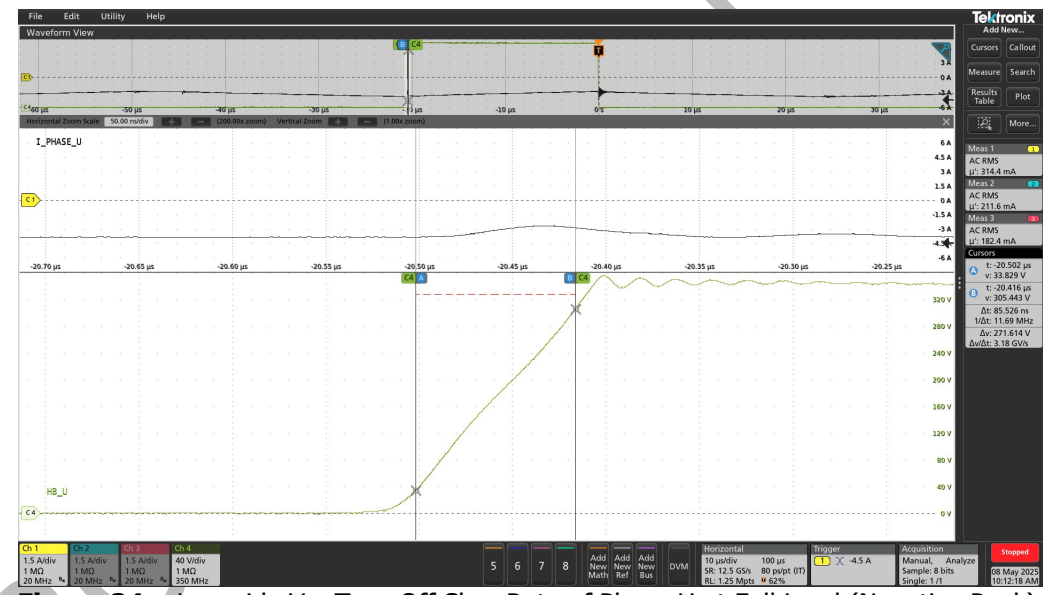

Figure 24 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Full Load (Negative Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.18 V/µs

The table below summarizes the measured V_{DS} slew rates at different loading conditions and opposite current peaks:

	Positive Peak		Negative Peak	
	Turn-On	**Turn-Off**	**Turn-On**	**Turn-Off**
Light Load	0.95 V/µs	3.06 V/µs	4.05 V/µs	0.95 V/µs
Full Load	3.03 V/µs	3.29 V/µs	4.33 V/µs	3.18 V/µs

Table 6 – Low-side V_{DS} Slew Rate.

7.2.3 BPL and BPH Ripple at Steady-State

The following waveforms show the bypass supply voltage DC levels and voltage ripple during steady-state operation at light load and full load conditions.

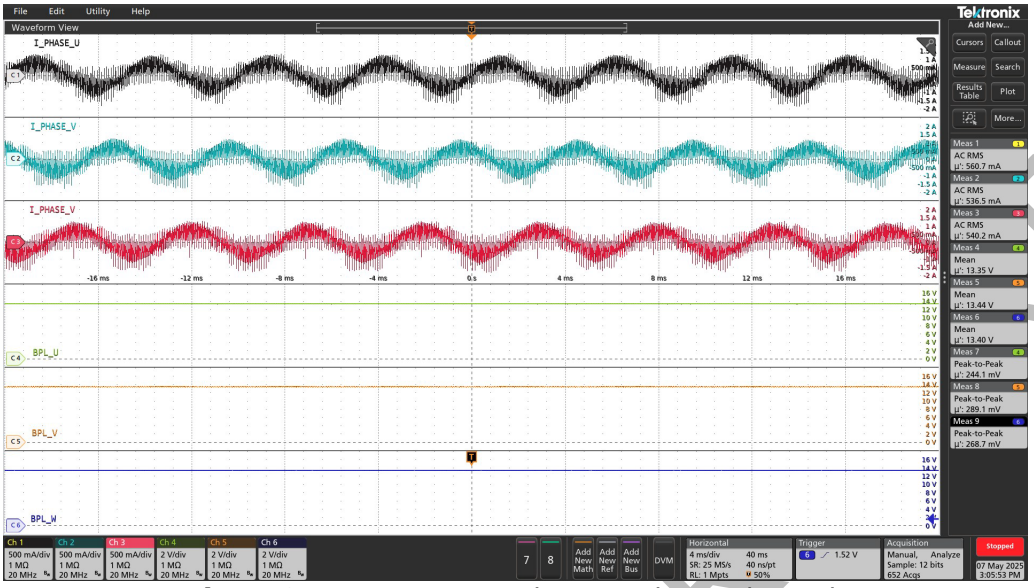

Figure 25 – Average BPL Voltage Levels at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPL_U}, 2 V/div $V_{BPL\_U, AVERAGE}$ = 13.4 V
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPL_V}, 2 V/div $V_{BPL\_V, AVERAGE}$ = 13.4 V
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPL_W}, 2 V/div $V_{BPL\_W, AVERAGE}$ = 13.4 V
Time Scale: 4 ms/div

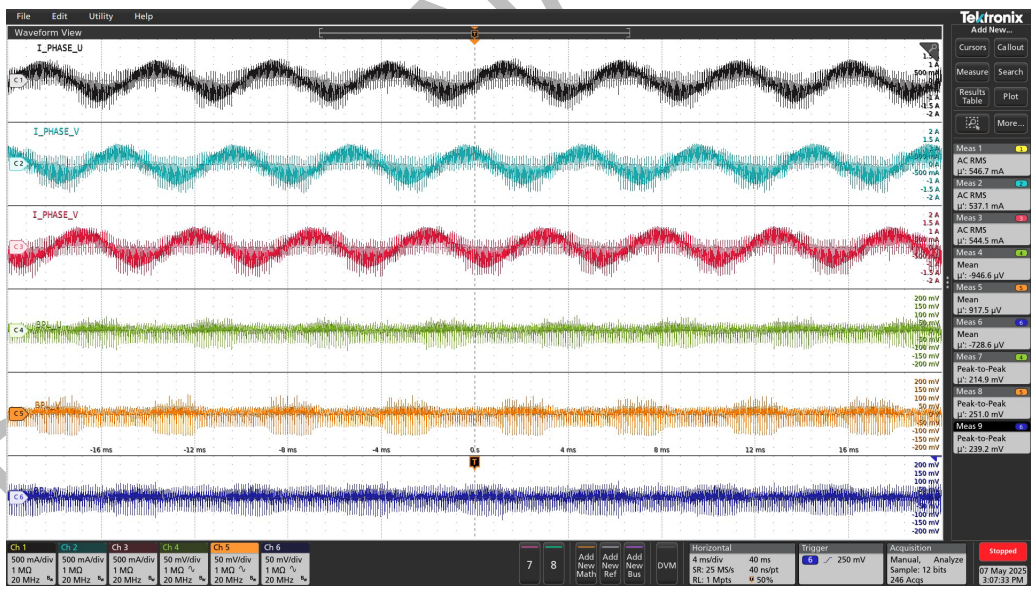

Figure 26 – BPL Ripple Voltage at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPL_U}, 50 mV/div $V_{BPL\_U, RIPPLE}$ = 215 mV_{pp}
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPL_V}, 50 mV/div $V_{BPL\_V, RIPPLE}$ = 251 mV_{pp}
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPL_W}, 50 mV/div $V_{BPL\_W, RIPPLE}$ = 239 mV_{pp}
Time Scale: 4 ms/div

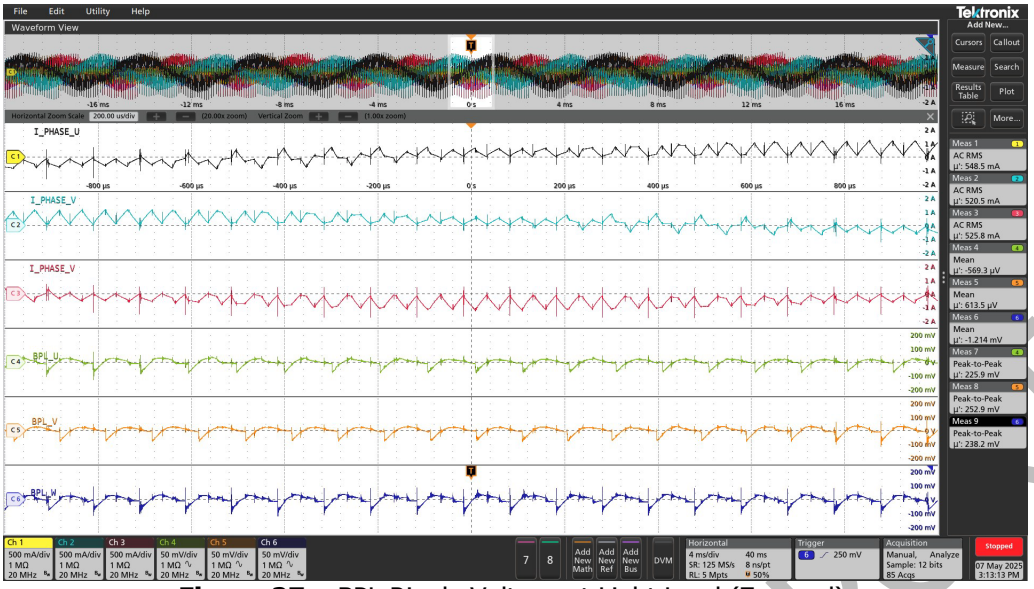

Figure 27 – BPL Ripple Voltage at Light Load (Zoomed).

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPL_U}, 50 mV/div $V_{BPL\_U, RIPPLE}$ = 215 mV_{pp}
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPL_V}, 50 mV/div $V_{BPL\_V, RIPPLE}$ = 251 mV_{pp}
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPL_W}, 50 mV/div $V_{BPL\_W, RIPPLE}$ = 239 mV_{pp}
Time Scale (Zoomed Area): 200 µs/div

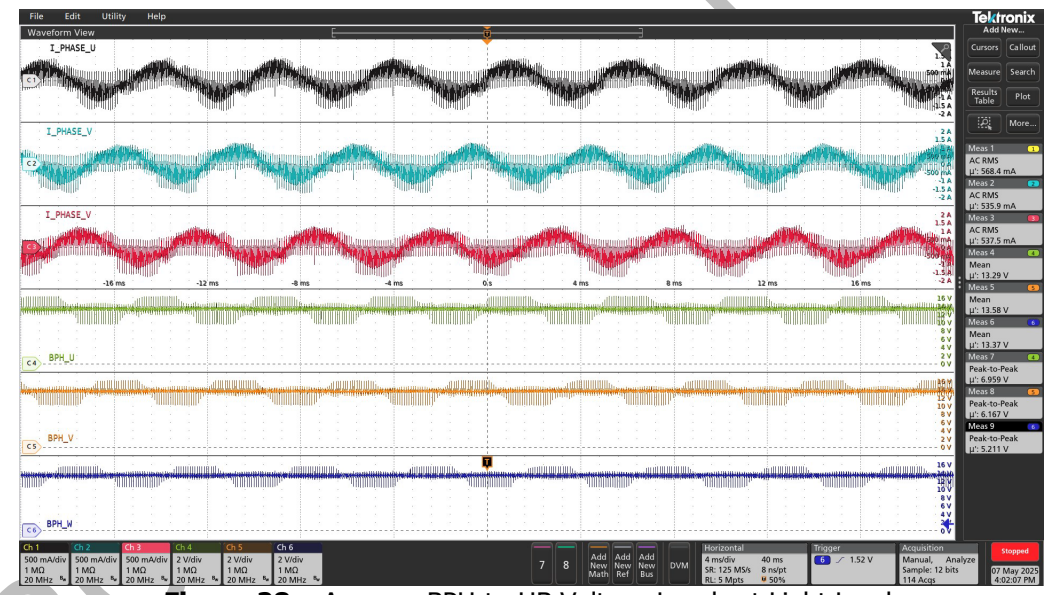

Figure 28 – Average BPH-to-HB Voltage Levels at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPH_U}, 2 V/div $V_{BPH\_U, AVERAGE}$ = 13.3 V
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPH_V}, 2 V/div $V_{BPH\_V, AVERAGE}$ = 13.6 V
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPH_W}, 2 V/div $V_{BPH\_W, AVERAGE}$ = 13.4 V
Time Scale: 4 ms/div

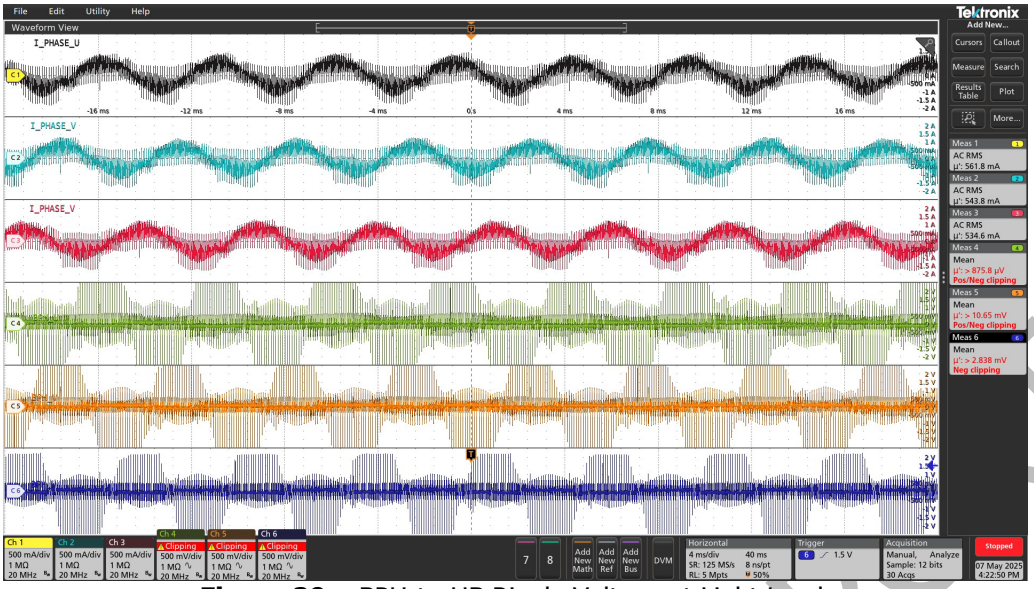

Figure 29 – BPH-to-HB Ripple Voltage at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPH_U}, 0.5 V/div
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPH_V}, 0.5 V/div
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPH_W}, 0.5 V/div
Time Scale: 4 ms/div

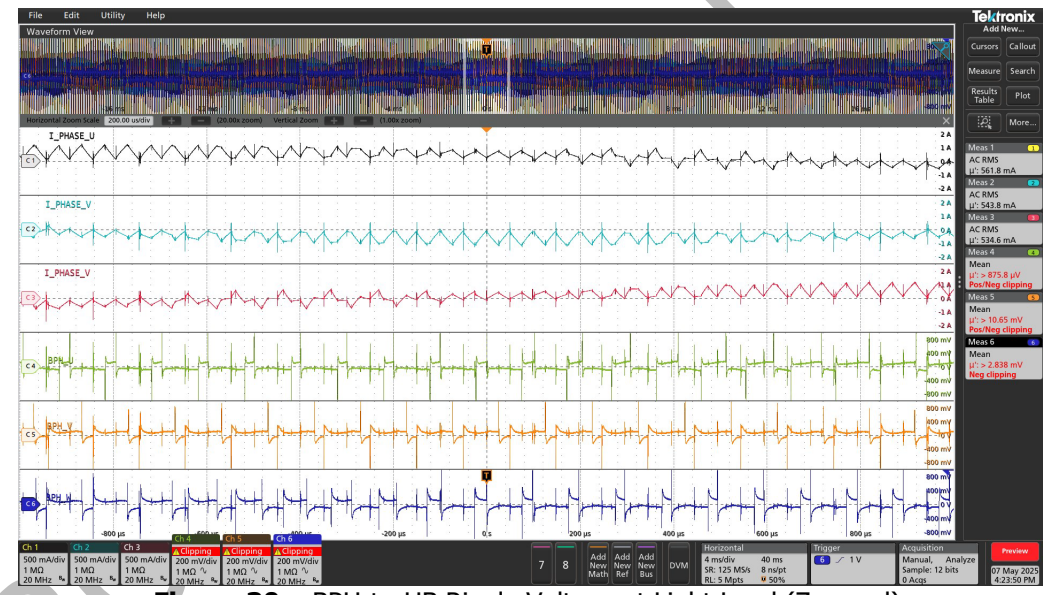

Figure 30 – BPH-to-HB Ripple Voltage at Light Load (Zoomed).

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPH_U}, 0.2 V/div $V_{BPH\_U,\ RIPPLE}$ < 900 mV_{pp}
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPH_V}, 0.2 V/div $V_{BPH\_V,\ RIPPLE}$ < 900 mV_{pp}
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPH_W}, 0.2 V/div $V_{BPH\_W,\ RIPPLE}$ < 900 mV_{pp}
Time Scale (Zoomed Area): 200 µs/div

Note: Measurements exclude high-frequency, switching-induced voltage spikes.

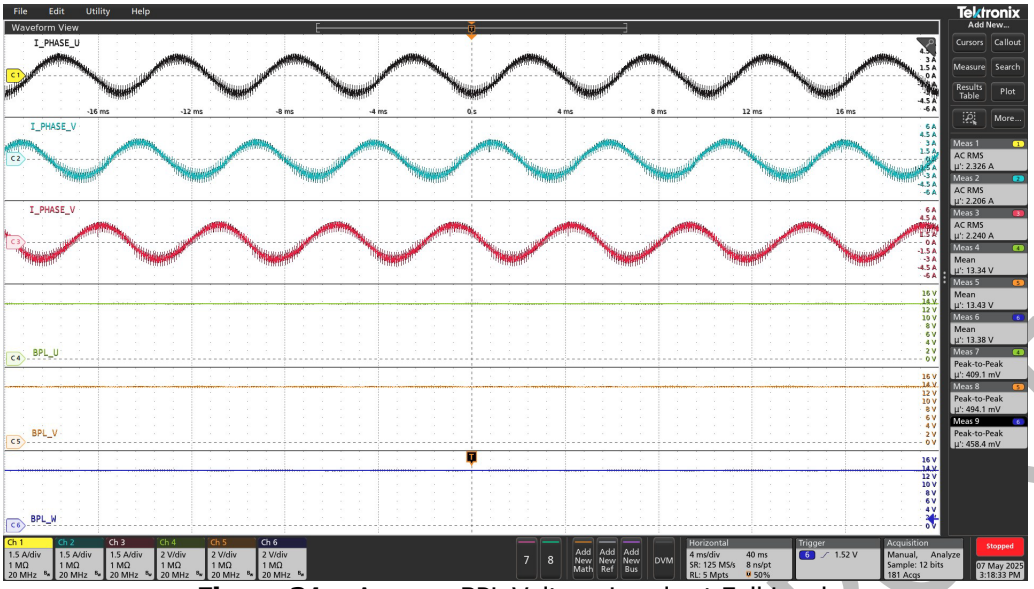

Figure 31 – Average BPL Voltage Levels at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 2 V/div $V_{BPL\_U, AVERAGE}$ = 13.3 V
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 2 V/div $V_{BPL\_V, AVERAGE}$ = 13.4 V
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 2 V/div $V_{BPL\_W, AVERAGE}$ = 13.4 V
Time Scale: 4 ms/div

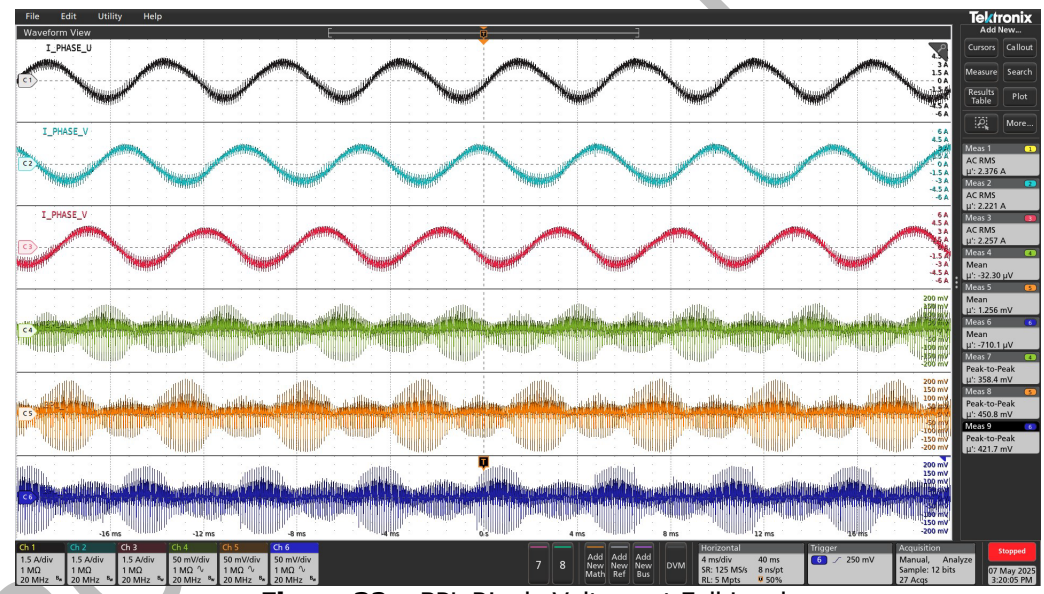

Figure 32 – BPL Ripple Voltage at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 50 mV/div $V_{BPL\_U, RIPPLE}$ = 358 mV_{pp}
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 50 mV/div $V_{BPL\_V, RIPPLE}$ = 451 mV_{pp}
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 50 mV/div $V_{BPL\_W, RIPPLE}$ = 422 mV_{pp}
Time Scale: 4 ms/div

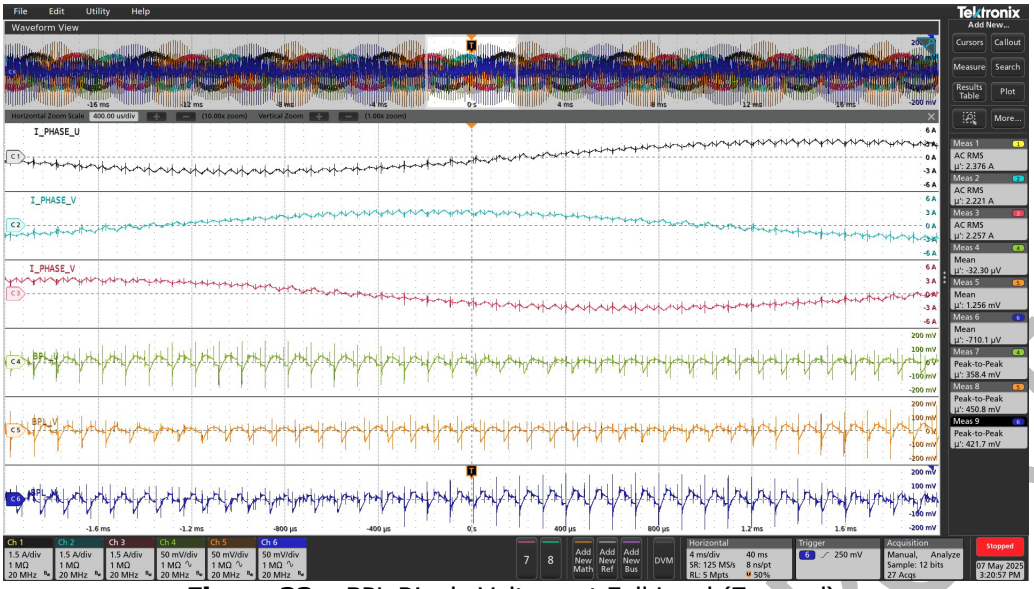

Figure 33 – BPL Ripple Voltage at Full Load (Zoomed).

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 50 mV/div $V_{BPL\_U,\ RIPPLE}$ = 358 mV_{pp}
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 50 mV/div $V_{BPL\_V,\ RIPPLE}$ = 451 mV_{pp}
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 50 mV/div $V_{BPL\_W,\ RIPPLE}$ = 422 mV_{pp}
Time Scale (Zoomed Area): 400 µs/div

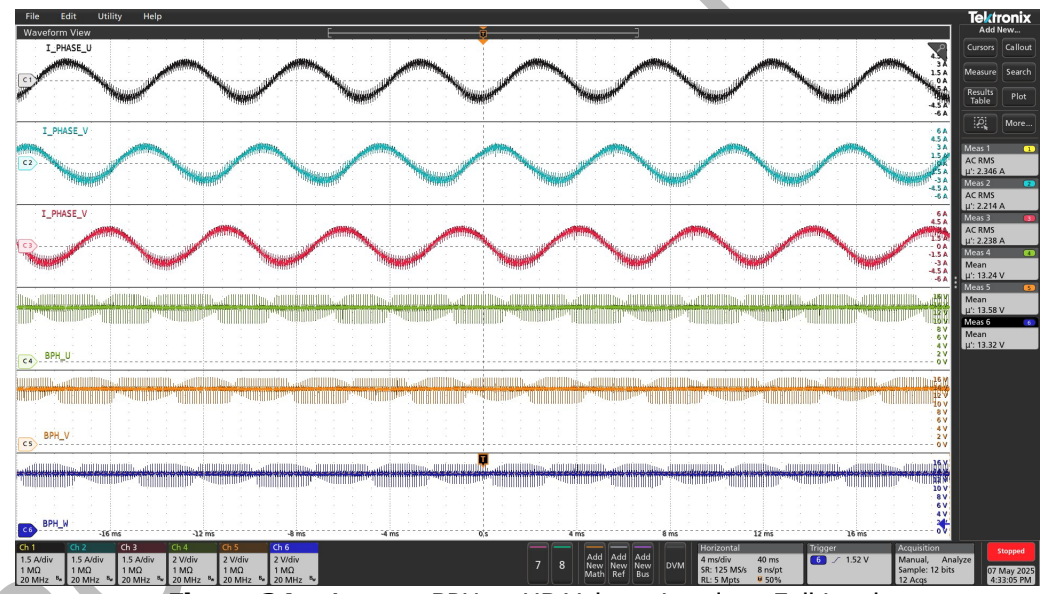

Figure 34 – Average BPH-to-HB Voltage Levels at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 2 V/div $V_{BPH\_U,\ AVERAGE}$ = 13.2 V
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 2 V/div $V_{BPH\_V,\ AVERAGE}$ = 13.6 V
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 2 V/div $V_{BPH\_W,\ AVERAGE}$ = 13.3 V
Time Scale: 4 ms/div

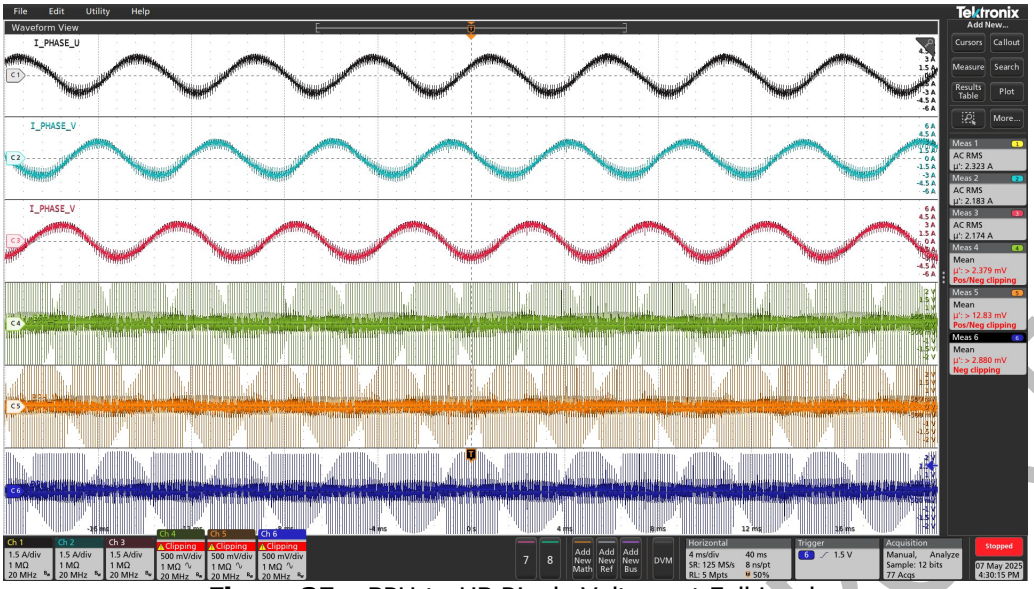

Figure 35 – BPH-to-HB Ripple Voltage at Full Load.
CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 0.5 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 0.5 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 0.5 V/div
Time Scale: 4 ms/div

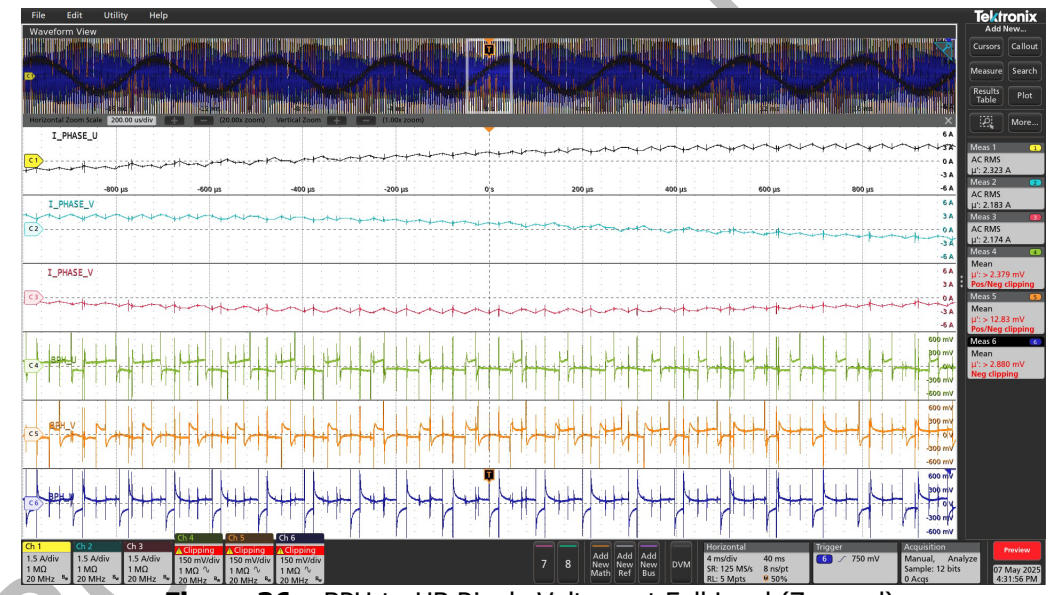

Figure 36 – BPH-to-HB Ripple Voltage at Full Load (Zoomed).
CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{BPH_U}, 150 mV/div $V_{BPH\_U, RIPPLE}$ < 900 mV_{pp}
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{BPH_V}, 150 mV/div $V_{BPH\_V, RIPPLE}$ < 900 mV_{pp}
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{BPH_W}, 150 mV/div $V_{BPH\_W, RIPPLE}$ < 900 mV_{pp}
Time Scale: 4 ms/div

Note: Measurements exclude high-frequency, switching-induced voltage spikes.

	V_{BPL}			V_{BPH}		
	Phase U	**Phase V**	**Phase W**	**Phase U**	**Phase V**	**Phase W**
DC Level (Light Load)	13.4 V	13.4 V	13.4 V	13.3 V	13.6 V	13.4 V
AC Ripple (Light Load)	215 mV_{pp}	251 mV_{pp}	239 mV_{pp}	< 900 mV_{pp}	< 900 mV_{pp}	< 900 mV_{pp}
DC Level (Full Load)	13.3 V	13.4 V	13.4 V	13.2 V	13.6 V	13.3 V
AC Ripple (Full Load)	358 mV_{pp}	451 mV_{pp}	422 mV_{pp}	< 900 mV_{pp}	< 900 mV_{pp}	< 900 mV_{pp}

Table 7 – BPL and BPH DC Voltage Levels.

7.3 Thermal Performance

The thermal performance of the BRD2469WB devices under various load conditions was measured after a 30-minute soak period to ensure steady-state operation of the inverter and motor setup. An acrylic enclosure around the board minimized the influence of external airflow, maintaining an ambient temperature of about 23.0 °C.

Motor speed was maintained at the rated 3000 RPM. At this speed and the full load phase current of 2.2 A_{RMS}, the inverter output power reaches 580 W. For 750 W (1 HP) inverter operation, the phase current was overdriven to nearly 3.0 A_{RMS}.

To isolate the inverter's thermal performance from other on-board circuits, external components were disabled as follows: J12 was shorted to bypass the input diode D1 and fuse F1, J7 and J8 were opened to disable the on-board 15 V regulator U4, and shunt resistors R19, R20, and R21 were shorted since the IPH feedback is used. An external 15 V supply was applied to J9 to power the on-board 3.3 V regulator U5.

By default, the BRD2469WB's IPH pin provides current feedback. The MotorXpert Suite reconstructs IPH signals as described in Section 8.4 of the Appendix.

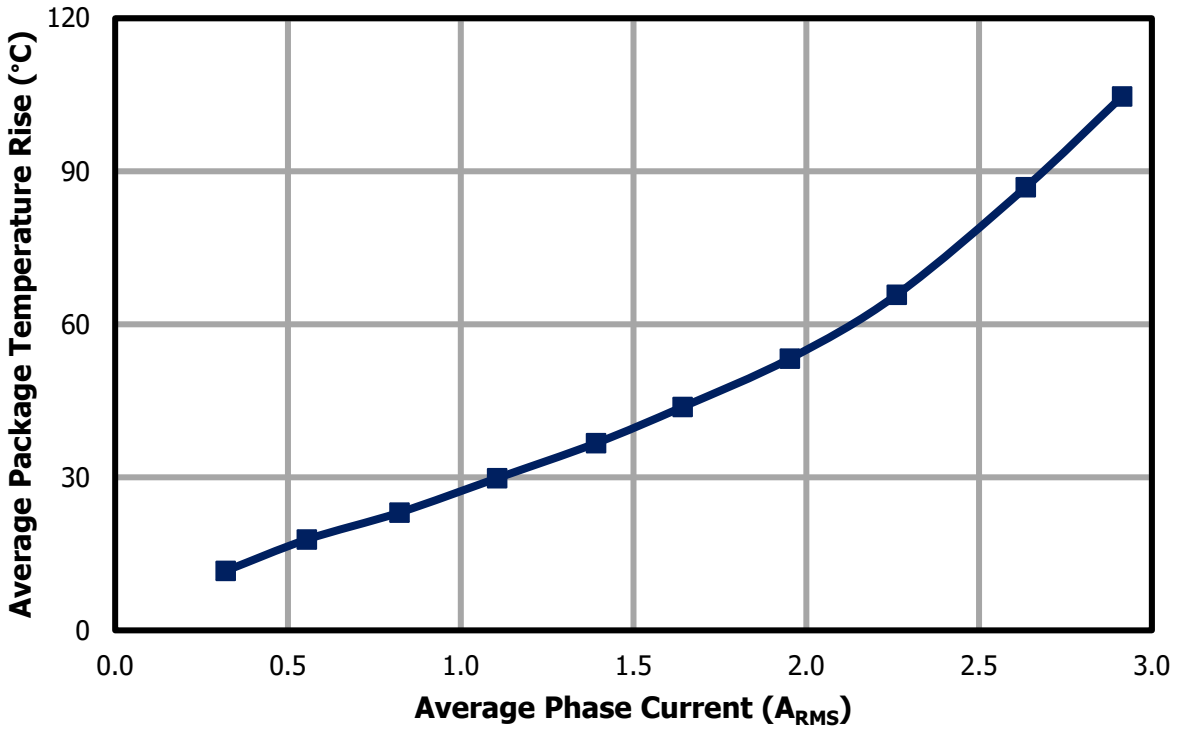

Figure 37 – Average Package Temperature Rise vs. Motor Phase Current.

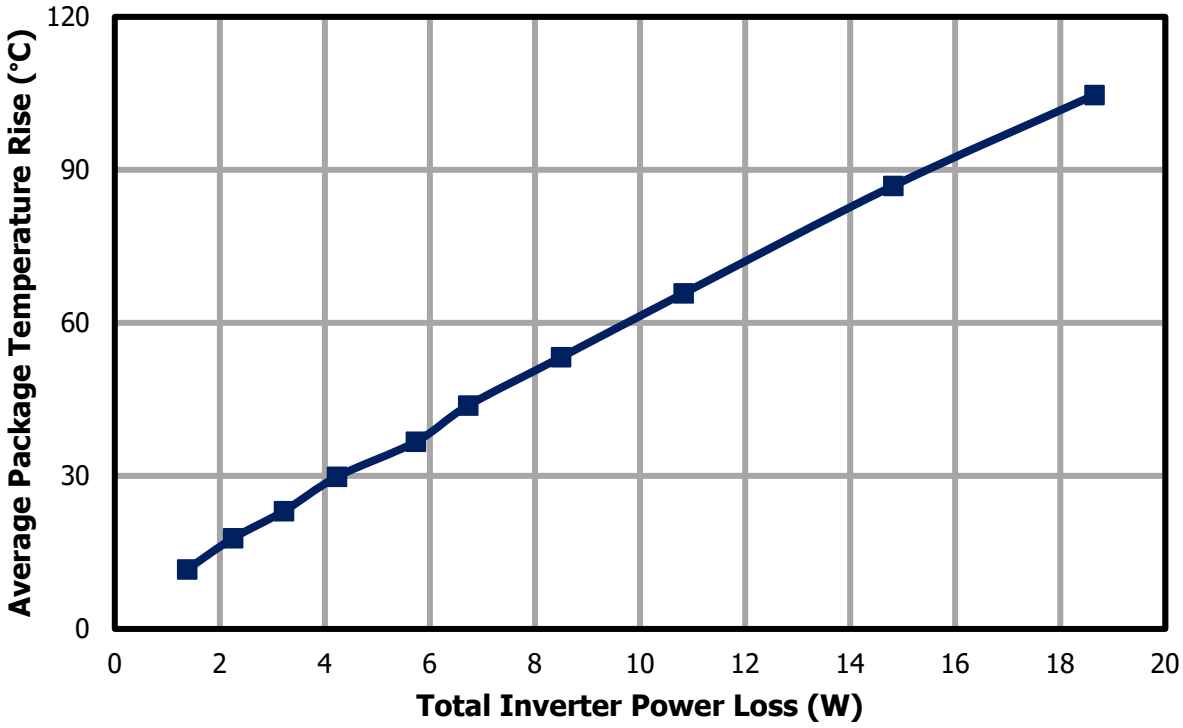

Figure 38 – Average Package Temperature Rise vs. Total Inverter Power Loss.

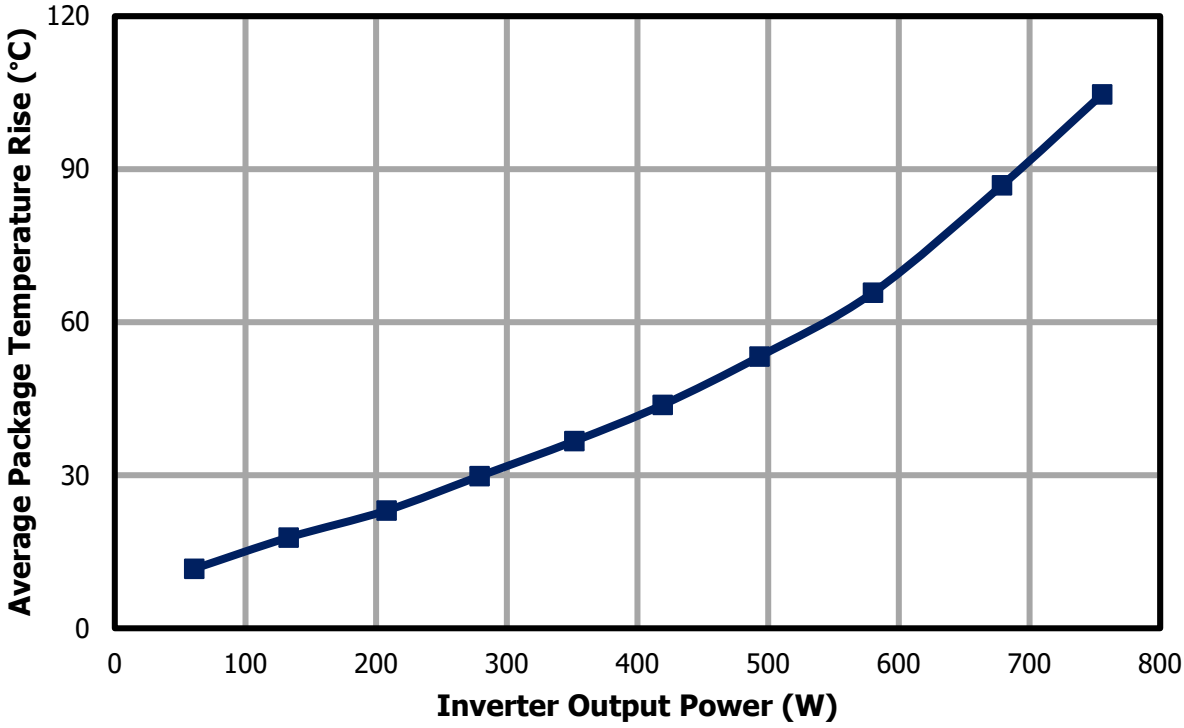

Figure 39 – Average Package Temperature Rise vs. Inverter Output Power.

7.3.1 Thermal Scans Across Loading Conditions

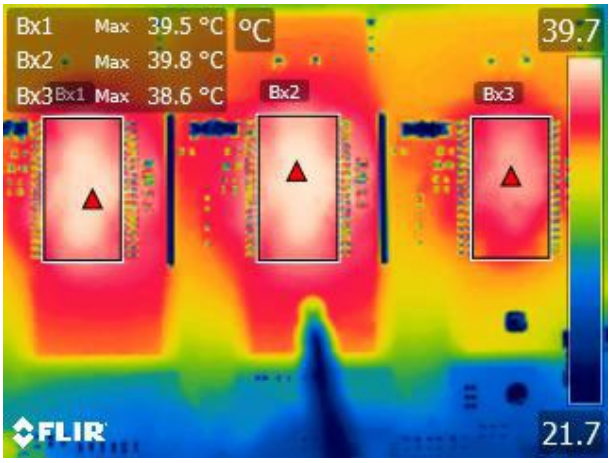

Figure 40 – Thermal Scan at 0.554 A_{RMS}
Ambient = 21.5 °C.

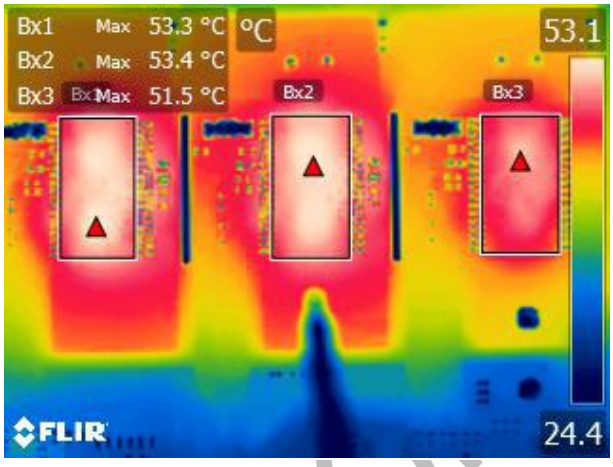

Figure 41 – Thermal Scan at 1.11 A_{RMS}
Ambient = 22.9 °C.

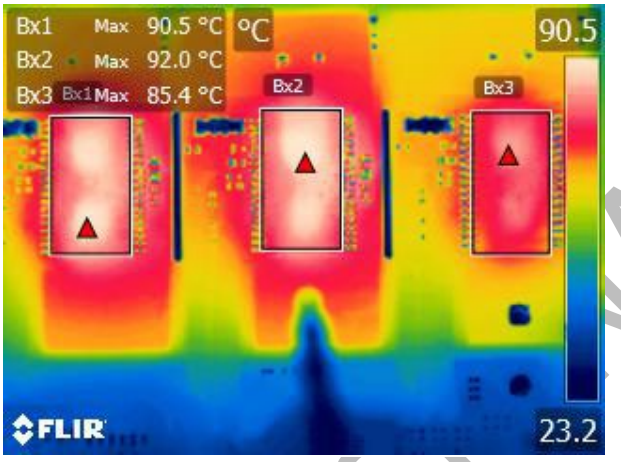

Figure 42 – Thermal Scan at 2.26 A_{RMS}
Ambient = 23.5 °C.

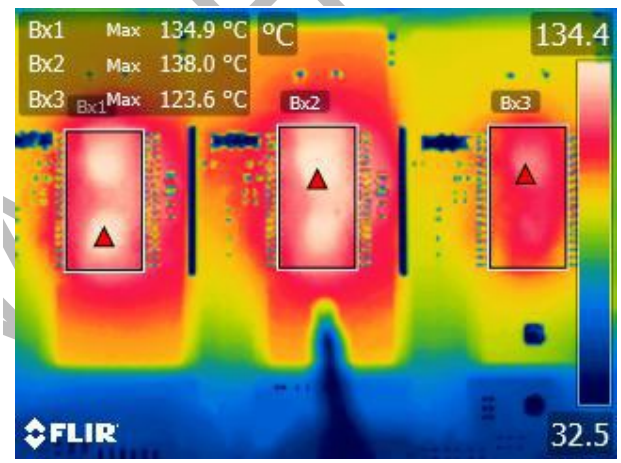

Figure 43 – Thermal Scan at 2.91 A_{RMS}
Ambient = 27.5 °C.

7.3.2 Thermal Performance Summary

Ave. Phase Current	$I_{PHASE-U}$	$I_{PHASE-V}$	$I_{PHASE-W}$	$T_{CASE, AVG}$	$T_{AMBIENT}$	$T_{RISE, AVG}$
0.320 A_{RMS}	0.321 A_{RMS}	0.321 A_{RMS}	0.317 A_{RMS}	**32.5 °C**	20.8 °C	**11.7 °C**
0.554 A_{RMS}	0.573 A_{RMS}	0.545 A_{RMS}	0.545 A_{RMS}	**39.3 °C**	21.5 °C	**17.8 °C**
0.823 A_{RMS}	0.857 A_{RMS}	0.801 A_{RMS}	0.810 A_{RMS}	**44.9 °C**	21.8 °C	**23.1 °C**
1.11 A_{RMS}	1.15 A_{RMS}	1.08 A_{RMS}	1.09 A_{RMS}	**52.7 °C**	22.9 °C	**29.8 °C**
1.39 A_{RMS}	1.45 A_{RMS}	1.36 A_{RMS}	1.36 A_{RMS}	**60.0 °C**	23.3 °C	**36.7 °C**
1.64 A_{RMS}	1.71 A_{RMS}	1.61 A_{RMS}	1.61 A_{RMS}	**67.5 °C**	23.7 °C	**43.8 °C**
1.95 A_{RMS}	2.03 A_{RMS}	1.91 A_{RMS}	1.92 A_{RMS}	**76.2 °C**	22.9 °C	**53.3 °C**
2.26 A_{RMS}	2.36 A_{RMS}	2.21 A_{RMS}	2.22 A_{RMS}	**89.3 °C**	23.5 °C	**65.8 °C**
2.64 A_{RMS}	2.74 A_{RMS}	2.60 A_{RMS}	2.57 A_{RMS}	**111 °C**	24.2 °C	**86.9 °C**
2.91 A_{RMS}	3.03 A_{RMS}	2.89 A_{RMS}	2.83 A_{RMS}	**132 °C**	27.5 °C	**105 °C**

Table 8 – Thermal Performance Summary.

7.4 Inverter Efficiency

The inverter efficiency of the BRD2469WB devices under various load conditions was recorded after a 30-minute soak period to ensure steady-state operation of the inverter and motor. An acrylic enclosure around the board minimized the effects of external airflow, maintaining an ambient temperature of about 23.0 °C.

Motor speed was maintained at the rated 3000 RPM. At this speed and the full load phase current of 2.2 A_{RMS}, the inverter output power reaches 580 W. For 750 W (1 HP) inverter operation, the phase current was overdriven to nearly 3.0 A_{RMS}.

Efficiency measurements were isolated to reflect inverter power losses only by disabling external circuits that add to the input power without contributing to the output power. This was accomplished by shorting J12 to bypass the input diode D1 and fuse F1, opening J7 and J8 to disable the on-board 15 V regulator U4, and shorting shunt resistors R19, R20, and R21. An external 15 V supply was applied to J9 to power up the built-in 3.3 V regulator U5.

The three-phase power meter setup used for the efficiency and power measurements is detailed in Section 8.3 of the Appendix.

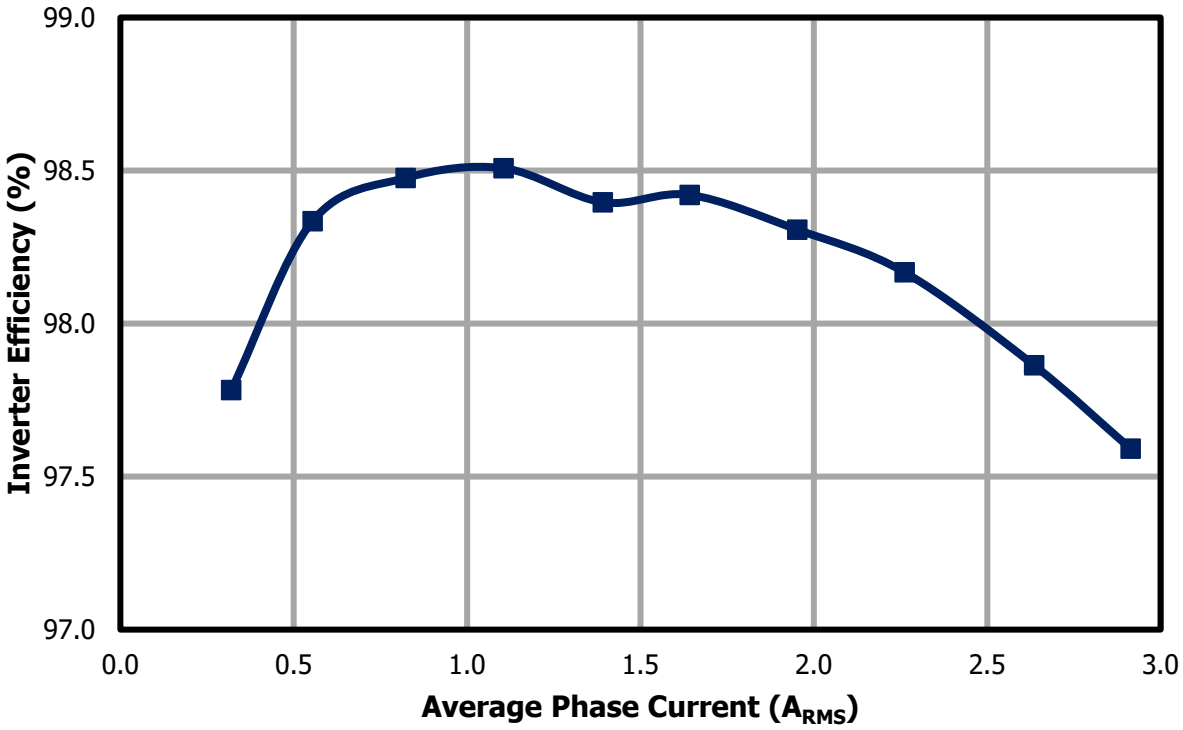

Figure 44 – Inverter Efficiency vs. Phase Current.

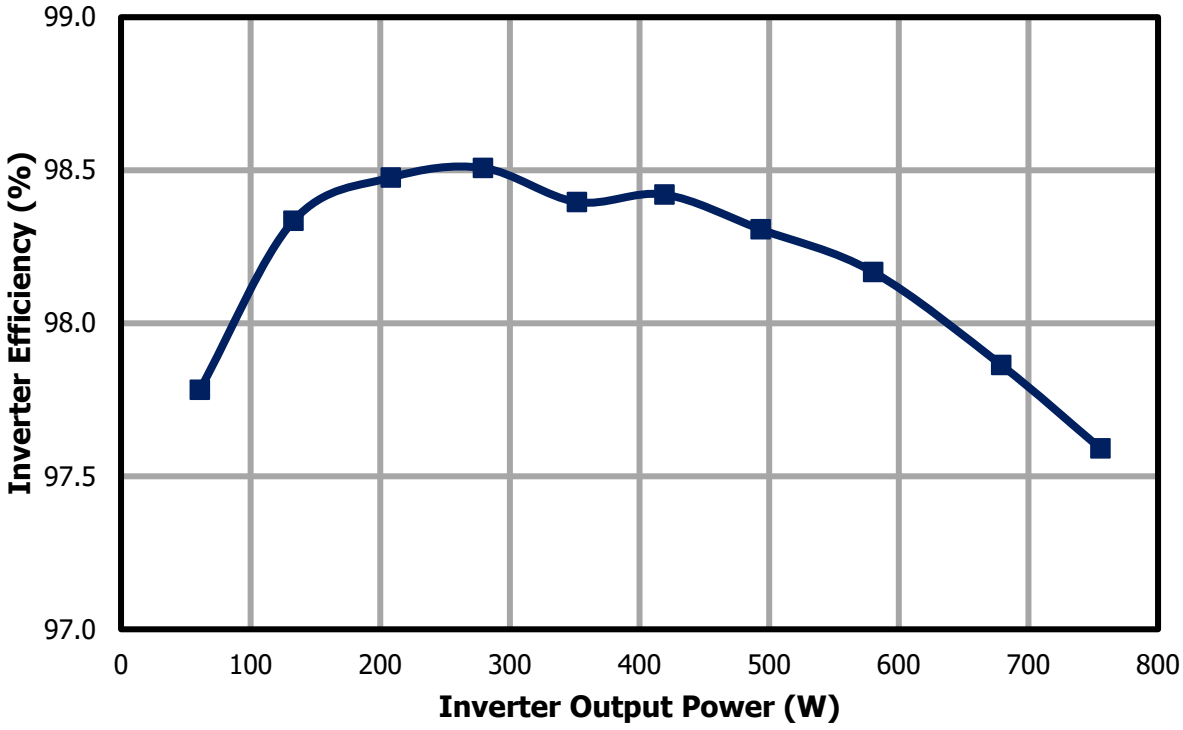

Figure 45 – Inverter Efficiency vs. Inverter Output Power.

7.4.1 Efficiency Table

DC Input Voltage (V_{IN})	Input DC Current (A)	Input Power (W)	Average Phase Current (A_{RMS})	$I_{PHASE-U}$ (A_{RMS})	$I_{PHASE-V}$ (A_{RMS})	$I_{PHASE-W}$ (A_{RMS})	Inverter Output Power (W)	Power Loss (W)	Inverter Efficiency (%)
340	0.183	62.1	0.320	0.321	0.321	0.317	60.7	1.38	97.8
340	0.398	135	0.554	0.573	0.545	0.545	133	2.25	98.3
340	0.621	211	0.823	0.857	0.801	0.810	208	3.22	98.5
340	0.834	283	1.11	1.15	1.08	1.09	279	4.23	98.5
340	1.05	357	1.39	1.45	1.36	1.36	352	5.73	98.4
340	1.25	426	1.64	1.71	1.61	1.61	419	6.73	98.4
340	1.48	502	1.95	2.03	1.91	1.92	493	8.50	98.3
340	1.74	591	2.26	2.36	2.21	2.22	580	10.8	98.2
340	2.04	694	2.64	2.74	2.60	2.57	679	14.8	97.9
340	2.28	774	2.91	3.03	2.89	2.83	756	18.7	97.6

Table 9 – Efficiency Table.

7.5 Device and System Level Protection

The BridgeSwitch-2 introduces an Error Flag pin to simplify fault handling in motor applications. Under normal operation, the EF pin remains HIGH. It is automatically pulled LOW in response to destructive faults, including overtemperature, overvoltage, and sustained overcurrent events. Pulling the EF pin LOW inhibits FREDFET switching on all devices. Switching remains disabled until the MCU issues a latch reset signal or the system undergoes a power reset.

FAULT Protection	Remarks
Latching Overcurrent Protection (OCP)	• Applies only to the low-side FREDFET. • EF pin goes LOW after 16 consecutive low-side OC events. • SLP pull-down resistor should be set to 133 kΩ.
Overvoltage Protection (OVP)	• EF pin goes LOW when bus voltage exceeds the OV threshold. • EF pin returns HIGH once bus voltage drops below $OV_{THRESHOLD}$ - $OV_{HYSTERESIS}$.
Overtemperature Protection (OTP)	• EF pin goes LOW when junction temperature reaches the thermal shutdown threshold (T_{SD}). • **Hysteretic OTP** (R_{SLP} = 9.53 kΩ): – EF pin returns HIGH once junction temperature drops below the restart threshold (T_{RES}). • **Latching OTP** (R_{SLP} = 133 kΩ or OPEN): – EF pin latches OFF until either an EF latch reset from the MCU or a power recycle occurs, re-enabling FREDFET switching.

Table 10 – Error Flag Fault Response.

8 Appendix

8.1 Board Quick Reference

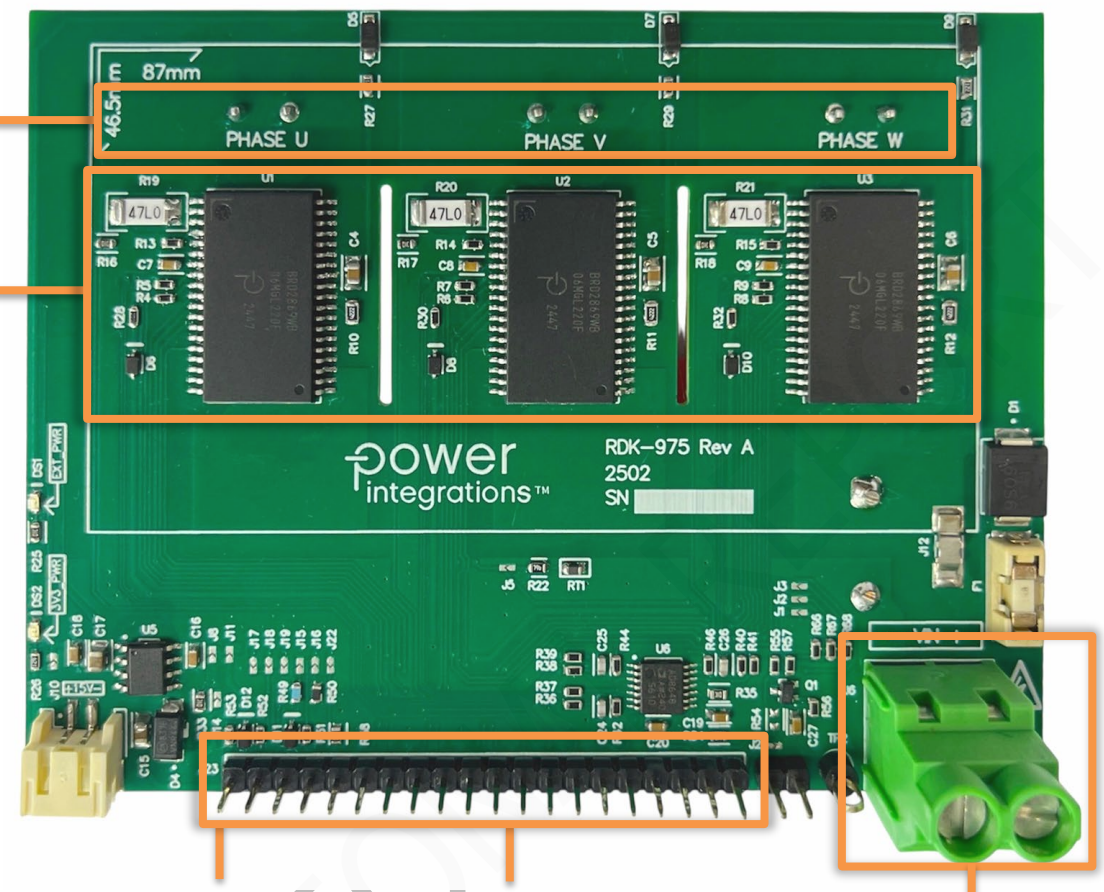

Figure 46 – RDK-975 Board Quick Reference.

8.1.1 Microcontroller (MCU) Interface Pins Designation

Pin Order	Pin Name	Pin Type	Pin Description
1	EF_RST	Input	Error Flag reset signal. Momentarily pulling this pin high re-enables device switching after a latching fault.
2	EF_BUS	Open-drain, I/O	Error Flag state monitoring. Pulling this low inhibits FREDFET switching for BridgeSwitch-2 devices with EF functionality.
3	SLEEP	Input	Pulling this pin high enables SLEEP mode on BridgeSwitch-2 devices with the self-supply feature (not used in this design).
4	FAULT_BUS	Open-drain, I/O	FAULT bus monitoring for BridgeSwitch-2 devices. The MCU can pull this low for 160 µs to request status updates, or for 320 µs to re-enable switching after a latching fault.
5	GND	MCU Ground	Microcontroller ground reference.
6	INL_U	Input	Phase U (U1) low-side FREDFET PWM control signal.
7	INH_U	Input	Phase U (U1) high-side FREDFET PWM control signal.
8	INL_V	Input	Phase V (U2) low-side FREDFET PWM control signal.
9	INH_V	Input	Phase V (U2) high-side FREDFET PWM control signal.
10	INL_W	Input	Phase W (U3) low-side FREDFET PWM control signal.
11	INH_W	Input	Phase W (U3) high-side FREDFET PWM control signal.
12	IPH_U	Output	Phase U (U1) IPH output.
13	IPH_V	Output	Phase V (U2) IPH output.
14	IPH_W	Output	Phase W (U3) IPH output.
15	SENSE_CURRENT_U	Output	Phase U (U1) R_{SHUNT} voltage amplifier output.
16	SENSE_CURRENT_V	Output	Phase V (U2) R_{SHUNT} voltage amplifier output.
17	SENSE_CURRENT_W	Output	Phase W (U3) R_{SHUNT} voltage amplifier output.
18	SM_W	Input	Optional SM pin input for Phase W (U3).
19	3V3	Power Input	3.3 V microcontroller supply input.
20	VBUS_SENSE	Output	Voltage divider output for high-voltage DC bus sensing (scale-down factor: 0.0055).

Table 11 – J23 Connector Pin Designation.

Note: Pin labels are located on the bottom-layer silkscreen of the board.

8.2 Recommended Start-up Sequence

In BridgeSwitch-2 devices, the low-side and high-side gate drivers are supplied via the BPL and BPH pins. Proper inverter operation at start-up requires adequate voltage levels across these pins. The system microcontroller (MCU) should follow the recommended power-up sequence illustrated below:

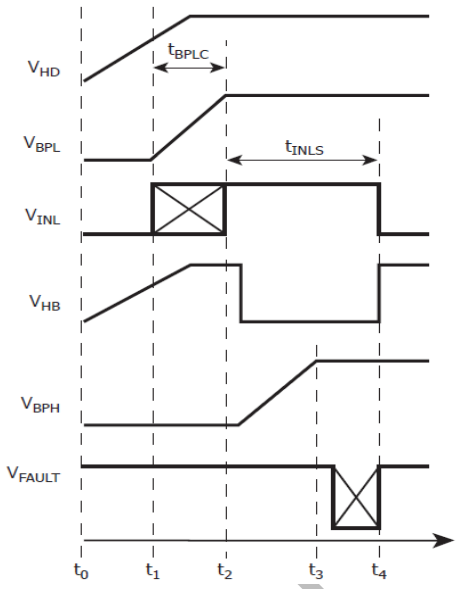

Figure 47 – Recommended Power-up Sequence.

The table below summarizes each stage of the recommended power-up sequence:

Time Point	Activity
t_0	• A high-voltage DC bus is applied.
t_1	• The internal current source begins charging the BPL pin capacitor once the HD pin voltage reaches $V_{HD(START)}$. • The system MCU may start setting the low-side FREDFET control signal (INL) high.
t_2	• The BPL pin voltage reaches the recommended level (V_{BPL}, typ. 12.8 V). • External device settings are configured. • The internal Gate drive logic turns the low-side FREDFET on after device setup completes and INL is high. • The internal current source begins charging the BPH pin capacitor.
t_3	• The BPH pin voltage reaches the recommended level relative to the HB pin (typ. 12.8 V). • The device communicates a successful power-up via the FAULT pin (for FAULT variants only). Note: No status update is sent if the internal power-up sequence does not complete successfully.
t_4	• The BridgeSwitch-2 device is ready for operation. • The system MCU may turn off the low-side FREDFET.

Table 12 – Power-up Sequence Stages.

8.3 Inverter Output Power Measurement

A six-channel power analyzer (WT1806E) was used to measure inverter power and efficiency. Figure 48 shows the output power meter connections in a three-wattmeter configuration, enabling phase current measurements for all motor phases. The third motor phase was used as the voltmeter reference for the other two phases, eliminating the need for a false neutral node and providing a total output power calculation equivalent to the two-wattmeter method.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

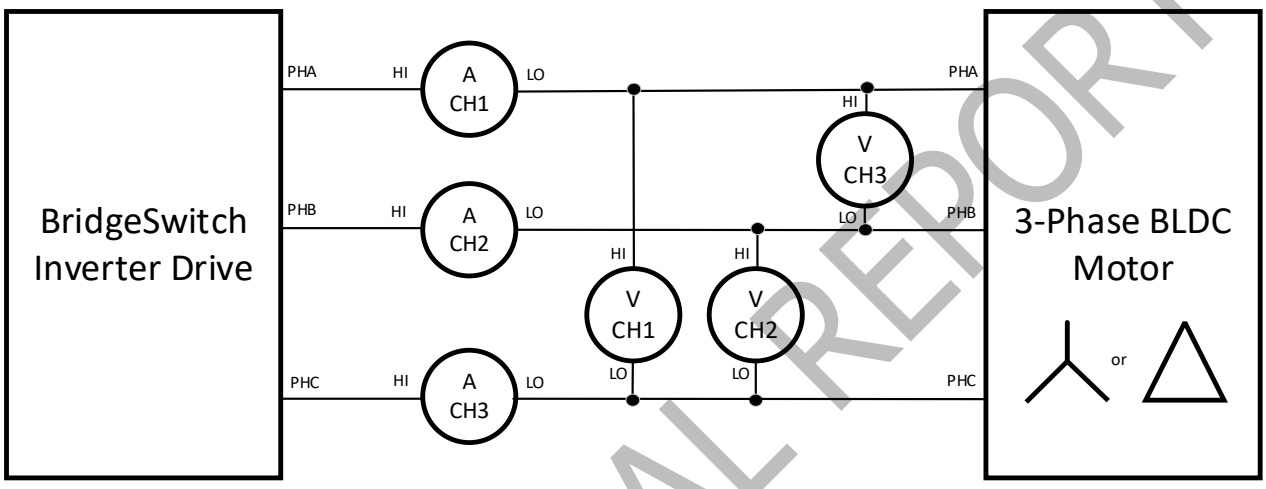

Figure 48 – Inverter Output Power Measurement (Three-wattmeter Setup).

Alternatively, the two-wattmeter setup shown in Figure 49 simplifies connections and reduces the number of required power meter channels, while providing readings comparable to the three-wattmeter method.

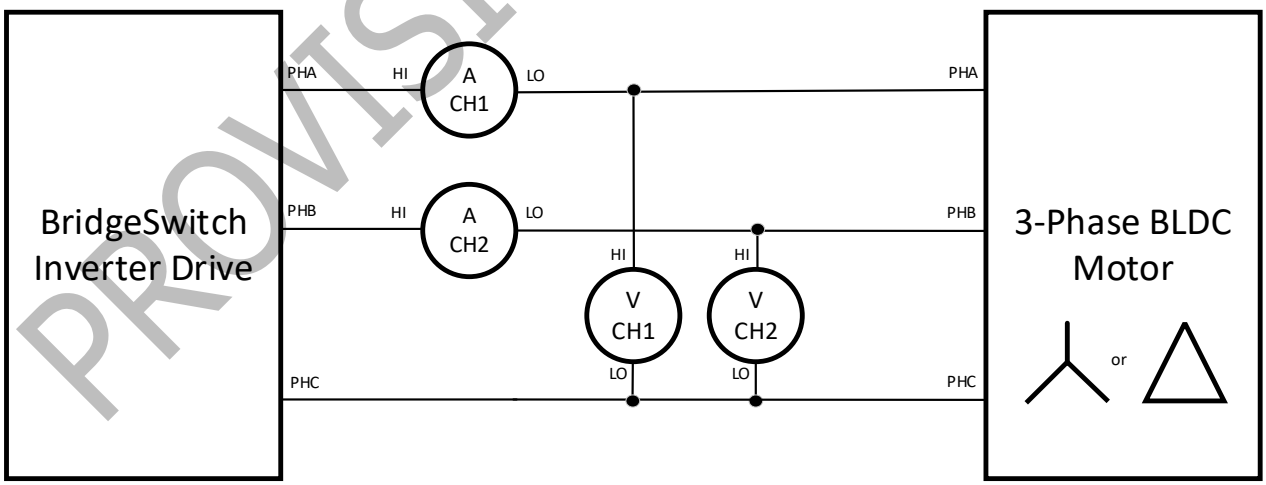

Figure 49 – Inverter Output Power Measurement (Two-wattmeter Setup).

8.4 IPH Reconstruction by the MotorXpert Suite 3.0

The instantaneous phase current (IPH) output, shown in Figure 50, provides a low-voltage signal proportional to the positive half-cycle of the current through the low-side power FREDFET. For field-oriented control applications, a reconstruction algorithm is required to derive the negative half-cycle of the phase current for use as current feedback.

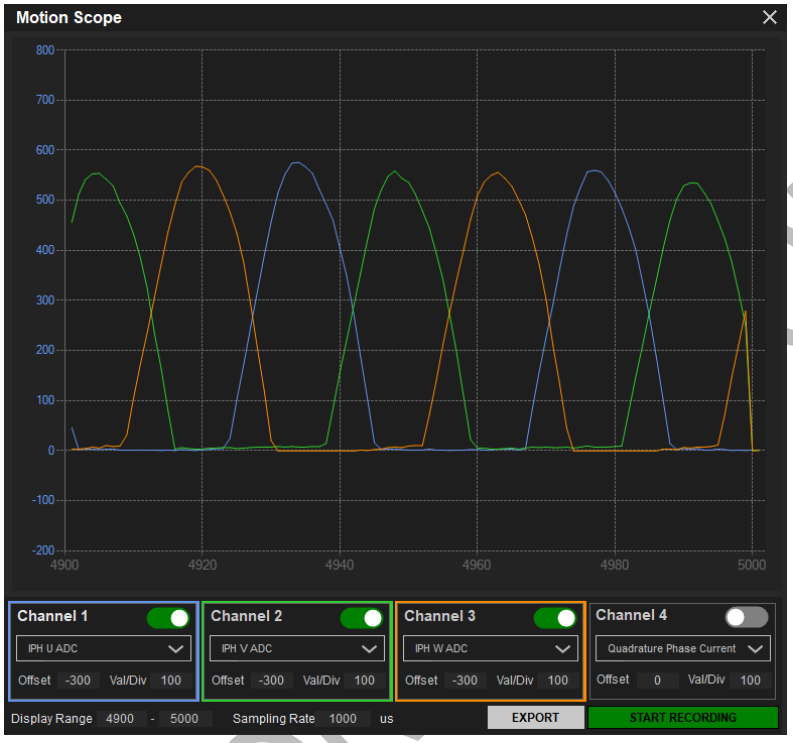

Figure 50 – IPH Signals before Current Reconstruction.

Figure 51 – Phase Current Output after Current Reconstruction.

Figure 51 illustrates the phase current output reconstructed from the trigonometric relationships of the phase current signals. Since the IPH signals provide only the positive half-cycle, the reconstruction restores the negative half-cycle, effectively doubling the data resolution and improving current control. This reconstruction can be readily performed using MotorXpert Suite 3.0.

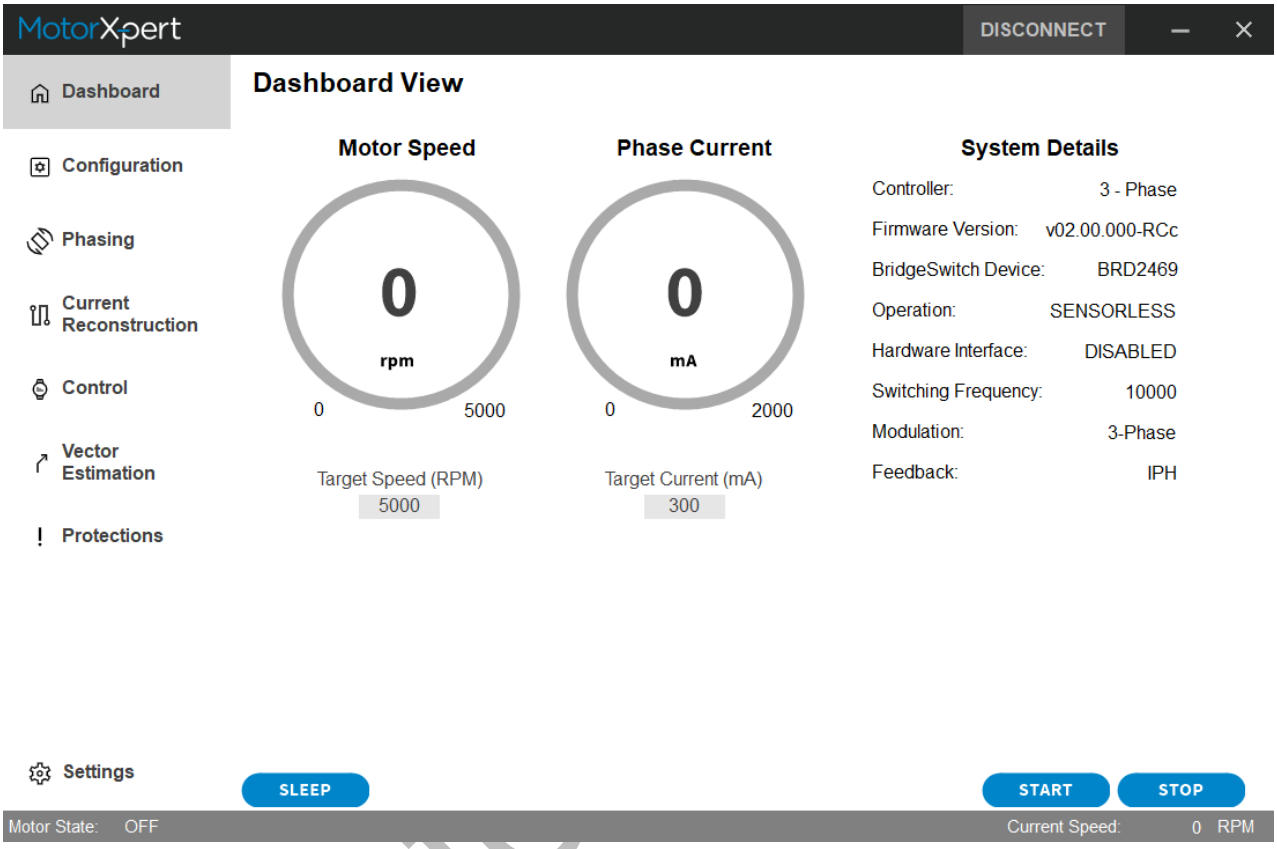

Figure 52 – MotorXpert Suite Dashboard.

For more information on the MotorXpert Suite, visit: https://www.power.com/design-support/motorxpert-suite-bridgeswitch

8.5 FAULT and Error Flag Configurations

This reference design supports both FAULT and Error Flag variants of the BridgeSwitch-2 devices. Both signals are normally HIGH and require an external pull-up to the microcontroller supply voltage (3.3 V or 5 V). The recommended bus configuration enables collective fault reporting, allowing multiple BridgeSwitch-2 devices to communicate fault conditions using a single microcontroller pin.

8.5.1 FAULT Signal

The FAULT bus communicates all state changes and destructive faults via a 7-bit word, enabling the simultaneous reporting of multiple fault conditions to the MCU. Figure 53 shows the available status codes for the FAULT signal.

Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I_{OV}	0	0	1	X	X	X	X
High-voltage bus UV 100%	I_{UV100}	0	1	0	X	X	X	X
High-voltage bus UV 85%	I_{UV85}	0	1	1	X	X	X	X
High-voltage bus UV 70%	I_{UV70}	1	0	0	X	X	X	X
High-voltage bus UV 55%	I_{UV55}	1	0	1	X	X	X	X
System thermal fault	$V_{TH(TM)}$	1	1	0	X	X	X	X
LS Driver not ready[1]	n/a	1	1	1	X	X	X	X
LS FET thermal warning	T_{WA}	X	X	X	0	1	X	X
LS Device shutdown[3]	$T_{SD,}$ $t_{D(OCL)}$	X	X	X	1	0	X	X
HS Driver not ready[2]	I_{COM}	X	X	X	1	1	X	X
LS FET over-current	$V_{X(TH)}$	X	X	X	X	X	1	X
HS FET over-current	$V_{X(TH)}$	X	X	X	X	X	X	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

Figure 53 – FAULT Signal Status Word Encoding.

8.5.2 Error Flag Signal

Compared to the FAULT signal, the Error Flag signal simplifies fault reporting. It remains HIGH during normal operation and is automatically pulled LOW during destructive faults. While LOW, the EF signal inhibits FREDFET switching for all BridgeSwitch-2 devices connected to the EF bus. Additionally, the microcontroller can intentionally pull the EF bus LOW to disable inverter operation.

Table 13 summarizes the status changes flagged by each EF pin.

FAULT Conditions	Error Flag (Default)	FAULT
HV Bus OV	✓	✓
HV Bus UV (100%, 85%, 70%, 55%)		✓
System Thermal Fault		✓
LS Driver Not Ready		✓
LS FET Thermal Warning		✓
LS Device Shutdown (OTP, Latching OCP)	✓	✓
HS Driver Not Ready		✓
LS FET Cycle-by-cycle Overcurrent		✓
HS FET Cycle-by-cycle Overcurrent		✓
LS FET Latching Overcurrent	✓	✓
Device Ready (No Faults)		✓

Table 13 – Error Flag and FAULT Bus Triggers.

8.5.3 Fault Handling Feature Selection

To isolate each functionality, PCB jumpers are incorporated into the design. Table 14 summarizes the jumper settings for enabling the respective fault reporting features.

Configuration	Error Flag	FAULT
Shorted Jumpers	J17, J18, J19	J22

Table 14 – Error Flag and FAULT Feature Jumper Configuration.

8.6 Test Bench Set-up

Figure 54 illustrates the RDK-975 board connections to the high-voltage DC supply and microcontroller unit. An interface board was designed to enable direct signal connections between the MCU and the inverter board.

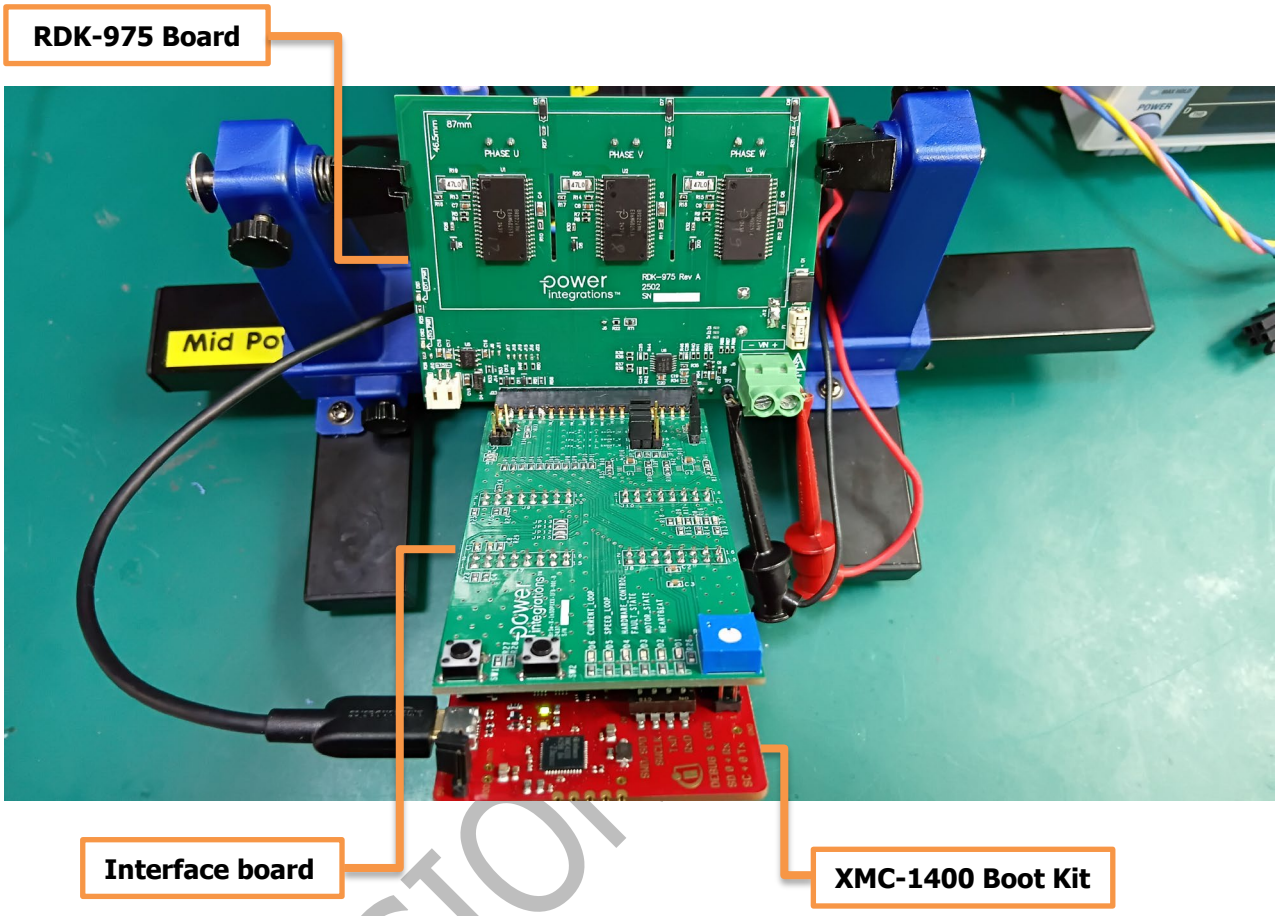

Figure 54 – RDK-975 Board with Microcontroller.

The setup shown in Figure 55 ensures accurate temperature and efficiency measurements for the board under test. An acrylic case was used to minimize the influence of ambient airflow on the performance data.

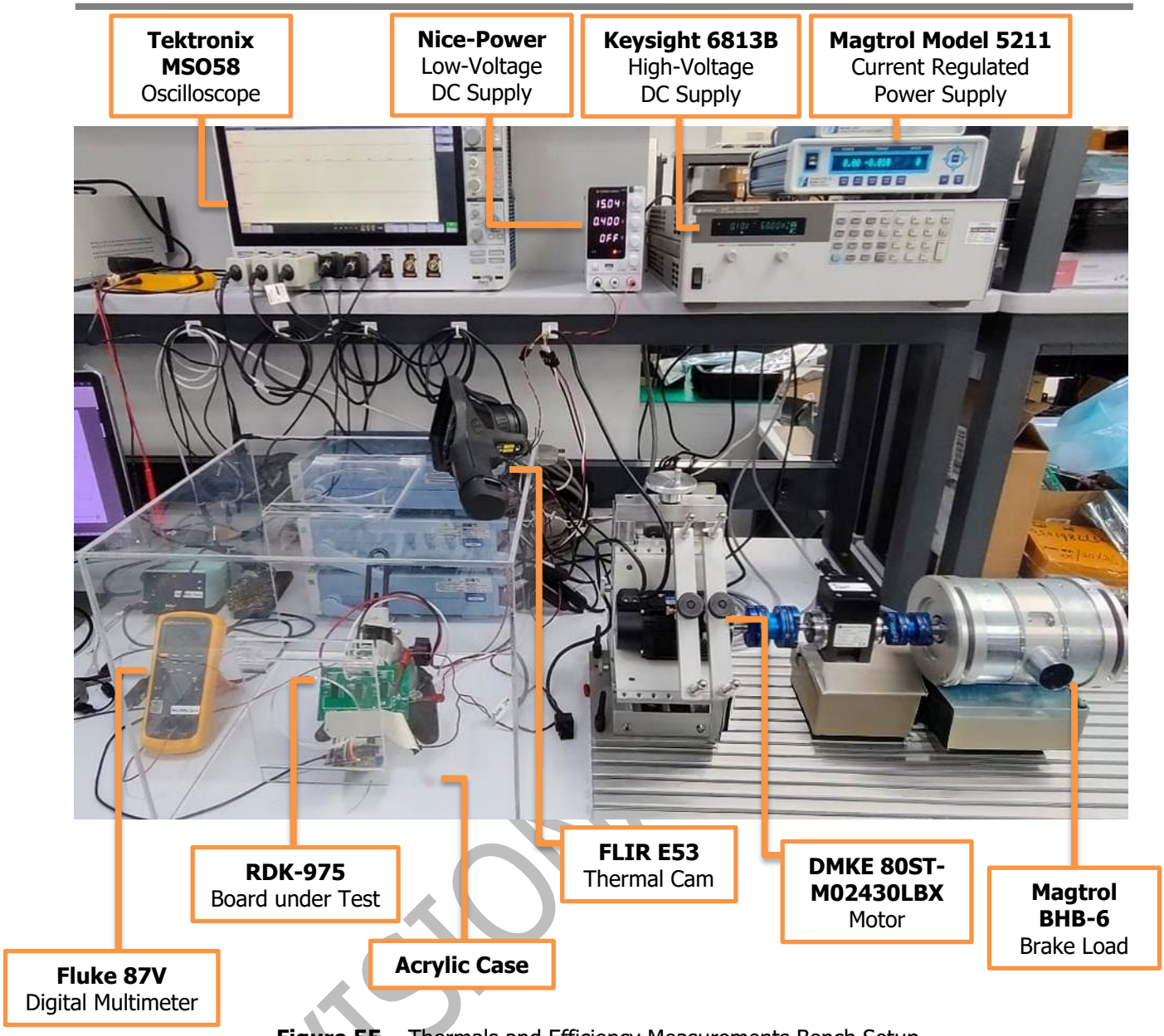

Figure 55 – Thermals and Efficiency Measurements Bench Setup.

8.6.1 Equipment Used

1. **Tektronix MSO58** (Oscilloscope) – 350 MHz, 6.25 GS/s resolution
2. **Nice-Power** (Low-Voltage DC Supply) – 30 VDC, 10 A maximum output
3. **Keysight 6813B** (High-Voltage DC Supply) – 300 V_{RMS}, 1750 VA rated
4. **Magtrol Model 5211** (Current Regulated Power Supply) – 24 VDC, 0 to 1000 mA output
5. **Fluke 87V** (Digital Multimeter) – -200 °C to 1090 °C temperature range
6. **FLIR E53** (Thermal Camera) – 40 mK thermal sensitivity, -20 °C to 650 °C temperature range
7. **DMKE 80ST-M02430LBX** (Motor) – 750 W, 220 V, 3 A, 3000 RPM rated
8. **BHB-6** (Brake Load) – 24 VDC, 1.5 A, 20,000 RPM rated
9. **WT1806E** (Precision Power Analyzer) – 6-channel, 2 MS/s (16 bits), 0.1 Hz to 1 MHz measurement bandwidth

9 Revision History

Date	Author	Rev.	Description & Changes	Approval
3-Sep-25	MAT, SM	A	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

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