Title	**750 W (~1 HP) Three-Phase High Voltage Motor Drive Inverter Using BridgeSwitch-2 (BRD2869WB) and LinkSwitch-TN2 LNK3205D in FOC Operation**
Specification	340 VDC Input, 750 W Continuous Three-Phase Inverter Output Power, 3.0 A_{RMS} Continuous Motor Phase Current
Application	High-Voltage Brushless DC (BLDC) Motor Drive
Author	Applications Engineering Department
Document No.	RDR-975
Date	June 3, 2026
Revision	B

Summary and Features

- BridgeSwitch™-2 high-voltage half-bridge motor driver
- Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- No heat sink
- High-side and low-side cycle-by-cycle current limit (OCP)
- Optional latching low-side current limit
- Configurable latching or hysteretic over-temperature protection (OTP)
- High-voltage bus monitor for overvoltage protection (OVP)
- Error flagging through the Error Flag (EF) pin
- Supports any microcontroller (MCU) for sensorless field-oriented control (FOC)
- Instantaneous phase current output through the IPH pin of each BridgeSwitch-2 device

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/

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Important Notice:
During operation, the reference design board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

1 Introduction

This document presents a 750 W, three-phase inverter designed for high-voltage brushless DC (BLDC) motor applications, utilizing three BridgeSwitch-2 BRD2869WB devices, achieving 97.6% efficiency with a peak of 98.5%. It details both the device and system-level performance, as well as the fault protection capabilities provided by the highly integrated BridgeSwitch-2 half-bridge motor driver IC. A high-voltage buck converter, implemented with minimal component count using the LinkSwitch™-TN2 LNK3205D device, supplies the required external bias for the BRD2869WB components. An optional current sense amplifier is also included to support applications requiring shunt resistor-based current feedback.

This document also provides the inverter specifications, schematic, bill of materials (BOM), printed circuit board (PCB) layout, performance metrics, and an overview of the test setup and procedure. The waveforms and performance data are obtained using a sensorless Field-Oriented Control (FOC) method based on the Space Vector Modulation (SVM) technique, commonly referred to as three-phase modulation. This control is implemented via the MotorXpert™ Suite, using the BRD2869WB's instantaneous phase current (IPH) data for current feedback.

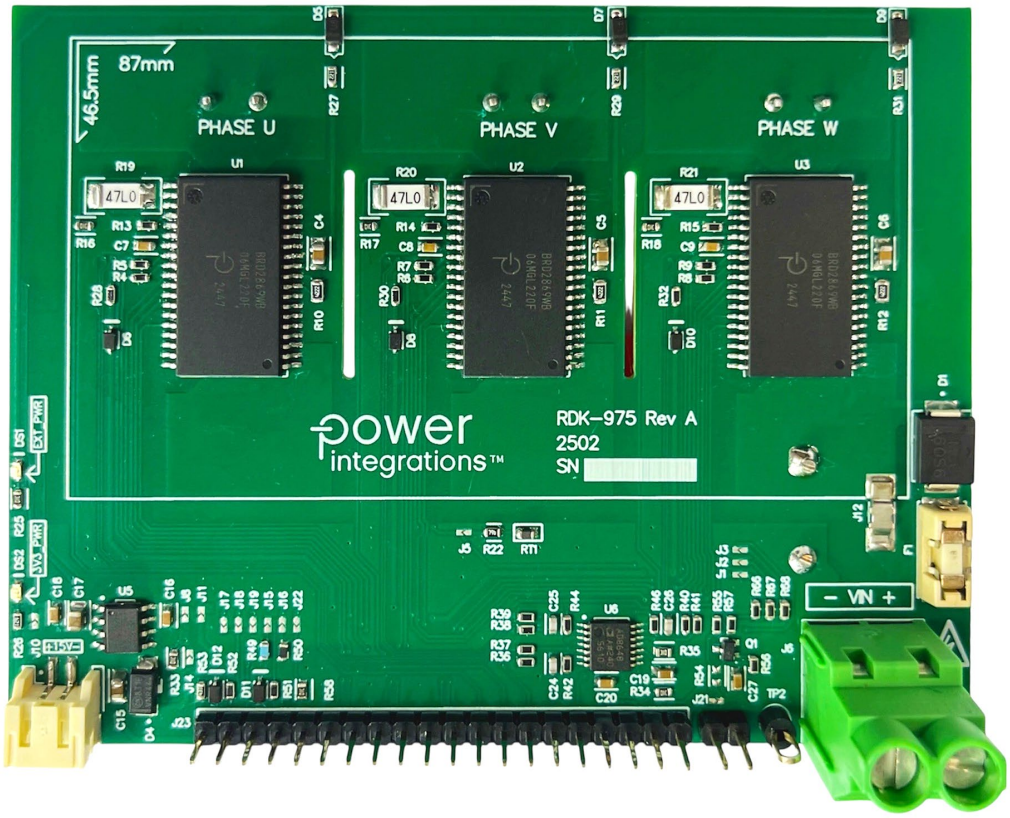

Figure 1 – Populated Circuit Board Top View.

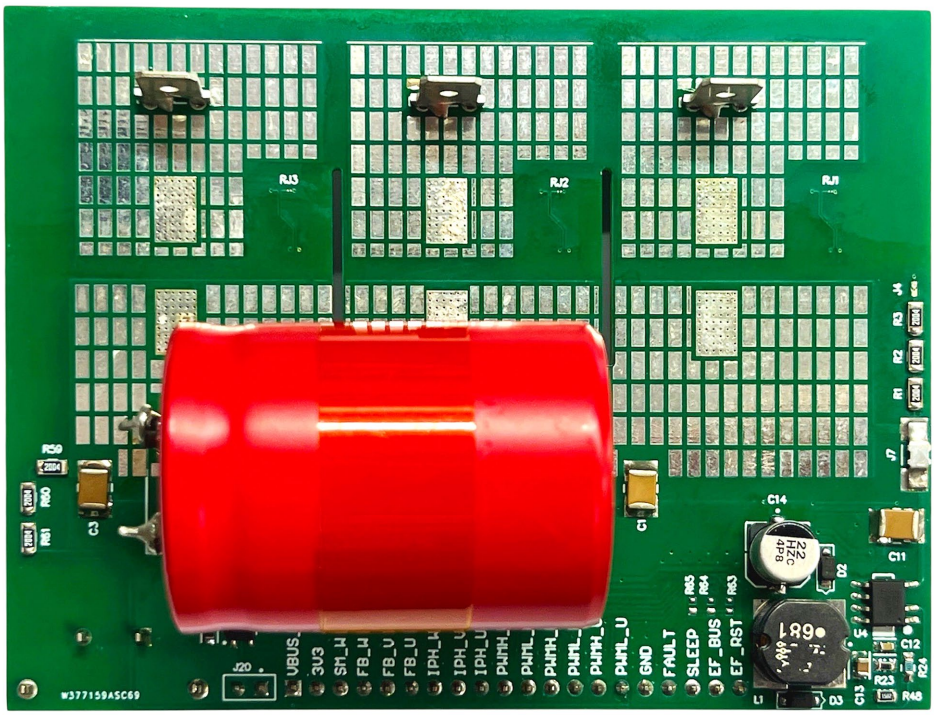

Figure 2 – Populated Circuit Board Bottom View.

2 Inverter Specification

The following table presents the electrical specifications and performance results of the three-phase inverter design.

Description	Symbol	Min	Typ	Max	Unit	Comment
Input						
Input Voltage	V_{IN}	270	340	365	V	Two-wire DC Input
Rated Input Current(1)	$I_{IN, RATED}$		1.74		A	Rated Input DC Current
Max. Input Current(2)	$I_{IN, MAX}$		2.29		A	Max. Input DC Current
Rated Input Power(1)	$P_{IN, RATED}$		591		W	Rated Inverter Input Power
Max. Input Power(2)	$P_{IN, MAX}$		777		W	Max. Inverter Input Power
Output						
Rated Output Power(1)	$P_{OUT, RATED}$		580		W	Rated Inverter Output Power
Max. Output Power(2)	$P_{OUT, MAX}$		758		W	Max. Inverter Output Power
Rated Inverter Efficiency(1)	η_{RATED}		98.0		%	At the rated loading condition
Max. Inverter Efficiency(2)	η_{MAX}		97.5		%	At the maximum loading condition
Rated Inverter Output Current (RMS)(1)	$I_{MOT(RMS), RATED}$		2.26		A	Rated RMS Current Per Phase
Max. Inverter Output Current (RMS)(2)	$I_{MOT(RMS), MAX}$		2.90		A	Max. RMS Current Per Phase
PWM Carrier Frequency(3)	f_{PWM}		10.0		kHz	Three-Phase FOC Modulation
Motor Speed	ω		3000		RPM	
Environmental						
Rated Ambient Temperature(1)	$T_{AMB, RATED}$		25.2		°C	Closed case. No airflow. Free Convection.
Max. Ambient Temperature(2)	$T_{AMB, MAX}$		27.1		°C	
Rated Device Case Temperature(1)	$T_{PACKAGE, RATED}$		93.9		°C	
Max. Device Case Temperature(2)	$T_{PACKAGE, MAX}$		135		°C	
System Level Monitoring						
DC Bus Sensing						Reported through the Error Flag (EF) Pin
OV Threshold	V_{OV}		362		V	
Over Current (OCP) Threshold(4)	I_{OCP}		7.00		A_{PK}	XL/XH = 42.2 kΩ

Notes:
1. At 2.23 A_{RMS} operating at 3000 RPM, resulting in an inverter output power of 580 W.
2. At 2.87 A_{RMS} to achieve the 750 W inverter output power at 3000 RPM.
3. 20 kHz is the maximum recommended PWM frequency.
4. This can be manually configured by adjusting the XL/XH resistor value. For BRD2869WB, the maximum current protection level is 7.00 A using an XL/XH resistance of 42.2 kΩ.

Table 1 – Inverter Specification.

3 Schematic

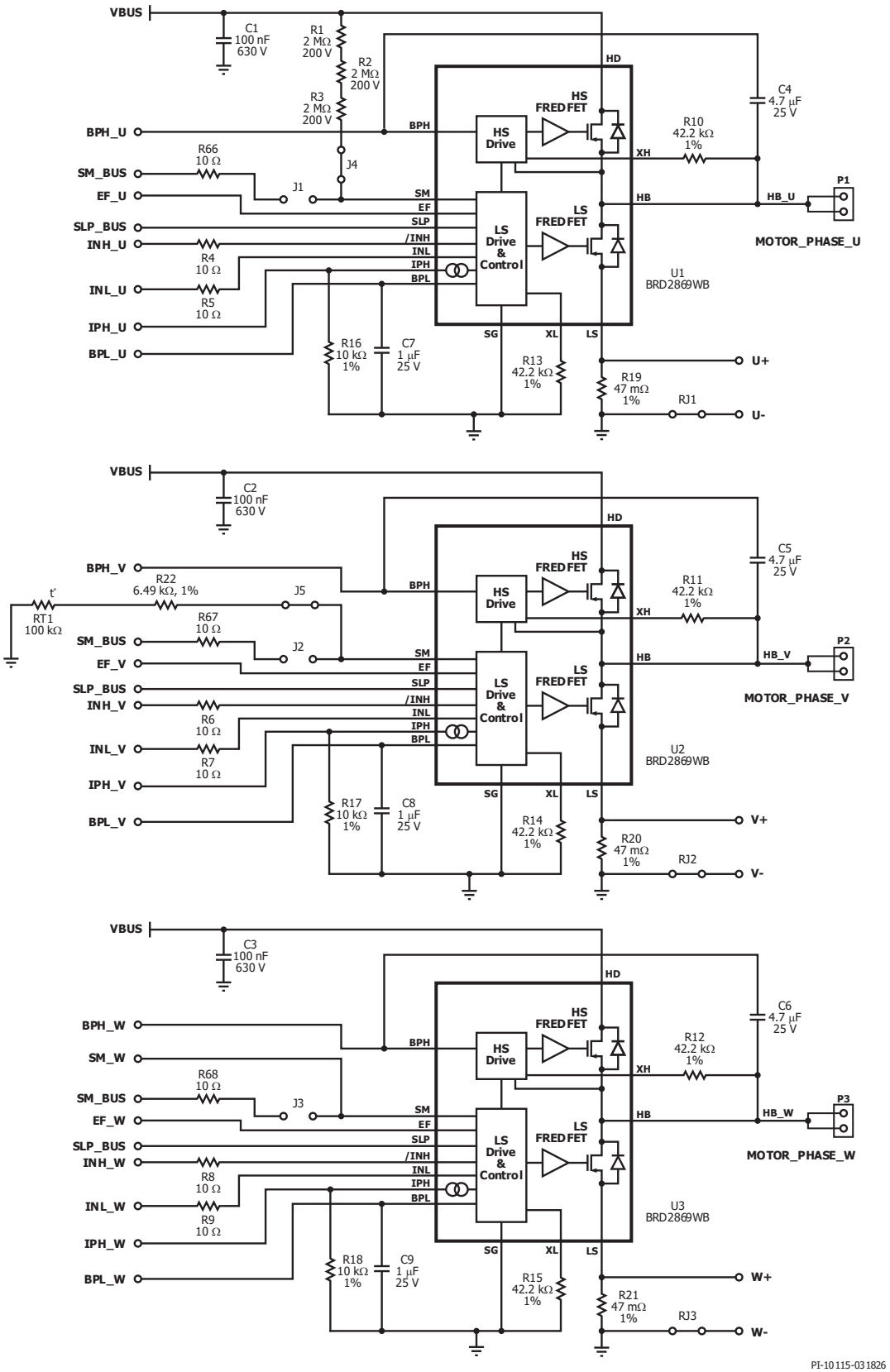

Figure 3 – Inverter Section.

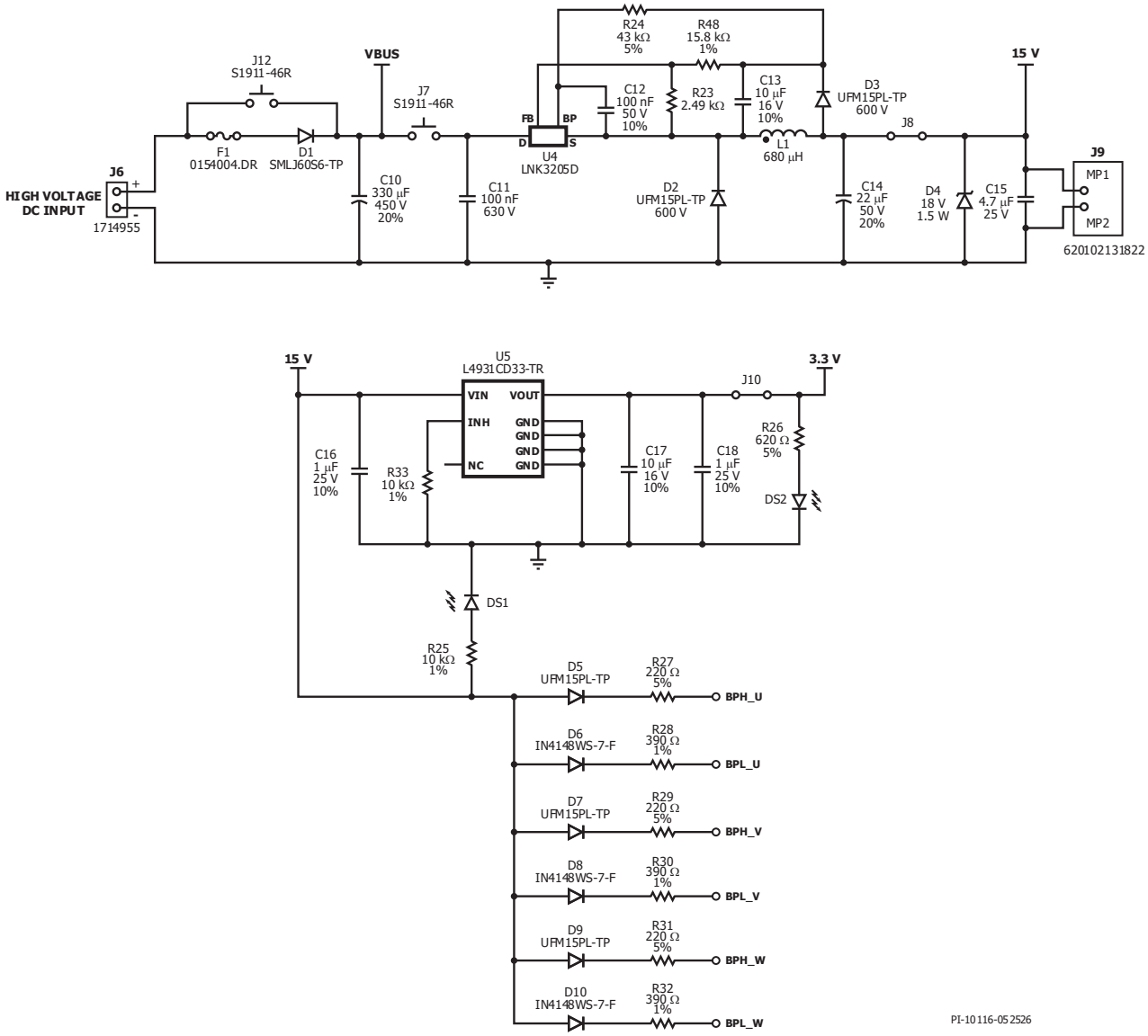

Figure 4 – Auxiliary Supply Section.

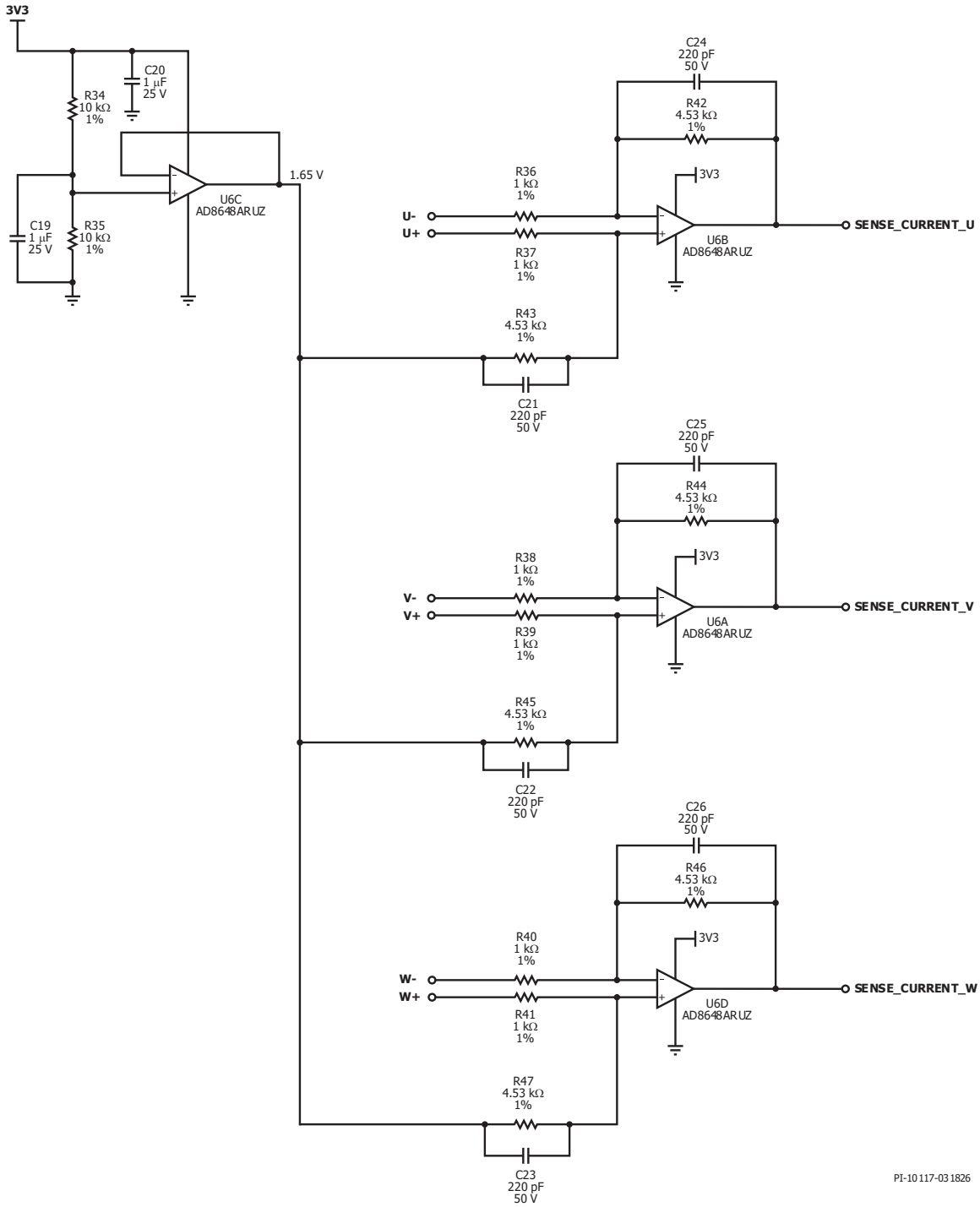

Figure 5 – Current Feedback Section.

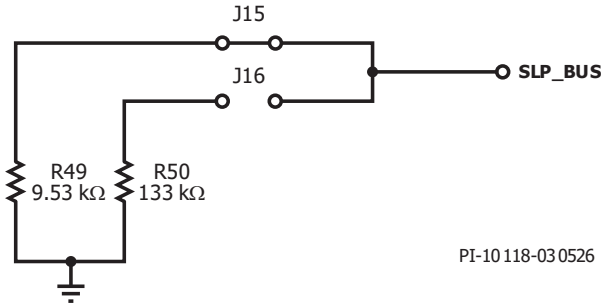

Figure 6 – SLP Pin Programming.

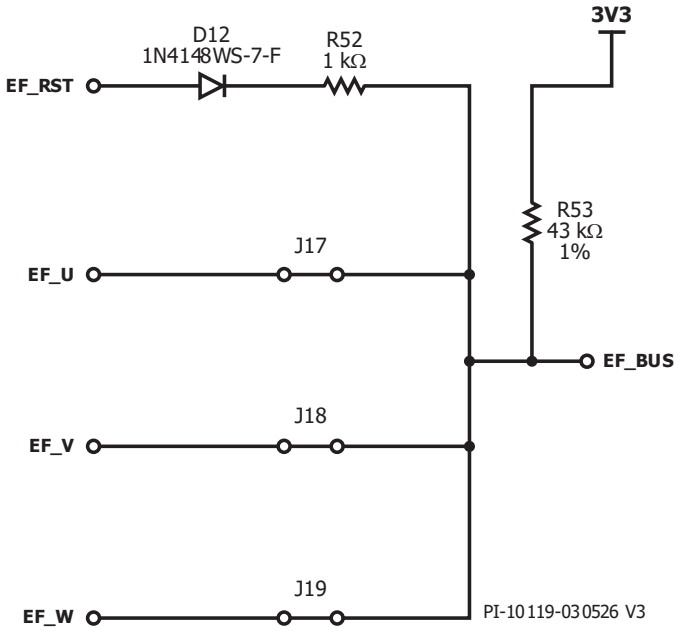

Figure 7 – Error Flag Circuit.

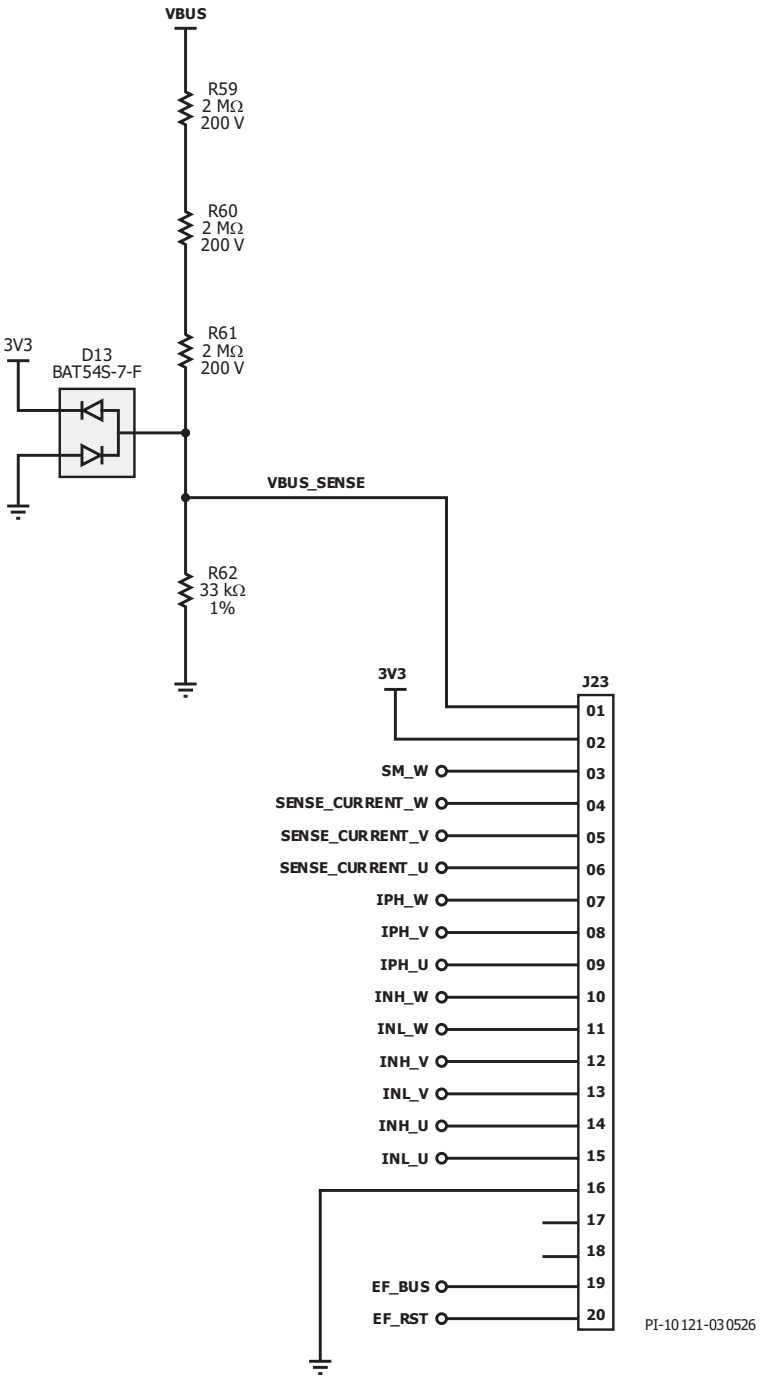

Figure 8 – Microcontroller (MCU) Interface.

4 Circuit Description

This reference design features a three-phase inverter that utilizes three BridgeSwitch-2 BRD2869WB components to drive a high-voltage, three-phase, brushless DC motor. Each BridgeSwitch-2 device integrates two 600 V, N-channel power FREDFETs along with their respective gate drivers into a compact surface-mount package. The power FREDFET incorporates an ultra-soft, fast-recovery diode that is ideally suited for use in inverter drives. A LinkSwitch-TN2 LNK3205D device configured as a high-voltage buck converter supplies the necessary 15 V bias power for the BRD2869WB component. The 3.3 V linear regulator steps down the 15 V external supply voltage to supply power to both the external MCU and the current sensing amplifier circuit.

Each BridgeSwitch-2 device incorporates various fault protection features, such as cycle-by-cycle overcurrent protection (OCP) for both low-side and high-side FREDFETs, over-temperature protection (OTP), and overvoltage protection (OVP). The BridgeSwitch-2 device also features the new error flag (EF) pin, which inhibits the device from switching when pulled down by an external microcontroller, and upon encountering any of the following destructive fault conditions: overvoltage (OV), overtemperature (OT), and sixteen consecutive low-side overcurrent (OC) events, when configured in latching mode.

4.1 Inverter Section

The BRD2869WB devices U1, U2, and U3 form the three-phase inverter. The output of the inverter connects to the three-phase BLDC motor through connectors P1, P2, and P3. In the PCB layout, the motor connectors are directly connected to the HB pad (Pin 39) of each BRD2869WB device, but not to the HB pins (Pins 28 and 31). The HB pad and pin are internally connected in the device, allowing more creepage and clearance headroom in the PCB layout.

4.2 Power Section

The power section consists of four main blocks: the input stage, the 15 V auxiliary supply, the 3.3 V low-dropout (LDO) regulator, and the external bias circuitry for each BRD2869WB device.

4.2.1 Input Section

The input section comprises the DC input connector (J6), input diode (D1), input fuse (F1), bypass jumper (J12), and bulk capacitor (C10). Diode D1 provides reverse-polarity protection for the DC input, while fuse F1 safeguards against overcurrent conditions. Capacitor C10 serves as the main bulk capacitance for the entire inverter. Jumper J12 remains open during normal operation and is shorted during efficiency measurements to bypass the fuse and diode. For stable high-voltage DC input applications, a 330 μF capacitor at C10 is sufficient, whereas AC input applications require a minimum of 750 μF. In this reference design, a high-voltage DC supply is used.

4.2.2 15 V Auxiliary Supply

The LNK3205D device (U4), configured as a buck converter, generates the 15 V external bias from the high-voltage DC bus input. Jumper J8 connects the buck converter output to the 15 V DC rail. Alternatively, connector J9 allows the bias voltage to be supplied

externally, with jumpers J7 and J8 left open to disable the buck converter and disconnect its output from the external source. For inverter efficiency measurements, using an external 15 V supply is recommended to isolate inverter performance from overall system efficiency.

For detailed information on the LNK3205D, refer to the datasheet: https://ac-dc.power.com/design-support/product-documents/data-sheets/linkswitch-tn2-data-sheet/

4.2.3 3.3 V LDO

The 3.3 V low-dropout regulator (U5) powers both the external microcontroller (MCU) and the optional current amplifier circuit for shunt-based current feedback applications. Jumper J10, shorted by default, connects the LDO output to the 3.3 V rail. Alternatively, Pin 2 of connector J23 allows the 3.3 V rail to be supplied externally via the MCU interface. If done so, J10 should remain open. LED DS2 provides a visual indication of the 3.3 V rail status.

4.2.4 BridgeSwitch-2 External Supply Biasing

A 15 V external supply is required for the BRD2869WB low-side and high-side drivers. Resistors R27, R28, R29, R30, R31, and R32 limit the current to approximately 2.5 mA into the gate driver supply pins (BPL and BPH). Diodes D5, D7, and D9 serve as high-voltage bootstrap diodes for the high-side gate drivers, while diodes D6, D8, and D10, which are used to isolate the BPL pins, are optional and may be shorted if not required. Capacitors C4, C5, C6, C7, C8, and C9 provide local decoupling for both the low-side and high-side gate driver supplies.

4.3 PWM Input

The input PWM signals INL_U, INH_U, INL_V, INH_V, INL_W, and INH_W control the switching states of the integrated high-side and low-side power FREDFETs. These signals are generated by the system microcontroller at the desired switching frequency. Resistors R4, R5, R6, R7, R8, and R9 act as PWM input filters before routing the signals to the INL and /INH pins of each BRD2869WB device.

4.4 Cycle-by-Cycle Current Limit

Resistors R10, R11, R12, R13, R14, and R15 define the cycle-by-cycle current limit for the integrated low-side and high-side power FREDFETs. With a resistance value of 42.2 kΩ, the current limit is set to 100% of the default overcurrent threshold (7.0 A for the BRD2869WB). For the low-side FREDFET, the cycle-by-cycle overcurrent protection response is selected by configuring the SLP resistor: either 9.53 kΩ by shorting J15, or ≥1 MΩ by keeping both J15 and J16 open. The high-side FREDFET OCP response is fixed to cycle-by-cycle operation by default and is not influenced by the SLP resistor value.

4.5 Latching Current Limit

Setting the SLP programming resistor to 133 kΩ by shorting J16 enables latching current limit protection for the low-side power FREDFET. In this mode, the low-side FREDFET latches off after sixteen consecutive overcurrent events. The Error Flag pin is then driven low to inhibit switching and is only released after either a power cycle or an EF reset command from the MCU. The high-side FREDFET OCP response remains fixed to cycle-by-cycle operation by default and is unaffected by the SLP resistor setting.

4.6 Overvoltage (OV) Protection

The SM pin of BridgeSwitch-2 device U1 is configured to monitor the DC bus voltage via resistors R1, R2, and R3. A total resistance of 6 MΩ sets the overvoltage protection threshold to 362 VDC. When this threshold is exceeded, the EF bus inhibits FREDFET switching on all BridgeSwitch-2 devices after an 80 μs delay. Switching is automatically re-enabled once the bus voltage falls below the hysteresis threshold of approximately 338 VDC, at which point the EF bus is released.

4.7 Error Flag

The Error Flag (EF) pin is an open-drain pin that facilitates fault communication with the microcontroller. It requires a minimum pull-up resistance of 43 kΩ for compatibility with both 3.3 V and 5 V MCUs and is typically connected to other EF pins to form the EF bus.

Under latching fault conditions, such as latching overcurrent or overtemperature faults, the EF pin is driven low to inhibit FREDFET switching. It remains latched until cleared by either a power cycle or an EF reset command via D12 and R52. For hysteretic protection events, such as overvoltage or hysteretic overtemperature, the EF pin is automatically released once safe operating conditions are re-established.

4.8 External Temperature Monitoring

When using the EF bus functionality, the SM pin can also be configured for external temperature monitoring. This is achieved by shorting J5, which connects thermistor RT1 and resistor R22 to the SM pin of device U2. RT1 should be an NTC-type thermistor, while R22 is selected such that the product of the equivalent resistance of RT1 at the desired temperature threshold and R22, multiplied by 100 μA, yields approximately 1.17 V.

4.9 IPH Feedback

This reference design utilizes the instantaneous phase current (IPH) signals as current feedback for Field-Oriented Control implementation via MotorXpert. The IPH pin functions as a current source that outputs the instantaneous low-side FREDFET current, scaled according to the device's gain. Resistors R16, R17, and R18 convert the IPH current signal into a corresponding voltage signal, which is fed directly to the microcontroller for current feedback.

For the BRD2869WB, the IPH gain is 30 μA/A, resulting in a 30 μA IPH output for a 1 A low-side FREDFET current. Using a 10 kΩ IPH resistor converts this current into a 300 mV voltage signal, suitable as input to the microcontroller's ADC pin.

4.10 Current Sense Amplifier

This reference design includes on-board op-amp amplifier circuits for a traditional shunt resistor current feedback method. Op-amps U6A, U6B, and U6D act as current sense amplifiers, converting voltage drops across shunt resistors R19, R20, and R21 into voltage signals suitable for the microcontroller ADC inputs. Op-amp U6C generates a 1.65 VDC offset from the 3.3 VDC supply, shifting the current signals into the positive range for ADC compatibility.

The shunt resistors are sized to produce a maximum of ±0.33 V across the LS-to-SG pins at the device's overcurrent protection threshold of 7.0 A. With a differential gain of 4.53, the amplifier circuits output a 1.5 V peak signal centered at 1.65 VDC.

4.11 Microcontroller (MCU) Interface

Connector J23 provides the interface between the BridgeSwitch-2 three-phase inverter board and an external microcontroller.
Table 2 lists the MCU interface pin assignments.

Pin No.	Pin Name	Pin Type	Pin Description
1	VBUS_SENSE	Output	Voltage divider output for high-voltage DC bus sensing (scale-down factor: 0.0055).
2	3V3	Power Input	3.3 V microcontroller supply input.
3	SM_W	Input	Optional SM pin input for Phase W (U3).
4	SENSE_CURRENT_W	Output	Phase W (U3) R_{SHUNT} voltage amplifier output.
5	SENSE_CURRENT_V	Output	Phase V (U2) R_{SHUNT} voltage amplifier output.
6	SENSE_CURRENT_U	Output	Phase U (U1) R_{SHUNT} voltage amplifier output.
7	IPH_W	Output	Phase W (U3) IPH output.
8	IPH_V	Output	Phase V (U2) IPH output.
9	IPH_U	Output	Phase U (U1) IPH output.
10	INH_W	Input	Phase W (U3) high-side FREDFET PWM control signal.
11	INL_W	Input	Phase W (U3) low-side FREDFET PWM control signal.
12	INH_V	Input	Phase V (U2) high-side FREDFET PWM control signal.
13	INL_V	Input	Phase V (U2) low-side FREDFET PWM control signal.
14	INH_U	Input	Phase U (U1) high-side FREDFET PWM control signal.
15	INL_U	Input	Phase U (U1) low-side FREDFET PWM control signal.
16	GND	MCU Ground	Microcontroller ground reference.
19	EF_BUS	Open-drain, I/O	Error Flag state monitoring. Pulling this low inhibits FREDFET switching for BridgeSwitch-2 devices with EF functionality.
20	EF_RST	Input	Error Flag reset signal. Momentarily pulling this pin high re-enables device switching after a latching fault.

Note: Pins 17 and 18 are not used

Table 2 – MCU Interface Pinout Description.

5 Printed Circuit Board Layout

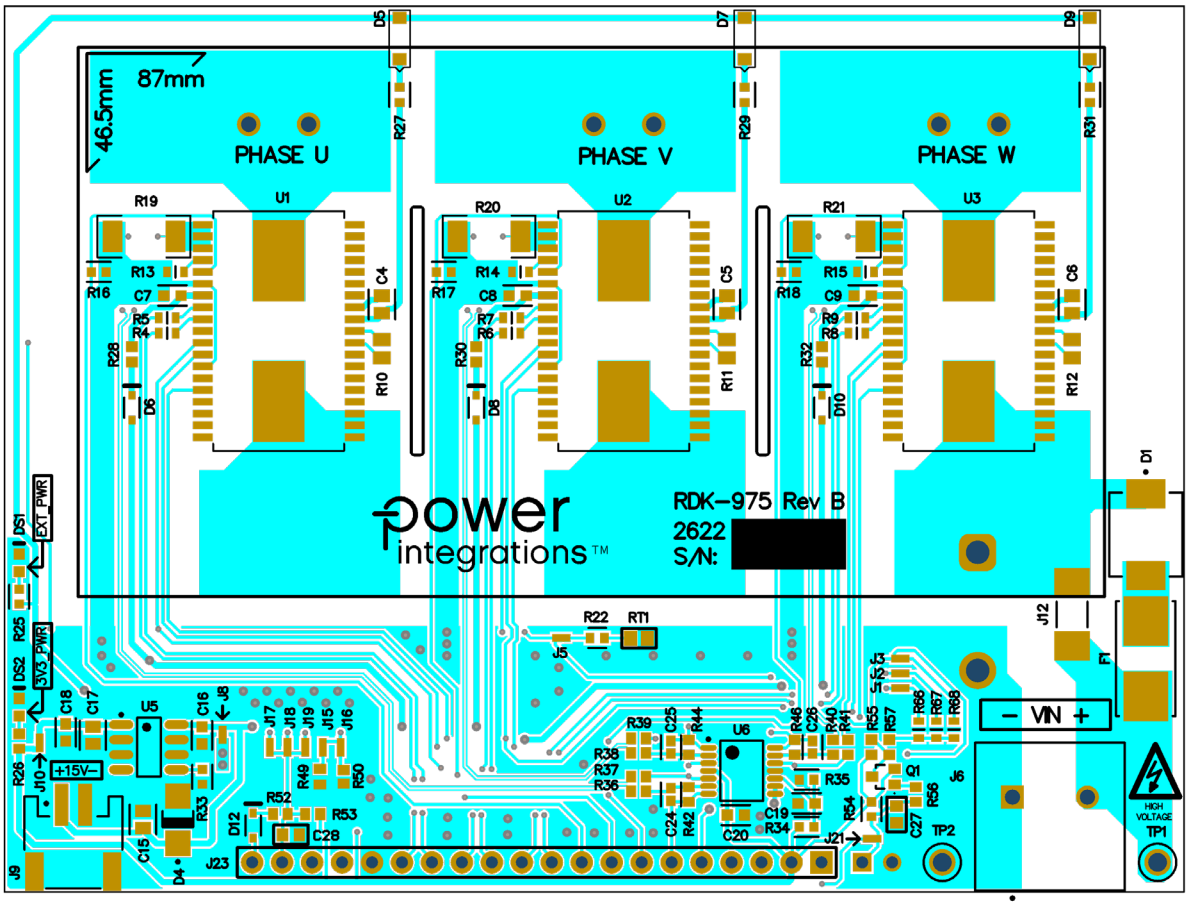

Figure 9 – Printed Circuit Board Layout Top View.

Notes:

1. The overall PCB dimension is 100 mm x 75 mm (L x W).
2. The inverter PCB dimension is 87 mm x 46.5 mm (L x W) – outlined by the black rectangle.
3. PCB Specifications:
   - Board thickness: 2 mm
   - Board material: FR4
   - Copper weight: 2 oz
   - No. of layers: 2

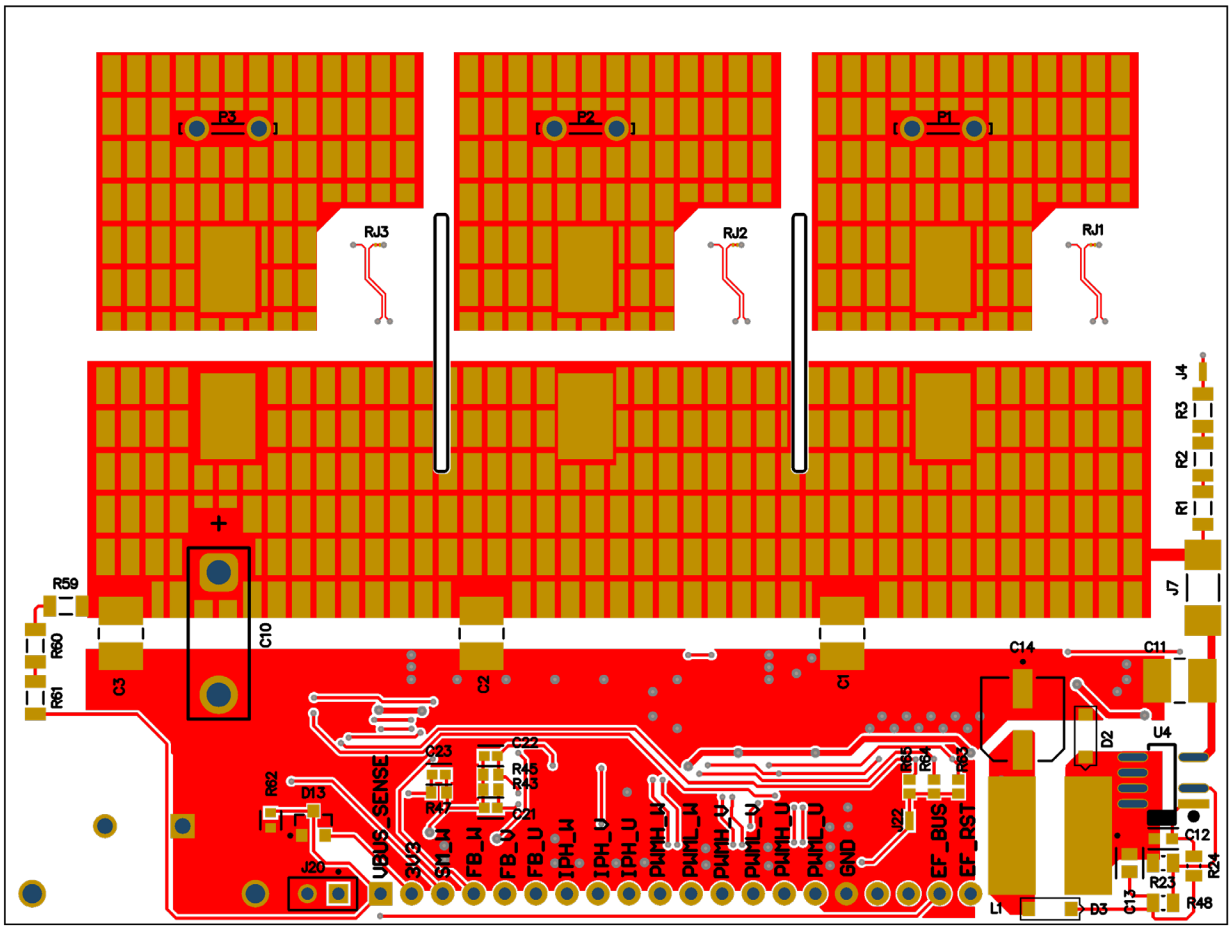

Figure 10 – Printed Circuit Board Layout Bottom View.

6 Bill of Materials

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	4	C1, C2, C3, C11	0.1 μF, 630 V, Ceramic, X7R, 1812	GRM43DR72J104KW01K	Murata Electronics
2	4	C4, C5, C6, C15	4.7 μF, 25 V, Ceramic, X7R, 0805	CL21B475KAFNNNE	Samsung
3	7	C7, C8, C9, C16, C18, C19, C20	1 μF, 25 V, Ceramic, X7R, 0603	GCM188R71E105KA64D	Murata Electronics
4	1	C10	330 μF, 20%, 450 V, Aluminum, TH	861221485017	Würth Elektronik
5	1	C12	0.1 μF, 50 V, Ceramic, X7R, 0603	CL10B104KB8NNND	Samsung
6	2	C13, C17	10 μF, 16 V, Ceramic, X7R, 0805	CL21B106KOQNNNE	Samsung
7	1	C14	22 μF, 20%, 50 V, Aluminum Hybrid, SMD	EEH-ZC1H220P	Panasonic
8	6	C21, C22, C23, C24, C25, C26	220 pF, 50 V, Ceramic, C0G, 0603	C1608C0G1H221J080AA	TDK Corporation
9	1	D1	600 V, 6 A, Standard, DO-214AB	SMLJ60S6-TP	Micro Commercial
10	5	D2, D3, D5, D7, D9	600 V, 1 A, Standard, SOD-123FL	UFM15PL-TP	Micro Commercial
11	1	D4	18 V, 1.5 W, Zener, SMA	SZ1SMA5931BT3G	Onsemi
12	4	D6, D8, D10, D12	75 V, 150 mA, Standard, SOD-323	1N4148WS-7-F	Diodes Incorporated
13	1	D13	30 V, 200 mA, Schottky, SOT-23	BAT54S-7-F	Diodes Incorporated
14	2	DS1, DS2	Red, LED, Chip SMD	LTST-C190KRKT	Lite-On Inc.
15	1	F1	4 A, 125 VAC/VDC, 2-SMD	0154004.DR	Littelfuse Inc.
16	13	J1, J2, J3, J4, J5, J8, J10, J15, J16, J17, J18, J19	PCB Jumper	JUMPER	
17	1	J6	2P, 6.35 mm, Terminal Block, Side Ent.	1714955	Phoenix Contact
18	2	J7, J12	Tin Jumper, SMD	S1911-46R	Harwin Inc.
19	1	J9	2 pos, 2 mm pitch, Header, SMD R/A	620102131822	Würth Elektronik
20	1	J23	20 pos, 2.54 mm, Header, Vertical	PH1-20-UA	Adam Tech
21	1	L1	680 μH, 360 mA, 2.25 Ω, SMD	744776268	Würth Elektronik
22	3	P1, P2, P3	0.250”, Quick Connect Tab	1287-ST	Keystone Electronics
23	6	R1, R2, R3, R59, R60, R61	RES, 2 MΩ, 1%, 1/4 W, 1206	ERJ-8ENF2004V	Panasonic
24	9	R4, R5, R6, R7, R8, R9, R66, R67, R68	RES, 10 Ω, 1%, 1/10 W, 0603	ERJ-3EKF10R0V	Panasonic
25	3	R10, R11, R12	RES, 42.2 kΩ, 1%, 1/8 W, 0805	ERJ-6ENF4222V	Panasonic
26	3	R13, R14, R15	RES, 42.2 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF4222V	Panasonic
27	7	R16, R17, R18, R25, R33, R34, R35	RES, 10 kΩ, 1%, 1/10 W, 0603	CRGCQ0603F10K	TE Connectivity
28	3	R19, R20, R21	RES, 47 mΩ, 1%, 3/4 W, 2010	UR73D2HTTE47L0F	KOA Speer Electronics
29	1	R22	RES, 6.49 kΩ, 1%, 1/10 W, 0603	CRCW06036K49FKEA	Vishay Dale
30	1	R23	RES, 2.49 kΩ, 1%, 1/4 W, 0805	RK73H2ATTD2491F	KOA Speer Electronics
31	1	R24	RES, 43 kΩ, 5%, 1/8 W, 0805	RC0805JR-0743KL	YAGEO
32	1	R26	RES, 620 Ω, 5%, 1/10 W, 0603	ERJ-3GEYJ621V	Panasonic
33	3	R27, R29, R31	RES, 220 Ω, 5%, 1/10 W, 0603	ERJ-3GEYJ221V	Panasonic
34	3	R28, R30, R32	RES, 390 Ω, 1%, 1/10 W, 0603	ERJ-3EKF3900V	Panasonic

35	7	R36, R37, R38, R39, R40, R41, R52	RES, 1 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF1001V	Panasonic
36	6	R42, R43, R44, R45, R46, R47	RES, 4.53 kΩ, 1%, 1/10 W, 0603	ERJ-3EKF4531V	Panasonic
37	1	R48	RES, 15.8 kΩ, 1%, 1/4 W, 0805	RK73H2ATTD1582F	KOA Speer Electronics
38	1	R49	RES, 9.53 kΩ, 1%, 1/10 W, 0603	RK73H1JTTD9531F	KOA Speer Electronics
39	1	R50	RES, 133 kΩ, 1%, 1/10 W, 0603	CRCW0603133KFKEA	Vishay Dale
40	1	R53	RES, 43 kΩ, 1%, 1/10 W, 0603	RK73H1JTTD4302F	KOA Speer Electronics
41	1	R62	RES, 33 kΩ, 1%, 1/10 W, 0603	CRCW060333K0FKEA	Vishay Dale
42	1	RT1	100 kΩ, 4330 K, NTC Thermistor, 0603	ERT-J1VS104JA	Panasonic
43	1	TP1	Test Point, Red, Thru-hole Mount	5010	Keystone Electronics
44	1	TP2	Test Point, Black, Thru-hole Mount	5011	Keystone Electronics
45	3	U1, U2, U3	BridgeSwitch-2, Max. BLDC Motor Current 7 A (DC), InSOP-L38C	BRD2869WB	Power Integrations
46	1	U4	LinkSwitch-TN2, SO-8C	LNK3205D	Power Integrations
47	1	U5	IC, REG, LDO, 3.3 V, 250 mA, 8-SOIC	L4931CD33-TR	STMicroelectronics
48	1	U6	IC, GP Op-Amp, Quad Circuit, 14-TSSOP	AD8648ARUZ	Analog Devices Inc.

Table 3 – Bill of Materials.

7 Performance Data

This section presents the waveforms and performance data of the RDK-975 BRD2869WB inverter. Unless otherwise noted in a specific subsection, all measurements were taken under the default test conditions listed in Table 4.

Parameter	Value	Remarks
Input Voltage (DC)	340 VDC	Supplied by a stable high-voltage DC source.
Motor Control Algorithm	Sensorless FOC with IPH Current Reconstruction	Configured via MotorXpert Suite 3.0
PWM Switching Frequency	10.0 kHz	-
Startup Control Scheme	I/F Control	-
FOC Control Loop Frequency	10.0 kHz	-
Motor Speed	3000 RPM	Steady-state operation
Phase Current (Light Load)	550 mA_{RMS}	-
Phase Current (Full Load)	2.20 A_{RMS}	Rated phase current of the BRD2869WB
Current Feedback	IPH	Shunt resistors R19, R20, and R21 shorted
Ambient Temperature	23.0 °C	-
SLP Pull-down Resistor	133 kΩ	Configuration: • J15 Open (9.53 kΩ) • J16 Shorted (133 kΩ)
Error Flag (EF) Fault Response	-	• Latching LS OCP • Latching OTP

Table 4 – Default Test Conditions.

7.1 Start-Up Operation

7.1.1 Start-Up Waveforms

A 340 VDC bus voltage is applied with a 50 V/ms slew rate, producing the start-up waveforms shown below. The plots display the 15 V rail voltage, low-side bypass pin voltage, and high-side bypass pin voltage.

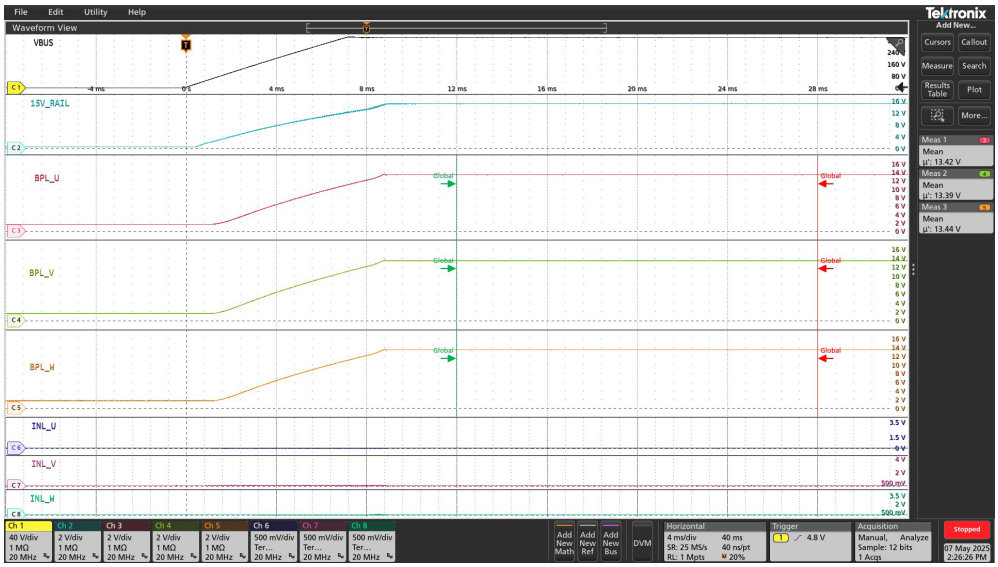

Figure 11 – 15 V Rail and BPL-to-SG Voltages at Start-up.

CH1: V_{BUS}, 40 V/div CH5: V_{BPL_W}, 2 V/div
CH2: V_{15V_RAIL}, 2 V/div CH6: V_{INL_U}, 0.5 V/div
CH3: V_{BPL_U}, 2 V/div CH7: V_{INL_V}, 0.5 V/div
CH4: V_{BPL_V}, 2 V/div CH8: V_{INL_W}, 0.5 V/div
Time Scale: 4 ms/div

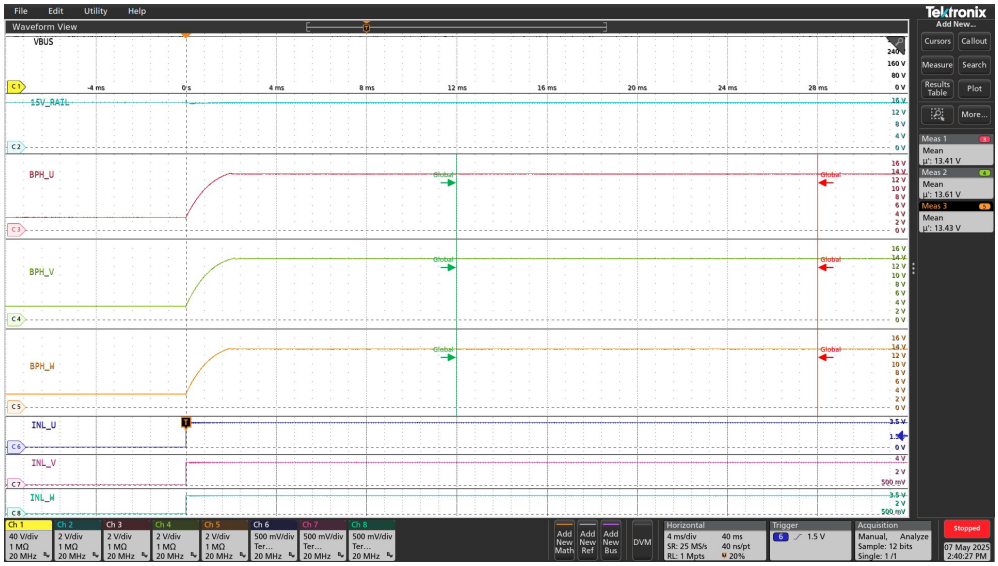

Figure 12 – BPH-to-HB Voltages at Start-up.

CH1: V_{BUS}, 40 V/div CH5: V_{BPH_W}, 2 V/div
CH2: V_{15V_RAIL}, 2 V/div CH6: V_{INL_U}, 0.5 V/div
CH3: V_{BPH_U}, 2 V/div CH7: V_{INL_V}, 0.5 V/div
CH4: V_{BPH_V}, 2 V/div CH8: V_{INL_W}, 0.5 V/div
Time Scale: 4 ms/div

7.1.2 Motor Start-Up Waveforms

The following waveforms illustrate the motor start-up behavior under light-load (550 mA_{RMS}) and full-load (2.2 A_{RMS}) conditions.

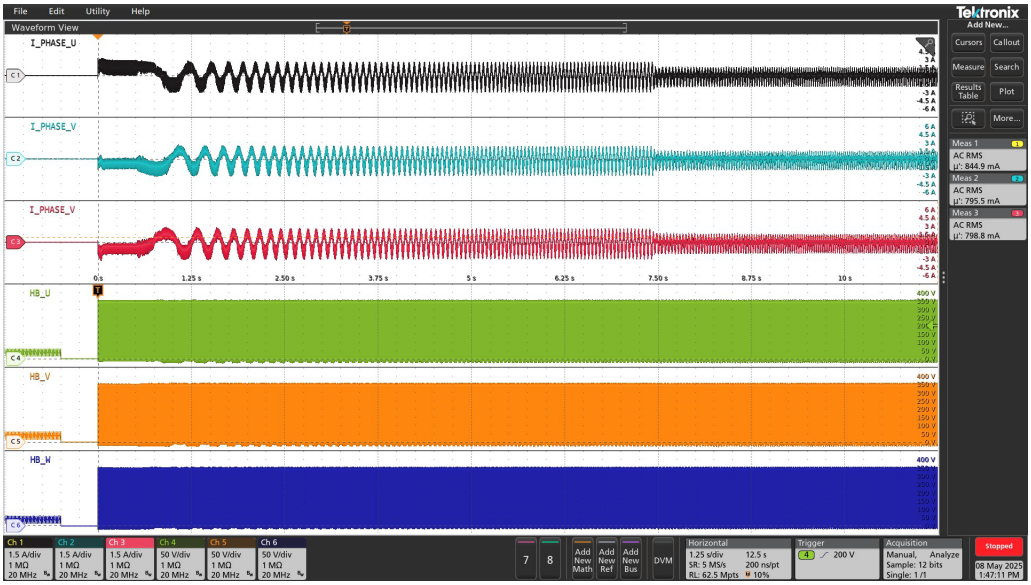

Figure 13 – Motor Start-up at Light Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1.25 s/div

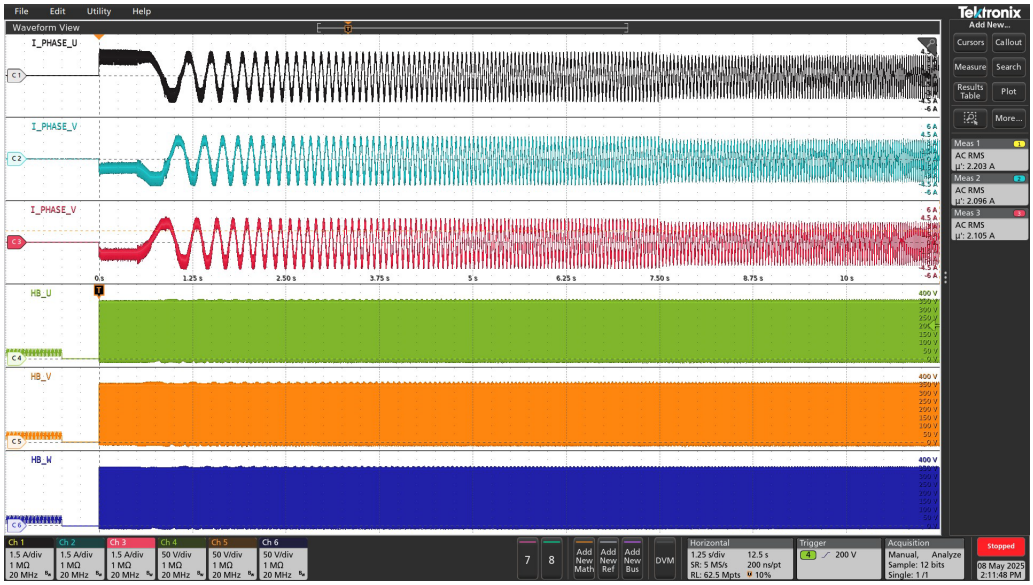

Figure 14 – Motor Start-up at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1.25 s/div

7.2 Steady-State Operation

7.2.1 Phase Voltages and Motor Phase Currents at Steady-State

The following waveforms present the phase voltage (low-side V_{DS}) and motor phase currents during operation at light load (550 mA_{RMS}) and full load (2.2 A_{RMS}).

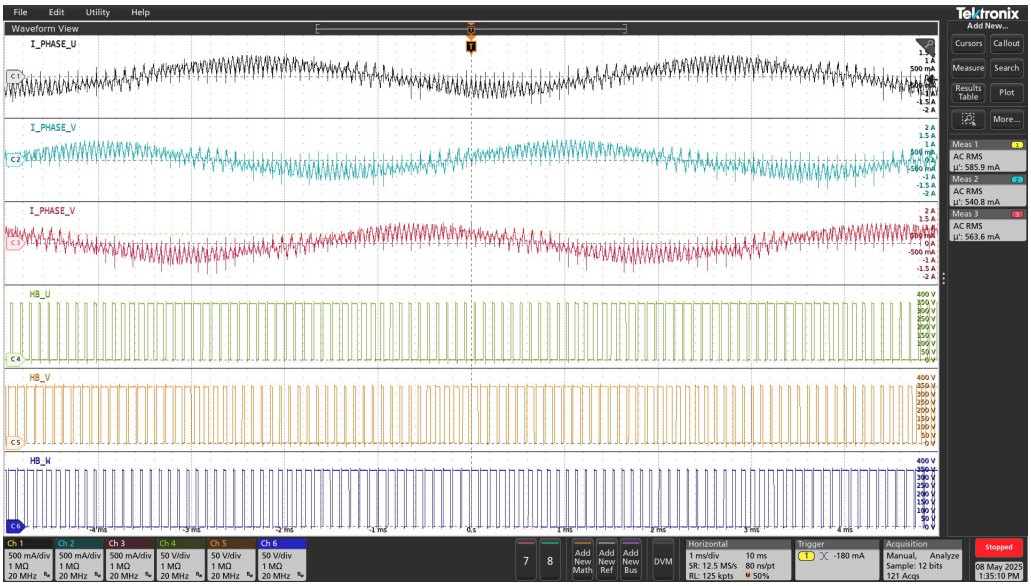

Figure 15 – Steady State Phase Voltages and Phase Currents at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1 ms/div

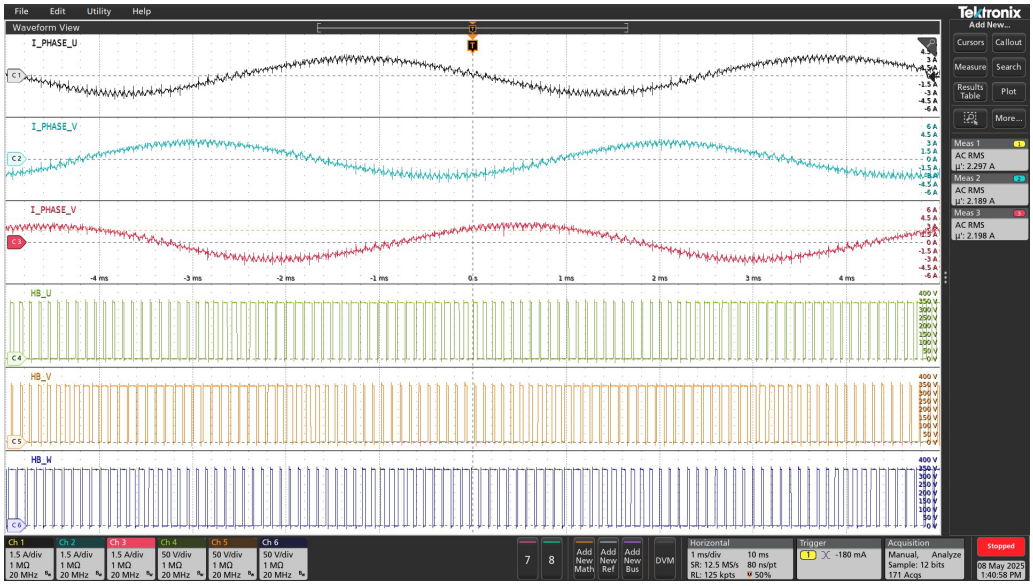

Figure 16 – Steady State Phase Voltages and Phase Currents at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div CH4: V_{HB_U}, 50 V/div
CH2: I_{PHASE_V}, 1.5 A/div CH5: V_{HB_V}, 50 V/div
CH3: I_{PHASE_W}, 1.5 A/div CH6: V_{HB_W}, 50 V/div
Time Scale: 1 ms/div

7.2.2 Low-Side Drain-to-Source Voltage Slew Rate at Steady State

The following waveforms show the voltage slew rate at the turn-on and turn-off transitions of the low-side FREDFET. Measurements were taken at light load and full load conditions, captured at both the positive and negative peaks of the phase current.

Table 5 summarizes the measured V_{DS} slew rates at different loading conditions and opposite current peaks:

	Positive Peak		Negative Peak	
	Turn-On	**Turn-Off**	**Turn-On**	**Turn-Off**
Light Load	0.95 V/µs	3.06 V/µs	4.05 V/µs	0.95 V/µs
Full Load	3.03 V/µs	3.29 V/µs	4.33 V/µs	3.18 V/µs

Table 5 – Low-side V_{DS} Slew Rate.

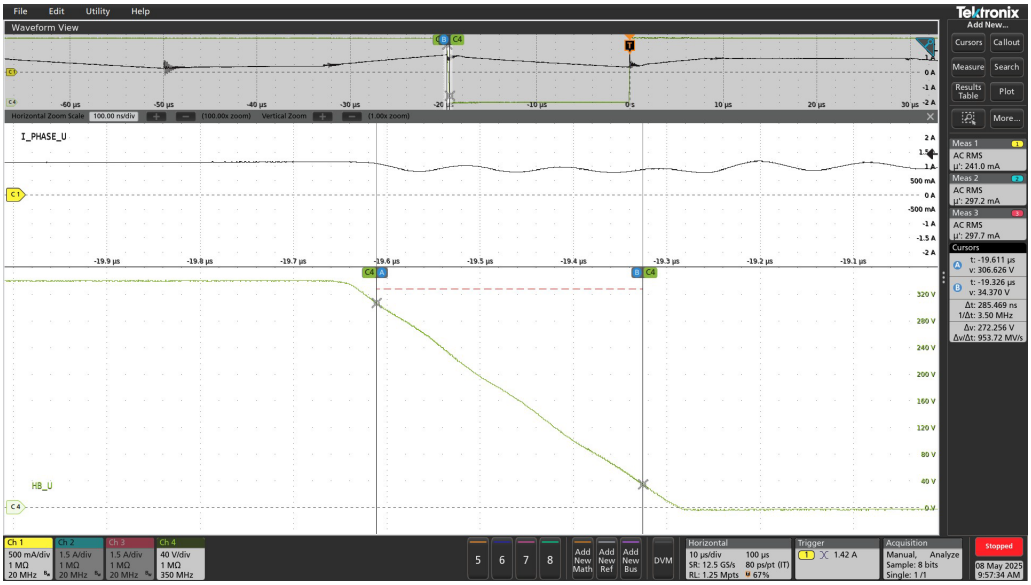

Figure 17 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Light Load (Positive Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 0.95 V/µs

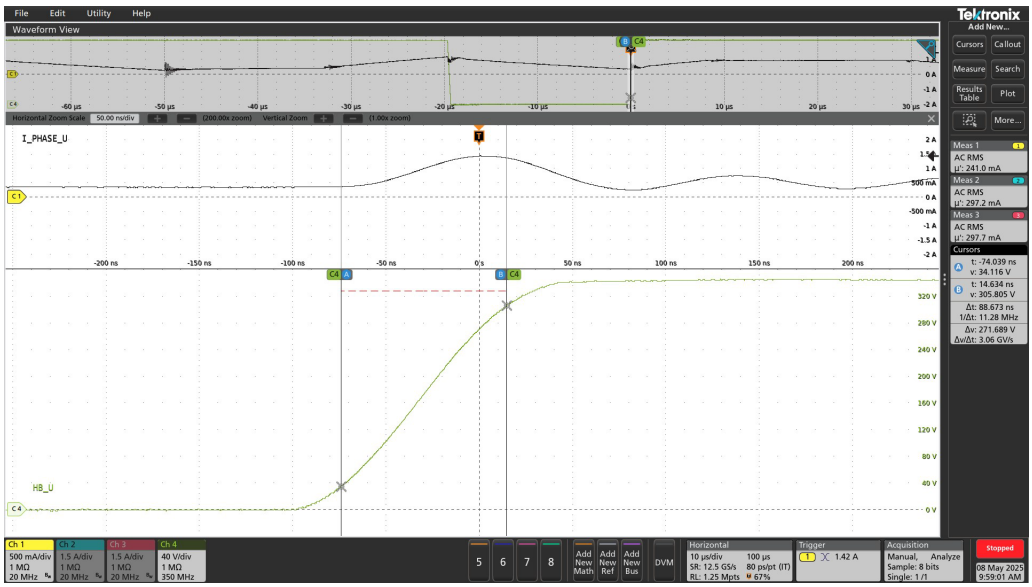

Figure 18 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Light Load (Positive Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.06 V/µs

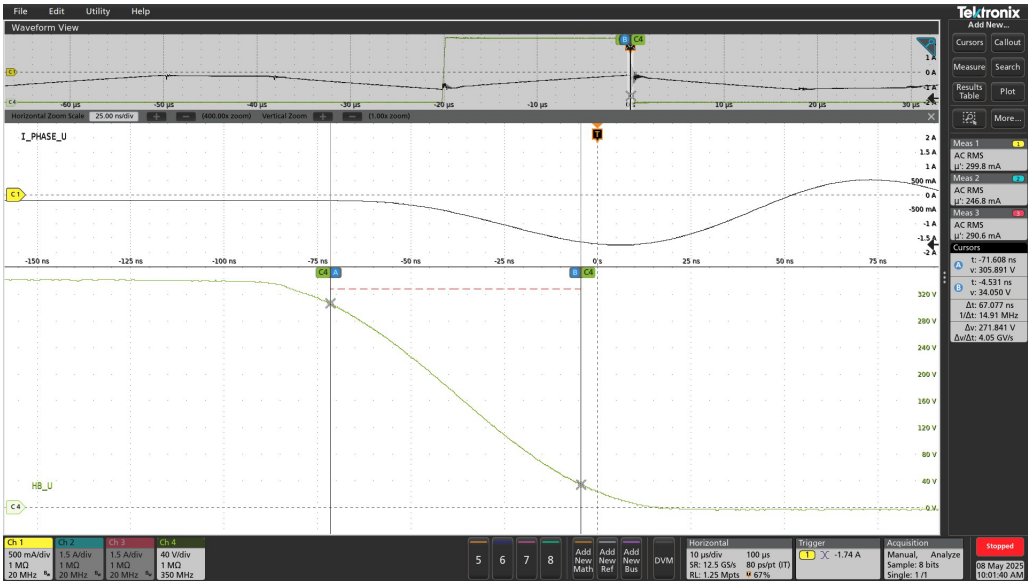

Figure 19 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Light Load (Negative Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 4.05 V/µs

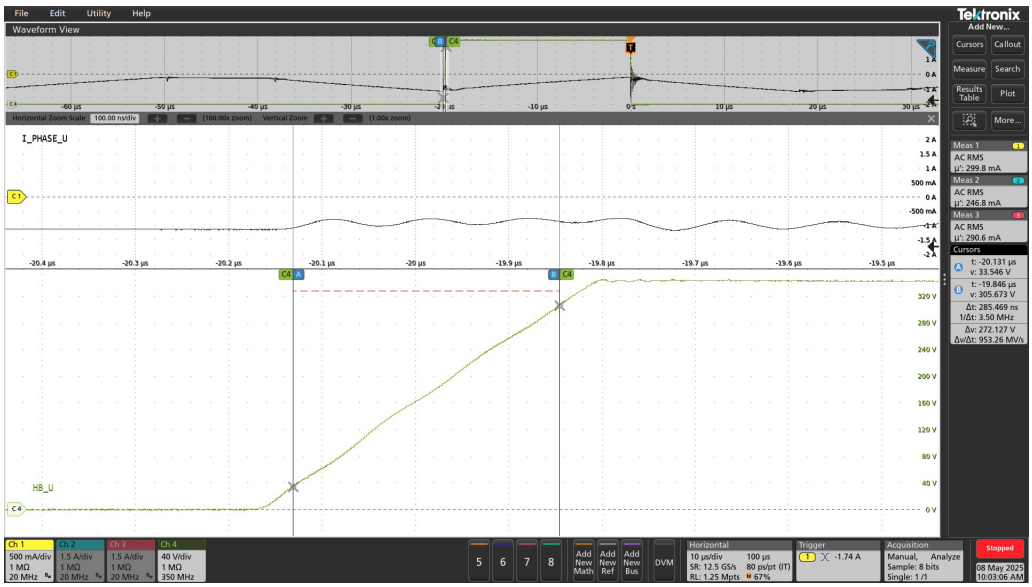

Figure 20 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Light Load (Negative Peak).
CH1: I_{PHASE_U}, 0.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 0.95 V/µs

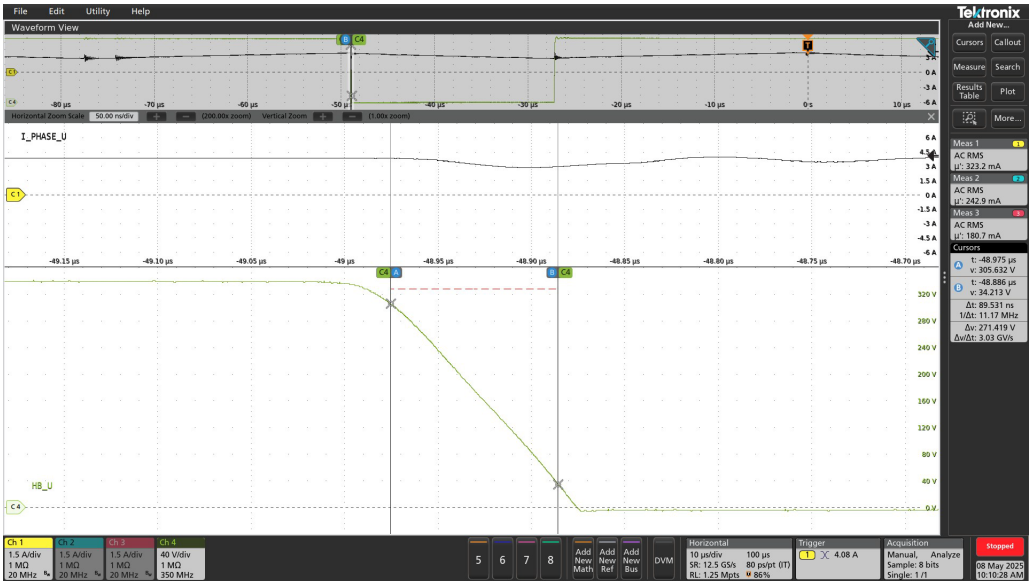

Figure 21 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Full Load (Positive Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.03 V/µs

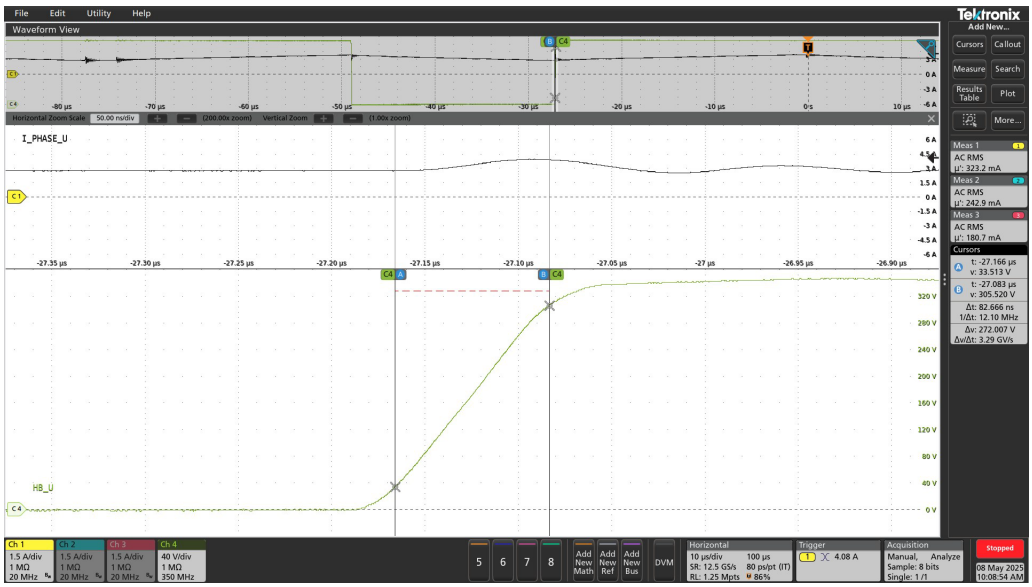

Figure 22 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Full Load (Positive Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 3.29 V/µs

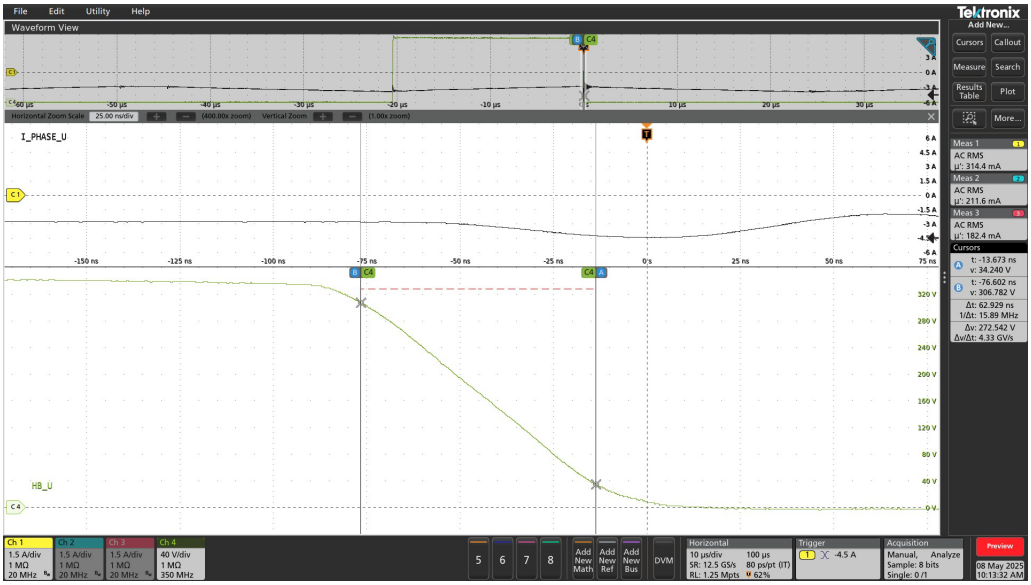

Figure 23 – Low-side V_{DS} Turn-On Slew Rate of Phase U at Full Load (Negative Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
Time Scale: 10 µs/div
Slew Rate: 4.33 V/µs

Figure 24 – Low-side V_{DS} Turn-Off Slew Rate of Phase U at Full Load (Negative Peak).
CH1: I_{PHASE_U}, 1.5 A/div
CH4: V_{HB_U}, 40 V/div
ime Scale: 10 µs/div
Slew Rate: 3.18 V/µs

7.2.3 BPL/BPH Level at Steady-State

The following waveforms show the bypass supply voltage DC levels during steady-state operation at light load and full load conditions.

Table 6 summarizes the measured BPL/BPH average voltage level at different loading conditions:

	V_{BPL}			V_{BPH}		
	Phase U	**Phase V**	**Phase W**	**Phase U**	**Phase V**	**Phase W**
DC Level (Light Load)	13.4	13.4	13.4	13.3	13.6	13.4
DC Level (Full Load)	13.3	13.4	13.4	13.2	13.6	13.3

Table 6 – BPL and BPH DC Voltage Levels.

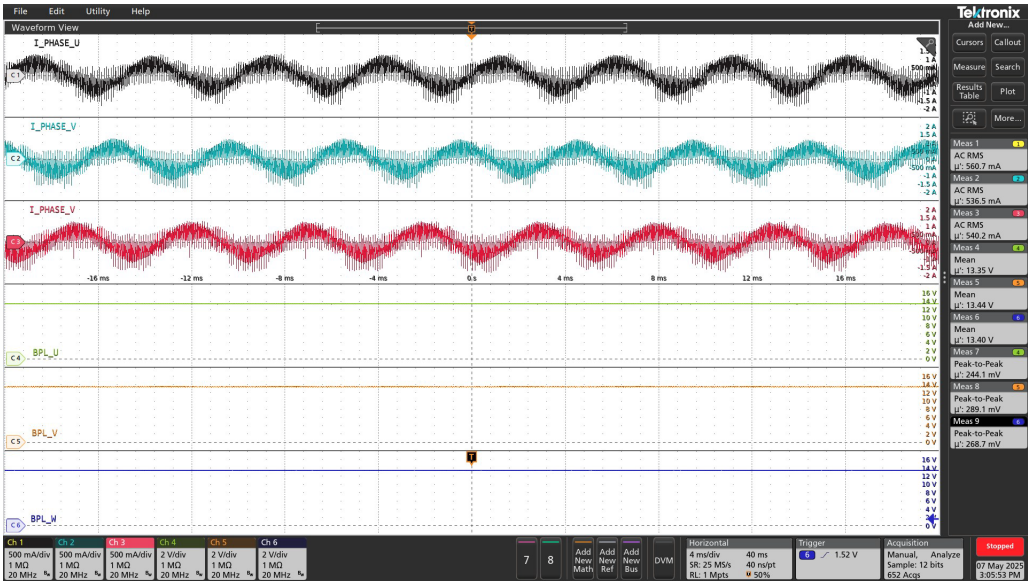

Figure 25 – Average BPL Voltage Levels at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPL_U}, 2 V/div $V_{BPL\_U, AVERAGE}$ = 13.4 V
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPL_V}, 2 V/div $V_{BPL\_V, AVERAGE}$ = 13.4 V
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPL_W}, 2 V/div $V_{BPL\_W, AVERAGE}$ = 13.4 V
Time Scale: 4 ms/div

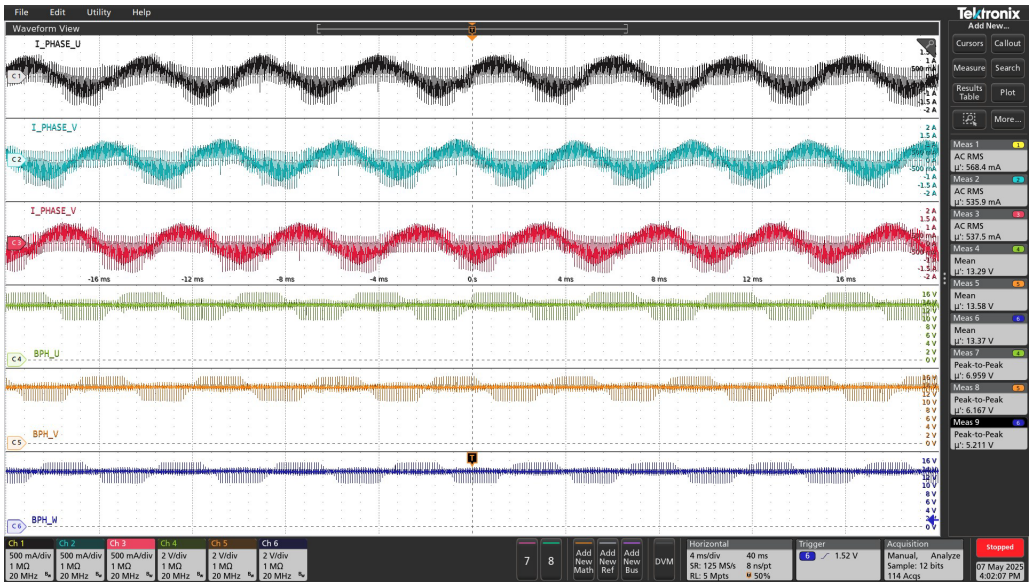

Figure 26 – Average BPH-to-HB Voltage Levels at Light Load.

CH1: I_{PHASE_U}, 0.5 A/div CH4: V_{BPH_U}, 2 V/div $V_{BPH\_U, AVERAGE}$ = 13.3 V
CH2: I_{PHASE_V}, 0.5 A/div CH5: V_{BPH_V}, 2 V/div $V_{BPH\_V, AVERAGE}$ = 13.6 V
CH3: I_{PHASE_W}, 0.5 A/div CH6: V_{BPH_W}, 2 V/div $V_{BPH\_W, AVERAGE}$ = 13.4 V
Time Scale: 4 ms/div

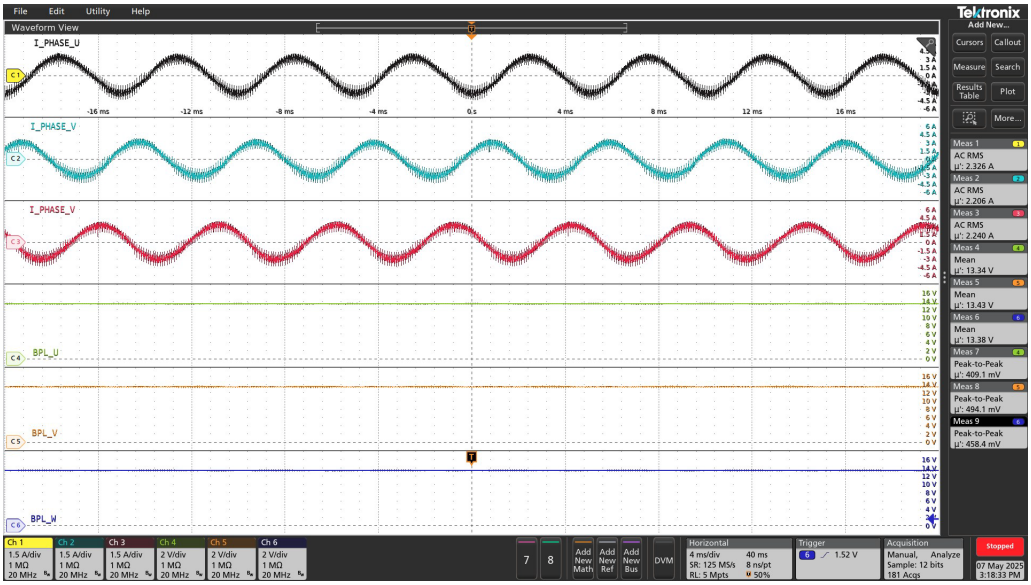

Figure 27 – Average BPL Voltage Levels at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div	CH4: V_{BPH_U}, 2 V/div	$V_{BPL\_U, AVERAGE}$ = 13.3 V
CH2: I_{PHASE_V}, 1.5 A/div	CH5: V_{BPH_V}, 2 V/div	$V_{BPL\_V, AVERAGE}$ = 13.4 V
CH3: I_{PHASE_W}, 1.5 A/div	CH6: V_{BPH_W}, 2 V/div	$V_{BPL\_W, AVERAGE}$ = 13.4 V

Time Scale: 4 ms/div

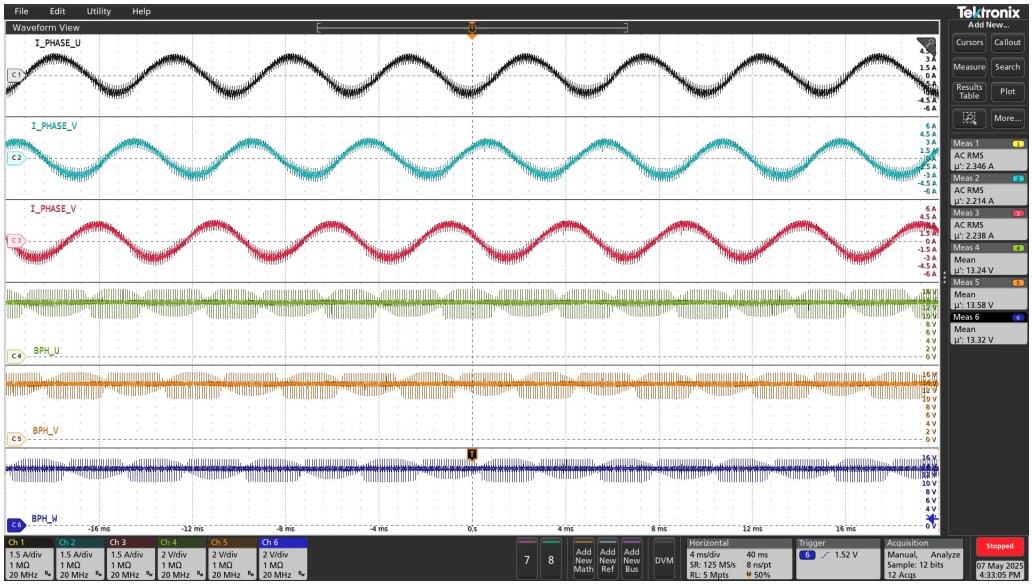

Figure 28 – Average BPH-to-HB Voltage Levels at Full Load.

CH1: I_{PHASE_U}, 1.5 A/div	CH4: V_{BPH_U}, 2 V/div	$V_{BPH\_U, AVERAGE}$ = 13.2 V
CH2: I_{PHASE_V}, 1.5 A/div	CH5: V_{BPH_V}, 2 V/div	$V_{BPH\_V, AVERAGE}$ = 13.6 V
CH3: I_{PHASE_W}, 1.5 A/div	CH6: V_{BPH_W}, 2 V/div	$V_{BPH\_W, AVERAGE}$ = 13.3 V

Time Scale: 4 ms/div

7.3 Thermal Performance

The thermal performance of the BRD2869WB devices under various load conditions was measured after a 30-minute soak period to ensure steady-state operation of the inverter and motor setup. An acrylic enclosure around the board minimized the influence of external airflow.

Motor speed was maintained at the rated 3000 RPM. At this speed and the full load phase current of 2.2 A_{RMS}, the inverter output power reaches 580 W. For 750 W (1 HP) inverter operation, the phase current was overdriven to nearly 3.0 A_{RMS}.

To isolate the inverter's thermal performance from other on-board circuits, external components were disabled as follows: J12 was shorted to bypass the input diode D1 and fuse F1, J7 and J8 were opened to disable the on-board 15 V regulator U4, and shunt resistors R19, R20, and R21 were shorted since the IPH feedback is used. An external 15 V supply was applied to J9 to power the on-board 3.3 V regulator U5 and provide bias voltage to the BridgeSwitch-2 devices.

By default, the BRD2869WB's IPH pin provides current feedback. The MotorXpert Suite reconstructs IPH signals as described in Section 8.4 of the Appendix.

Table 7 summarizes the measured thermal performance at different phase current conditions.

Average Phase Current (A_{RMS})	$I_{PHASE-U}$ (A_{RMS})	$I_{PHASE-V}$ (A_{RMS})	$I_{PHASE-W}$ (A_{RMS})	$T_{CASE, AVG}$ (°C)	$T_{AMBIENT}$ (°C)	$T_{RISE, AVG}$ (°C)
0.320	0.317	0.321	0.323	**38.3**	26.3	**12.0**
0.549	0.555	0.55	0.543	**44.7**	26.4	**18.3**
0.822	0.826	0.812	0.828	**51.2**	26.6	**24.6**
1.10	1.13	1.10	1.08	**56.3**	26.2	**30.1**
1.38	1.43	1.37	1.36	**64.8**	26.8	**38.0**
1.64	1.69	1.63	1.62	**71.0**	25.4	**45.6**
1.92	1.96	1.90	1.90	**80.0**	24.3	**55.7**
2.26	2.29	2.25	2.24	**94.0**	25.2	**68.8**
2.62	2.66	2.58	2.61	**113**	25.3	**87.7**
2.90	2.96	2.89	2.87	**135**	27.1	**108**

Table 7 – Thermal Performance Summary.

7.3.1 Thermal Scans Across Loading Conditions

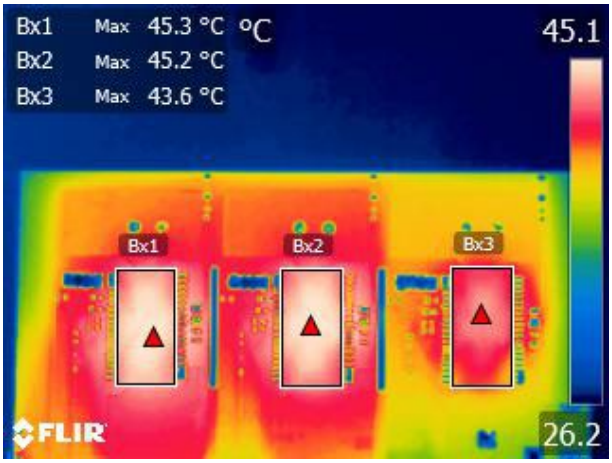

Figure 29 – Thermal Scan at 0.549 A_{RMS}
Ambient = 26.4 °C.

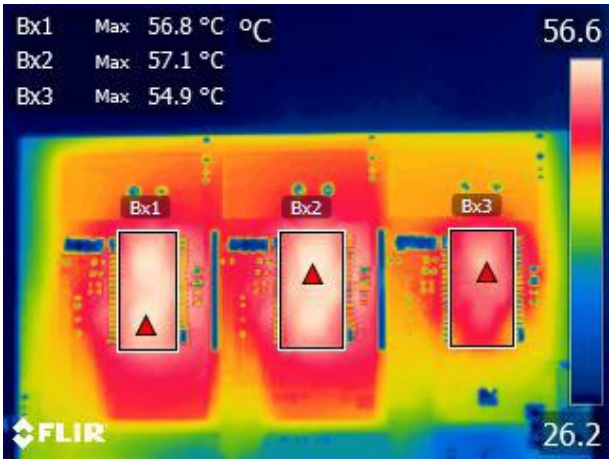

Figure 30 – Thermal Scan at 1.10 A_{RMS}
Ambient = 26.2 °C.

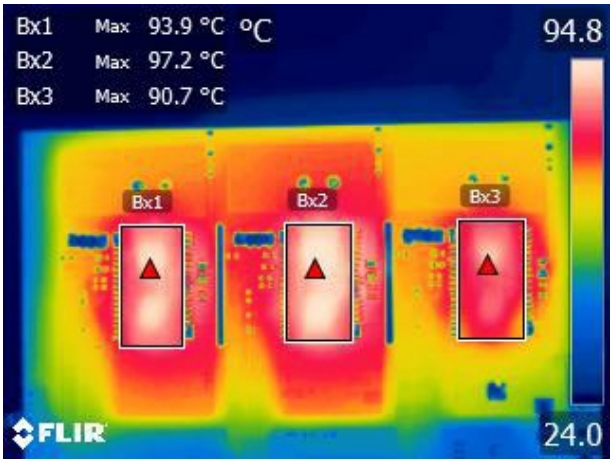

Figure 31 – Thermal Scan at 2.26 A_{RMS}
Ambient = 25.2 °C.

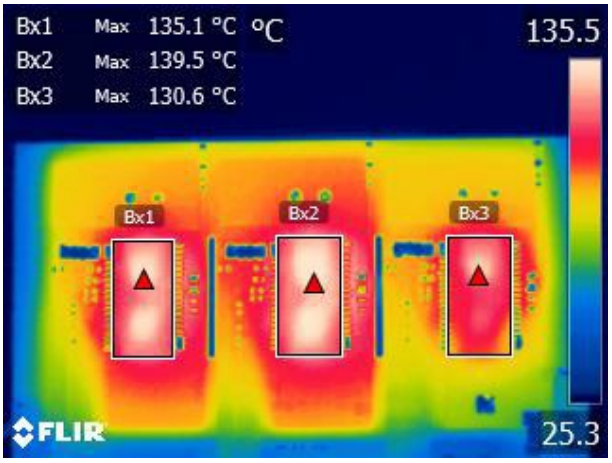

Figure 32 – Thermal Scan at 2.90 A_{RMS}
Ambient = 27.1 °C.

7.3.2 Thermal Performance Graphs

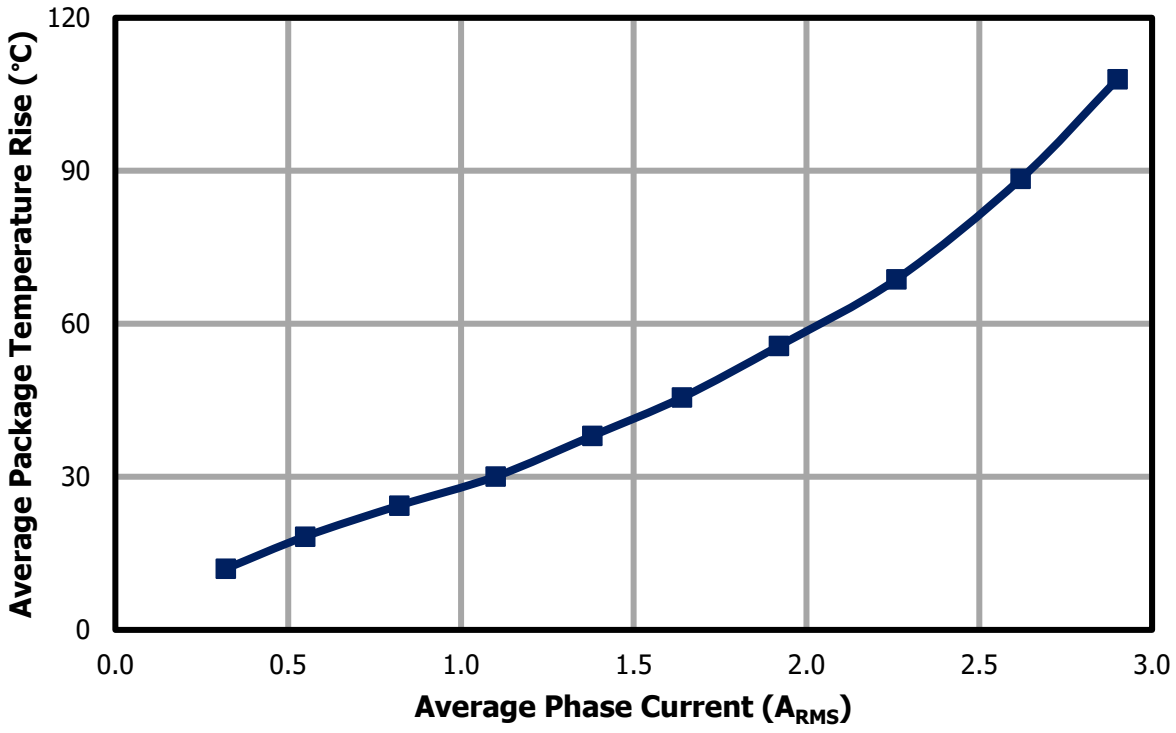

Figure 33 – Average Package Temperature Rise vs. Motor Phase Current.

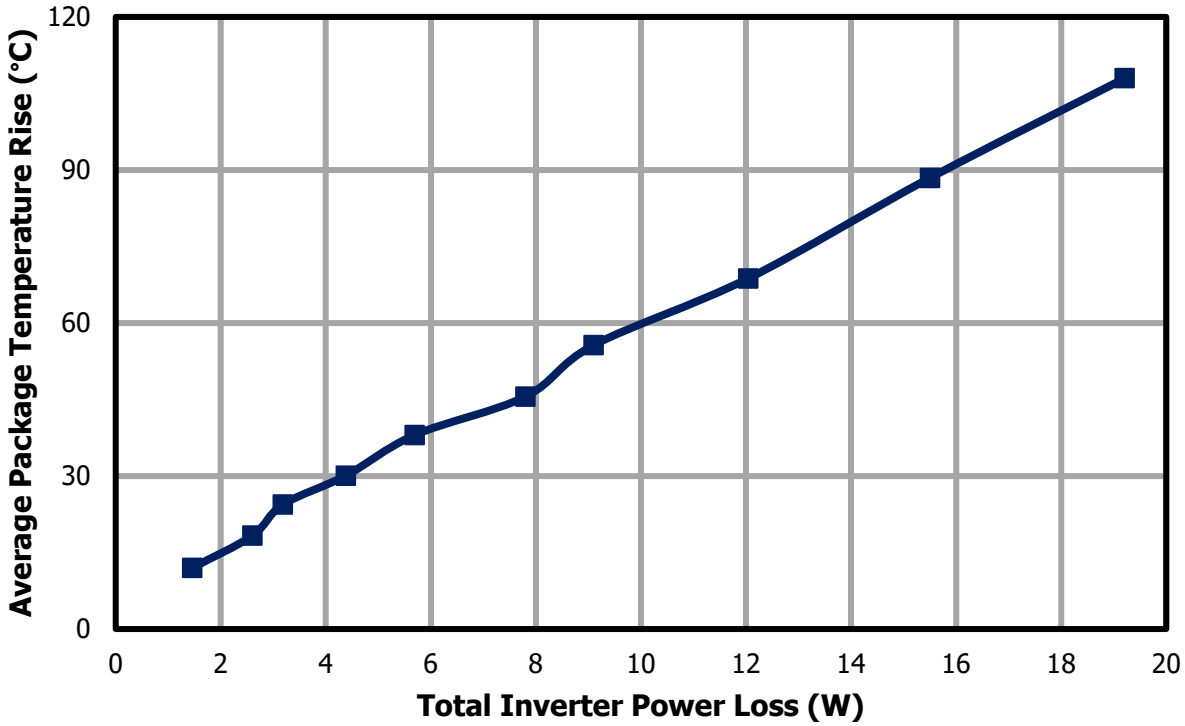

Figure 34 – Average Package Temperature Rise vs. Total Inverter Power Loss.

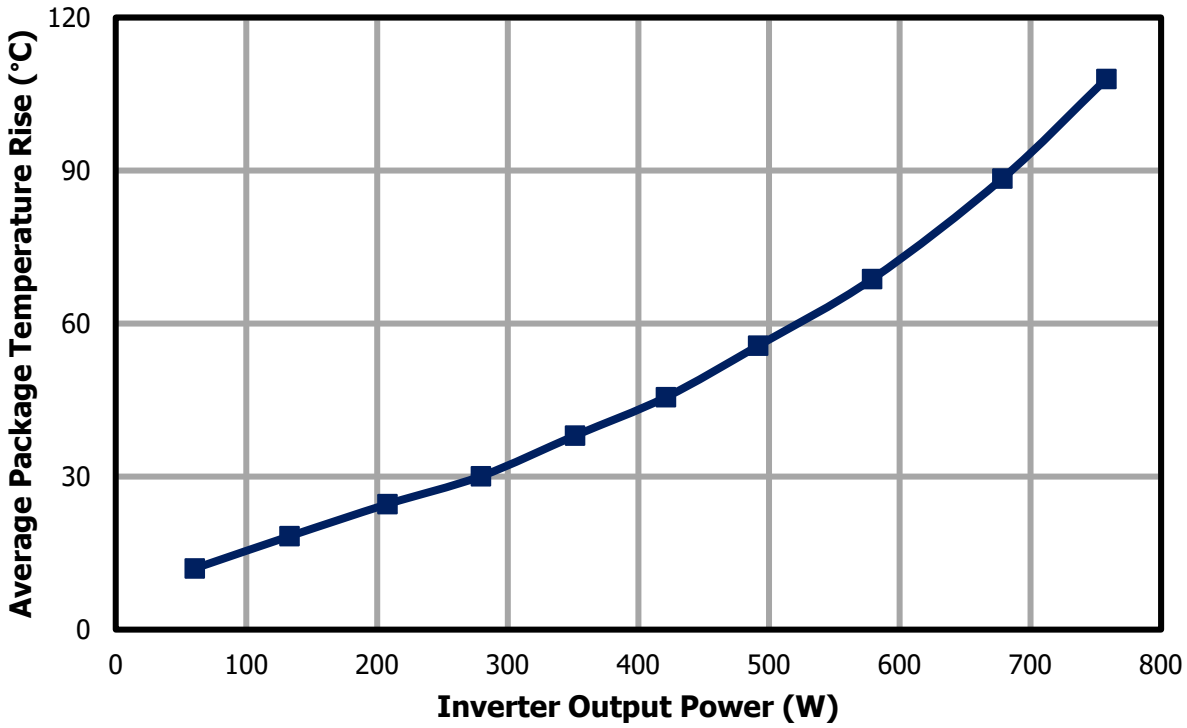

Figure 35 – Average Package Temperature Rise vs. Inverter Output Power.

7.4 Inverter Efficiency

The inverter efficiency of the BRD2869WB devices under various load conditions was recorded after a 30-minute soak period to ensure steady-state operation of the inverter and motor. An acrylic enclosure around the board minimized the effects of external airflow, maintaining an ambient temperature of about 23.0 °C.

Motor speed was maintained at the rated 3000 RPM. At this speed and the full load phase current of 2.2 A_{RMS}, the inverter output power reaches 580 W. For 750 W (1 HP) inverter operation, the phase current was overdriven to nearly 3.0 A_{RMS}.

Efficiency measurements were isolated to reflect inverter power losses only by disabling external circuits that add to the input power without contributing to the output power. This was accomplished by shorting J12 to bypass the input diode D1 and fuse F1, opening J7 and J8 to disable the on-board 15 V regulator U4, and shorting shunt resistors R19, R20, and R21. An external 15 V supply was applied to J9 to power up the built-in 3.3 V regulator U5 and provide bias voltage to the BridgeSwitch-2 devices.

The three-phase power meter setup used for the efficiency and power measurements is detailed in Section 8.3 of the Appendix.

Table 8 summarizes the measured efficiency at different loading conditions.

DC Input Voltage (V_{IN})	Input DC Current (A)	Input Power (W)	Average Phase Current (A_{RMS})	$I_{PHASE-U}$ (A_{RMS})	$I_{PHASE-V}$ (A_{RMS})	$I_{PHASE-W}$ (A_{RMS})	Inverter Output Power (W)	Power Loss (W)	Inverter Efficiency (%)
340	0.206	62.0	0.320	0.317	0.321	0.323	60.6	1.46	97.6
340	0.409	136	0.549	0.555	0.55	0.543	133	2.50	98.2
340	0.627	211	0.822	0.826	0.812	0.828	208	3.18	98.5
340	0.840	284	1.10	1.13	1.10	1.08	279	4.38	98.5
340	1.05	357	1.38	1.43	1.37	1.36	352	5.69	98.4
340	1.26	429	1.64	1.69	1.63	1.62	422	7.50	98.3
340	1.48	503	1.92	1.96	1.90	1.90	494	9.10	98.2
340	1.74	591	2.26	2.29	2.25	2.24	579	12.0	98.0
340	2.04	694	2.62	2.66	2.58	2.61	678	15.5	97.8
340	2.29	777	2.90	2.96	2.89	2.87	758	19.2	97.5

Table 8 – Efficiency Table.

7.4.1 Efficiency Performance Graphs

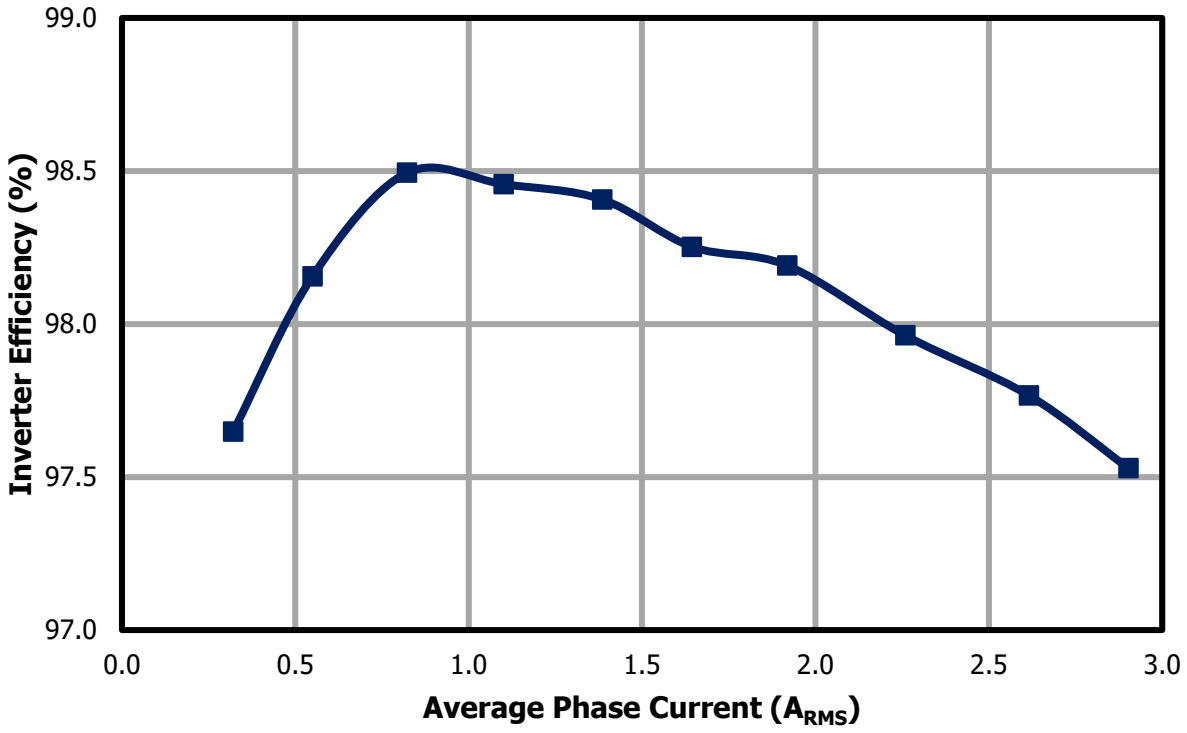

Figure 36 – Inverter Efficiency vs. Phase Current.

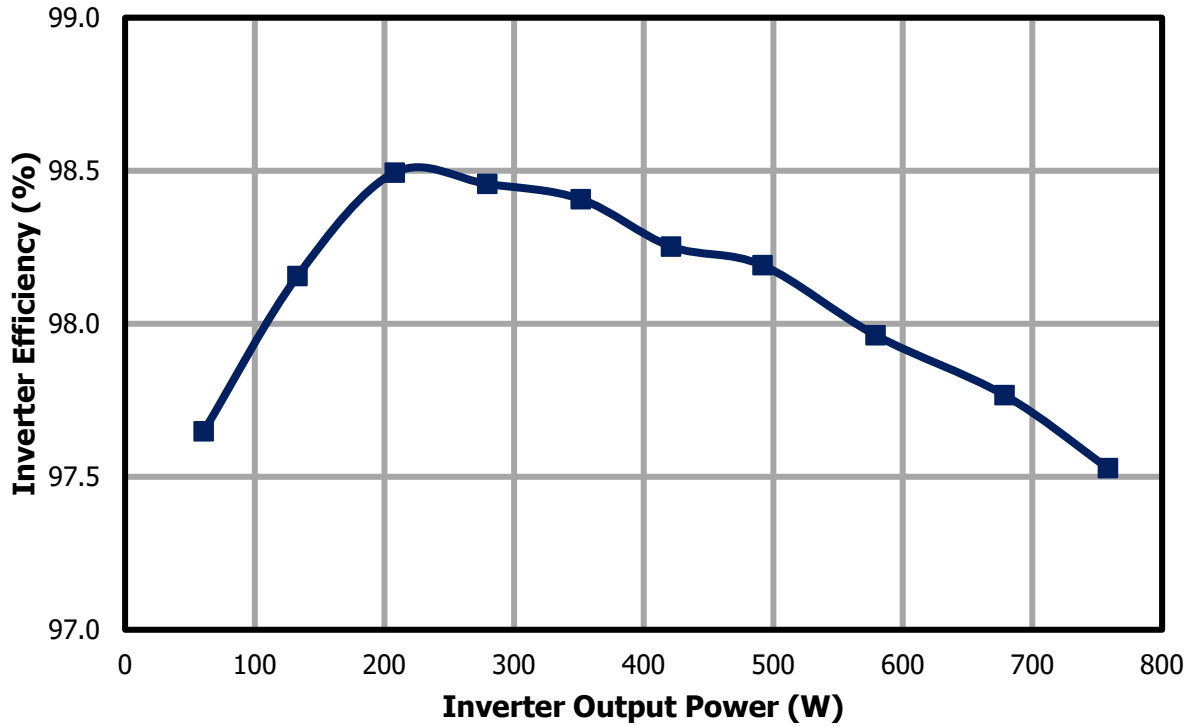

Figure 37 – Inverter Efficiency vs. Inverter Output Power.

7.5 Device and System Level Protection

The BridgeSwitch-2 device introduces an Error Flag pin to simplify fault handling in motor applications. Under normal operation, the EF pin remains HIGH. It is automatically pulled LOW in response to destructive faults, including overtemperature, overvoltage, and sustained overcurrent events. Pulling the EF pin LOW inhibits FREDFET switching on all devices. Switching remains disabled until the MCU issues a latch reset signal or the system undergoes a power reset. All EF pin waveform captures were taken using a voltage probe with a 100 nF capacitor across it.

Fault Protection	Remarks
Latching Overcurrent Protection (OCP)	• Applies only to the low-side FREDFET. • EF pin goes LOW after 16 consecutive low-side OC events. • SLP pull-down resistor should be set to 133 kΩ.
Overvoltage Protection (OVP)	• EF pin goes LOW when bus voltage exceeds the OV threshold. • EF pin returns HIGH once bus voltage drops below $OV_{THRESHOLD}$ - $OV_{HYSTERESIS}$.
Overtemperature Protection (OTP)	• EF pin goes LOW when junction temperature reaches the thermal shutdown threshold (T_{SD}). • **Hysteretic OTP** (R_{SLP} = 9.53 kΩ): – EF pin returns HIGH once junction temperature drops below the restart threshold (T_{RES}). • **Latching OTP** (R_{SLP} = 133 kΩ or OPEN): – EF pin latches OFF until either an EF latch reset from the MCU or a power recycle occurs, re-enabling FREDFET switching.

Table 9 – Error Flag Response.

7.5.1 Cycle-by-Cycle Overcurrent Protection (OCP)

The current limiting function of the BridgeSwitch-2 device is demonstrated below by increasing the open-loop duty cycle during the start-up phase. For the first set of waveforms, the default current limit of 7.0 A_{PK} was maintained. Minor clipping of the phase current can be observed on Figure 38 as the phase current slightly exceeds the current limit. With the current limit decreased to 44% of its default value (2.94 A_{PK}), the clipping becomes more apparent as seen on Figure 39.

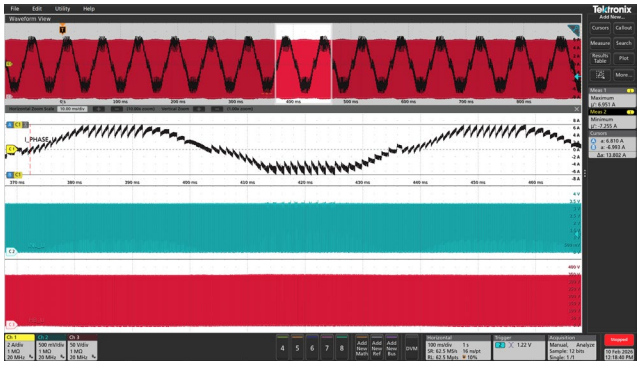

Figure 38 – Overcurrent Operation, I_{LIM} = 7.00 A.
CH1: I_{PHASE_U}, 2 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
Time Scale: 100 ms/div.
Time Scale (Zoom): 10 ms/div.

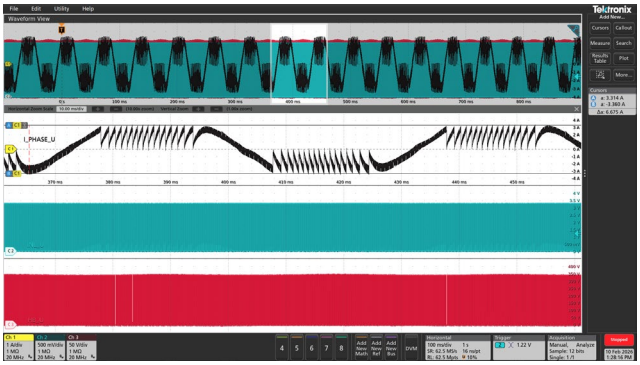

Figure 39 – Overcurrent Operation, I_{LIM} = 2.94 A.
CH1: I_{PHASE_U}, 2 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
Time Scale: 100 ms/div.
Time Scale (Zoom): 10 ms/div.

7.5.2 Over-temperature Protection

The succeeding waveforms below depict the low-side FREDFET over-temperature shutdown. An external heat source was applied to a single BridgeSwitch-2 device increasing the case temperature to the thermal shutdown threshold (150 °C).

7.5.2.1 Hysteretic Thermal Shutdown

The default SLP resistor (9.53 kΩ) sets the thermal shutdown response to hysteretic. This allows the inverter to restart switching once the device temperature drops below the hysteresis level. The EF bus inhibits switching for all devices when pulled LOW and automatically goes HIGH once the device temperature is within the safe operating range.

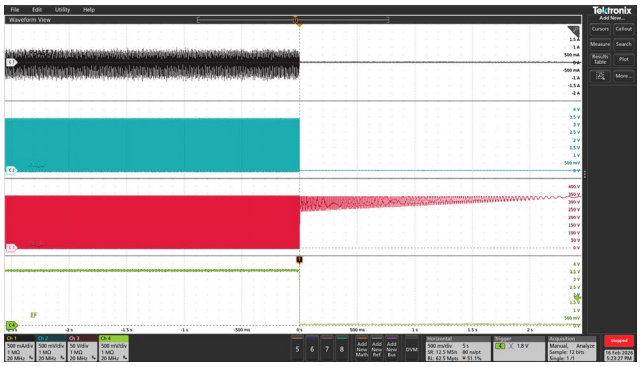

Figure 40 – Hysteretic Thermal Shutdown.
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 1 ms/div.

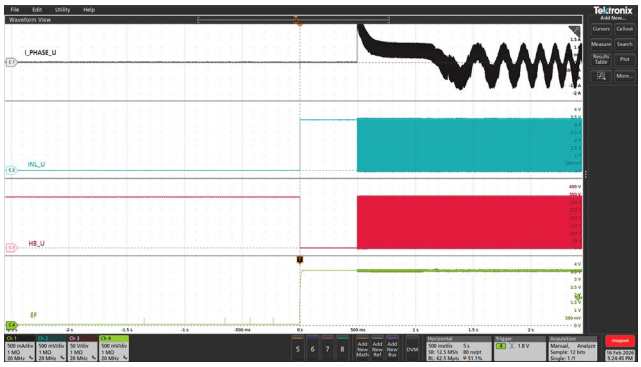

Figure 41 – Hysteretic Thermal Shutdown Reset.
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 1 ms/div.

7.5.2.2 Latching Thermal Shutdown

Depopulating the SLP programming resistor (≥1 MΩ) or replacing it with a 133 kΩ resistor sets the thermal shutdown response to latching. Shown below is the latching thermal shutdown response followed by an EF reset signal. For this configuration, switching is inhibited for all devices connected to the EF bus until either an EF reset signal is received, or a power recycle is performed.

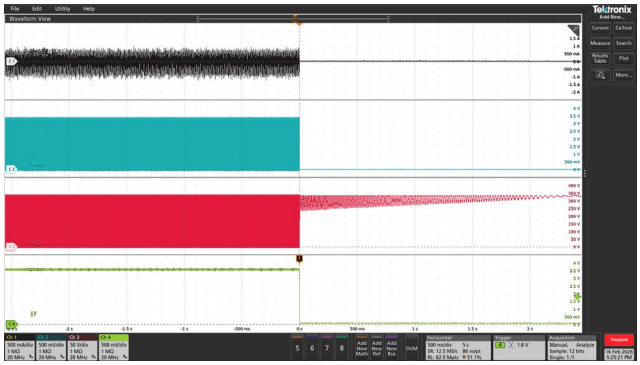

Figure 42 – Latching Thermal Shutdown.
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

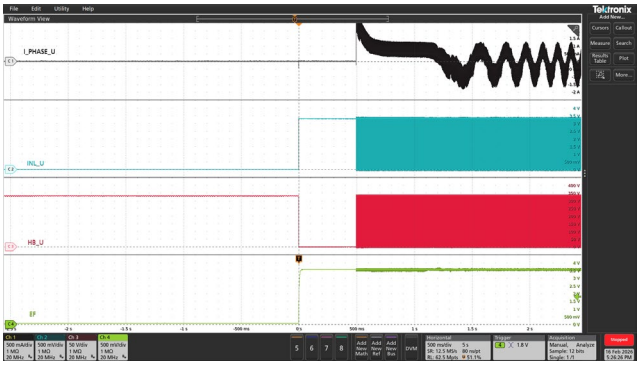

Figure 43 – Latching Thermal Shutdown Reset (via EF Reset Signal).
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

7.5.3 Overvoltage Protection (OVP)

The waveforms below depict the bus voltage monitoring feature with the overvoltage threshold set to 362 VDC through the total resistance value of components R21, R22, and R23 (6 MΩ). Device switching is inhibited when the EF pin voltage is pulled down after exceeding the overvoltage threshold. Switching resumes once the bus voltage level drops below the overvoltage hysteresis level, automatically pulling the EF voltage HIGH.

Due to the common EF connection between the BridgeSwitch-2 devices, all device switching is inhibited ensuring reliable protection against destructive faults. A full start-up cycle is required to resume normal operation afterwards.

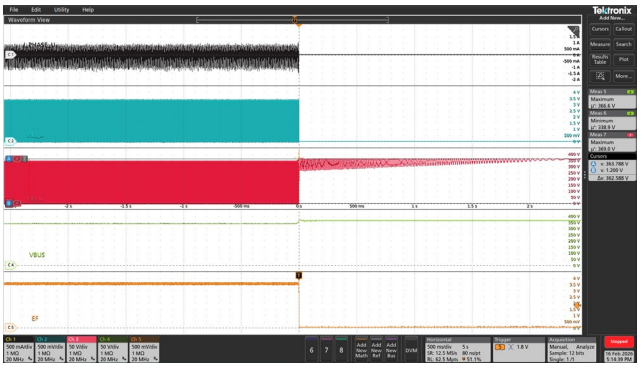

Figure 44 – OVP, 340 V to 365 V.
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{BUS}, 50 V/div.
CH5: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

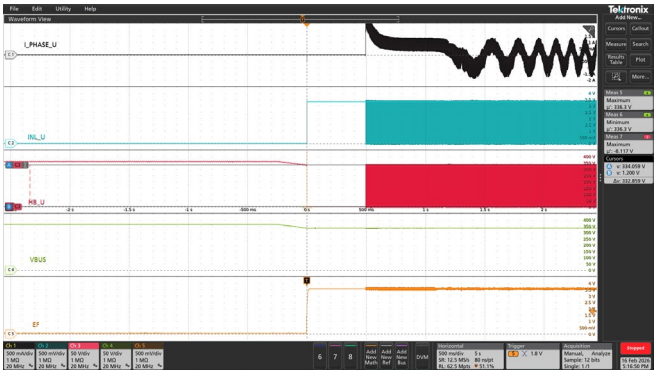

Figure 45 – OVP Clear, 362 V to 330 V.
CH1: I_{PHASE_U}, 0.5 A/div.
CH2: V_{INL_U}, 0.5 V/div.
CH3: V_{HB_U}, 50 V/div.
CH4: V_{BUS}, 50 V/div.
CH5: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

7.6 Abnormal Motor Operation Test

This section presents the abnormal operation test results for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). It includes the following tests:

- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

The test results demonstrate the integrated protection features of the BridgeSwitch-2 device under these abnormal conditions.

7.6.1 Operation under Stalled Motor Conditions

For this test, the inverter was set to initially run at 340 VDC, with a phase current of 1.1 A_{RMS} and 2.2 A_{RMS}, and a motor speed of 2000 RPM. After steady-state conditions are achieved, the load was increased drastically to simulate sudden braking of the motor. Once the motor stalls, the overcurrent protection of the BridgeSwitch-2 device engages, and no damage is observed on both the inverter board and the motor. The resulting waveforms are shown below:

Stalled Condition at 1.1 A_{RMS} Load

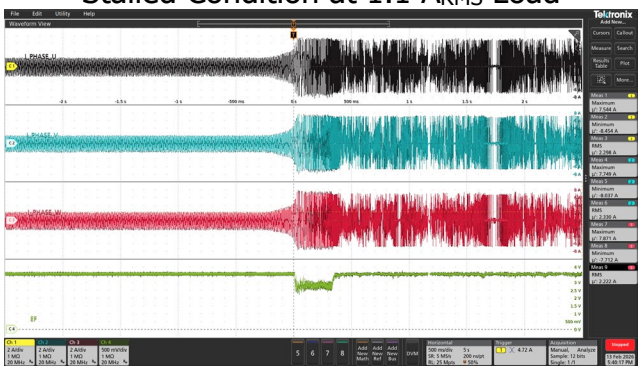

Figure 46 – Stalled Motor Condition, 1.1 A_{RMS} Load.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

Stalled Condition at 2.2 A_{RMS} Load

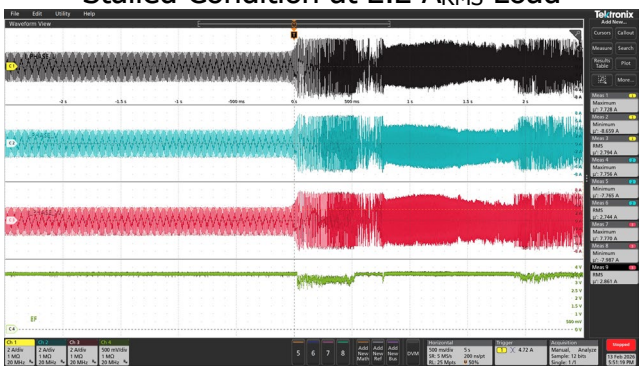

Figure 47 – Stalled Motor Condition, 2.2 A_{RMS} Load.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

7.6.2 Operation with One Motor Winding Disconnected

For this test, the inverter was set to initially run at 340 VDC, with a phase current of 1.1 A_{RMS} and 2.2 A_{RMS}, and a motor speed of 2000 RPM. After steady-state conditions are achieved, one motor winding is disconnected through a switch.

At 1.1 A_{RMS} load, motor operation continues with increased phase current levels on the remaining motor phases. Reconnecting the motor winding reverts the operating conditions back to its initial state.

At 2.2 A_{RMS} load, the overcurrent protection is triggered after disconnecting one phase causing the motor to stall. The full start-up sequence is required after reconnection to run the motor normally. No damage was incurred by both the BridgeSwitch-2 inverter board and motor during and after this test.

Phase U Disconnected at 1.1 A_{RMS} Load

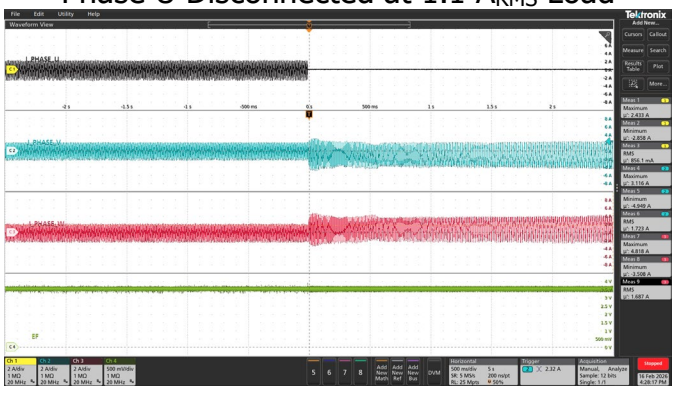

Figure 48 – Motor Winding Disconnection, 1.1 A_{RMS} Load.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

Phase U Reconnected at 1.1 A_{RMS} Load

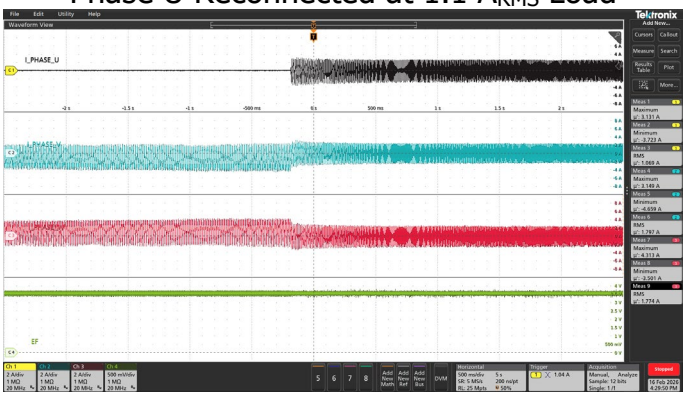

Figure 49 – Motor Winding Reconnection, 1.1 A_{RMS} Load.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

Phase U Disconnected at 2.2 A_{RMS} Load

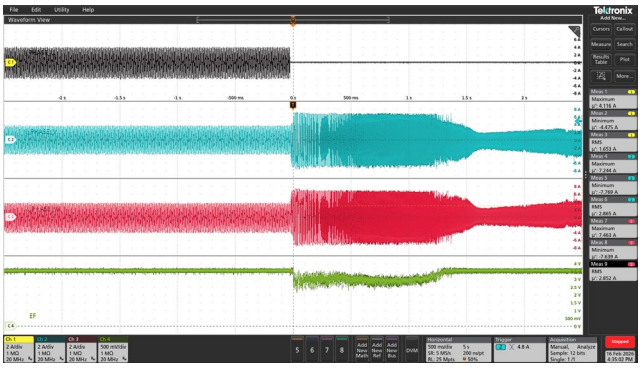

Figure 50 – Motor Winding Disconnection, 2.2 A_{RMS} Load.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

Note: At 2.2 A_{RMS} load, the motor stalls after one motor winding is disconnected and maintains its stalled condition after the motor winding is reconnected.

7.6.3 Running Overload Test

The running overload test is performed by gradually increasing the current through the motor windings until the motor stalls. For this test, the increase is done in ten percent increments and steady-state conditions are achieved each time. This is repeated until the motor stops spinning.

Figure 51 displays the motor phase currents at the overloaded conditions until the motor stalls. No damage is incurred by both the BridgeSwitch-2 inverter board and motor during and after this test.

Running Overload Test > 3.5 A_{rms}

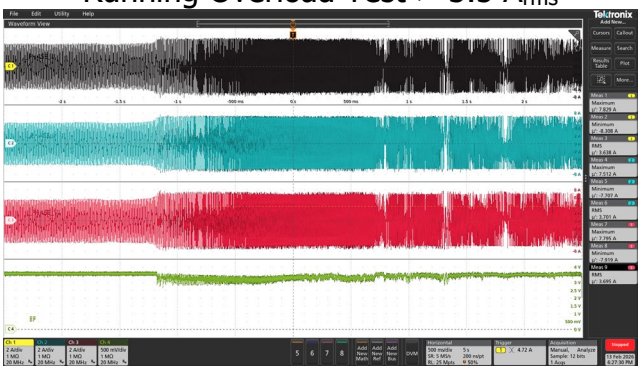

Figure 51 – Running Overload Test.
CH1: I_{PHASE_U}, 2 A/div.
CH2: I_{PHASE_V}, 2 A/div.
CH3: I_{PHASE_W}, 2 A/div.
CH4: V_{EF}, 0.5 V/div.
Time Scale: 500 ms/div.

8 Appendix

8.1 Board Quick Reference

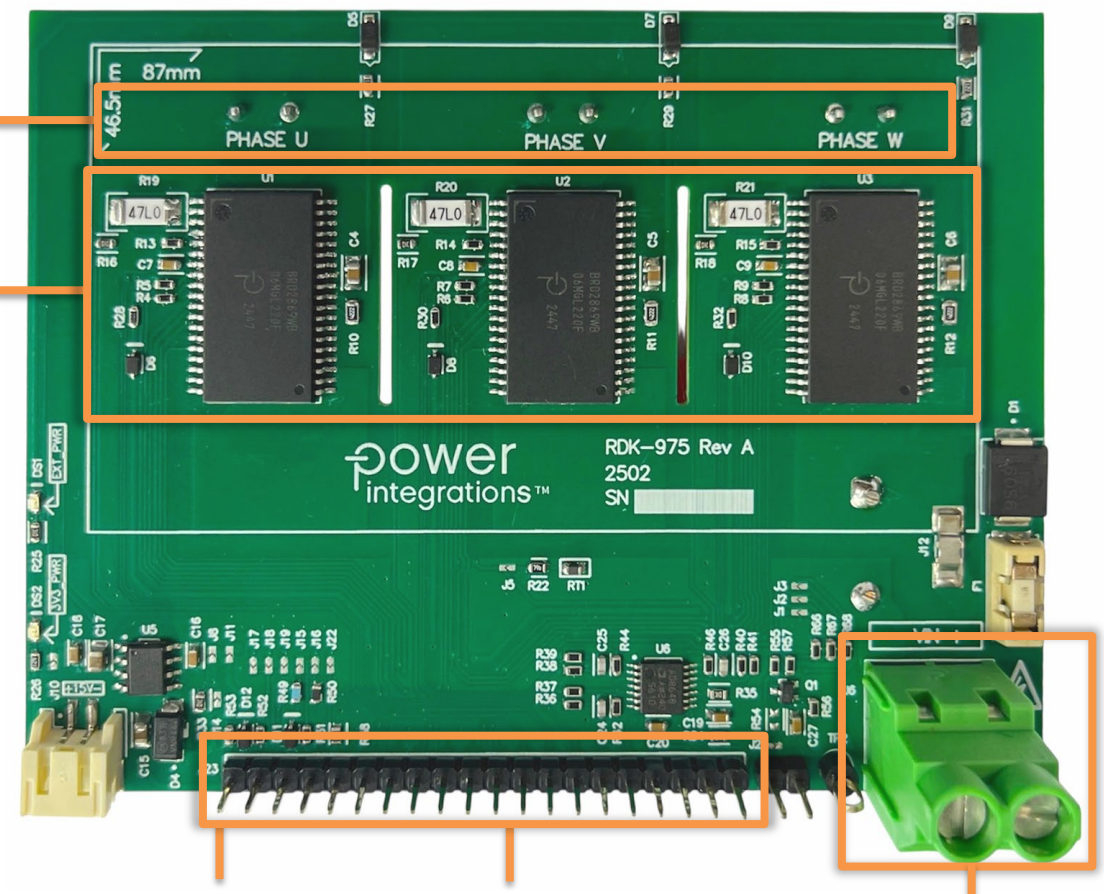

Figure 52 – RDK-975 Board Quick Reference.

8.1.1 Microcontroller (MCU) Interface Pins Designation

Pin No.	Pin Name	Pin Type	Pin Description
1	VBUS_SENSE	Output	Voltage divider output for high-voltage DC bus sensing (scale-down factor: 0.0055).
2	3V3	Power Input	3.3 V microcontroller supply input.
3	SM_W	Input	Optional SM pin input for Phase W (U3).
4	SENSE_CURRENT_W	Output	Phase W (U3) R_{SHUNT} voltage amplifier output.
5	SENSE_CURRENT_V	Output	Phase V (U2) R_{SHUNT} voltage amplifier output.
6	SENSE_CURRENT_U	Output	Phase U (U1) R_{SHUNT} voltage amplifier output.
7	IPH_W	Output	Phase W (U3) IPH output.
8	IPH_V	Output	Phase V (U2) IPH output.
9	IPH_U	Output	Phase U (U1) IPH output.
10	INH_W	Input	Phase W (U3) high-side FREDFET PWM control signal.
11	INL_W	Input	Phase W (U3) low-side FREDFET PWM control signal.
12	INH_V	Input	Phase V (U2) high-side FREDFET PWM control signal.
13	INL_V	Input	Phase V (U2) low-side FREDFET PWM control signal.
14	INH_U	Input	Phase U (U1) high-side FREDFET PWM control signal.
15	INL_U	Input	Phase U (U1) low-side FREDFET PWM control signal.
16	GND	MCU Ground	Microcontroller ground reference.
19	EF_BUS	Open-drain, I/O	Error Flag state monitoring. Pulling this low inhibits FREDFET switching for BridgeSwitch-2 devices with EF functionality.
20	EF_RST	Input	Error Flag reset signal. Momentarily pulling this pin high re-enables device switching after a latching fault.

Table 10 – J23 Connector Pin Designation.

Note: Pin labels are located on the bottom-layer silkscreen of the board.
Pins 17 and 18 are not used

8.1.2 Board Jumpers Configurations

Board Section		Jumpers Configuration

Inverter Section	Phase U	• Default: **J4** = SHORTED, **J1** = OPEN
		  ○ Phase U is configured for OV/UV sensing
		• If **J4** = OPEN, **J1** = SHORTED:
		  ○ Phase U is connected to **SM_BUS**

	Phase V	• Default: **J5** = SHORTED, **J2** = OPEN
		  ○ Phase V is configured for system thermal monitoring
		• If **J5** = OPEN, **J2** = SHORTED:
		  ○ Phase V is connected to **SM_BUS**

	Phase W	• Default: **J3** = OPEN • If **J3** = SHORTED: ○ Phase W is connected to **SM_BUS**
Power Section	Input	• Default: **J12** = OPEN • If J12 = SHORTED: ○ Input Fuse and Input Diode is bypassed
	15 V Auxiliary Supply	• Default: **J7** = SHORTED, **J8** = SHORTED • **If J7** = OPEN, **J8** = OPEN, ○ External 15VDC supply connected to J9 is used to supply bias voltage

	3.3 V LDO	• Default: **J10** = SHORTED
		  ○ Onboard LDO is used
		• If **J10** = OPEN:
		  ○ External 3.3V/5V supply from a MCU is used

SLP Pin Programming	SLP Pin Programming	• Default: **J15** = SHORTED, **J16** = OPEN
		  ○ LS OCP configured as cycle-by-cycle
		  ○ OTP configured as warning & hysteretic
		• If **J15** = OPEN, and **J16** = SHORTED:
		  ○ LS OCP configured as Latching
		  ○ OTP configured as warning & latching
		• If **J15** = OPEN, and **J16** = OPEN:
		  ○ LS OCP configured as cycle-by-cycle
		  ○ OTP configured as warning & latching

Error Flag Circuit	Error Flag (EF) Feature	• Default: **J17**, **J18**, and **J19** = SHORTED ○ All EF pins are connected to EF_BUS which allows one phase to inhibit switching of all the other phases

Table 11 – RDK-975 Jumpers Configurations.

Note: All other Jumpers are **OPEN** by default

8.2 Schematic – Showing Optional Circuit and Component Positions

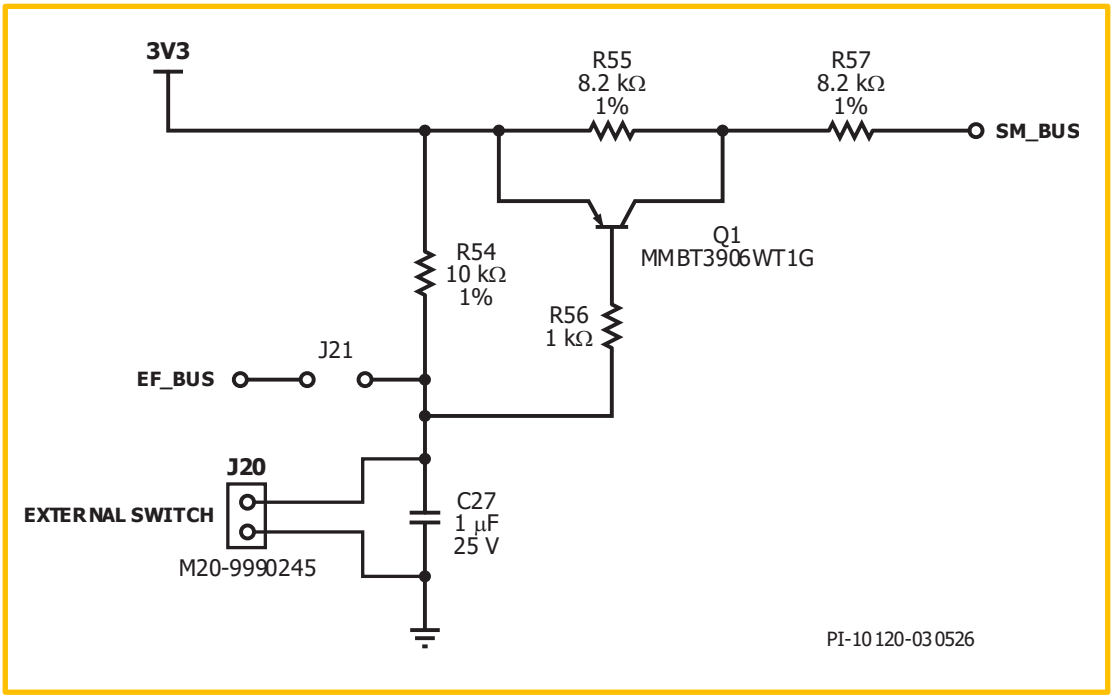

Figure 53 – External Inhibit Circuit.

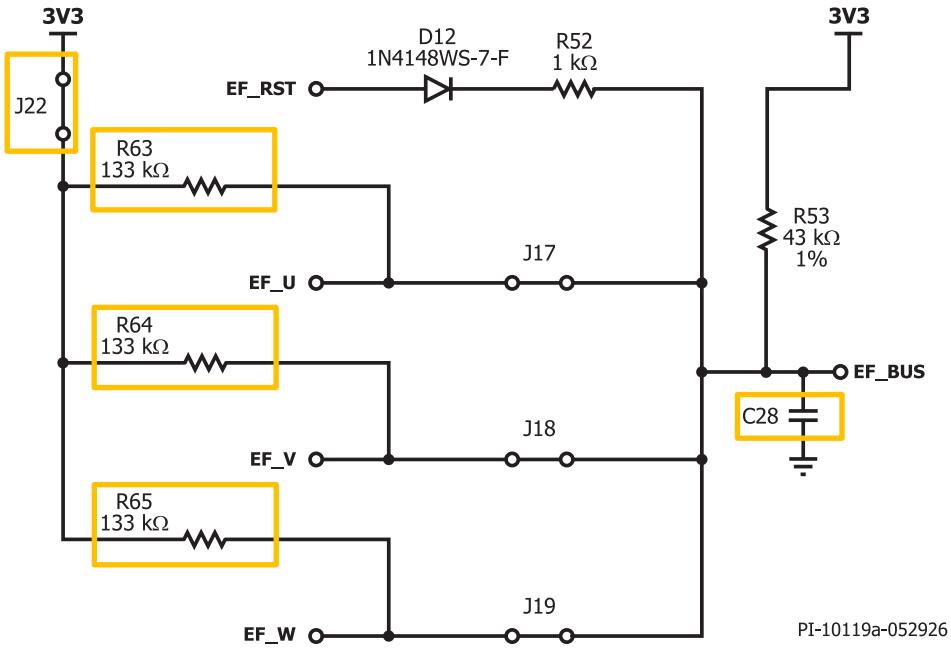

Figure 54 – Error Flag Circuit Complete Schematic.

The components and connections highlighted in Figures 53 and 54 are optional.

- J17, J18, J19, J22, R63, R64, R65 – Used for individual BridgeSwitch-2 Error Flag (EF) evaluation. To enable this feature, short J22. To evaluate a specific phase, short the corresponding jumper: J17 for Phase U, J18 for Phase V, and J19 for Phase W.

- C28 – Provision for a noise filter to improve EF signal integrity to the MCU.

- R54, R55, R56, R57, Q1, C27, J20 and J21 – Used for external inhibit function. This is an extended feature that utilizes the BridgeSwitch-2 EF and SM pins. An external switch can be connected to J20 to inhibit switching. Component configurations for the circuit are shown at Table 12.

External Inhibit Circuit Function	Component Configuration	Description
SM Pin Inhibit	R54, R55, R56, R57, Q1, C27, J20 (connected to external switch), J21 (open)	When the external switch is shorted, it simulates the current through the SM pin corresponding to an over-voltage (OV) condition. Pre-requisite for this function is to connect SM pin of each BridgeSwitch-2 device to the SM_BUS. J1, J2, and J3 need to be shorted.
EF Inhibit	R54 (Do not Populate), R55, R56, R57, Q1, C27, J20 (connected to external switch), J21 (shorted)	When the external switch is shorted, switching of BridgeSwitch-2 devices are inhibited by pulling the Error Flag (EF) signal down. Pre-requisite for this function is to connect EF pin of each BridgeSwitch-2 device to the EF_BUS. J17, J18, and J19 need to be shorted.

Table 12 – External Inhibit Circuit Configurations.

8.3 Inverter Output Power Measurement

A six-channel power analyzer (WT1806E) was used to measure inverter power and efficiency. Figure 55 shows the output power meter connections in a three-wattmeter configuration, enabling phase current measurements for all motor phases. The third motor phase was used as the voltmeter reference for the other two phases, eliminating the need for a false neutral node and providing a total output power calculation equivalent to the two-wattmeter method.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

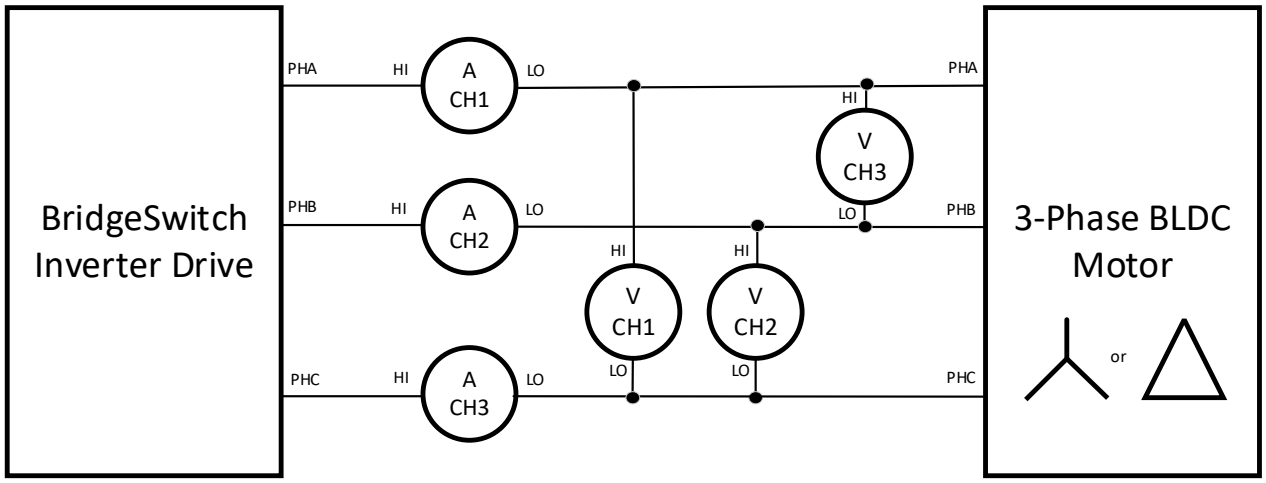

Figure 55 – Inverter Output Power Measurement (Three-wattmeter Setup).

Alternatively, the two-wattmeter setup shown in Figure 56 simplifies connections and reduces the number of required power meter channels, while providing readings comparable to the three-wattmeter method.

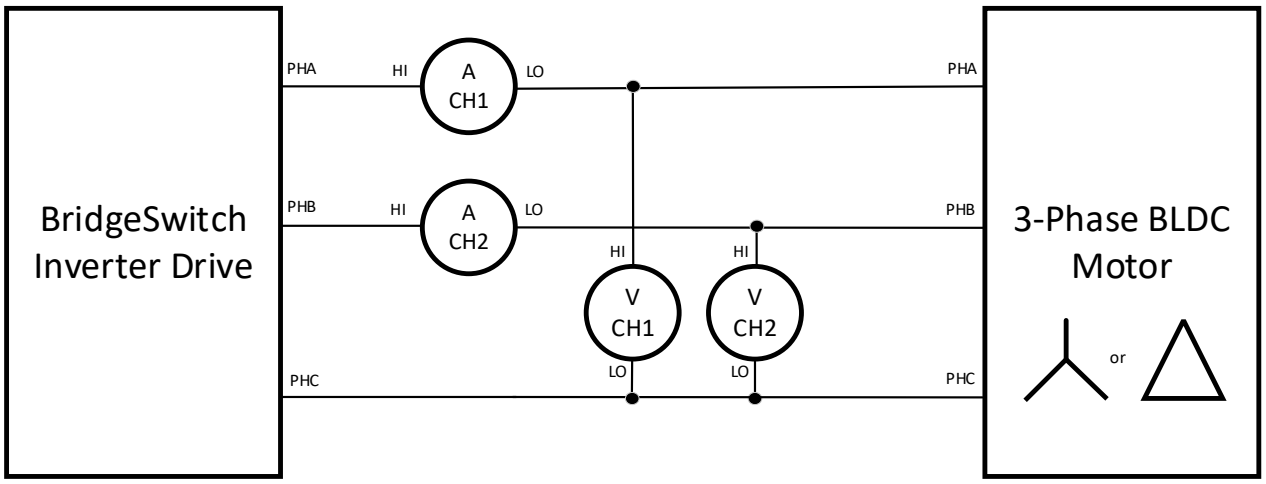

Figure 56 – Inverter Output Power Measurement (Two-wattmeter Setup).

8.4 IPH Reconstruction by the MotorXpert Suite 3.0

The instantaneous phase current (IPH) output, shown in Figure 57, provides a low-voltage signal proportional to the positive half-cycle of the current through the low-side power FREDFET. For field-oriented control applications, a reconstruction algorithm is required to derive the negative half-cycle of the phase current for use as current feedback.

Figure 57 – IPH Signals before Current Reconstruction.

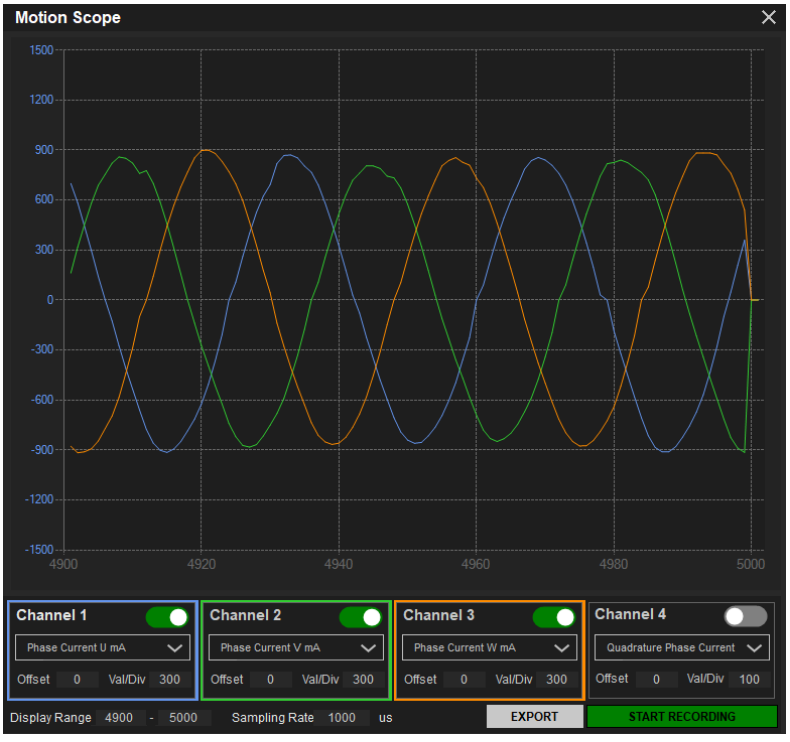

Figure 58 – Phase Current Output after Current Reconstruction.

Figure 58 illustrates the phase current output reconstructed from the trigonometric relationships of the phase current signals. Since the IPH signals provide only the positive half-cycle, the reconstruction restores the negative half-cycle, effectively doubling the data resolution and improving current control. This reconstruction can be readily performed using MotorXpert Suite 3.0.

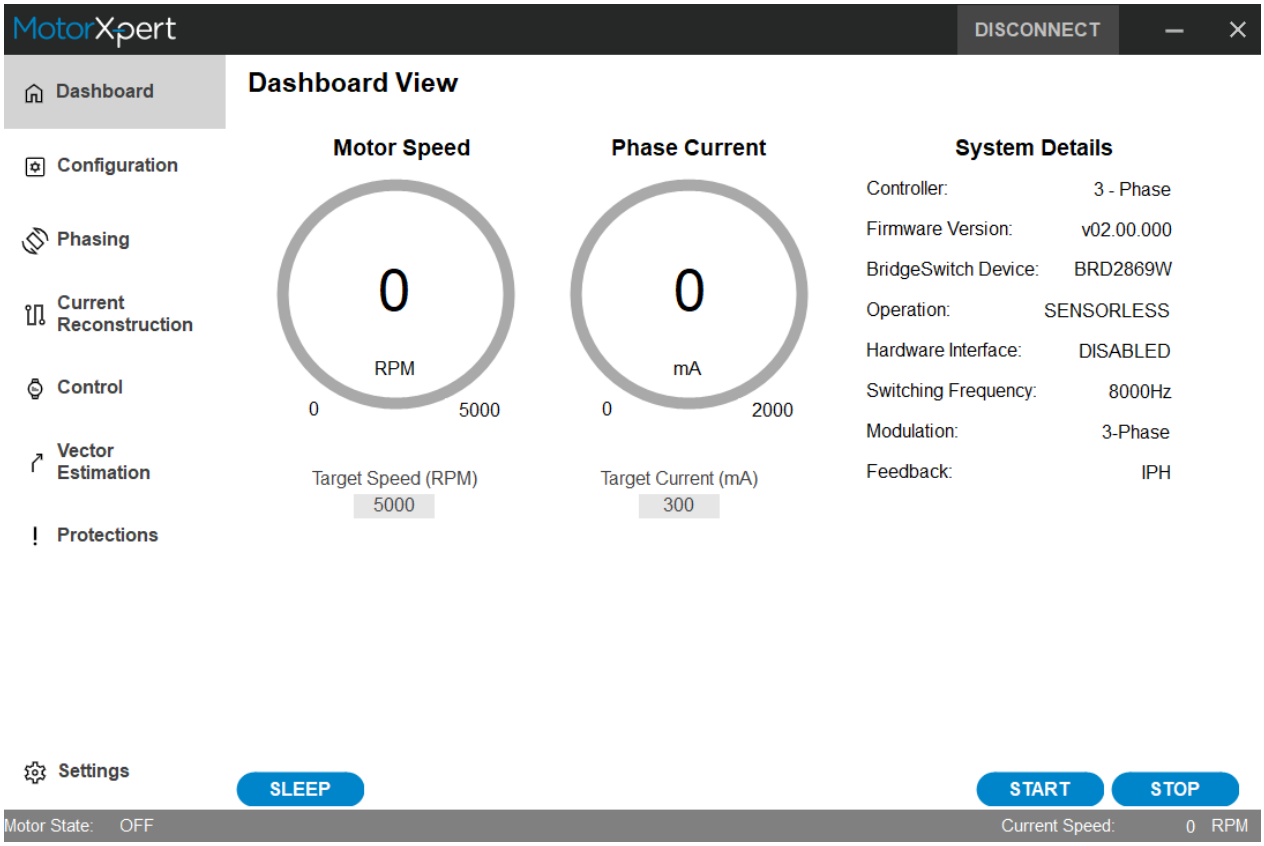

Figure 59 – MotorXpert Suite Dashboard.

For more information on the MotorXpert Suite, visit: https://www.power.com/design-support/motorxpert-suite-bridgeswitch

8.5 Error Flag (EF) Configuration

This reference design supports the Error Flag of the BridgeSwitch-2 devices. EF signal is normally HIGH and require an external pull-up to the microcontroller supply voltage (3.3 V or 5 V).

8.5.1 Error Flag (EF) Signal

It remains HIGH during normal operation and is automatically pulled LOW during destructive faults. While LOW, the EF signal inhibits FREDFET switching for all BridgeSwitch-2 devices connected to the EF bus. Additionally, the microcontroller can intentionally pull the EF bus LOW to disable inverter operation.

Table 13 summarizes the status changes flagged by each EF pin.

Fault Conditions	Error Flag (Default)
HV Bus OV	✓
LS Device Shutdown (OTP, Latching OCP)	✓
LS FET Latching Overcurrent	✓

Table 13 – Error Flag Bus Triggers.

8.6 Test Bench Set-up

Figure 60 illustrates the RDK-975 board connections to the high-voltage DC supply and microcontroller unit. An interface board was designed to enable direct signal connections between the MCU and the inverter board.

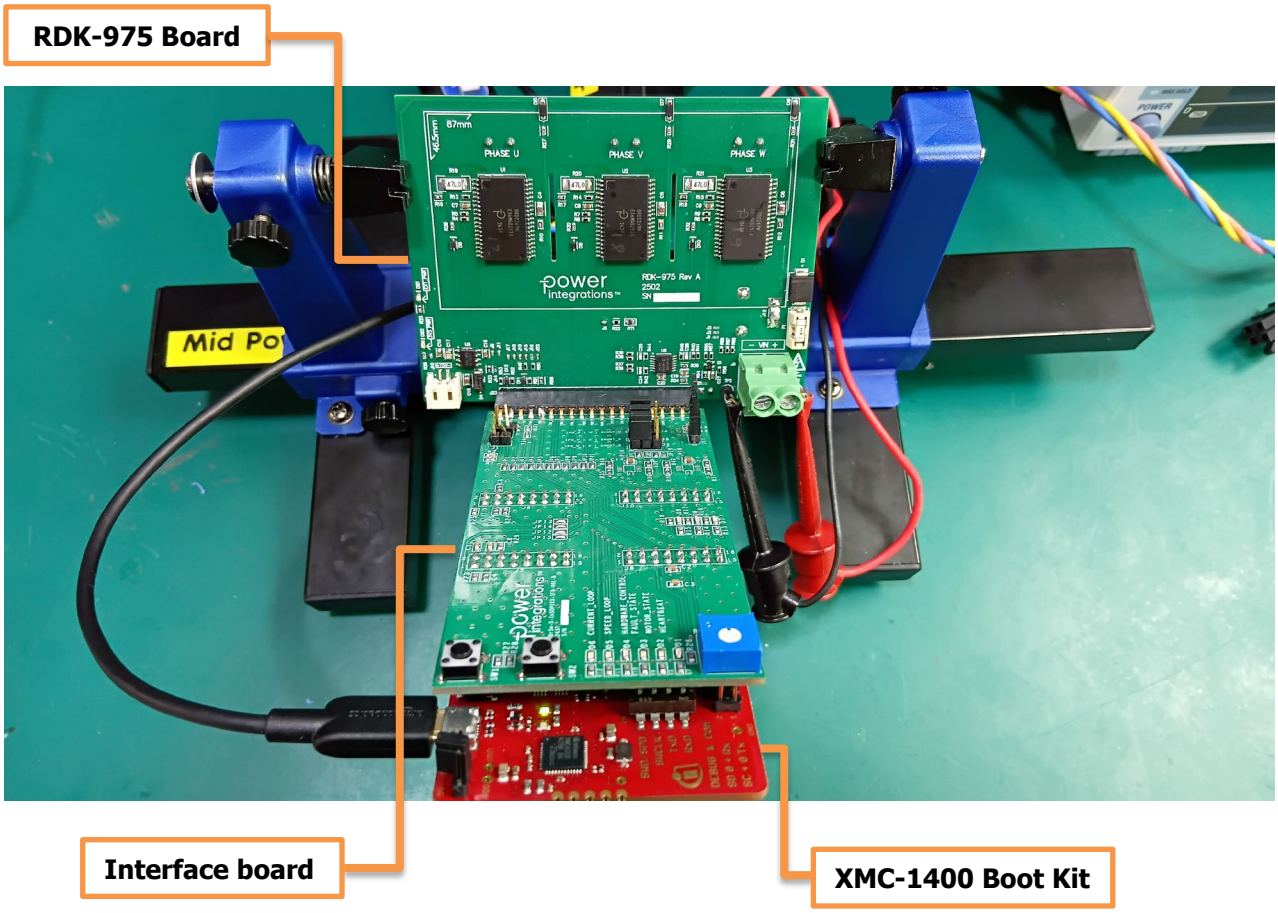

Figure 60 – RDK-975 Board with Microcontroller.

The setup shown in Figure 61 ensures accurate temperature and efficiency measurements for the board under test. An acrylic case was used to minimize the influence of ambient airflow on the performance data.

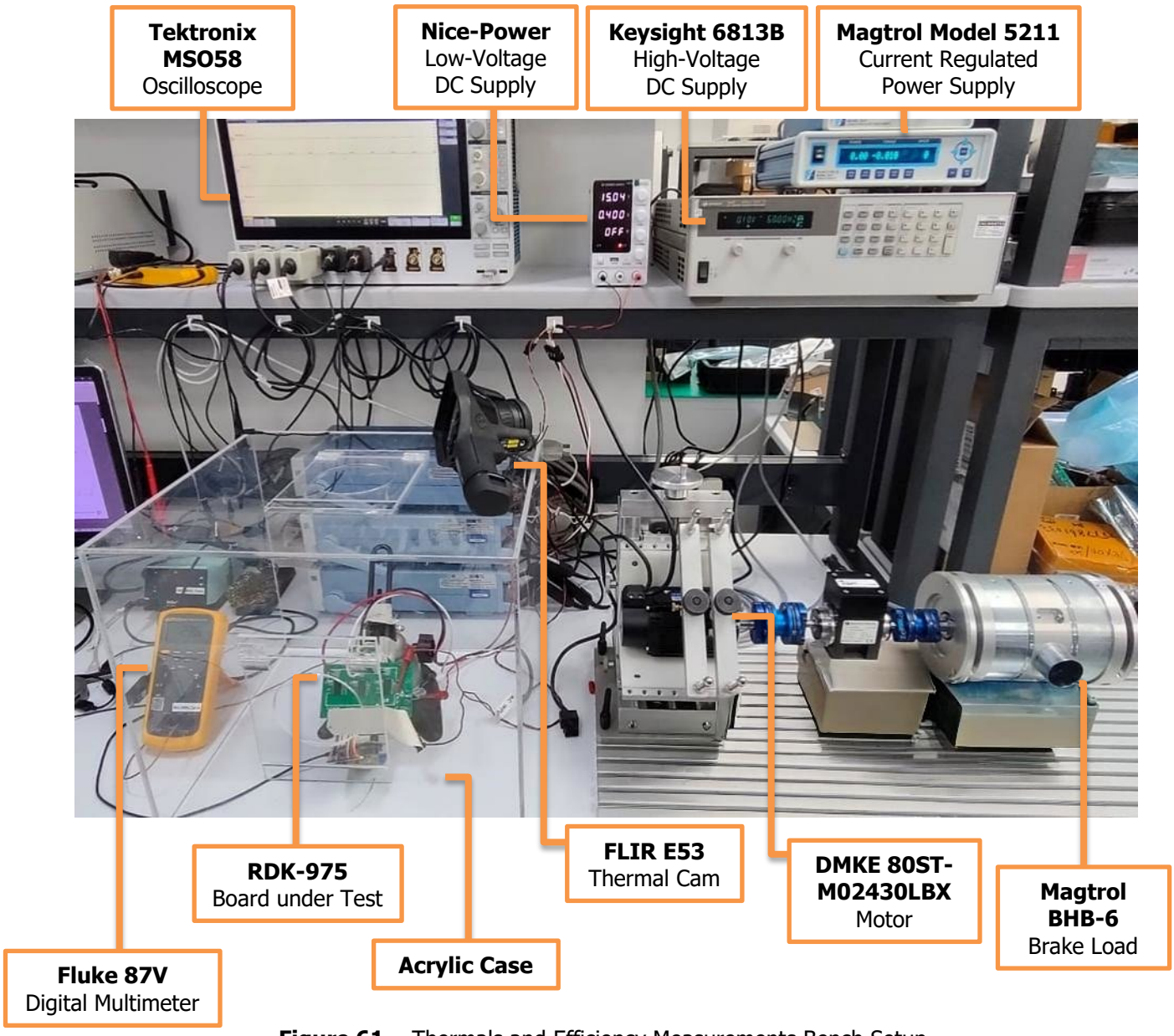

Figure 61 – Thermals and Efficiency Measurements Bench Setup.

8.6.1 Equipment Used

1. **Tektronix MSO58** (Oscilloscope) – 350 MHz, 6.25 GS/s resolution
2. **Nice-Power** (Low-Voltage DC Supply) – 30 VDC, 10 A maximum output
3. **Keysight 6813B** (High-Voltage DC Supply) – 300 V_{RMS}, 1750 VA rated
4. **Magtrol Model 5211** (Current Regulated Power Supply) – 24 VDC, 0 to 1000 mA output
5. **Fluke 87V** (Digital Multimeter) – -200 °C to 1090 °C temperature range
6. **FLIR E53** (Thermal Camera) – 40 mK thermal sensitivity, -20 °C to 650 °C temperature range
7. **DMKE 80ST-M02430LBX** (Motor) – 750 W, 220 V, 3 A, 3000 RPM rated
8. **BHB-6** (Brake Load) – 24 VDC, 1.5 A, 20,000 RPM rated
9. **WT1806E** (Precision Power Analyzer) – 6-channel, 2 MS/s (16 bits), 0.1 Hz to 1 MHz measurement bandwidth

9 Revision History

Date	Author	Revision	Description & Changes	Approval
19-Mar-26	MQC, ACD	A	Initial Release.	Apps & Mktg
03-Jun-26	MQC, ACD	B	Updated Schematic.	Apps & Mktg

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