Reference Design Report

Title	**46 W Power Supply with 80 W Peak Power Using InnoSwitch3™-AQ INN3990CQ with PowiGaN™**
Specification	100 VDC – 150 VDC Input; 12 V / 3.84 A Nominal Output Current with 6.67 A Peak Output Current
Application	Solar Race Car Auxiliary Power Supply
Author	Applications Engineering Department
Document Number	RDR-85SLR
Date	July 24, 2025
Revision	A

Summary and Features

- Low component count (only 51 electrical components)
- Nominal and peak output power delivery from 100 VDC to 150 VDC input
- ≥95% full load efficiency across the input voltage range
- Built in synchronous rectification for high efficiency
- Secondary-side control without optocouplers
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface mounted (SMD) components
- Low profile, only 30 mm high

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Disclaimer:

The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. Parameters, numbers, values, and other technical data included in the technical information were calculated and determined, to our best knowledge, to be in accordance with the relevant technical norms (if any). They may be based on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein.

No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations, or opinions communicated and any liability for any direct, indirect, or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

1 Introduction

This document is an engineering report describing a 46 W single-output power supply delivering up to 80 W peak power for use as an auxiliary power supply for a solar race car. The design supports an input range of 100 VDC to 150 VDC.

This design uses the 900 V rated PowiGaN switch INN3990CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration, and is itself based on RDR-85SLR.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides by observing the creepage and clearance requirements according to IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic, printed circuit board (PCB) layout, bill of materials (BOM), specification for the magnetics, and performance data.

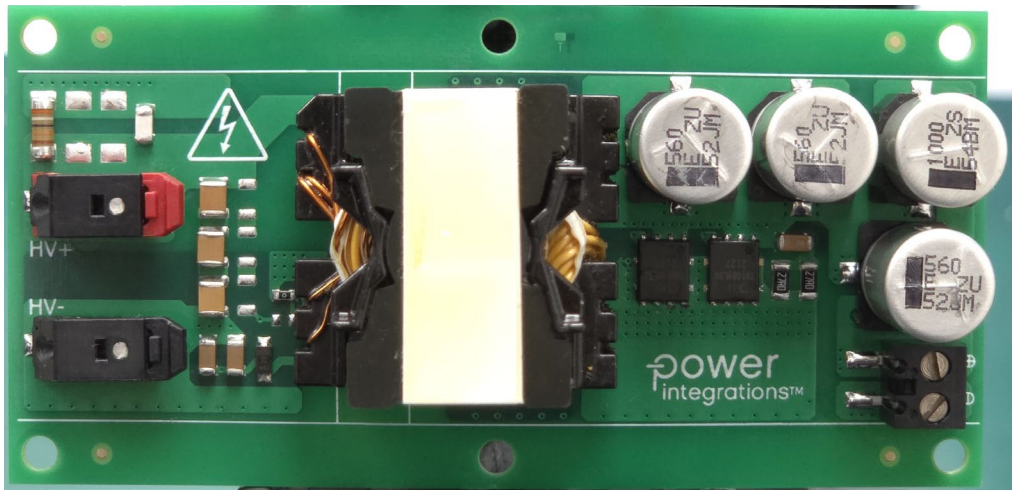


Figure 1 – Populated Circuit Board, Top.

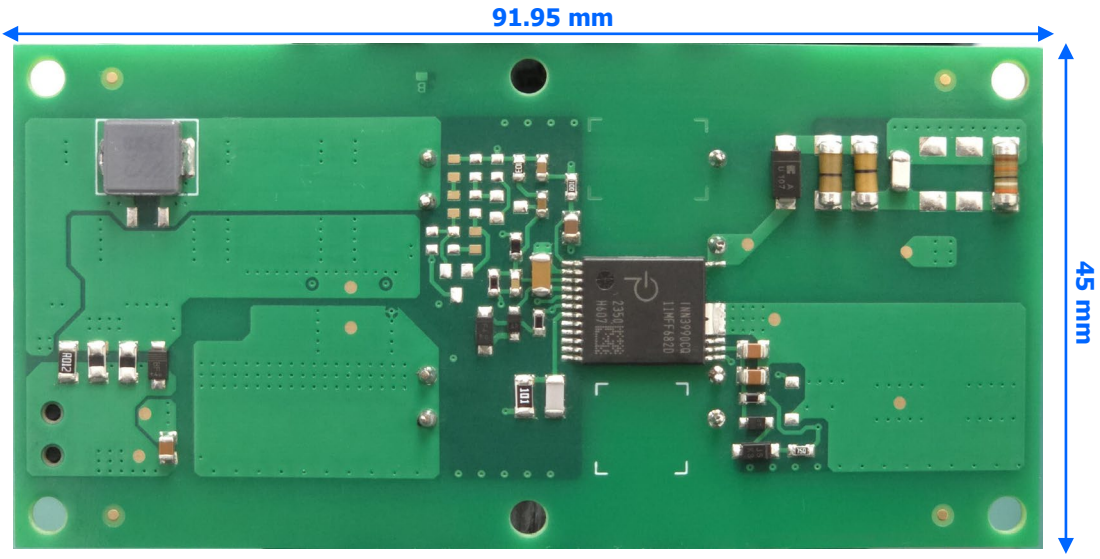


Figure 2 – Populated Circuit Board, Bottom.

2 Design Specification

The following tables represent the performance requirement for the design.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	V_{INPUT}	100	120	150	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	11.4	12.0	12.6	VDC
Ripple Voltage Measured on Board	V_{RIPPLE}			150	mV
Output Current Parameters					
Nominal Output Current	I_{OUT_NOM}		3.84		A
Peak Output Current	I_{OUT_PEAK}		6.67		
Output Power Parameters					
Continuous Output Power	P_{OUT_NOM}		46.0		W
Peak Output Power	P_{OUT_PEAK}		80.0		
Operating Temperature					
Ambient Temperature	T_{AMB}	0		50	°C

Table 1 – Electrical Specifications.

3 Schematic

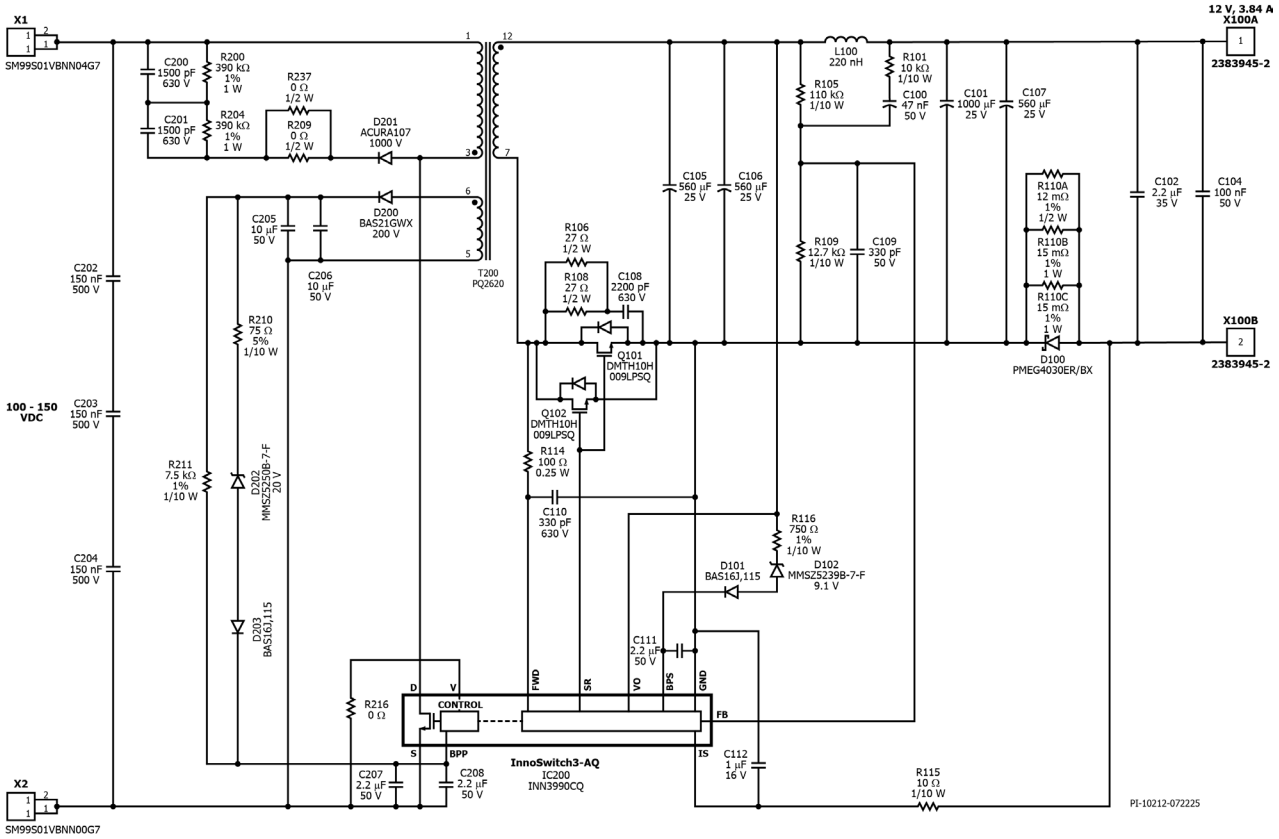


Figure 3 – RDR-85SLR Power Conversion Stage.

4 Circuit Description

4.1 Primary Section

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from a DC battery input. The flyback transformer T200 primary winding is connected between the DC input, with decoupling capacitors C202, C203, and C204, and the drain terminal of the PowiGaN power switch integrated into the InnoSwitch3-AQ IC (IC200).

An R2CD-type snubber circuit is placed across the primary winding to limit the drain-source voltage peaks during turn-off. A super-fast (or better) surface-mount, AEC-Q qualified diode should be used for the snubber. Diode D201 meets creepage and clearance requirements and ensures that the reverse voltage across the diode does not exceed 75% rating. Capacitors C200 and C201 store the energy from the leakage inductance of the transformer (T200). The capacitor values are selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation through the switching cycle. Resistors R200 and R204 dissipate the energy stored by the snubber capacitors. The resistor values are selected such that the snubber voltage will not exceed 80% of their voltage rating and to ensure that they will dissipate less than 50% of their rated power. Resistors R209 and R237 provide connection for the primary clamp, and their values can be adjusted to reduce the ringing in the primary drain-source voltage caused by leakage inductance.

The transformer auxiliary winding provides power to the primary-side of the InnoSwitch3-AQ IC during normal operation. This minimizes the power derived from the internal high-voltage current source, improving overall efficiency, and reducing heating of InnoSwitch3-AQ IC. The auxiliary winding output is rectified and filtered by diode D200 and capacitors C205 and C206. The InnoSwitch3-AQ IC is self-starting, using an internal high-voltage current source to charge the BPP capacitors (C207 and C208). Current is fed to the BPP pin through resistor R211. Diodes D203, D202, and resistor R210 serve as a primary-sensed output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) if the fault is present.

4.2 InnoSwitch3 Input Undervoltage Protection

The V pin of the InnoSwitch3-AQ IC is used to provide line undervoltage protection.

For this board, the V pin is disabled by connecting the pin to the input RTN by using jumper resistor R216.

4.3 Secondary Section

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q101 and Q102 rectify the voltage across the secondary winding of the transformer (T200), which is then filtered by output capacitors C105 and C106. Additional post filters

L100, C101, C104, and C107 are added to improve output ripple performance. An RC-type snubber formed by resistors R106 and R108 and capacitor C108 damps high-frequency ringing across the SR FET.

The secondary-side controller inside InnoSwitch3-AQ IC controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed from the FWD pin via resistor R114. Capacitor C110 and resistor R114 form a low pass filter that reduces the voltage spike seen by the FWD pin during SR turn-off and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode, the SR gate signal is turned off before the secondary-side controller requests a new switching cycle from the primary. In discontinuous conduction mode, the SR FET is turned off when the voltage across it rises above $V_{SR(TH)}$ (~-3.3 mV). Secondary-side control of the primary-side power MOSFET eliminates cross-conduction and ensures reliable operation.

The secondary-side of InnoSwitch3-AQ IC is powered by either the secondary winding forward voltage (thru R114 and the FWD pin) or the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C111 via an internal regulator.

Diodes D101, D102, and resistor R116 provide a secondary-side output overvoltage protection (secondary OVP). During output overvoltage events, current will be injected into the BPS pin of InnoSwitch3-AQ IC through these components and causes the IC to enter auto-restart (AR) mode. This network protect for faults on the secondary when the secondary controller is functional. When the secondary controller is not functional, the primary side BPP pin based output OV function is recommended.

The InnoSwitch3-AQ IC has an internal reference of 1.265 V which is presented on the FB pin. Resistors R105 and R109 form a voltage divider feedback network. Capacitor C109 provides decoupling from high-frequency. Capacitor C100 and resistor R101 form a feedforward network to speed up response time and lower output ripple.

Output current is sensed by monitoring the voltage drop across parallel resistors R110A to R110C. The resulting analog current is filtered using R115 and C112 and monitored by the IS pin reference to SECONDARY GROUND. An internal current sense threshold of approximately 35 mV is used to reduce losses. Once the threshold is met, InnoSwitch3-AQ IC will control the number of pulses and amplitude of primary switching cycles to maintain a fixed output current. The IC enters auto-restart (AR) operation when the output voltage falls below 90% of regulation and recovers when the load current is reduced below the CC limit. Diode D100 limits the voltage drop across R110A to R110C to protect the IS pin during overload or short-circuit conditions.

5 PCB Layout

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

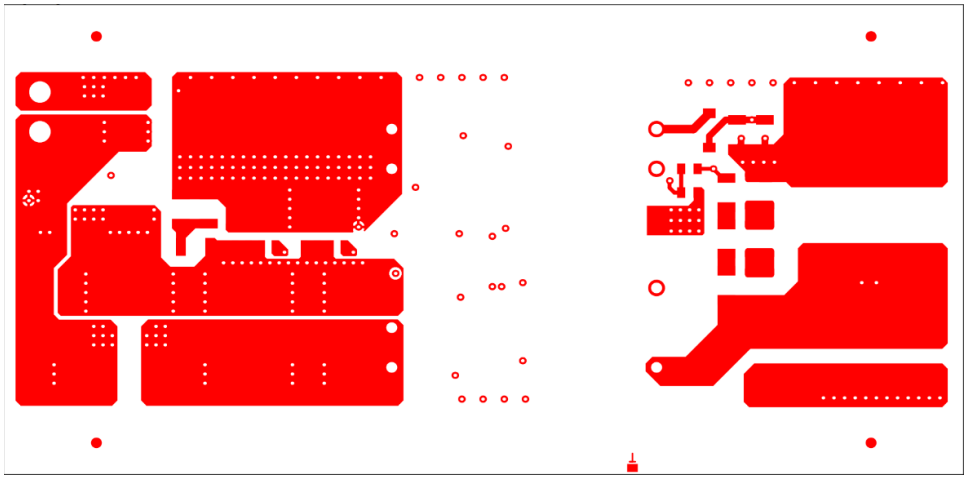


Figure 4 – RDR-85SLR Top Layer PCB Layout.

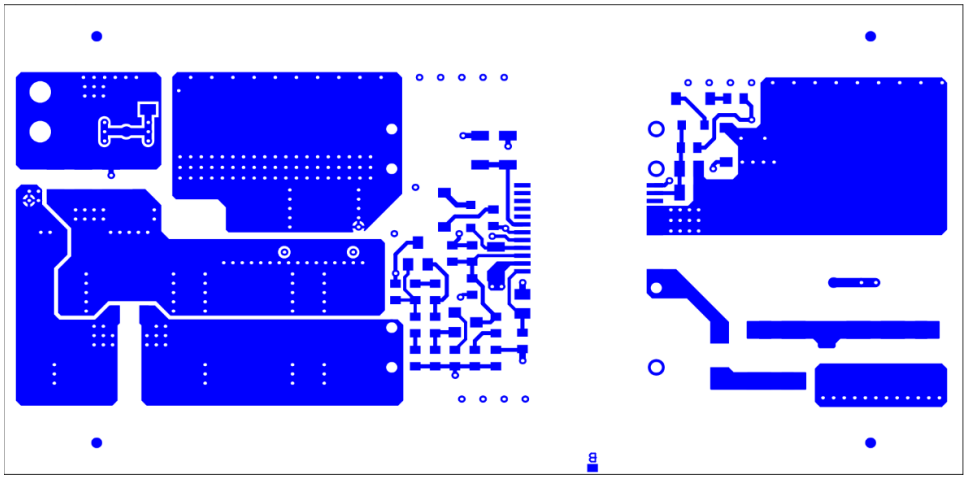


Figure 5 – RDR-85SLR Bottom Layer PCB Layout.

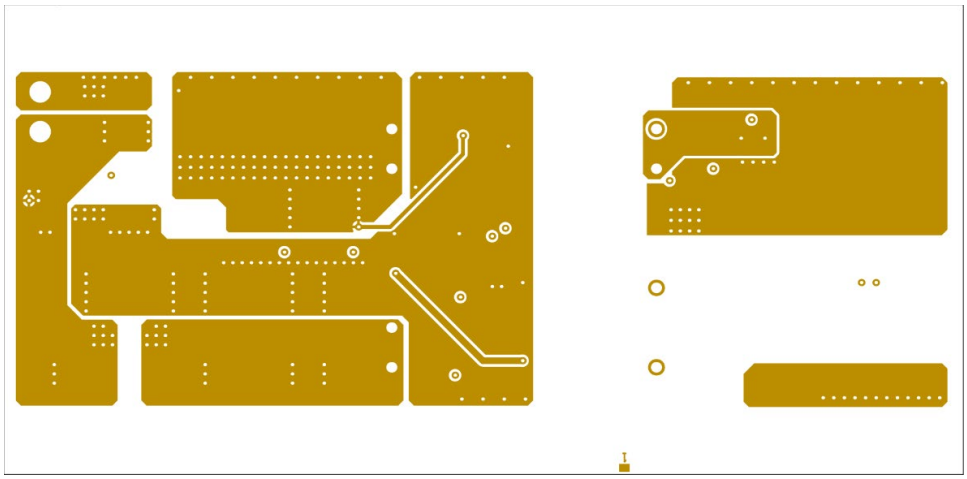


Figure 6 – RDR-85SLR Mid-Layer 1 PCB Layout.

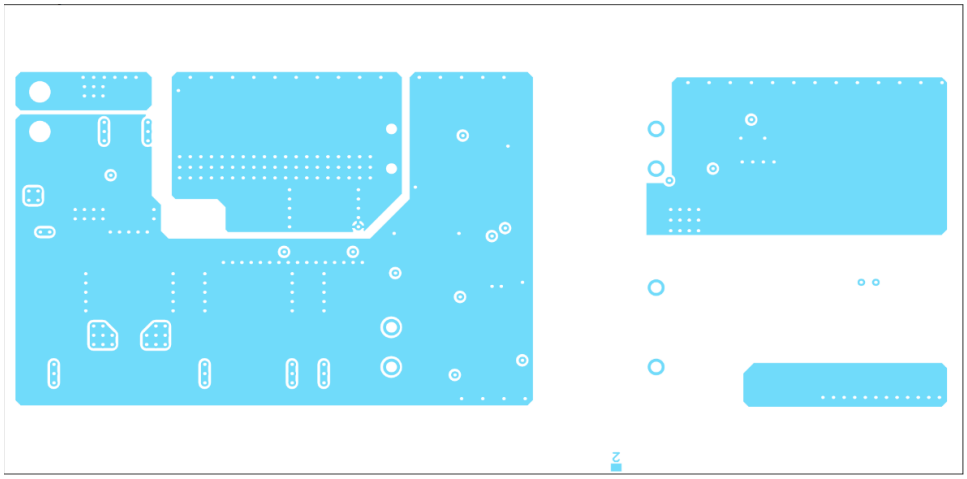


Figure 7 – RDR-85SLR Mid-Layer 2 PCB Layout.

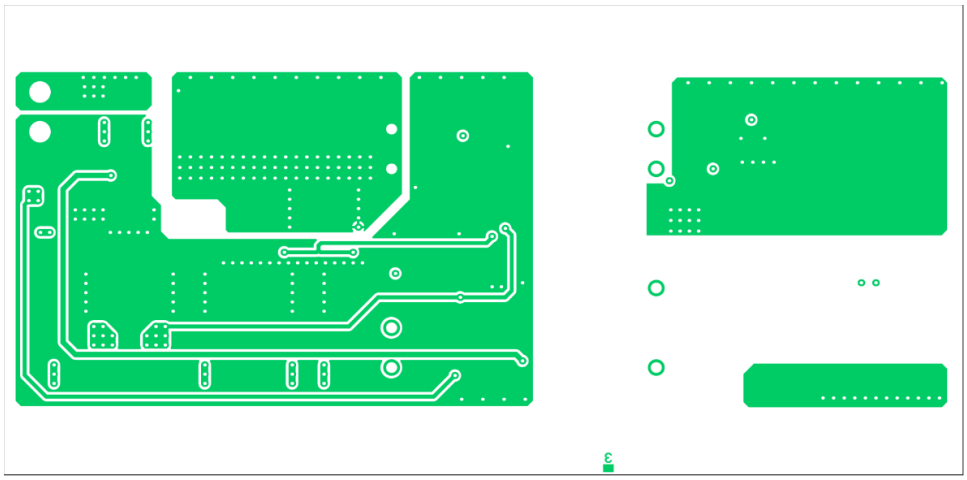


Figure 8 – RDR-85SLR Mid-Layer 3 PCB Layout.

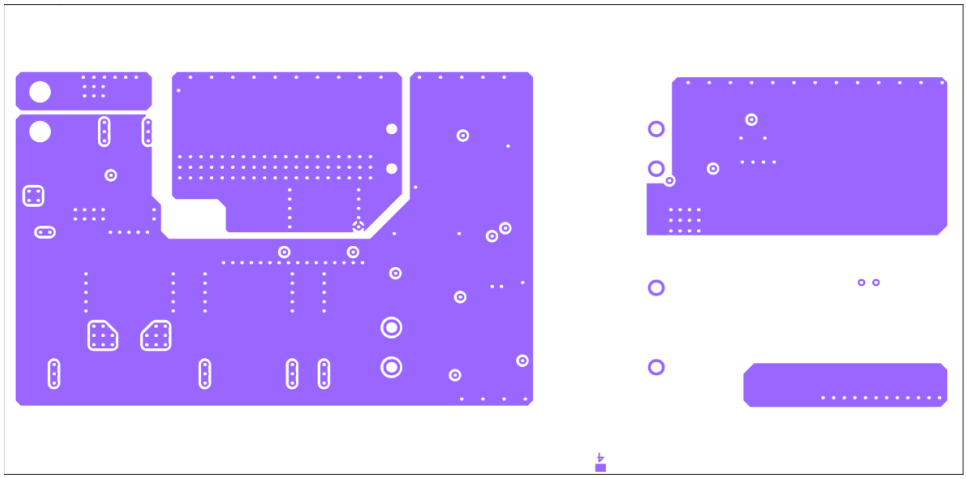


Figure 9 – RDR-85SLR Mid-Layer 4 PCB Layout.

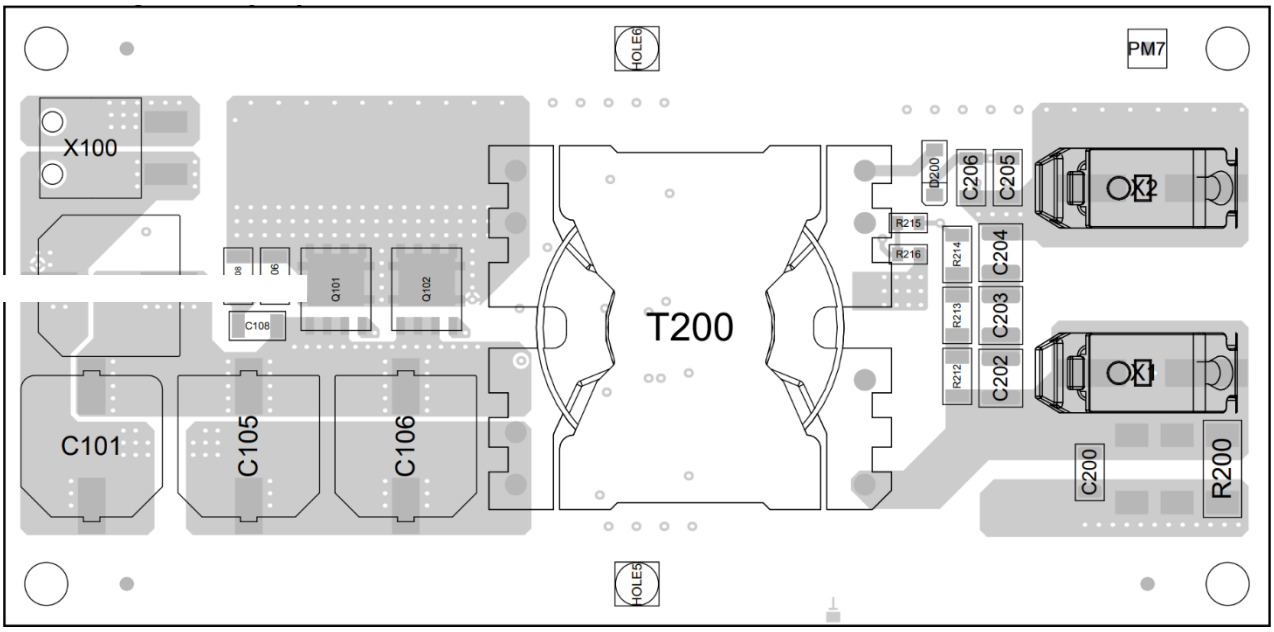


Figure 10 – RDR-85SLR PCB Assembly (Top).

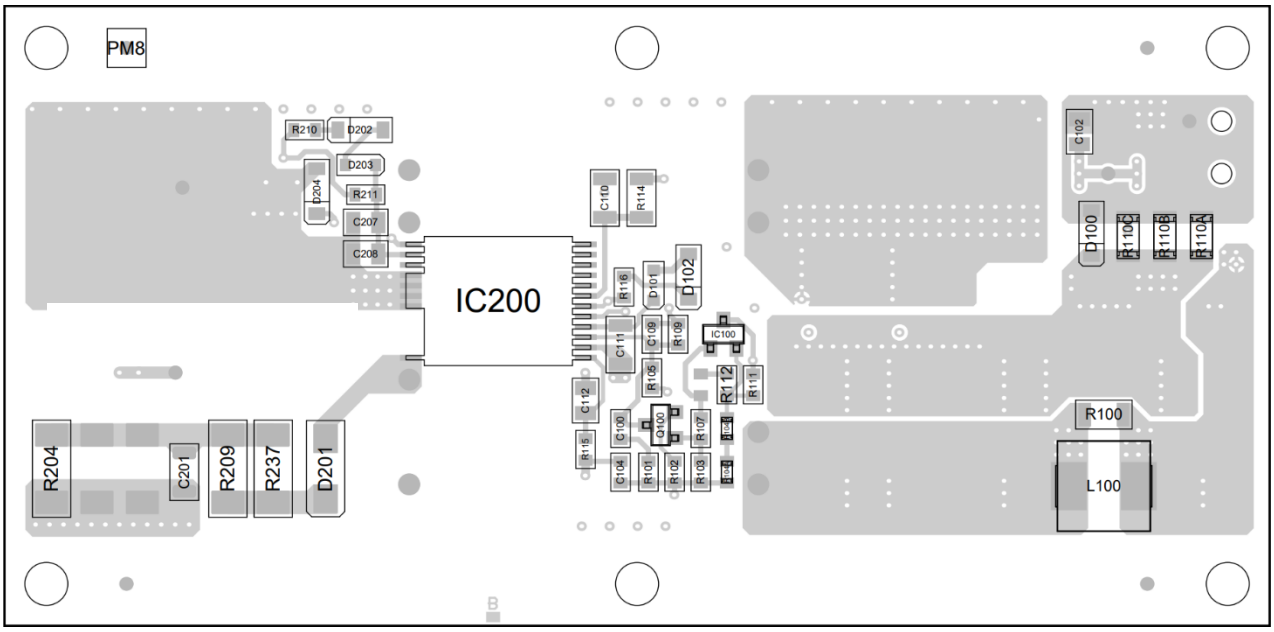


Figure 11 – RDR-85SLR PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 47 nF X7R/50 V/10% 0603	GCJ188R71H473KA12D	Murata
2	1	C101	Polymer Aluminium Capacitor 1000 µF AL/25 V/20% 10.3X10.3 mm	EEH-ZS1E102UP	Panasonic
3	1	C102	Ceramic Chip Capacitor 2.2 µF X7R/35 V/10% 0805	CGA4J1X7R1V225K125AC	TDK
4	1	C104	Ceramic Chip Capacitor 100 nF X7R/50 V/10% 0603	CGA3E2X7R1H104K080AA	TDK
5	3	C105, C106, C107	Polymer Aluminium Capacitor 560 µF AL/25 V/20% 10.3X10.3 mm	EEH-ZU1E561P	Panasonic
6	1	C108	Ceramic Chip Capacitor 2.2 nF C0G/630 V/5% 1206	GCM31B5C2J222JX01L	Murata
7	1	C109	Ceramic Chip Capacitor 330 pF C0G/50 V/5% 0603	GCM1885C1H331JA16D	Murata
8	1	C110	Ceramic Chip Capacitor 330 pF C0G/630 V/5% 1206	CGA5C4C0G2J331J060AA	TDK
9	1	C111	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 1206	GCM31CR71H225KA55K	Murata
10	1	C112	Ceramic Chip Capacitor 1 µF X7R/50 V/10% 0805	CGA4J3X7R1H105K125AB	TDK
11	2	C200, C201	Ceramic Chip Capacitor 1500 pF C0G/630 V/5% 1206	CGA5H4C0G2J152J115AA	TDK
12	3	C202, C203, C204	Ceramic Chip Capacitor 150 nF X7R/500 V/10% 1210	C1210X154KCRACAUTO	KEMET
13	2	C205, C206	Ceramic Chip Capacitor 10 µF X7R/50 V/10% 1206	CGA5L1X7R1H106K160AC	TDK
14	2	C207, C208	Ceramic Chip Capacitor 2.2 µF X7R/50 V/10% 0805	CGA4J3X7R1H225K125AE	TDK
15	1	D100	Schottky Diode PMEG4030ER/8X 40 V/3 A SOD123W	PMEG4030ER/8X	Nexperia
16	2	D101, D203	Diode 100 V 250 mA Surface Mount SOD-323F	BAS16J,115	Nexperia
17	1	D102	Zener Diode 9.1 V 500 mW ±5% SMT SOD-123 MMSZ5239B-7-F 9.1 V SOD-123	MMSZ5239B-7-F	Diodes, Inc.
18	1	D200	Diode Standard 200 V 225 mA (DC) SMT SOD-123 BAS21GWX 200 V / 225 mA SOD-123	BAS21GWX	Nexperia
19	1	D201	DIODE SCHOTTKY 1 kV 1 A ACURA107 1000 V / 1 A DO-214AC (SMA)	ACURA107-HF	Comchip
20	1	D202	Zener Diode 20 V 500 mW ±5% Surface Mount SOD-123	MMSZ5250B-7-F	Diodes, Inc.
21	1	IC200	InnoSwitch3-AQ 900 V InSOP-24D	INN3990CQ	Power Integrations
22	1	L100	Shielded Power Inductor 220 nH 7.00 mm x 6.60 mm	SRP7028A-R22Y	Bourns
23	2	Q101, Q102	N-Channel 100 V 15A (Ta), 91A (Tc) 1.5W (Ta), 100W (Tc) Surface Mount PowerDI5060-8	DMTH10H009LPSQ	Diodes, Inc.
24	1	R101	Thick Film Chip Resistor 10 kΩ 5%/0.1 W/75 V 0603	AC0603JR-0710KL	YAGEO
25	1	R105	Thick Film Chip Resistor 110 kΩ 5%/0.1 W/150 V 0603	RMCF0603JT110K	Stackpole
26	2	R106, R108	Thick Film Chip Resistor 27 Ω 1%/0.5 W/500 V 1206	SR1206FR-7W27RL	YAGEO
27	1	R109	RES, 12.7 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1272V	Panasonic
28	1	R110A	Current Sense Resistors - SMD 1/2watt 0.012ohms 1%	WSL1206R0120FEA18	Vishay / Dale
29	2	R110B, R110C	RES, 15 mΩ, 1% 1W 1206	WSLP1206R0150FEA	Vishay / Dale
30	1	R114	Thick Film Chip Resistor 100 Ω 5%/0.25 W/200 V 1206	RMCF1206JT100R	Stackpole
31	1	R115	Thick Film Chip Resistor 10 Ω 5%/0.1 W/75 V 0603	CRGCQ0603J10R	TE Connectivity
32	1	R116	Thick Film Chip Resistor 750 Ω 1%/0.1 W/75 V 0603	CQ03WAF7500T5E	ROYALOHM
33	2	R200, R204	MELF Resistors 390 kΩ 1%/1 W/350 V MELF 0207	MMB02070C3903FB200	Vishay
34	2	R209, R237	RES SMD 0 OHM JUMPER 1W 0207	MMB02070Z0000ZB700	Vishay
35	1	R210	RES, 75 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ750V	Panasonic
36	1	R211	RES, 7.5 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
37	1	R216	Thick Film Chip Resistor 0R 0603	RMCF0603ZT0R00	Stackpole
38	1	T200	PQ2620_THT PQ2620	PQ2620	Power Integrations
39	1	X1	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN04G7 RED	SM99S01VBNN04G7	METZ CONNECT
40	1	X100	TERMI-BLOK SMD MOUNT 180_2P_3.81 2383945-2 12 A 1x2Pin, Pitch 3.81 mm	2383945-2	TE
41	1	X2	TERM BLOCK 1POS SIDE ENTRY SMD SM99S01VBNN00G7 BLACK	SM99S01VBNN00G7	METZ CONNECT
41	1	Z1	Printed Circuit Board PCB 1.55 mm PCB thickness 1.55 mm N		

Table 2 – RDR-85SLR Bill of Materials[1].

[1] All components are AEC-Q qualified except the connectors and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

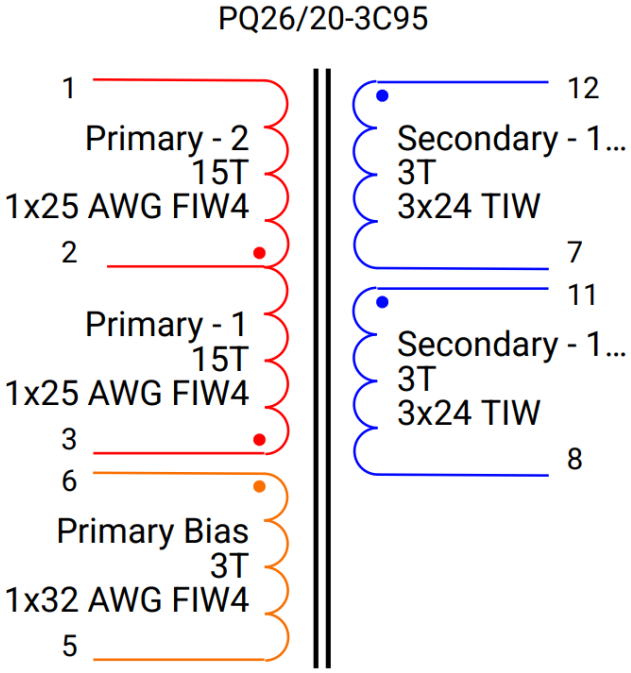


Figure 12 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side		46.0	80.0	W
Input voltage VDC	Flyback topology	100	120	150	V
Switching frequency	Flyback topology			78.6	kHz
Electrical Strength	60 second, 60 Hz, from pins 1, 2, 3, 4, 5, 6 to 7, 8, 9, 10, 11, 12.		3000		VAC
Nominal Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 and pin 3, with all other windings open at 25 °C		447		µH
Part to part tolerance	Tolerance of Primary Inductance		5.0		%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.		8		µH

Table 3 – Transformer (T200) Electrical Specifications.

7.3 Transformer Build Diagram

WD5:2nd Primary	15T – 1 x #25 AWG FIW4
WD4: 2nd Secondary	3T – 3 x #24 AWG TIW
WD3: 1st Secondary	3T – 3 x #24 AWG TIW
WD2: Bias	3T – 1 x #32 AWG FIW4
WD1: 1st Primary	15T – 1 x#25 AWG FIW4

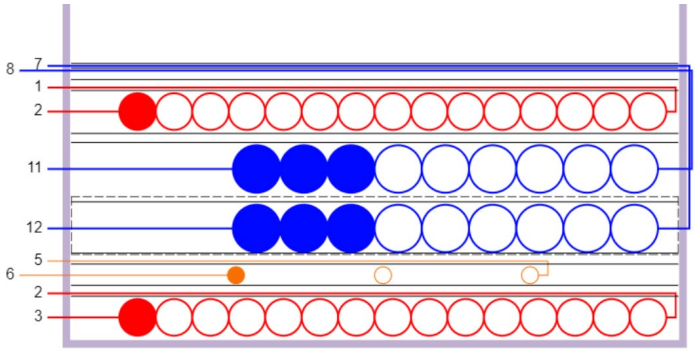


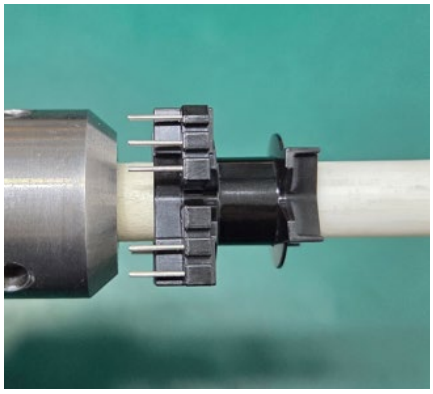
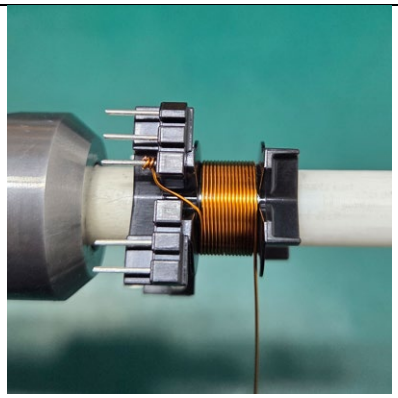
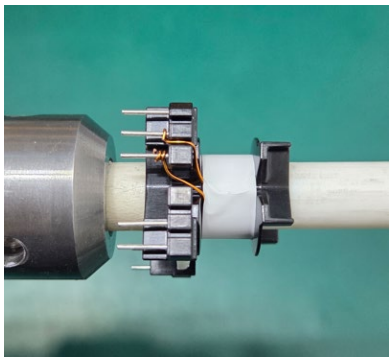
Figure 13 – Transformer Build Diagram.

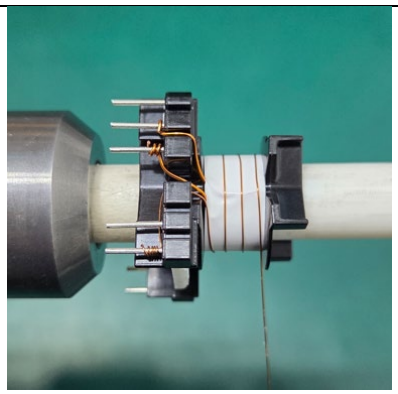
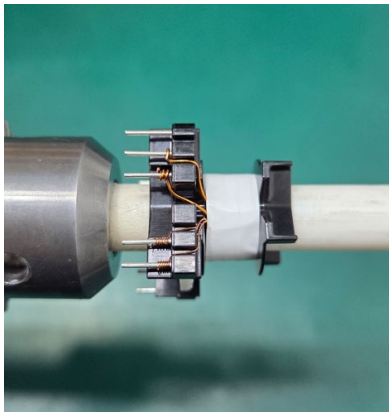
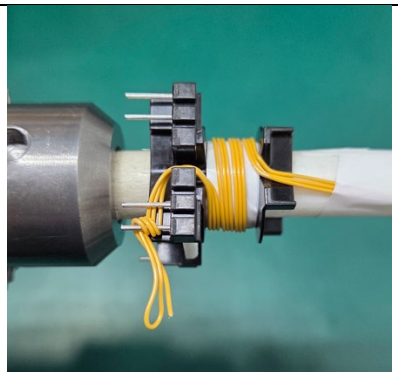
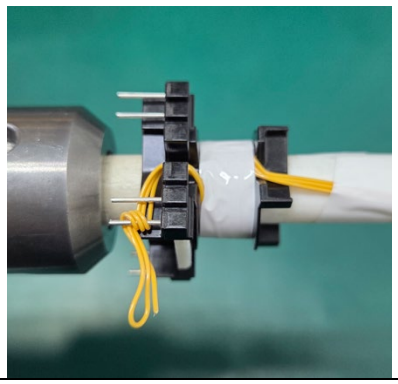
7.4 Material List

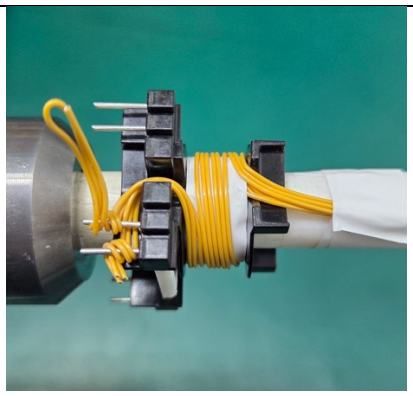
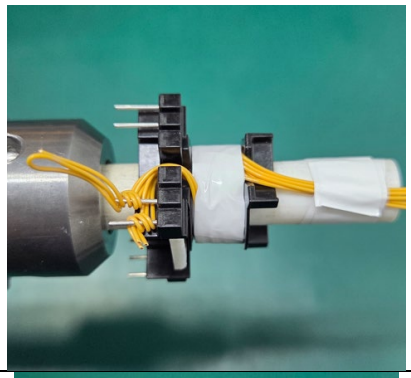
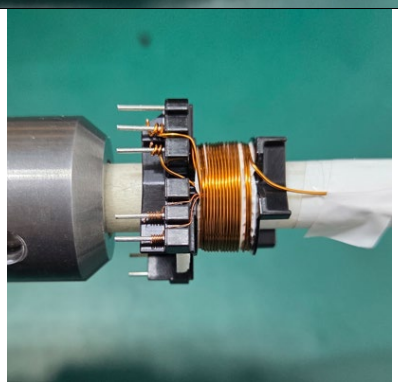
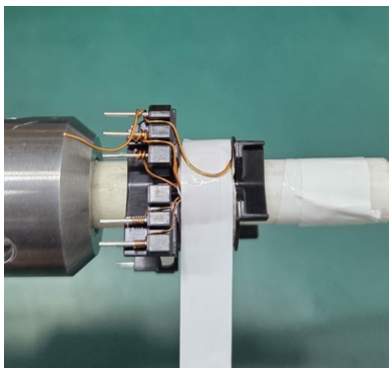
Item	Description
[1]	Core: PQ26/20, 3C95
[2]	Bobbin: PQ26/20 – 2 (P6-S6), FerroxCube
[3]	Varnish: Dolph BC-359.
[4]	Fully Insulated Wire: 0.450mm (Appr Eq.: 25AWG), Grade 4 (OD: 0.549mm) IEC 60172/P80, IEC 61558-1
[5]	Separation Tape: Polyester flm [1 mil (25.4 micrometers) base thickness], 9 mm wide
[6]	Fully Insulated Wire: 0.200mm (Appr Eq.: 32AWG), Grade 4 (OD: 0.253mm) IEC 60172/P80, IEC 61558-1
[7]	Triple Insulated Wire: 24 AWG (0.511mm), insulation TEX-E (OD: 0.711mm) UL 2353 UL 1950/ IEC 60950-1, Annex U (UL 1411, UL 60950-1) 1000V Vrms, class B, reinforced insolation

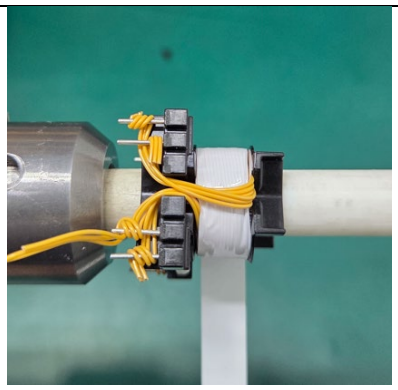
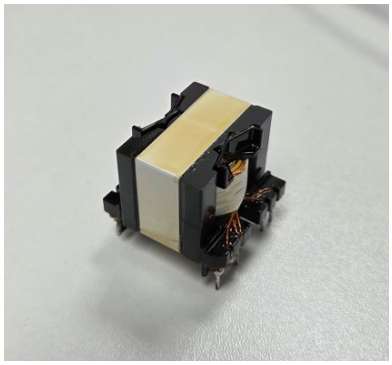
Table 4 – Transformer (T200) Material List.

7.5 Transformer Winding Instructions

Winding Preparation	 	Start by removing the unused pins 4, 9, and 10 of the bobbin. Position the bobbin, Item [2], on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction.
WD1 (1st Primary)	 	Using 1 lead of Item [4], start on pin 3 and wind the primary winding's first layer, 15 turns from left to right. Spread the winding evenly along the bobbin's width. Add 1 layer of tape, Item [5], between the exit lead and winding. Finish this winding on Pin 2.

WD2 (Bias)	 	Using 1 lead of Item [6], start on pin 6 and wind 3 turns of bias winding from left to right. Spread the winding evenly along the bobbin's width. Add 1 layer of tape, Item [5], between the exit lead and winding. Finish this winding on Pin 5.
WD3 (1st Secondary)	 	Using 3 leads of Item [7], start on pin 12 and wind the secondary winding's first layer, 3 turns from left to right. Spread the winding evenly along the bobbin's width. Bring this winding to the right and leave it unconnected temporarily. Do not terminate yet. Add 1 layer of tape, Item [5], on the top.

WD4 (2nd Secondary)	 	Using 3 leads of Item [7], start on pin 11 and wind the secondary winding's second layer, 3 turns from left to right. Spread the winding evenly along the bobbin's width. Bring this winding to the right and leave it unconnected temporarily. Do not terminate yet. Add 1 layer of tape, Item [5], on the top.
WD5 (2nd Primary)	 	Using 1 lead of Item [4], start on pin 2 and wind the primary winding's second layer, 15 turns from left to right. Spread the winding evenly along the bobbin's width. Add 1 layer of tape, Item [5], between the exit lead and winding. Do not cut the tape yet. Finish this winding on Pin 2.

Finishing		 	Bring the wires of the 1st and 2nd secondary windings to the top, and from right to left, terminate both to Pins 7 and 8. Continue to secure the windings using 2 layers of tape, Item [5]. Gap the core halves to get 447 µH (±5.0 %) and secure the core on the bobbin with tape. Varnish with Item [3].

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_032525; Rev.4.0; Copyright Power Integrations 2025	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	12.00		12.00	V	Output Voltage
4	OPERATING CONDITION 1					
5	VINDC1	150.00		150.00	V	Input DC voltage 1
6	IOUT1	6.670		6.670	A	Output current 1
7	POUT1			80.04	W	Output power 1
8	EFFICIENCY1	0.94		0.94		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
10						
11	OPERATING CONDITION 2					
12	VINDC2	100.00		100.00	V	Input DC voltage 2
13	IOUT2	6.670		6.670	A	Output current 2
14	POUT2		Info	80.04	W	The device is capable of delivering 40W at the specified input voltage. Verify thermal performance.
15	EFFICIENCY2	0.94		0.94		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
17						
18	OPERATING CONDITION 3					
19	VINDC5	150.00		150.00	V	Input DC voltage 5
20	IOUT5	3.840		3.840	A	Output current 5
21	POUT5			46.08	W	Output power 5
22	EFFICIENCY5	0.94		0.94		Converter efficiency for output 5
23	Z_FACTOR5			0.50		Z-factor for output 5
24						
25	OPERATING CONDITION 4					
26	VINDC6	100.00		100.00	V	Input DC voltage 6
27	IOUT6	3.840		3.840	A	Output current 6
28	POUT6		Info	46.08	W	The device is capable of delivering 40W at the specified input voltage. Verify thermal performance.
29	EFFICIENCY6	0.94		0.94		Converter efficiency for output 6
30	Z_FACTOR6			0.50		Z-factor for output 6
31						
32	TEMPERATURE_AMBIENT			40.0	°C	System ambient temperature
33						
34	**PRIMARY CONTROLLER SELECTION**					
35	ILIMIT_MODE	INCREASED		INCREASED		INCREASED Device current limit mode
36	VDRAIN_BREAKDOWN	900		900	V	Device breakdown voltage
37	DEVICE_GENERIC			INN39X0		Device selection
38	DEVICE_CODE	INN3990CQ		INN3990CQ		Device code
39	PDEVICE_MAX			40	W	Device maximum power capability
40	RDSON_25DEG			0.39	Ω	Primary switch on-time resistance at 25°C
41	RDSON_125DEG			0.61	Ω	Primary switch on-time resistance at 125°C

42	ILIMIT_MIN			2.395	A	Primary switch minimum current limit
43	ILIMIT_TYP			2.576	A	Primary switch typical current limit
44	ILIMIT_MAX			2.756	A	Primary switch maximum current limit
45	VDRAIN_ON_PRSW			0.51	V	Primary switch on-time voltage drop
46	VDRAIN_OFF_PRSW			300	V	Peak drain voltage on the primary switch during turn-off at maximum input DC voltage and allowable leakage ring
47	VCLAMP			150.0	V	Voltage across clamp circuit
48	CU_AREA_INNO			1.00	in2	Primary switch copper cooling area
49	TEMP_INNO_MIN			63.37	°C	Device minimum operating temperature with respect to ambient, observed at 150V VINDC
50	TEMP_INNO_MAX			103.82	°C	Device maximum operating temperature with respect to ambient, observed at 100V VINDC
51	**WORST CASE ELECTRICAL PARAMETERS**					
52	FSWITCHING_MAX	78600		78600	Hz	Maximum switching frequency at full load and minimum DC input voltage
53	VOR	120.0		120.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
54	KP			0.686		Measure of continuous/discontinuous mode of operation
55	MODE_OPERATION			CCM		Mode of operation
56	DUTYCYCLE			0.547		Primary switch duty cycle
57	TIME_ON_MIN			6.081	us	Minimum primary switch on-time
58	TIME_ON_MAX			11.58	us	Maximum primary switch on-time
59	TIME_OFF			5.77	us	Primary switch off-time
60	LPRIMARY_MIN			424.6	uH	Minimum primary magnetizing inductance
61	LPRIMARY_TYP			446.9	uH	Typical primary magnetizing inductance
62	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
63	LPRIMARY_MAX			469.3	uH	Maximum primary magnetizing inductance
64	**PRIMARY CURRENT**					
65	IAVG_PRIMARY			0.830	A	Primary switch average current
66	IPEAK_PRIMARY			2.583	A	Primary switch peak current
67	IPEDESTAL_PRIMARY			0.725	A	Primary switch current pedestal
68	IRIPPLE_PRIMARY			2.572	A	Primary switch ripple current
69	IRMS_PRIMARY			1.211	A	Primary switch RMS current
70	**TRANSFORMER CONSTRUCTION PARAMETERS**					
71	CORE SELECTION					
72	CORE	PQ26		PQ26		Core selection
73	CORE NAME			PQ26/20-3C95		Core code
74	AE			121.0	mm^2	Core cross sectional area
75	LE			45.0	mm	Core magnetic path length
76	AL			7020	nH	Ungapped core effective inductance per turns squared
77	VE			5470	mm^3	Core volume
78	BOBBIN NAME			CPV-PQ26/20-1S-12P-Z		Bobbin name

79	AW			31.1	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
80	BW			9.00	mm	Bobbin width
81	BH			3.70	mm	Bobbin height
82	MARGIN			0.0	mm	Bobbin safety margin
83	**PRIMARY WINDING**					
84	NPRIMARY			30		Primary winding number of turns
85	BPEAK			3647	Gauss	Peak flux density
86	BMAX			3298	Gauss	Maximum flux density
87	BAC			1641	Gauss	AC flux density (0.5 x Peak to Peak)
88	ALG			497	nH	Typical gapped core effective inductance per turns squared
89	LG			0.285	mm	Core gap length
90	**SECONDARY WINDING**					
91	NSECONDARY	3		3		Secondary winding number of turns
92	**BIAS WINDING**					
93	NBIAS			3		Bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
96	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
97	UNDERVOLTAGE PARAMETERS					
98	BROWN-IN REQUIRED			95.00	V	Required DC bus brown-in voltage threshold
99	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
100	VZ			9.10	V	Zener diode reverse voltage
101	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
102	ILKG			2.00	uA	Zener diode maximum reverse leakage current (at high ambient temperatures, typically 125 degC)
103	ILKG_MIN			0.10	uA	Zener diode minimum reverse leakage current (at low ambient temperatures, typically 25 degC)
104	BROWN-IN ACTUAL			64.18 - 94.97	V	Actual brown-in voltage range using standard resistors considering tolerances due to part and temperature variations
105	BROWN-OUT ACTUAL			57.38 - 85.14	V	Actual brown-out voltage range using standard resistors considering tolerances due to part and temperature variations
106	**OVERVOLTAGE PARAMETERS**					
107	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
108	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
109	VF				V	OV diode forward voltage
110	VRRM				V	OV diode reverse voltage
111	PIV				V	OV diode peak inverse voltage
112	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled

113	DC BUS SENSE RESISTORS					
114	RLS_H			2.74	MΩ	DC bus upper sense resistor to the V-pin for the required UV/OV threshold
115	RLS_L			124.00	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
116	**BIAS WINDING**					
117	VBIAS			9.00	V	Rectified bias voltage
118	VF_BIAS			0.70	V	Bias winding diode forward drop
119	VREVERSE_BIASDIODE			24.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
120	CBIAS			22	uF	Bias winding rectification capacitor
121	CBPP			4.70	uF	BPP pin capacitor
122	**SECONDARY COMPONENTS SELECTION**					
123	FEEDBACK COMPONENTS					
124	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
125	RFB_LOWER			11.80	kΩ	Lower feedback resistor
126	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
127	**MULTIPLE OUTPUT PARAMETERS**					
128	OUTPUT 1					
129	VOUT1			12.00	V	Output 1 voltage
130	IOUT1			6.670	A	Output 1 current
131	POUT1			80.04	W	Output 1 power
132	IRMS_SECONDARY1			11.028	A	Root mean squared value of the secondary current for output 1
133	IRIPPLE_CAP_OUTPUT1			8.783	A	Current ripple on the secondary waveform for output 1
134	NSECONDARY1			3		Number of turns for output 1
135	VREVERSE_RECTIFIER1			27.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
136	SRFET1	AUTO		DMT6005 LPS		Secondary rectifier (Logic MOSFET) for output 1
137	NUM_SRFET1	2		2		Number of SRFETs in parallel for output 1
138	VF_SRFET1			0.90	V	SRFET typical on-time drain voltage for output 1
139	VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
140	RDSON_SRFET1			9.4	mΩ	SRFET estimated on-time drain resistance at 100°C and VGS=4.4V for output 1
141	RTHJA_SRFET1			47.00	°C/W	SRFET max. thermal impedance for output 1
142	TEMP_SRFET1_MIN			46.9	°C	SRFET minimum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 100V VINDC
143	TEMP_SRFET1_MAX			56.2	°C	SRFET maximum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 100V VINDC
144						
145	PO_TOTAL	N/A		80.04	w	Total power of all outputs

Table 5 – RDR-85SLR PIXls Spreadsheet.

9 Performance data

All measurements were made with a 100 uF 400 V input-rail stabilization capacitor connected to the board unless otherwise noted.

9.1 No-Load Input Power

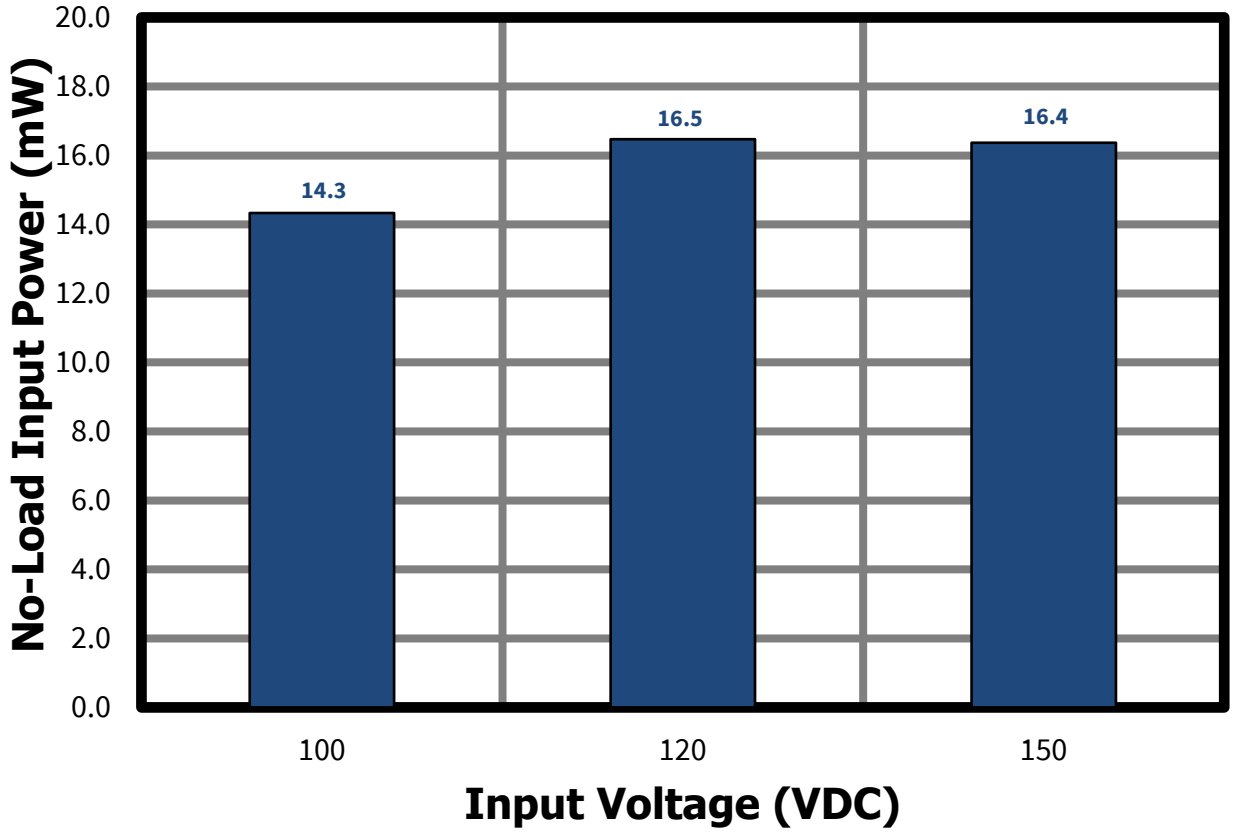


Figure 14 – No-Load Input Power vs. Input Voltage, Room Temperature.

9.2 Efficiency

9.2.1 Efficiency Across Line

Efficiency across line describes how the input voltage change affects the unit's overall efficiency. The points in the graph were taken at 100% nominal loading conditions.

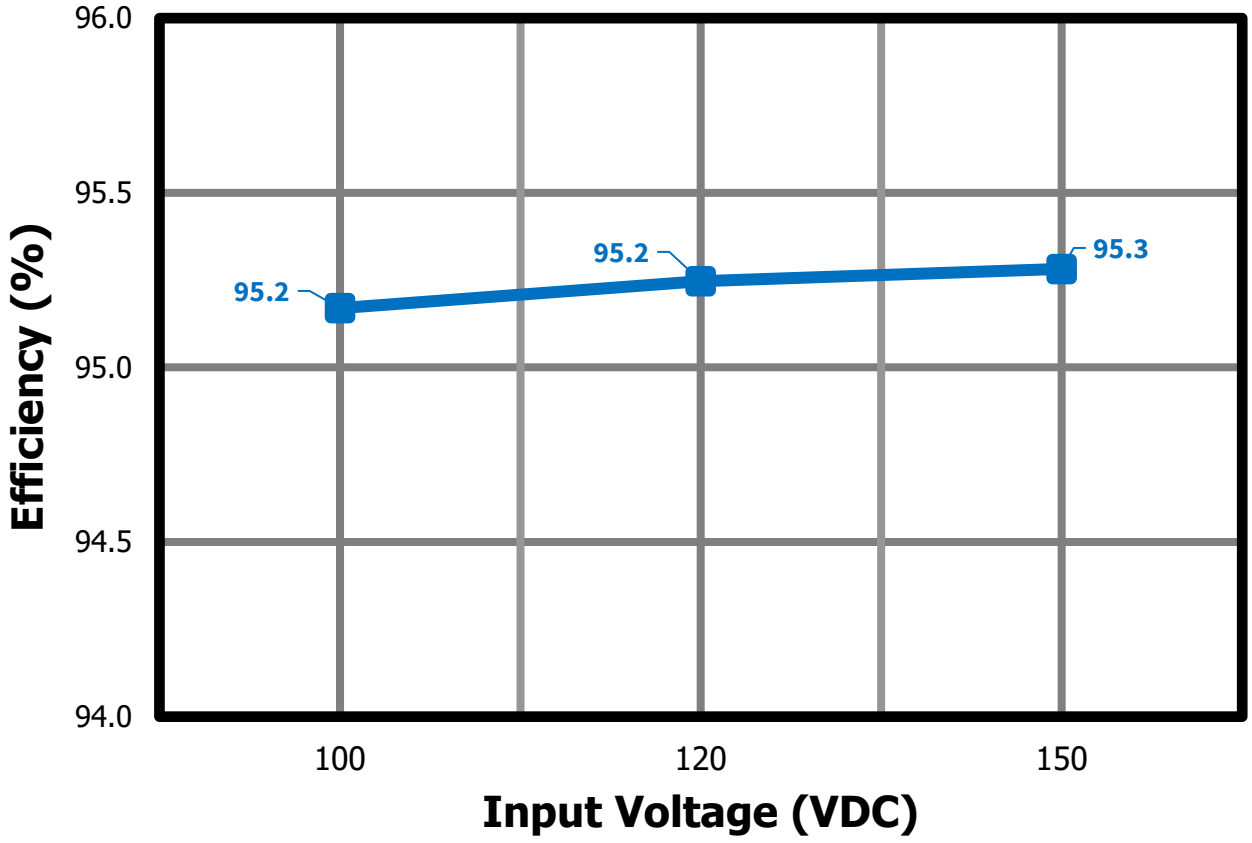


Figure 15 – Full Load Efficiency vs. Input Line Voltage, Room Temperature.

9.2.2 Efficiency Across Load

This test describes how the change in output loading affects overall efficiency.

9.2.2.1 Efficiency Across Load at Nominal Power

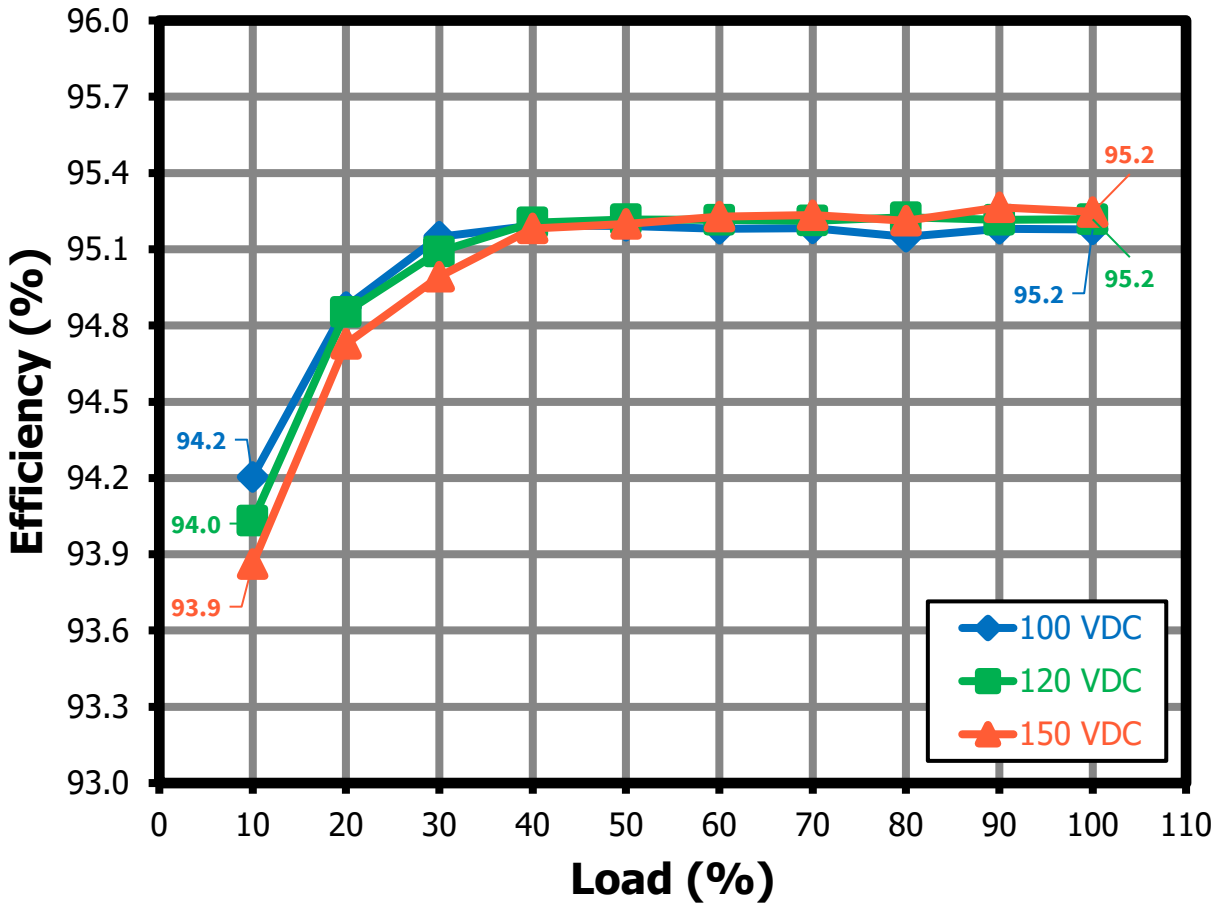


Figure 16 – Efficiency vs. Load at Different Input Voltages, Room Temperature.

9.2.2.2 Efficiency Across Load from Nominal to Peak Power

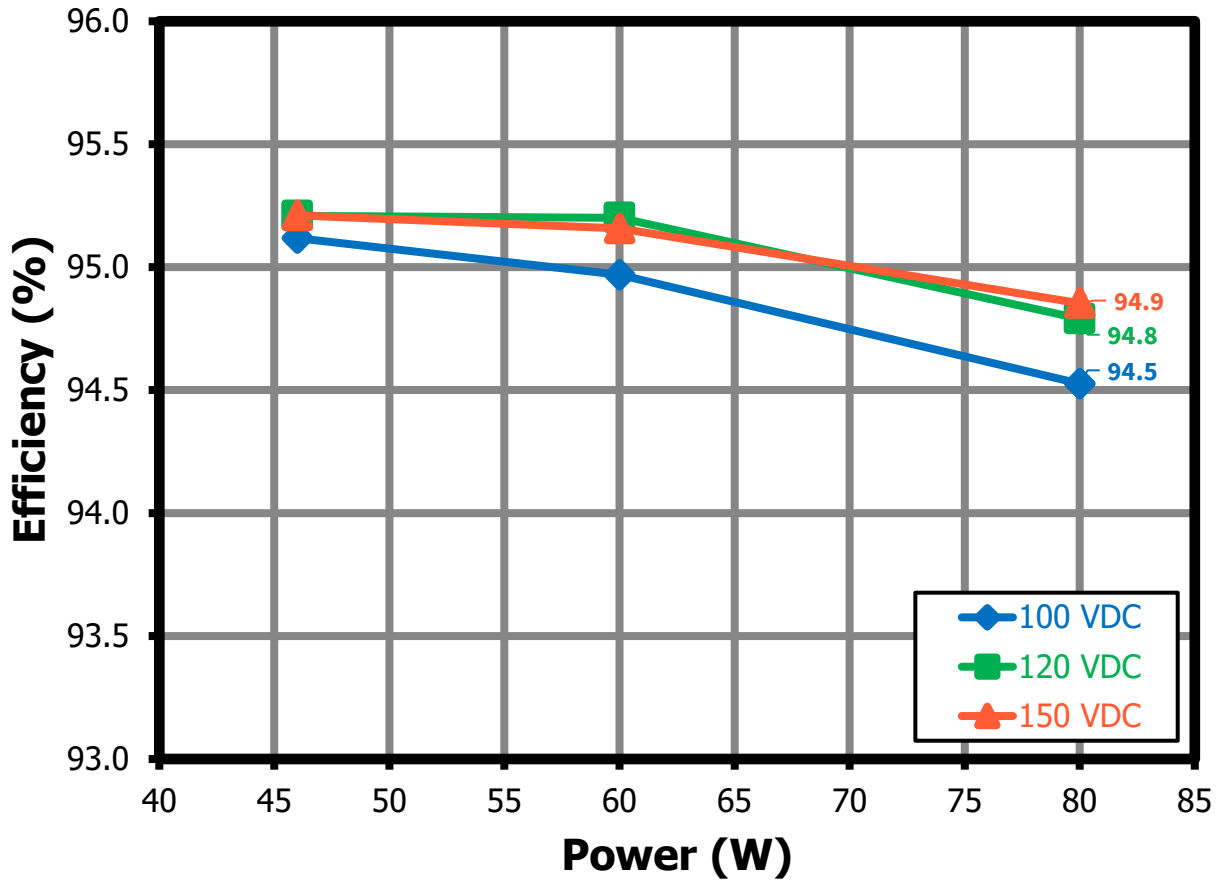


Figure 17 – Efficiency vs. Peak Power at Different Input Voltages, Room Temperature.

9.3 Line and Load Regulation

9.3.1 Load Regulation

Load regulation describes how the change in output load affects the output voltage of the unit.

9.3.1.1 Load Regulation at Nominal Power

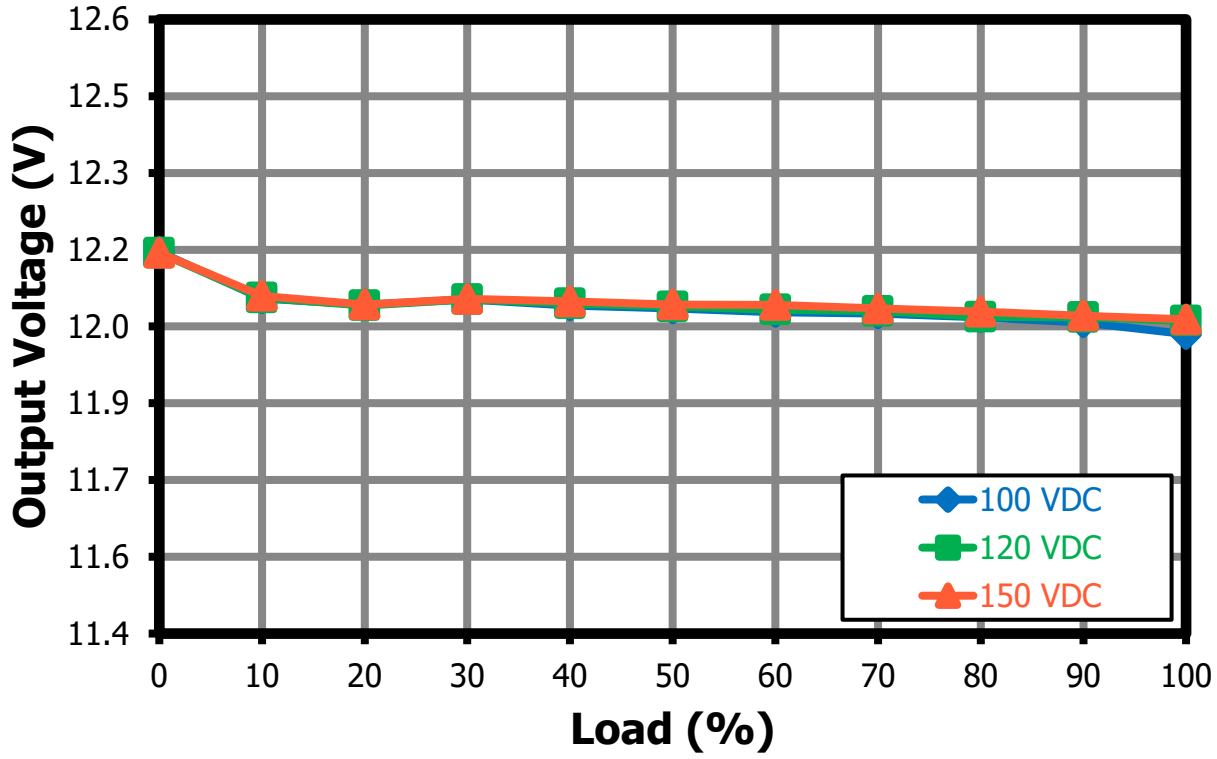


Figure 18 – Output Regulation vs. Load at Different Input Voltages, Room Temperature.

9.3.1.2 Load Regulation at Peak Power

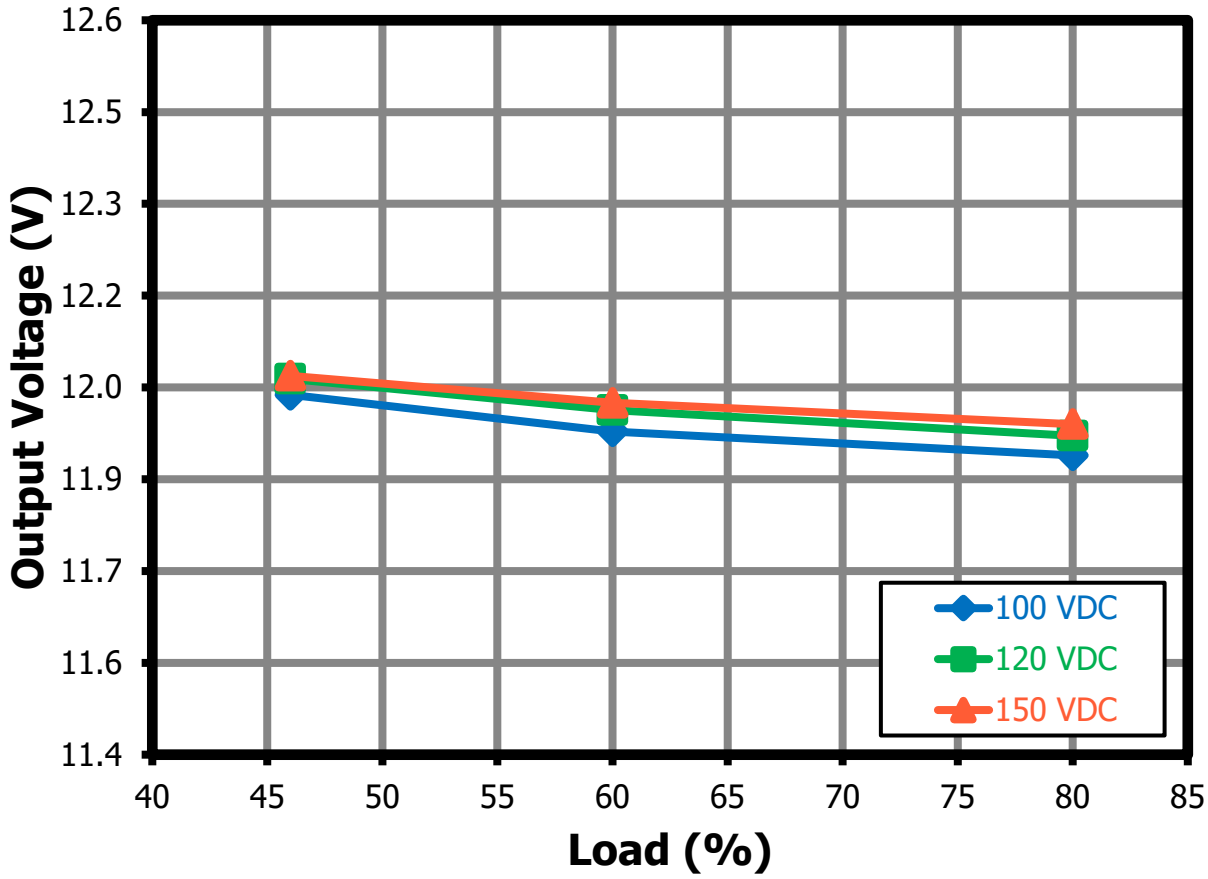


Figure 19 – Output Regulation vs. Load at Different Input Voltages, Room Temperature.

9.3.2 Line Regulation

Line regulation describes how the change in input voltage affects the average output voltage of the unit. The points in the following graph were taken at 100% nominal loading conditions.

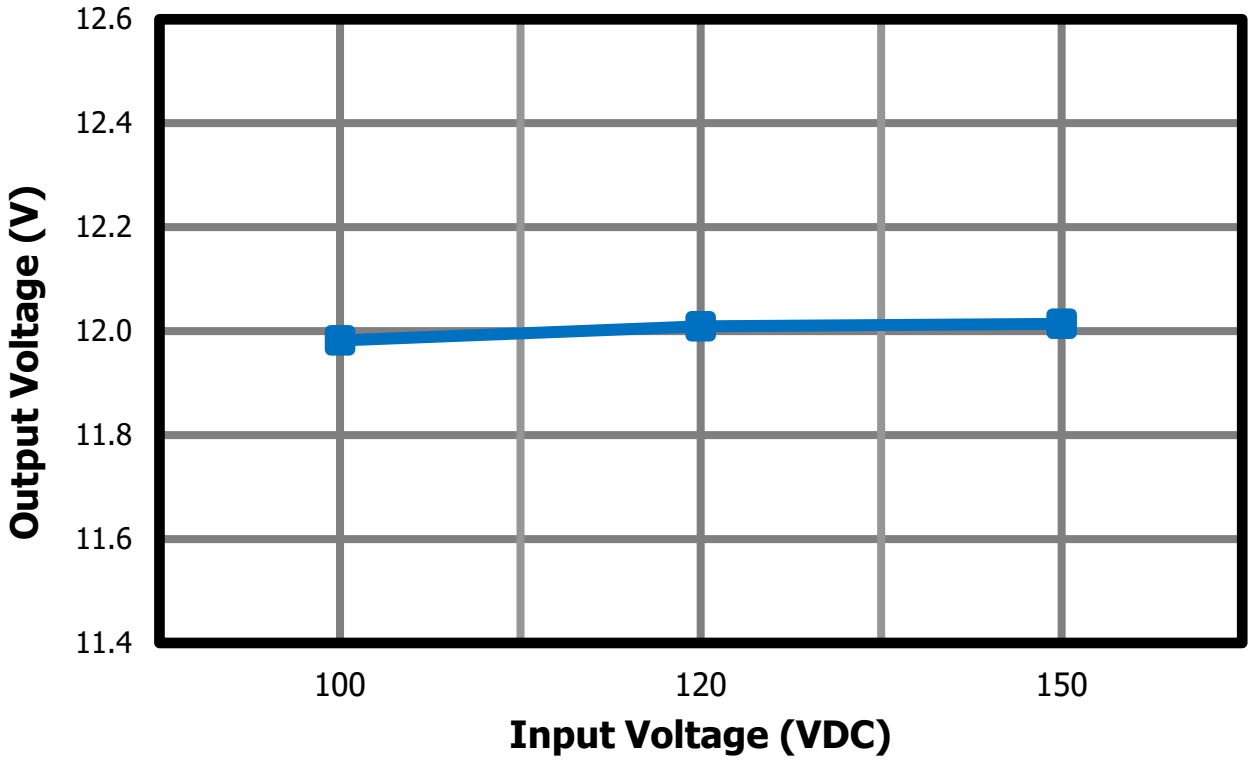


Figure 20 – Output Voltage vs Input Voltage at Full Load, Room Temperature.

10 Thermal Performance

The following thermal scans were captured using a FLIR thermal imager after soaking for 1 hour running on nominal power of 46 W. The setup was placed inside an enclosure to minimize the effect of airflow.

10.1 Thermal Image Data at Room Temperature

Layer	Designator	Critical Components	Temperature (°C)
BOTTOM	Bx1	InnoSwitch3- AQ (IC200)	44.4
	Bx2	Primary Snubber Resistor (R204)	35.5
	Bx3	Primary Snubber Diode (D201)	37.7
	Bx4	Output Current Sense Resistor (R110A)	37.9
TOP	Bx1	Transformer Core	46.1
	Bx2	Transformer Winding	48.7
	Bx3	Synchronous Rectifier MOSFET (Q102)	46.0
	Bx4	Synchronous Rectifier MOSFET (Q101)	45.4
	Bx5	Secondary Snubber Resistor (R106)	44.5
	El1	Output Capacitor (C106)	40.2

Table 6 – Thermal Data at 100 VDC Input Voltage.

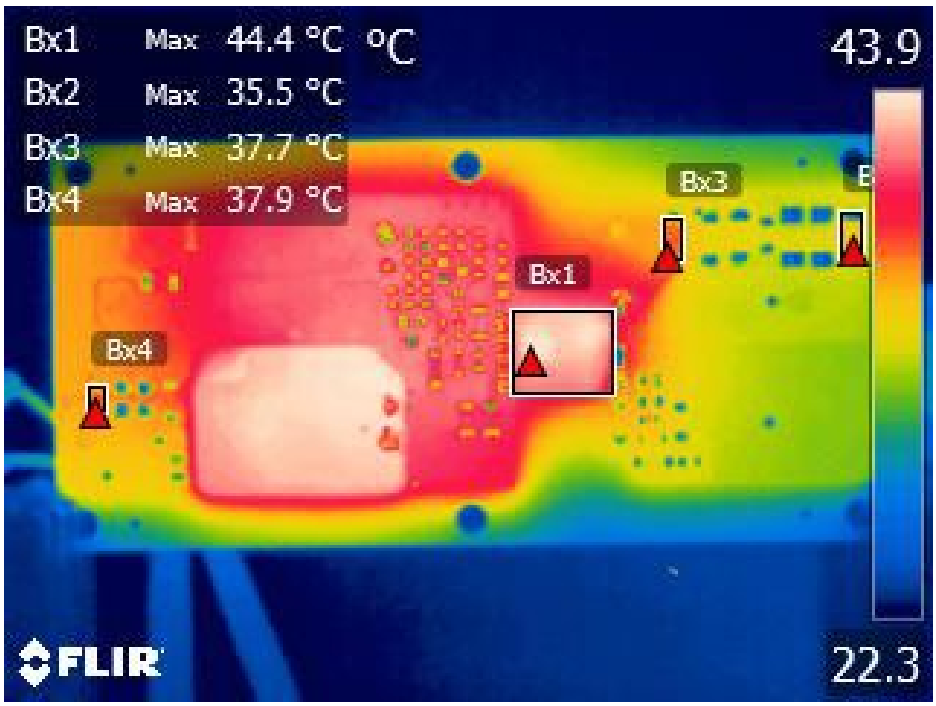


Figure 21 –Thermal Scan of the Bottom Layer of the PCB at 100 VDC Input.

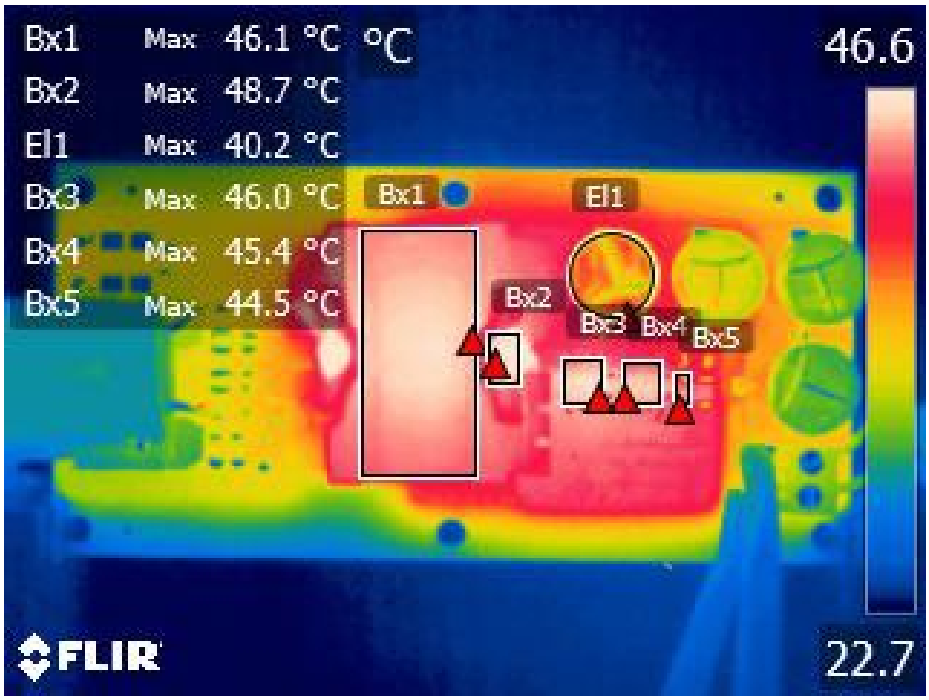


Figure 22 –Thermal Scan of the Top Layer of the PCB at 100 VDC Input.

Layer	Designator	Critical Components	Temperature (°C)
BOTTOM	Bx1	InnoSwitch3- AQ (IC200)	43.7
	Bx2	Primary Snubber Resistor (R204)	34.7
	Bx3	Primary Snubber Diode (D201)	37.2
	Bx4	Output Current Sense Resistor (R110A)	38.0
TOP	Bx1	Transformer Core	45.1
	Bx2	Transformer Winding	47.4
	Bx3	Synchronous Rectifier MOSFET (Q102)	45.5
	Bx4	Synchronous Rectifier MOSFET (Q101)	45.0
	Bx5	Secondary Snubber Resistor (R106)	45.1
	El1	Output Capacitor (C106)	39.6

Table 7 – Thermal Data at 150 VDC Input Voltage.

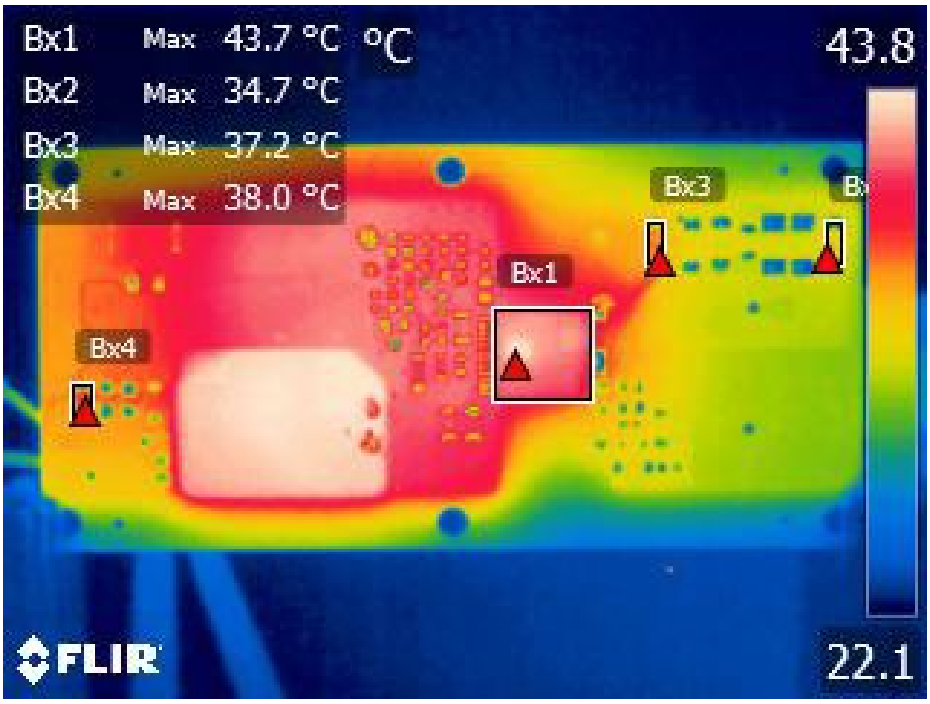


Figure 23 –Thermal Scan of the Bottom Layer of the PCB at 150 VDC Input.

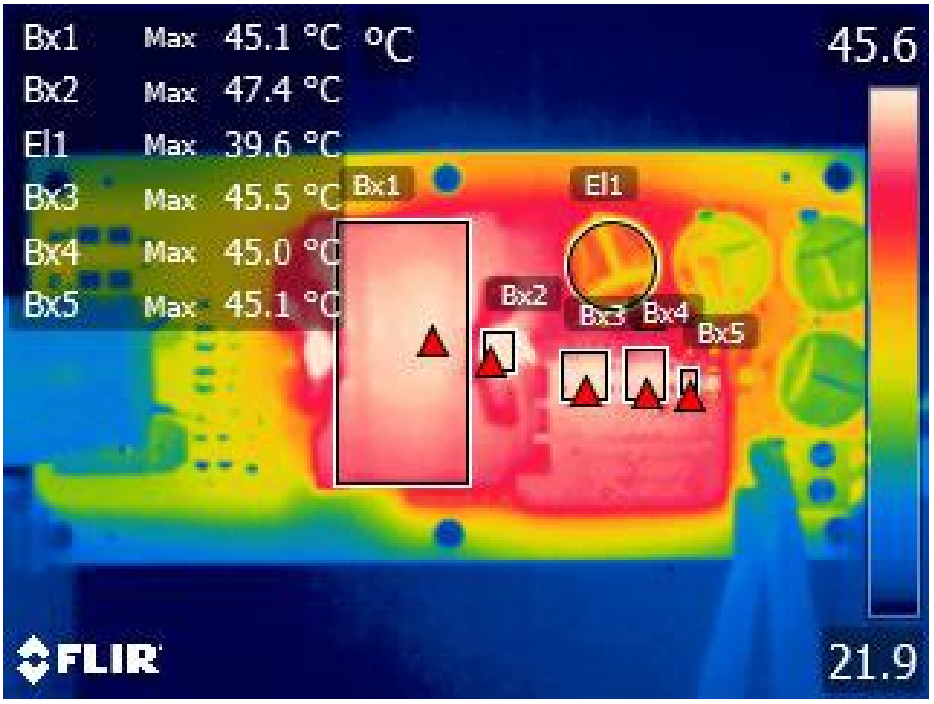


Figure 24 –Thermal Scan of the Top Layer of the PCB at 150 VDC Input.

11 Waveforms

11.1 Start-Up Waveforms at Nominal Power

The following measurements were taken by connecting the unit under test at different test input voltages. An electronic load configured for constant current and constant resistance was used for V_{OUT} and I_{OUT} start-up tests and constant current mode only for InnoSwitch3-AQ and SR FET startup tests.

11.1.1 Output Voltage and Current at Room Temperature (CC Mode)

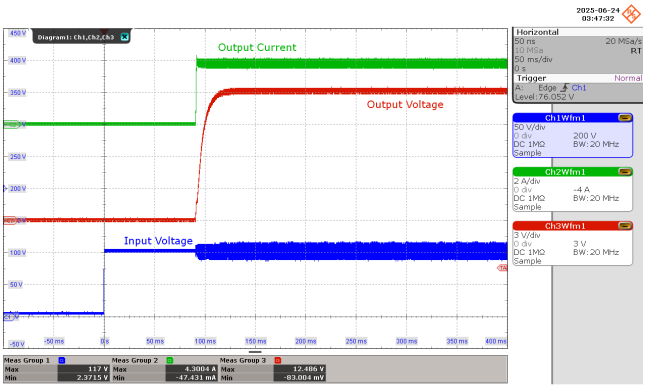


Figure 25 – Output Voltage and Current.
100 VDC, 3.84 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

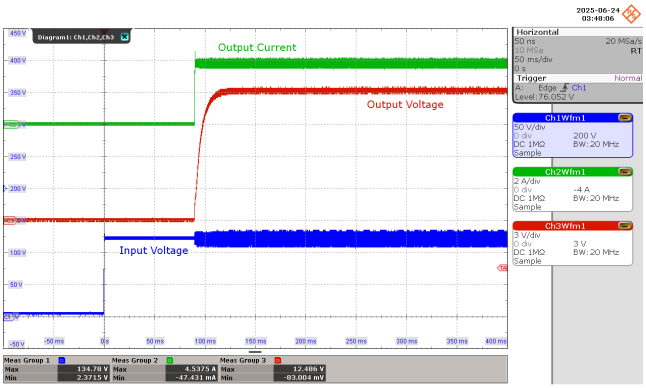


Figure 26 – Output Voltage and Current.
120 VDC, 3.84 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

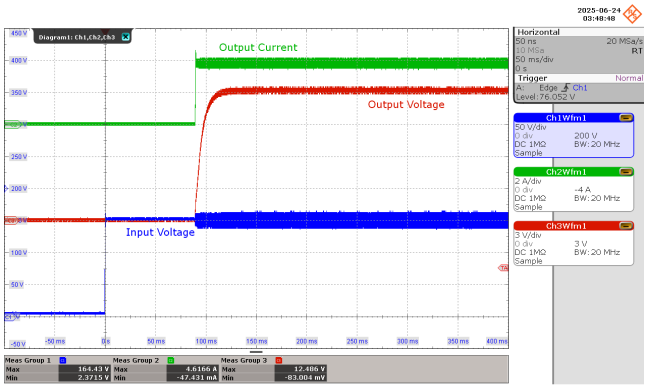


Figure 27 – Output Voltage and Current.
150 VDC, 3.84 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

11.1.2 Output Voltage and Current at Room Temperature (CR Mode)

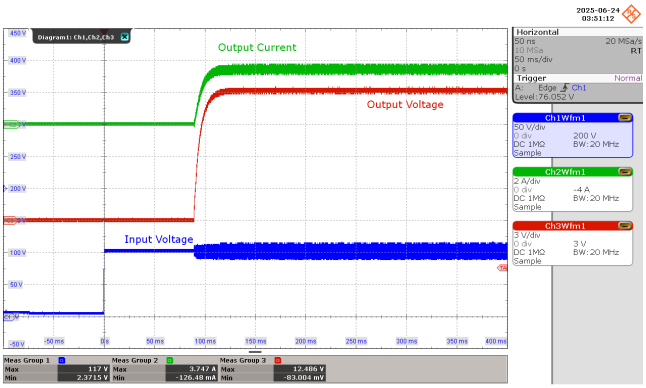


Figure 28 – Output Voltage and Current.
100 VDC, 3.125 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

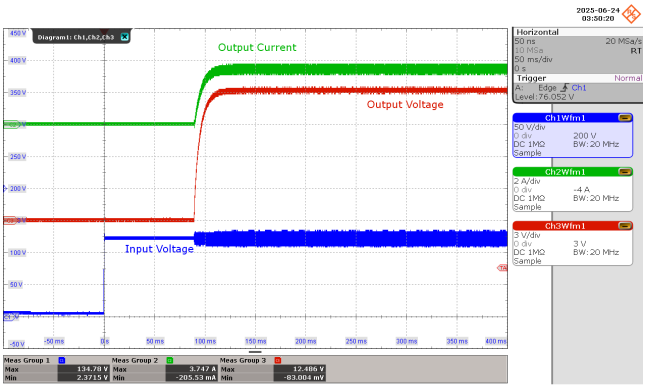


Figure 29 – Output Voltage and Current.
120 VDC, 3.125 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

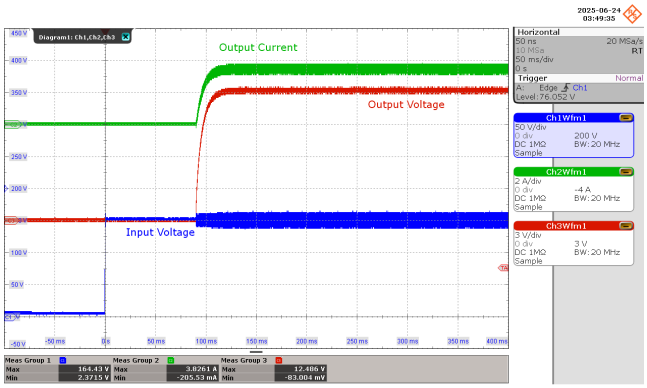


Figure 30 – Output Voltage and Current.
150 VDC, 3.125 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 2 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

11.1.3 InnoSwitch3-AQ Drain Voltage and Current at Room Temperature

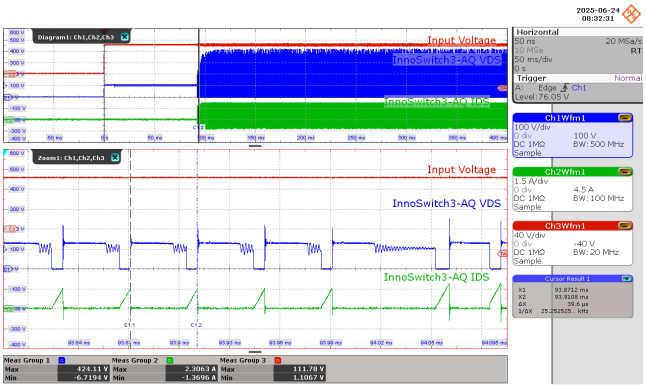


Figure 31 – INN3990CQ Drain Voltage and Current.
100 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 424 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.31 A)
CH3: V_{IN}, 40 V / div.
Time: 50 ms / div.

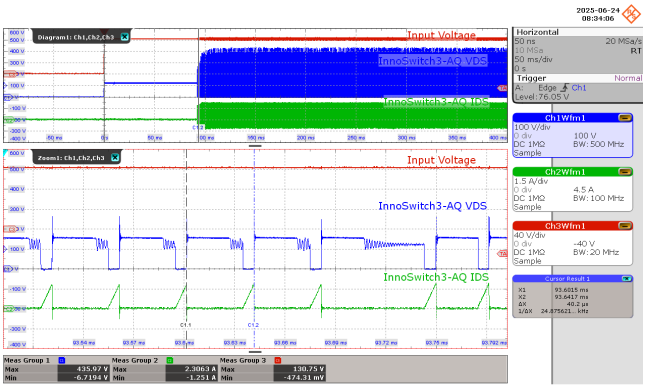


Figure 32 – INN3990CQ Drain Voltage and Current.
120 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 436 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.31 A)
CH3: V_{IN}, 40 V / div.
Time: 50 ms / div.

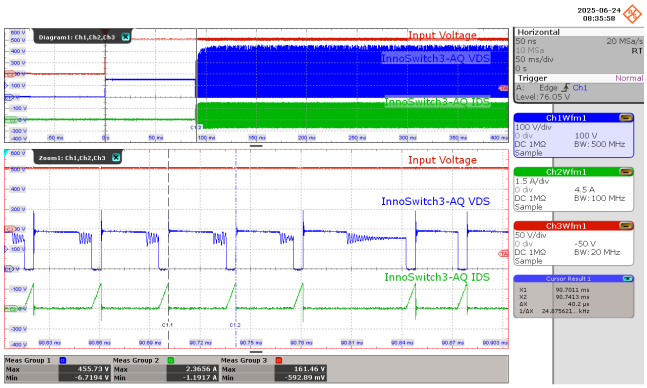


Figure 33 – INN3990CQ Drain Voltage and Current.
150 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 456 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.37 A)
CH3: V_{IN}, 50 V / div.
Time: 50 ms / div.

11.1.4 SR FET Drain Voltage and Current at Room Temperature

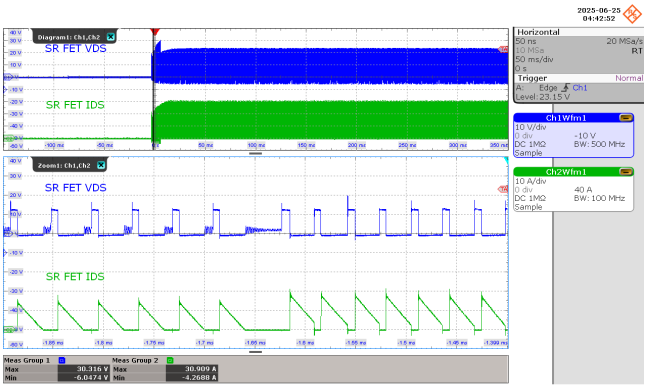


Figure 34 – SR FET Drain Voltage and Current.
100 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 30.3 V)
CH2: I_{DS}, 10 A / div. (Max = 30.9 A)
Time: 50 ms / div.

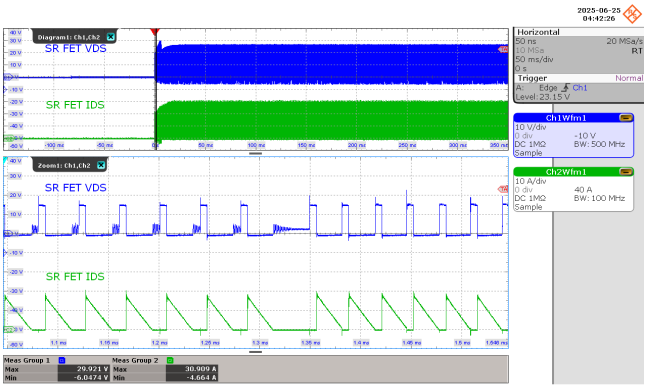


Figure 35 – SR FET Drain Voltage and Current.
120 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 29.9 V)
CH2: I_{DS}, 10 A / div. (Max = 30.9 A)
Time: 50 ms / div.

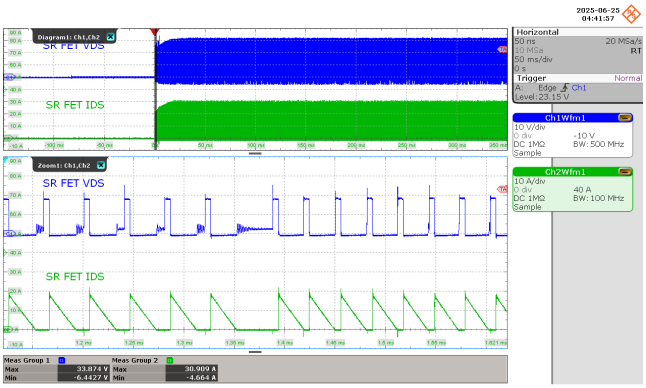


Figure 36 – SR FET Drain Voltage and Current.
150 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 33.9 V)
CH2: I_{DS}, 10 A / div. (Max = 30.9 A)
Time: 50 ms / div.

11.2 Start-Up Waveforms at Peak Power

11.2.1 Output Voltage and Current at Room Temperature (CC Mode)

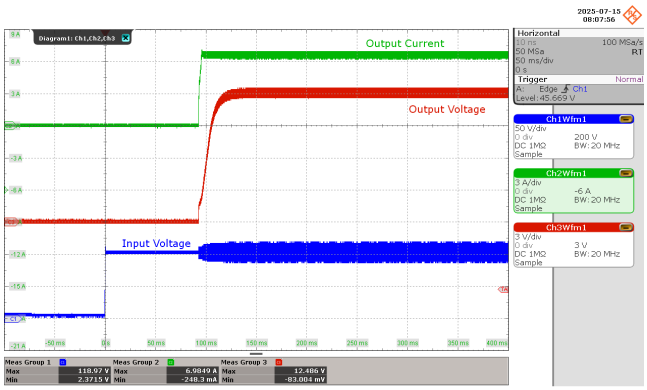


Figure 37 – Output Voltage and Current.
100 VDC, 6.67 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

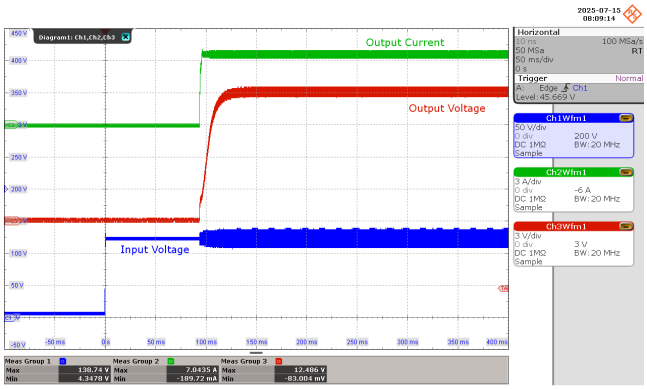


Figure 38 – Output Voltage and Current.
120 VDC, 6.67 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

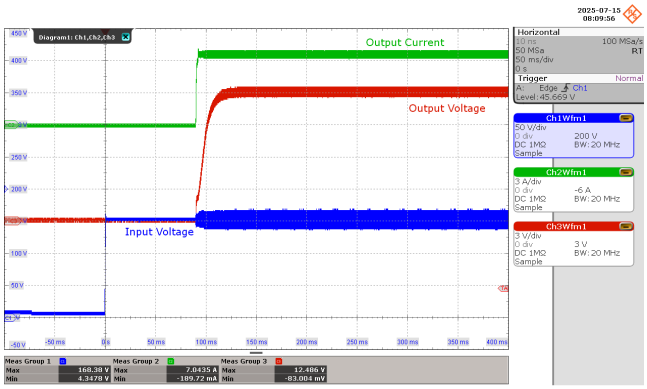


Figure 39 – Output Voltage and Current.
150 VDC, 6.67 A Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

11.2.2 Output Voltage and Current at Room Temperature (CR Mode)

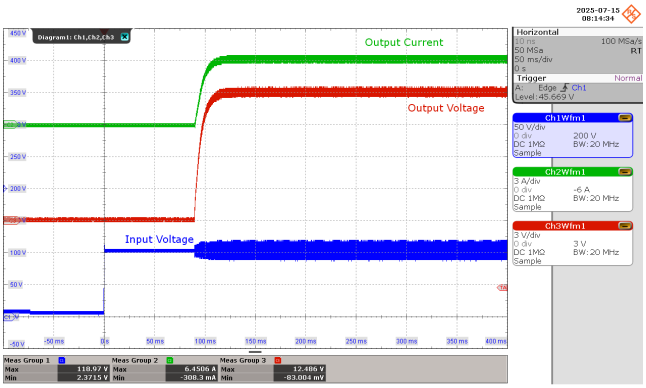


Figure 40 – Output Voltage and Current.
100 VDC, 1.8 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

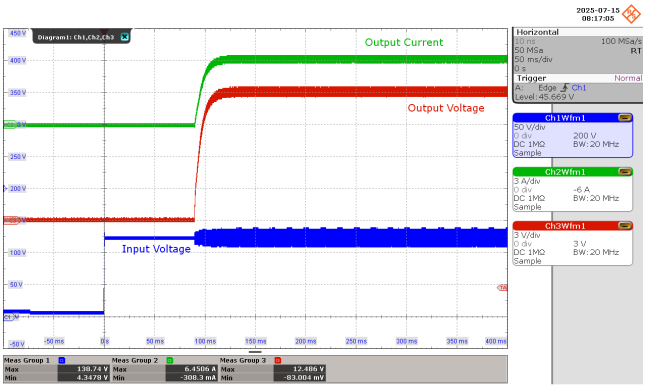


Figure 41 – Output Voltage and Current.
120 VDC, 1.8 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

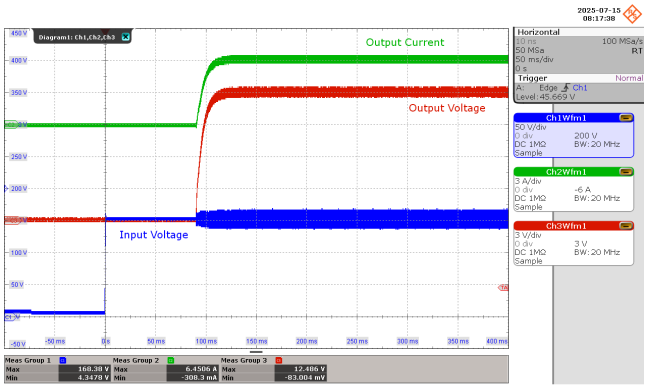


Figure 42 – Output Voltage and Current.
150 VDC, 1.8 Ω Load.
CH1: V_{IN}, 50 V / div.
CH2: I_{OUT}, 3 A / div.
CH3: V_{OUT}, 3 V / div. (Max = 12.5 V)
Time: 50 ms / div.

11.3 Steady-State Waveforms at Nominal Power

11.3.1 InnoSwitch3-AQ Drain Voltage and Current at Room Temperature

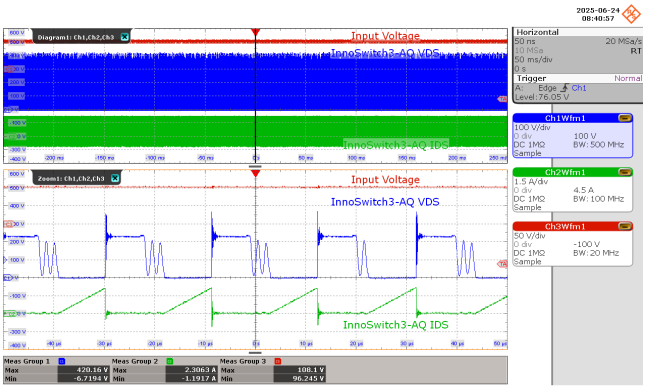


Figure 43 – INN3990CQ Drain Voltage and Current.
100 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 420 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.31 A)
CH3: V_{IN}, 50 V / div.
Time: 50 ms / div.

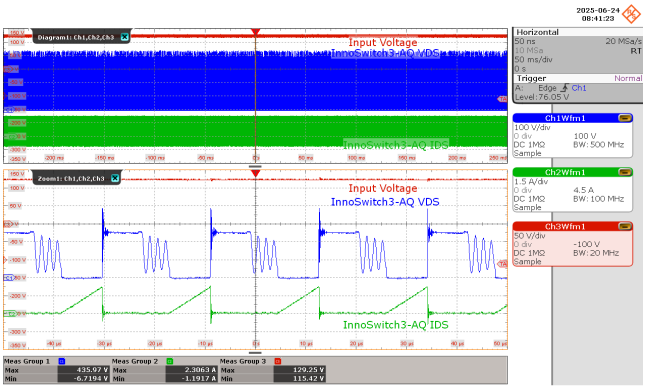


Figure 44 – INN3990CQ Drain Voltage and Current.
120 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 436 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.31 A)
CH3: V_{IN}, 50 V / div.
Time: 50 ms / div.

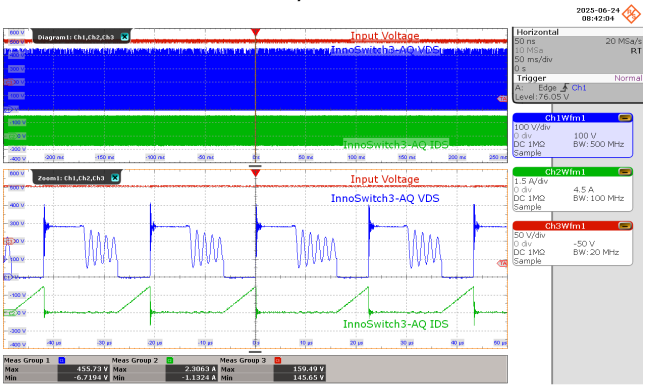


Figure 45 – INN3990CQ Drain Voltage and Current.
150 VDC, 3.84 A Load.
CH1: V_{DS}, 100 V / div. (Max = 456 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.31 A)
CH3: V_{IN}, 50 V / div.
Time: 50 ms / div.

11.3.2 SR FET Drain Voltage and Current at Room Temperature

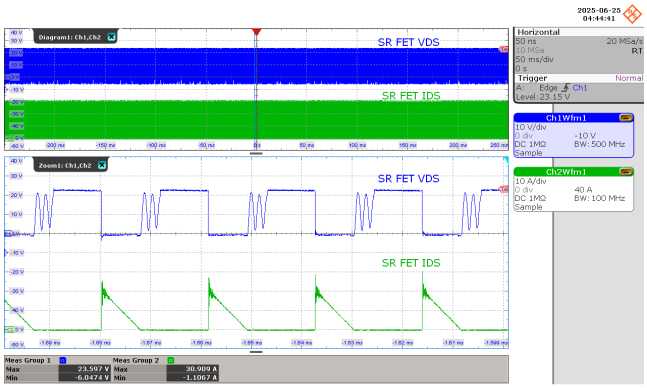


Figure 46 – SR FET Drain Voltage and Current.
100 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 23.6 V)
CH2: I_{DS}, 10 A / div. (Max = 30.9 A)
Time: 50 ms / div.

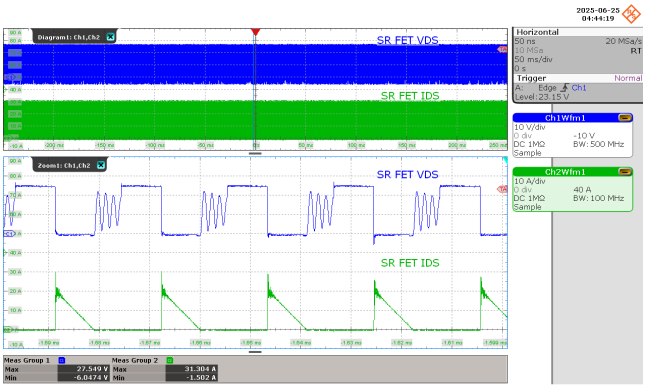


Figure 47 – SR FET Drain Voltage and Current.
120 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 27.5 V)
CH2: I_{DS}, 10 A / div. (Max = 31.3 A)
Time: 50 ms / div.

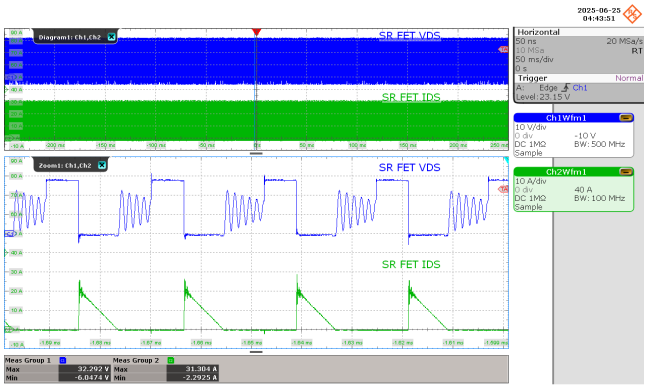


Figure 48 – SR FET Drain Voltage and Current.
150 VDC, 3.84 A Load.
CH1: V_{DS}, 10 V / div. (Max = 32.3 V)
CH2: I_{DS}, 10 A / div. (Max = 31.3 A)
Time: 50 ms / div.

11.4 Short-Circuit Response at Room Temperature

The unit was tested by applying an output short circuit during startup and normal operation. During normal operation, the short circuit was removed to see if the unit could recover and operate normally. The expected response during short circuit is for the unit to go to auto-restart (AR) mode and attempt recovery every 1.7 to 2.11 seconds. The full load setting was 3.125 Ω constant resistance.

11.4.1 Startup Short

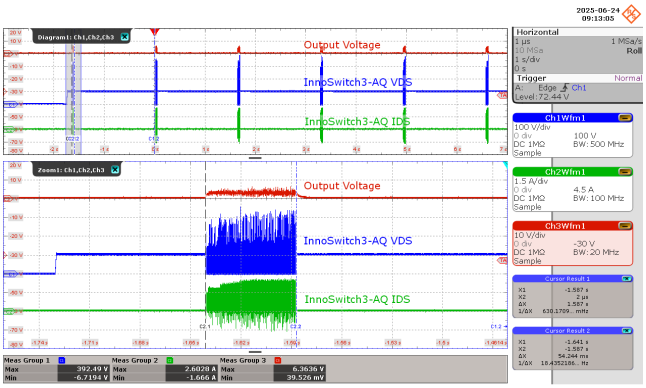


Figure 49 – INN3990CQ Drain Voltage and Current.
100 VDC, Output Short.
CH1: V_{DS}, 100 V / div. (Max = 392 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.60 A)
CH3: V_{OUT}, 10 V / div.
Time: 1 s / div.

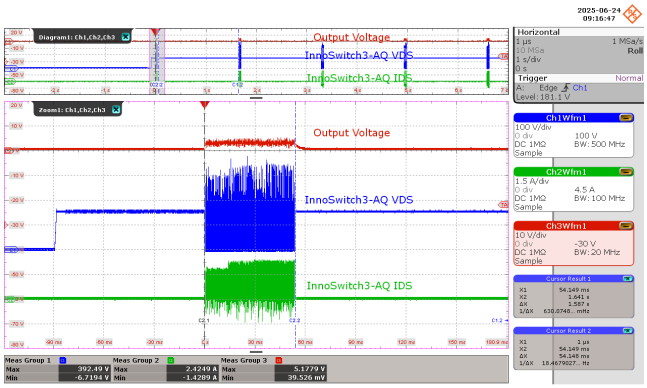


Figure 50 – INN3990CQ Drain Voltage and Current.
150 VDC, Output Short.
CH1: V_{DS}, 100 V / div. (Max = 392 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.42 A)
CH3: V_{OUT}, 10 V / div.
Time: 1 s / div.

11.4.2 Normal Operation to Short

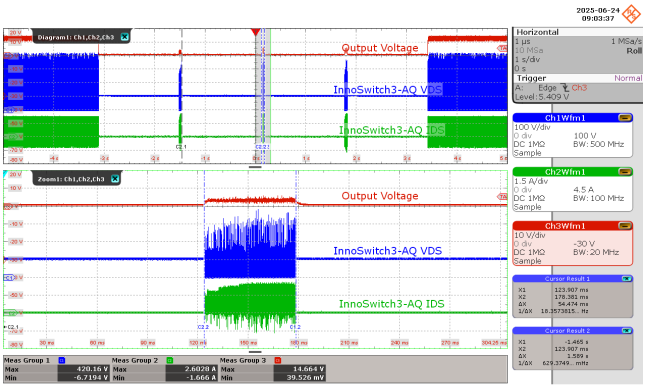


Figure 51 – INN3990CQ Drain Voltage and Current.
100 VDC, Output Short.
CH1: V_{DS}, 100 V / div. (Max = 420 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.60 A)
CH3: V_{OUT}, 10 V / div.
Time: 1 s / div.

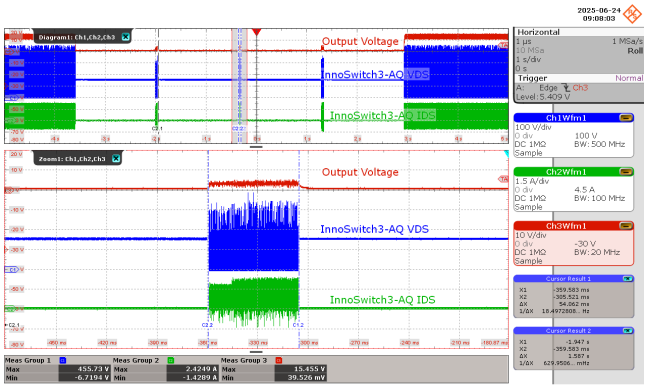


Figure 52 – INN3990CQ Drain Voltage and Current.
150 VDC, Output Short.
CH1: V_{DS}, 100 V / div. (Max = 456 V)
CH2: I_{DS}, 1.5 A / div. (Max = 2.42 A)
CH3: V_{OUT}, 10 V / div.
Time: 1 s / div.

11.5 Load Transient Response

The output voltage waveform was captured during a dynamic load transient from 0% to 100% of nominal load and from nominal power to peak power.

Test condition: Dynamic load frequency = 10 Hz, Duty Cycle = 50%, Slew Rate = 0.8 A / µs.

11.5.1 Output Voltage Ripple from 0% - 100% - 0% Transient Load at Room Temperature.

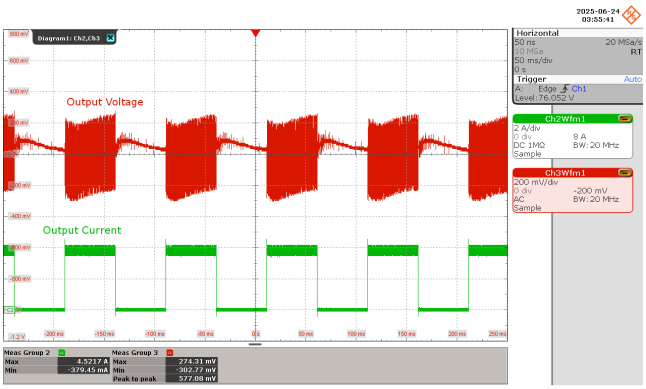


Figure 53 – Output Voltage and Current.
100 VDC, 0 A - 3.84 A - 0 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 274 mV, Min = -303 mV)
Time: 50 ms / div.

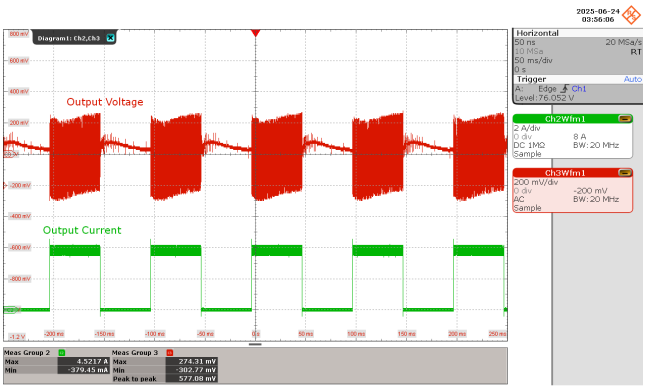


Figure 54 – Output Voltage and Current.
120 VDC, 0 A - 3.84 A - 0 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 274 mV, Min = -303 mV)
Time: 50 ms / div.

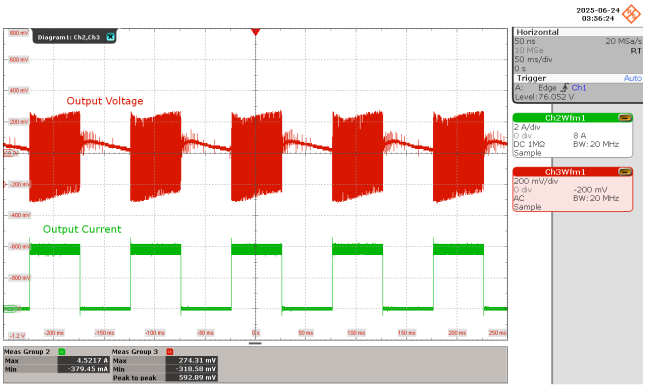


Figure 55 – Output Voltage and Current.
150 VDC, 0 A - 3.84 A - 0 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 274 mV, Min = -319 mV)
Time: 50 ms / div.

11.5.2 Output Voltage Ripple from nominal power – peak power – nominal power Transient Load at Room Temperature.

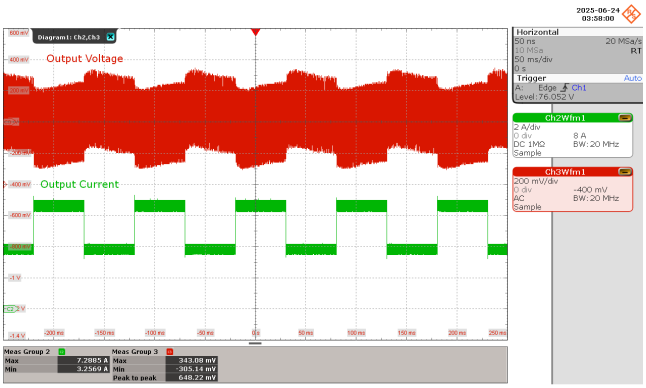


Figure 56 – Output Voltage and Current.
100 VDC, 3.84 A - 6.67 A - 3.84 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 343 mV, Min = -305 mV)
Time: 50 ms / div.

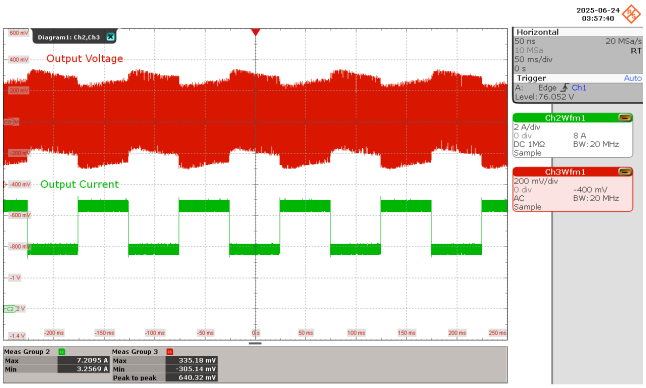


Figure 57 – Output Voltage and Current.
120 VDC, 3.84 A - 6.67 A - 3.84 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 335 mV, Min = -305 mV)
Time: 50 ms / div.

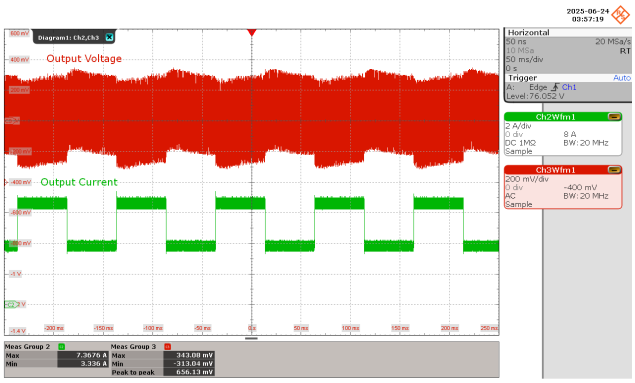


Figure 58 – Output Voltage and Current.
150 VDC, 3.84 A - 6.67 A - 3.84 A Transient Load
CH2: I_{OUT}, 2 A / div.
CH3: V_{RIPPLE}, 200 mV / div. (Max = 343 mV, Min = -313 mV)
Time: 50 ms / div.

11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

A modified oscilloscope test probe must be utilized for DC output ripple measurements to reduce spurious signals due to noise pick-up. Details of the probe modification are provided in 59 and Figure 60 below.

A 4987BA probe adapter was affixed with two capacitors tied in parallel to the probe tip and GND terminal. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). A twisted pair of wires, kept as short as possible, were soldered directly between the probe adapter and the output terminals.

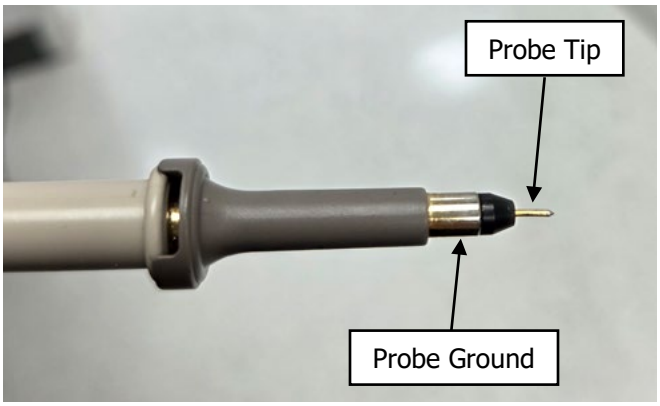


Figure 59 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

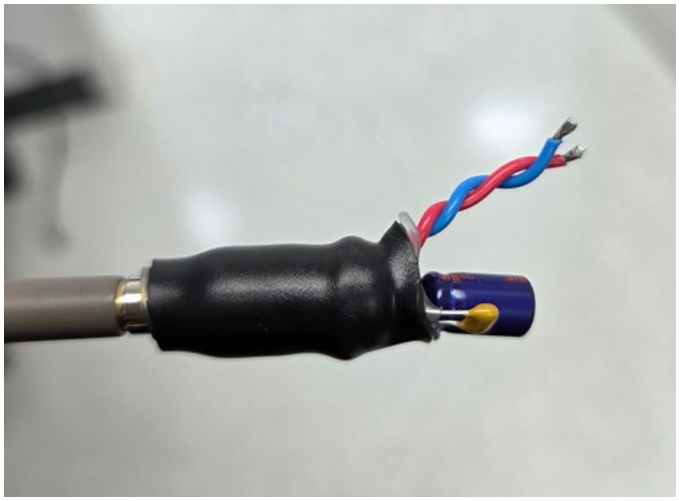


Figure 60 – Oscilloscope Probe with Probe Master (https://probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurements, and two parallel decoupling capacitors added.)

11.6.2 Output Voltage Ripple Waveforms at Nominal Power

Output voltage ripple waveform was captured at the output terminals using the ripple measurement probe with a decoupling capacitor running at nominal power. The waveforms shown were taken at the load setting where the highest ripple was observed and repeated for a range of input voltages.

11.6.2.1 Output Voltage Ripple at Room Temperature with Constant Full Load

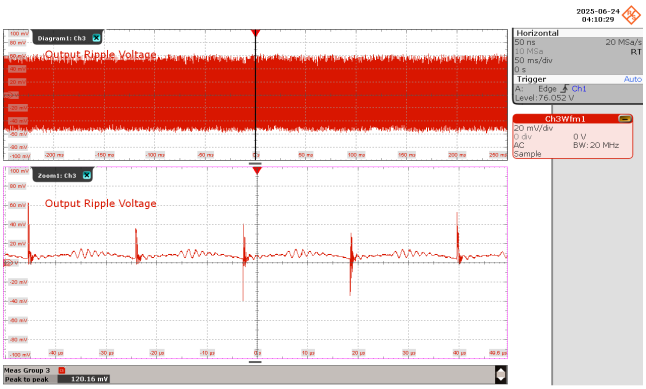


Figure 61 – Output Voltage Ripple.
100 VDC, 3.84 A Load.
CH3: V_{RIPPLE}, 20 mV / div.
Time: 50 ms / div.
V_{RIPPLE_PK-PK} = 120 mV.

Figure 62 – Output Voltage Ripple.
120 VDC, 3.84 A Load.
CH3: V_{RIPPLE}, 20 mV / div.
Time: 50 ms / div.
V_{RIPPLE_PK-PK} = 124 mV.

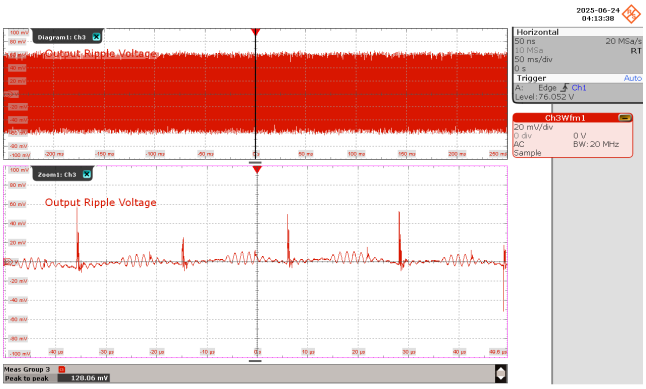


Figure 63 – Output Voltage Ripple.
150 VDC, 3.84 A Load.
CH3: V_{RIPPLE}, 20 mV / div.
Time: 50 ms / div.
V_{RIPPLE_PK-PK} = 128 mV.

11.6.3 Output Ripple vs. Load

11.6.3.1 Output Ripple at Room Temperature

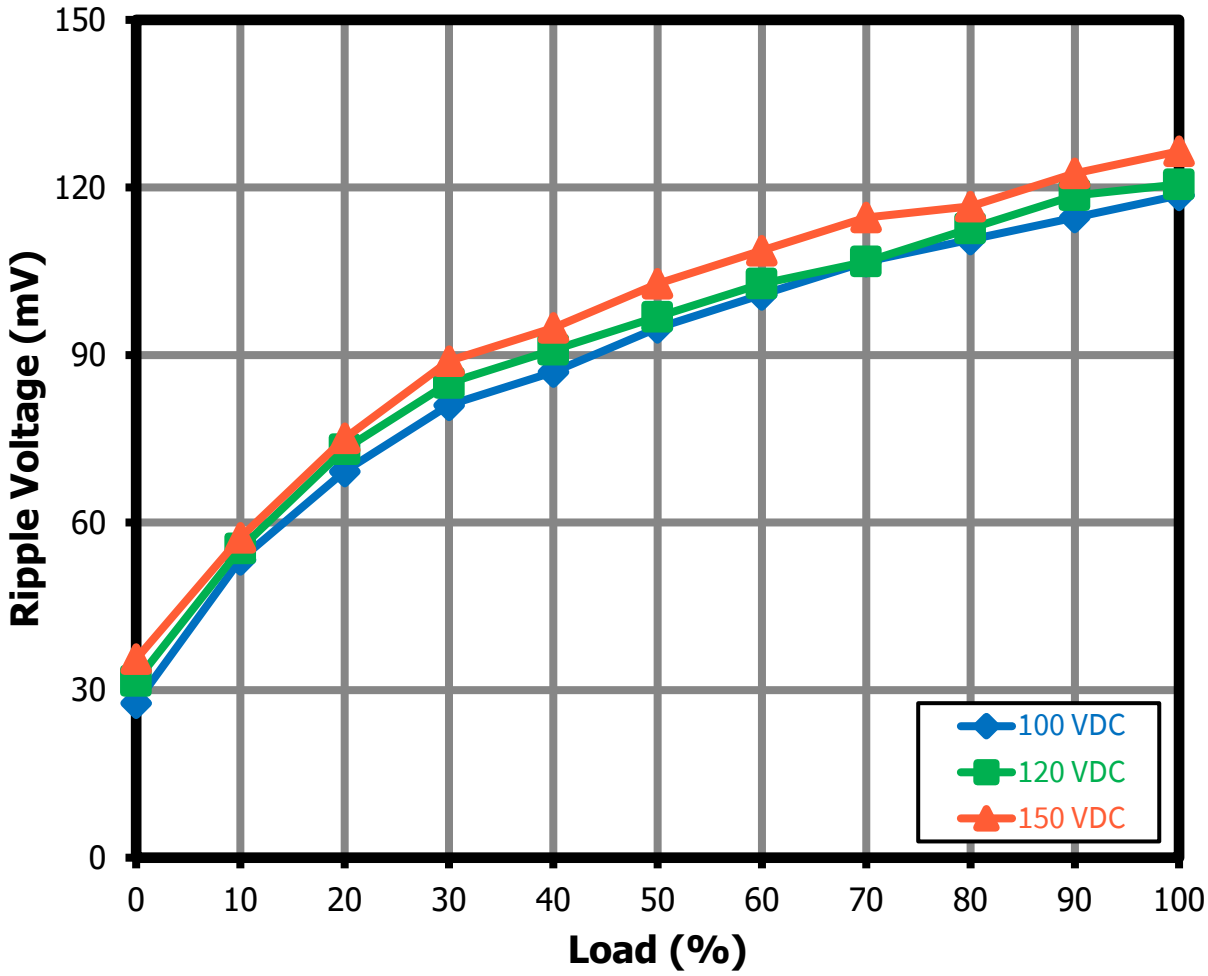


Figure 64 – Output Ripple Voltage Across Nominal Load Range at Different Input Voltages.

12 Output Overload

The overload protection of the INN3990CQ-H607 device is configured such that once the load current reaches the current limit threshold set by the IS pin resistor(s), the output voltage will fold back, and auto-restart will occur once the output voltage falls below 90% of regulation for a time period exceeding the AR timer.

The prototype unit was tested to verify at what specific output current it will trigger the overload protection of the IC. For every loading condition, unit under test was allowed to stabilize for 5 seconds before output voltage and current measurements were taken.

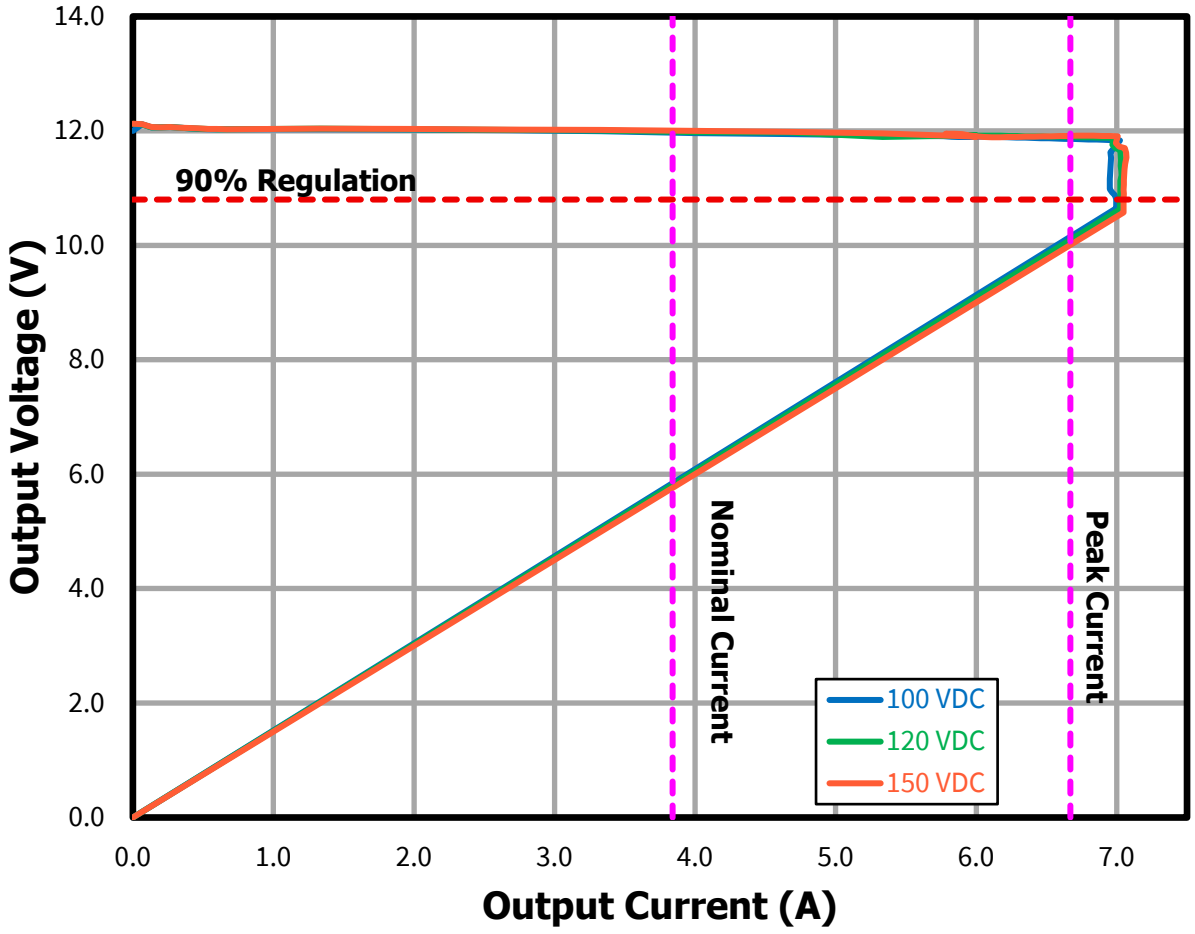


Figure 65 – 12 V Output Overload Curve at Room Temperature.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
24-Jul-25	MJL	A	Initial Release.	Apps & Mktg

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