Title	***60 W Flyback Converter with Two Independently Regulated Outputs Using InnoMux™2-EP IMX2353F-H415***
Specification	70 VDC – 1000 VDC Input 300 VDC – 1000 VDC: 60 W 70 VDC: 3 W Output 1: 5 V 2.5 A Output 2: 24 V 2 A
Application	Industrial and Appliance Applications
Author	Applications Engineering Department
Document Number	RDR-1053
Date	November 07, 2024
Revision	A

Summary and Features

Unique single-stage conversion, multi-output, flyback architecture.

- Ultra-wide range input
- >90% full load efficiency
  - Zero Voltage switching (ZVS)
  - 1700 V PowiGaN™ primary switch
  - Synchronous rectification (SR)
- Constant high efficiency across input voltage and load range
- Accurate regulation – better than ±1% across line and load
- Safety features
  - Output overvoltage protection (OVP)
  - Accurate thermal protection with hysteretic shutdown

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a switch-mode power supply (SMPS) intended for appliance and industrial applications, utilizing IMX2353F-H415 from the InnoMux2-EP family of ICs.

The SMPS features two Constant Voltage (CV) outputs and can deliver a maximum total output power of 60 W, with an input voltage of up to 1000 VDC. This design demonstrates high efficiency and accurate output regulation, made possible by InnoMux-2's multiplexing power control algorithm and a high level of integration.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

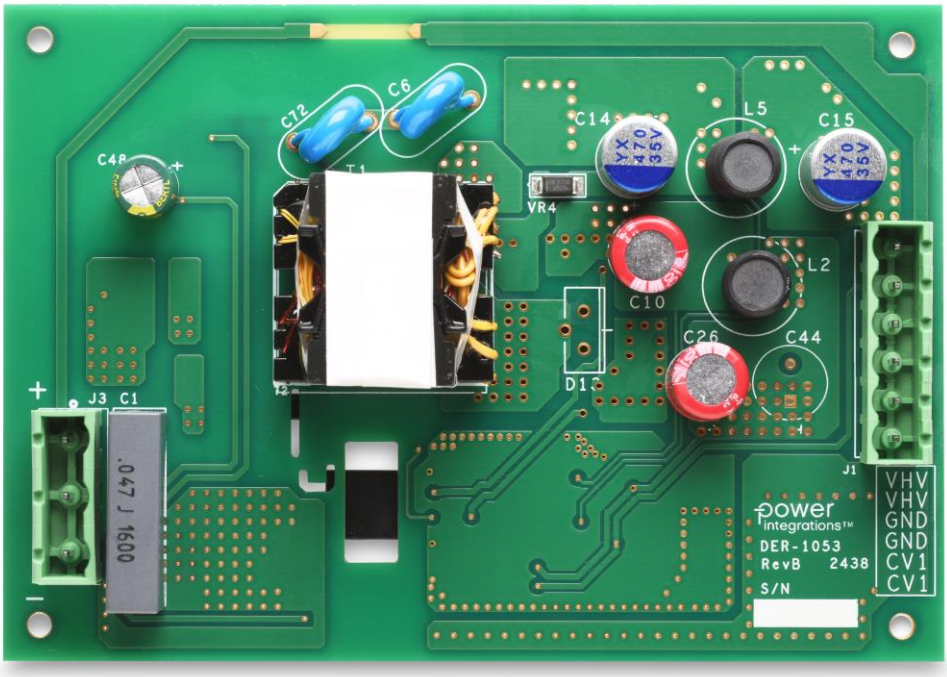


Figure 1 – Populated Circuit Board Photograph, Top View.

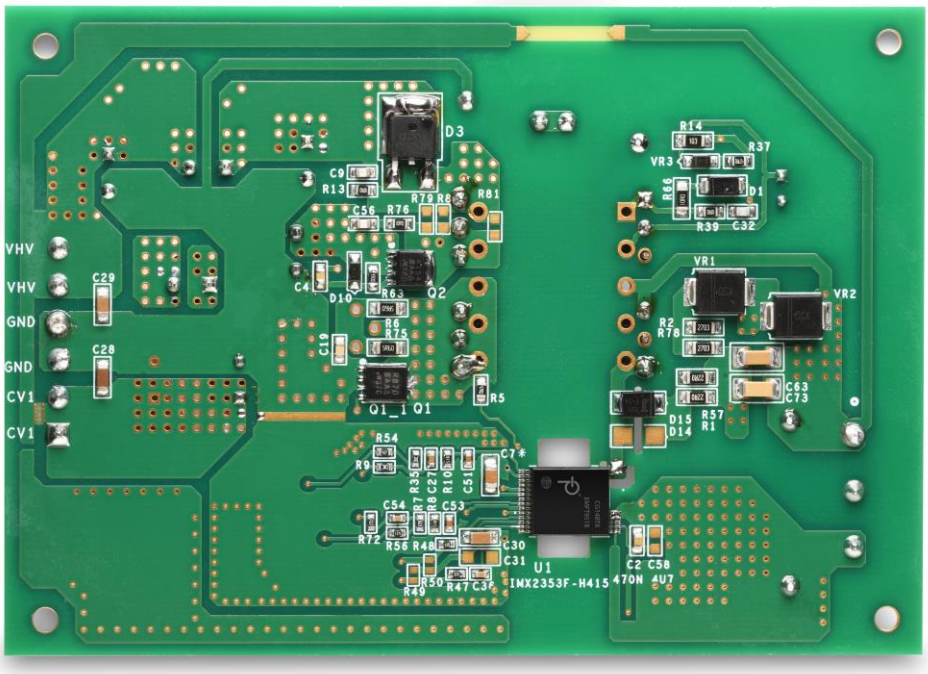


Figure 2 – Populated Circuit Board Photograph, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	70		1000	VDC	
Output						
VCV1						
Rated Voltage	V_{CV1}		5.10		V	±1% initial set point tolerance from factory
Line and Load Regulation[1]			±1%			Measured from 300 to 1000 VDC, 0% to 100% load
Dynamic Response			±5%			0-100% load step
Ripple Voltage	V_{CV1_RIPPLE}			150	mV	±1.5%, 20 MHz bandwidth
Rated Current	I_{CV1}		2.5		A	
VCVHV						
Rated Voltage	V_{CVHV}		24		V	±1% initial set point tolerance from factory
Line and Load Regulation[1]			±1%			Measured from 300 to 1000 VDC, 0% to 100% load
Dynamic Response			±5%			0-100% load step
Ripple Voltage	V_{CVHV_RIPPLE}			480	mV	±1%, 20 MHz bandwidth
Rated Current	I_{CVHV}		2		A	
Total Output Power						
Output Power	P_{OUT}		60		W	300 – 1000 VDC input, CV1 12 W CVHV 40 W
			40		W	200 VDC input, CV1 8 W CVHV 32W
			15		W	100 VDC input, CV1 5 W CVHV 10 W
			3		W	70 VDC input, CV1 1W CVHV 2 W
Efficiency						
Full Load	η		90		%	Measured at 800 VDC, 25 ºC
Standby Input Power				<0.3	W	Measured at 800 VDC, 25 ºC, CV1 150 mW
Environmental						
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Table 1 – Power Supply Specifications.

Note:
1. Measured across both input line and load change

3 Schematic

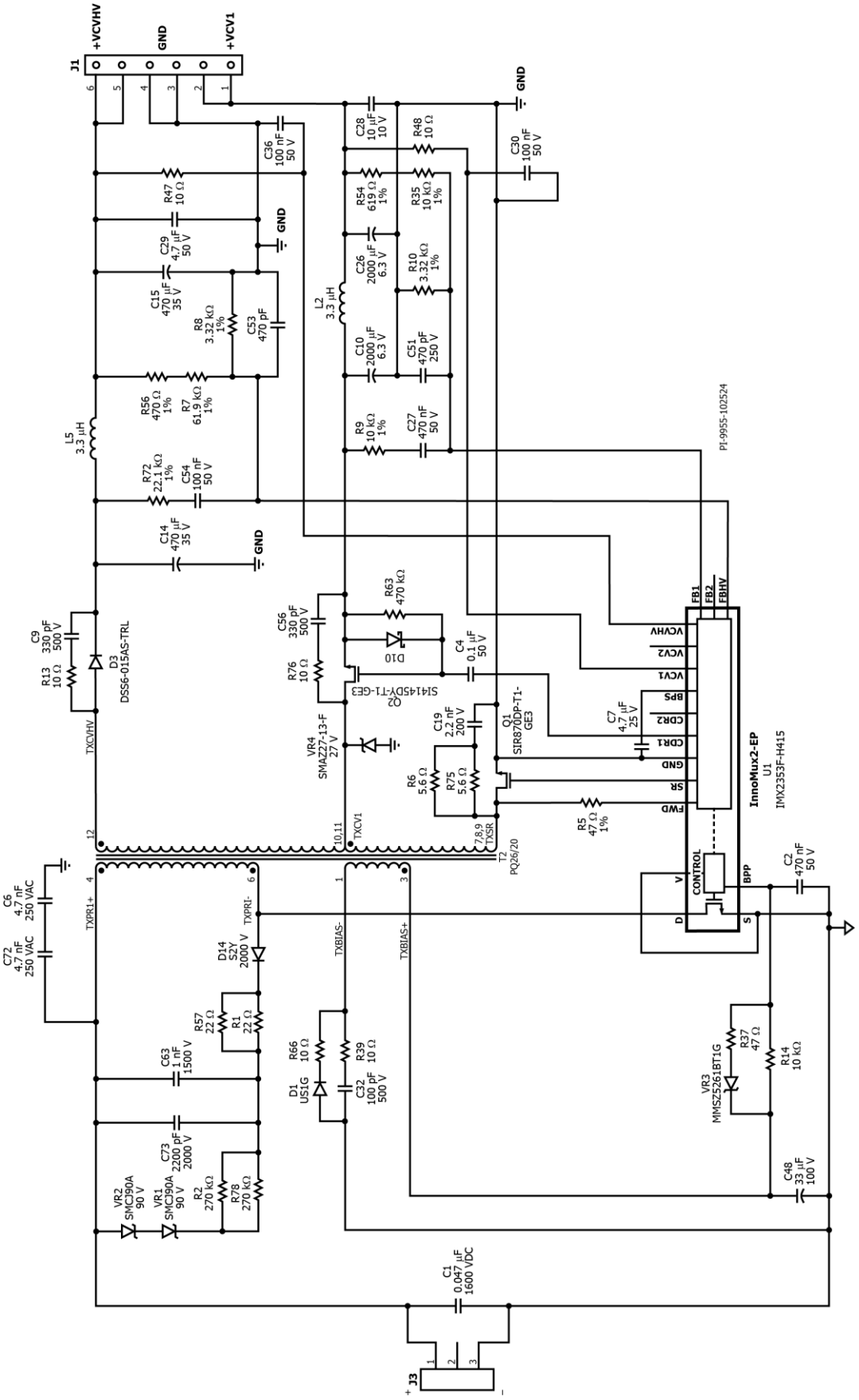


Figure 3 – Full Schematic

4 Circuit Description

4.1 Primary-Side

4.1.1 Input Capacitor

The film capacitor C1 is connected in parallel with the DC input connector J3, and provides filtering for ripple on the DC input.

4.1.2 Primary Switching Circuit

The primary side of the transformer is connected between the input DC bus (TXPRI+) and the drain of the integrated primary switch of InnoMux2-EP IC (U1, pin 28). The primary current loop closes at the negative terminal of C2 via the S pin (tab) of U1 (pin 18/19). An RCD-type primary clamp (D14, R1, R57, R2, R78, VR1, VR2, C63 and C73) is used to limit the peak drain voltage spike on the integrated primary switch, caused by the leakage inductance of the transformer when the switch turns off.

4.1.3 Primary-Side Controller Power Source

The primary-side controller is integrated into the InnoMux2-EP IC (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor (C2) when AC voltage is first applied to the converter input. During normal operation (steady-state), the primary-side controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D1 and capacitor C48. Resistor R66 is inserted into the discharge circuit to limit transient current. The output of the primary-side auxiliary supply is connected to the BPP pin via a current-limiting resistor, R14.

4.1.4 Primary-Side OVP

Primary-side output overvoltage protection (OVP) is implemented by the Zener diode VR3 and series resistor R37. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding causes the Zener diode VR3 to conduct, increasing the current into the BPP pin. If this current exceeds the I_{SD} limit (7.5 mA), OVP protection is triggered, and the controller implements a latching shutdown.

4.1.5 Primary Peak Current Limit

The value of capacitor C2 is used to set the maximum primary current to either STANDARD or INCREASED level. In this case, a 470 nF capacitor sets the primary-side controller peak current limit to its STANDARD level of 1.85 A.

4.2 Secondary-Side

The secondary side of the InnoMux2-EP IC (U1) is powered from an internal regulator connected to BPS pin (U1, pin 6). At the beginning of startup, power for the BPS regulator is provided by the FORWARD pin (U1, pin 10). Capacitor C7 is a decoupling capacitor.

4.2.1 Primary to Secondary-Side Communication

The secondary side of the InnoMux2-EP IC (U1) sends a request to the primary-side controller to initiate a switching cycle. This is done by sending a pulse via the internal safety-isolated FluxLink™ communication channel.

4.2.2 InnoMux2-EP Power Supply

During startup, the InnoMux2-EP secondary-side controller is also powered from CVHV via resistor R47. A local decoupling capacitor, C36, is connected close to the VCVHV pin of U1. Resistor R47 and C36 are optional and provide additional ESD protection. The internal regulator lowers the VCVHV voltage to 5 V and supplies it to the BPS rail.

In steady-state operation, when the voltage on VCV1 (U1, pin 11) rises to the BPS Direct Power Range threshold, $V_{CV5V(BPS)}$ (4.65 V~5.45 V), the internal BPS regulator switches off, and the secondary-side controller is powered directly from VCV1. This direct power mode operation reduces the power consumption on the BPS regulator. Resistor R48 and capacitor C30 provide local decoupling and ESD protection.

4.2.3 Synchronous Rectifier (SR) MOSFET Drive

The SR pin drives the synchronous rectifier (SR) MOSFET (Q1) when the transformer is delivering energy to the secondary circuit. Before the end of secondary discharge, the gate voltage of the SR MOSFET is reduced to maintain a fixed source-to-drain voltage across the SR MOSFET. This functionality plays a crucial role in preventing the premature turn-off of the SR MOSFET.

In DCM operation, the SR MOSFET (Q1) is turned on for a short period just before the primary switch turns on. This action generates a reverse current in the CV1 secondary winding, which then commutates to cause a reverse current flow in the transformer on the primary side when the SR MOSFET turns off. Subsequently, the reverse current discharges the voltage across the primary switch, allowing it to turn on at zero (or near zero) voltage. This mechanism, termed SR-ZVS, substantially minimizes switching loss, significantly reducing the turn-on loss for the primary switch, especially with high input voltage.

4.2.4 Selection MOSFET Drive for Q2

The gate drive amplitude for the selection MOSFET (Q2) is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic-level MOSFETs must be used. When the CDR1 pin voltage is low, capacitor C4 is charged up to the level of V_{CV1} from the CV1 output via diode D10. When the selection MOSFET Q2 needs to turn on, the CDR1 pin voltage rises from GND to BPS, causing the gate voltage of the selection MOSFET to rise to $V_{CV1}+V_{BPS}$.

The secondary control circuit in the InnoMux2-EP IC requires access to the idle ring waveform through the FWD pin to calculate timing and facilitate SR ZVS. This access is ensured by keeping the selection MOSFET (Q2) on even after the secondary conduction time is completed.

4.2.5 Output Control

Output rectification for the CV1 output is provided by the SR MOSFET (Q1) and the CV1 selection MOSFET (Q2). To ensure low output ripple voltage, a Π filter consisting of capacitors C10, C26 and inductor L2 is employed. A low ESR capacitor, C10, is used in the first stage to attenuate ripple current, while capacitor C26, an aluminum polymer type, minimizes switching noise. Additionally, a multilayer ceramic capacitor (MLCC), C28, is connected across the CV1 output terminals to provide a low-impedance bypass for any high-frequency noise.

Output rectification for the CVHV output is provided by SR MOSFET (Q1) and diode D3. Low-ESR capacitors, C14 and C15, serve as energy storage and filtering components at the CVHV output. An inductor L5 is inserted between C14 and C15 to further reduce ripple and noise at the CVHV output.

The RC snubber network consisting of R6, R75 and C19 serves to dampen high-frequency ringing across the SR MOSFET (Q1). This ringing results from the oscillation of transformer leakage inductance and secondary trace inductance with the MOSFET body capacitance. Another RC snubber network, made up of R76 and C56, dampens high-frequency ringing across the CV1 selection MOSFET Q2. Finally, an RC snubber network, comprising R13 and C9, reduces high-frequency voltage transients across the CVHV diode (D3).

When both the selection MOSFET (Q2) and the SR FET (Q1) are turned on, the transformer secondary windings are designed so that the voltage on the anode of D3 is below VCVHV. As a result, D3 remains reverse-biased, ensuring that all the transformer energy is directed to the CV1 output through Q1.

When the selection MOSFET (Q2) is turned off and the SR MOSFET (Q1) is turned on, the voltage on the anode of D3 rises until it becomes forward-biased. In this state, all transformer energy is directed to the CVHV output.

The output voltage on CV1 is controlled by R35, R54, R10 and C51, which provide an analog current signal to FB1 (U1, pin 1). Loop compensation is necessary due to the use of L2 and is provided by R9 and C27. The CVHV output voltage is set by R7, R56, R8 and C53 which deliver a current to FBHV (U1, pin 8). Loop compensation is necessary due to the use of L5 and is provided by R72 and C54.

5 PCB Layout

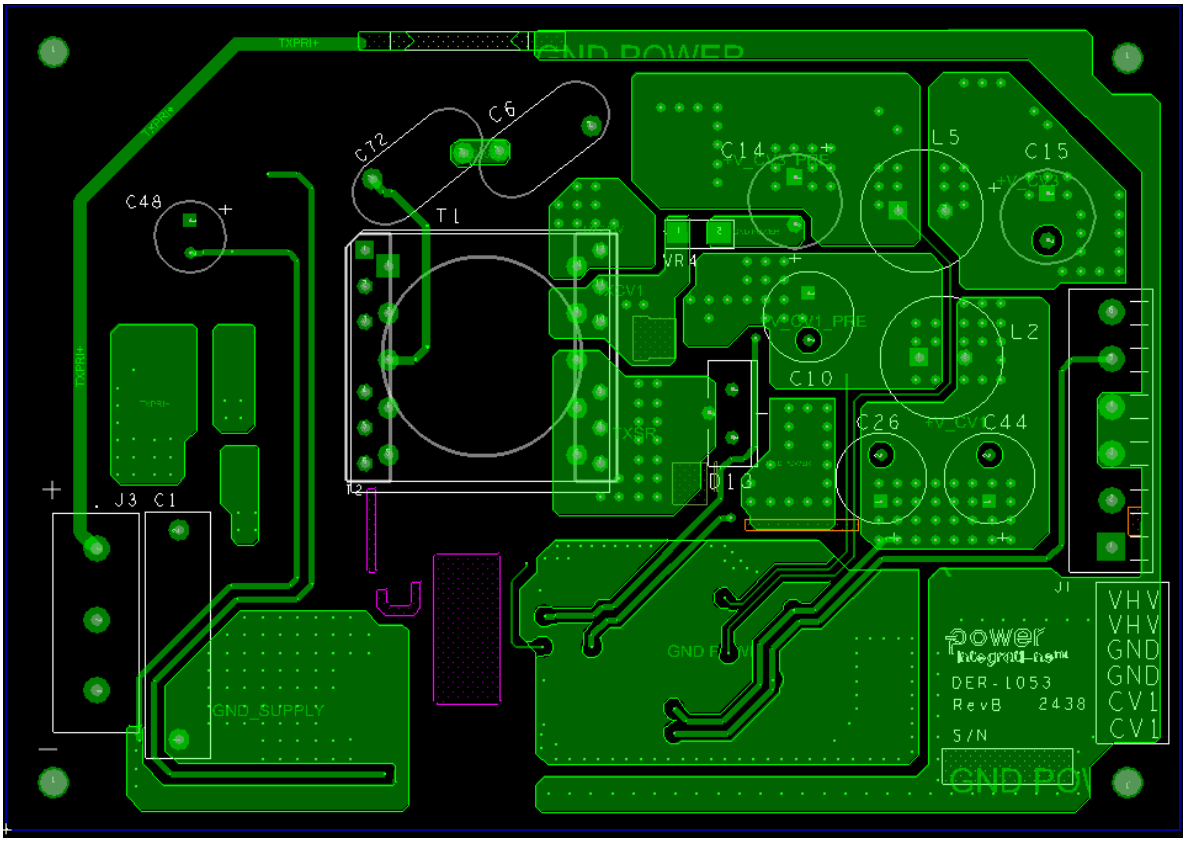


Figure 4 – Printed Circuit Board Layout, Top

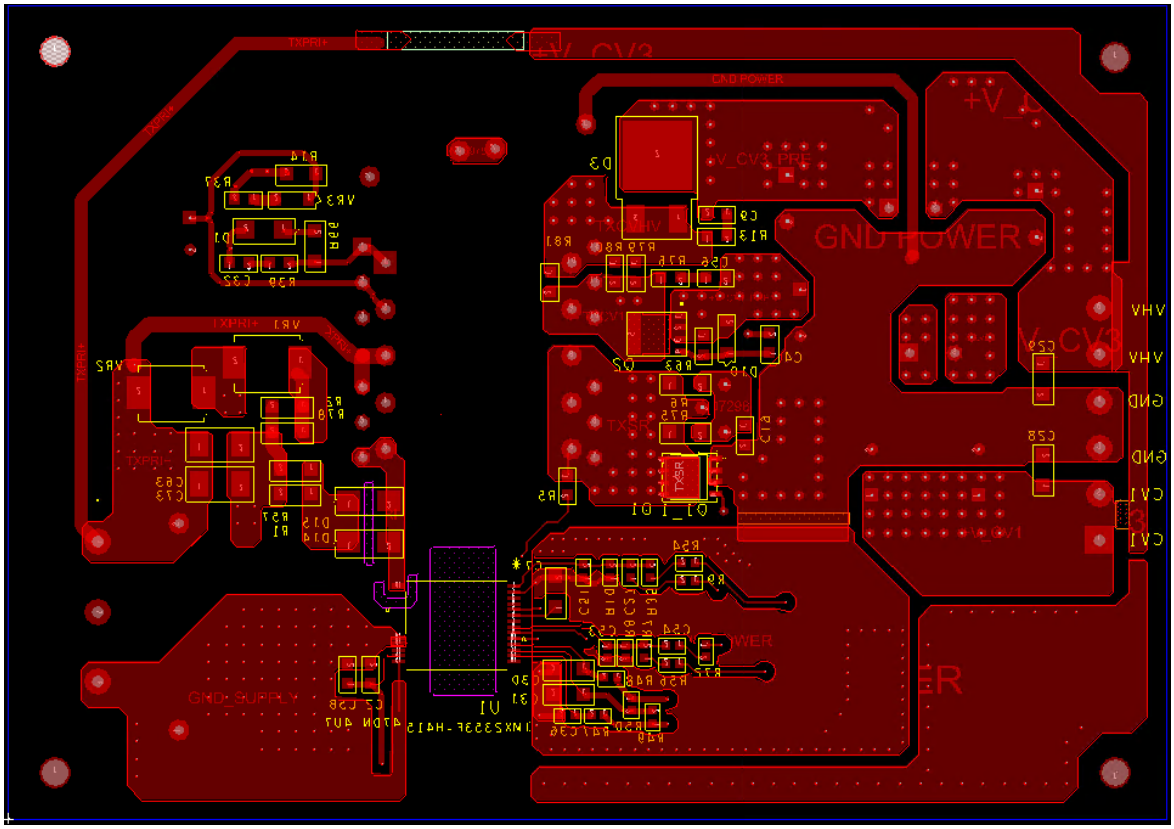


Figure 5 – Printed Circuit Board Layout, Bottom.

6 Bill of Materials

Item	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	C1	0.047 µF, ±5%, Film Capacitor, Automotive, AEC-Q200, 650VAC, 1600VDC (1.6kVDC), Polypropylene (PP), Metallized Radial	R76TN24704040J	KEMET
2	C2	470 nF, ±10%,50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung Electro-Mechanics
3	C4	OPS|CAP|0.1 µF ±10% 50V Ceramic, X7R 0805	VJ0805Y104KBABE31	Vishay Vitramon
4	C6	4.7 nF, Ceramic, Y1	440LD47-R	Vishay
5	C7	4.7 uF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
6	C9	330 pF, 500 V, Ceramic, X7R, 0805	C0805C331KCRACTU	Panasonic
7	C10	2000 µF, ±20%, 6.3 V, Aluminum - Polymer Capacitors Radial, Can, 9mOhm, 2000 Hrs @ 125°C ,(10 x 12.5)	870135175009	Würth Elektronik
8	C14	470 uF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
9	C15	470 uF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
10	C19	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX Corp
11	C26	2000 µF, ±20%, 6.3 V, Aluminum - Polymer Capacitors Radial, Can, 9mOhm, 2000 Hrs @ 125°C ,(10 x 12.5)	870135175009	Würth Elektronik
12	C27	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
13	C28	10 µF, ±10%, 10V, Ceramic Capacitor X7R,AEC-Q200, 1206 (3216 Metric)	CL31B106KPHVPNE	Samsung Electro-Mechanics America, Inc.
14	C29	4.7 uF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
15	C30	100 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB104	Yageo
16	C32	100 pF, 500 V, Ceramic, NP0, 0805	501R15N101KV4T	Johanson Dielectrics Inc.
17	C36	0.1 µF(100 nF) ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
18	C48	33 uF,±20%, 100 V, Al Electrolytic, Gen. Purpose, Can, (8mm x 13mm)	EEU-FS2A330B	Panasonic Electronic Components
19	C51	470 pF, ±10%, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B471KB8NFNC	Samsung
20	C53	470 pF, ±10%, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B471KB8NFNC	Samsung
21	C54	0.1 µF(100 nF) ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
22	C56	330 pF, 500 V, Ceramic, X7R, 0805	C0805C331KCRACTU	Panasonic
23	C63	1 nF, 1500 V, Ceramic, X7R, 1808	1808SC102KAT1A	AVX
24	C72	4.7 nF, Ceramic, Y1	440LD47-R	Vishay
25	C73	CAP, 2200 pF, ±10%, 2000V (2kV), Ceramic Capacitor X7R 1808 (4520 Metric)	C1808X222KGRAC7800	KEMET
26	D1	DIODE ULTRA FAST, GPP, 400V, 1A SMA	US1G-13-F	Diodes, Inc
27	D3	Diode 150 V 6A Surface Mount TO-252AA,TO-252-3, DPak (2 Leads + Tab), SC-63	DSS6-015AS-TRL	IXYS
28	D10	DIODE, SCHOTKY, 100V, 0.075A, SOD123	BAT46W-TP	Micro Commercial
29	D14	Diode, 2000 V, 2A, Surface Mount DO-214AA (SMB)	S2Y	Diotec Semiconductor
30	J1	CONN TERM BLOCK 5.08MM 6POS, Screw - Leaf Spring, Wire Guard	OSTTA064163	On Shore Technology Inc
31	J3	3 Position Wire to Board Terminal Block, Horizontal with Board, 0.300" (7.62mm) Through Hole	282845-3	TE Connectivity AMP Connectors
32	L2	FIXED IND, 3.3UH, ±20%,5.2A, 16 MOHM, TH	ELC-10E471L	PANASONIC ELECTRONIC COMPONENTS
33	L5	FIXED IND, 3.3UH, ±20%,5.2A, 16 MOHM, TH	ELC-10E471L	PANASONIC ELECTRONIC COMPONENTS
34	Q1	MOSFET, N-Channel 100 V 60A (Tc) 6.25W (Ta), 104W (Tc) Surface Mount PowerPAK® SO-8, PowerPAK SO-8	SIR870DP-T1-GE3	Vishay/Siliconix
35	Q2	MOSFET,N-Channel, 40V, 36A (Tc), 3.5W (Ta), 7.8W (Tc), Surface Mount, 8-SO	SI4154DY-T1-GE3	Vishay Siliconix
36	R1	RES, 22 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J220V	Panasonic
37	R2	RES, 270 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J274V	Panasonic
38	R5	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic

39	R6	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
40	R7	RES, 61.9 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6192V	Panasonic
41	R8	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
42	R9	RES, 10.0 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
43	R10	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
44	R13	RES, 10 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
45	R14	RES, 10 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J103V	Panasonic
46	R35	RES, 10.0 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
47	R37	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
48	R39	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
49	R47	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
50	R48	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
51	R54	RES, 619 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6190V	Panasonic
52	R56	RES, 470 R, 1%, 1/10 W, Thick Film, 0603 (1608 Metric)	ERJ-3EKF4700V	Panasonic
53	R57	RES, 22 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J220V	Panasonic
54	R63	RES, 470 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ474V	Panasonic
55	R66	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
56	R72	RES, 22.1 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2212V	Panasonic
57	R75	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
58	R76	RES, 10 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
59	R78	RES, 270 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J274V	Panasonic
60	T2	Bobbin, PQ26/20, Vertical, 12 pins Custom, RDK-1053 Transformer, PQ26/20.	B65878E0012D001 POL-INN065	EPCOS (TDK) Premier Magnetics
61	U1	IMX2353F-H415, InSOP-T28G	10-01592-00	Power Integrations
62	VR1	Tvs Diode, Unidirectional, 90V Reverse Standoff, 146V Clamp, 10.3A Ipp, Surface Mount SMC (DO-214AB)	SMCJ90A	TAIWAN SEMICONDUCTOR
63	VR2	Tvs Diode, Unidirectional, 90V Reverse Standoff, 146V Clamp, 10.3A Ipp, Surface Mount SMC (DO-214AB)	SMCJ90A	TAIWAN SEMICONDUCTOR
64	VR3	DIODE ZENER 47V 500MW SOD123	MMSZ5261BT1G	ON Semi
65	VR4	Zener Diode, 27 V, 1 W, ±5%, Surface Mount DO-214AC (SMA)	SMAZ27-13-F	Diodes Incorporated

Table 2 – Bill of Materials.

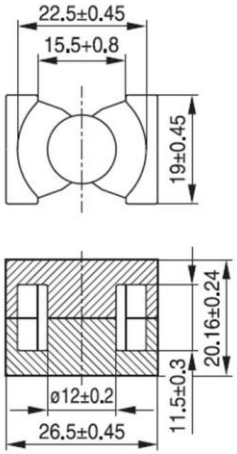
7 Transformer (T2) Specification

7.1 Core Information

PQ 26/20

Core **B65877B**

- To IEC 63093-13
- Delivery mode: sets



Magnetic characteristics (per set)

$\Sigma l/A$ = 0.362 mm^{-1}
l_e = 44.4 mm
A_e = 122.6 mm^2
A_{min} = 108.8 mm^2
V_e = 5440 mm^3

Approx. weight 31 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N49	3850 +30/–20%	1110	< 1.90 (50 mT, 500 kHz, 100 °C)	B65877B0000R049
N92	3850 +30/–20%	1110	< 3.70 (200 mT, 100 kHz, 100 °C)	B65877B0000R092
N87	5000 +30/–20%	1440	< 3.20 (200 mT, 100 kHz, 100 °C)	B65877B0000R087
N97	5150 +30/–20%	1480	< 2.70 (200 mT, 100 kHz, 100 °C)	B65877B0000R097
N95	6300 +30/–20%	1820	< 3.00 (200 mT, 100 kHz, 25 °C – 100 °C) < 3.60 (200 mT, 100 kHz, 120 °C)	B65877B0000R095

Figure 6 – PQ2620 Core Information.

7.2 Bobbin Information

PQ 26/20

Accessories **B65878E**

Coil former

Material: GFR thermosetting plastic (UL 94 V-0, insulation class to IEC 60085: F ≙ max. operating temperature 155 °C), color code black
Sumikon PM 9820® [E41429 (M)], SUMITOMO BAKELITE CO LTD
Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s
Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s

Sections	A_N mm²	l_N mm	A_R value μΩ	Terminals	Ordering code
1	33	56	58	12	B65878E0012D001

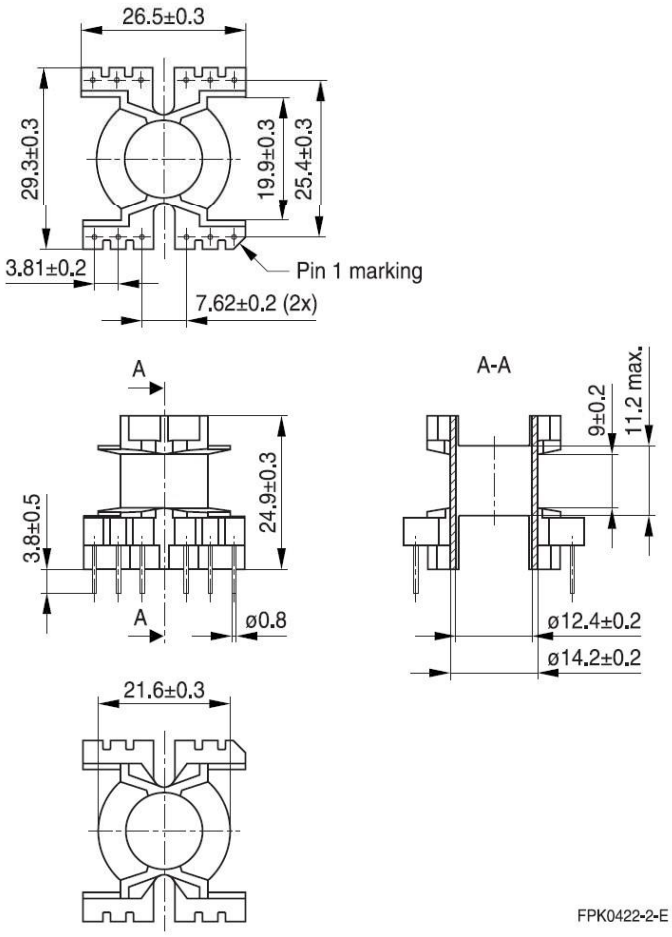


Figure 7 – PQ2620 Bobbin Information.

7.3 Transformer Electrical Diagram

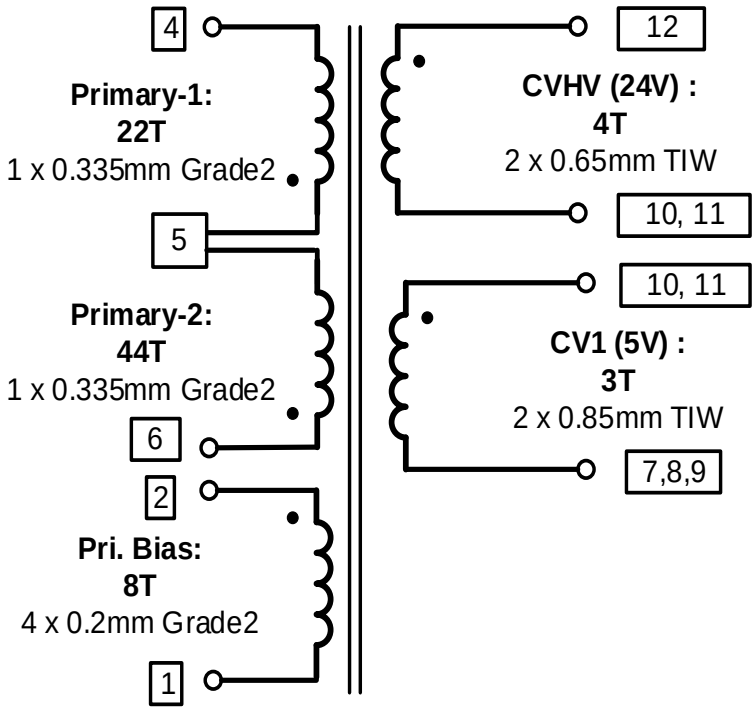


Figure 8 – Transformer Electrical Diagram.

7.4 Transformer Electrical Specification

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins1, 2, 4, 5, 6 to 7, 8, 9, 10, 11, 12	3000Vac
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 6, with all other windings open.	**1100 µH ±5%**
Resonant Frequency	Between pin 4 and 6, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 6, with all secondary windings shorted (pins 7, 8, 9, 10, 11, 12), and primary bias winding opened (pins 1, 2)	< 21 µH

Table 3 – Transformer Electrical Specifications.

7.5 Winding Stack Diagram

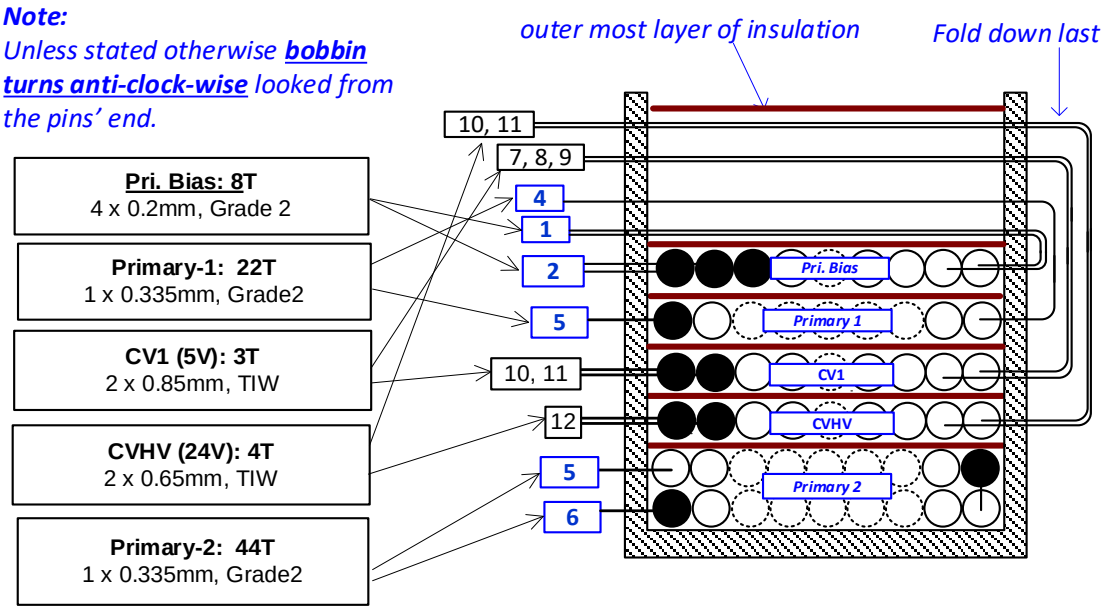


Figure 9 – Transformer Build Diagram.

7.6 List of Materials

Item	Description
[1]	Core: PQ2620.
[2]	Bobbin with Cover: PQ2620, 12pins (5/5).
[3]	Magnet Wire: 0.335 mm, Grade 2 ECW.
[4]	Magnet Wire: 0.2 mm, Grade 2 ECW.
[5]	TEX-E Wire: 0.65 mm, Triple Insulated.
[6]	TEX-E Wire: 0.85 mm, Triple Insulated.
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 11.5 mm Wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9 mm Wide.
[9]	Varnish: Recommended, E962-A (alternative: Dolph BC-359).
[10]	Glue: Recommended, H907 (alternative: Devcon 5-minute Epoxy).

Table 4 – Transformer Materials List.

8 Performance

8.1 Full Load Efficiency vs. Line

The full load efficiency vs. line measurement is shown below. Results were obtained across line voltage (300 VDC, 500 VDC, 800 VDC, 1000 VDC) measured at full load (CV1 = 5 V @ 2.5 A, CVHV = 24 V @ 2A).

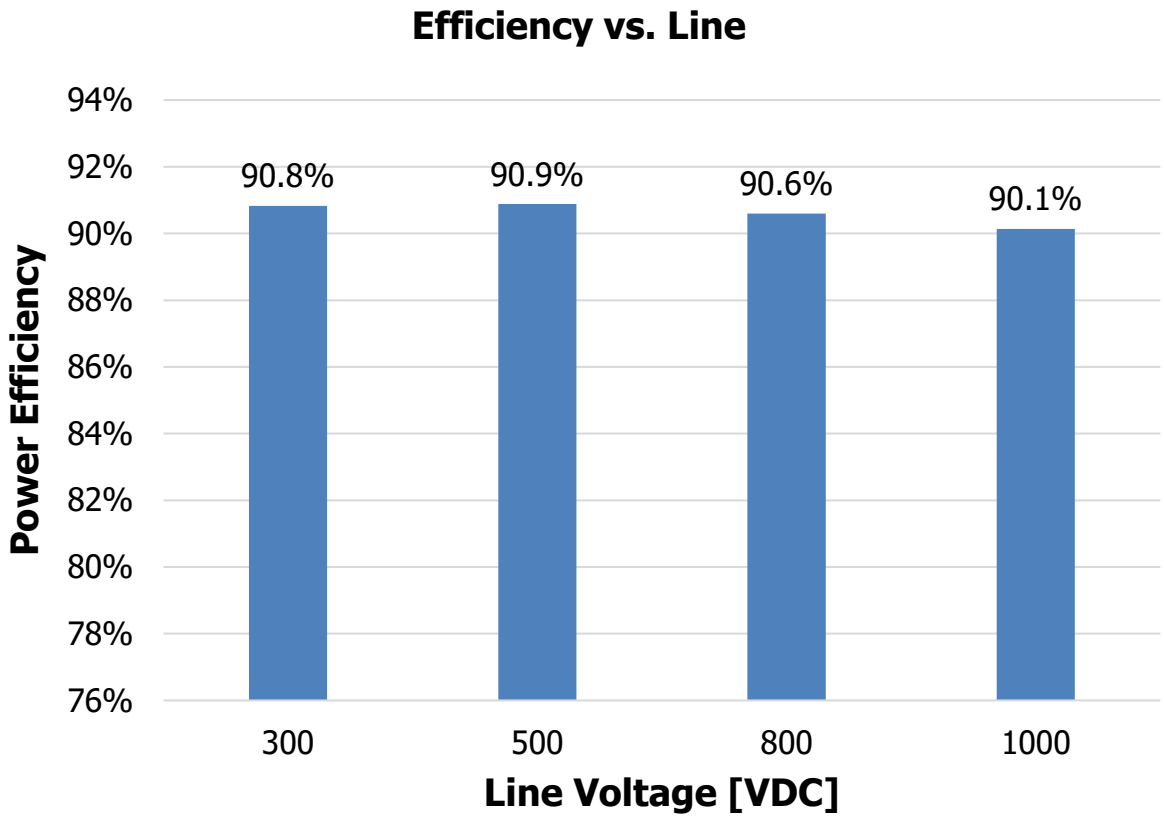


Figure 10 – Full Power Efficiency vs. Line Voltage at Room Temperature.

8.2 Efficiency vs. Load

The efficiency vs. load measurement is shown below and was obtained for combinations of:

- Input line voltages (300 VDC, 500 VDC, 800 VDC, 1000 VDC)
- CV1 = 5 V @ 2.5 A (10% to 100% with 10% load increments)
- CVHV = 24 V @ 2 A (10% to 100% with 10% load increments)

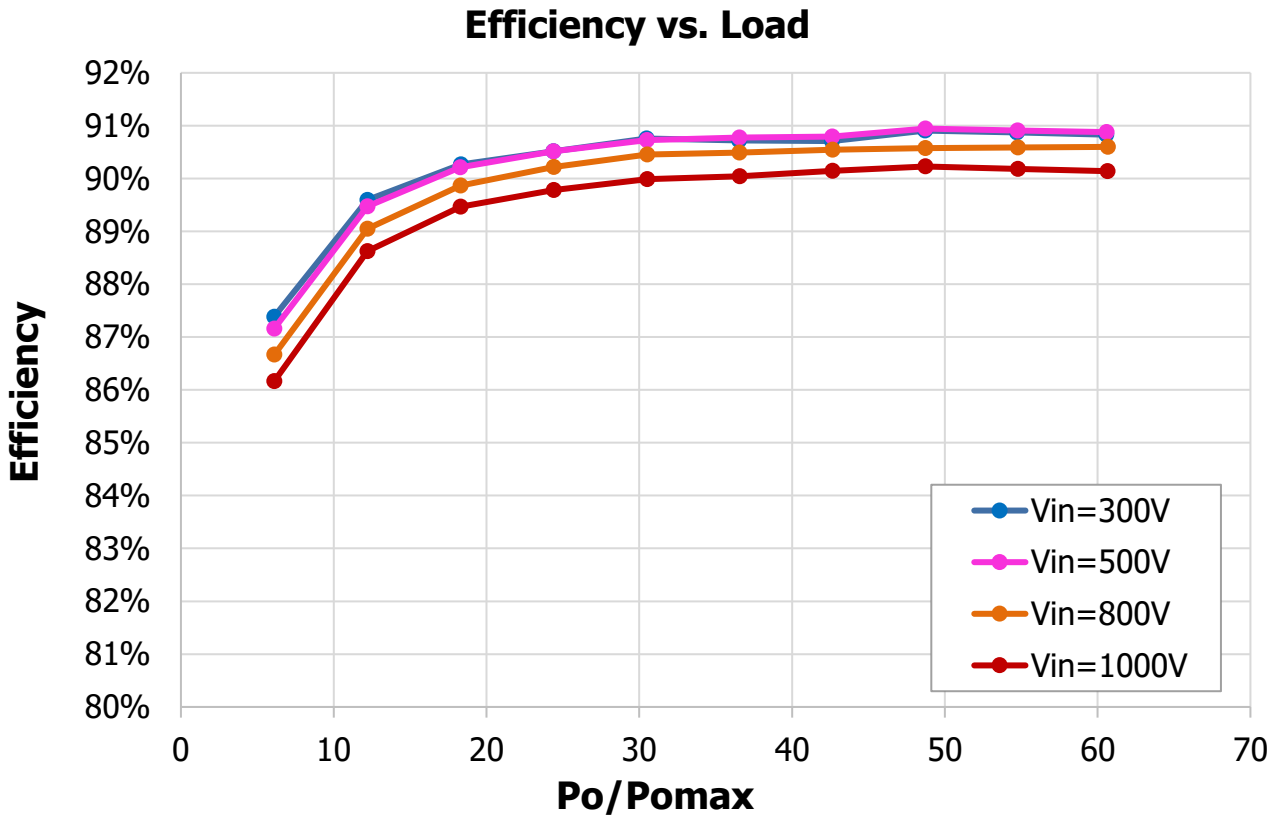


Figure 11 – Efficiency vs. Load for All Line Inputs, Room Temperature.

8.3 Output Load Regulation

The output voltage regulation error vs. load measurement is shown below. Results were obtained for all combinations of:

- Input line voltages = 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- CV1 = 5 V @ 2.5 A (0 to 100% with 20% load increment)
- CVHV = 24 V @ 2 A (0 to 100% with 5% load increment)

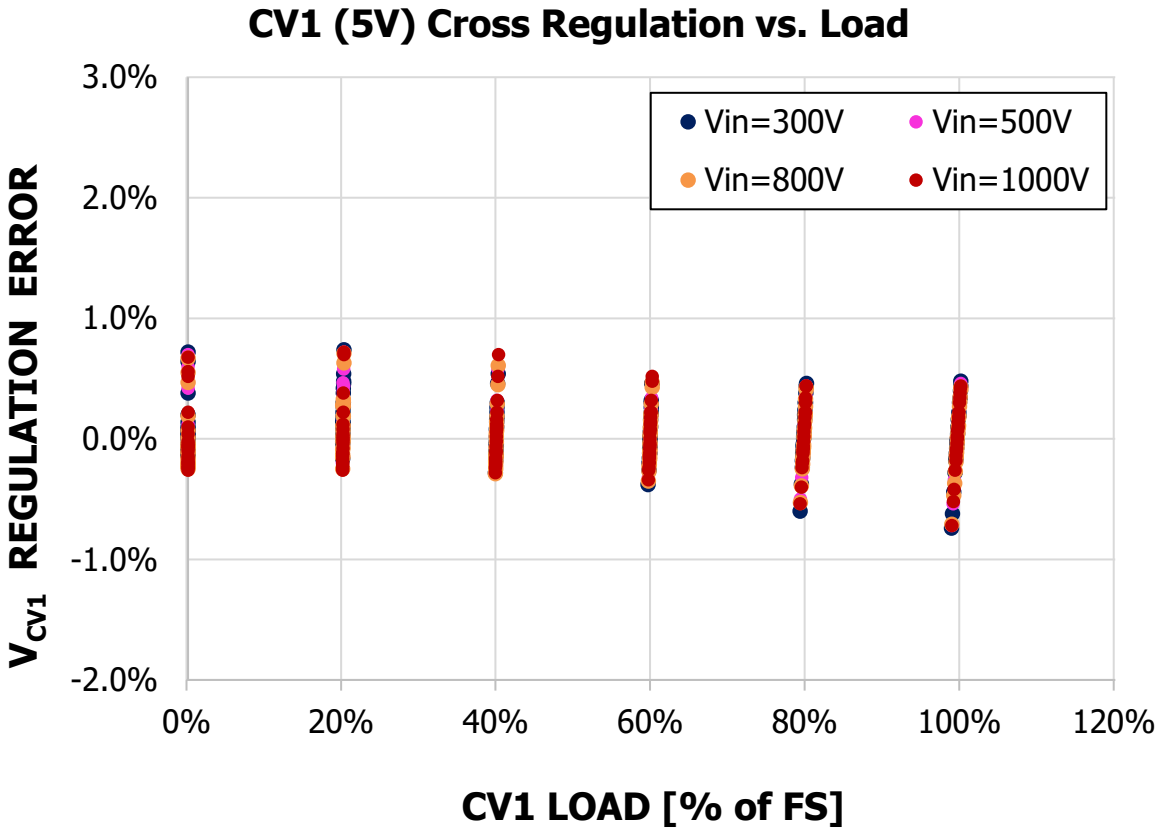


Figure 12 – CV1 Output Voltage Error vs. Output Load, Room Temperature.

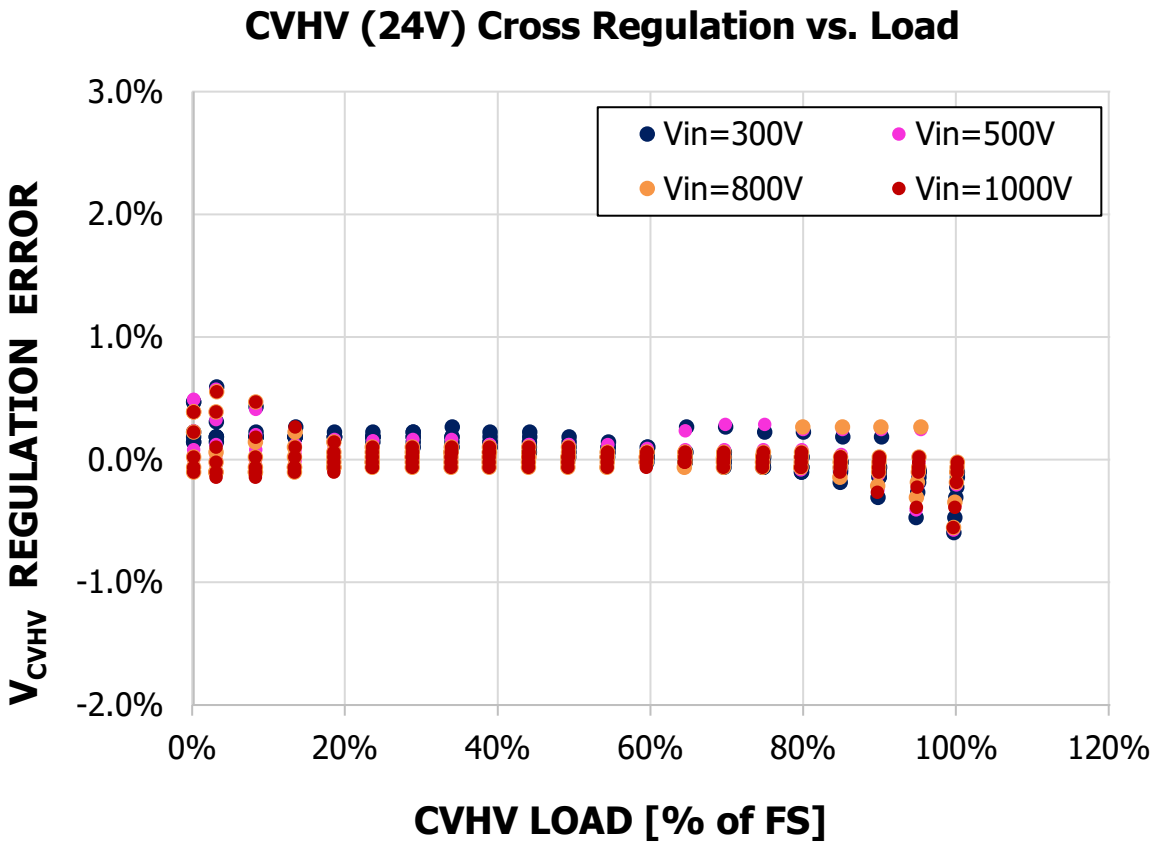


Figure 13 – CVHV Output Voltage Error vs. Output Load, Room Temperature.

8.4 No-Load and Standby Input Power (I_{CVHV} = 0 A)

Output power vs. input power in standby are shown below. Results were obtained under the following test conditions:

- Input line voltages = 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- CV1 output = 0 mW to 250 mW; 0 mW to 1000 mW
- CVHV output = 0 W

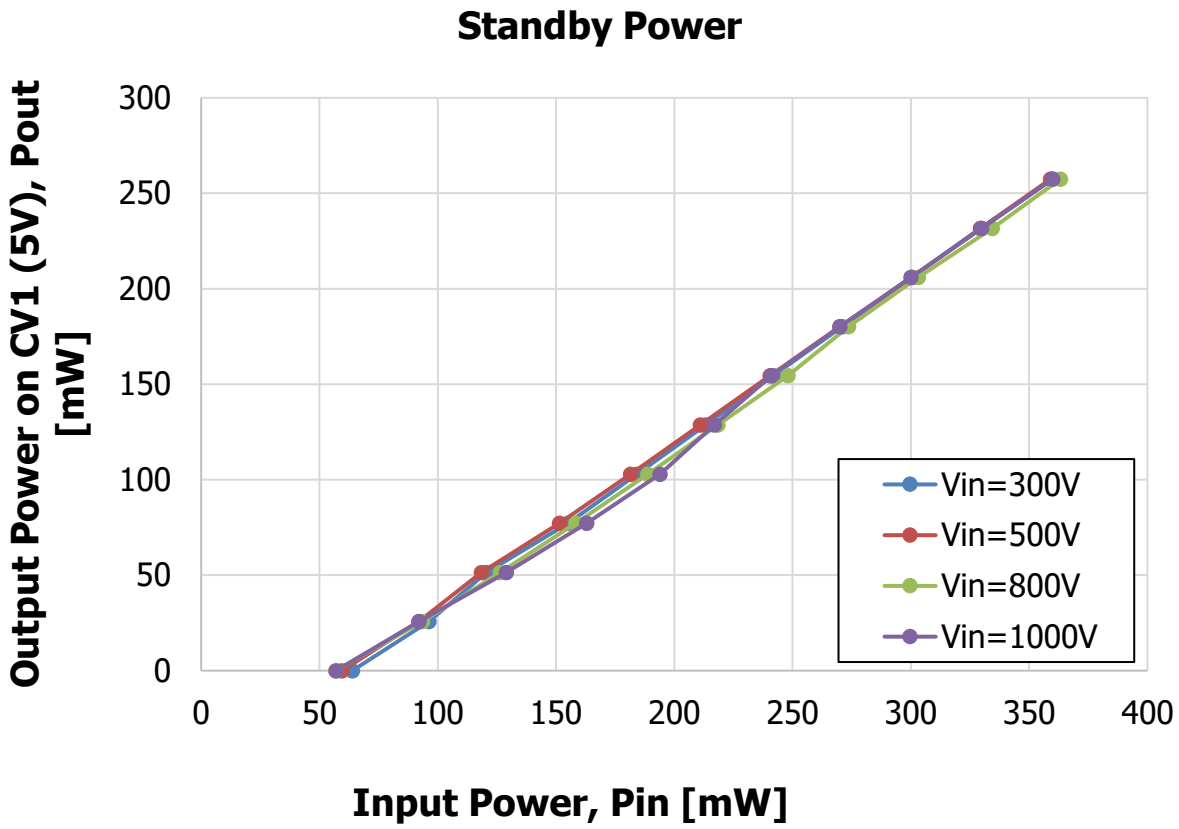


Figure 14 – Available Standby Power Measured against Input Power (0 – 400 mW). Across Input Voltage. Test Performed at Room Temperature.

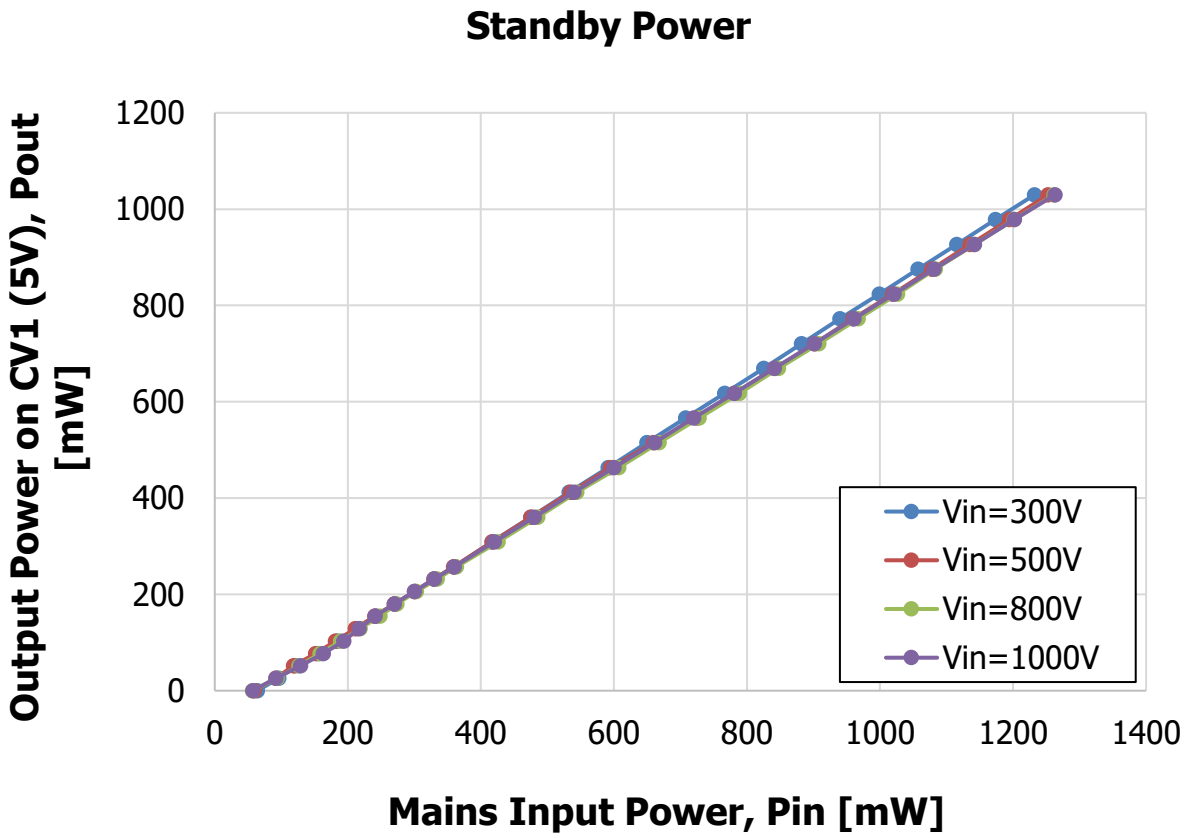


Figure 15 – Available Standby Power Measured against Input Power (0 – 1400 mW input) Across Input Voltage. Test Performed at Room Temperature

8.5 Load Transient Response

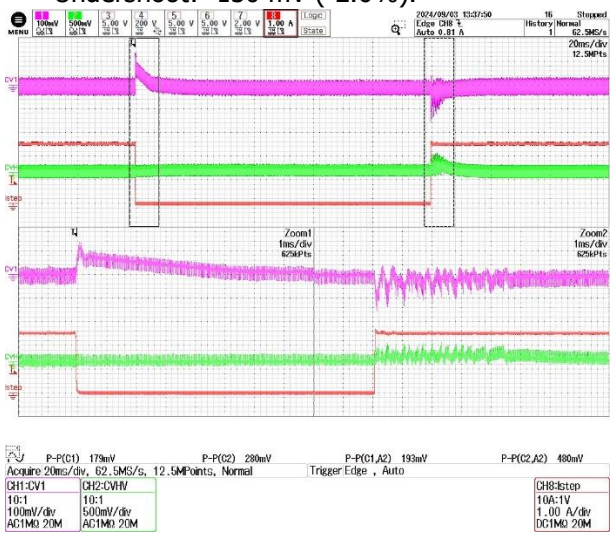
8.5.1 CV1 Step Load Transient Response

The load transient test was performed under the following test conditions:

- Input line voltage = 300 VDC, 1000 VDC
- CV1 load step between 0 A and 2.5 A (0% and 100% load) and back to 0 A
- CVHV = 0 A (0% load), 1A (50% load), 2A (100% load)

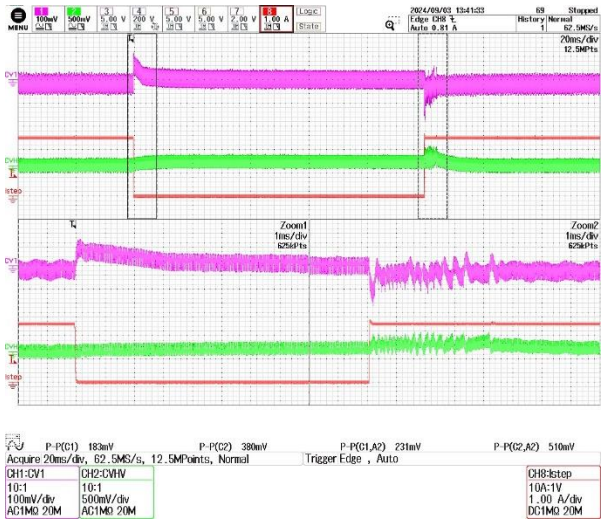
(a) 300 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 0 A.
Overshoot: 136 mV (2.7%).
Undershoot: -130 mV (-2.6%).

(b) 1000 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 0 A.
Overshoot: 140 mV (2.8%).
Undershoot: -141 mV (-2.8%).

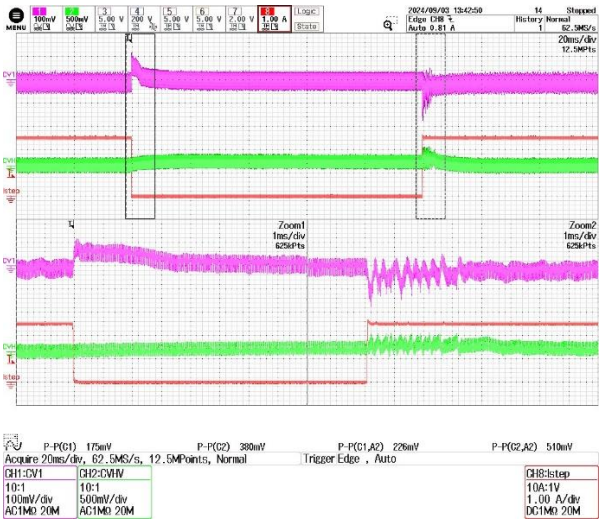


(c) 300 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 1 A.
Overshoot: 179 mV (3.6%).
Undershoot: -193 mV (-3.9%).

(d) 1000 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 1 A.
Overshoot: 172 mV (3.4%).
Undershoot: -196 mV (-3.9%).



(e) 300 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 2 A.
Overshoot: 183 mV (3.7%).
Undershoot: -231 mV (-4.6%).



(f) 1000 VDC, ICV1 = 0 A -> 2.5 A (100%) -> 0 A.
ICVHV = 2 A.
Overshoot: 175 mV (3.5%).
Undershoot: -226 mV (-4.5%).

Figure 16 – CV1 (5 V) Load Transient.

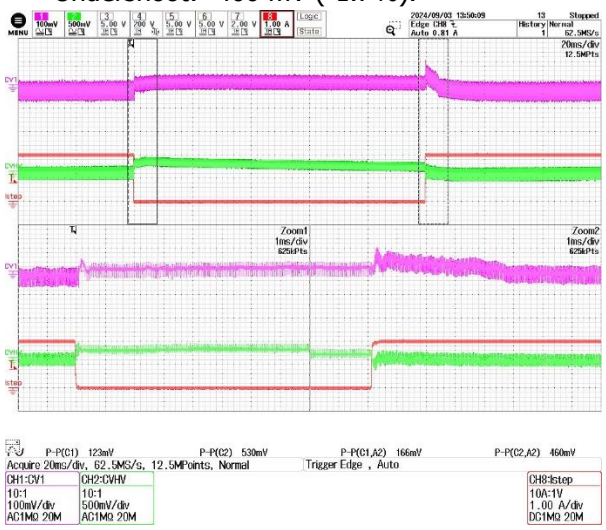
8.5.2 CVHV Step Load Transient

The load transient test was performed under the following test conditions:

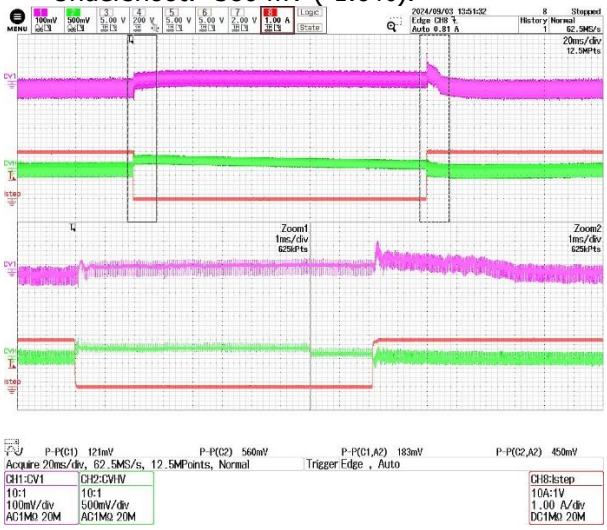
- Input line voltage = 300 VDC, 1000 VDC
- CV1 = 0 A (0% load); 1.25 A (50% load); 2.5 A (100% load)
- CVHV load step from 0 A to 2 A and back to 0 A

(a) 300 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 0 A.
Overshoot: 520 mV (2.2%).
Undershoot: -400 mV (-1.7%).

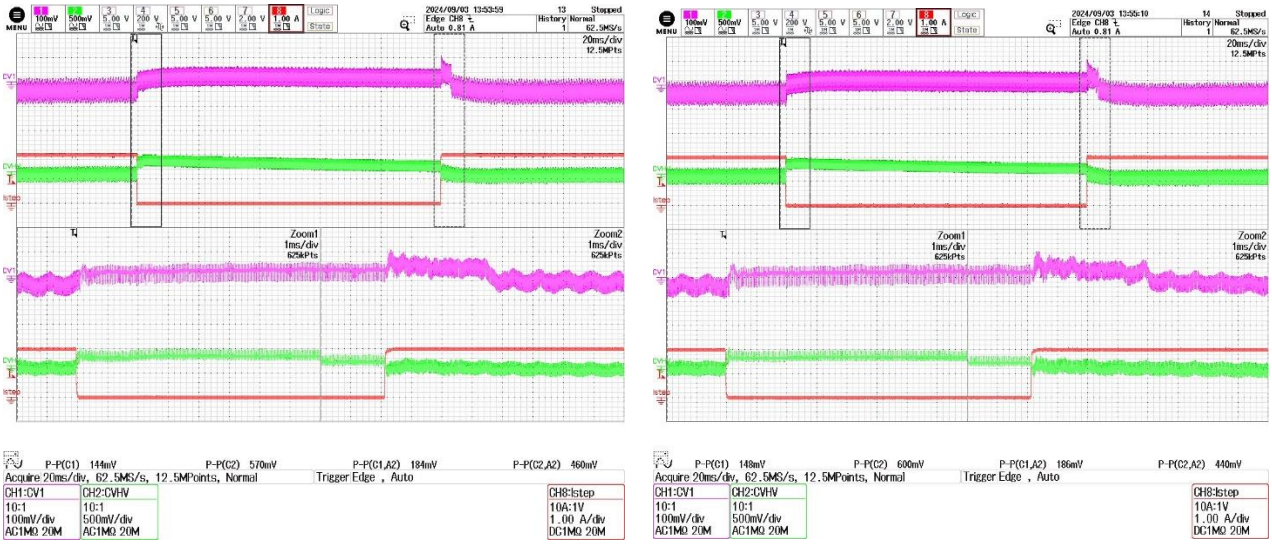
(b) 1000 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 0 A.
Overshoot: 500 mV (2.1%).
Undershoot: -380 mV (-1.6%).



(c) 300 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 1.25 A.
Overshoot: 530 mV (2.2%).
Undershoot: -460 mV (-1.9%).



(d) 1000 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 1.25 A.
Overshoot: 560 mV (2.3%).
Undershoot: -450 mV (-1.9%).



(e) 300 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 2.5 A.
Overshoot: 570 mV (2.4%).
Undershoot: -460 mV (-1.9%).

(f) 1000 VDC, ICVHV = 0 A -> 2 A (100%) -> 0 A.
ICV1 = 2.5 A.
Overshoot: 600 mV (2.5%).
Undershoot: -440 mV (-1.8%).

Figure 17 – CVHV (24 V) Load Transient.

8.6 Switching Waveforms

8.6.1 Primary Switch Maximum Voltage

The primary switch (U1) maximum voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Full load on both outputs:
  - CV1 = 5 V @ 2.5 A
  - CVHV = 24 V @ 2 A
- Full bandwidth selected on the oscilloscope

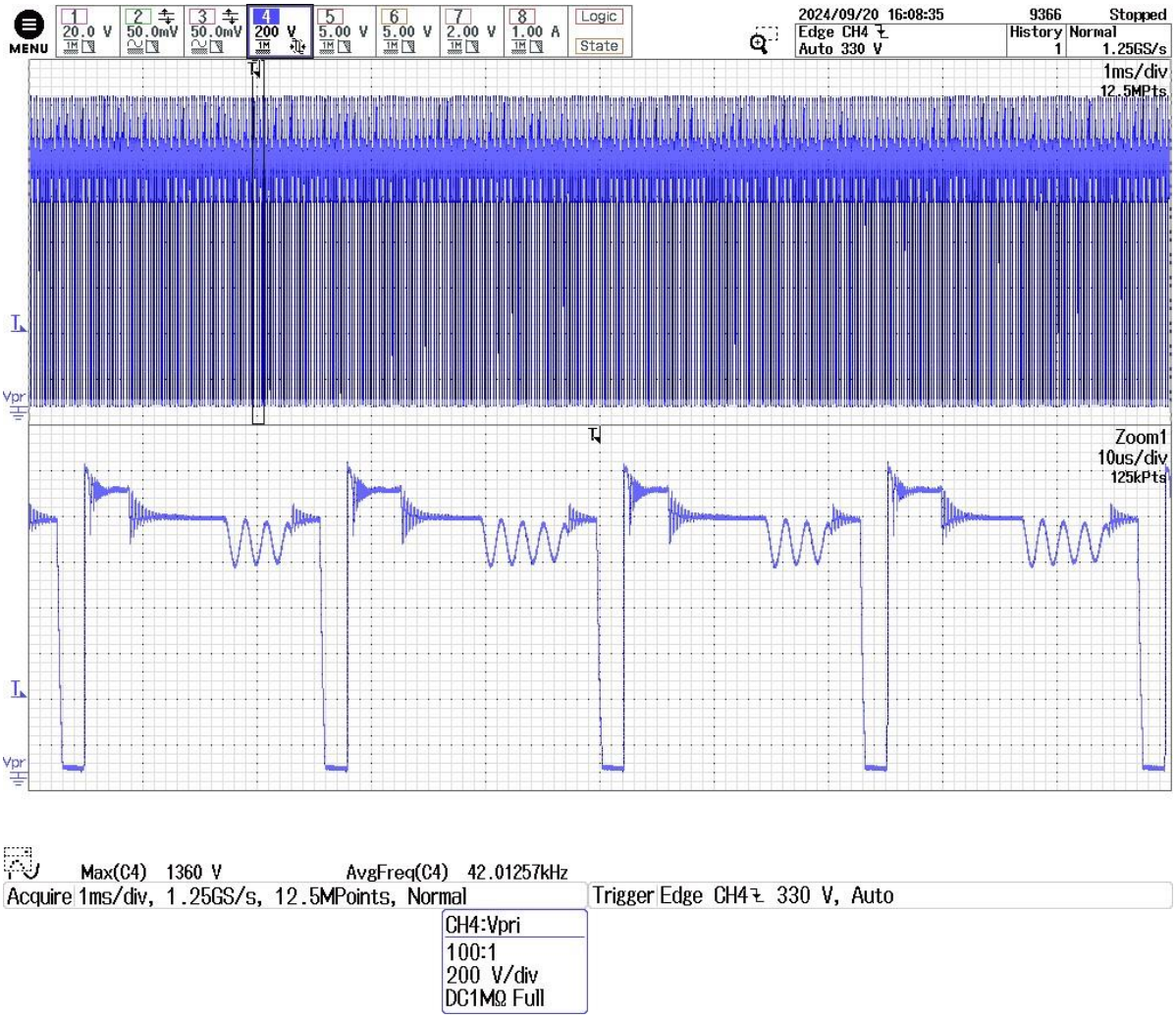


Figure 18 – Primary Switch Worst Case Peak Voltage, V_{PRI_PK} = 1360 V

8.6.2 SR FET Voltage Waveform

The SR FET (Q1) maximum voltage test was performed under the following conditions:

- Line input voltage 1000 VDC
- Start-up with full load on both outputs
  - CV1 (5 V) full load to 2.5 A
  - CVHV (24 V) full load to 2 A
- 100 MHz bandwidth selected on the oscilloscope

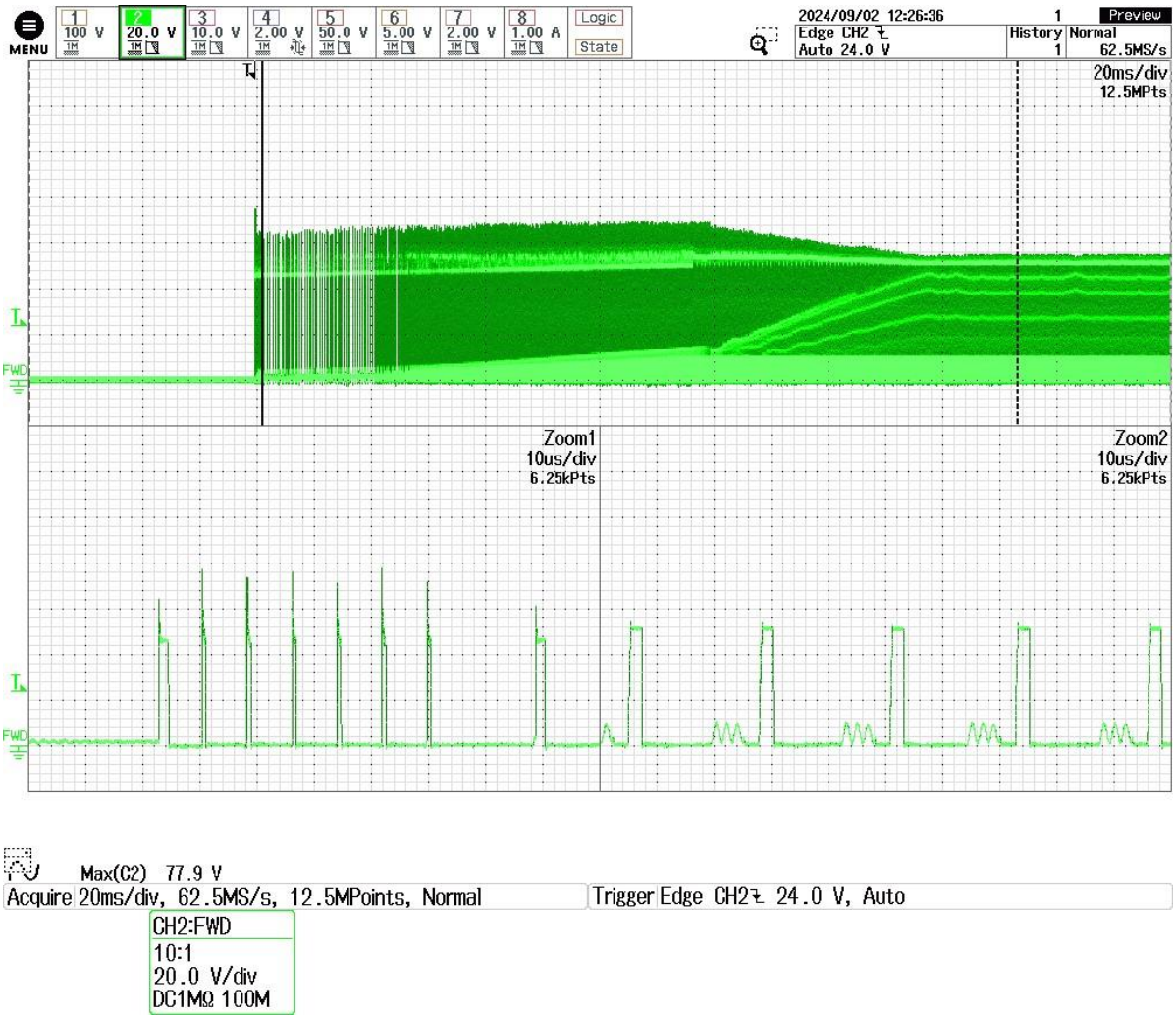


Figure 19 – SR FET Worst Case Peak Voltage, V_{SR_PK} = 77.9 V

8.6.3 Selection FET Voltage Waveform

The Selection FET (Q2) maximum voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Start-up with full load on both outputs
  - CV1 (5 V) full load to 2.5 A
  - CVHV (24 V) full load to 2 A
- 100 MHz bandwidth selected on the oscilloscope

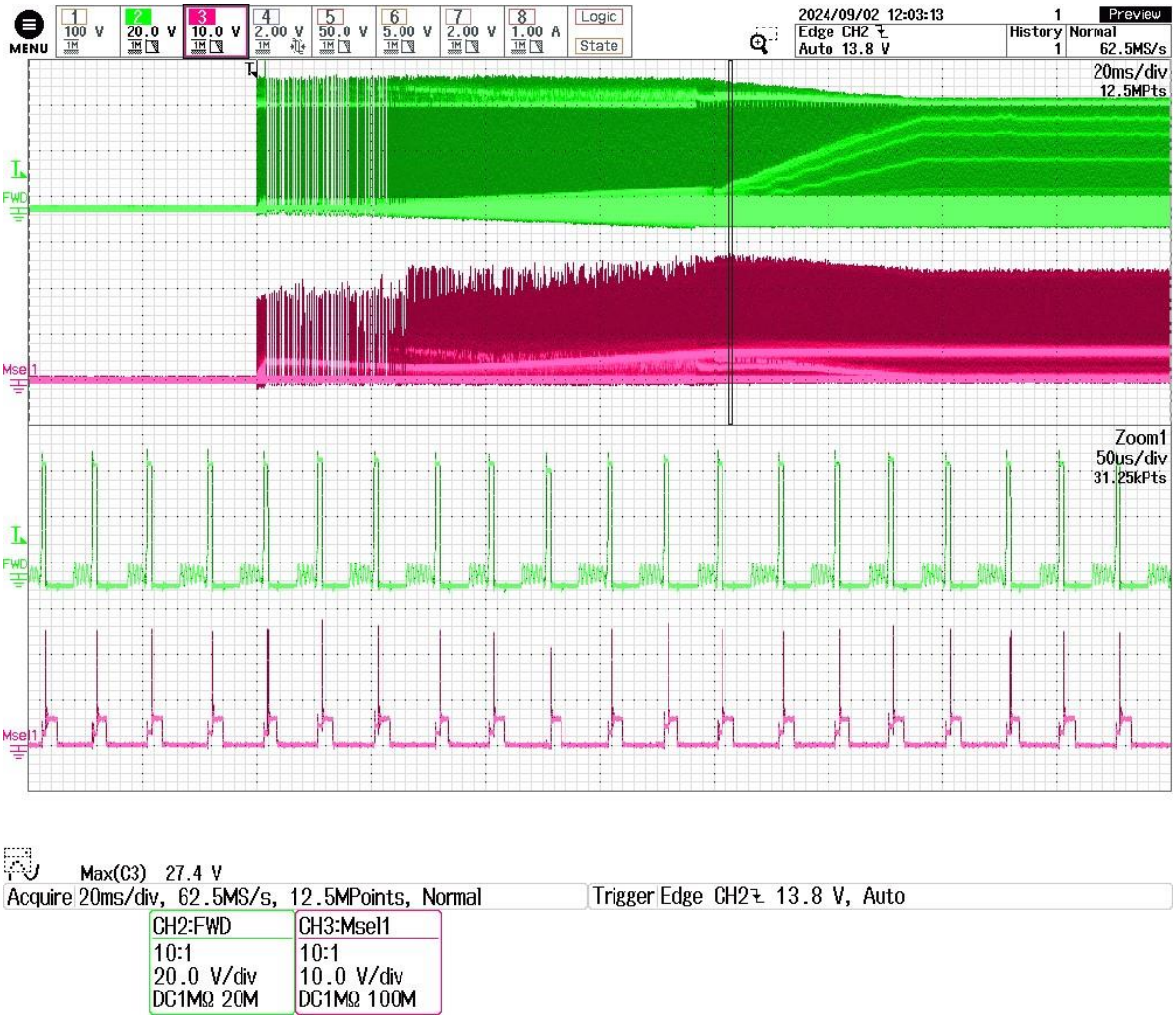


Figure 20 – Selection FET Worst Case Peak Voltage, V_{SEL_PK} = 27.4 V.

8.6.4 CVHV Diode Reverse Voltage Waveform

The CVHV Diode (D3) maximum reverse voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Start-up with full load on both outputs
  - CV1 (5 V) full load to 2.5 A
  - CVHV (24 V) full load to 2 A
- 100 MHz bandwidth selected on the oscilloscope

Figure 21 – CVHV Diode Worst Case Reverse Voltage, V_{D3_PK} = 124 V

8.6.5 BPP Rectifier Diode Reverse Voltage Waveform

The BPP rectifier diode (D1) maximum reverse voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Start-up with full load on both outputs
  - CV1 (5 V) full load to 2.5 A
  - CVHV (24 V) full load to 2 A
- 100 MHz bandwidth selected on the oscilloscope

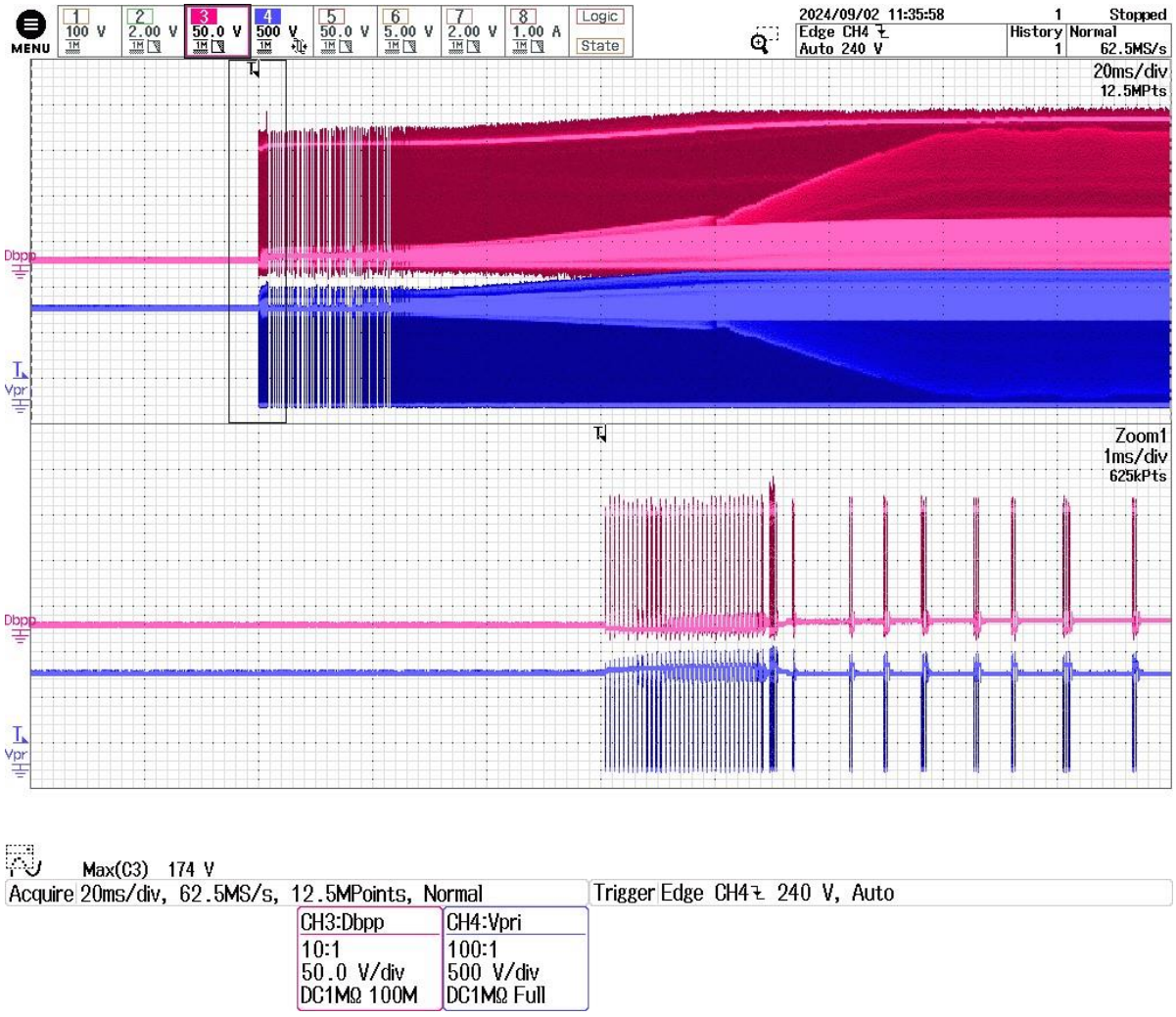


Figure 22 – BPP Rectifier Diode Worst Case Reverse Voltage, V_{D1_PK} = 174 V.

8.6.6 Maximum Voltage Stress

The voltage waveforms on each key component, i.e., MOSFETs & diodes, were checked to confirm that maximum voltages were below the component voltage ratings. Maximum voltage stress can occur under different combinations of input line voltages, output loads, start-up and load step. Most design specifications call for 10% ~ 20% margin between the maximum voltage stress and component rating. The table below lists the maximum voltage stress on key components:

Component	Part Number	Component Rating [V]	Voltage Stress	
			[V]	Derating [%]
InnoMux2 (U1)	IMX2353F-H415	1700	1360	**80%**
SR FET (Q1)	SIR870DP-T1-GE3	100	77.9	**78%**
Selection FET (Q2)	SI4154DY-T1-GE3	40	27.4	**69%**
CVHV Diode (D3)	DSS6-015AS-TRL	150	124	**83%**
BPP Diode (D1)	US1G	400	174	**44%**

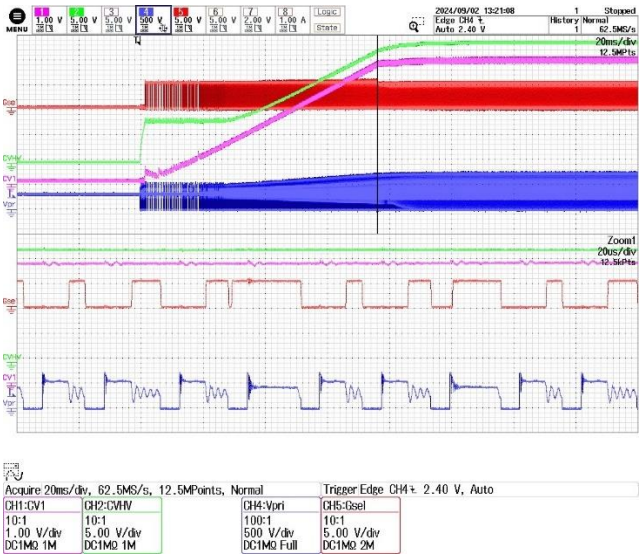
Table 5 – Maximum Voltages on key components.

8.7 Start-Up

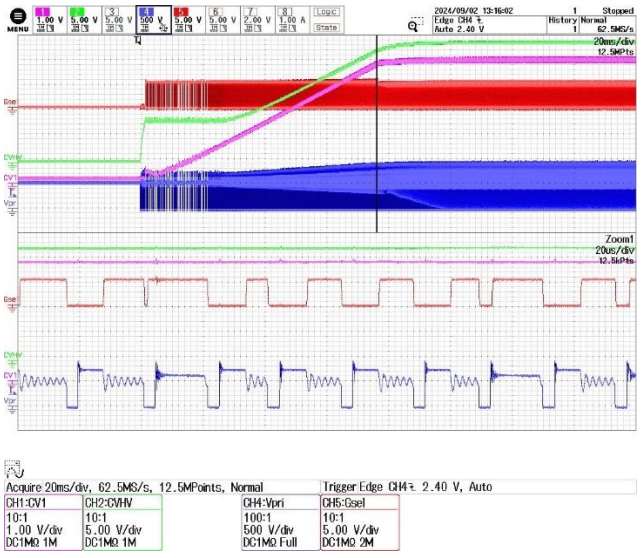
8.7.1 Start-up under Output Load

The start-up test was performed using the following test conditions:

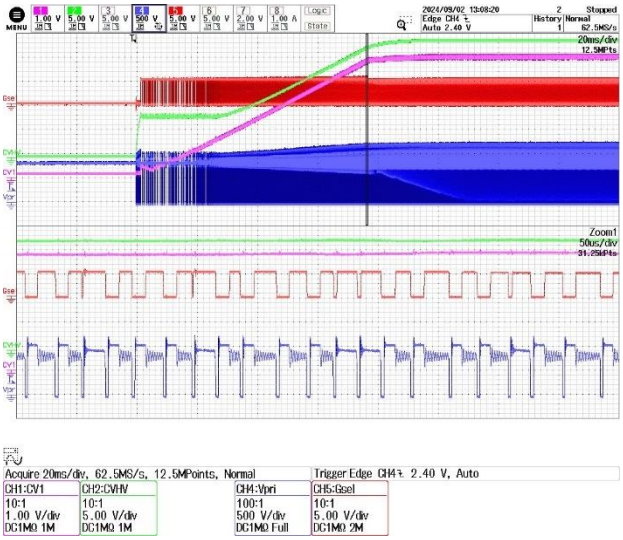
- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC
  - CV1 = 5 V @ 12.5 W (Full Load)
  - CVHV = 24 V @ 48 W (Full Load)
- Input line voltage 70 VDC
  - CV1 = 5 V @ 1 W
  - CVHV = 24 V @ 2 W
- Input line voltage 100 VDC
  - CV1 = 5 V @ 5 W
  - CVHV = 24 V @ 10 W
- Input line voltage 200 VDC
  - CV1 = 5 V @ 8 W
  - CVHV = 24 V @ 32 W



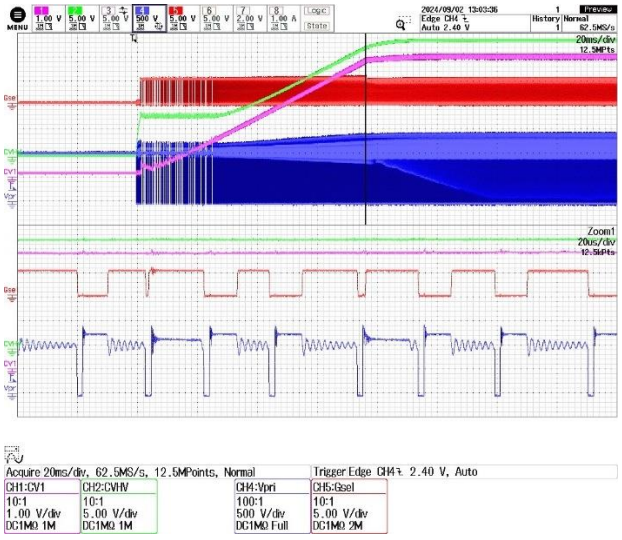
(a) 300 VDC Input Line Voltage.
CV1 = 5 V @ 2.5 A
CVHV = 24 V @ 2 A



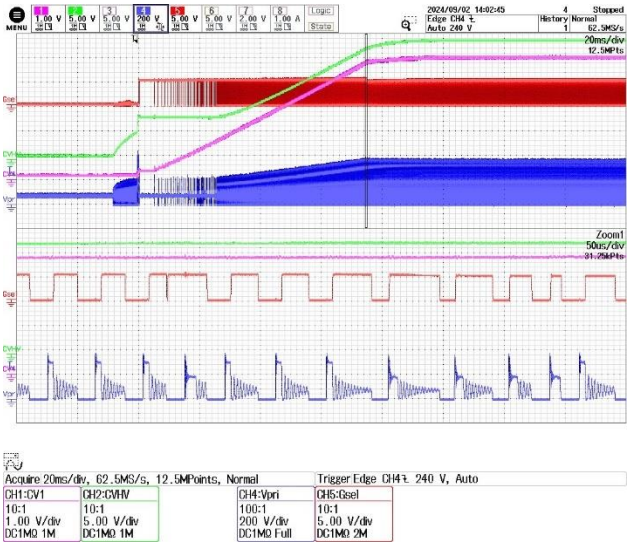
(b) 500 VDC Input Line Voltage.
CV1 = 5 V @ 2.5 A
CVHV = 24 V @ 2 A



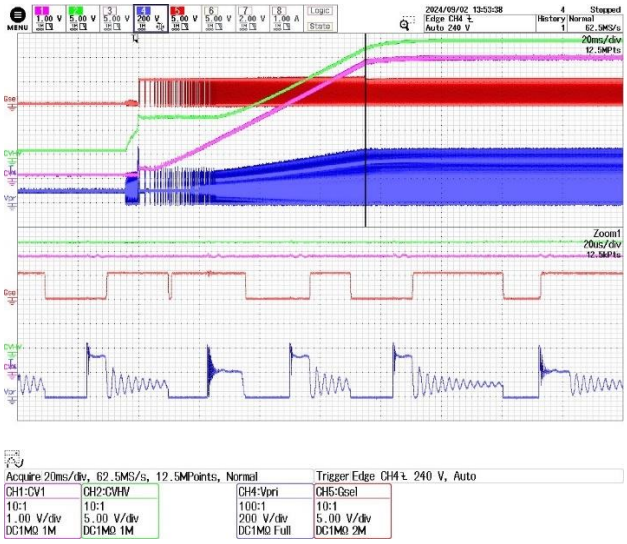
(c) 800 VDC Input Line Voltage.
CV1 = 5 V @ 2.5 A
CVHV = 24 V @ 2 A



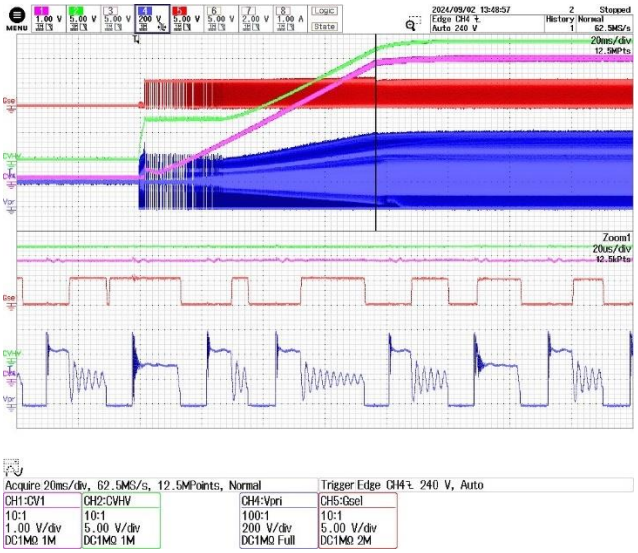
(d) 1000 VDC Input Line Voltage.
CV1 = 5 V @ 2.5 A
CVHV = 24 V @ 2 A



(e) 70 VDC Input Line Voltage.
CV1 = 5 V @ 1 W
CVHV = 24 V @ 2 W



(f) 100 VDC Input Line Voltage.
CV1 = 5 V @ 5 W
CVHV = 24 V @ 10 W



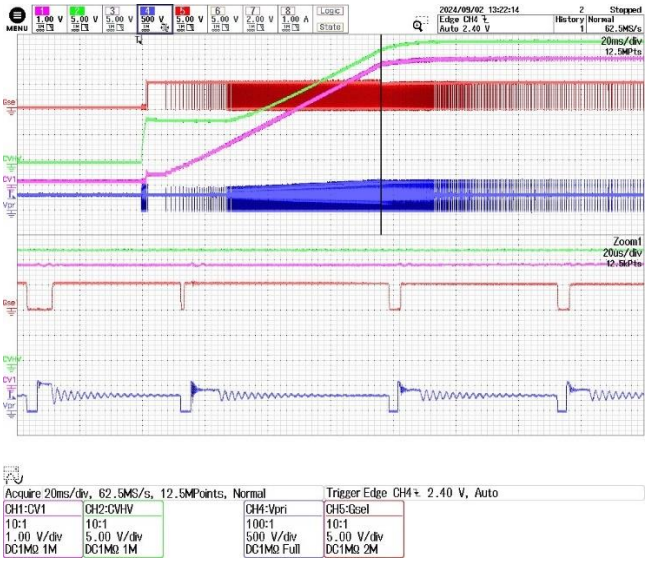
(g) 200 VDC Input Line Voltage.
CV1 = 5 V @ 8 W
CVHV = 24 V @ 32 W

Figure 23 – Start-up with Output Loads

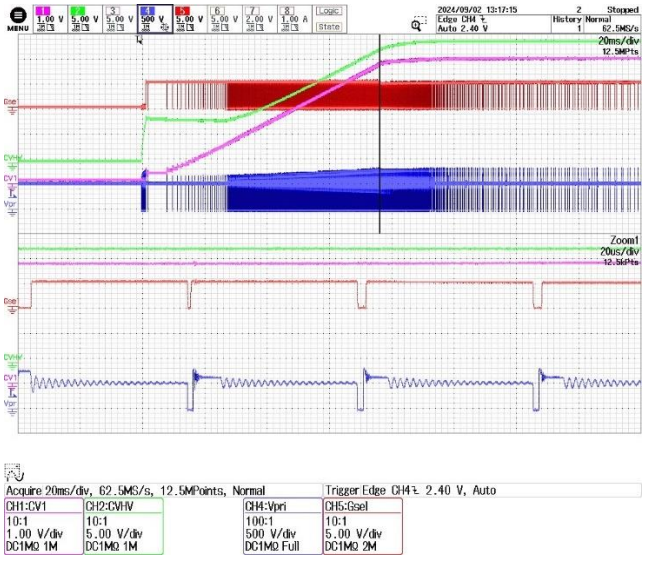
8.7.2 No-Load Start-up

The no load start-up test was performed using the following test conditions:

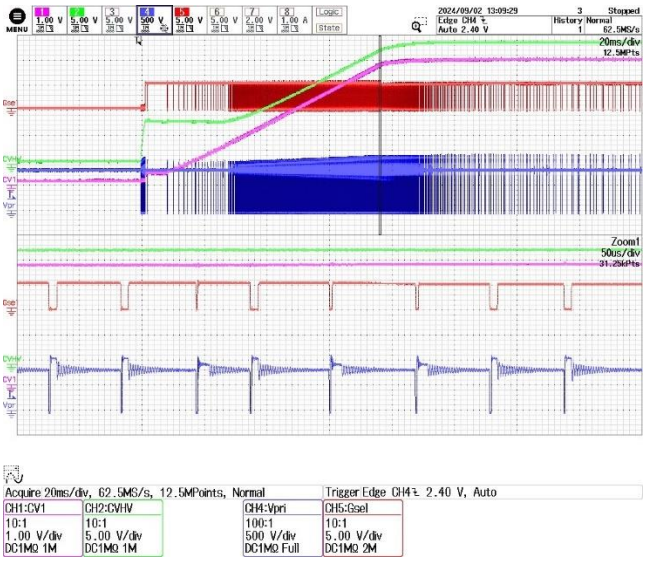
- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- No load on either output



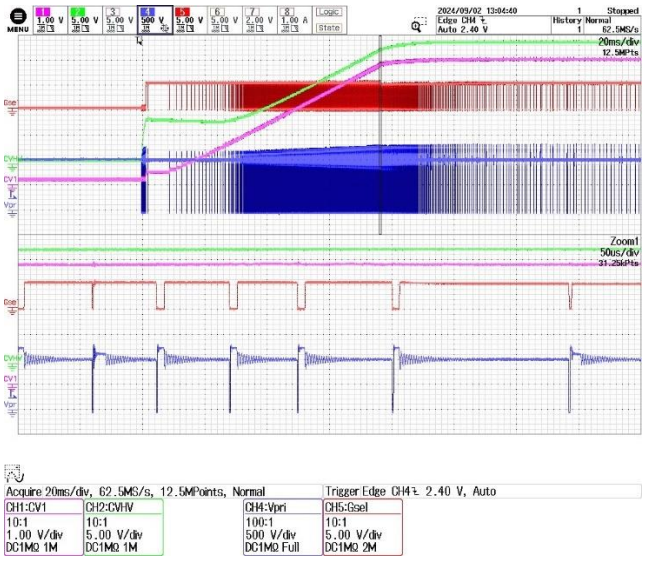
(a) 300 VDC Input Line Voltage.



(b) 500 VDC Input Line Voltage.



(c) 800 VDC Input Line Voltage.



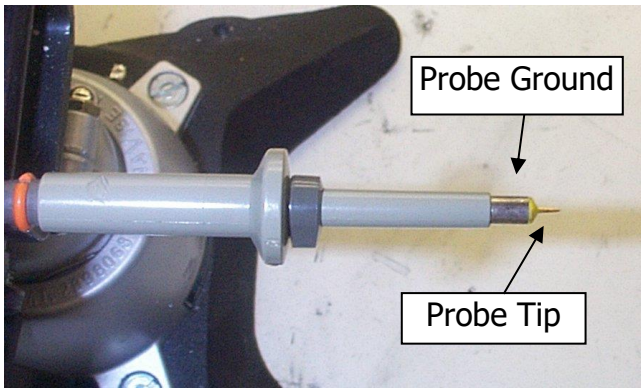
(d) 1000 VDC Input Line Voltage.

Figure 24 – No-load Start-up.

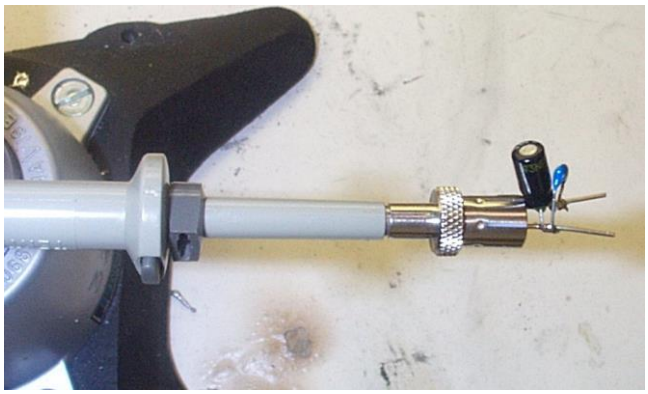
8.8 Output Ripple Measurements

8.8.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to minimize noise pick-up. The probe adapter configuration is shown below. It includes a coaxial cable with two parallel capacitors connected to the measurement points. The capacitors are a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.



End Cap and Ground Lead Removed.



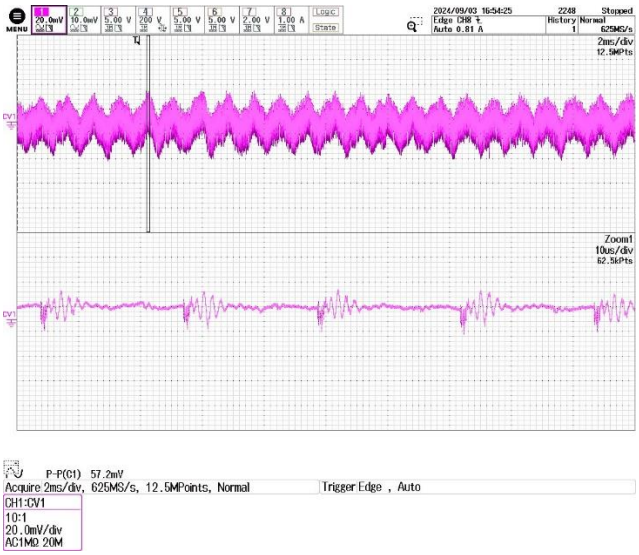
Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

Figure 25 – Oscilloscope Probe Prepared for Ripple Measurement.

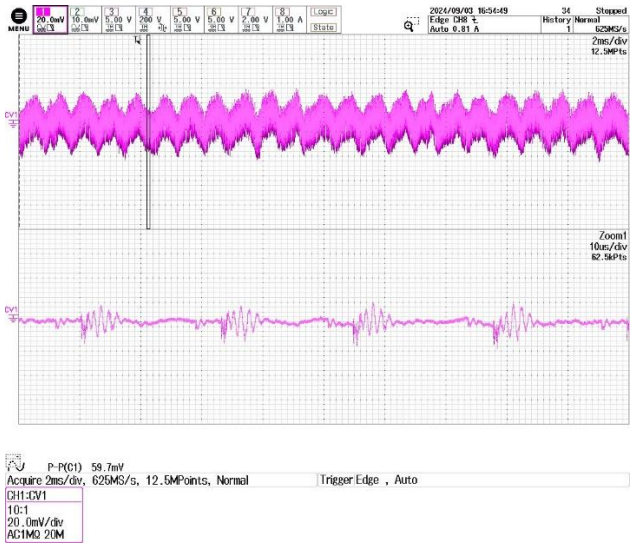
8.8.2 CV1 and CVHV Output Ripple

The CV1 and CVHV output ripple were tested under the following conditions:

- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- CV1 = 5 V @ 2.5 A
- CVHV = 24 V @ 2 A
- 20 MHz bandwidth selected on the oscilloscope



(a) 300 VDC Input Line Voltage
V_{RIPPLE_CV1} = 57.2 mV



(b) 500 VDC Input Line Voltage
V_{RIPPLE_CV1} = 59.7 mV

(c) 800 VDC Input Line Voltage
V_{RIPPLE_CV1} = 58.6 mV

(d) 1000 VDC Input Line Voltage
V_{RIPPLE_CV1} = 62 mV

(e) 300 VDC Input Line Voltage
V_{RIPPLE_CVHV} = 339 mV

(f) 500 VDC Input Line Voltage
V_{RIPPLE_CVHV} = 328 mV

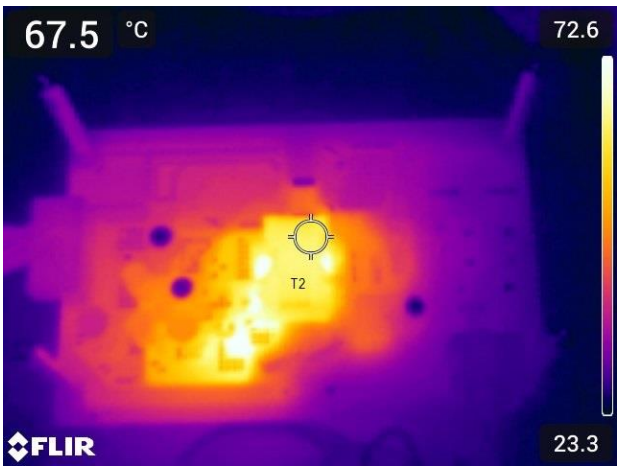
(g) 800 VDC Input Line Voltage
V_{RIPPLE_CVHV} = 336 mV

(h) 1000 VDC Input Line Voltage
V_{RIPPLE_CVHV} = 352 mV

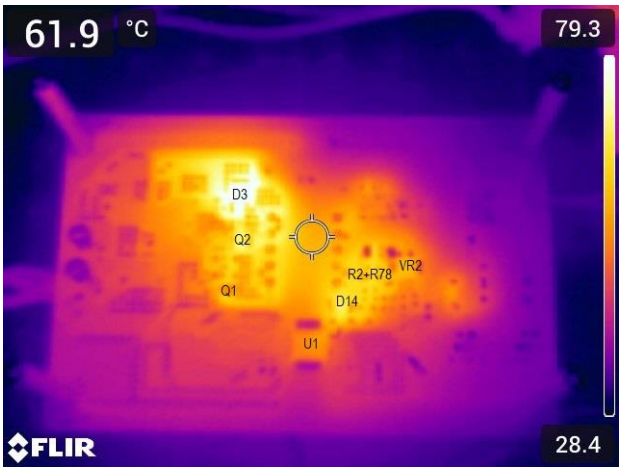
Figure 26 – VCV1 and VCVHV Ripple and Noise.

8.9 Thermal Performance

Heatsinks are not required for the design. Instead copper pour area on the PCB is used for cooling the InnoMux2-EP IC. No forced air-cooling was required during any test. The temperatures of the hottest components in the assembly are shown below.

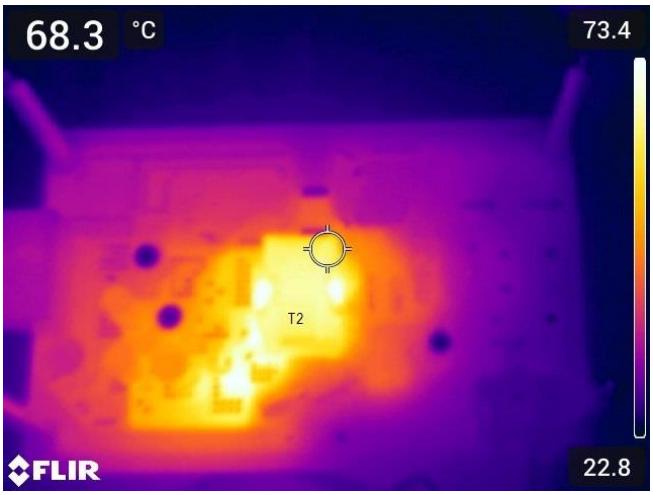


(a) Top View

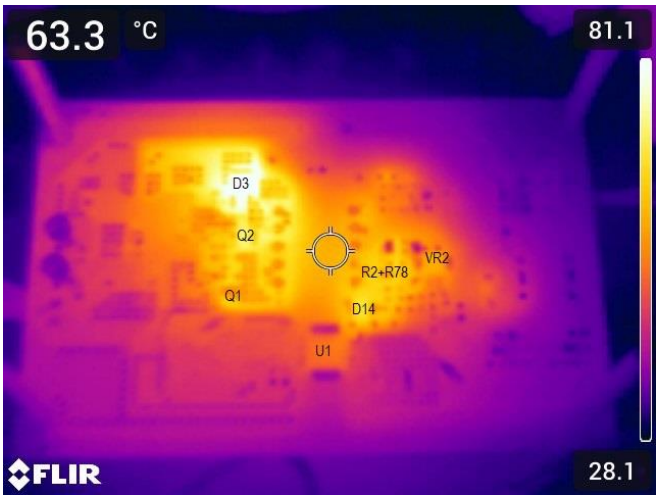


(b) Bottom View

Figure 27 – Thermal Image, 300 VDC, Full Power.

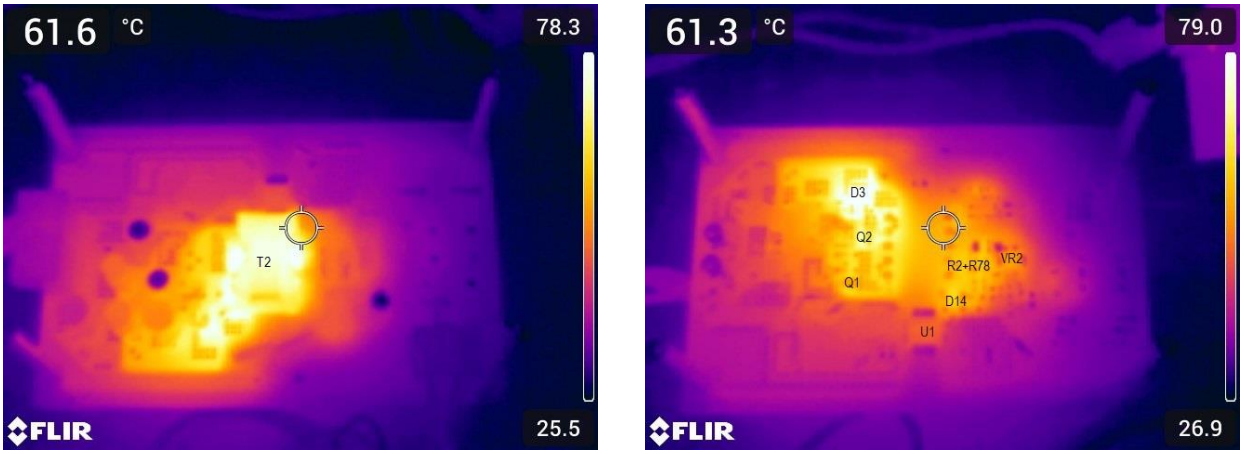


(a) Top View



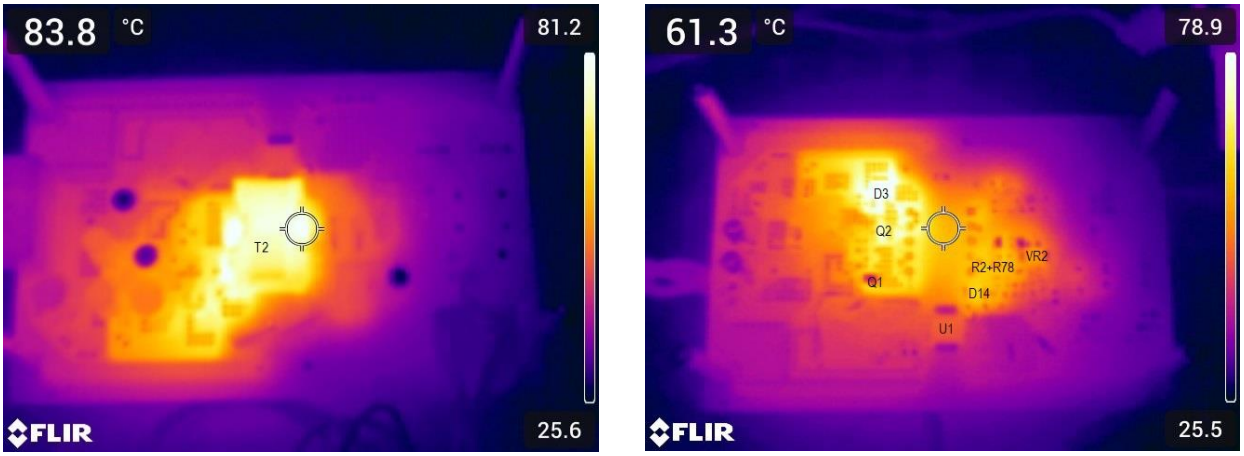
(b) Bottom View

Figure 28 – Thermal Image, 500 VDC, Full Power.



(a) Top View (b) Bottom View

Figure 29 – Thermal Image, 800 VDC, Full Power.



(a) Top View (b) Bottom View

Figure 30 – Thermal Image, 1000 VDC, Full Power

Component	Description	Bottom Side Component Temperature [˚C]			
		Vin = 300 VDC	Vin = 500 VDC	Vin = 800 VDC	Vin = 1000 VDC
U1	InnoMux2	56.6	54.3	50.6	50.0
D14	Snub Diode	70.8	70.1	67.1	66.9
VR2	Snub Zener	62.9	62.2	59.9	58.8
R2+R78	Snub Resistor	68.1	68.2	65.3	65.4
D3	CVHV Diode	90.3	90.7	89.8	91.4
Q2	Selection FET	74.0	75.6	76.7	78.1
Q1	SR FET	66.5	67.3	68.6	71.4
	Ambient	29.4	29.5	28.2	27.7

Table 6 – Bottom Side Component Temperatures, 300 VDC, 500 VDC, 800 VDC and 1000 VDC, Full Load (60 W).

Component	Description	Top Side Component Temperature [˚C]			
		Vin = 300 VDC	Vin = 500 VDC	Vin = 800 VDC	Vin = 1000 VDC
Transformer T2	Core	69.2	69.5	77.0	79.8
	Winding	76.3	77.7	86.9	90.7
	Ambient	25.6	23.7	26.2	26.0

Table 7 – Top Side Component Temperatures, 300 VDC, 500 VDC, 800 VDC and 1000 VDC, Full Load (60 W).

9 Revision History

Date	Author	Revision	Description & Changes	Reviewed
30-Oct-24	HC	A	Initial Release.	Apps & Mktg
07-Nov-24	HC	A	Minor Changes: Additional subpart for T2 in BOM table, Removed NTC in section 8.2, Replaced LED Output with CVHV Output in Page 10.	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY
(AC-DC/LED/Motor Control Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com