Reference Design Report

Title	**168 W Isolated Flyback Power Supply Using TOPSwitchGaN (TOP7075E)**
Specification	85 – 265 VAC Input; 42 V / 4 A Output
Application	E-bike Charger
Author	Applications Engineering Department
Document Number	RDR-1018
Date	March 16, 2026
Revision	A

Summary and Features

- >90% full load efficiency at 115 VAC and 92% full load efficiency at 230 VAC
- ≥90% efficient at 10% load at 115 VAC and 230 VAC Input
- >90% average efficiency at 115 VAC and 230 VAC
- Extensive protection features including:
    - Line overvoltage and undervoltage protection
    - Over Temperature Protection (OTP)
    - Short circuit protection
- Class B conducted EMI with > 6 dB margin

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www.power.com

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a flyback converter that provides an isolated output voltage of 42 V at 4 A from a wide input voltage range of 85 VAC to 265 VAC. This power supply utilizes the TOP7075E from the TOPSwitchGaN™ family of ICs.

This document contains the complete power supply specification, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

Figure 1 – Oblique View.

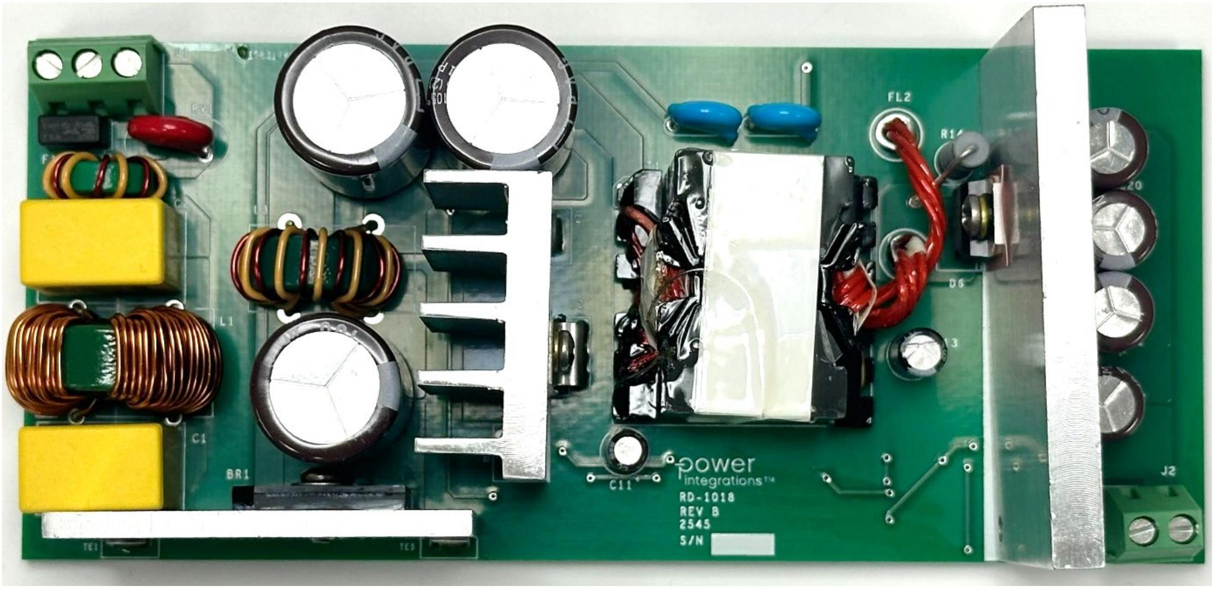

Figure 2 – Top View.

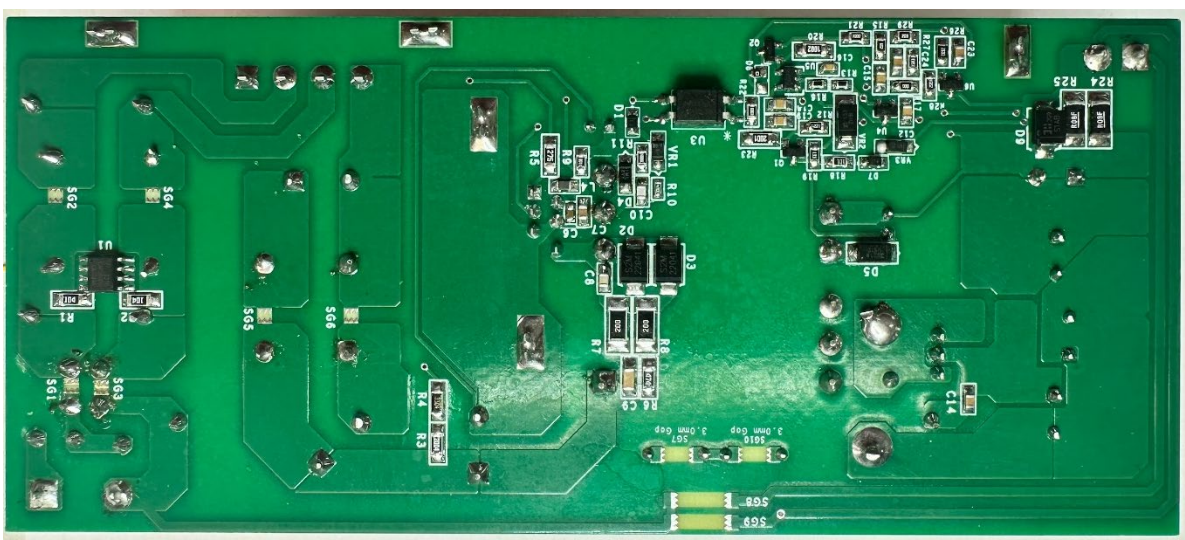

Figure 3 – Bottom View.

2 Power Supply Specification

The table represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50 / 60	64	Hz	
No-load Input Power (230 VAC)				500	mW	
Output1						
Output Voltage	V_{OUT1}	39.9	42	44.1	V	± 5%
Output Ripple Voltage	$V_{RIPPLE1}$			420	mV	20 MHz Bandwidth.
Output Current	I_{OUT1}	0		4	A	
Total Output Power						
Continuous Output Power	P_{OUT}		168		W	
Efficiency						
Full Load 115 VAC	$\eta_{115 VAC}$		90.8		%	Measured at P_{OUT} 25 °C.
Full Load 230 VAC	$\eta_{230 VAC}$		92.8		%	
Average efficiency at 25, 50, 75 and 100% of P_{OUT}	η_{DOE}		91.9		%	Measured at Nominal Input 115 VAC and 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				±2	kV	1.2/50 µs Surge, IEC 61000-4-5 Differential Mode: Series Impedance = 2 Ω
Ring Wave (Common Mode)				±6	kV	100 kHz Ring Wave Common Mode: Series Impedance = 12 Ω
Electrical Fast Transient (EFT)				±4	kV	15 ms @ 5 kHz 0.75 ms @ 100 kHz
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 Schematic

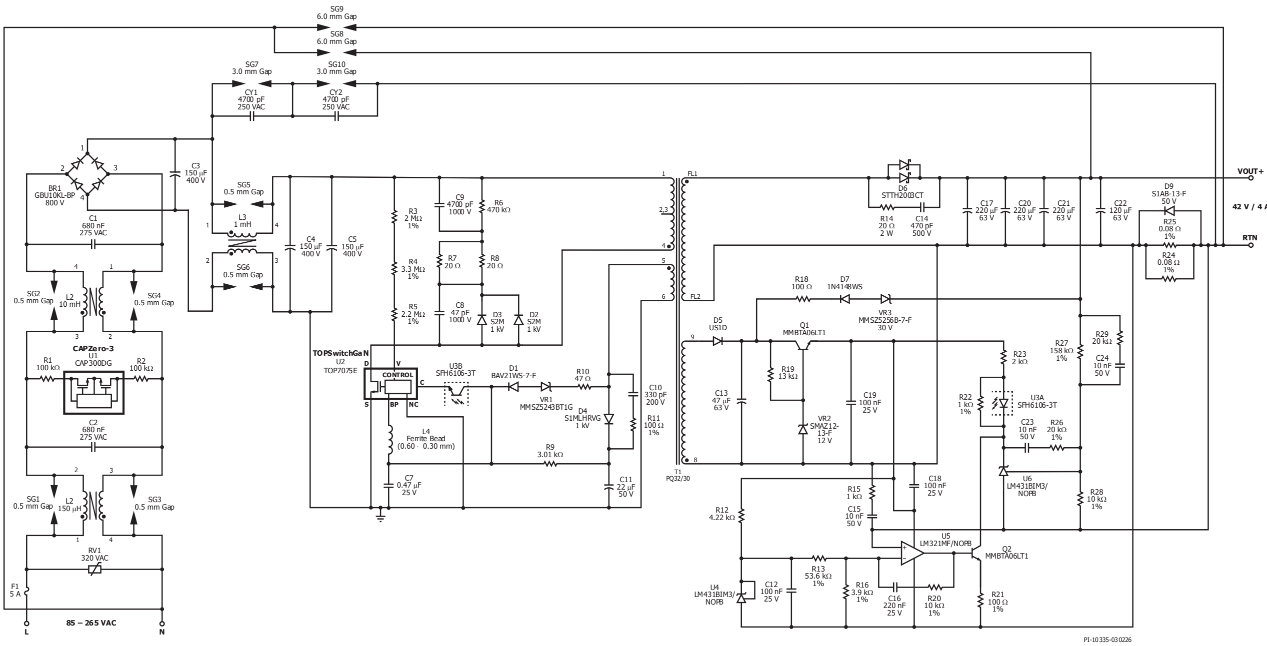


Figure 4 – Schematic.

Note: Full Schematic (Figure – 104) is in the Appendix Section

4 Circuit Description

This power supply employs a TOP7075E off-line switcher IC, (U2), in a flyback configuration. U2 has an integrated high voltage PowiGaN™ switch. It regulates the output by adjusting the PowiGaN switch off time duration, which is proportional to the current fed into its CONTROL pin. ILIM is adjusted according to switching frequency.

4.1 Input EMI Filtering and Rectification

Fuse F1 isolates the circuit and provides protection from component failure. X-Capacitors C1 and C2 together with common mode choke (CMC) L1, L2 and L3 forms an EMI filter that attenuates both common mode and differential mode conducted EMI. BR1 converts the AC line voltage into the DC voltage seen across bulk capacitors C3, C4 and C5. The CAPZero™-2 IC (U1) along with bleed resistors, R1 and R2, discharges the stored energy in X capacitor C1 when AC is disconnected, meeting safety requirements. When AC is connected the resistors are disconnected, reducing no-load power consumption.

4.2 TOPSwitchGaN Primary

The TOP7075E device (U2) integrates an oscillator, a switch controller, start-up and protection circuitry, and PowiGaN™ switch, all on one monolithic IC. One side of the power transformer (T1) primary winding is connected to the positive side of the bulk capacitors C3, C4 & C5 and the other side is connected to the DRAIN pin (D pin) of U2. When the PowiGaN™ switch turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The spike amplitude is limited by an RCD clamp network that consists of D2, D3, R6, R7, R8, C8 and C9. Resistors R7 and R8 are used together with capacitor C9 and resistor R6 to damp high frequency ringing and improve EMI. This arrangement was selected to reduce clamp losses under light and no-load conditions. Y capacitors CY1 and CY2, connected between the primary and secondary side helps improve EMI.

The TOP7075E regulates the output by adjusting the power PowiGaN switch off-time duration in proportion to the current into its CONTROL pin. The power supply output voltage is sensed on the secondary side by shunt regulator U6 and provides a feedback signal to the primary side through optocoupler U3.

Line undervoltage and overvoltage thresholds are determined by the current supplied from resistors R3, R4 and R5 to the V pin. R10, D1, and VR1 provide output overvoltage protection (OVP). An increase in output voltage causes an increase in the bias winding voltage, sensed by VR1. Once VR1 is activated, it will inject current to the BP pin causing the IC U2 to shut down and enter auto-restart (AR).

At start-up, bypass capacitor C7 is charged through the DRAIN (D) pin, which is placed as close as possible to U2. Once it is charged, U2 begins to switch. Capacitor C7 stores enough energy to ensure the TOPSwitchGaN IC is powered until the output reaches regulation. After start-up, the bias winding delivers current via diode D4 and R9 to charge capacitor

C11 which in turn powers the controller. Resistor R9 is used to set the typical bias current of the IC U4. Ferrite bead L4 and capacitor C6 minimizes the noise on the BP Pin.

4.3 Output Rectification

Ultrafast rectifier D6 rectifies the secondary winding output of T1. The output voltage is filtered by C17, C20, C21 and C22. Resistor R14 and capacitor C14 snubs the voltage spike caused by the commutation of D6. Low ESR capacitors C17, C20, C21 and C22 help in minimizing output voltage ripple.

A forward biased winding referred to secondary return is used to power the secondary CV/CC circuitry. The winding is rectified and filtered by D5 and C13. Components Q1, R19, VR2 and C19 comprise a simple series-pass regulator to remove the line frequency ripple component from the secondary bias supply and set its voltage to ~12 V. This regulation cleans up the output voltage and current ripple by removing line frequency components for the secondary bias. Bootstrap circuit R18, D7 and VR3 provides DC voltage to C13 when there is no input to the series pass regulator during Line UV conditions.

4.4 Output Current and Voltage Control

Output current is sensed via resistor R24 and R25. This resistor is clamped by diode D9 to avoid damage to the current control circuitry during an output short-circuit. Components R12 and U4 provide a voltage reference for current sense amplifier U5. The reference voltage for current sense amplifier U5 is divided down by R13 and R16. The nominal current limit setting is 4.2 A, as programmed by R13 and R16. The non-inverting input of U5 is referenced to ground via R15 and R17. Op-amp U5 together with Q2 drives optocoupler U3. Components C12, C15, C16, C18, R15, R17, R20 and R21 are used for frequency compensation of the current loop.

The programmable shunt regulator IC, U6 (LM431BIM3/NOPB), is used for the output constant voltage control when the output current limit is not engaged. U6 is programmed via the feedback resistor divider composed of R27 and R28. The LM431BIM/NOPB varies its cathode voltage to keep its input voltage constant (2.495 V, ±1%). As the cathode voltage changes, the current through the optocoupler LED and corresponding phototransistor within U2 changes. C23, C24, R23, R26 and R29 ensure stable operation, while resistor R22 maintains minimum bias to U3.

5 PCB Layout

5.1 PCB Specification

- Layer: 1
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz
- Finishing: LF HASL
- Material: FR4
- Solder mask: Green
- Silkscreen: White

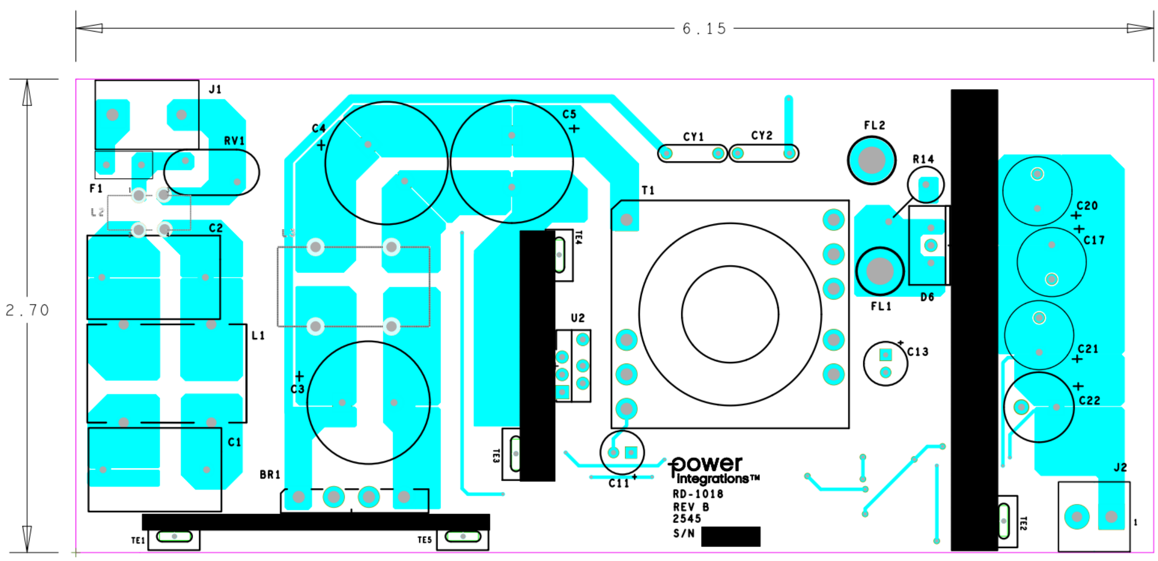


Figure 5 – Printed Circuit Board, Top View.

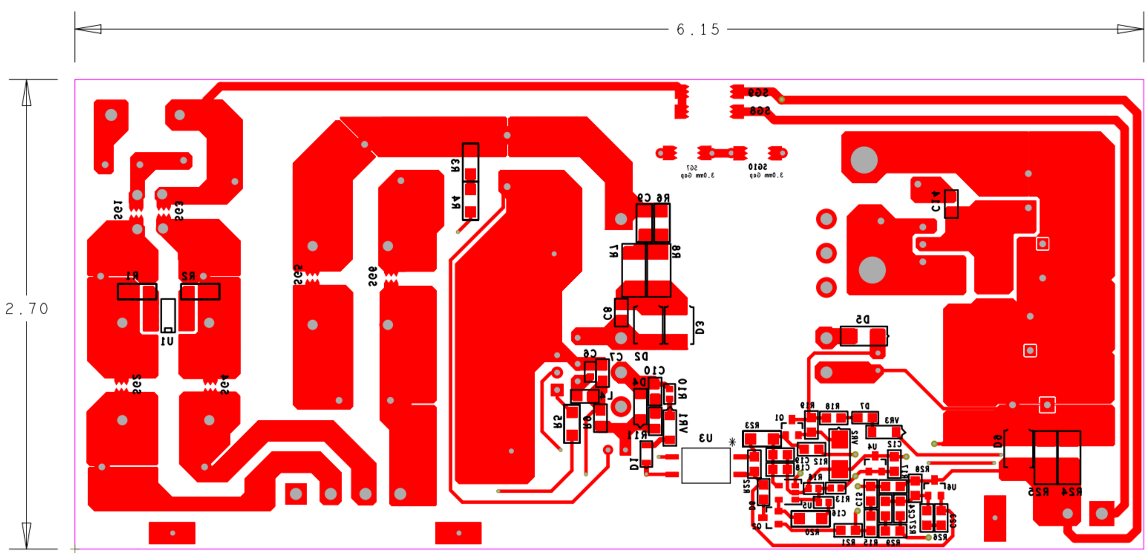


Figure 6 – Printed Circuit Board, Bottom View.

6 Bill of Materials

6.1 Electrical BOM

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	BR1	800 V, 10 A, Bridge Rectifier, GBU Case	GBU10KL-BP	Micro Commercial Co
2	2	C1 C2	680 nF, ±10%, 275 VAC, Film Capacitor, X2, 18 mm x 11 mm	PX684K3ID6	Carli
3	3	C3 C4 C5	150 μF, ±20%, 400 V, Aluminum Electrolytic Capacitor, 18 mm x 37 mm	EPAG401ELL151MM35S	Nippon Chemi-Con
4	1	C7	0.47 μF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	CGA4J2X7R1E474K125AA	TDK Corporation
5	1	C8	47 pF, ±10%, 1000 V, Ceramic Capacitor, NP0, 0805 (2012 Metric)	VJ0805A470JXGAT5Z	Vishay Vitramon
6	1	C9	4700 pF, ±10%, 1000 V, Ceramic Capacitor, X7R, 1206 (3216 Metric)	C1206C472KDRACAUTO	Kemet
7	1	C10	330 pF, ±5%, 200 V, Ceramic Capacitor, C0G, NP0, 0805 (2012 Metric)	C0805C331J2GACAUTO	Kemet
8	1	C11	22 μF, ±20%, 50 V, Aluminum Electrolytic Capacitor, Very Low ESR, 340 mohm, 5 mm x 11 mm	EKZE500ELL220ME11D	Nippon Chemi-Con
9	3	C12 C18 C19	100 nF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	08053C104KAT2A	AVX Corp
10	1	C13	47 μF, ±20%, 63 V, Aluminum Electrolytic Capacitor, General Purpose, 6.3 mm x 13 mm	63YXJ47M6.3X11	Rubycon
11	1	C14	470 pF, ±10%, 500 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	C0805C471KCRACTU	Kemet
12	1	C15	10 nF, ±10%, 50 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	C0805C103K5RACTU	Kemet
13	1	C16	220 nF, ±10%, 25 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	06033D224KAT2A	AVX
14	3	C17 C20 C21	220 μF, ±20%, 63 V, Aluminum Electrolytic Capacitor, General Purpose, 10 mm x 25 mm	EKZE630ELL221MJ25S	United Chemi-con
15	1	C22	120 μF, ±20%, 63 V, Aluminum Electrolytic Capacitor, Low ESR, 10 mm x 16 mm	EKZE630ELL121MJ16S	United Chemi-con
16	2	C23 C24	10 nF, ±10%, 50 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	C0805X103K5RAC7210	Kemet
17	2	CY1 CY2	4700 pF, ±20%, 250 VAC, Ceramic Capacitor, Radial, X1, Y2	DE2E3SA472MN3AT02F	Murata Electronics
18	1	D1	200 V, 200 mA, Diode, Standard, SOD-323	BAV21WS-7-F	Diodes, Inc.
19	2	D2 D3	1000 V, 2 A, Diode, Standard, SMB	S2M	SMC Diode Solutions
20	1	D4	1000 V, 1 A, Diode, Standard, SMA	S1MLHRVG	Taiwan Semiconductor
21	1	D5	200 V, 1 A, Diode, Ultrafast, SMA	US1D-13-F	Diodes, Inc.
22	1	D6	300 V, 10 A, Diode, Ultrafast, TO-220AB	STTH2003CT	ST Microelectronics
23	1	D7	75 V, 150 mA, Diode, General Purpose, SOD-323	1N4148WS-7-F	Diodes Inc
24	1	D9	50 V, 1 A, Standard Recovery, General Purpose, SMB	S1AB-13-F	Diodes, Inc.
25	1	F1	5 A, 250 V, Fuse Board Mount, Slow Blow, Radial	RST 5	Belfuse
26	1	L1	10 mH, 60 mohms, Toroidal, Common Mode Choke	XF0093PI-VOCMC	XFMRS
27	1	L2	150 μH, Toroidal, Common Mode Choke	Custom	Power Integrations
28	1	L3	1 mH, Toroidal, Common Mode Choke	Custom	Power Integrations
29	1	L4	80 ohms @ 100 MHz, Ferrite Bead, 0805 (2012 Metric)	EBMS201209K800	Max Echo
30	2	Q1 Q2	80 V, 0.5 A, BJT, Small Signal, SOT-23	MMBTA06LT1	Infineon Tech
31	2	R1 R2	100 kΩ, ±5%, 2/3 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-P08J104V	Panasonic

32	1	R3	2 MΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	AC1206FR-072ML	Yageo
33	1	R4	3.3 MΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	KTR18EZPF3304	Rohm Semiconductor
34	1	R5	2.2 MΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-8ENF2204V	Panasonic
35	1	R6	470 kΩ, ±5%, 2/3 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-P08J474V	Panasonic
36	2	R7 R8	20 Ω, ±5%, 3/4 W Chip Resistor, Thick Film, 2010 (3216 Metric)	RMCF2010JT20R0	Stackpole Electronics Inc
37	1	R9	3.01 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF3011V	Panasonic
38	1	R10	47 Ω, ±5%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	ERJ-3GEYJ470V	Panasonic
39	2	R11 R21	100 Ω, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	RMCF0805FT100R	Stackpole Electronics Inc
40	1	R12	4.22 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF4221V	Panasonic
41	1	R13	53.6 kΩ, ±1%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	ERJ-3EKF5362V	Panasonic
42	1	R14	20 Ω, ±5%, 2 W Through Hole Resistor, Metal Oxide	RSF200JB-20R	Yageo
43	1	R15	1 kΩ, ±5%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6GEYJ102V	Panasonic
44	1	R16	3.9 kΩ, ±1%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	ERJ-3EKF3901V	Panasonic
45	1	R17	0 Ω, ±1%, 1/4 W Chip Resistor, Thick Film, 0805 (2012 Metric)	RK73Z2ARTTD	KOA Speer Electronics, Inc.
46	1	R18	100 Ω, ±1%, 1/4 W Chip Resistor, Thick Film, 0805 (2012 Metric)	RK73H2ATTD1000F	KOA Speer Electronics, Inc.
47	1	R19	13 kΩ, ±5%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6GEYJ133V	Panasonic
48	1	R20	10 kΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-8ENF1002V	Panasonic
49	1	R22	1 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF1001V	Panasonic
50	1	R23	2 kΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-8ENF2001V	Panasonic
51	2	R24 R25	80 mΩ, ±1%, 1 W Chip Resistor, Thick Film, 2010 (5025 Metric)	WSL2010R0800FEA18	Vishay Dale
52	1	R26	20 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF2002V	Panasonic
53	1	R27	158 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF1583V	Panasonic
54	1	R28	10 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF1002V	Panasonic
55	1	R29	20 kΩ, ±5%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6GEYJ203V	Panasonic
56	1	R30	0 Ω, ±1%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	RC0603FR-070RL	Yageo
57	1	RV1	320 VAC, 23 J, Through Hole Disc, 10 mm	V320LA10P	Littelfuse
58	1	T1	PQ32/30, Bobbin, Vertical, 12 pins	B65880E2012D001	TDK
59	1	U1	CAPZero-3, CAP300DG, SO-8C	CAP300DG	Power Integrations
60	1	U2	TOPSwitchGaN, TOP7075E, eSOP-12B	TOP7075E	Power Integrations
61	1	U3	Optoisolator, Transistor Output, 5300 VRMS, 70 V, CTR 100-6200%, 1 Channel 4-SMD	SFH6106-3T	Vishay Semiconductor Opto Division
62	2	U4 U6	2.495 V ±1%, Shunt Regulator IC, -40 to 85 °C, SOT-23	LM431BIM3/NOPB	National Semiconductor

63	1	U5	OPAMP, General Purpose, 1 Circuit, SOT-23-5	LM321MF/NOPB	Texas Instruments
64	1	VR1	13 V, ±5%, 500 mW, Diode, Zener, SOD-123	MMSZ5243BT1G	ON Semiconductor
65	1	VR2	12 V, ±5%, 1 W, Diode, Zener, SMA	SMAZ12-13-F	Diodes, Inc.
66	1	VR3	30 V, ±5%, 500 mW, Diode, Zener, SOD-123	MMSZ5256B-7-F	Diodes, Inc.

6.2 Mechanical BOM

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	J1	3 Position (1 x 3) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	1715035	Phoenix Contact
2	1	J2	2 Position (1 x 2) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	1715022	Phoenix Contact
3	5	TE1 TE2 TE3 TE4 TE5	Terminal, Eyelet, Tin Plated Brass, Zierick, PN 190	190	Keystone
4	1	HS1	Bridge Rectifier Heatsink		Power Integrations
5	1	HS2	TOPSwitchGaN Heatsink		Power Integrations
6	1	HS3	Output Rectifier Heatsink		Power Integrations
7	3		Flat Washer, #4		
8	3		Machine Screw #4-40x0.250		
9	1		eSIP-7C Edge Clip		
10	1		Thermal Pad, BER103, 0.009-THK-TO-220		
11	1		Washer Shoulder, #4, 0.140 Shoulder		
12	1		Wakefield Thermal Joint Compound		Wakefield

7 Transformer Specification

7.1 Electrical Diagram

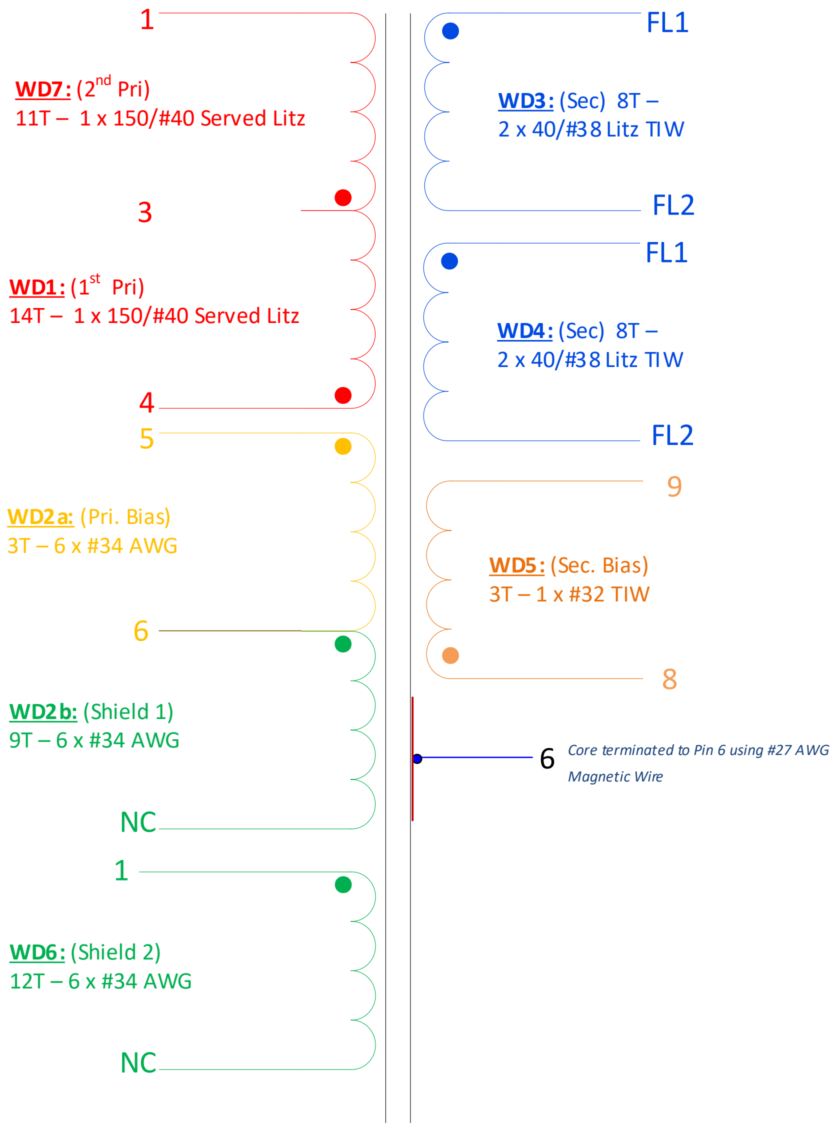


Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK} and 100 kHz frequency, between pin 1 to pin 4, with all other Windings open.	240 μH
Tolerance	Tolerance of Primary Inductance.	±5%
Leakage Inductance	Measured across primary winding with all other windings shorted.	< 2.5 μH

7.3 Material List

Item	Description
[1]	Core: PQ3230, TDK-PC95.
[2]	Bobbin: PQ32/30-Vert-12 pins (6/6); PI#: 25-01198-00; or equivalent.
[3]	Magnet wire: #34 AWG, Double Coated.
[4]	Magnet wire: #32 AWG, Triple Insulated Wire.
[5]	Magnet wire: 150/#40 Served Litz.
[6]	Magnet wire: 40/#38 Litz, Triple Insulated Wire.
[7]	Bus wire: #28 AWG, Alpha wire, tinned copper.
[8]	Tape: 3M 13450-F, Polyester Film, 18.6 mm, 1 mil thick.
[9]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

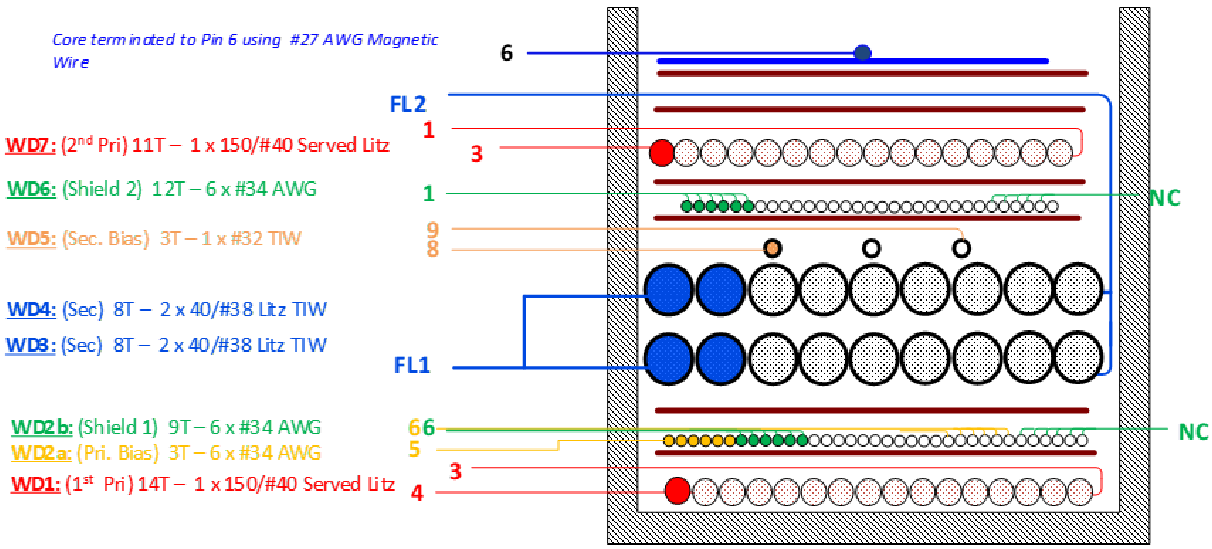
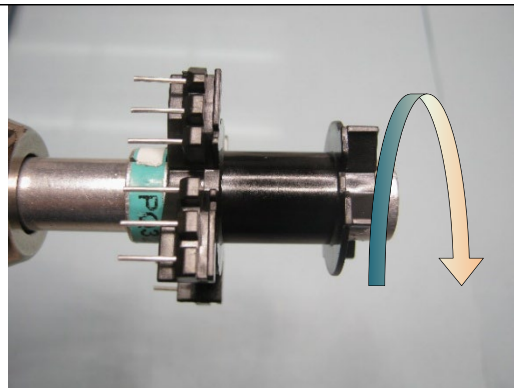
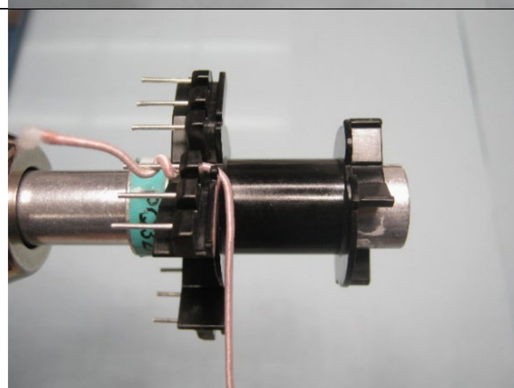
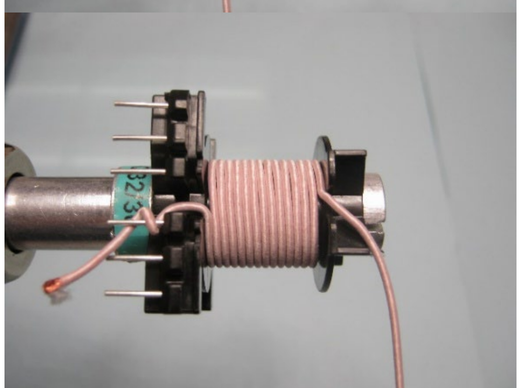
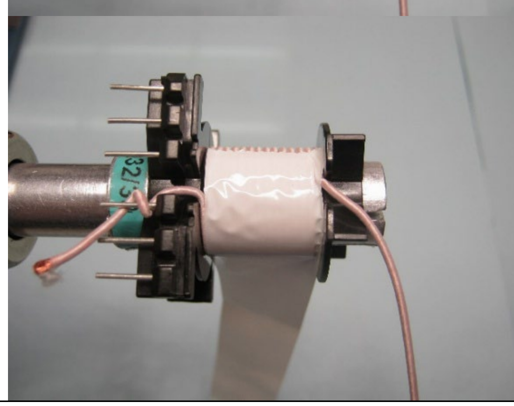


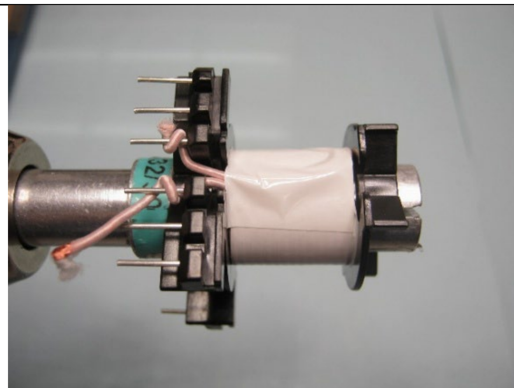
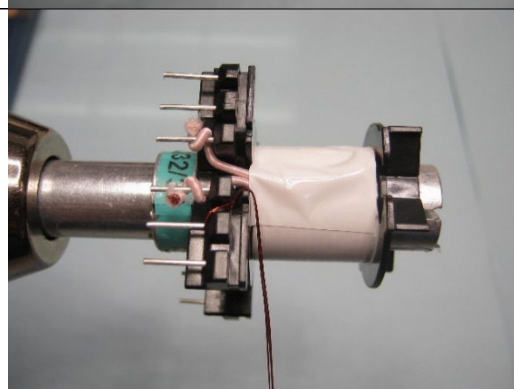
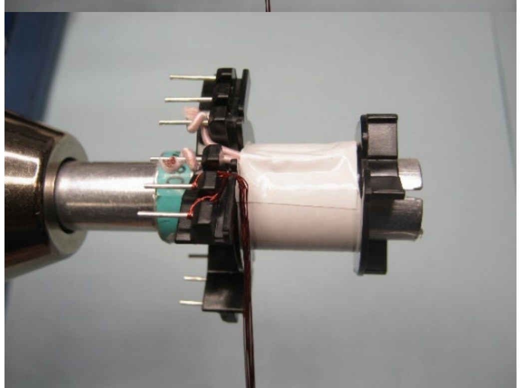
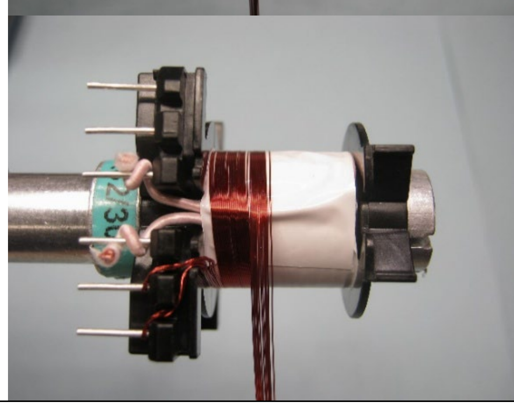
Figure 8 – Transformer Build Diagram.

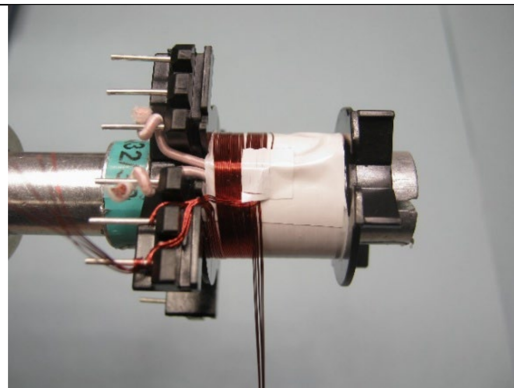
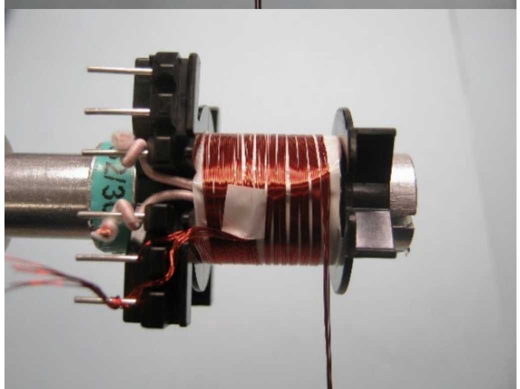
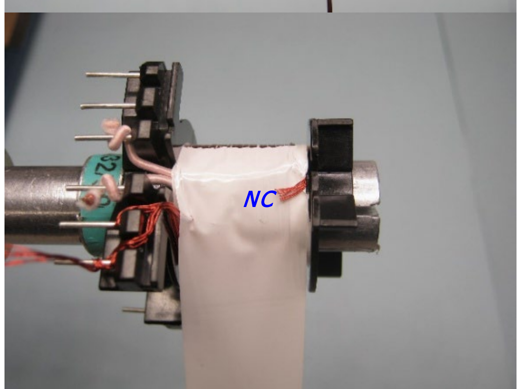
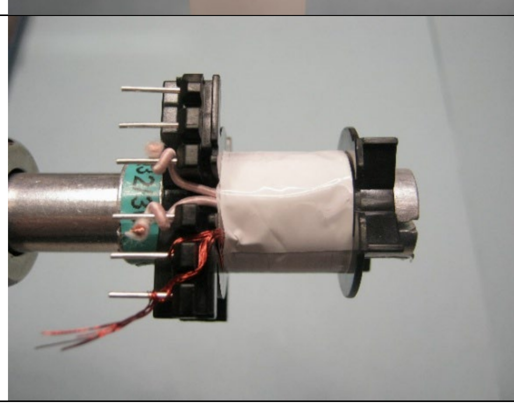
7.5 Transformer Instructions

Winding preparation	Position the bobbin Item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**	Start at pin 4, wind 14 turns of wire Item [5] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 3.
Insulation	1 layer of tape Item [8].
WD2a: Pri. Bias **&** **WD2b: Shield1**	Use 6 wires Item [3] start at pin 5 for Primary Bias winding, also use 6 wires same Item [3] start at pin 6 for Shield1 winding. Wind all 12 wires in parallel, at the 3rd turn, place 1 small piece of tape to hold the wires then bring 6 wires of Bias winding to the left and terminate at pin 6. Continue winding 6 wires of Shield1 winding to 9th turn and cut short as No-Connect.
Insulation	1 layer of tape Item [8].
WD3 & WD4 **Secondary**	Start at left slot of secondary side, use 2 wires Item [6], leaving ~ 40.0 mm floating, and mark as FL1. Wind 8 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 60.0 mm floating, and mark FL2 for Winding 3. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2 for Winding 4.
WD5 **Sec. Bias**	Start at pin 8, wind 3 turns of wire Item [4] on top of secondary windings and terminate at pin 9.
Insulation	1 layer of tape Item [8].
WD6 **Shield 2**	Use 6 wires Item [3], start at pin 1, wind 12 turns from left to right, spread the wires evenly. At the last turn, cut short as No-Connect.
Insulation	1 layer of tape Item [8].
WD7 **2nd Primary**	Start at pin 3, wind 11 turns of wire Item [5] from left to right, spread the wire evenly. At the last turn, bring the wire to left and terminate at pin 1.
Insulation	1 layer of tape Item [8].
Finish	Bring 4 wires marked as F2 to left and secure with 2 layers of tape Item [8]. Gap core halves to get 240 μH. Solder pin 6 with bus-wire Item [7] then lean along core halves and secure with tape. Remove extra pins 2 & 7. Varnish with Item [9].

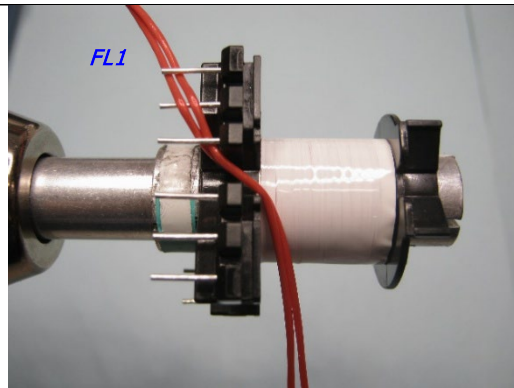
7.6 Transformer Winding Illustrations

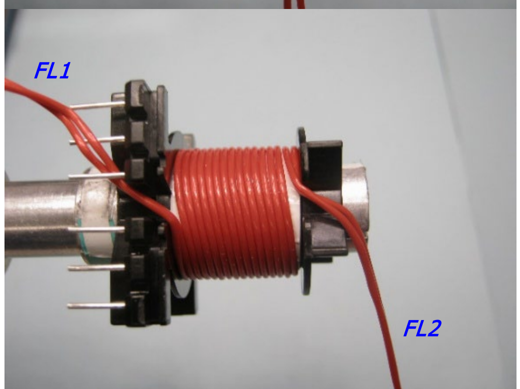
Winding preparation		Position the bobbin Item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**	  	Start at pin 4, wind 14 turns of wire Item [5] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 3.

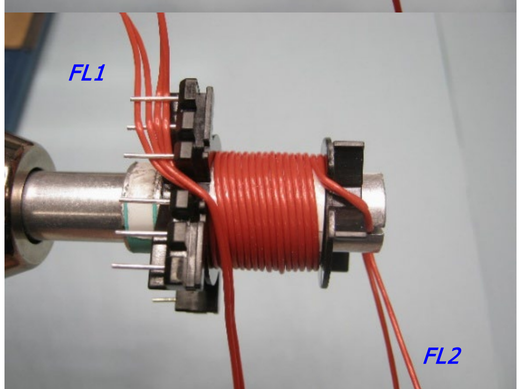
Insulation		1 layer of tape Item [8].
WD2a: Pri. Bias & WD2b: Shield1	  	Use 6 wires Item [3] start at pin 5 for Primary Bias winding, also use 6 wires same Item [3] start at pin 6 for Shield1 winding. Wind all 12 wires in parallel, at the 3rd turn, place 1 small piece of tape to hold the wires, then bring 6 wires of Bias winding to the left and terminate at pin 6. Continue winding 6 wires of Shield1 winding to 9th turn and cut short as No-Connect.

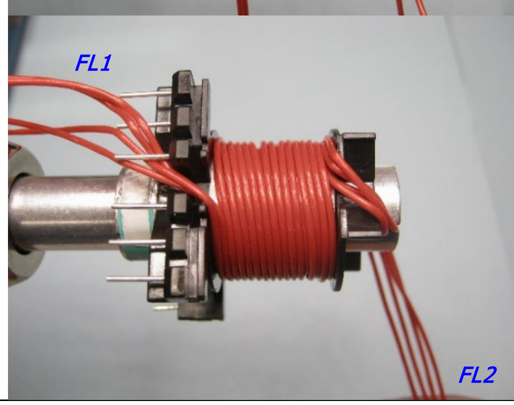
	  	
Insulation		1 layer of tape Item [8].

WD3 & WD4 Secondary

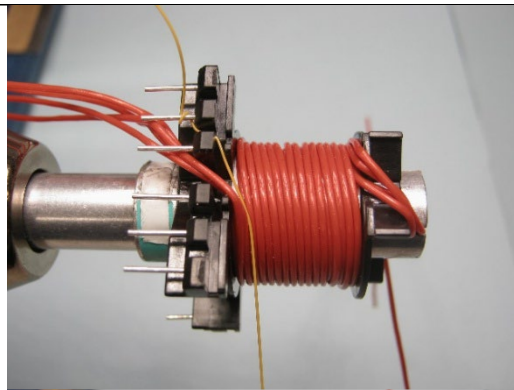
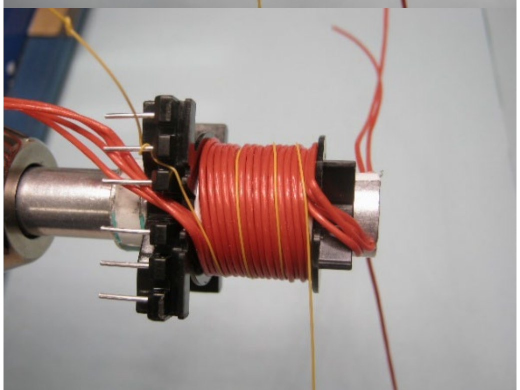
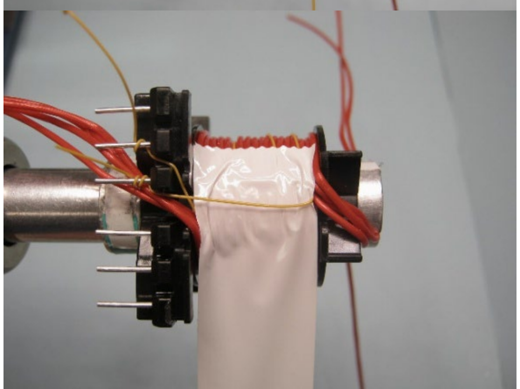
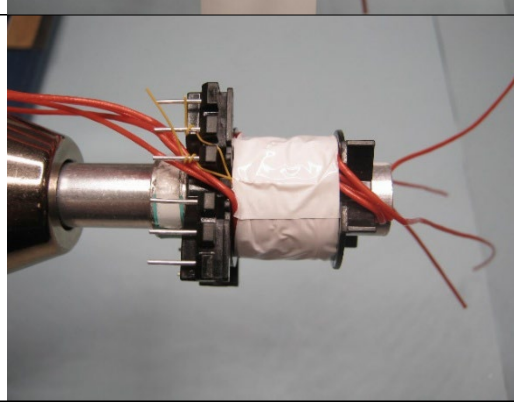


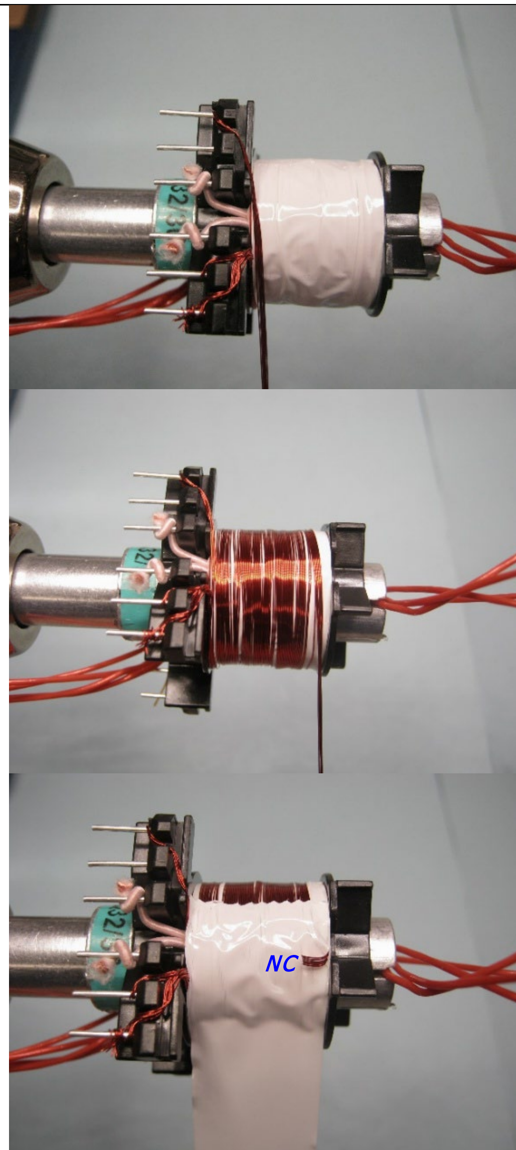
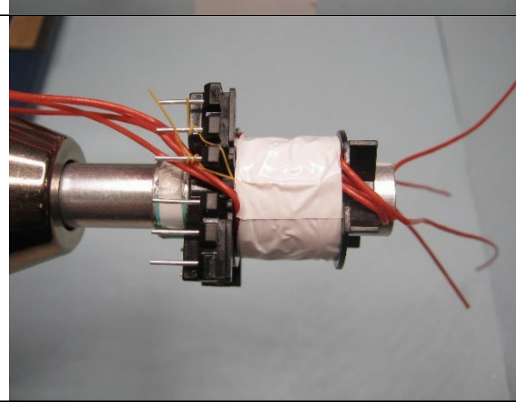


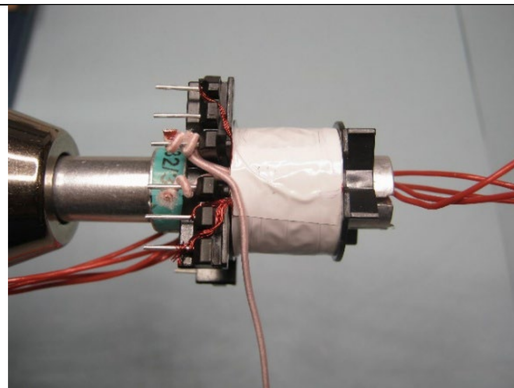
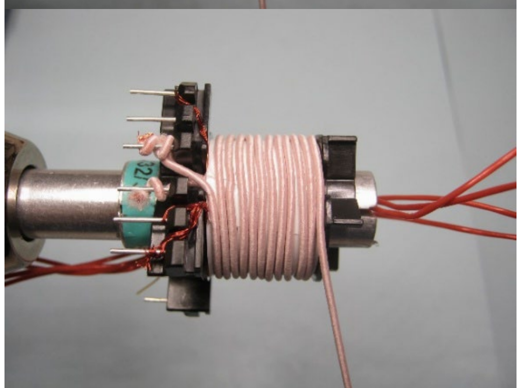
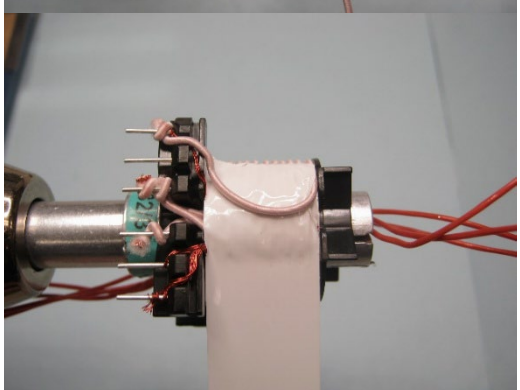
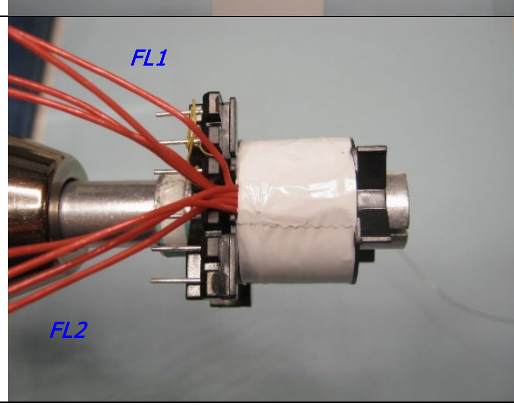


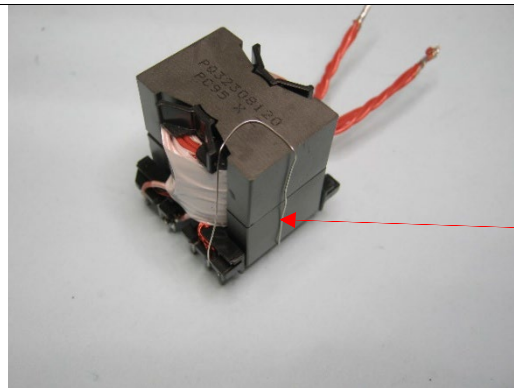
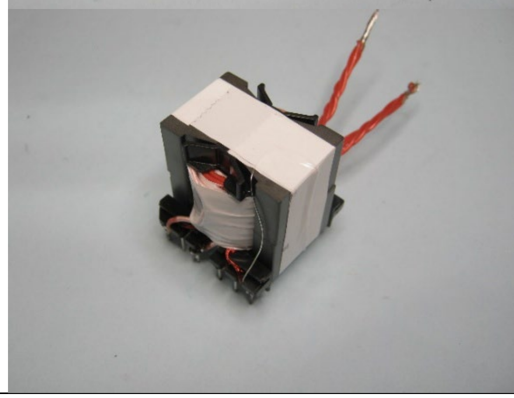


Start at left slot of secondary side, use 2 wires Item [6], leaving ~ 40.0 mm floating, and mark as FL1. Wind 8 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 60.0 mm floating, and mark FL2 for Winding 3.
Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2 for Winding 4.

WD5 **Sec Bias**		Start at pin 8, wind 3 turns of wire Item [4] on top of secondary windings and terminate at pin 9.
Insulation		1 layer of tape Item [8].

WD6 **Shield 2**	 	Use 6 wires Item [3], start at pin 1, wind 12 turns from left to right, spread the wires evenly. At the last turn, cut short as No-Connect.
Insulation		1 layer of tape Item [8].

WD7 **2nd Primary**	  	Start at pin 3, wind 11 turns of wire Item [5] from left to right, spread the wire evenly. At the last turn, bring the wire to left and terminate at pin 1.
Insulation		1 layer of tape Item [8].

Finish	 	Bring 4 wires marked as F2 to left and secure with 2 layers of tape Item [8]. Gap core halves to get 240 μH. Solder pin 6 with bus-wire Item [7] then lean along core halves and secure with tape. Removes extra pins 2 & 7. Varnish with Item [9].

8 Design Spreadsheet

1	**ACDC_TOPSwitchGaN_Flyback_102425; Rev.0.4; Copyright Power Integrations 2025**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**TOPSwitchGaN Single/Multi Output Flyback Design Spreadsheet**
2	APPLICATION VARIABLES					Design Title
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	85		85	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			85-265 VAC		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	450.0		450.0	μF	Input capacitor
9	VOUT	42.00		42.00	V	Output voltage at the board
10	IOUT	4.000		4.000	A	Output current
11	POUT		Info	168.00	W	The specified output power exceeds the device power capability: Verify thermal performance if no other warnings
12	EFFICIENCY	0.89		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.60		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
15						
16						
17						
18	PRIMARY CONTROLLER SELECTION					
19	PACKAGE_DEVICE	eSIP		eSIP		Device Package
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	TOP7075		TOP7075		Generic device code
22	DEVICE_CODE			TOP7075E		Actual device code
23	POUT_MAX		Warning	165	W	Power output desired is more than the power capability of device. Please select a different device or reduce power output desired.
24	RDSON_100DEG			0.49	Ω	Primary switch on time drain resistance at 100 °C
25	ILIMIT_MIN			4.185	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			4.500	A	Typical current limit of the primary switch
27	ILIMIT_MAX			4.815	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			800	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.94	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			634.7	V	Peak drain voltage on the primary switch during turn-off. A 131 V leakage spike voltage is assumed
31						
32						
33						

34	WORST CASE ELECTRICAL PARAMETERS					
35	FSWITCHING_MAX	126000		126000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage.
36	VOR	130.0		130.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			94.62	V	Valley of the minimum input AC voltage at full load
38	KP		Info	0.44		Design is too continuous and may result in leading edge SOA triggering: increase the VOR
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.581		Primary switch duty cycle
41	TIME_ON_MAX			12.50	μs	Primary switch on-time
42	TIME_ON_AT_FSWITCHING_MAX			4.61	μs	Primary switch on-time at FSWITCHING_MAX
43	TIME_OFF			3.32	μs	Primary switch off-time at 85 VAC, 168 W, and 126000 Hz.
44	LPRIMARY_MIN			226.4	μH	Minimum primary inductance
45	LPRIMARY_TYP			238.3	μH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			250.2	μH	Maximum primary inductance
48						
49	PRIMARY CURRENT					
50	IPEAK_PRIMARY			4.734	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			2.385	A	Primary switch current pedestal
52	IAVG_PRIMARY			1.926	A	Primary switch average current
53	IRIPPLE_PRIMARY			2.838	A	Primary switch ripple current
54	IRMS_PRIMARY			2.603	A	Primary switch RMS current
55						
56	SECONDARY CURRENT					
57	IPEAK_SECONDARY			14.793	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			7.452	A	Secondary winding current pedestal
59	IRMS_SECONDARY			6.905	A	Secondary winding RMS current
60						
61						
62						
63	TRANSFORMER CONSTRUCTION PARAMETERS					
64	CORE SELECTION					
65	CORE	PQ32		PQ32		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
66	CORE CODE			PQ32/30-3C95		Core code
67	AE			167.00	mm^2	Core cross sectional area
68	LE			74.70	mm	Core magnetic path length
69	AL			6570	nH/turns^2	Ungapped core effective inductance
70	VE			12500.0	mm^3	Core volume
71	BOBBIN			CPV-PQ32/30-1S-12P-Z		Bobbin

72	AW			98.18	mm^2	Window area of the bobbin
73	BW			18.70	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75						
76	PRIMARY WINDING					
77	NPRIMARY			25		Primary turns
78	BPEAK			2978	Gauss	Peak flux density
79	BMAX			2813	Gauss	Maximum flux density
80	BAC			826	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			381	nH/turns^2	Typical gapped core effective inductance
82	LG			0.519	mm	Core gap length
83						
84	PRIMARY BIAS WINDING					
85	NBIAS_PRIMARY			3	turns	Primary bias winding number of turns
86						
87	SECONDARY WINDING					
88	NSECONDARY	8		8	turns	Secondary winding number of turns
89						
90	SECONDARY BIAS WINDING					
91	NBIAS_SECONDARY			3	turns	Secondary bias winding number of turns
92						
93						
94						
95	PRIMARY COMPONENTS SELECTION					
96	LINE UNDERVOLTAGE					
97	BROWN-IN REQURED			66.30	V	Required AC RMS/DC line voltage brown-in threshold
98	RLS			6.80	MΩ	Connect two 3.4 MOhm resistors to the V-pin for the required UV/OV threshold
99	BROWN-IN ACTUAL			55 V - 67.7 V	V	Actual AC RMS/DC brown-in range
100	BROWN-OUT ACTUAL			46.9 V - 58.5 V	V	Actual AC RMS/DC brown-out range
101						
102	LINE OVERVOLTAGE					
103	OVERVOLTAGE_LINE		Info	256.4 V - 287.7 V	V	The line over-voltage threshold is lower than the maximum input AC RMS/DC voltage
104						
105	PRIMARY BIAS DIODE					
106	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
107	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE_PRIMARY			60.55	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS_PRIMARY			22	μF	Bias winding rectification capacitor
110	CBP			0.47	μF	BP pin capacitor
111						

112						
113						
114	SECONDARY COMPONENTS					
115	VREF_REG			1.25	V	Reference voltage of the feedback
116	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
117	RFB_LOWER			3.09	kΩ	Lower feedback resistor
118						
119	SECONDARY BIAS DIODE					
120	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
121	VBIAS_SECONDARY	12.0		12.0	V	Rectified secondary bias voltage
122	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
123	VREVERSE_BIASDIODE_SECONDARY			56.80	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
124	CBIAS_SECONDARY			10	μF	Bias winding rectification capacitor
125						
126						
127	MULTIPLE OUTPUT PARAMETERS					
128	OUTPUT 1					
129	VOUT1			42.00	V	Output 1 voltage
130	IOUT1			4.00	A	Output 1 current
131	POUT1			168.00	W	Output 1 power
132	VD1			0.70	V	Forward voltage drop of diode for output 1
133	NS1			8.00	turns	Number of turns for output 1
134	ISPEAK1			14.79	A	Instantaneous peak value of the secondary current for output 1
135	ISRMS1			6.905	A	Root-mean-squared value of the secondary current for output 1
136	ISRIPPLE1			5.628	A	Current ripple on the secondary waveform for output 1
137	PIV1_CALCULATED			193.41	V	Computed peak inverse voltage stress on the diode for output 1
138	OUTPUT_RECTIFIER1	AUTO		BYV32-200		Recommended diode for output 1.
139	PIV1_RATING			200.00	V	Peak inverse voltage rating on the diode for output 1
140	TRR1			25.00	ns	Reverse recovery time of the diode for output 1
141	IFM1			18.00	A	Maximum forward continuous current of the diode for output 1
142	PLOSS_DIODE1			8.18	W	Maximum diode power loss for output 1
143						
144	OUTPUT 2					
145	VOUT2			0.00	V	Output 2 voltage
146	IOUT2			0.000	A	Output 2 current
147	POUT2			0.00	W	Output 2 power
148	VD2			N/A	V	Forward voltage drop of diode for output 2
149	NS2			N/A	turns	Number of turns for output 2
150	ISPEAK2			N/A	A	Instantaneous peak value of the secondary current for output 1

151	ISRMS2			N/A	A	Root mean squared value of the secondary current for output 2
152	ISRIPPLE2			N/A	A	Current ripple on the secondary waveform for output 2
153	PIV2			N/A	V	Computed peak inverse voltage stress on the diode for output 2
154	OUTPUT_RECTIFIER2	AUTO		N/A		Recommended diode for output 2.
155	PIV2_RATING			N/A	V	Peak inverse voltage rating on the diode for output 2
156	TRR2			N/A	ns	Reverse recovery time of the diode for output 2
157	IFM2			N/A	A	Maximum forward continuous current of the diode for output 2
158	PLOSS_DIODE2			N/A	W	Maximum diode power loss for output 2
159						
160	OUTPUT 3					
161	VOUT3			0.00	V	Output 3 voltage
162	IOUT3			0.000	A	Output 3 current
163	POUT3			0.00	W	Output 3 power
164	VD3			N/A	V	Forward voltage drop of diode for output 3
165	NS3			N/A	turns	Number of turns for output 3
166	ISPEAK3			N/A	A	Instantaneous peak value of the secondary current for output 1
167	ISRMS3			N/A	A	Root mean squared value of the secondary current for output 3
168	ISRIPPLE3			N/A	A	Current ripple on the secondary waveform for output 3
169	PIV3			N/A	V	Computed peak inverse voltage stress on the diode for output 3
170	OUTPUT_RECTIFIER3	AUTO		N/A		Recommended diode for output 3
171	PIV3_RATING			N/A	V	Peak inverse voltage rating on the diode for output 3
172	TRR3			N/A	ns	Reverse recovery time of the diode for output 3
173	IFM3			N/A	A	Maximum forward continuous current of the diode for output 3
174	PLOSS_DIODE3			N/A	W	Maximum diode power loss for output 2
175						
176	PO_TOTAL			168.00	W	Total power of all outputs
177	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
178						
179						

9 Common Mode Choke L2 Assembly

9.1 Electrical Diagram

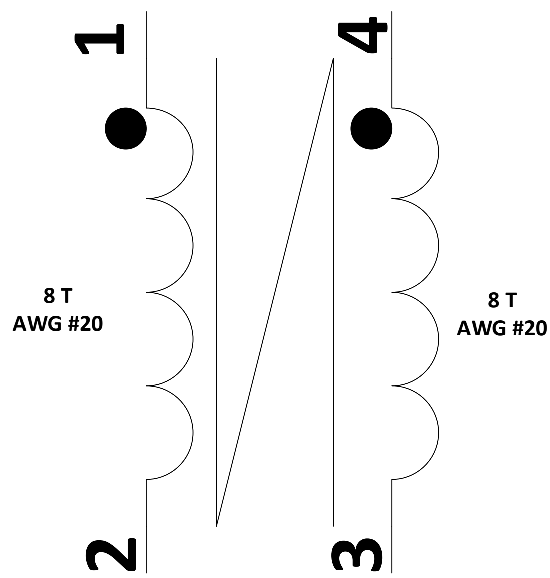


Figure 9 – Inductor Electrical Diagram.

Figure 10 – CMC Assembled Photo.

9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and pin 3 or pin 2 and pin 4 with all other windings open.	150 μH
Tolerance	Tolerance of Primary Inductance.	±20%

9.3 Materials

Item	Description
[1]	Toroid Core: PI P/N 32-00315-00 (Green)
[2]	Magnet Wire: #20 AWG
[3]	TIW Wire: #20 AWG

9.4 Inductor Construction

1. Winding 1 - Wind 8 turns of item 2 and 3 in bifilar as shown in figure 10.

10 Common Mode Choke L3 Assembly

10.1 Electrical Diagram

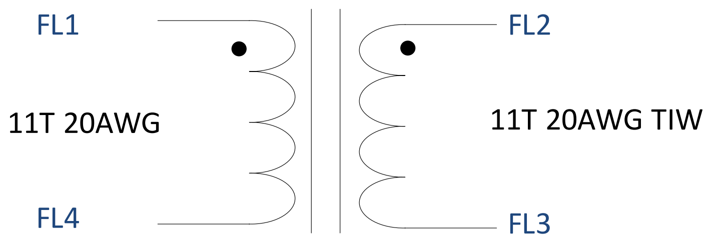


Figure 11 – Inductor Electrical Diagram.

10.2 Electrical Specifications

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	1 mH, ±15%

10.3 Material List

Item	Description
[1]	Ferrite Core Toroid: Encom Ltd., YJ15K-T18/10/7C. PI P/N 30-00398-00
[2]	Insulated Wire: #20 AWG, Solderable Double Coated
[3]	Triple Insulated Wire: #20 AWG, Furukawa TEX-E or Equivalent

10.4 Construction Details

1. Wind 11 turns of Items [2] and [3] together as shown in figure 12.

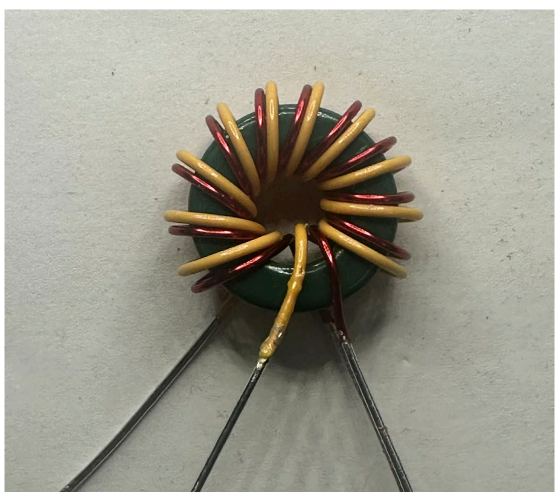
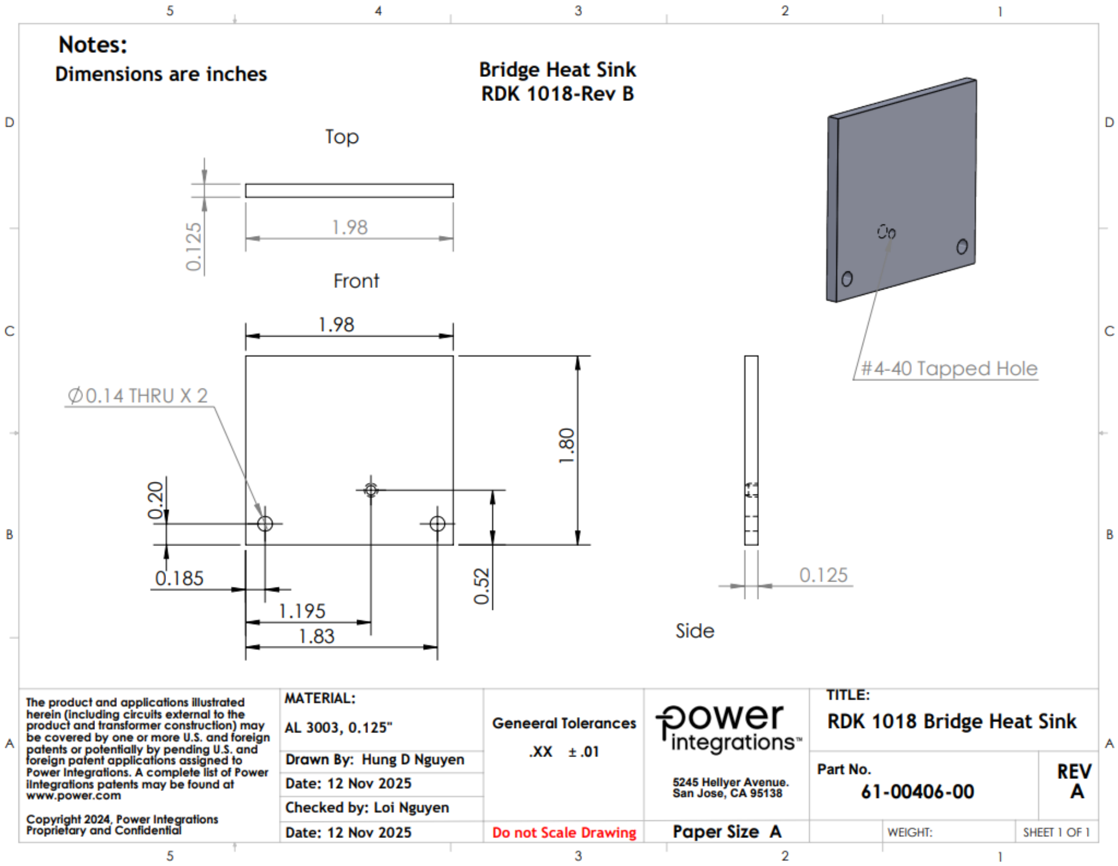


Figure 12 – Finished Part, Front View.

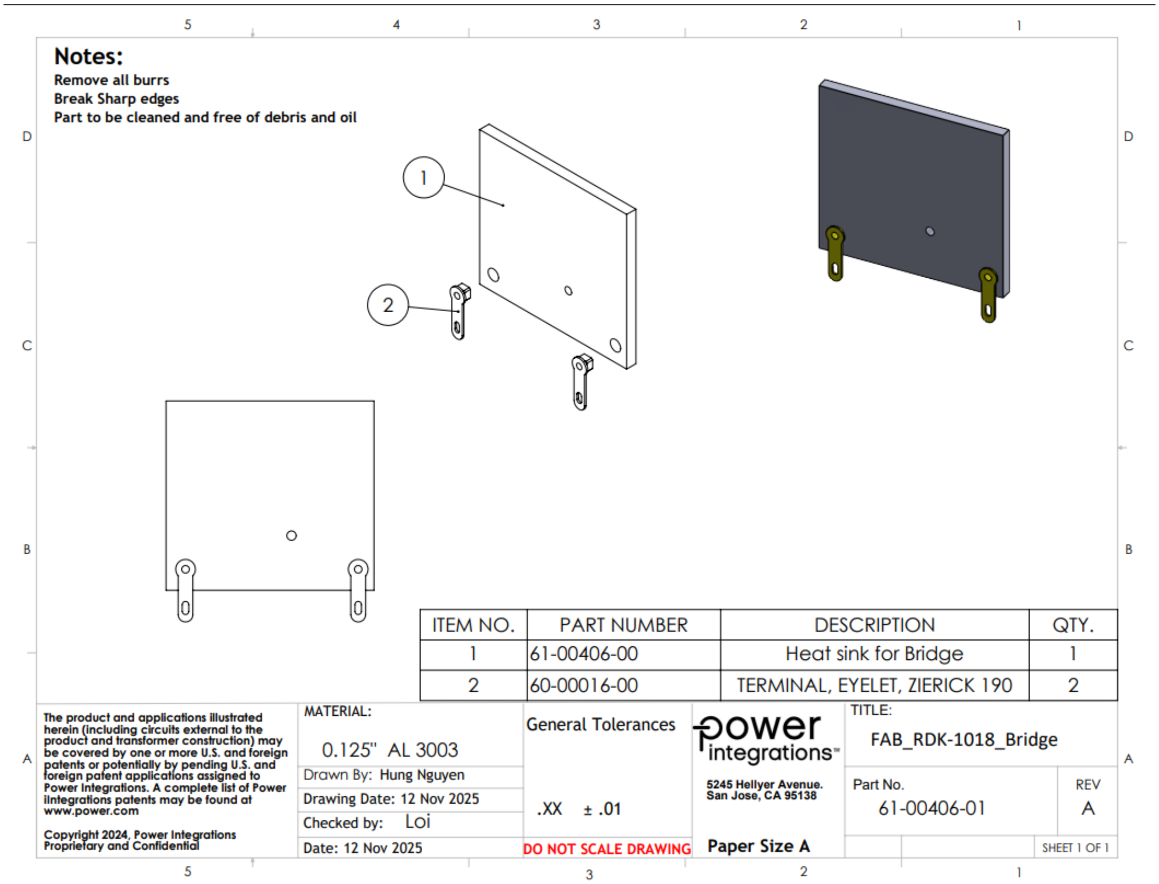
11 Heatsink Assembly

11.1 Bridge Rectifier Heatsink

11.1.1 Drawing

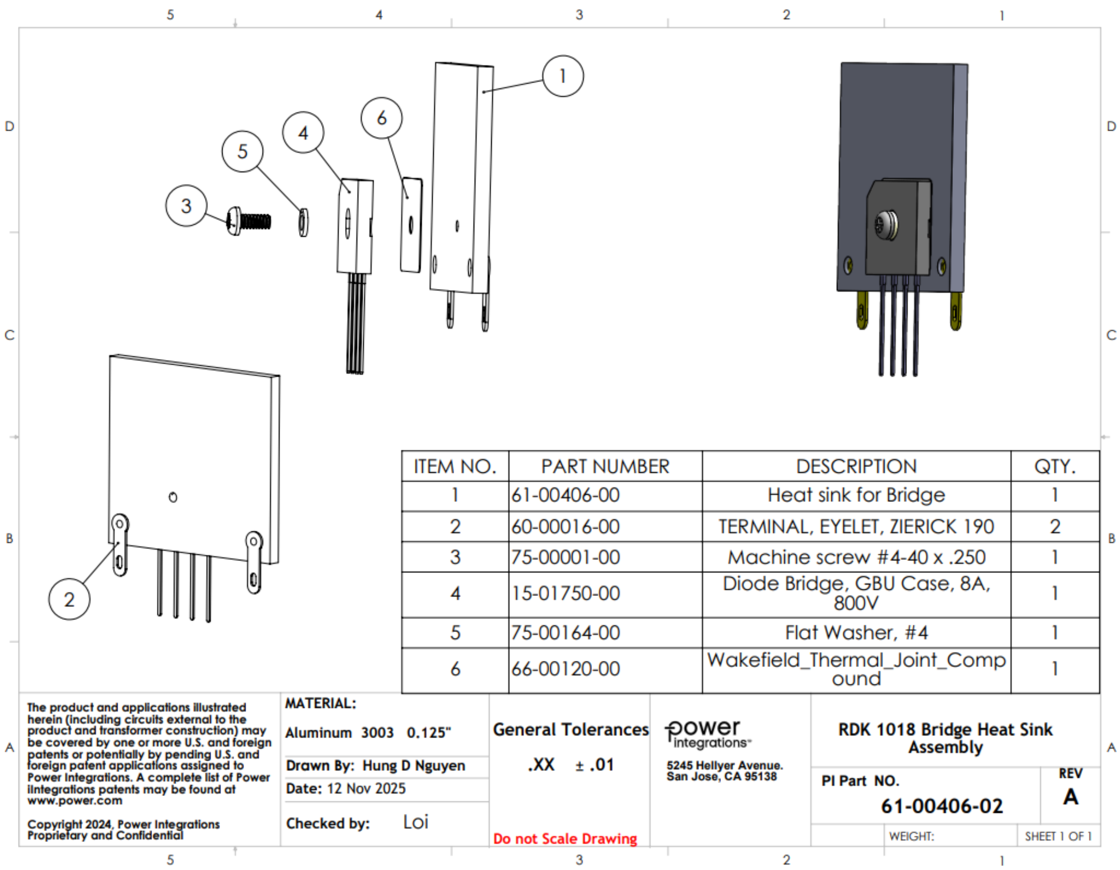


11.1.2 Fabrication



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00406-00	Heat sink for Bridge	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	2

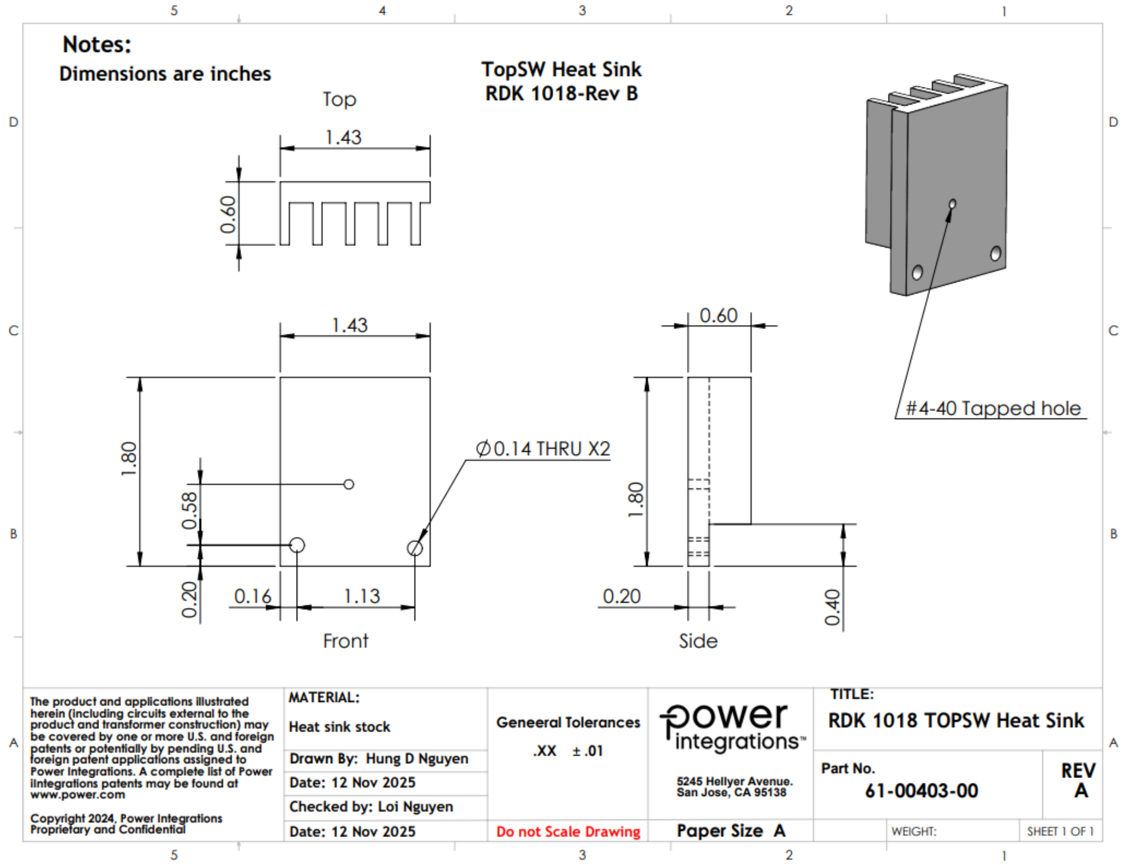
11.1.3 Assembly



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00406-00	Heat sink for Bridge	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	2
3	75-00001-00	Machine screw #4-40 x .250	1
4	15-01750-00	Diode Bridge, GBU Case, 8A, 800V	1
5	75-00164-00	Flat Washer, #4	1
6	66-00120-00	Wakefield_Thermal_Joint_Compound	1

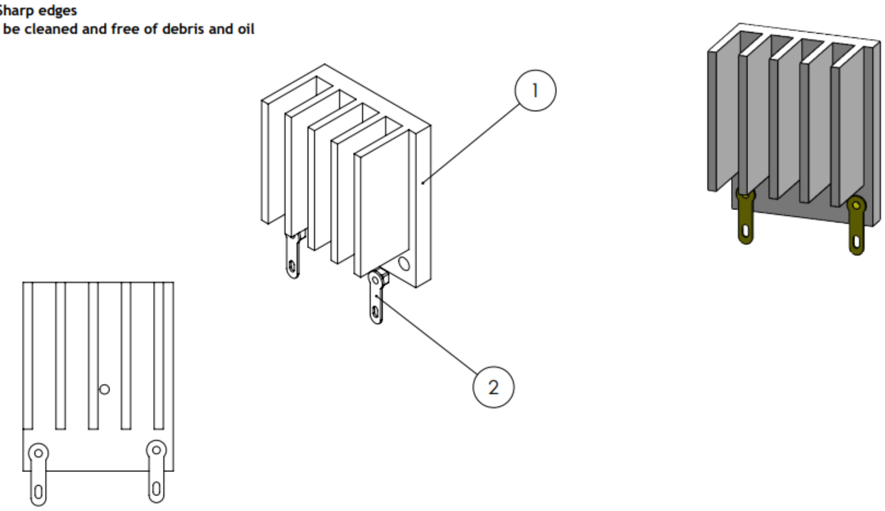
11.2 TOPSwitchGaN IC Heatsink

11.2.1 Drawing



11.2.2 Fabrication

Notes:
Remove all burrs
Break Sharp edges
Part to be cleaned and free of debris and oil



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00403-00	HEATSINK FOR TOPSW	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	2

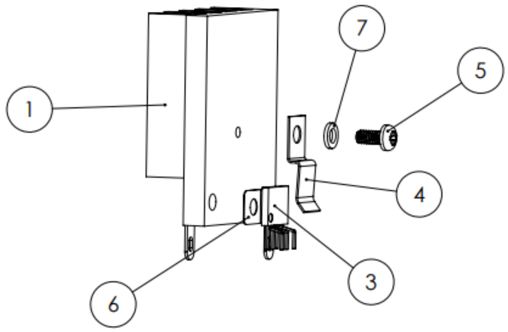
MATERIAL: Heat sink stock
Drawn By: Hung Nguyen
Drawing Date: 12 Nov 2025
Checked by: Loi
Date: 12 Nov 2025

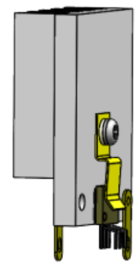
General Tolerances
.XX ± .01
DO NOT SCALE DRAWING

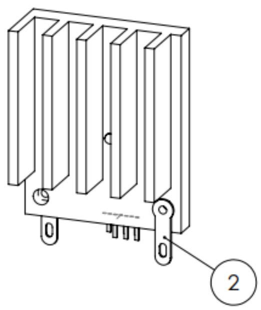
power integrations
5245 Hellyer Avenue. San Jose, CA 95138
Paper Size A

TITLE: FAB_RDK-1018_TOPSW
Part No. 61-00403-01
REV A
SHEET 1 OF 1

11.2.3 Assembly







ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00403-00	HEATSINK FOR TOPSW	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	2
3	10-01638-00	TOPSwitch-GaN, TOP7075E, eSIP-7C	1
4	60-00042-00	eSIP-7C Edge Clip	1
5	75-00001-00	Machine screw #4-40 x .250	1
6	60-00099-00	Thermal Grease	1
7	75-00164-00	Flat Washer, #4	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Iintegrations patents may be found at www.power.com

MATERIAL: Heat sink stock

Drawn By: Hung D Nguyen

Date: 12 Nov 2025

Checked by: Loi

General Tolerances .XX ± .01

Do not Scale Drawing

power integrations

5245 Hellyer Avenue. San Jose, CA 95138

RDK 1018 TOPSW Heat Sink Assembly

PI Part NO. 61-00403-02

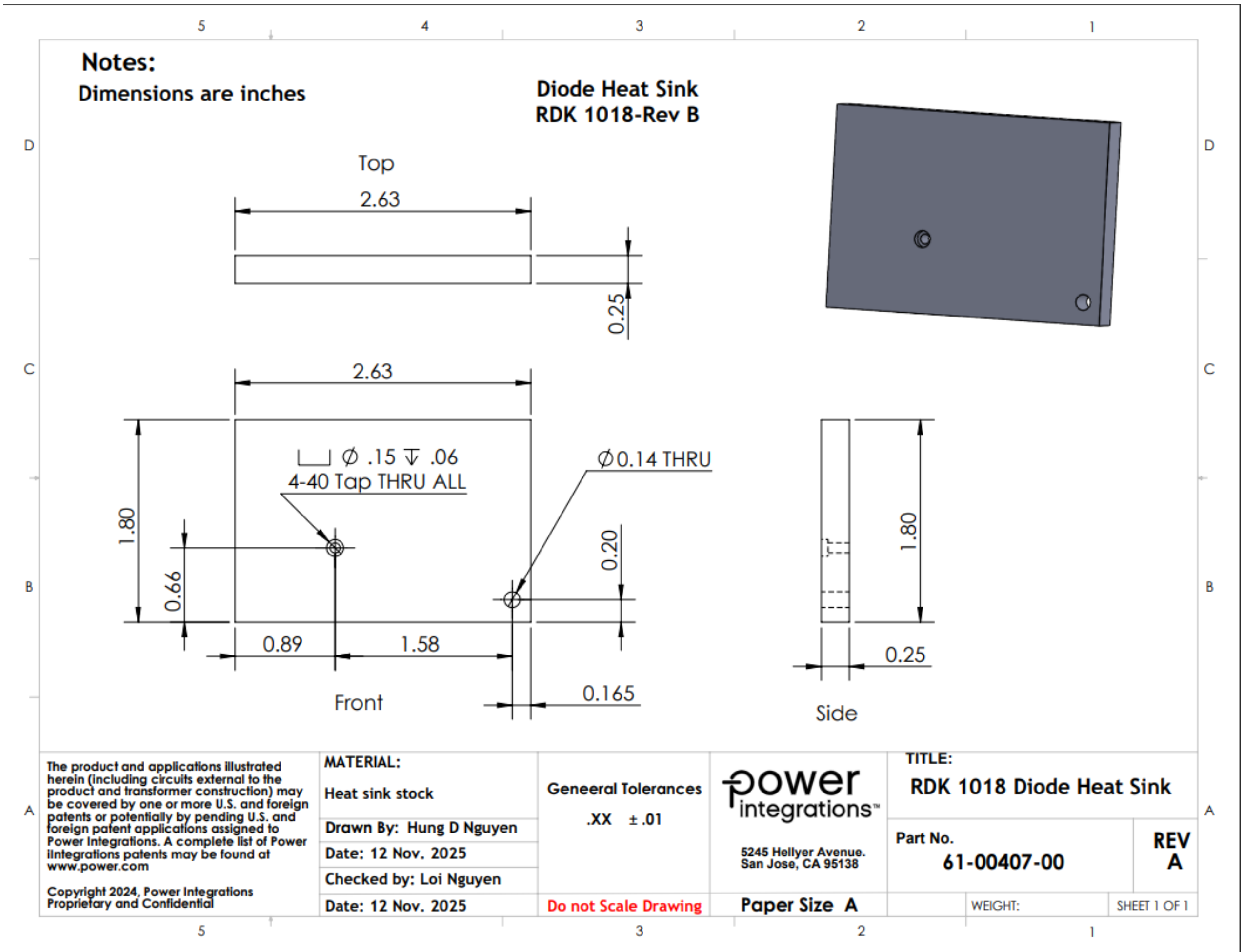
REV A

WEIGHT:

SHEET 1 OF 1

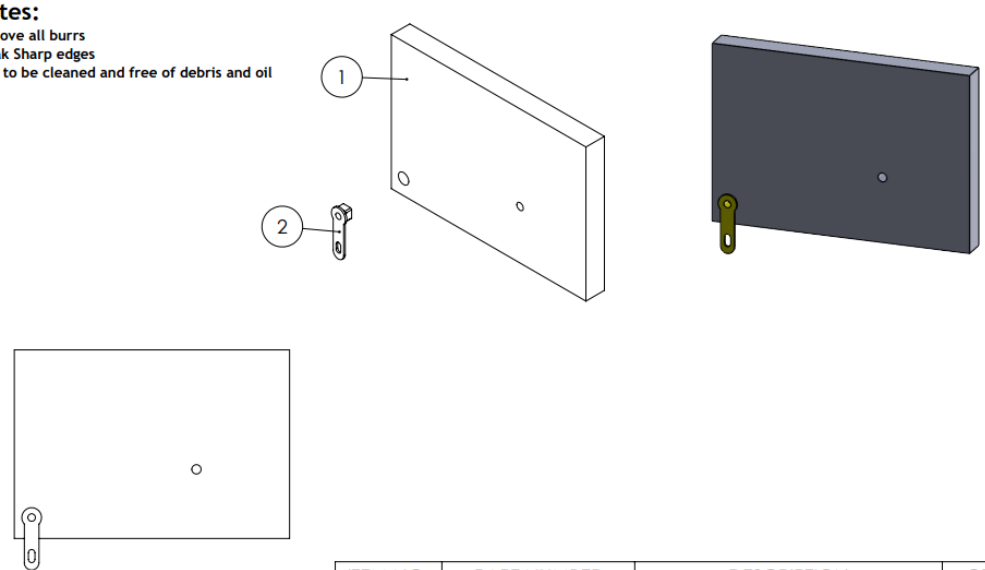
11.3 Output Rectifier Heatsink

11.3.1 Drawing



11.3.2 Fabrication

Notes:
Remove all burrs
Break Sharp edges
Part to be cleaned and free of debris and oil



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00407-00	Heat sink for Bridge	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

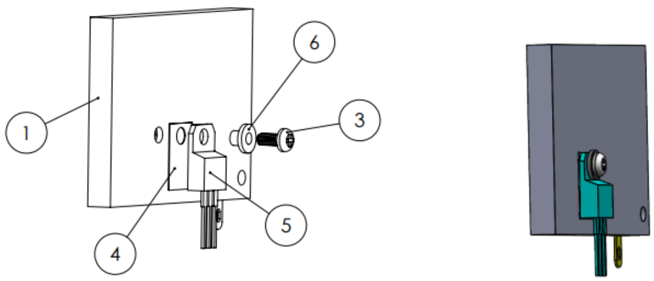
MATERIAL: Heat sink stock
Drawn By: Hung Nguyen
Drawing Date: 12 Nov 2025
Checked by: Loi
Date: 12 Nov 2025

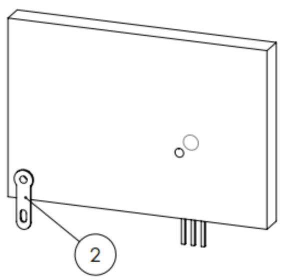
General Tolerances
.XX ± .01
DO NOT SCALE DRAWING

power integrations
5245 Hellyer Avenue. San Jose, CA 95138
Paper Size A

TITLE: FAB_RDK-1018_Diode
Part No. 61-00407-01
REV A
SHEET 1 OF 1

11.3.3 Assembly





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00407-00	Heat sink for Bridge	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1
3	75-00001-00	Machine screw #4-40 x .250	1
4	66-00096-00	THERMAL PAD-BER103, 0.009-THK-TO-220	1
5	15-01079-00	Diode	1
6	75-00154-00	WASHER SHOULDER, #4, .140 shoulder	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Iintegrations patents may be found at www.power.com

MATERIAL:
Heat sink stock

Drawn By: Hung D Nguyen
Date: 12 Nov 2025
Checked by: Loi

General Tolerances
.XX ± .01

Do not Scale Drawing

Power Integrations
5245 Hellyer Avenue.
San Jose, CA 95138

RDK 1018 Diode Heat Sink Assembly

PI Part NO. 61-00407-02
REV A
WEIGHT:
SHEET 1 OF 1

12 Performance Data

12.1 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line condition.

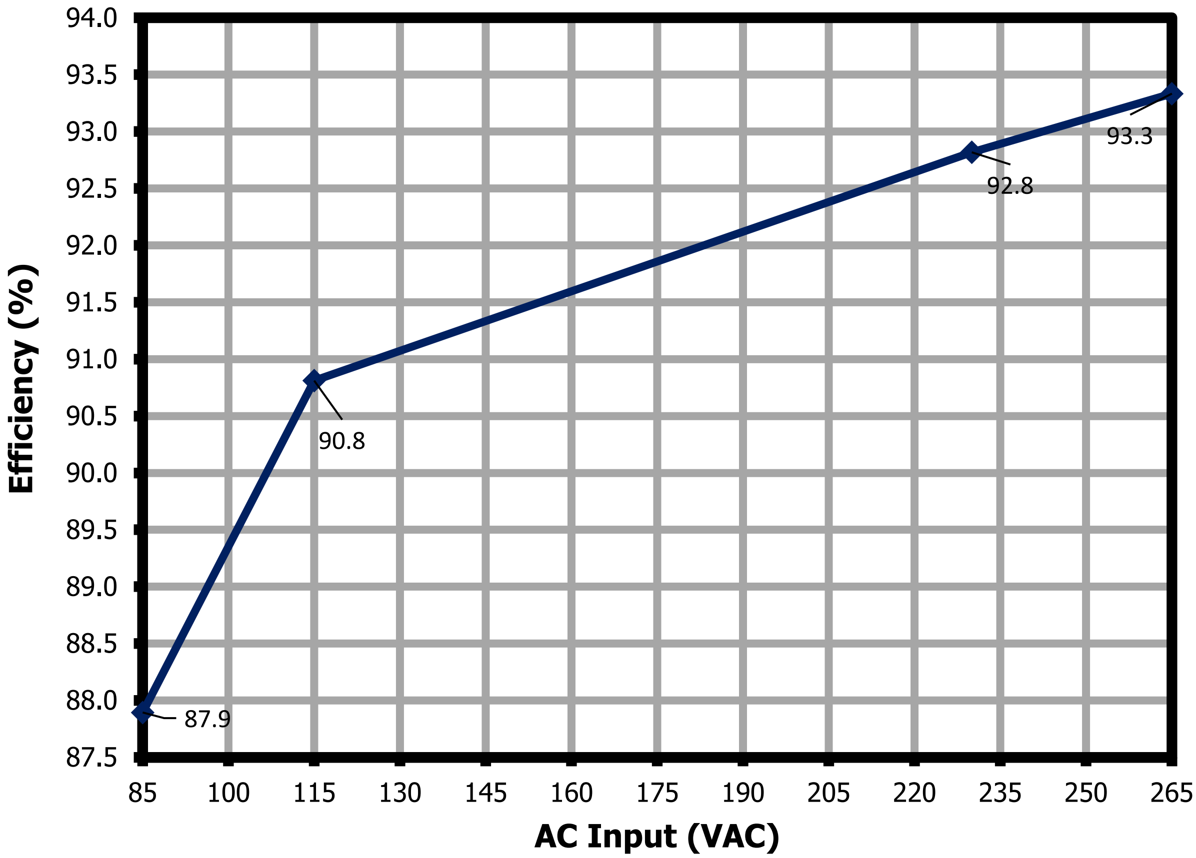


Figure 13 – Efficiency vs. Input Voltage.

VAC	Freq	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Efficiency
(RMS)	(Hz)	(W)	(V)	(A)	(W)	(%)
85	60	190	42	3.99	167	87.9
115	60	185	42	3.99	168	90.8
230	50	181	42	3.99	168	92.8
265	50	180	42	3.99	168	93.3

12.2 Efficiency vs. Load

Test Condition: Soak for 15 minutes at full load for each line voltage, and 10 seconds for each load point.

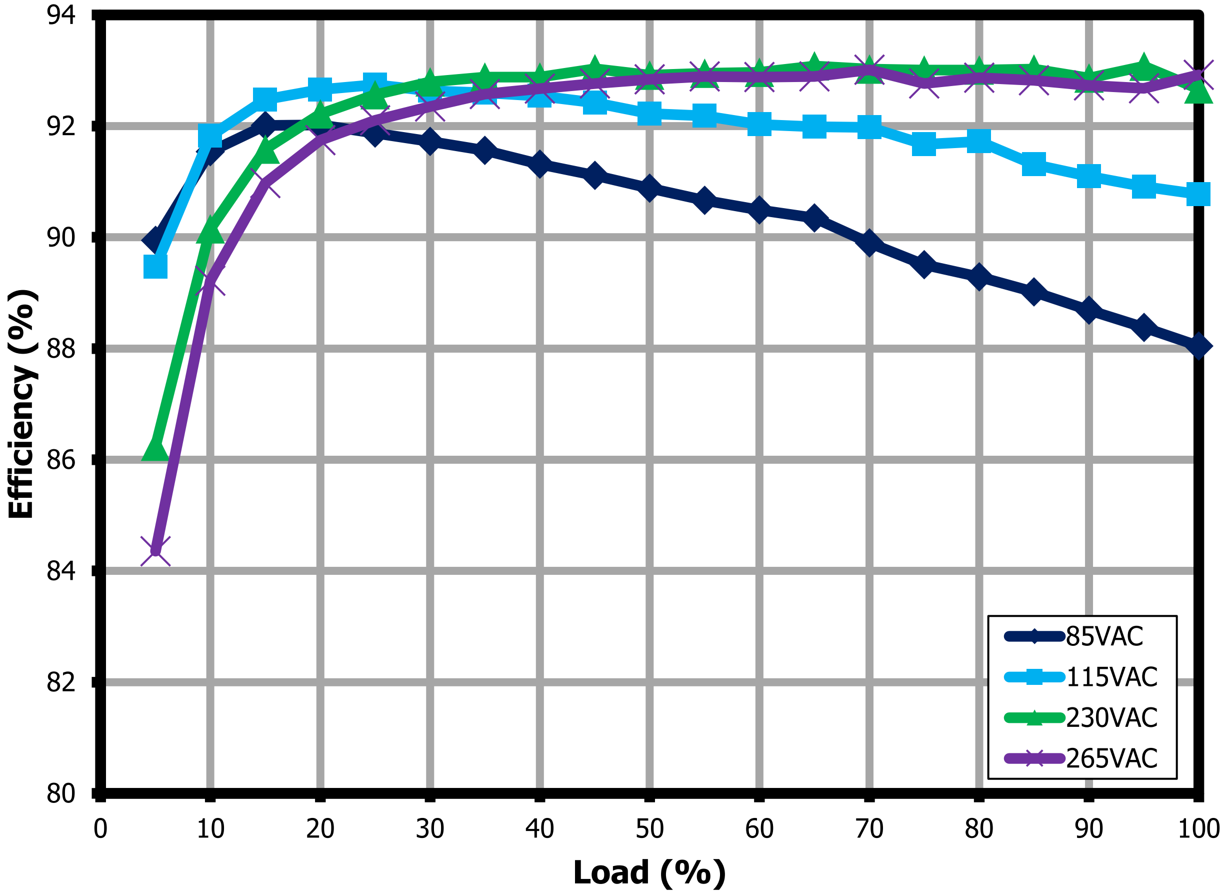


Figure 14 – Efficiency vs. Percentage Load.

12.2.1 Average and 10% Efficiency

12.2.1.1 Average Efficiency Standard

	Test	Average	Average	10% Load
Output Voltage (V)	Power (W)	DOE6 Limit (%)	CoC v5 Tier 2 (%)	CoC v5 Tier 2 (%)
42	168	88.0	89.0	79.0

12.2.1.2 Average and 10% Efficiency at 115 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	COC5T2 Limit
(A)	(W)	(V_{DC})	(A_{DC})	(W)	(%)	(%)	(%)
100%	185	42	3.99	168	90.8	**91.9**	89.0
75%	137	42	2.99	126	92.0		
50%	90.9	42	2.00	83.8	92.2		
25%	45.2	42	1.00	41.9	92.7		
10%	18.1	42	0.39	16.6	91.7	---	79.0

12.2.1.3 Average and 10% Efficiency at 230 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	COC5T2 Limit
(A)	(W)	(V_{DC})	(A_{DC})	(W)	(%)	(%)	(%)
100%	181	42	3.99	168	92.8	**92.9**	89.0
75%	135	42	2.99	126	93.3		
50%	90.1	42	2.00	83.8	93.0		
25%	45.2	42	1.00	41.8	92.5		
10%	18.4	42	0.39	16.6	90.2	---	79.0

12.2.2 No-Load Input Power

Test Condition: Soak for 15 minutes for each line voltage point with 5-minute integration time.

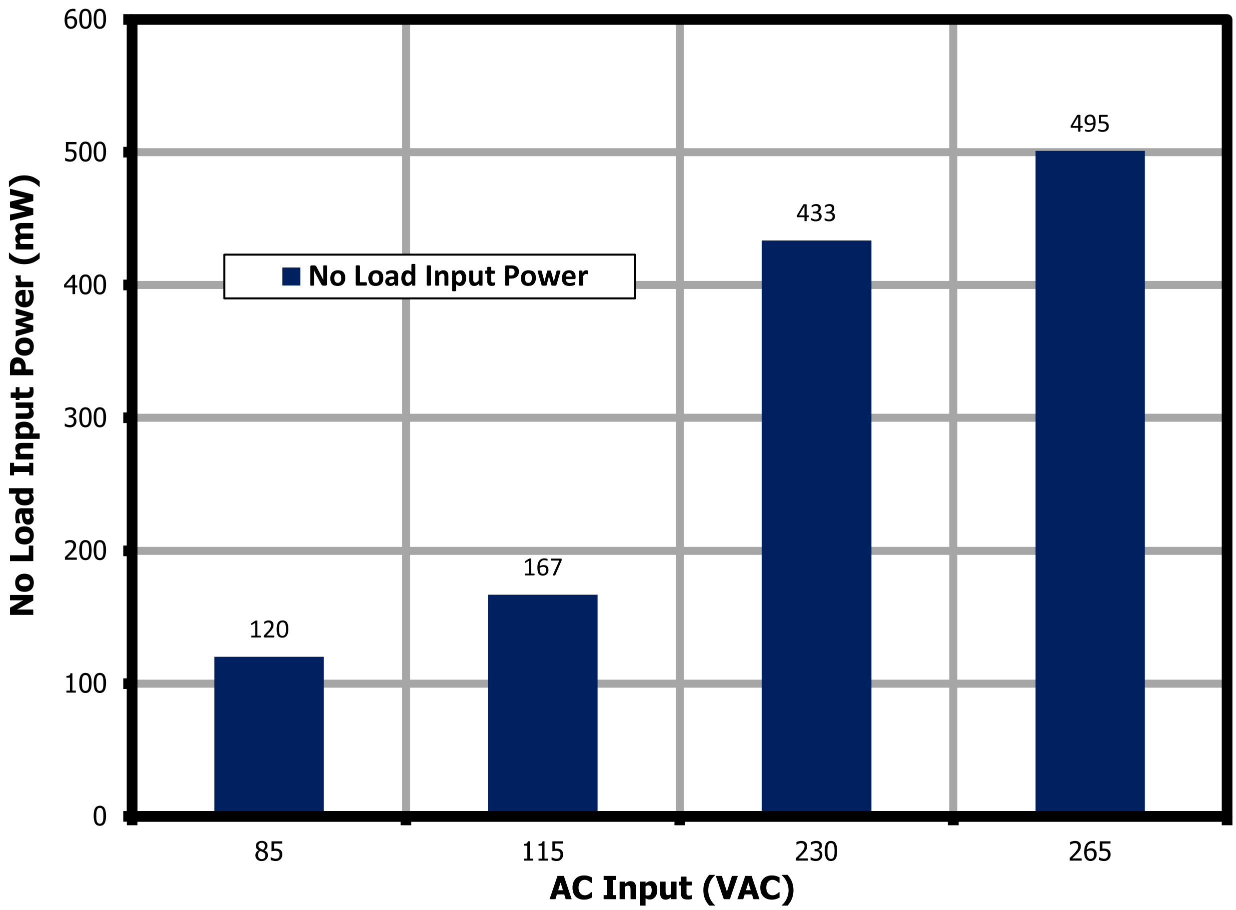


Figure 15 – No-Load Input Power vs. Line at Room Temperature.

12.2.3 Line Regulation

Test Condition: Soak for 15 minutes for each line voltage point.

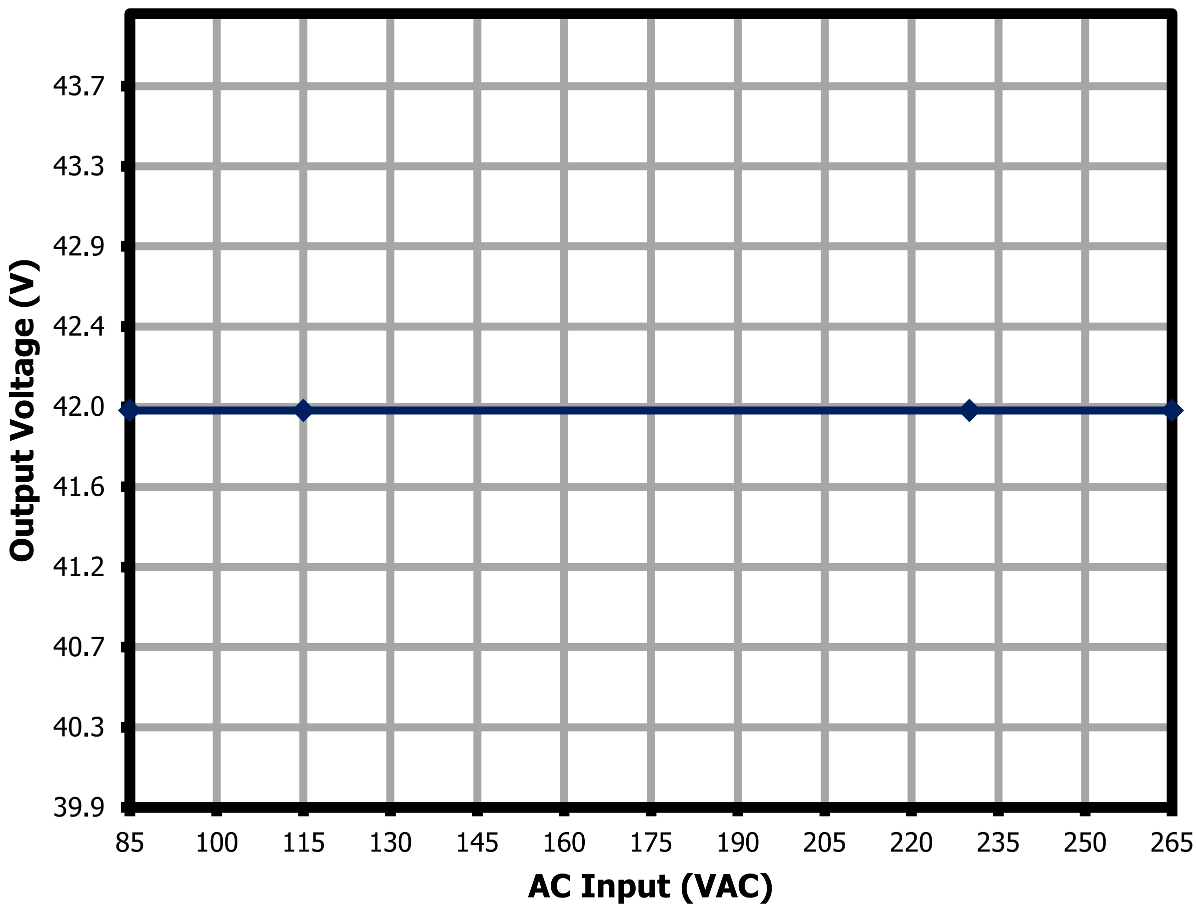


Figure 16 – Output Voltage vs. Line Voltage.

12.2.4 Load Regulation

Test Condition: Soak for 15 minutes each line voltage point at full load, and 10 seconds for each load.

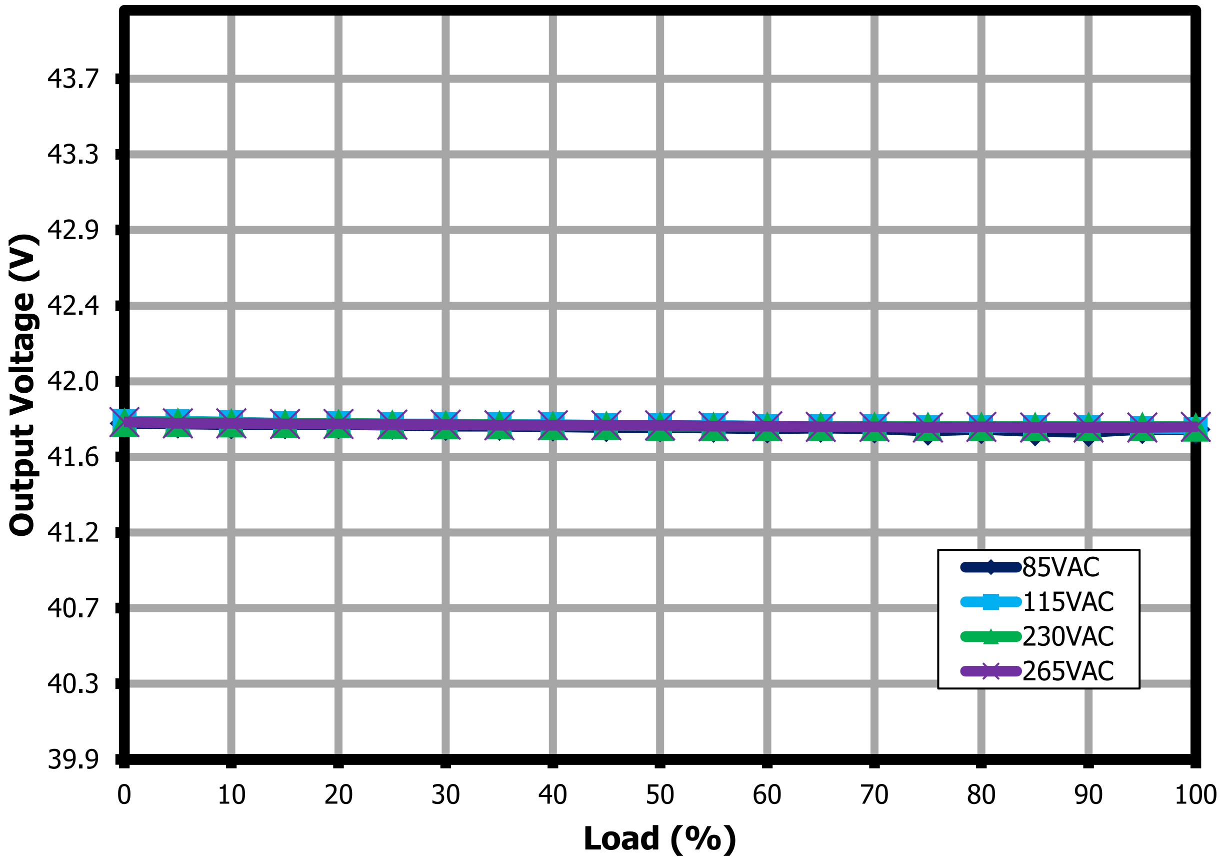


Figure 17 – Output Voltage vs. Percent Load.

13 Waveforms

13.1 Load Transient Response

Test Condition: Dynamic load frequency = 10 Hz, Duty cycle = 50%
Slew Rate = 0.4 A / μs

13.1.1 0% to 100% Output Load Transient Condition

Figure 18 – 85 VAC, 60 Hz. Io = 0 – 4 A (0-100%) load step.
CH1: V_{OUT}, 500 mV / div., 5 ms / div.
CH2: I_{OUT}, 2 A / div., 5 ms / div.
Output Voltage, max = 42.0 V
Output Voltage, min = 41.3 V

Figure 19 – 115 VAC, 60 Hz. Io = 0 – 4 A (0-100%) load step.
CH1: V_{OUT}, 500 mV / div., 5 ms / div.
CH2: I_{OUT}, 2 A / div., 5 ms / div.
Output Voltage, max = 41.9 V
Output Voltage, min = 41.3 V

Figure 20 – 230 VAC, 50 Hz. Io = 0 – 4 A (0-100%) load step.
CH1: V_{OUT}, 500 mV / div., 5 ms / div.
CH2: I_{OUT}, 2 A / div., 5 ms / div.
Output Voltage, max = 41.9 V
Output Voltage, min = 41.3 V

Figure 21 – 265 VAC, 50 Hz. Io = 0 – 4 A (0-100%) load step.
CH1: V_{OUT}, 500 mV / div., 5 ms / div.
CH2: I_{OUT}, 2 A / div., 5 ms / div.
Output Voltage, max = 41.9 V
Output Voltage, min = 41.3 V

13.2 Output Start-up

13.2.1 Full Load CC Mode

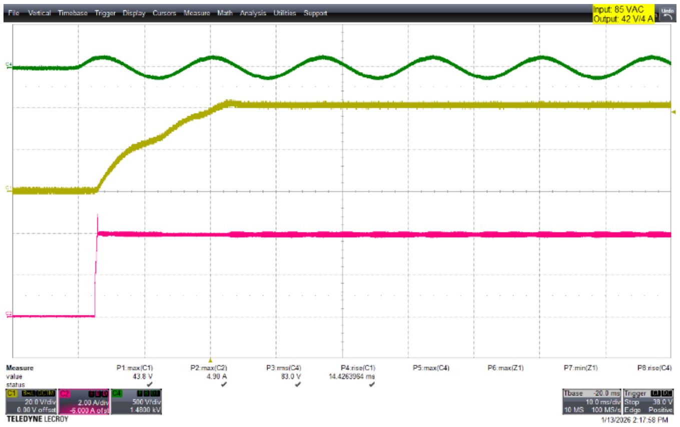


Figure 22 – 85 VAC, 60 Hz. 42 V / 4 A.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 14.4 ms

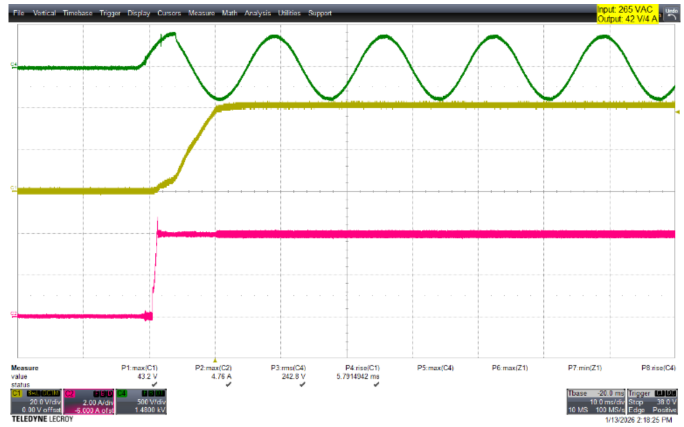


Figure 23 – 265 VAC, 50 Hz. 42 V / 4 A.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 5.79 ms

13.2.2 Full Load CR Mode

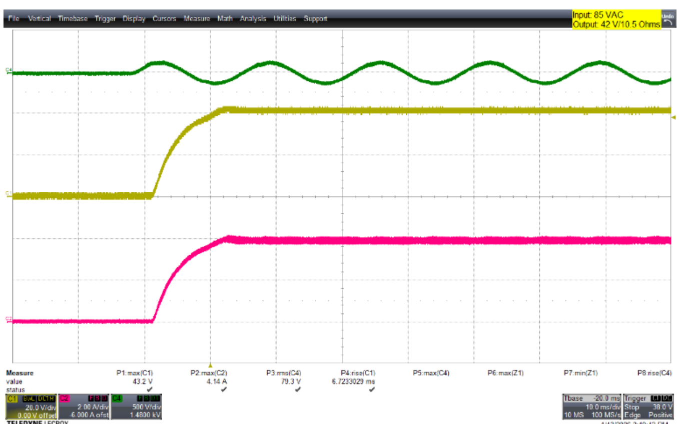


Figure 24 – 85 VAC, 60 Hz. 42 V / 10.5 Ω.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 6.72 ms

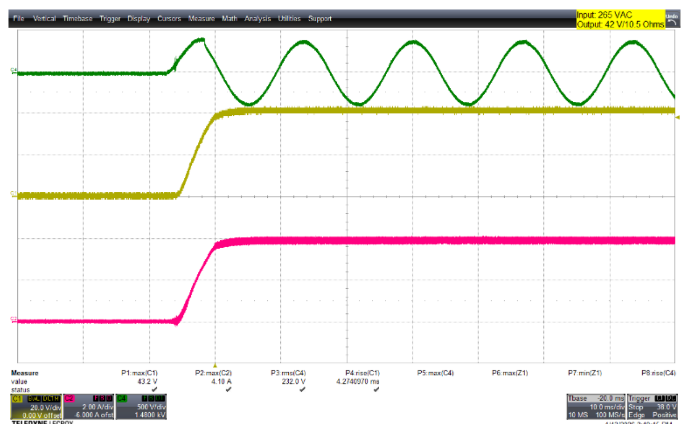


Figure 25 – 265 VAC, 50 Hz. 42 V / 10.5 Ω.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 4.27 ms

13.2.3 No Load

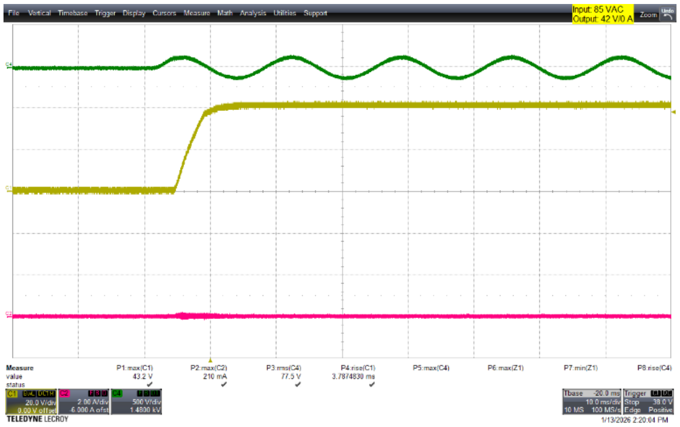


Figure 26 – 85 VAC, 60 Hz. 42 V / 0 A.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 3.79 ms

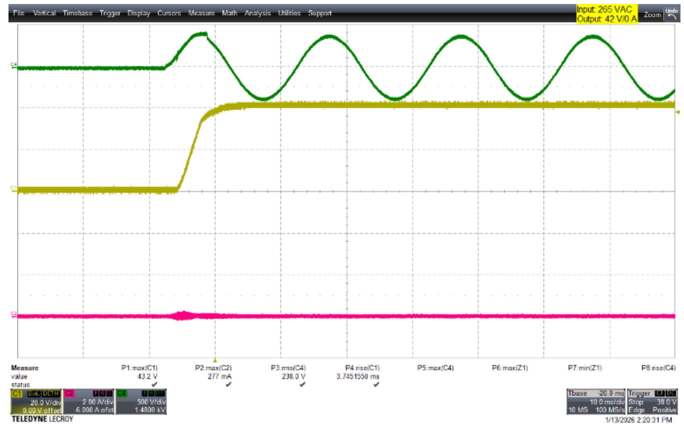


Figure 27 – 265 VAC, 50 Hz. 42 V / 0 A.
CH1: V_{OUT}, 20 V / div., 10 ms / div.
CH2: I_{OUT}, 1 A / div., 10 ms / div.
CH4: AC INPUT, 500 V / div., 10 ms / div.
Output Voltage Rise time = 3.75 ms

13.3 Switching Waveforms

13.3.1 Primary Drain Voltage and Current at Normal Operation

13.3.1.1 Full Load

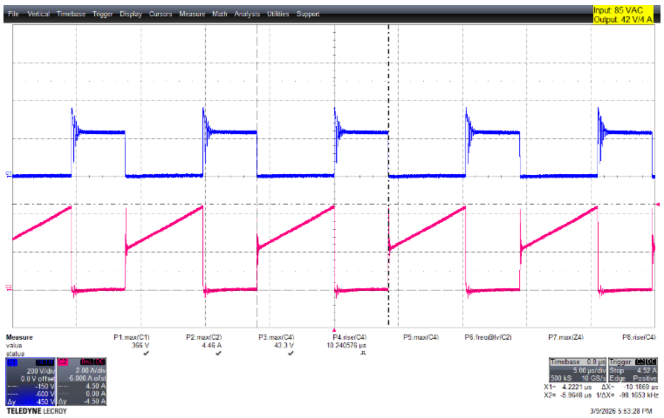


Figure 28 – 85 VAC, Io = 4 A (Full-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 5 µs / div.
TOP7075E Drain voltage, max = 366 V
TOP7075E Drain current, max = 4.46 A
ILIM = 4.5 A, F_{SW}= 98.2 kHz

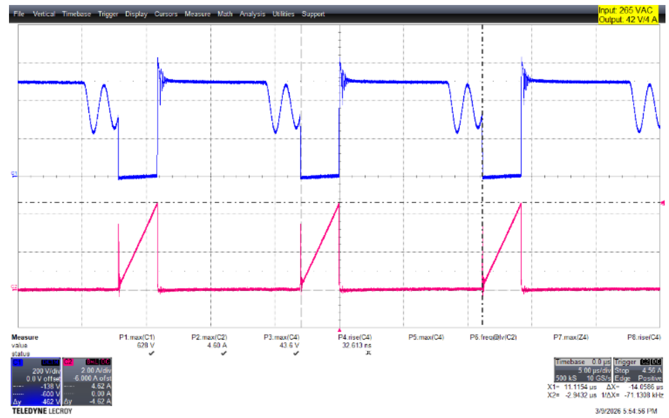


Figure 29 – 265 VAC, Io = 4 A (Full-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 5 µs / div.
TOP7075E Drain voltage, max = 628 V
TOP7075E Drain current, max = 4.6 A
ILIM = 4.6 A, F_{SW}= 71.1 kHz

13.3.1.2 No Load

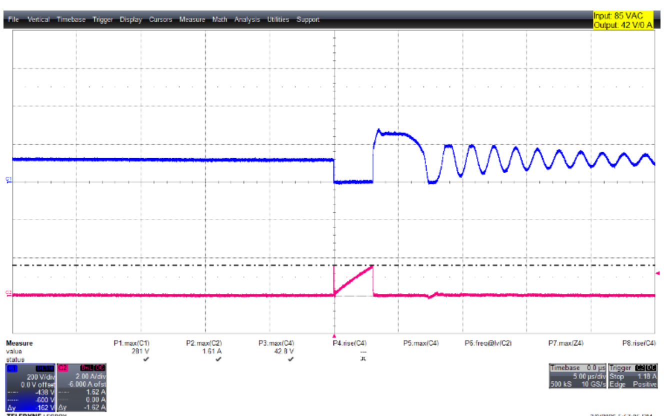


Figure 30 – 85 VAC, Io = 0 A (No-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 5 µs / div.
TOP7075E Drain voltage, max = 281 V
TOP7075E Drain current, max = 1.61 A
ILIM = 1.61 A

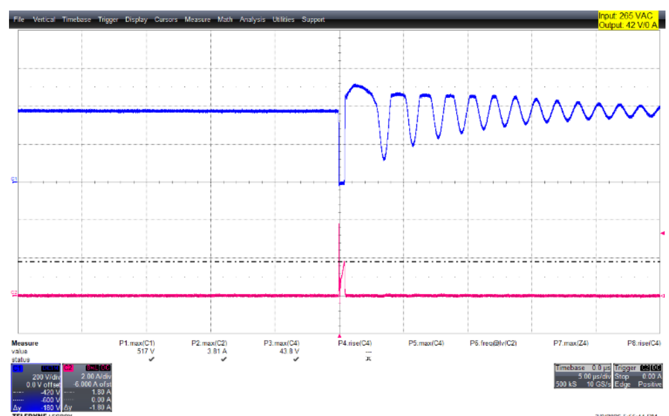


Figure 31 – 265 VAC, Io = 0 A (No-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 5 µs / div.
TOP7075E Drain voltage, max = 517 V
TOP7075E Drain current, max = 3.81 A
ILIM = 1.8 A

13.3.2 Primary Drain Voltage and Current at Start-up Operation

13.3.2.1 Full Load

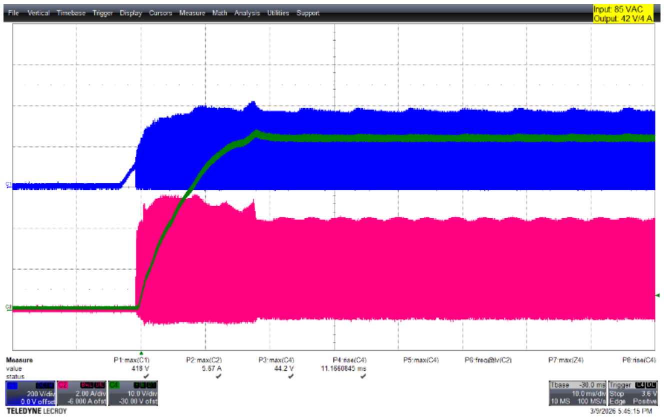


Figure 32 – 85 VAC, Io = 4 A (Full-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 10 V / div., 10 ms / div.
TOP7075E Drain voltage, max = 418 V
TOP7075E Drain current, max = 5.67 A

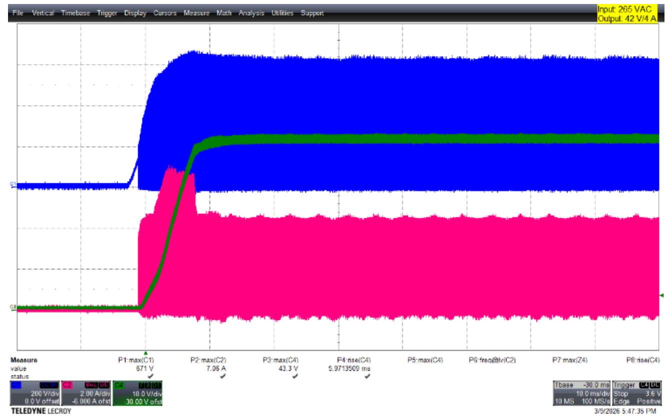


Figure 33 – 265 VAC, Io = 4 A (Full-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 10 V / div., 10 ms / div.
TOP7075E Drain voltage, max = 671 V
TOP7075E Drain current, max = 7.06 A

13.3.2.2 No Load

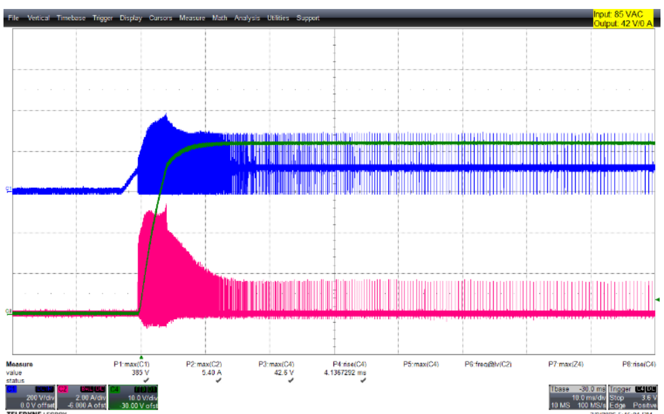


Figure 34 – 85 VAC, Io = 0 A (No-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 10 V / div., 10 ms / div.
TOP7075E Drain voltage, max = 385 V
TOP7075E Drain current, max = 5.4 A

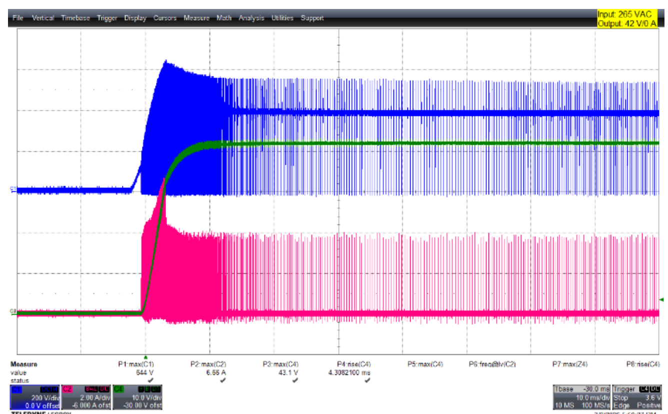


Figure 35 – 265 VAC, Io = 0 A (No-Load).
CH1: TOP7075E_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7075E_I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 10 V / div., 10 ms / div.
TOP7075E Drain voltage, max = 644 V
TOP7075E Drain current, max = 6.66 A

13.3.3 Freewheeling Diode Voltage at Normal Operation

13.3.3.1 Full Load

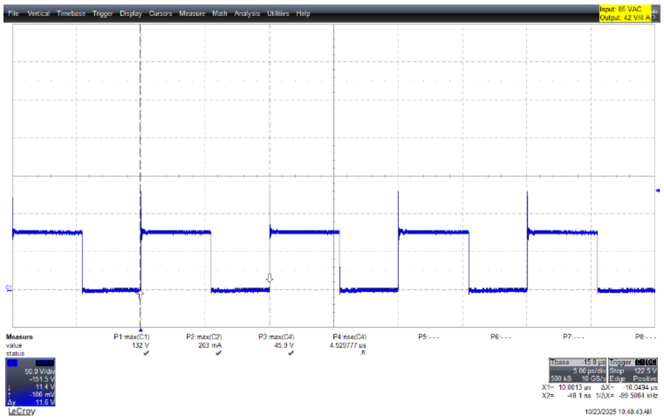


Figure 36 – 85 VAC, Io = 4 A (Full-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 5 µs / div.
OUTPUT RECTIFIER VOLTAGE, max = 132 V

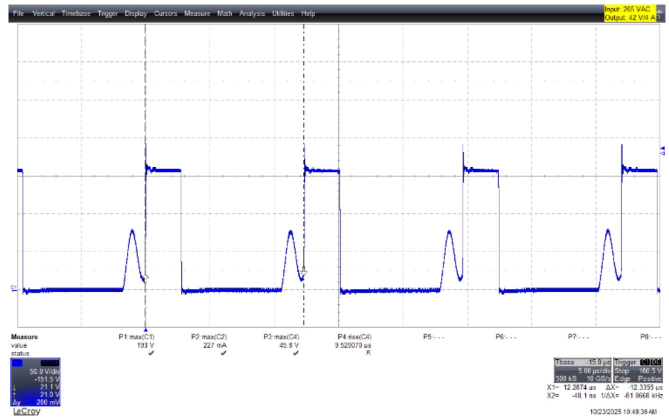


Figure 37 – 265 VAC, Io = 4 A (Full-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 5 µs / div.
OUTPUT RECTIFIER VOLTAGE, max = 193 V

13.3.3.2 No Load

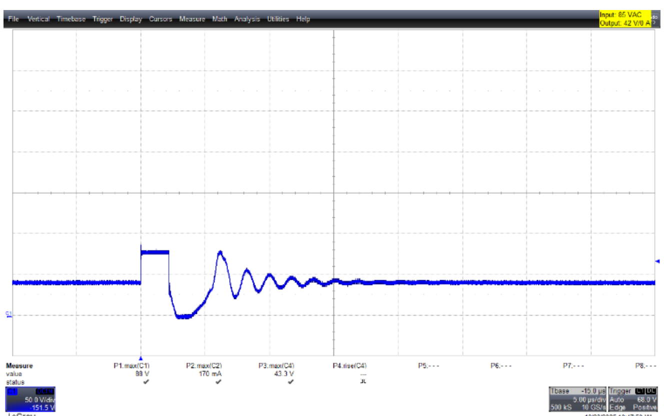


Figure 38 – 85 VAC, Io = 0 A (No-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 5 µs / div.
OUTPUT RECTIFIER VOLTAGE, max = 88 V

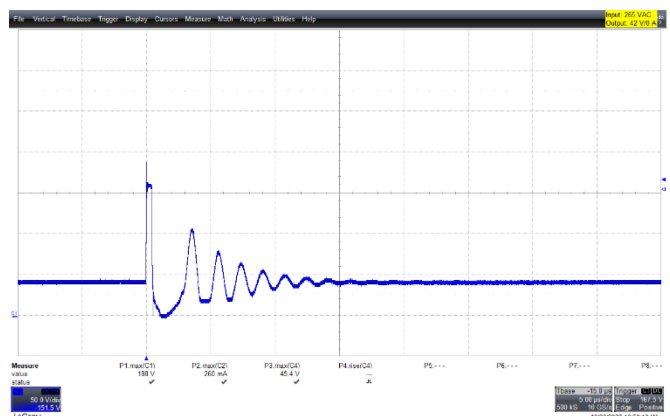


Figure 39 – 265 VAC, Io = 0 A (No-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 5 µs / div.
OUTPUT RECTIFIER VOLTAGE, max = 188 V

13.3.4 Freewheeling Diode Voltage at Start-Up

13.3.4.1 Full Load

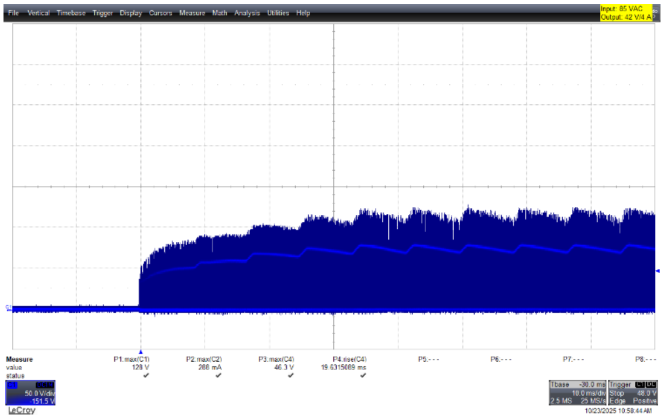


Figure 40 – 85 VAC, Io = 4 A (Full-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 10 ms / div.
OUTPUT RECTIFIER VOLTAGE, max = 128 V

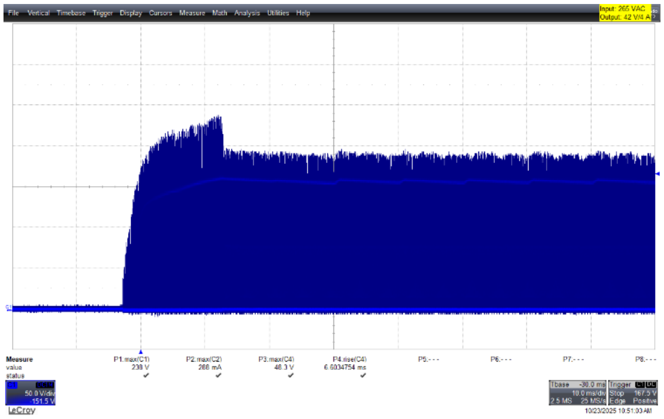


Figure 41 – 265 VAC, Io = 4 A (Full-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 10 ms / div.
OUTPUT RECTIFIER VOLTAGE, max = 238 V

13.3.4.2 No Load

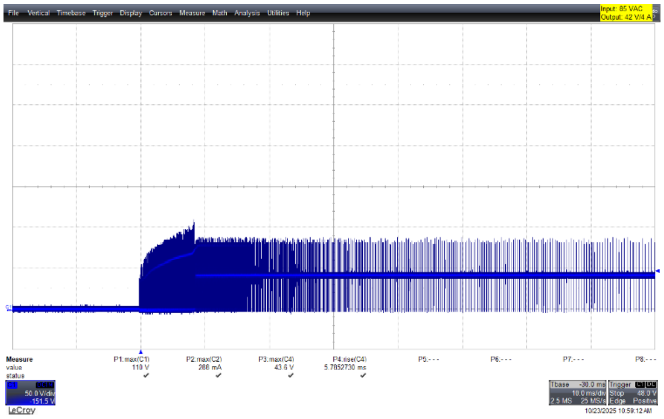


Figure 42 – 85 VAC, Io = 0 A (No-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 10 ms / div.
OUTPUT DIODE voltage, max = 110 V

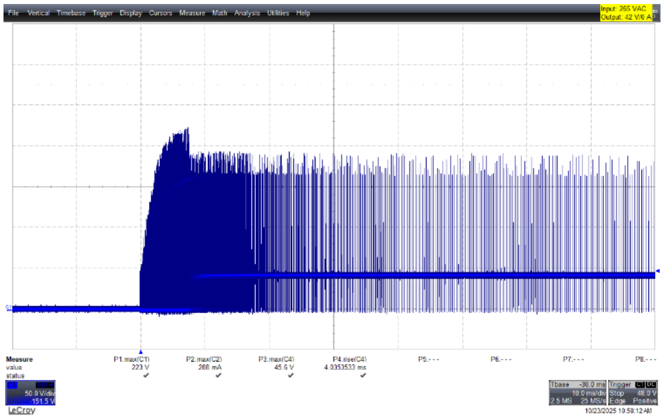


Figure 43 – 265 VAC, Io = 0 A (No-Load).
CH1: OUTPUT RECTIFIER VOLTAGE: 200 V / div., 10 ms / div.
OUTPUT DIODE voltage, max = 223 V

13.4 Output Voltage Ripple

13.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in figures 46 and 47.

The 4987BA probe adapter is affixed with two capacitors connected in parallel across the probe tip. The capacitors include one 0.1 μF / 100 V ceramic type and one 47 μF / 63 V aluminum electrolytic. The aluminum electrolytic capacitor is polarized, so proper polarity across DC outputs must be maintained during measurements.

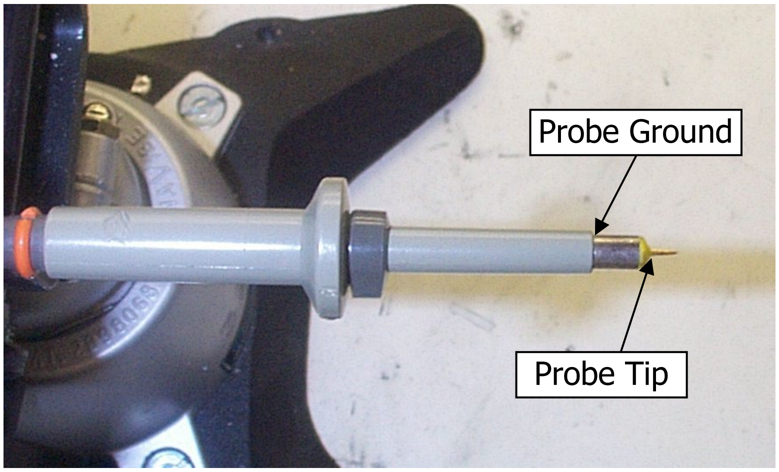


Figure 44 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

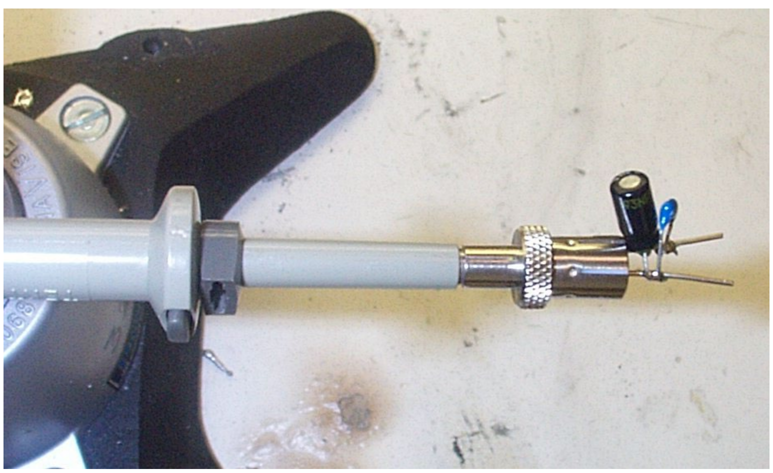


Figure 45 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

13.4.2 Measurement Results

Note: All ripple measurements were taken at PCB end.

13.4.2.1 100% Load Condition

85 VAC – 42 V/4 A

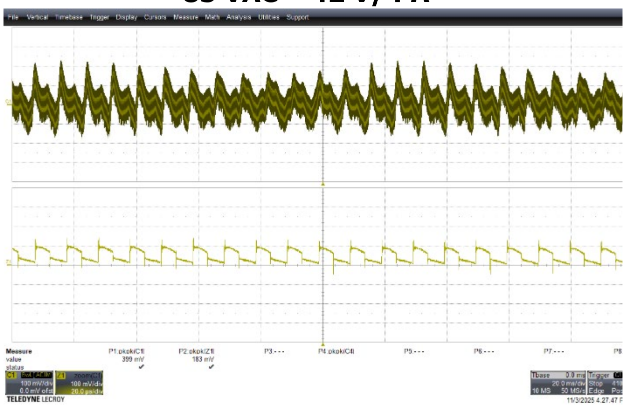


Figure 46 – 85 VAC, 60 Hz. 42 V / 4 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 μs / div.
V_{OUT} Ripple = 399 mV_{PK-PK}

115 VAC – 42 V/4 A

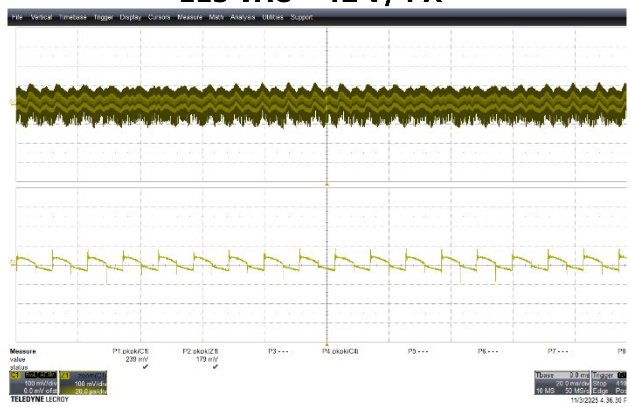


Figure 47 – 115 VAC, 60 Hz. 42 V / 4 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 μs / div.
V_{OUT} Ripple = 239 mV_{PK-PK}

230 VAC – 42 V/4 A

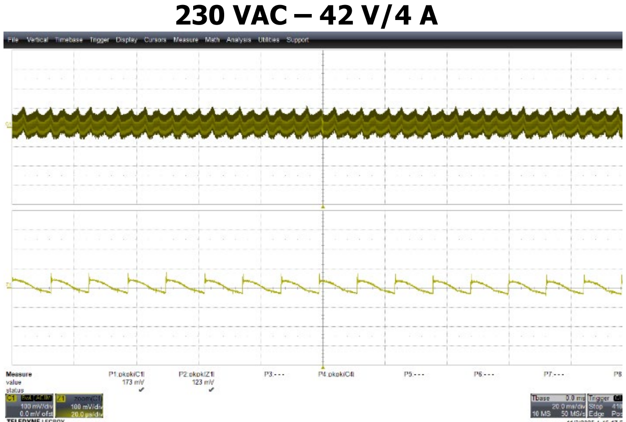


Figure 48 – 230 VAC, 50 Hz. 42 V / 4 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 μs / div.
V_{OUT} Ripple = 173 mV_{PK-PK}

265 VAC – 42 V/4 A

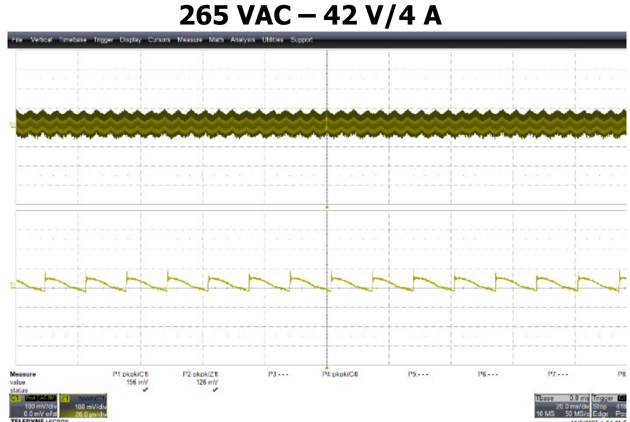


Figure 49 – 265 VAC, 50 Hz. 42 V / 4 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 μs / div.
V_{OUT} Ripple = 156 mV_{PK-PK}

13.4.2.2 75% Load Condition

85 VAC – 42 V/3 A

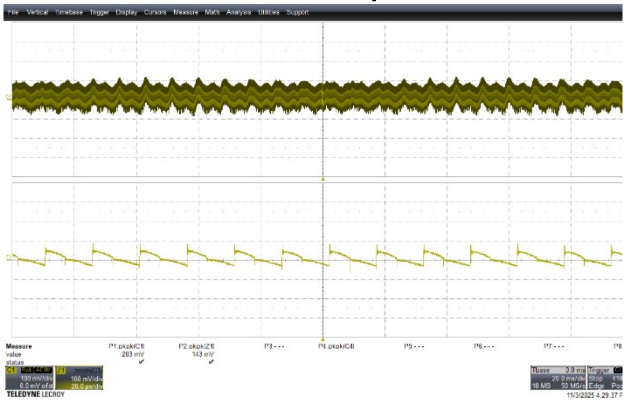


Figure 50 – 85 VAC, 60 Hz. 42 V / 3 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 203 mV_{PK-PK}

115 VAC – 42 V/3 A

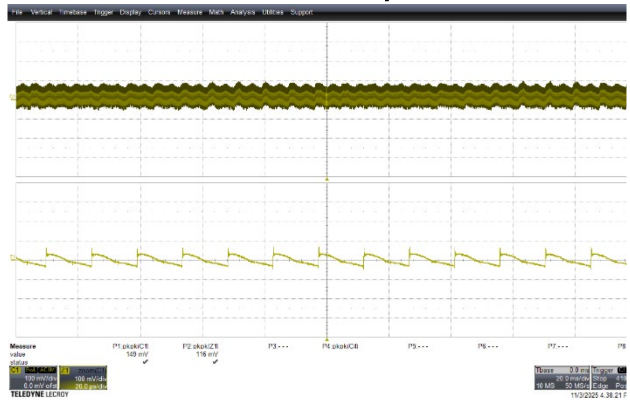


Figure 51 – 115 VAC, 60 Hz. 42 V / 3 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 149 mV_{PK-PK}

230 VAC – 42 V/3 A

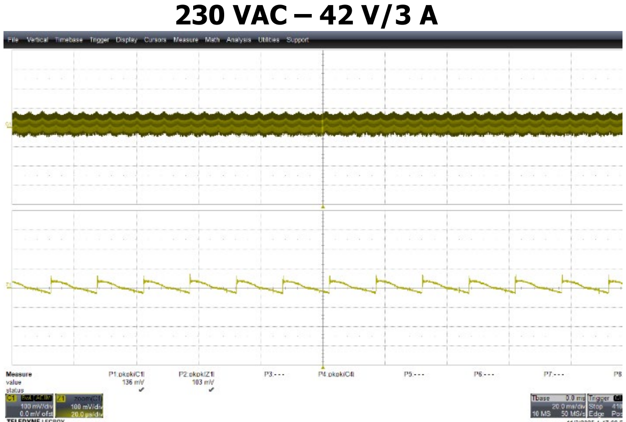


Figure 52 – 230 VAC, 50 Hz. 42 V / 3 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 136 mV_{PK-PK}

265 VAC – 42 V/3 A

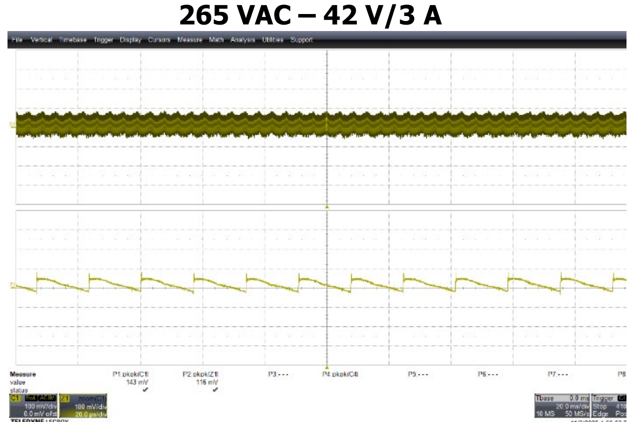


Figure 53 – 265 VAC, 50 Hz. 42 V / 3 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 143 mV_{PK-PK}

13.4.2.3 50% Load Condition

85 VAC – 42 V/2 A

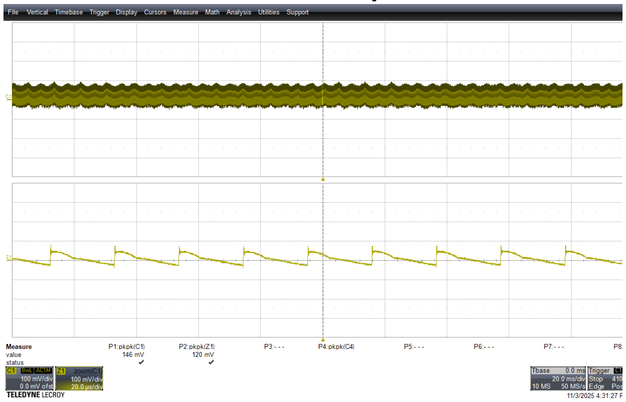


Figure 54 – 85 VAC, 60 Hz. 42 V / 2 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 146 mV_{PK-PK}

115 VAC – 42 V/2 A

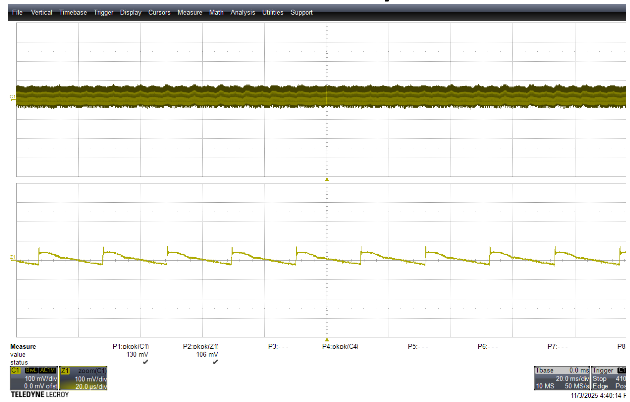


Figure 55 – 115 VAC, 60 Hz. 42 V / 2 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 130 mV_{PK-PK}

230 VAC – 42 V/2 A

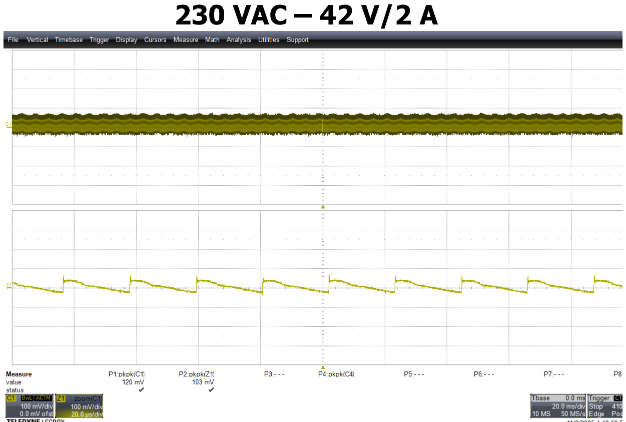


Figure 56 – 230 VAC, 50 Hz. 42 V / 2 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 120 mV_{PK-PK}

265 VAC – 42 V/2 A

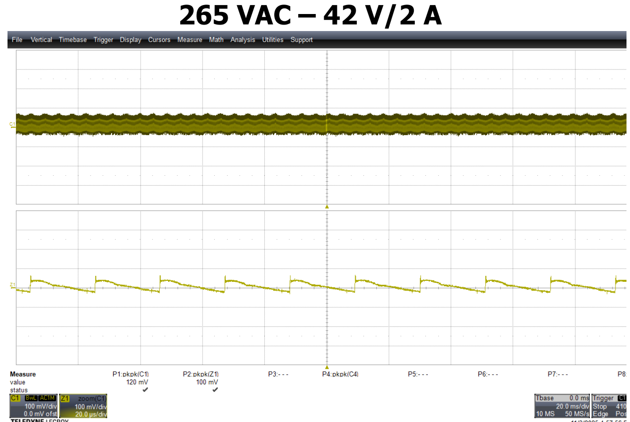


Figure 57 – 265 VAC, 50 Hz. 42 V / 2 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 120 mV_{PK-PK}

13.4.2.4 25% Load Condition

85 VAC – 42 V/1 A

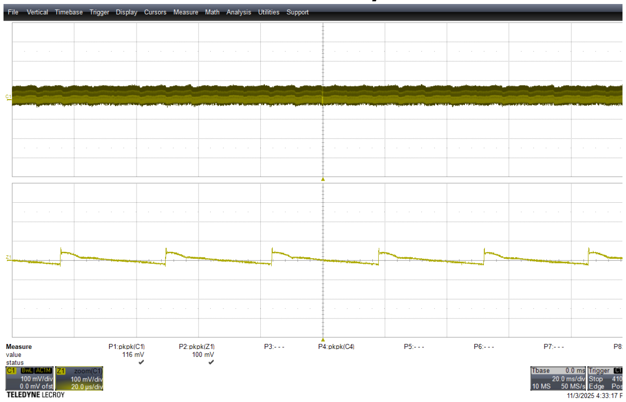


Figure 58 – 85 VAC, 60 Hz. 42 V / 1 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 116 mV_{PK-PK}

115 VAC – 42 V/1 A

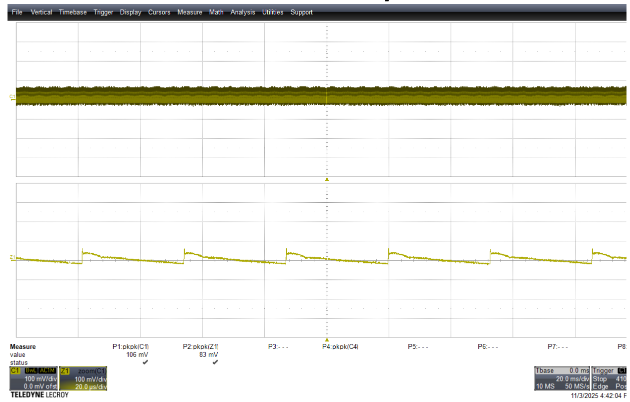


Figure 59 – 115 VAC, 60 Hz. 42 V / 1 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 106 mV_{PK-PK}

230 VAC – 42 V/1 A

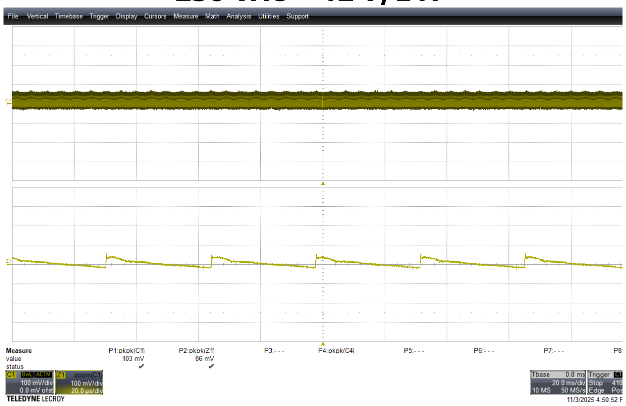


Figure 60 – 230 VAC, 50 Hz. 42 V / 1 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 103 mV_{PK-PK}

265 VAC – 42 V/1 A

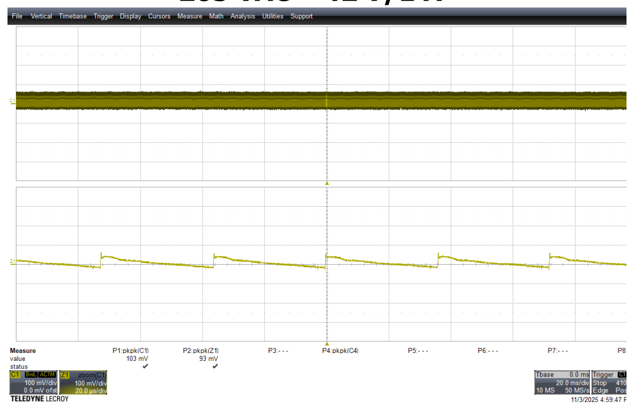


Figure 61 – 265 VAC, 50 Hz. 42 V / 1 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 103 mV_{PK-PK}

13.4.2.5 0% Load Condition

85 VAC – 42 V/0 A

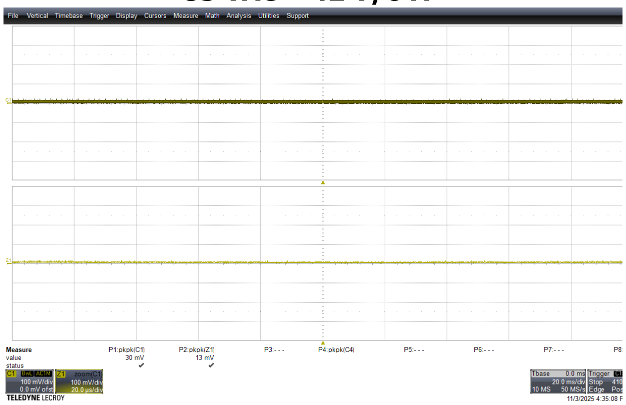


Figure 62 – 85 VAC, 60 Hz. 42 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 30 mV_{PK-PK}

115 VAC – 42 V/0 A

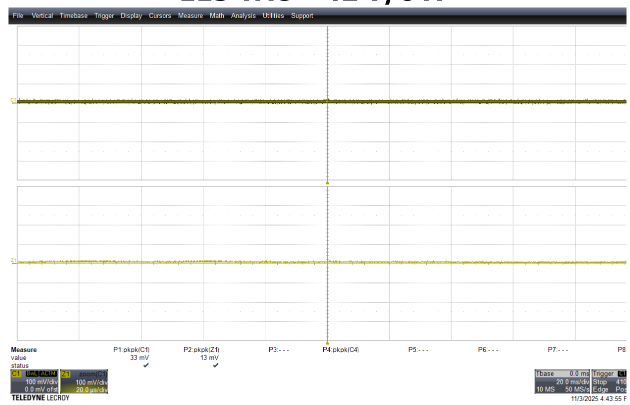


Figure 63 – 115 VAC, 60 Hz. 42 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 33 mV_{PK-PK}

230 VAC – 42 V/0 A

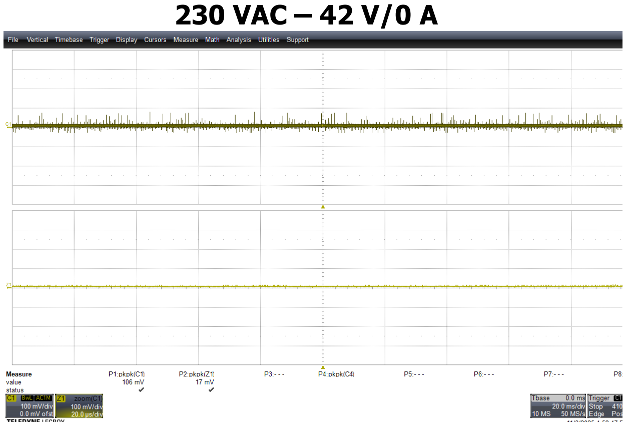


Figure 64 – 230 VAC, 50 Hz. 42 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 106 mV_{PK-PK}

265 VAC – 42 V/0 A

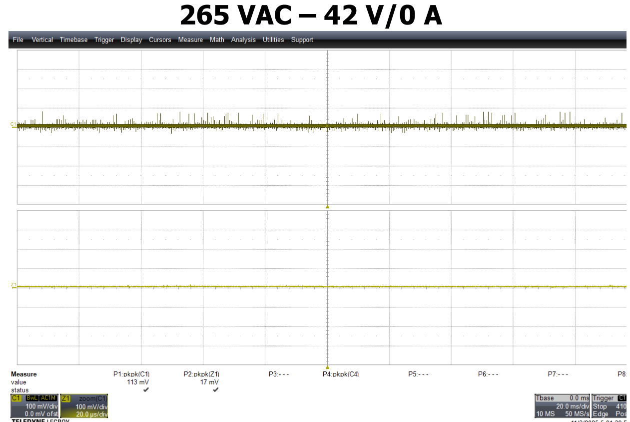


Figure 65 – 265 VAC, 50 Hz. 42 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 100 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 113 mV_{PK-PK}

13.4.3 Output Ripple Voltage Graph

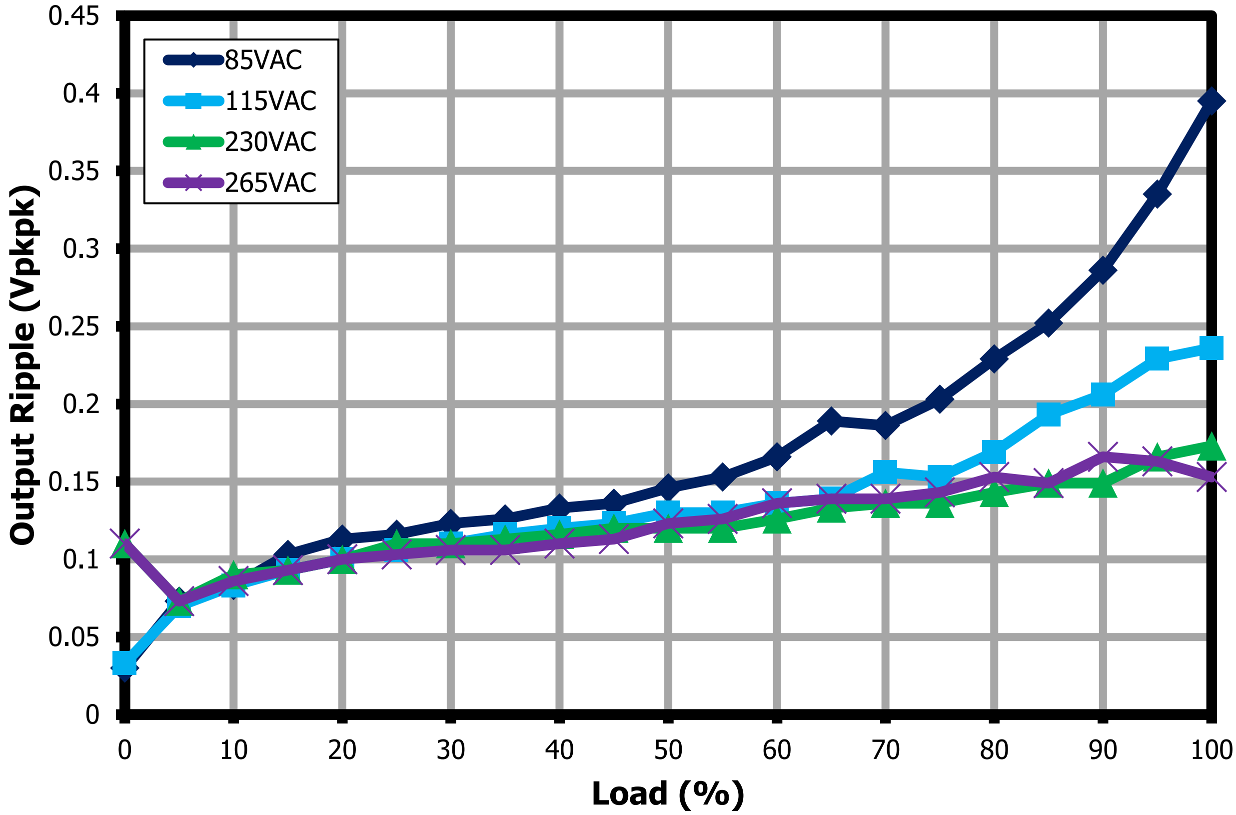


Figure 66 – Voltage Ripple (Measured at PCB End and at Room Temperature).

13.5 Brown In & Brown Out

Brown in and brown out slew rate set at 0.1 V/s.

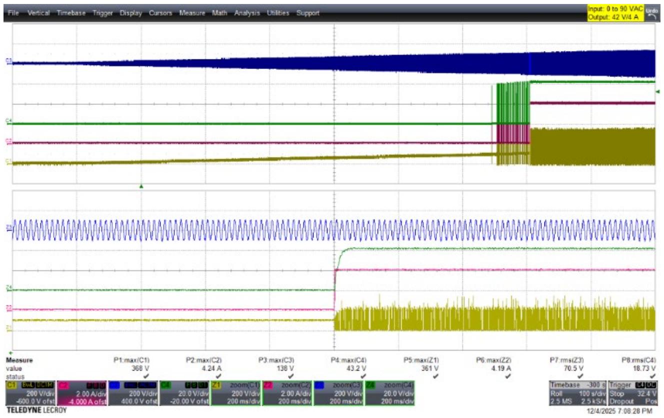


Figure 67 – Brown In, Full Load Condition – 0 to 90 VAC.
CH1: TOP7075E_V_{DS}, 200 V / div., 100 s / div.
CH2: I_{OUT}, 2 A / div., 100 s / div.
CH3: AC INPUT, 200 V / div., 100 s / div.
CH3: V_{OUT}, 20 V / div., 100 s / div.
Zoom: 200 ms/div.
Brown In Voltage = 70.5 VAC

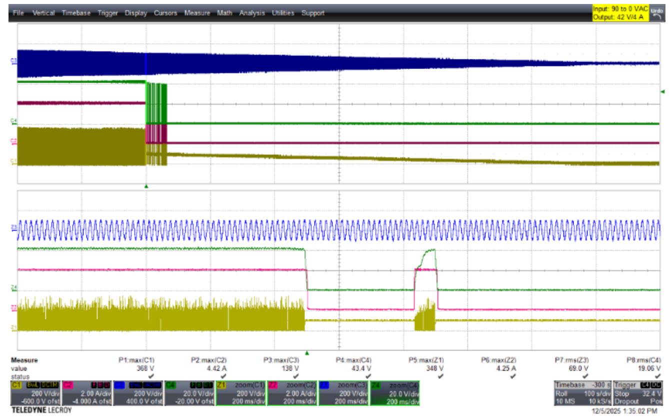


Figure 68 – Brown Out, Full Load Condition – 90 to 0 VAC.
CH1: TOP7075E_V_{DS}, 200 V / div., 100 s / div.
CH2: I_{OUT}, 2 A / div., 100 s / div.
CH3: AC INPUT, 200 V / div., 100 s / div.
CH3: V_{OUT}, 20 V / div., 100 s / div.
Zoom: 200 ms/div.
Brown Out Voltage = 69 VAC

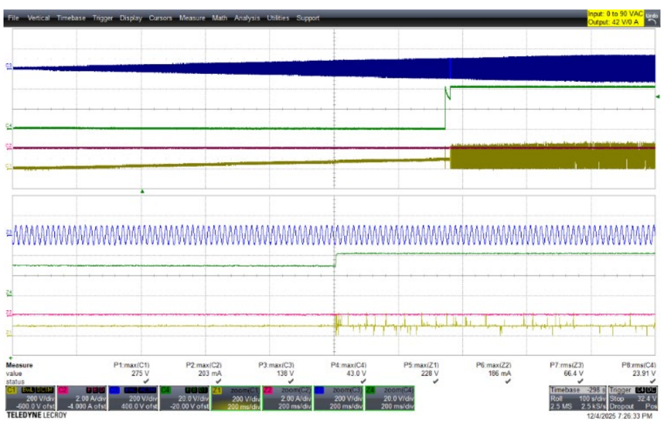


Figure 69 – Brown In, No Load Condition – 0 to 90 VAC.
CH1: TOP7075E_V_{DS}, 200 V / div., 100 s / div.
CH2: I_{OUT}, 2 A / div., 100 s / div.
CH3: AC INPUT, 200 V / div., 100 s / div.
CH3: V_{OUT}, 20 V / div., 100 s / div.
Zoom: 200 ms/div.
Brown In Voltage = 66.4 VAC

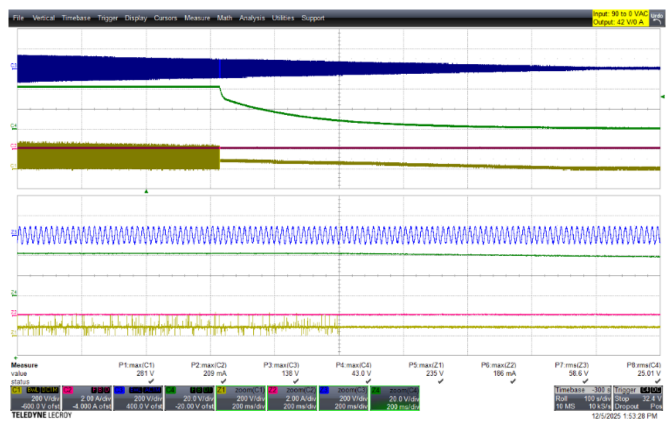


Figure 70 – Brown Out, No Load Condition – 90 to 0 VAC.
CH1: TOP7075E_V_{DS}, 200 V / div., 100 s / div.
CH2: I_{OUT}, 2 A / div., 100 s / div.
CH3: AC INPUT, 200 V / div., 100 s / div.
CH3: V_{OUT}, 20 V / div., 100 s / div.
Zoom: 200 ms/div.
Brown In Voltage = 58.6 VAC

14 Thermal Performance

14.1 Thermal Performance at Room Temperature

14.1.1 85 VAC Full Load at Room Ambient

Test result after 2 hours running continuously inside an enclosure at 85 VAC full load using FLIR thermal camera to measure component temperatures.

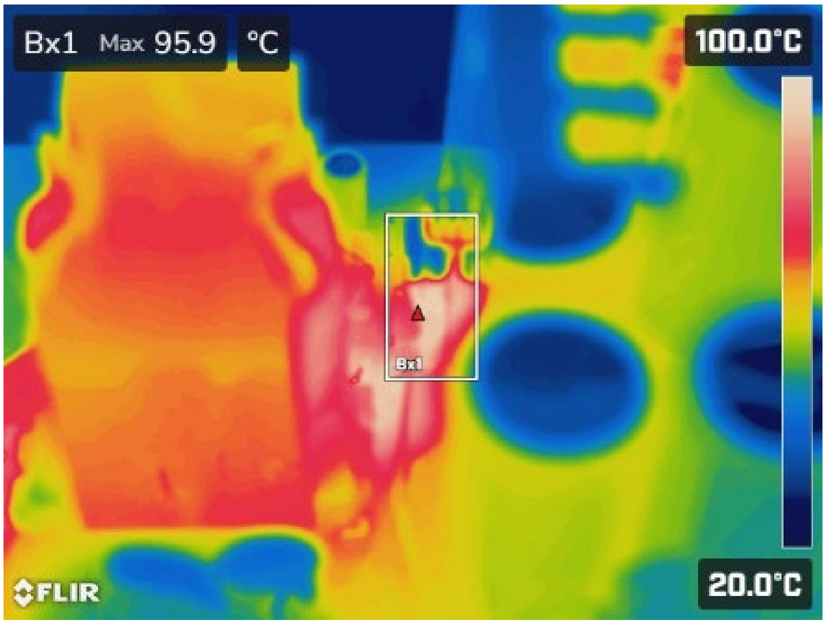


Figure 71 – 85 VAC 60 Hz. Thermals – TOP7075E (U2).

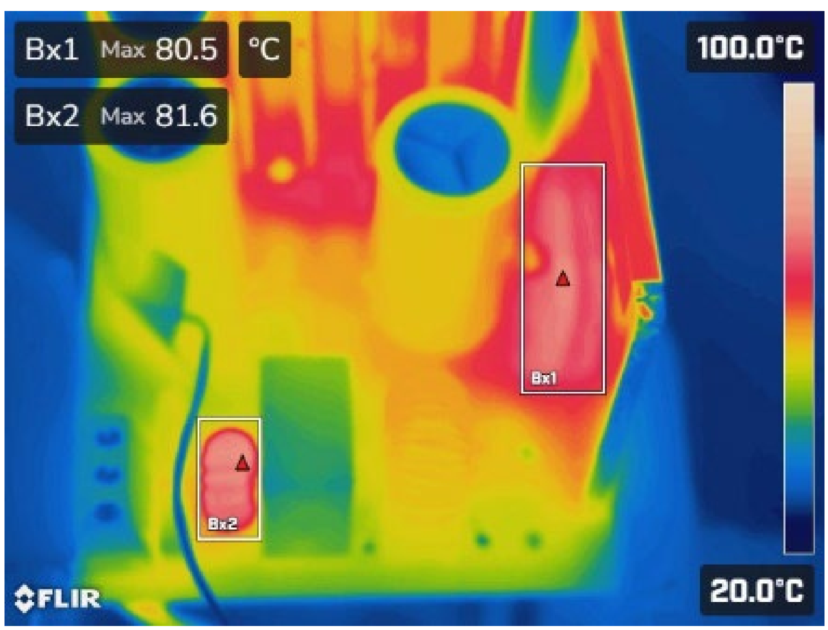


Figure 72 – 85 VAC 60 Hz. Thermals – Input Filter Side.

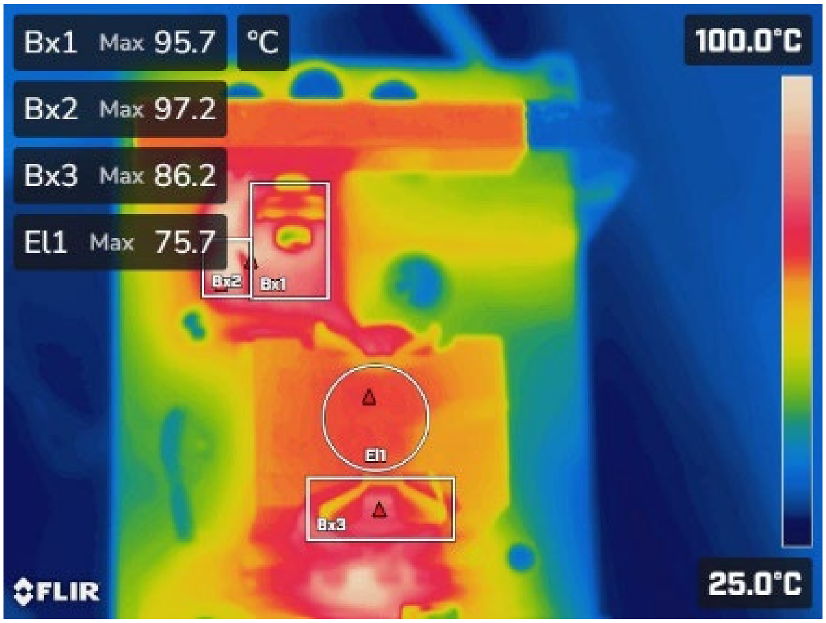


Figure 73 – 85 VAC 60 Hz. Thermals – Top Side.

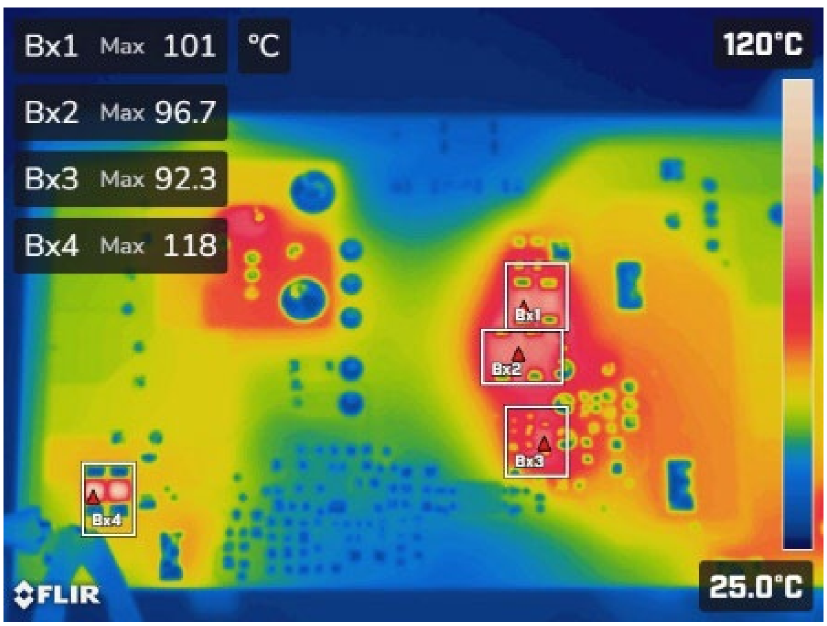


Figure 74 – 85 VAC 60 Hz. Thermals – Bottom Side.

Component		Actual Temperature	Projected temperature at maximum 40 °C Ambient (°C)
	Ambient	37.4	40
U2	TOP7075E	95.9	98.5
D2 & D3	Primary Snubber Diode	96.7	99.3
R7 & R8	Primary Snubber Resistor	101	104
D4	Primary Bias Diode	92.3	94.9
L2	CMC 1	81.6	84.2
BR1	Bridge Rectifier	80.5	83.1
T1	Transformer Core	75.7	78.3
T1	Transformer Winding	86.2	88.8
D6	Output Rectifier	95.7	98.3
R14	Secondary Snubber Resistor	97.2	99.8
R24 & R25	R_{SENSE}	118	121

14.1.2 265 VAC Full Load at Room Ambient

Test result after 2 hours running continuously inside an enclosure at 265 VAC full load using FLIR thermal camera to measure component temperatures.

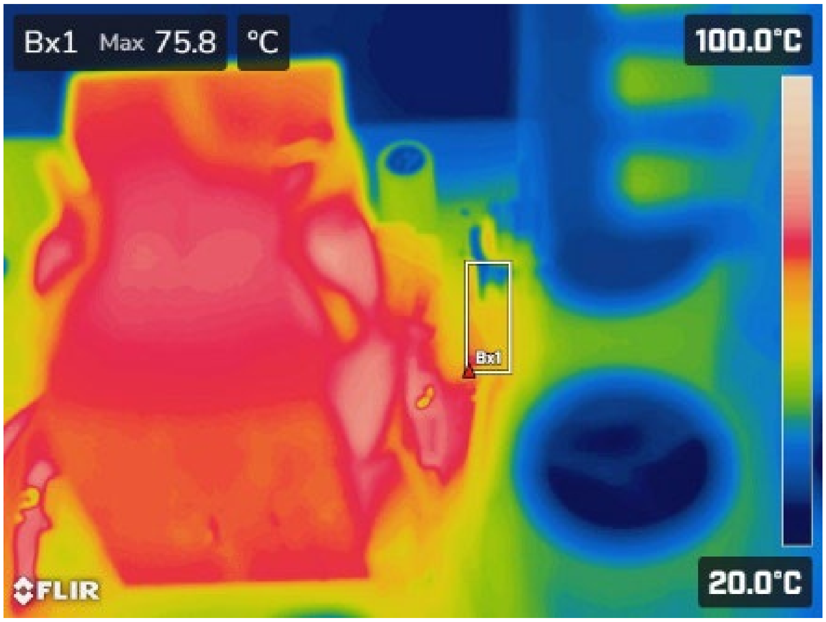


Figure 75 – 265 VAC 50 Hz. Thermals – TOP7075E (U2).

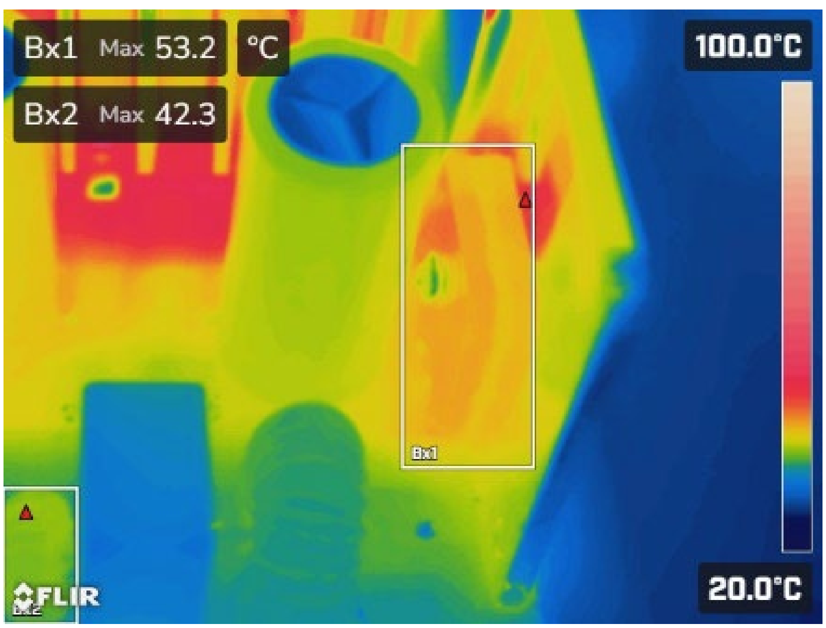


Figure 76 – 265 VAC 50 Hz. Thermals – Input Filter Side.

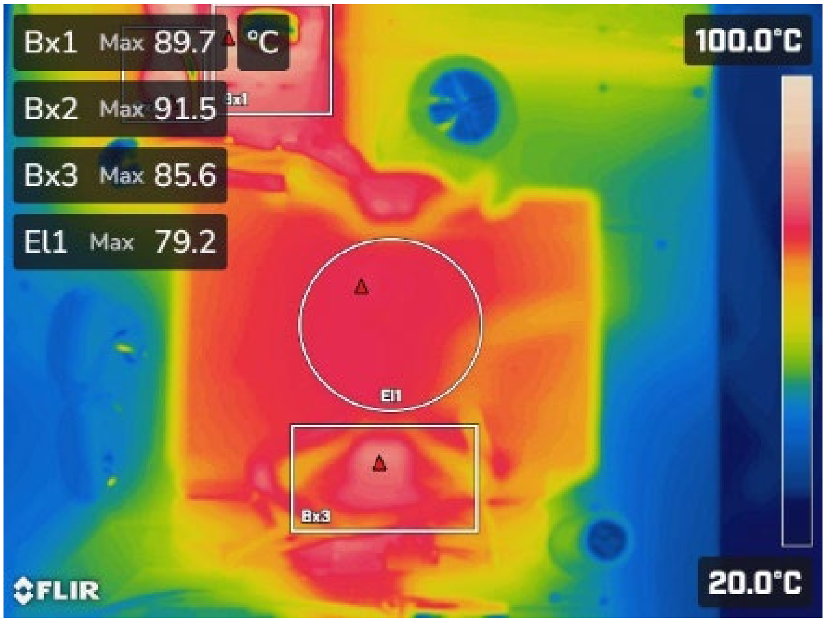


Figure 77 – 265 VAC 60 Hz. Thermals – Top Side.

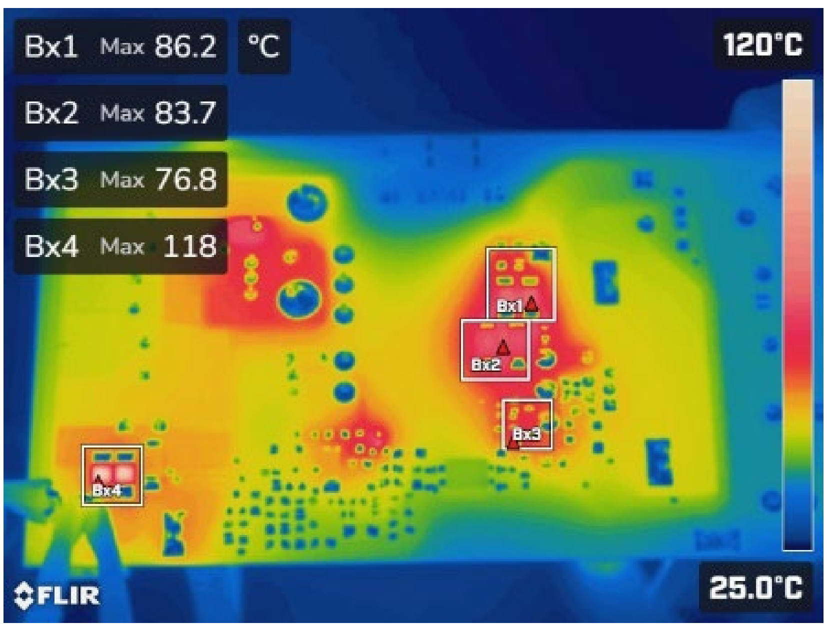


Figure 78 – 265 VAC 60 Hz. Thermals – Bottom Side.

Component		**Actual Temperature**	**Projected temperature at maximum 40 °C Ambient (°C)**
	Ambient	33.5	40
U2	TOP7075E	75.8	82.3
D2 & D3	Primary Snubber Diode	83.7	90.2
R7 & R8	Primary Snubber Resistor	86.2	92.7
D4	Primary Bias Diode	76.8	83.3
L2	CMC 1	42.3	48.8
BR1	Bridge Rectifier	53.2	59.7
T1	Transformer Core	79.2	85.7
T1	Transformer Winding	85.6	92.1
D6	Output Rectifier	89.7	96.2
R14	Secondary Snubber Resistor	91.5	98
R24 & R25	R_{SENSE}	118	124

14.2 Thermal Performance at 40 °C Ambient

14.2.1 85 VAC Full Load at 40 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 85 VAC full load using thermocouple to measure component temperatures.

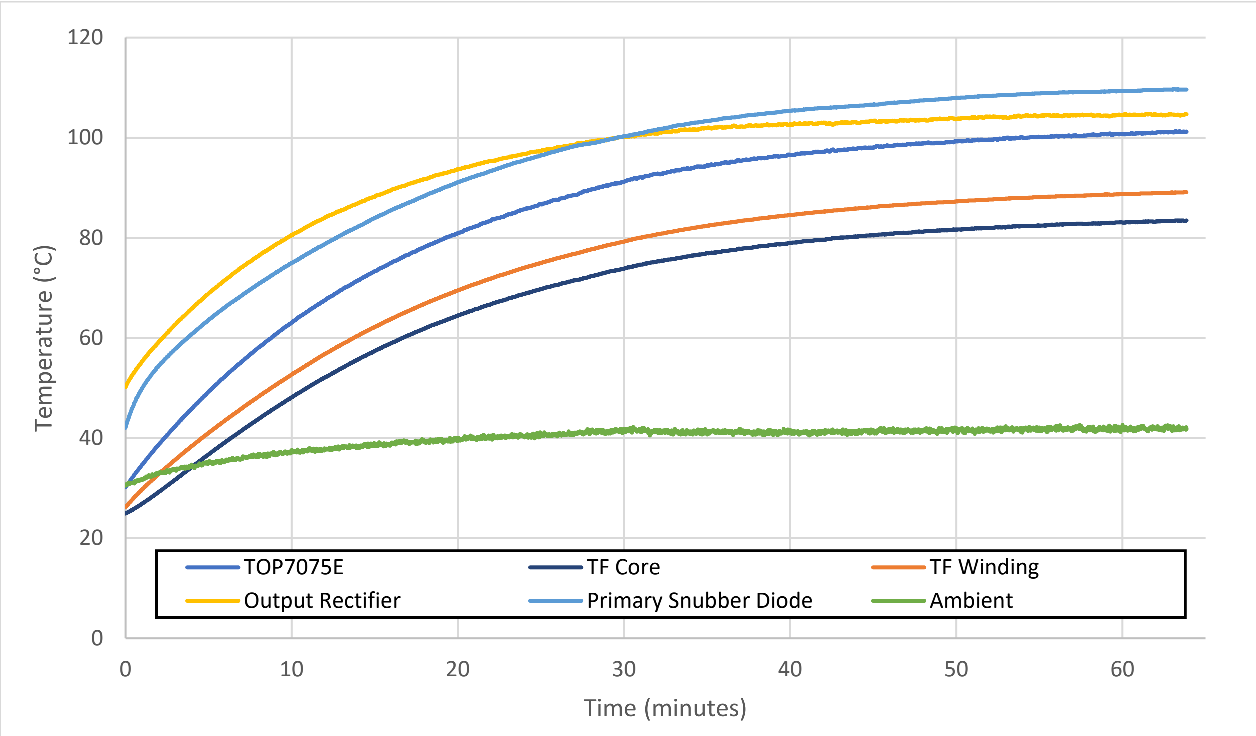


Figure 79 – 85 VAC 60 Hz Component Thermals.

Component	Temperature (°C)
TOP7075E	101
TF Core	83.5
TF Winding	89.1
Output Rectifier	104
Primary Snubber Diode	109
Ambient	42.7

14.2.2 265 VAC Full Load at 40 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 265 VAC full load using thermocouple to measure component temperatures.

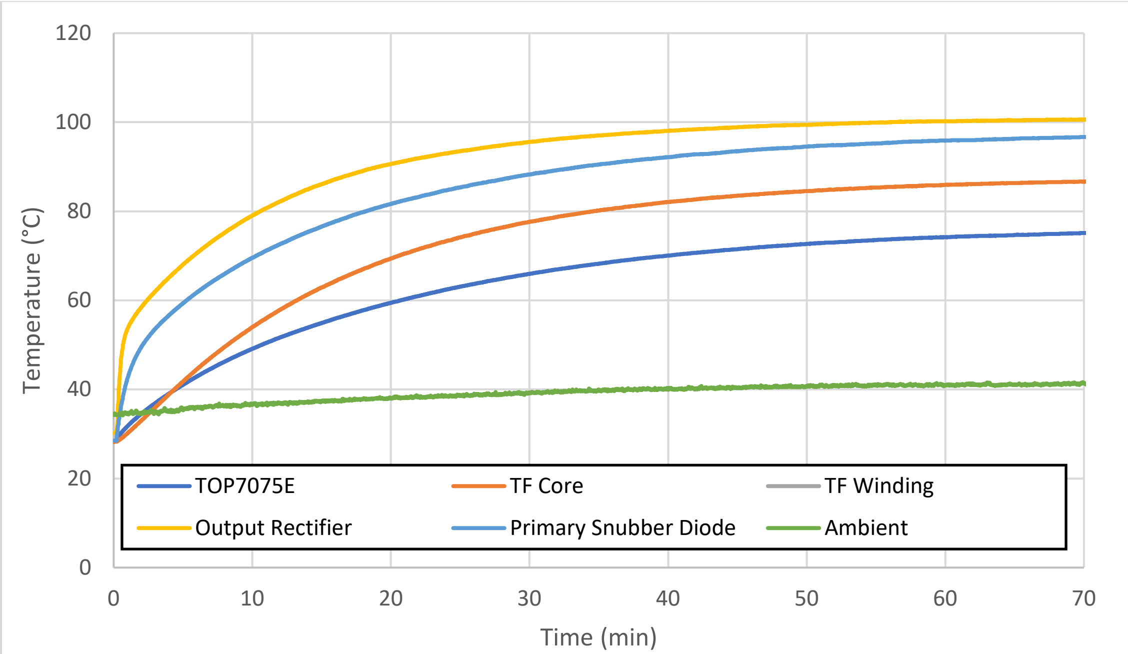


Figure 80 – 265 VAC 50 Hz Component Thermals.

Component	Temperature (°C)
TOP7075E	76.2
TF Core	87.4
TF Winding	89.8
Output Rectifier	101
Primary Snubber Diode	97.5
Ambient	41.9

15 CV/CC Operation

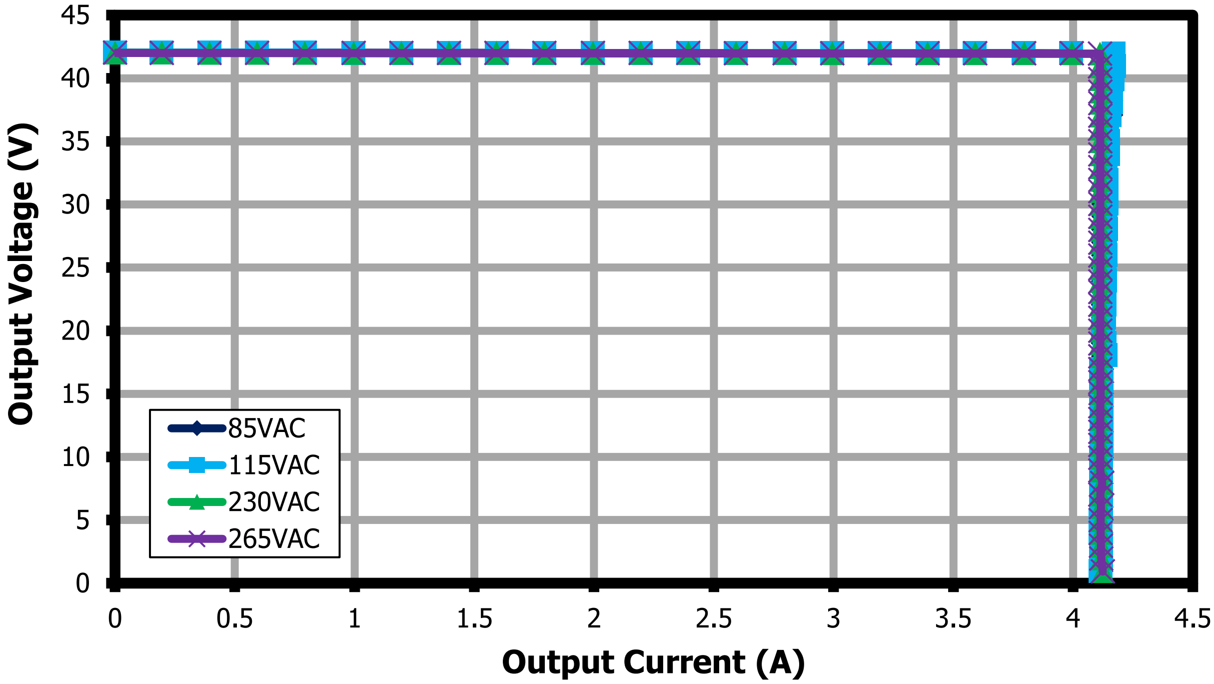


Figure 81 – 265 VAC 50 Hz Component Thermals.

16 Fault Protection

16.1 Output Overvoltage Protection

To trigger Output OVP, lower feedback resistor (R28) is shorted.

16.1.1 OVP during Start-Up Condition

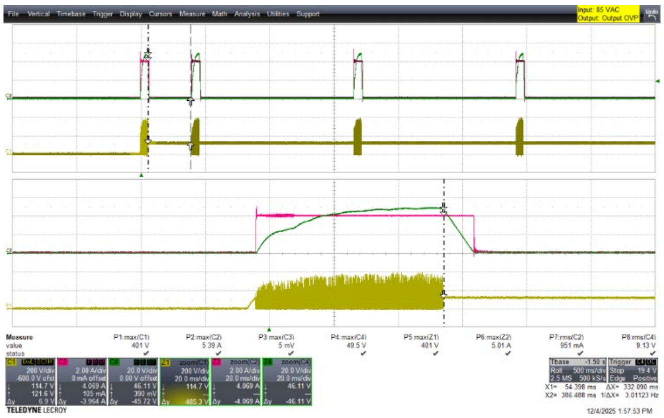


Figure 82 – 85 VAC, Full Load – OVP during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 49.5 V.

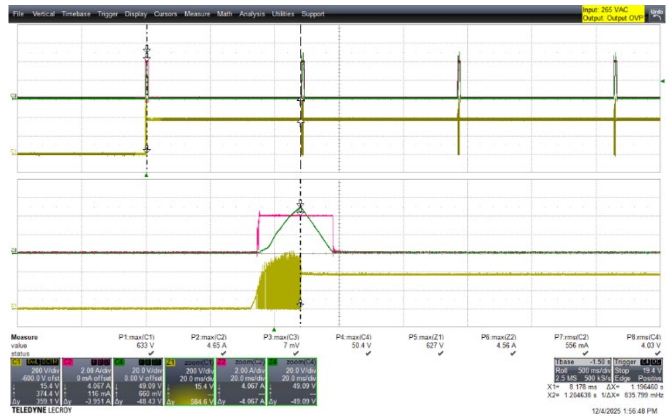


Figure 83 – 265 VAC, Full Load – OVP during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.4 V.

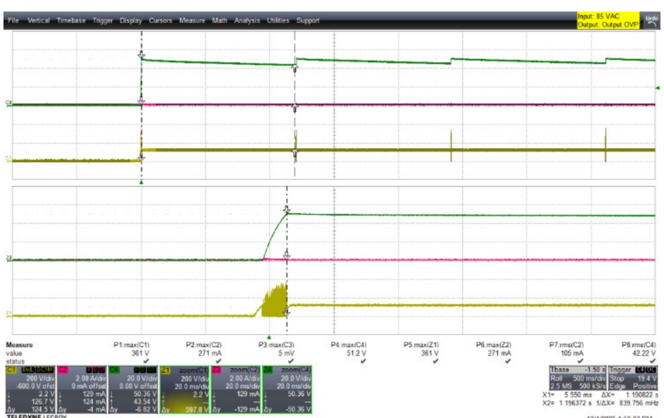


Figure 84 – 85 VAC, No Load – OVP during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 51.2 V.

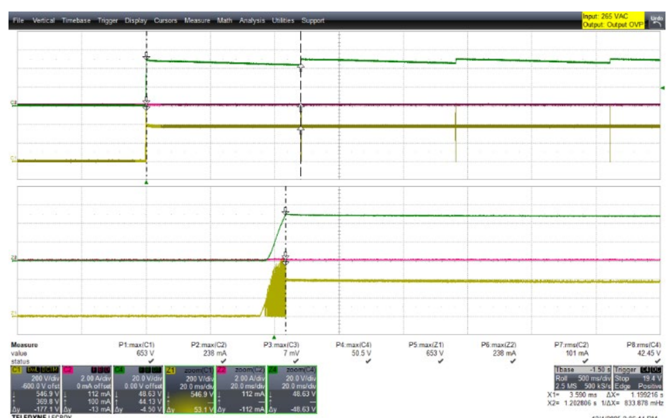


Figure 85 – 265 VAC, No Load – OVP during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.5 V.

16.1.2 OVP during Normal Condition

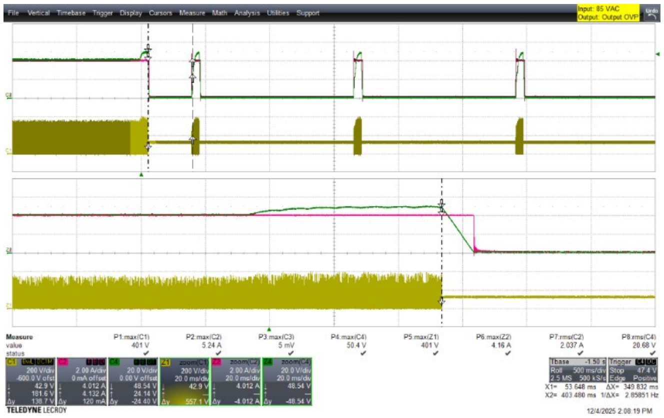


Figure 86 – 85 VAC, Full Load – OVP during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.4 V.

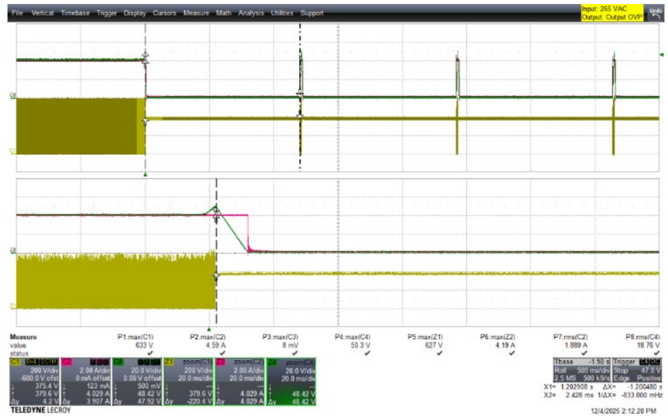


Figure 87 – 265 VAC, Full Load – OVP during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.3 V.

Figure 88 – 85 VAC, No Load – OVP during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.3 V.

Figure 89 – 265 VAC, No Load – OVP during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum Output Voltage = 50.6 V.

16.2 Output Short-Circuit Protection

To trigger Output OVP, Output Capacitor (C22) is shorted.

16.2.1 Output Short Circuit during Start-Up Condition

Figure 90 – 85 VAC, Full Load – Output short circuit during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 288 V.

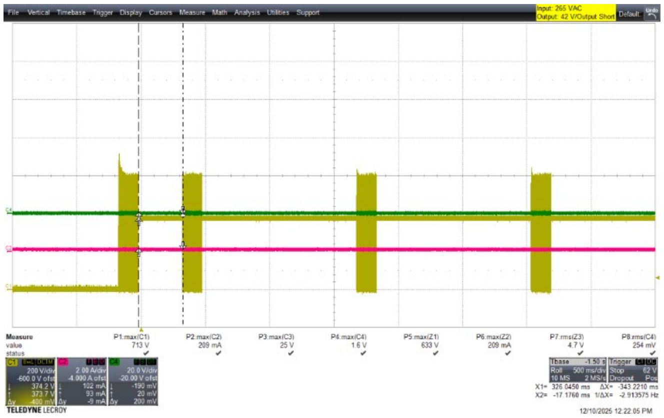


Figure 91 – 265 VAC, Full Load – Output short circuit during startup condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 713 V (89% derating).

16.2.2 Output Short Circuit during Normal Condition

Figure 92 – 85 VAC, Full Load – Output Short circuit during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 368 V.

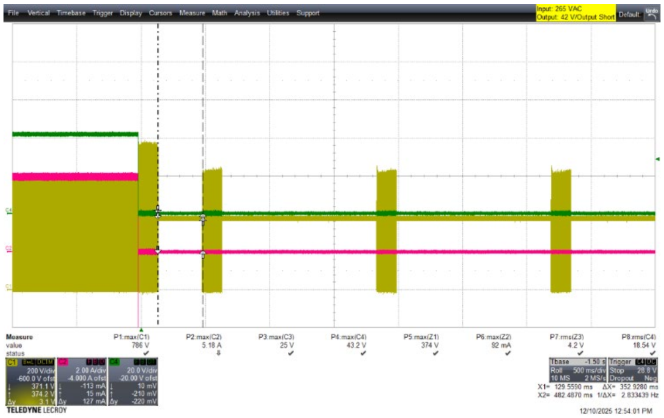


Figure 93 – 265 VAC, Full Load – Output Short circuit during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 786 V. (98% derating)

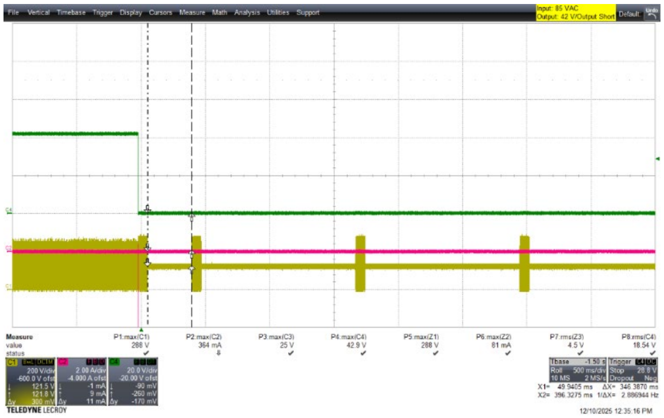


Figure 94 – 85 VAC, No Load – Output short circuit during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 288 V

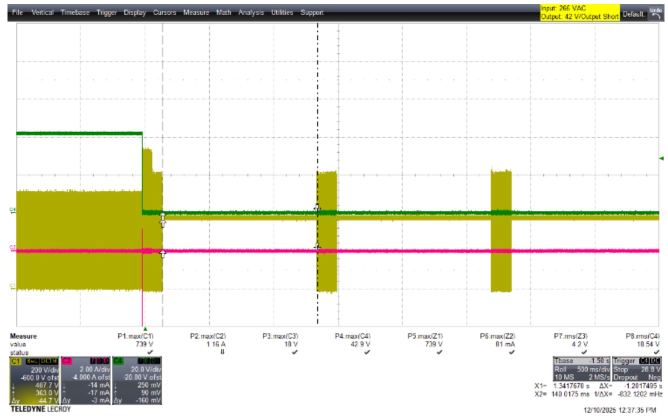


Figure 95 – 265 VAC, No Load – Output short circuit during normal condition.
CH1: TOP7075E_V_{DS}, 200 V / div., 500 ms / div.
CH2: I_{OUT}, 2 A / div., 500 ms / div.
CH3: V_{OUT}, 20 V / div., 500 ms / div.
Zoom: 20 ms/div.
Maximum TOP7075E_V_{DS} = 739 V (92% derating)

16.3 Line Overvoltage Protection

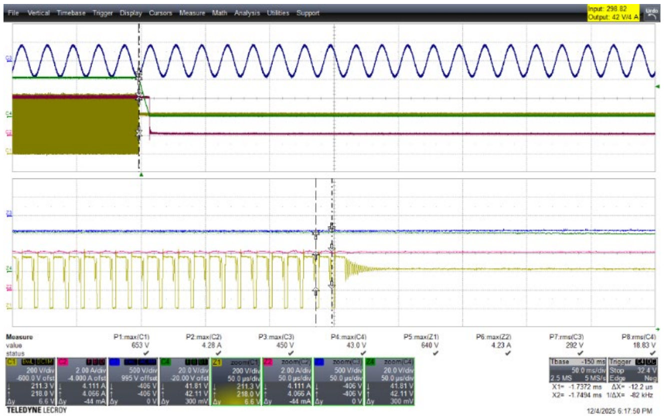


Figure 96 – Line OV+, Full Load.
CH1: TOP7075E_V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{OUT}, 2 A / div., 50 ms / div.
CH3: AC INPUT, 500 V / div., 50 ms / div.
CH3: V_{OUT}, 20 V / div., 50 ms / div.
Zoom: 50 μs/div.
Line_OV+ Voltage = 298 VAC, I_{OV+} = 56.2 μA

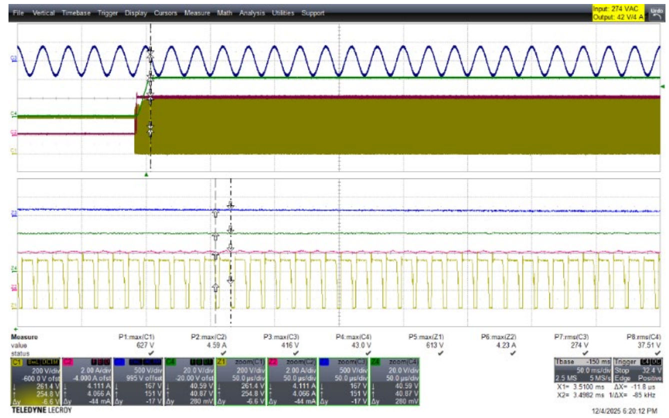


Figure 97 – Line OV-, Full Load.
CH1: TOP7075E_V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{OUT}, 2 A / div., 50 ms / div.
CH3: AC INPUT, 500 V / div., 50 ms / div.
CH3: V_{OUT}, 20 V / div., 50 ms / div.
Zoom: 50 μs/div.
Line_OV- Voltage = 274 VAC, I_{OV+} = 51.7 μA

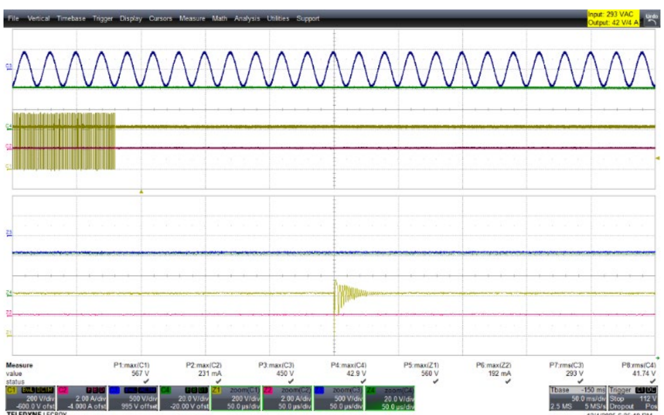


Figure 98 – Line OV+, No Load.
CH1: TOP7075E_V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{OUT}, 2 A / div., 50 ms / div.
CH3: AC INPUT, 500 V / div., 50 ms / div.
CH3: V_{OUT}, 20 V / div., 50 ms / div.
Zoom: 50 μs/div.
Line_OV+ Voltage = 293 VAC, I_{OV+} = 55.2 μA

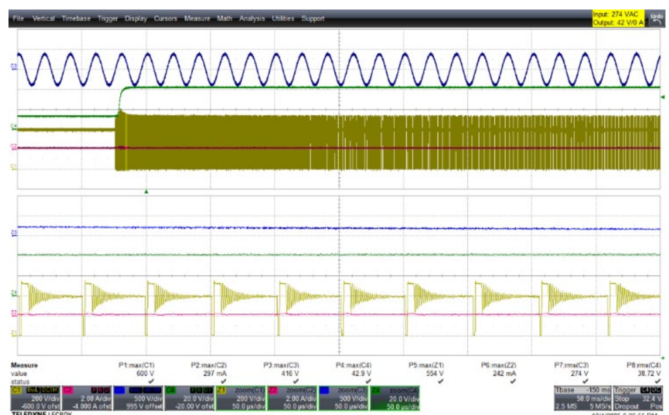


Figure 99 – Line OV-, No Load.
CH1: TOP7075E_V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{OUT}, 2 A / div., 50 ms / div.
CH3: AC INPUT, 500 V / div., 50 ms / div.
CH3: V_{OUT}, 20 V / div., 50 ms / div.
Zoom: 50 μs/div.
Line_OV+ Voltage = 274 VAC, I_{OV+} = 51.7 μA

16.4 Overtemperature Protection

The unit was placed inside the thermal chamber and ambient temperature was increased to trigger over-temperature conditions and then decreased for thermal recovery. IC case temperature was measured using thermocouple.

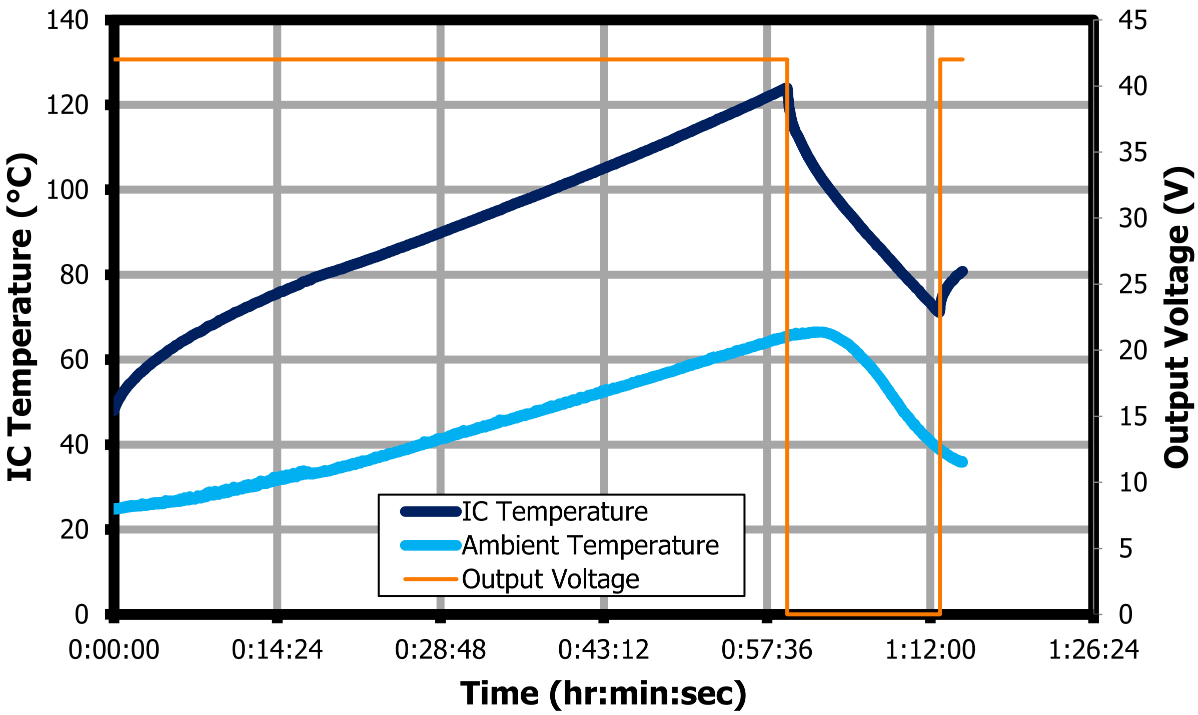


Figure 100 – 85 VAC Full Load OTP.

OTP Temperature	124 °C
Recovery Temperature	71.4 °C
Hysteresis	52.6 °C

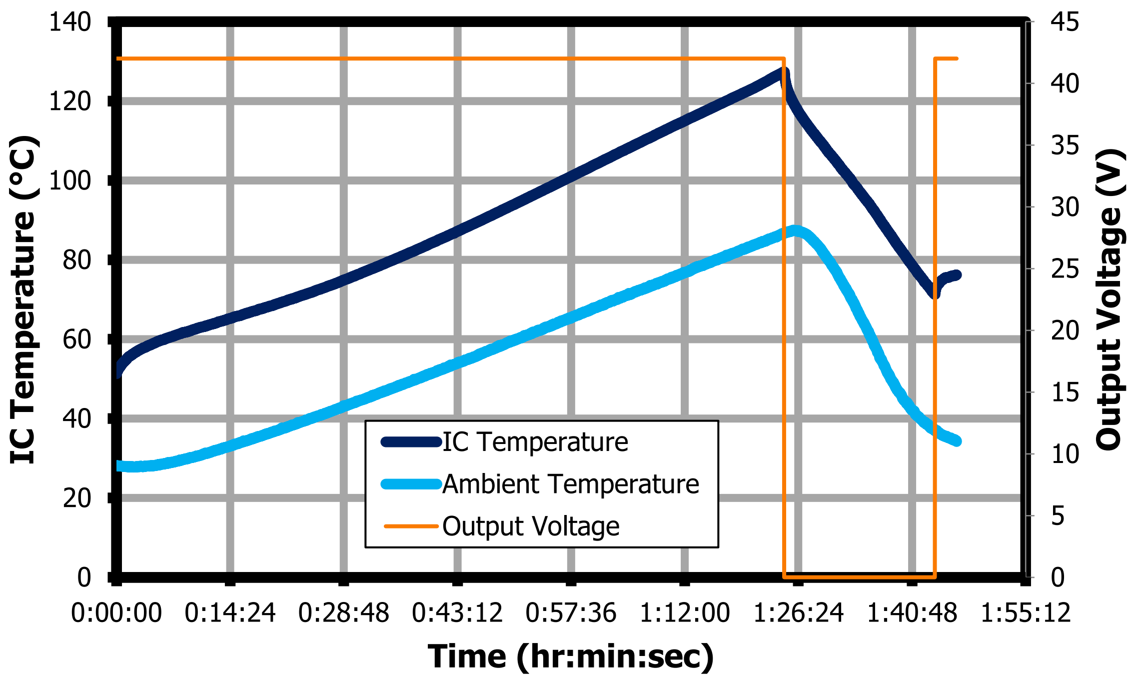


Figure 101 – 265 VAC Full Load OTP.

OTP Temperature	127 °C
Recovery Temperature	71.3 °C
Hysteresis	55.7 °C

17 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (42 V, 4 A). Measurements were taken with floating ground.

17.1 Test Set-up Equipment

17.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Input voltage set at 115 VAC and 230 VAC.
4. 42 V R_{LOAD} resistance is 10.5 Ohms.

17.2 Output Float

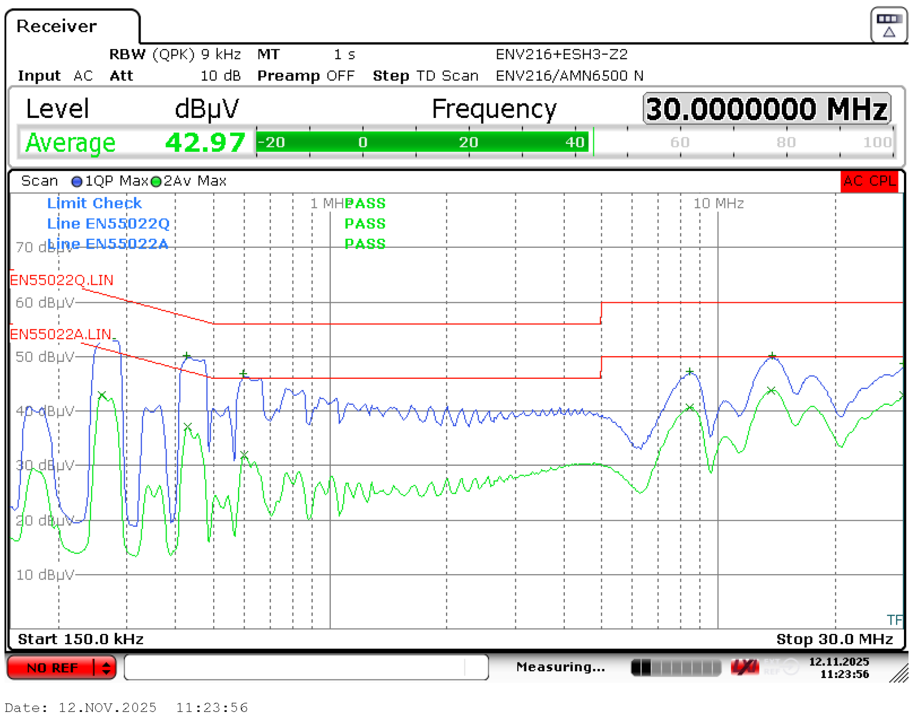


Figure 102 – 115 VAC 60 Hz.
Line / Neutral - Floating

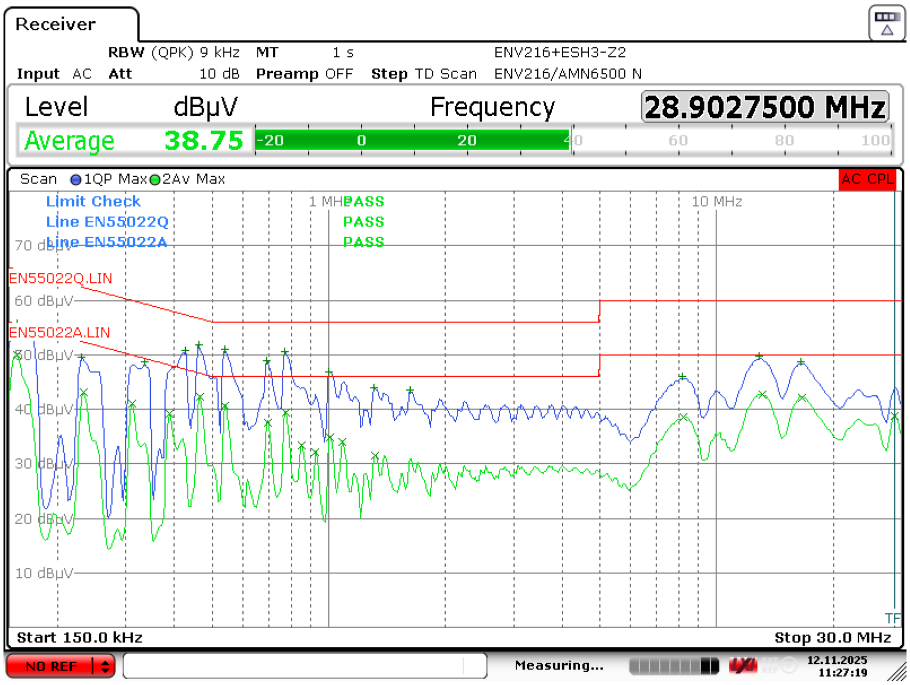


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Figure 103 – 230 VAC 50 Hz.
Line / Neutral - Floating

18 ESD

All ESD strikes were applied at PCB end with 115 and 230 VAC input voltage and full load.

Input: 115 VAC, Output: 42 V/10.5 Ω Full Load

Passed ±8.8 kV contact discharge

Contact Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+8.8	42 V	10	PASS
-8.8	42 V	10	PASS
+8.8	GND	10	PASS
-8.8	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Passed ±16.5 kV air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+16.5	42 V	10	PASS
-16.5	42 V	10	PASS
+16.5	GND	10	PASS
-16.5	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Input: 230 VAC, Output: 42 V/10.5 Ω Full Load

Passed ±8.8 kV contact discharge

Contact Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+8.8	42 V	10	PASS
-8.8	42 V	10	PASS
+8.8	GND	10	PASS
-8.8	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Passed ±16.5 kV air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+16.5	42 V	10	PASS
-16.5	42 V	10	PASS
+16.5	GND	10	PASS
-16.5	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

19 Combination Wave (Differential Mode)

Tested at 115 and 230 VAC input voltage and full load

Input: 115 VAC, Output: 42 V/10.5 Ω Full Load

Passed 2 kV Differential Mode Combination Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+2000 V	0°	L, N	2 Ω	10	PASS
–2000 V	0°	L, N	2 Ω	10	PASS
+2000 V	90°	L, N	2 Ω	10	PASS
–2000 V	90°	L, N	2 Ω	10	PASS
+2000 V	180°	L, N	2 Ω	10	PASS
–2000 V	180°	L, N	2 Ω	10	PASS
+2000 V	270°	L, N	2 Ω	10	PASS
–2000 V	270°	L, N	2 Ω	10	PASS

Input: 230 VAC, Output: 42 V/10.5 Ω Full Load

Passed 2 kV Differential Mode Combination Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+2000 V	0°	L, N	2 Ω	10	PASS
–2000 V	0°	L, N	2 Ω	10	PASS
+2000 V	90°	L, N	2 Ω	10	PASS
–2000 V	90°	L, N	2 Ω	10	PASS
+2000 V	180°	L, N	2 Ω	10	PASS
–2000 V	180°	L, N	2 Ω	10	PASS
+2000 V	270°	L, N	2 Ω	10	PASS
–2000 V	270°	L, N	2 Ω	10	PASS

20 Ring Wave (Common Mode)

Tested at 115 VAC and 230 VAC input voltage and full load

Input: 115 VAC, Output: 42 V/10.5 Ω Full Load

Passed 6 kV Common Mode Ring Wave Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+6000 V	0°	L/N - PE	12	10	PASS
–6000 V	0°	L/N - PE	12	10	PASS
+6000 V	90°	L/N - PE	12	10	PASS
–6000 V	90°	L/N - PE	12	10	PASS
+6000 V	180°	L/N - PE	12	10	PASS
–6000 V	180°	L/N - PE	12	10	PASS
+6000 V	270°	L/N - PE	12	10	PASS
–6000 V	270°	L/N - PE	12	10	PASS

Input: 230 VAC, Output: 42 V/10.5 Ω Full Load

Passed 6 kV Common Mode Ring Wave Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+6000 V	0°	L/N - PE	12	10	PASS
–6000 V	0°	L/N - PE	12	10	PASS
+6000 V	90°	L/N - PE	12	10	PASS
–6000 V	90°	L/N - PE	12	10	PASS
+6000 V	180°	L/N - PE	12	10	PASS
–6000 V	180°	L/N - PE	12	10	PASS
+6000 V	270°	L/N - PE	12	10	PASS
–6000 V	270°	L/N - PE	12	10	PASS

21 EFT

Tested at 115 VAC & VAC Input Voltage and Full Load
Input: 115 VAC, Output: 42 V/10.5 Ω Full Load

Passed 4 kV EFT Event

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass

Input: 230 VAC, Output: 42 V/10.5 Ω Full Load

Passed 4 kV EFT Event

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	0°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	100 kHz	750 µs	300 ms	120 s	L1/L2 - PE	Pass

22 Appendix

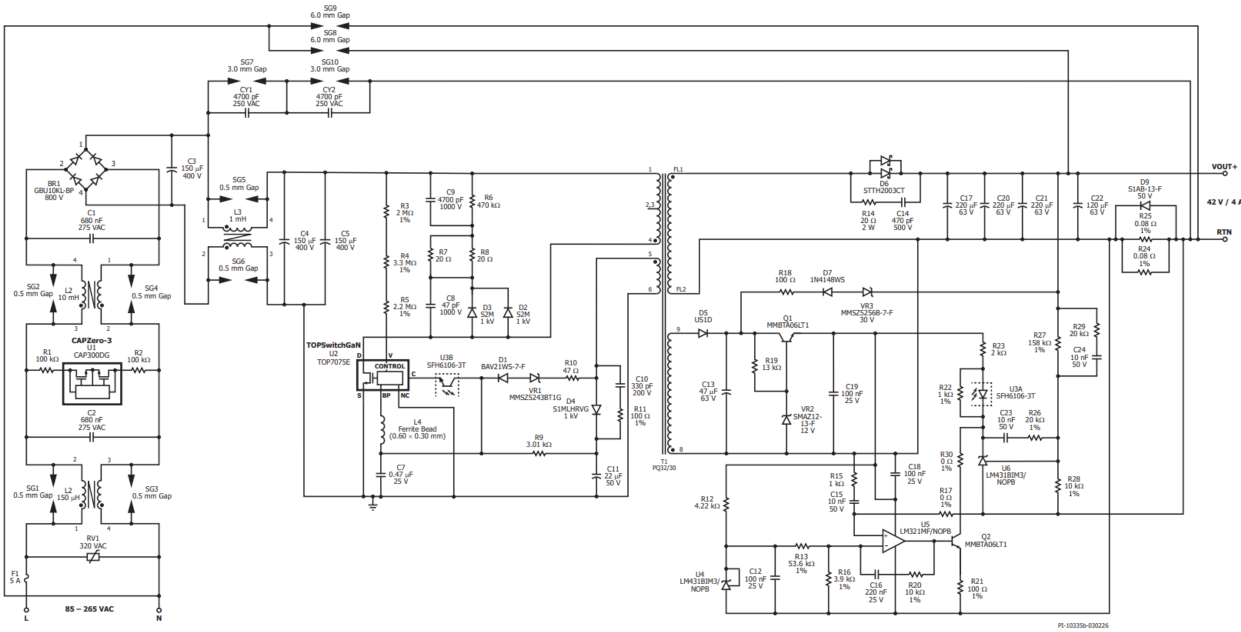

Figure 104 – Full Schematic with 0-ohm resistors.

R17 – 0 Ω, ±1 %.
R30 – 0 Ω, ±1 %.

23 Revision History

Date	Author	Revision	Description and Changes	Reviewed
16-Mar-26	MA	A	Initial Release	Apps & Mktg.

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