LNK3604, LNK3694 & 3696
LinkSwitch-XT2 Family

Energy Efficient, Low Power Off-Line Switcher IC
With Integrated System Level Protection

Product Highlights

Easy to Design

- Lowest component count switcher solution
- Selectable device current limit
- Fully integrated auto-restart for short-circuit and open-loop protection
- Optional self-biased supply
- Frequency jittering greatly reduces EMI
- Meets HV creepage requirements between DRAIN and all other pins both on the PCB and at the package
- Pin-out simplifies PCB heat sinking

Features Superior to Linear/RCC

- Output overvoltage protection (OVP)
- Input overvoltage line protection (OVL)
- Hysteretic over-temperature protection (OTP)
- Extended creepage between DRAIN pin and all other pins improves field reliability
- 725 V MOSFET rating series for excellent surge withstand
- 900 V MOSFET rating series for industrial design or extra safety margin
- Extremely low component count enhances reliability
  - Allows single-sided PCB and full SMD manufacturability

EcoSmart™ – Extremely Energy-Efficient

- Easily meets all global energy efficiency regulations
- No-load consumption <100 mW without bias winding at 265 VAC input (<10 mW with bias winding)
- ON/OFF control provides constant efficiency to very light loads

Applications

- Flyback converters
- Supplies for appliances, industrial systems, and metering

Description

LinkSwitch™-XT2 incorporates a 725 V / 900 V power MOSFET, oscillator, simple ON/OFF control scheme, a high-voltage switched current source, frequency jittering, cycle-by-cycle current limit and thermal shutdown circuitry onto a monolithic IC. The start-up and operating power are derived directly from the DRAIN pin, eliminating the need for a bias winding and associated circuitry.

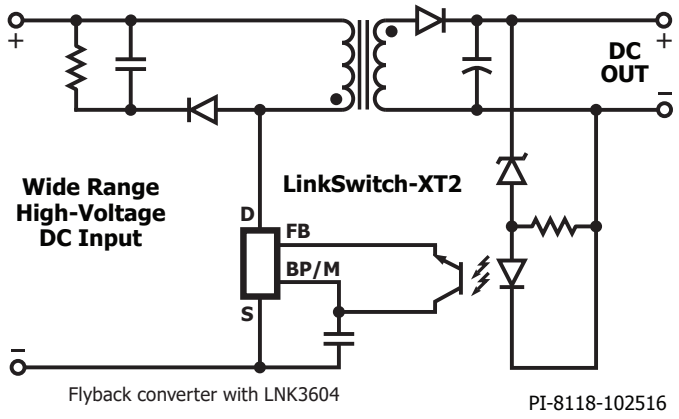


Figure 1. Typical Application with LinkSwitch-XT2.

Figure 2. Package Options. P: PDIP-8C, G: SMD-8C, D: SO-8C.

Output Power Table[4]		
Product[3]	Peak or Open Frame[1,2]	
	725 V MOSFET	
	230 VAC ±15%	85-265 VAC
LNK3604P/G/D	9.2 W	6.1 W
Product[3]	900 V MOSFET	
	230 VAC ±15%	85-484 VAC
LNK3694P/G	6 W	4 W
LNK3696P/G	11 W	8 W

Table 1. Output Power Table.

Notes:
1. Maximum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
3. Packages: P: DIP-8C, G: SMD-8C, D: SO-8C. Please see Part Ordering Information.
4. See Key Application Considerations section for complete description of assumptions.

This Product is Covered by Patents and/or Pending Patent Applications.

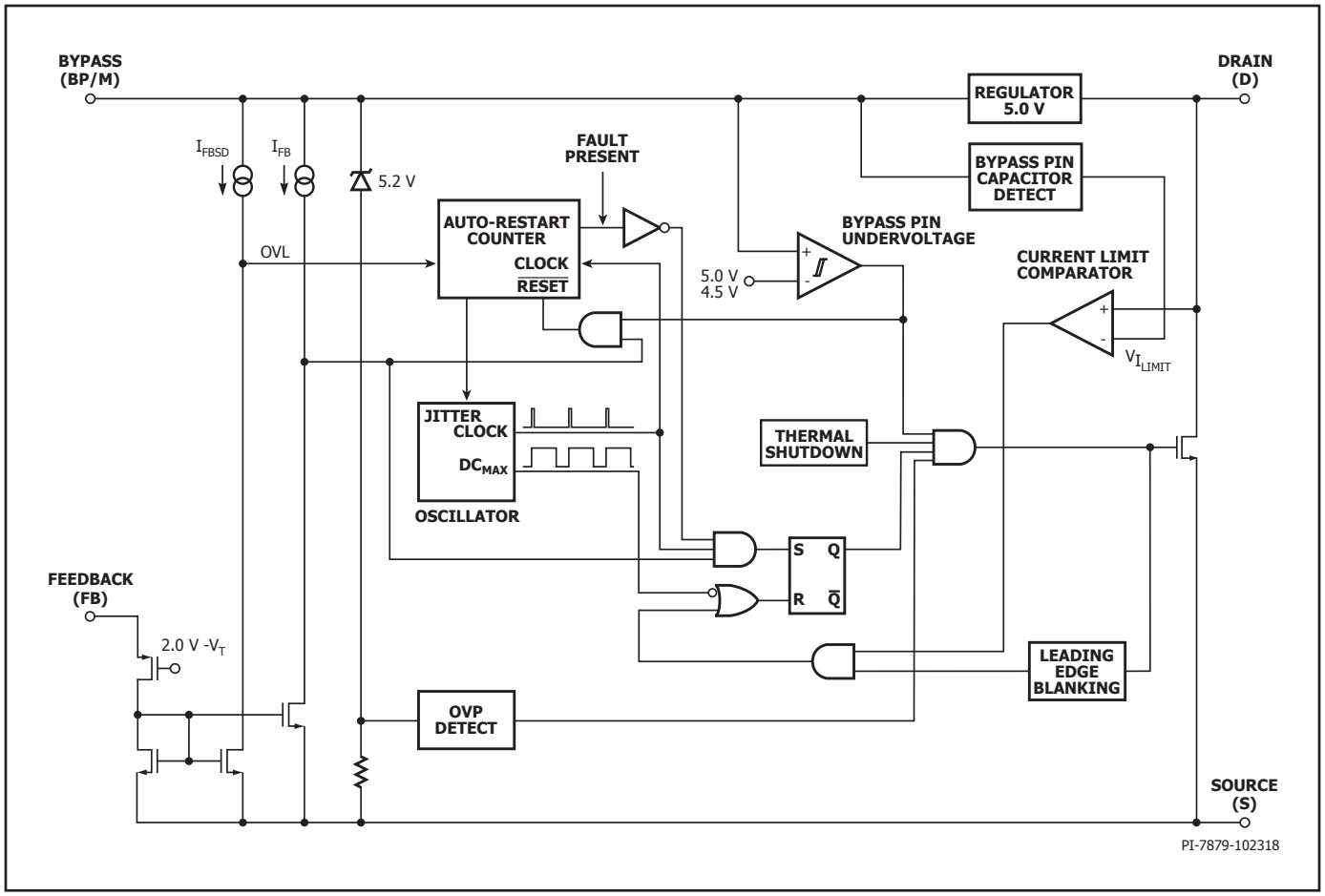


Figure 3. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP/M) Pin:
This pin has multiple functions:

- It is the connection point for an external bypass capacitor for the internally generated 5.0 V supply.
- It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1 μF capacitor results in the standard current limit value. Use of a 1 μF capacitor results in the current limit being reduced for lower power design.
- It provides a shutdown function. When the current into the BYPASS pin exceeds $I_{BP(SD)}$ for a time equal to 2 to 3 cycles of the internal oscillator (f_{OSC}), the device enters auto-restart. This can be used to provide an output overvoltage protection function with external circuitry.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by the FEEDBACK pin. The Power MOSFET switching is terminated when a current greater than I_{FB} (49 μA) is delivered into this pin. Line overvoltage protection is detected when a current greater than I_{FBSD} (670 μA) is delivered into this pin for 2 consecutive switching cycles.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

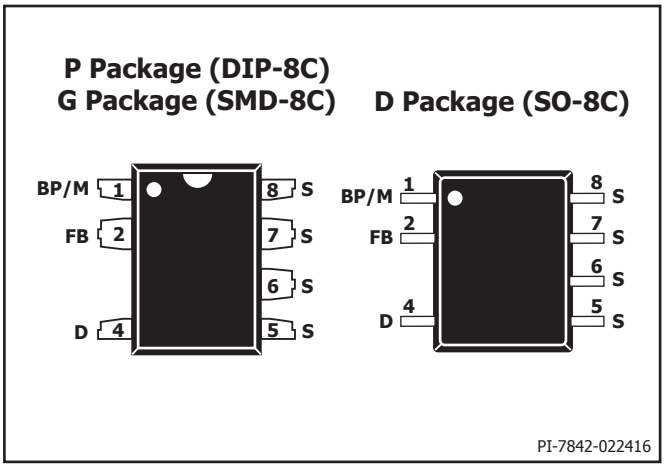


Figure 4. Pin Configuration.

LinkSwitch-XT2 Functional Description

LinkSwitch-XT2 IC combines a high-voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-XT2 ICs use a simple ON/OFF control to regulate the output voltage. The LinkSwitch-XT2 controller consists of an oscillator, feedback (sense and logic) circuit, 5.0 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a high-voltage power MOSFET. The LinkSwitch-XT2 incorporates additional circuitry for auto-restart.

Oscillator

The typical oscillator frequency is internally set to an average of f_{OSC} (66 kHz or 132 kHz). Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of each cycle.

The LinkSwitch-XT2 oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 4 kHz peak-to-peak (LNK369X) and 8 kHz peak-to-peak (LNK3604), to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 5 illustrates the frequency jitter of the LinkSwitch-XT2 IC.

Feedback Input Circuit

The feedback input circuit at the FEEDBACK pin consists of a low impedance source follower output set at V_{FB} (2.0 V). When the current delivered into this pin exceeds I_{FB} (49 µA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The sampling is done only at the beginning of each cycle. Subsequent changes in the FEEDBACK pin voltage or current during the remainder of the cycle do not impact the MOSFET enable/disable status. If a current greater than $I_{FB(SD)}$ is injected into the FEEDBACK pin while the power MOSFET is enabled for at least two consecutive cycles the part will stop switching and enter auto-restart off-time. Normal switching resumes after the auto-restart off-time expires. This shutdown function allows implementing line overvoltage protection (see Figure 7). The current into the FEEDBACK pin should be limited to less than 1.2 mA.

5.0 V Regulator and 5.2 V Shunt Voltage Clamp

The 5.0 V regulator charges the bypass capacitor connected to the BYPASS pin to V_{BP} by drawing a current from the voltage on the DRAIN, whenever the power MOSFET is off. The BYPASS pin is the internal supply voltage node for the LinkSwitch-XT2 IC. When the power MOSFET is on, the LinkSwitch-XT2 IC runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-XT2 IC to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a shunt regulator clamping the BYPASS pin at $V_{BP(SHUNT)}$ (5.2 V) when current is provided to the BYPASS pin through an external resistor. This facilitates powering of LinkSwitch-XT2 externally through a bias winding to decrease the no-load consumption to about 10 mW (flyback). The device stops switching instantly and enters auto-restart when a current $\geq I_{BP(SD)}$ is delivered into the BYPASS pin. Adding an external Zener diode from the output voltage to the BYPASS pin allows implementing an hysteretic OVP function (see Figure 6). The current into the BYPASS pin should be limited to less than 16 mA.

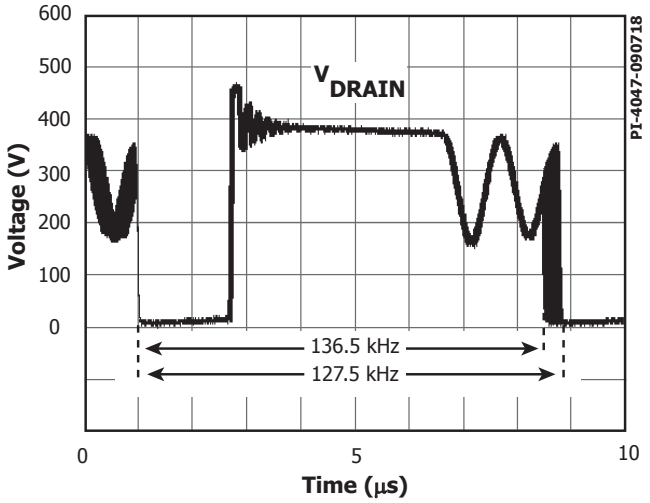


Figure 5a. Frequency Jitter (LNK3604).

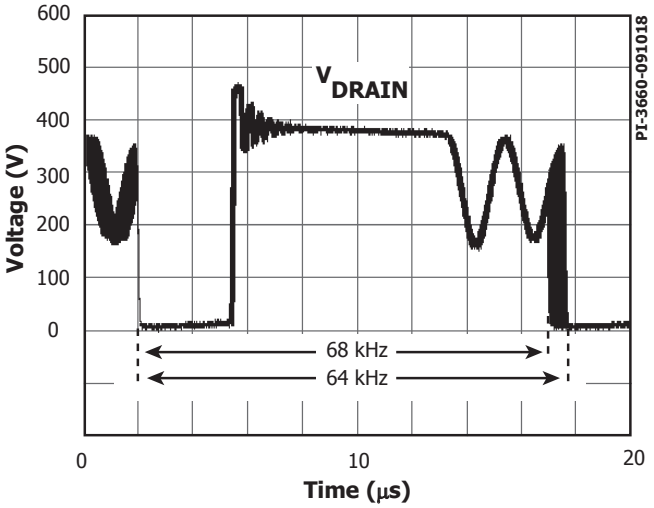


Figure 5b. Frequency Jitter (LNK369X).

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below V_{BP}–$V_{BP(H)}$ (approximately 4.5 V). Once the BYPASS pin voltage drops below this threshold, it must rise back to V_{BP} to enable (turn-on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at TSD (142 °C typical) with a 75 °C ($T_{SD(H)}$) hysteresis. When the die temperature rises above T_{SD} the power MOSFET is disabled and remains disabled until the die temperature falls to T_{SD}–$T_{SD(H)}$, at which point it is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the switching pulse. Current limit can be selected

using the BYPASS pin capacitor (0.1 μF for normal current limit / 1 μF for reduced current limit). LinkSwitch-XT2 ICs select between normal and reduced current limit at power-up prior to switching.

Auto-Restart

In the event of a fault condition such as output overload, output short, or an open-loop condition, LinkSwitch-XT2 ICs enter into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FEEDBACK pin is pulled high. If the FEEDBACK pin is not pulled high for $t_{AR(ON)}$ (50 ms), the power MOSFET switching is disabled for a time equal to the auto-restart off-time. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ First Off Period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ Subsequent Periods). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. The auto-restart counter is gated by the switch oscillator.

Hysteretic Output Overvoltage Protection

The output overvoltage protection provided by the LinkSwitch-XT2 IC uses auto-restart that is triggered by a current $>I_{BP(SD)}$ into the BYPASS pin. In addition to an internal filter, the BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE pin and BYPASS pins of the device.

The OVP function can be realized by connecting a Zener diode from the output supply to the BYPASS pin. The circuit example shown in Figure 6 describes simple method for implementing the output overvoltage protection. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode connected from the output to the BYPASS pin and bypass voltage, will cause a current in excess of $I_{BP(SD)}$ injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter the LinkSwitch-XT2 IC senses indirectly the DC bus overvoltage condition during the power MOSFET on-time by monitoring the current flowing into the FEEDBACK pin. Figure 7 shows one possible circuit implementation. During the power MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the input winding. The current flowing through transistor Q3 is therefore representing V_{BUS}. Indirect line sensing minimizes power dissipation and is used for line OV protection. The LinkSwitch-XT2 IC will go into auto-restart mode if the FEEDBACK pin current exceeds the line overvoltage threshold current $I_{FB(SD)}$ for at least 2 consecutive switching cycles.

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding which can introduce an error in the line OV sampling. In some designs, a RC snubber across the rectifier diode may be needed to damp the ringing at the secondary winding when line voltage is sampled.

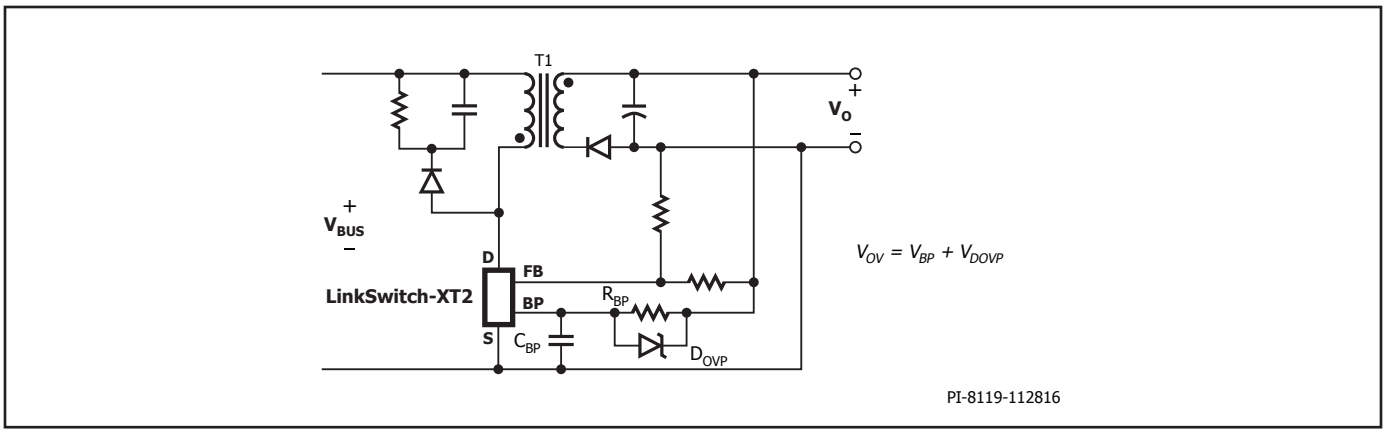
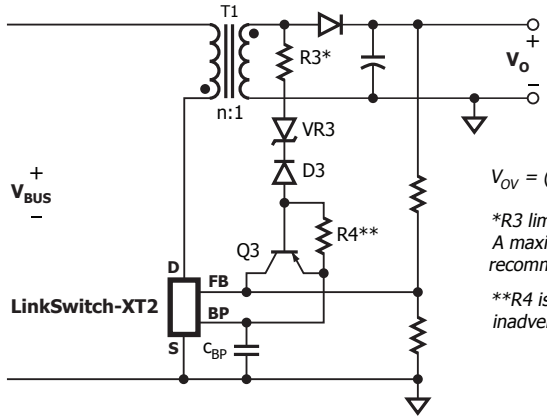


Figure 6. Non-Isolated Flyback Converter with Output Overvoltage Protection.



$V_{OV} = (V_{VR3} + V_{D3} + V_{BE(Q3)} - V_{BP} + V_{R3}) \times n + V_{DS}$

**R3 limits the current into the FEEDBACK pin. A maximum current of 120% of I_{FBSD} is recommended.*

***R4 is a pull-down resister for Q3 to avoid inadvertant triggering. 2 kΩ is a typical starting point*

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Figure 7. Line-Sensing for Overvoltage Protection by using FEEDBACK Pin.

Applications Example

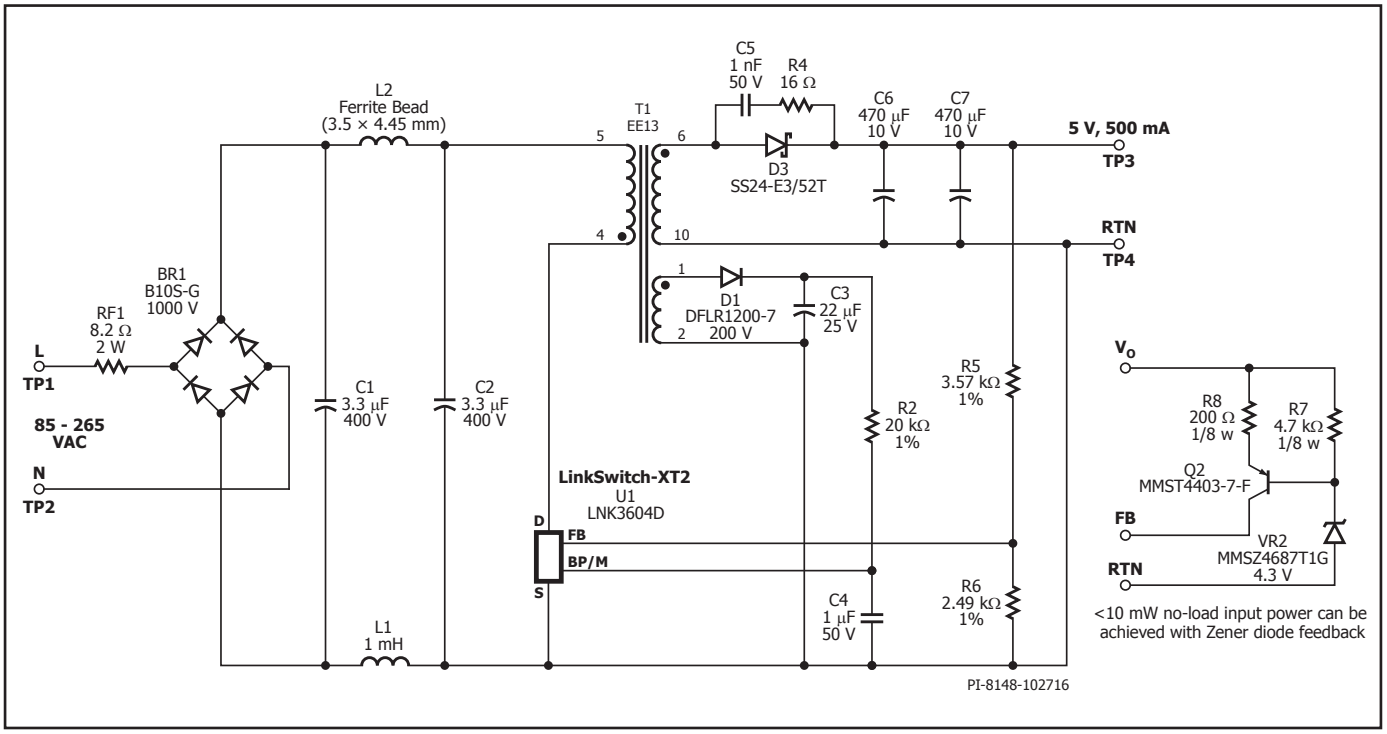


Figure 8. 2.5 W Universal Input Design using LNK3604.

A 5 V, 500 mA (2.5 W) Design

The schematic shown in Figure 8 is a typical implementation of a universal input, 5 V ±5%, 500 mA adapter using LNK3604D. This circuit makes use of the clampless technique to eliminate the primary clamp components and reduce the complexity of the circuit.

The EcoSmart features built into the LinkSwitch-XT2 family allow this design to easily meet all current and proposed energy efficiency standards, including the mandatory California Energy Commission (CEC) requirement for average operating efficiency.

The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C1 and C2. Resistor RF1 is a flameproof, fusible, wire wound type and functions as a fuse, inrush current limiter and, together with the filter formed by C1, C2, L1 and L2, differential mode noise attenuator.

This simple input stage, together with the frequency jittering of LinkSwitch-XT2 ICs, and PI's E-Shield™ windings within T1, allow the design to meet both conducted EMI limits with ≥10 dBV margin.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the primary is driven by the integrated power MOSFET in U1. No primary clamp is required as the low value and tight tolerance of the LNK3604D IC's internal current limit allows the primary winding capacitance of the transformer and drain-source capacitance of the power MOSFET in the LNK3604D to provide adequate clamping of the leakage inductance drain voltage spike. The secondary of the flyback transformer T1 is rectified by D3, a Schottky diode, and filtered by C6, C7, low ESR capacitor. The output voltage is sensed via resistor divider R5 and R6. Output voltage is regulated so as to achieve a voltage of 2 V on the FEEDBACK pin. To achieve <10 mW no-load input power, we can also use the Zener to do the feedback sense. The combined voltage drop across VR2, emitter to base voltage drop of transistor Q2 ($V_{EB(Q2)}$) and R8 determines the output voltage. When the output voltage exceeds this level, current will flow through transistor Q2. As the current increases, the current fed into the FEEDBACK pin of U1 increases until the turnoff threshold current (~49 µA) is reached, disabling further switching cycles of U1. At full load, almost all switching cycles will be enabled, and at very light loads, almost all the switching cycles will be disabled, giving a low effective frequency and providing high light load efficiency and low no-load consumption.

Resistor R7 provides ≈150 µA through VR2 to bias the Zener diode closer to its test current. The diode used is a low test current Zener diode which needs only 50 µA to conduct, this will provide <10 mW no-load input power. Resistor R8 limits the current into FEEDBACK pin to less than 1.2 mA for protection. For higher output accuracy, the Zener diode may be replaced with a reference IC such as the TL431.

The LinkSwitch-XT2 ICs can be completely self-powered from the DRAIN pin, requiring only a small ceramic capacitor C3 connected to the BYPASS pin. Resistor R2 supplies the BYPASS pin externally from the auxiliary winding for significantly lower no-load input power and increased efficiency over all load conditions. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than 120 µA. For the best full load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than 257 µA.

Key Application Considerations

LinkSwitch-XT2 Design Considerations
Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Secondary output of 6 V with a fast PN rectifier diode.
3. Assumed efficiency of 70%.
4. Voltage only output (no secondary-side constant current circuit).
5. A primary clamp (RCD or Zener) is used.
6. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
7. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

Discontinuous mode operation (KP > 1) is recommended for LNK3604. Below a value of 1, KP is the ratio of ripple to peak primary current. Above a value of 1, KP is the ratio of primary power MOSFET OFF-time to the secondary diode conduction time. Due to the flux density requirements described below, typically a LinkSwitch-XT2 design will be discontinuous, which also has the benefits of allowing fast (instead of ultrafast) output diodes and reducing EMI.

Clampless Designs
Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore, the maximum AC input line voltage, the value of VOR, the leakage inductance energy, a function of leakage inductance and peak primary current, and the primary winding capacitance determine the peak drain voltage. With no significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only clampless design:

1. A clampless design should only be used for $P_O \leq 2.5$ W, using the reduced current limit mode ($C_{BP} = 1\ \mu F$) and a VOR** ≤ 90 V.
2. For designs where $P_O \leq 2$ W, a two-layer primary should be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF.
3. For designs where $2 < P_O \leq 2.5$ W, a bias winding should be added to the transformer using a standard recovery rectifier diode to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias-winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
4. For designs where $P_O > 2.5$ W clampless designs are not practical and an external RCD or Zener clamp should be used.
5. Ensure that worst-case high line, peak drain voltage is below the BV_{DSS} specification of the internal power MOSFET and ideally $< V_{DSS} \times 0.9$ to allow margin for design variation.

†For 110 VAC only input designs it may be possible to extend the power range of clampless designs to include the standard current limit mode. However, the increased leakage ringing may degrade EMI performance.

**VOR is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The VOR adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.

Audible Noise
The cycle skipping mode of operation used in LinkSwitch-XT2 ICs can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 1500 gauss (150 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics, such as Z5U, when used in clamp circuits may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

LinkSwitch-XT2 Layout Considerations

See Figures 9, 10 and 11 for a recommended circuit board layout for LinkSwitch-XT2 (D, P and G packages).

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor C_{BP}
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and LinkSwitch-XT2 IC together should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and LinkSwitch-XT2 IC.

Thermal Considerations
The copper area underneath the LinkSwitch-XT2 IC acts not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it should be maximized for good heat sinking of LinkSwitch-XT2 IC. The same applies to the cathode of the output diode.

Y Capacitor
Y capacitor is generally not used for this power level. If you want to use, the placement of the Y type capacitor should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the LinkSwitch-XT2 device. Note that if an input pi (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Feedback Signal
Place the transistor Q2 physically close to the LinkSwitch-XT2 IC to minimize trace lengths from the transistor to FEEDBACK pin. Keep the high current, high-voltage drain and clamp traces away from the feedback signal to prevent noise pick up.

Output Diode
For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all LinkSwitch-XT2 designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that VDS does not exceed 90% of BV_{DSS} at the highest input voltage and peak (overload) output power. The 10% margin versus BV_{DSS} specification gives margin for design variation, especially in clampless designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for LinkSwitch-XT2 IC, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-XT2 IC as specified in the data sheet. Under low-line, maximum power, a maximum LinkSwitch-XT2 IC SOURCE pin temperature of 100 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations website: www.power.com

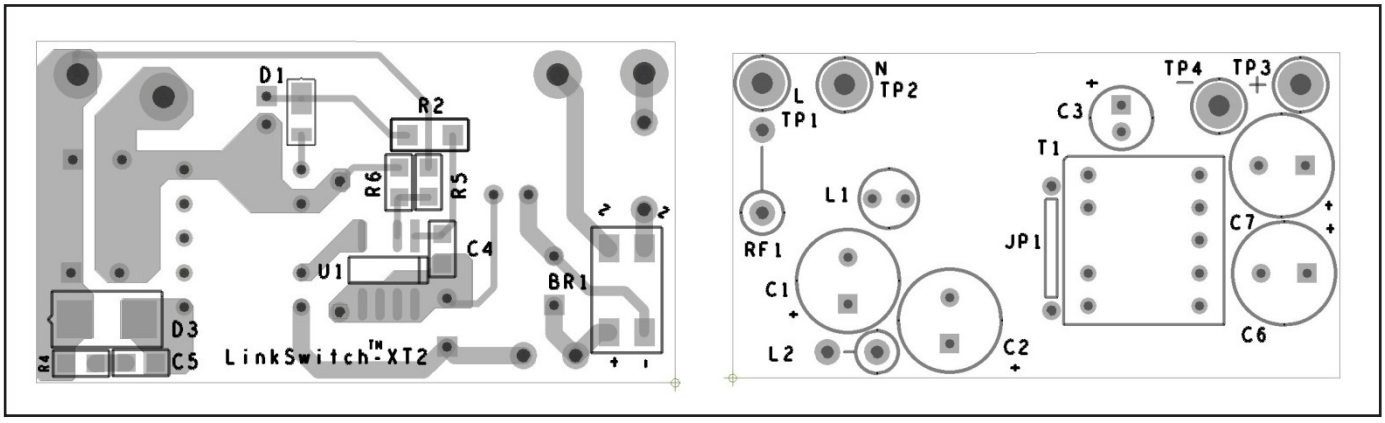


Figure 9. Recommended Printed Circuit Layout for LinkSwitch-XT2 using D Package in a Flyback Converter Configuration (Bottom Left, Top Right).

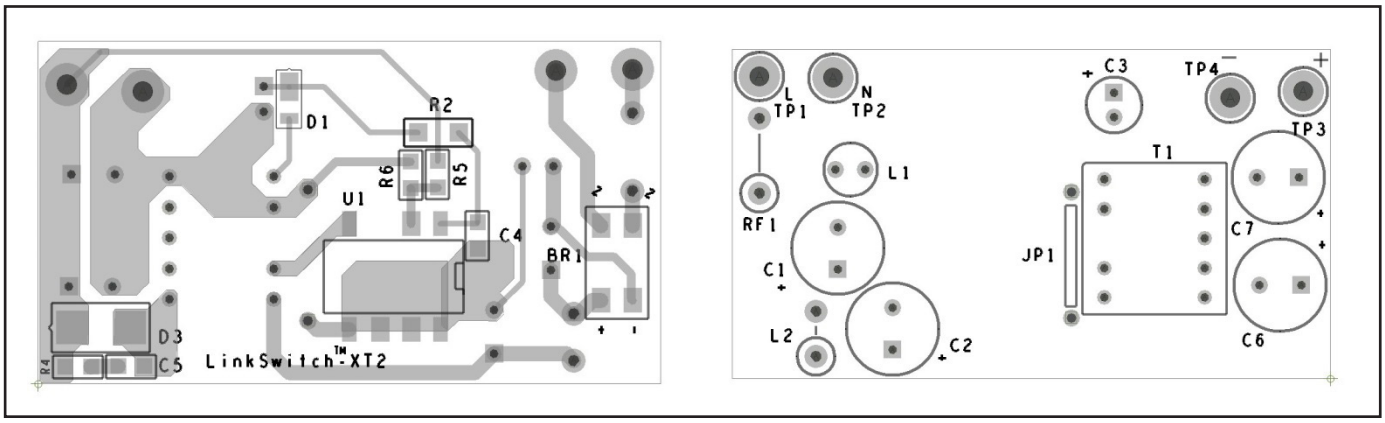


Figure 10. Recommended Printed Circuit Layout for LinkSwitch-XT2 using G Package in a Flyback Converter Configuration (Bottom Left, Top Right).

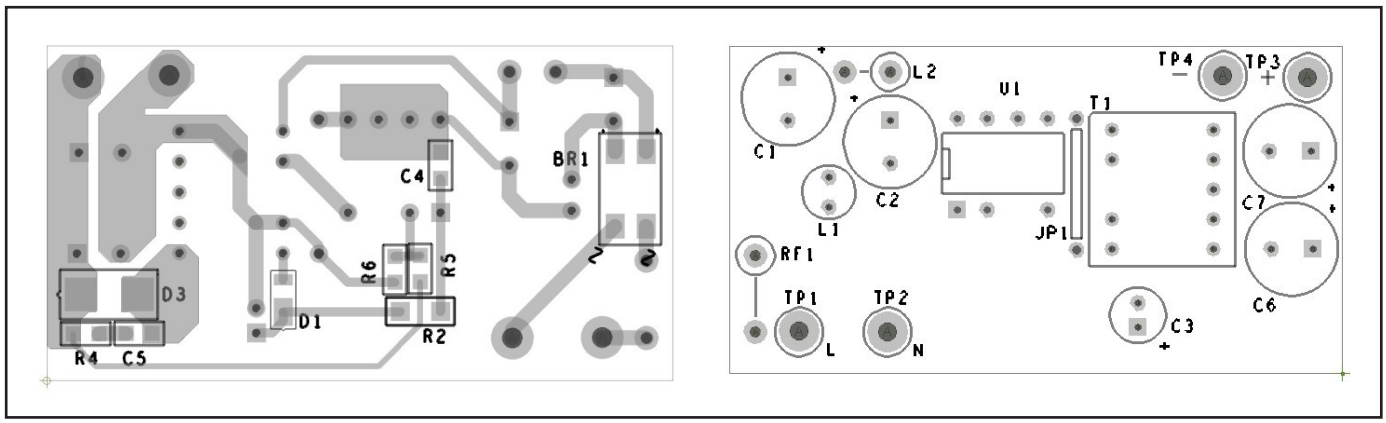


Figure 11. Recommended Printed Circuit Layout for LinkSwitch-XT2 using P Package in a Flyback Converter Configuration (Bottom Left, Top Right).

Absolute Maximum Ratings(1,5)

DRAIN Pin Voltage: LNK3604 .....-0.3 V to 725 V
LNK369X .....-0.3 V to 900 V
DRAIN Pin Peak Current: LNK3604 ..... 1230 mA(2)
LNK3694 ..... 2000 mA(2)
LNK3696 ..... 6000 mA(2)
FEEDBACK Pin Voltage..... -0.3 V to 7 V
FEEDBACK Pin Current.....100 mA
BYPASS Pin Voltage ..... -0.3 V to 7 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature(3) .....-40 °C to 150 °C
Lead Temperature(4) .....260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. See Figures 17 and 25 for V_{DS} > 400 V.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: P or G Package:
(θ_{JA}) ..... 70 °C/W(2); 60 °C/W(3)
(θ_{JC})(1) .....11 °C/W
D Package:
(θ_{JA}) ..... 100 °C/W(2); 80 °C/W(3)
(θ_{JC})(1) .....30 °C/W

Notes:
1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Output Frequency	f_{OSC}	LNK3604 T_J = 25 °C	Average	124	132	140	kHz
			Peak-Peak Jitter		8		
		LNK3694 / LNK3696 T_J = 25 °C	Average	62	66	70	
			Peak-Peak Jitter		4		
Maximum Duty Cycle	DC_{MAX}	S2 Open	LNK3604	66			%
			LNK3694 / LNK3696	65			
FEEDBACK Pin Turnoff Threshold Current	I_{FB}	V_{BP} = 5.0 V to 5.5 V T_J = 25 °C		44	49	54	µA
FEEDBACK Pin Voltage at Turnoff Threshold	V_{FB}	V_{BP} = 5.0 V to 5.5 V T_J = 25 °C		1.97	2.00	2.03	V
FEEDBACK Pin Instant Shutdown Current	$I_{FB(SD)}$	T_J = 25 °C		520	675	800	µA
FEEDBACK Pin Instant Shutdown Delay		T_J = 25 °C			2		Switch Cycles
FEEDBACK Pin Voltage at Shutdown Current	$V_{FB(SD)}$	V_{BP} = 5.0 V to 5.5 V T_J = 25 °C	LNK3604		3.3		V
			LNK3694 / LNK3696		3.1		
DRAIN Pin Supply Current	I_{S1}	V_{FB} = 2.1 V (MOSFET Not Switching) See Note A			75		µA
	I_{S2}	FEEDBACK Open (MOSFET Switching) See Notes A, B	LNK3604		150	230	µA
			LNK3694		120	170	
			LNK3696		205	320	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V T_J = 25 °C		-11	-7	-3	mA
	I_{CH2}	V_{BP} = 4 V T_J = 25 °C		-7.5	-5	-2.5	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BYPASS Pin Voltage	V_{BP}			4.7	5.0	5.2	V
BYPASS Pin Shutdown Threshold Current	$I_{BP(SD)}$	T_J = 25 °C			6	8	mA
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA		4.95	5.2	5.45	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$				0.47		V
BYPASS Pin Supply Current	$I_{BP(SC)}$	See Note C		55			µA
Circuit Protection							
Standard Current Limit (C_{BP} = 0.1 µF, See Note D, H)	I_{LIMIT}	di/dt = 65 mA/µs T_J = 25 °C	LNK3604	240	257	275	mA
		di/dt = 415 mA/µs T_J = 25 °C		278	317	356	
		di/dt = 33 mA/µs T_J = 25 °C	LNK3694	240.5	260	279.5	
		di/dt = 210 mA/µs T_J = 25 °C		265.5	287	308.5	
		di/dt = 60 mA/µs T_J = 25 °C	LNK3696	446	482	518	
		di/dt = 385 mA/µs T_J = 25 °C		496	535	575	
Reduced Current Limit (C_{BP} = 1 µF, See Note D, H)	$I_{LIMIT(RED)}$	di/dt = 65 mA/µs T_J = 25 °C	LNK3604	180	205	230	mA
		di/dt = 415 mA/µs T_J = 25 °C		227	258	289	
		di/dt = 33 mA/µs T_J = 25 °C	LNK3694	189	205	220	
		di/dt = 210 mA/µs T_J = 25 °C		212	230	247	
		di/dt = 60 mA/µs T_J = 25 °C	LNK3696	347	375	404	
		di/dt = 385 mA/µs T_J = 25 °C		388.5	420	451.5	
Minimum On-Time	$t_{ON(MIN)}$	See Note I	LNK3604	356	475	594	ns
			LNK3694	110	250	390	
			LNK3696	200	345	490	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note E	LNK3604	300	450		ns
			LNK3694 / LNK3696	140	215		
Thermal Shutdown Temperature	T_{SD}	See Note F		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note F			75		°C

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 12 (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK3604 I_D = 25 mA	T_J = 25 °C		24	27.6	Ω
			T_J = 100 °C		38	44.2	
		LNK3694 I_D = 86 mA	T_J = 25 °C		17	19.6	
			T_J = 100 °C		27	31	
		LNK3696 I_D = 163 mA	T_J = 25 °C		5.3	6.1	
			T_J = 100 °C		8.4	9.7	
OFF-State Drain Leakage Current	I_{DSS1}	V_{BP} = 5.4 V V_{FB} ≥2.1 V, V_{DS} = 560 V, T_J = 125 °C	LNK3604			200	µA
		V_{BP} = 5.4 V V_{FB} ≥2.1 V, V_{DS} = 720 V, T_J = 125 °C	LNK3694 / LNK3696				
	I_{DSS2}	V_{BPP} = V_{BPP} + 0.1V, V_{DSS} = 325 V, T_J = 25 °C			15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 5.4 V, V_{FB} ≥2.1 V, T_J = 25 °C	LNK3604	725			V
			LNK3694 / LNK3696	900			
DRAIN Pin Supply Voltage		T_J = 25 °C	LNK3604	18			V
			LNK369x	25			
Auto-Restart ON-Time	$t_{AR(ON)}$	T_J = 25 °C See Note G			50		ms
Auto-Restart OFF-Time	$t_{AR(OFF)}$	T_J = 25 °C See Note G	First Off Period		150		ms
			Subsequent Periods		1500		
Auto-Restart Duty Cycle	DC_{AR}	Subsequent Periods			3		%

NOTES:

A. Total current consumption is the sum of I_{S1} and I_{DSS} when FEEDBACK pin voltage is = 2.1 V (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when FEEDBACK pin is shorted to SOURCE (MOSFET switching).

B. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 5.1 V.

C. This current is only intended to supply an optional optocoupler connected between the BYPASS and FEEDBACK pins and not any other external circuitry.

D. For current limit at other di/dt values, refer to Figures 22, 23, 32 and 33.

E. This parameter is guaranteed by design.

F. This parameter is derived from characterization.

G. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

H. The BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application.

I. Measured using circuit in Figure 14 with 50 Ω drain pull-up. The width of the drain pulse is measured as the time from V_{FALL} = 42 V to V_{RISE} = 40 V (VDR = 50 V).

Nominal BP/M Pin Capacitor Value	**Tolerance Relative to Minimal Capacitor Value**	
	Min	Max
0.1 µF	-60%	+100%
1 µF	-50%	+100%

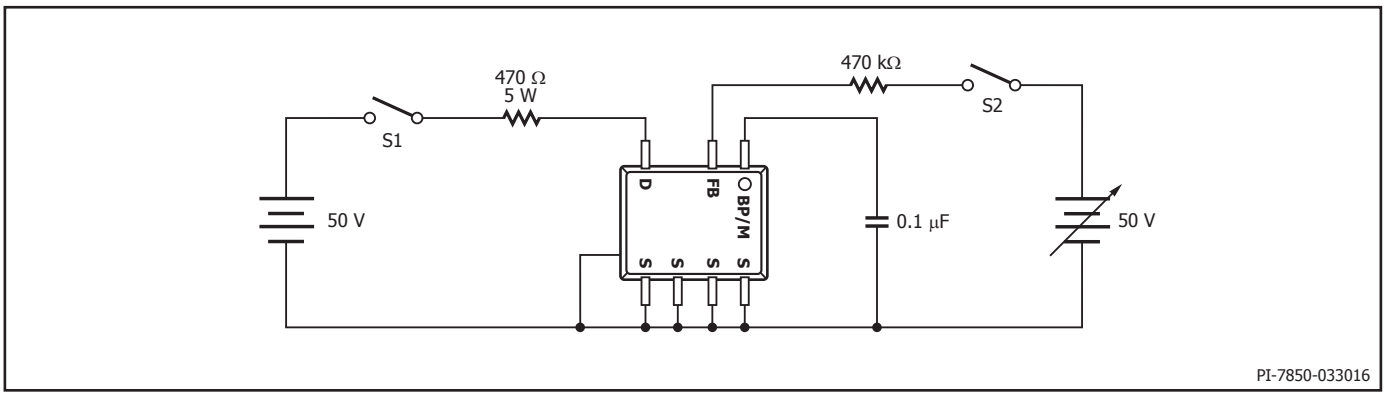


Figure 12. LinkSwitch-XT2 General Test Circuit.

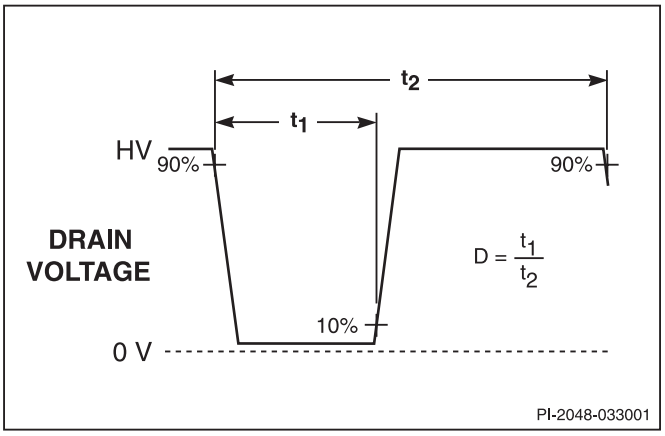


Figure 13. LinkSwitch-XT2 Duty Cycle Measurement.

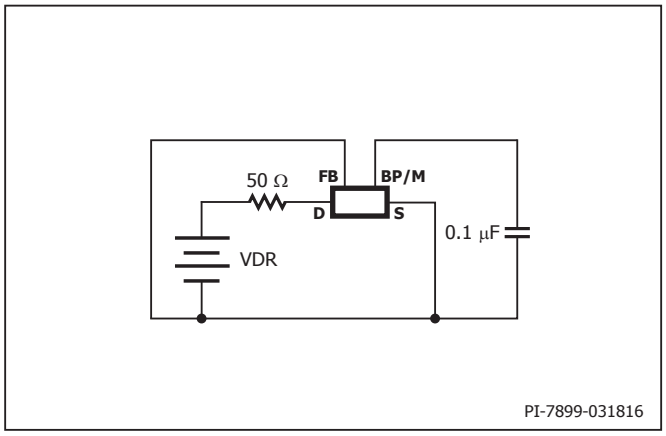


Figure 14. LinkSwitch-XT2 Minimum On-Time Test Circuit.

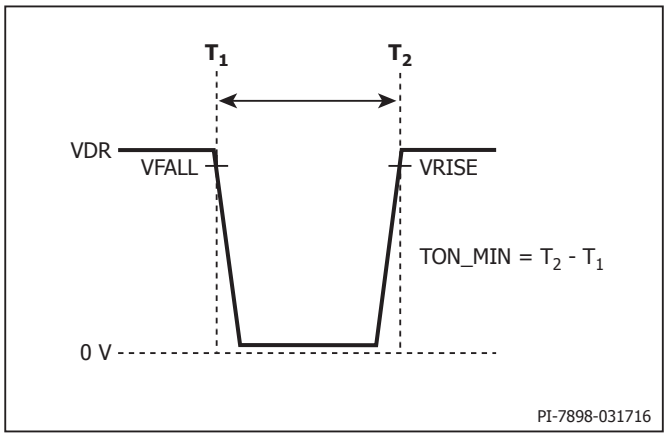


Figure 15. LinkSwitch-XT2 Minimum On-Time Measurement.

Typical Performance Characteristics

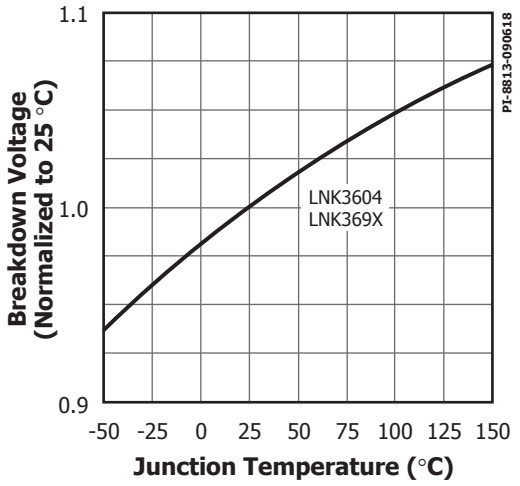


Figure 16. Breakdown vs. Temperature.

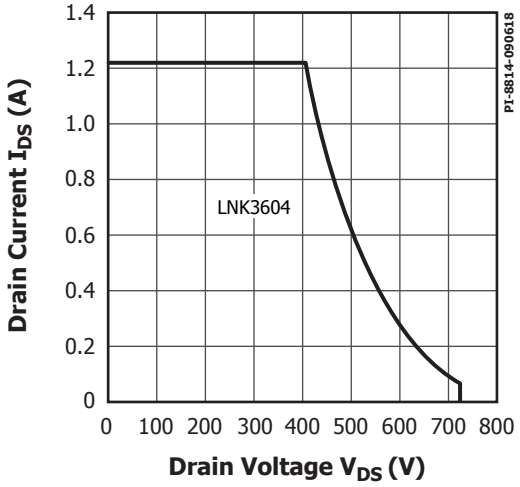


Figure 17. Maximum Allowable Drain Current vs. Drain Voltage.

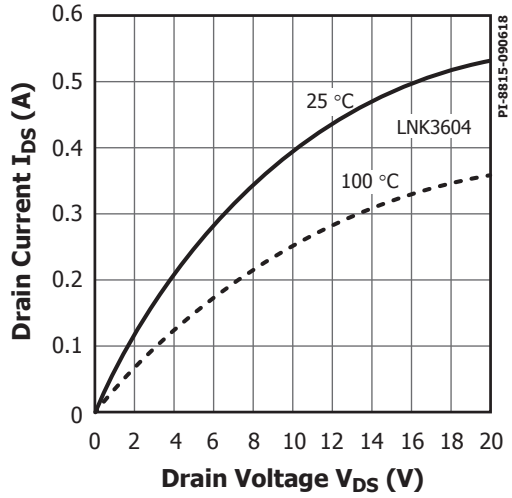


Figure 18. Output Characteristics.

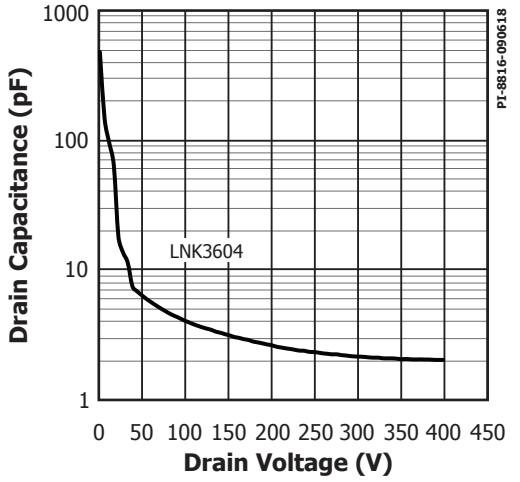


Figure 19. C_{OSS} vs. Drain Voltage.

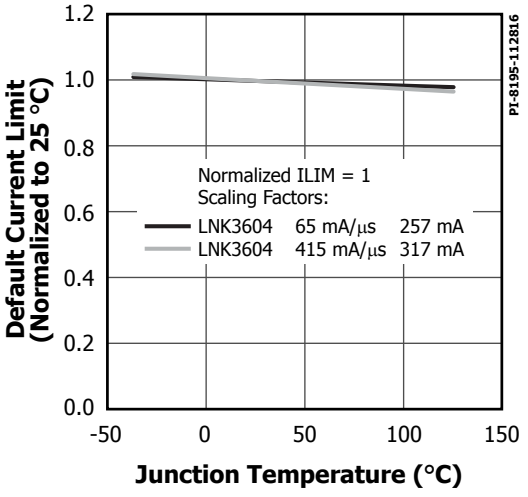


Figure 20. Default Current Limit vs. Junction Temperature.

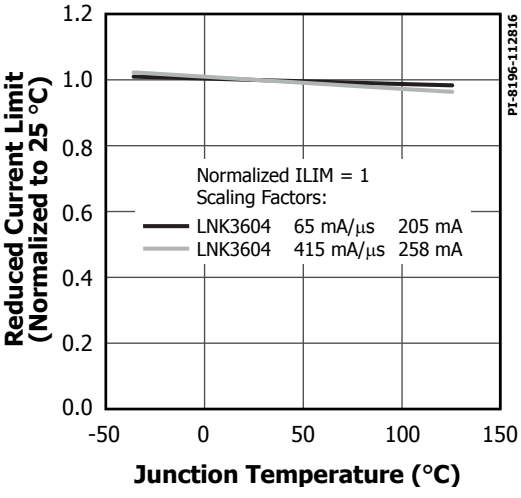


Figure 21. Reduced Current Limit vs. Junction Temperature.

Typical Performance Characteristics

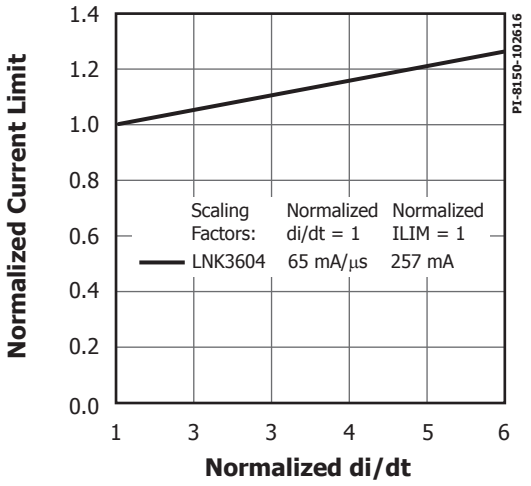


Figure 22. Default Current Limit vs. di/dt.

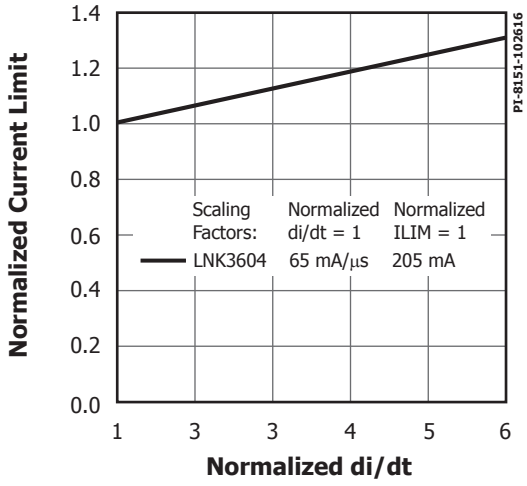


Figure 23. Reduced Current Limit vs. di/dt.

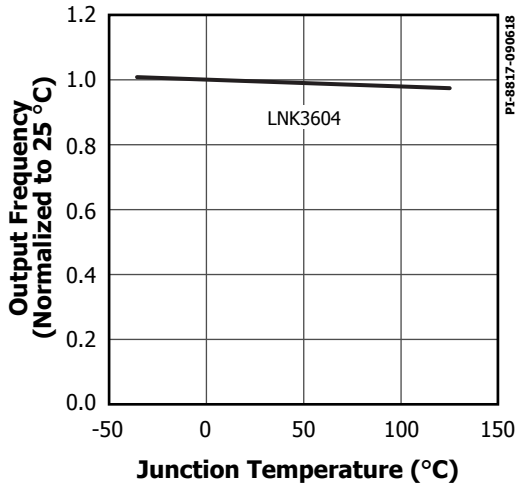


Figure 24. Output Frequency vs. Junction Temperature.

Typical Performance Characteristics

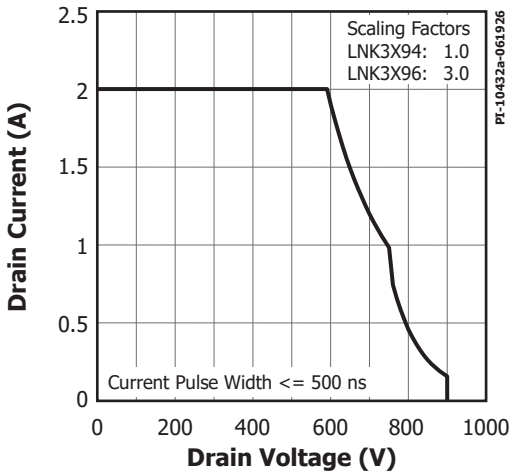


Figure 25. Maximum Allowable Drain Current vs. Drain Voltage.

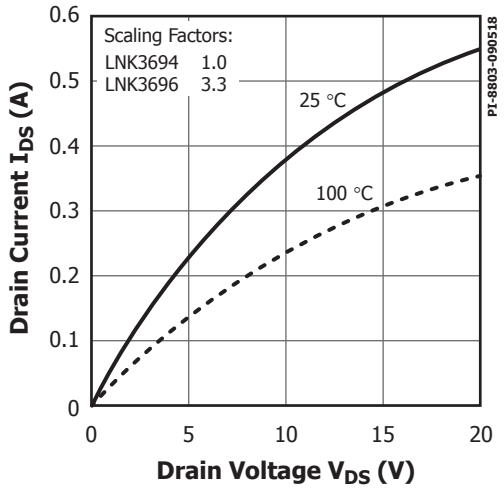


Figure 26. Output Characteristics.

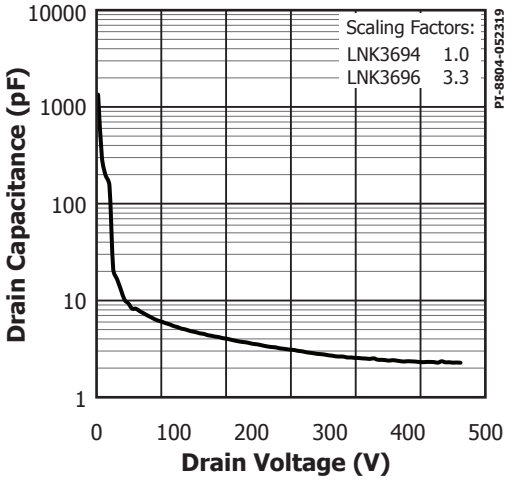


Figure 27. C_{OSS} vs. Drain Voltage.

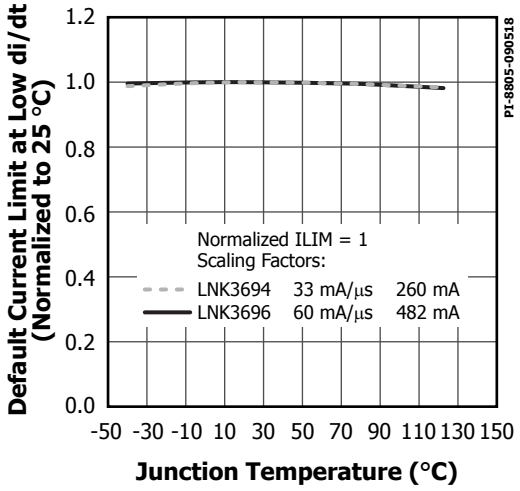


Figure 28. Default Current Limit vs. Junction Temperature.

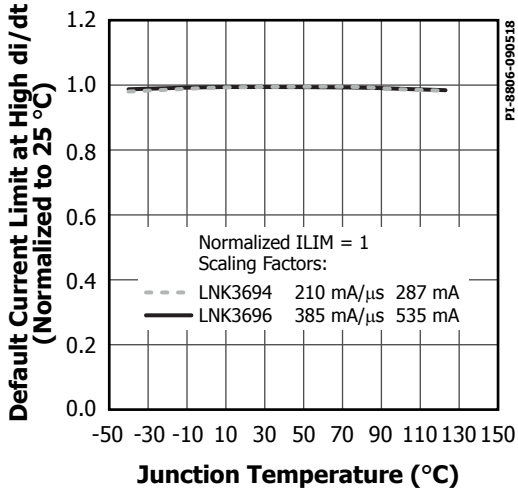


Figure 29. Default Current Limit vs. Junction Temperature.

Typical Performance Characteristics

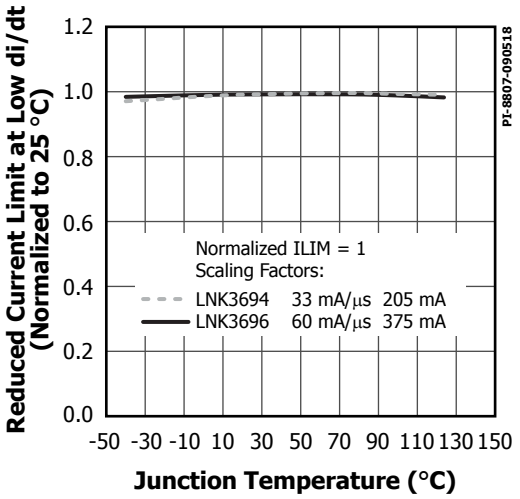


Figure 30. Reduced Current Limit vs. Junction Temperature.

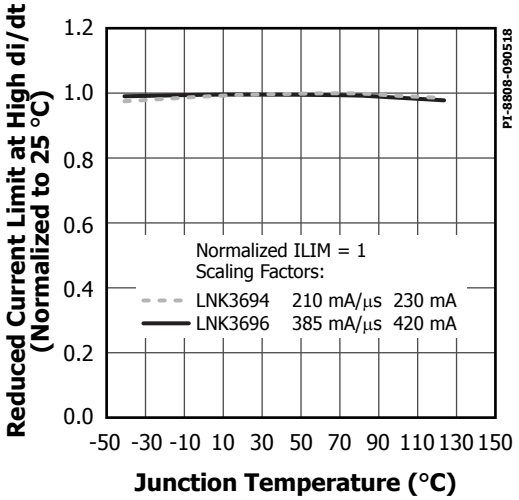


Figure 31. Reduced Current Limit vs. Junction Temperature.

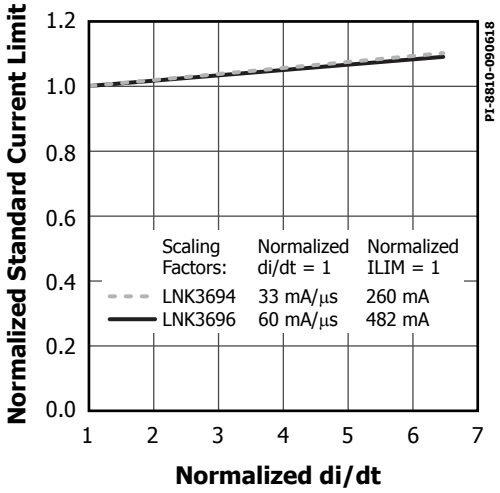


Figure 32. Standard Current Limit vs. di/dt.

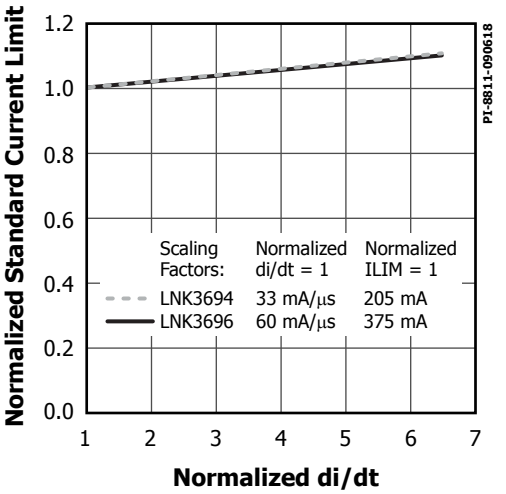


Figure 33. Reduced Current Limit vs. di/dt.

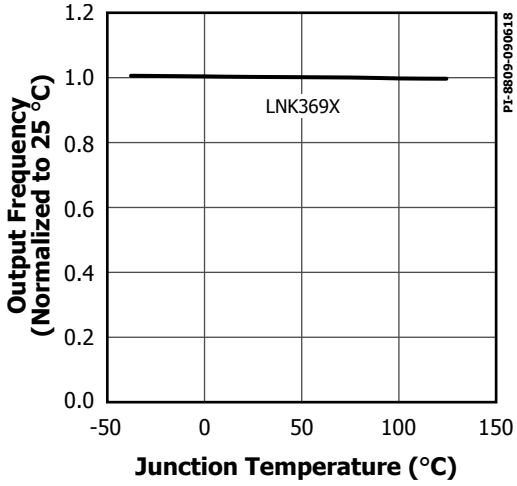
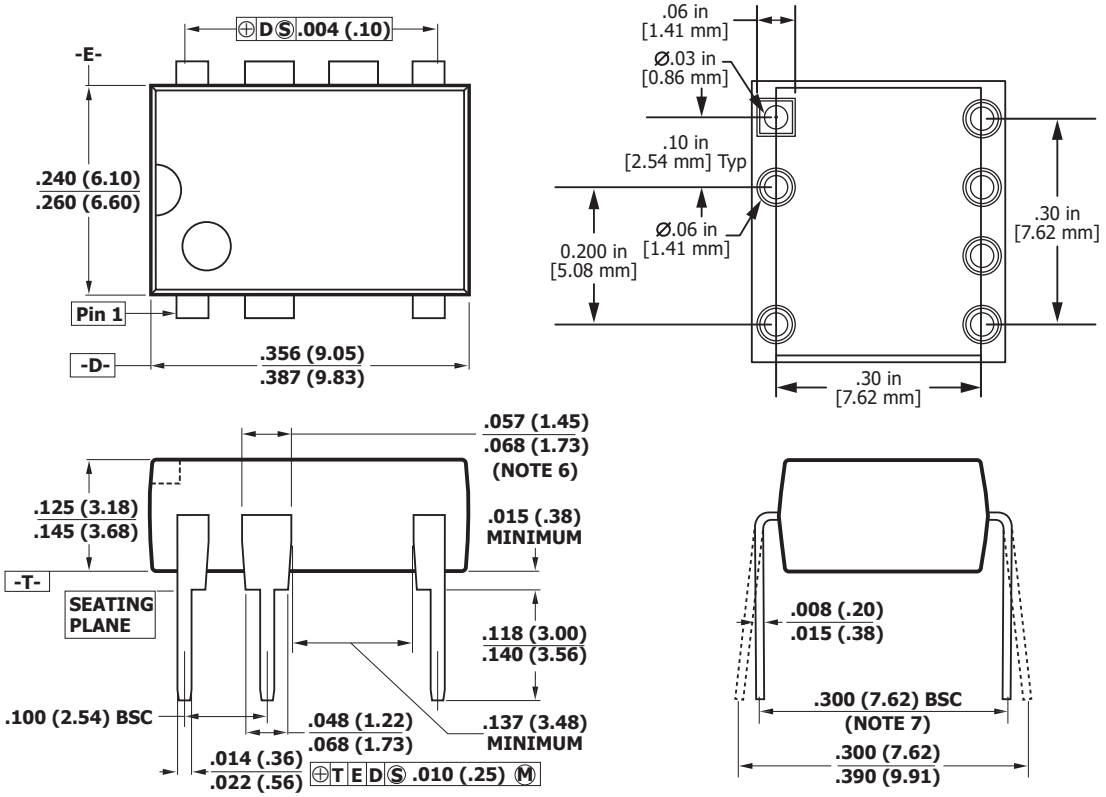


Figure 34. Output Frequency vs. Junction Temperature.

PDIP-8C (P Package)

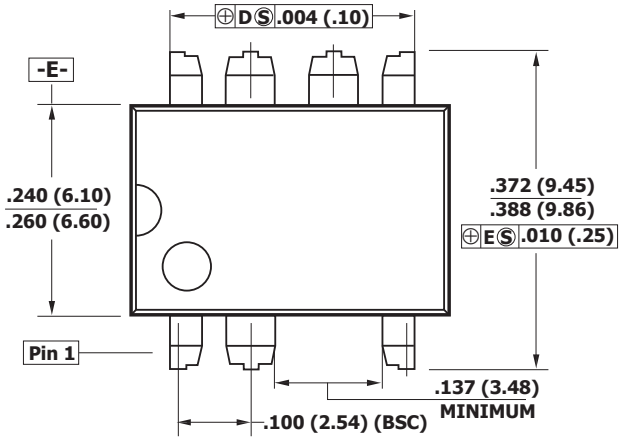


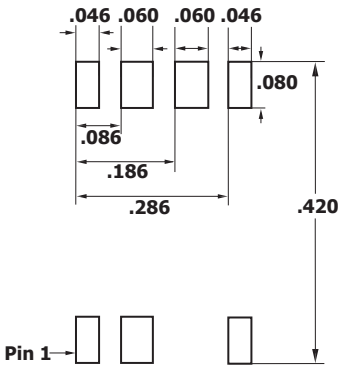
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.
2. Controlling dimensions are inches. Millimeter sizes are shown in parentheses.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. Pin locations start with Pin 1, and continue counter-clock-wise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.
5. Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).
6. Lead width measured at package body.
7. Lead spacing measured with the leads constrained to be perpendicular to plane T.

P08C

PI-3933b-092920

SMD-8C (G Package)

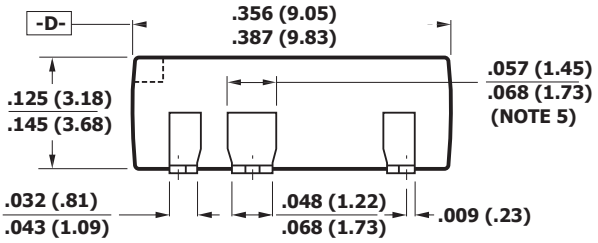


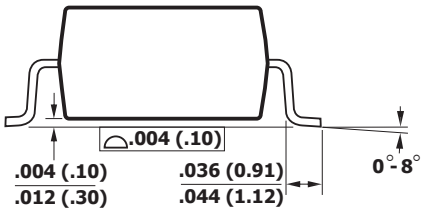


Solder Pad Dimensions

Notes:

1. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
2. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
3. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.**
4. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
5. **Lead width measured at package body.**
6. **D and E are referenced datums on the package body.**

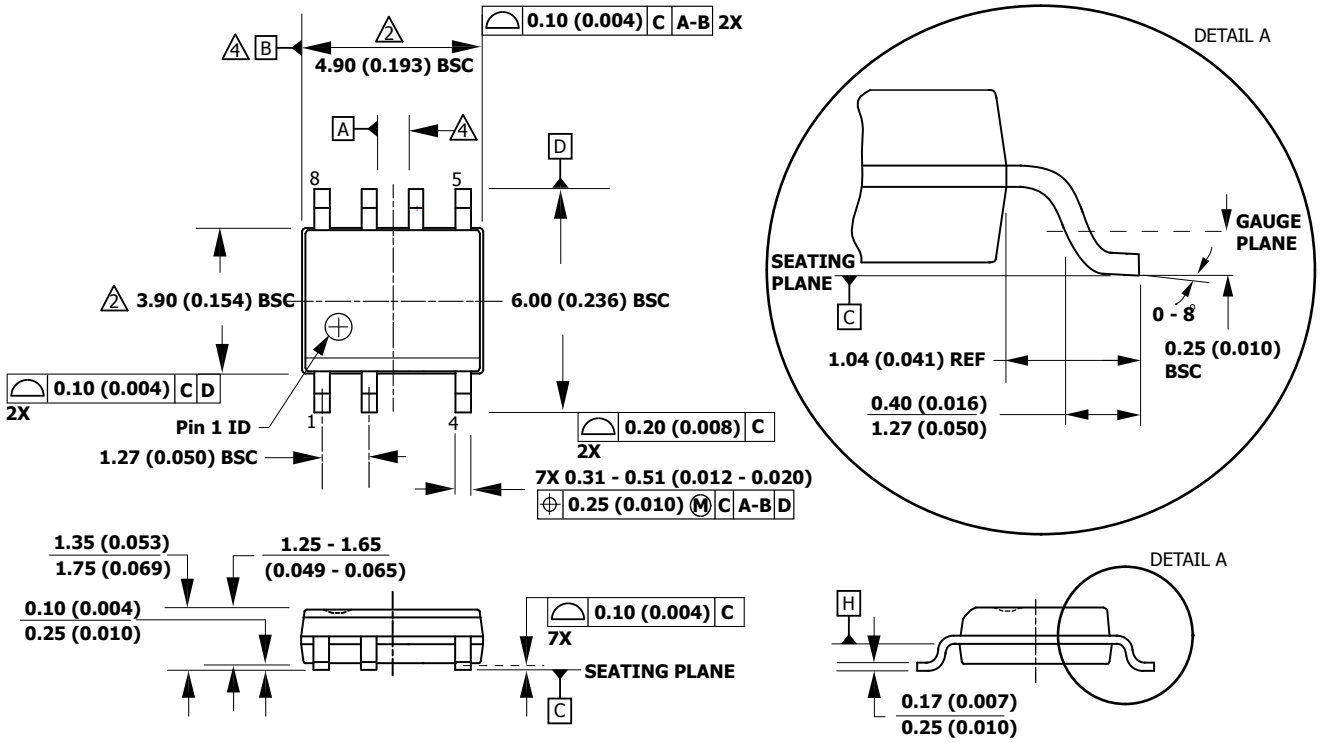




G08C

PI-4015b-072320

SO-8C (D Package)



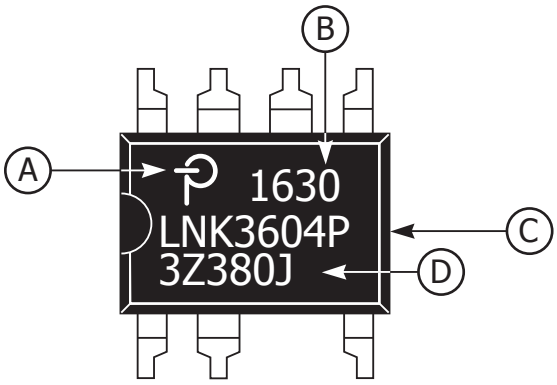
Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-012315

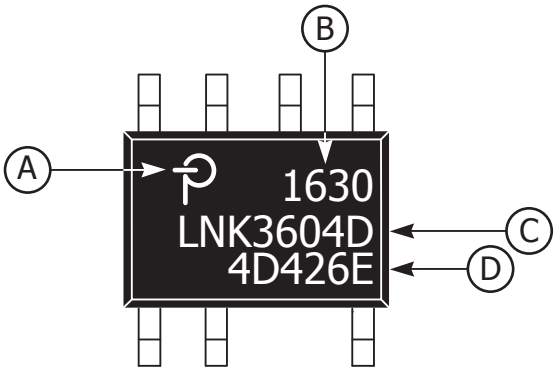
PDIP-8C (P) and SMD-8C (G) PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8127-100516

SO-8C (D) PACKAGE MARKING



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8126-100516

MSL Table

Part Number	MSL Rating
LNK3604P	N/A
LNK3694P	N/A
LNK3696P	N/A
LNK3604G	3
LNK3694G	3
LNK3696G	3
LNK3604D	1

ESD and Latch-Up

Test	Conditions	Results
Latch-up at 125 °C	EIA/JESD78	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	EIA/JESD22-A114-A	> ±2 kV on all pins
Machine Model ESD	EIA/JESD22-A115-A	> ±200 V on all pins

Part Ordering Information

LNK 3604 G - TL

- **LinkSwitch Product Family**
- **XT2 Series Number (725 V / 900 V)**
- **Package Identifier**
  - G — Plastic Surface Mount SMD-8C
  - P — Plastic PDIP-8C
  - D — Plastic SO-8C
- **Tape & Reel and Other Options**
  - TL — Tape and Reel, 1 k pcs minimum for G Package. 2.5 k pcs for D Package. Not available for P Package.

Revision	Notes	Date
A	Preliminary release.	10/16
B	Introduction release.	11/16
C	Production release.	11/16
D	Corrected DRAIN Pin Peak Current to match Figure 17 and Corrected Note 2 in Absolute Maximum Ratings.	01/06/17
D	Corrected Notes 1 and 2 in Table 1, updated Figure 5 and Reference Designator on page 5.	01/16/17
E	Added LNK3694 and LNK3696 parts.	09/18
F	Updated 900 V MOSFET VAC range in Table 1.	12/18
G	Updated ESD and Latch-Up table Results column.	04/19
H	Added Max values for I_{S2} and added I_{DSS2} at T_J - 125 °C	08/19
I	Updated ESD and Latch-Up table.	01/20
J	Updated per PCN-20321.	08/20
K	Updated package drawings PDIP-8C and SMD-8C.	10/20
L	Updated Minimum DRAIN Pin Supply Voltage.	06/23
M	Updated Drain Pin Peak Current value of LNK3694 and LNK3696 and Fg.25 and replaced with PI-10432a	06/26

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