InnoMux2-EP Family

Off-Line Zero Voltage Switching (ZVS) Flyback Switcher IC for Multi-Output Applications

Product Highlights

Highly Integrated, Compact Footprint

- Up to 3 independently regulated outputs using a single controller and transformer
  - Eliminates post regulators
- Incorporates a multi-mode Quasi-Resonant Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) flyback controller, 650 V, 725 V, 750 V or 1700 V power switch, secondary-side control and synchronous rectification driver
- Integrated FluxLink™ feedback link eliminates optocouplers
- Zero voltage switching (ZVS) using advanced SR FET control with DCM only mode
- Excellent transient response: <±5% CV with 100% load step
- Outputs up to 200 V for CV and CC (LED drive) configurations

EcoSmart™ – Energy Efficient

- PowiGaN™ technology enables >90% efficient power supplies
  - Designs easily meet global energy efficiency regulations
- Proprietary switching algorithm ensures high efficiency across load
- Low dissipation allows PCB cooling – no heat sinks required

Advanced Protection / Safety Features

- Primary sensed output OVP
- Open SR-FET gate detection
- Hysteretic thermal shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Overload protection for each output
- LED short / open protection

Full Safety and Regulatory Compliance[7]

- Reinforced isolation
- Isolation voltage >4000 VAC
- 100% production HIPOT tested
- UL1577 isolation voltage 4000 VAC (max), TUV (EN62368-1), CQC (GB4943.1) and DIN EN IEC 60747-17 (VDE 0884-17) See Note 7
- Enables designs required to meet class A performance criteria for EN61000-4 suite of test standards, including EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- High efficiency driver for monitors and TVs
  - Ideal for designs that need to meet Energy Star 8, CEC, and 2021/2023 EU labeling requirements
- High efficiency multi-output power supplies for industrial, smart-meter and appliance applications

Figure 5. Left - InnoMux2-EP in InSOP-24B Package.
Middle - InnoMux2-EP in InSOP-T28D/B Package.
Right - InnoMux2-EP in InSOP-T28G Package.

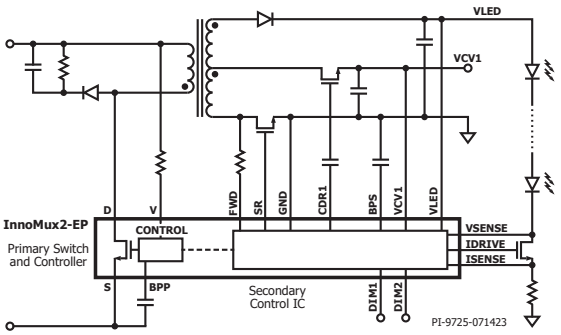


Figure 1. Typical Application with LED Driver. (IMX2353F (1700 V) does not support LED Driver)

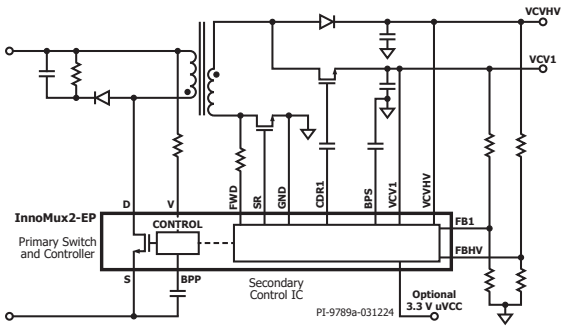


Figure 2. Typical Application with Two Constant Voltages.

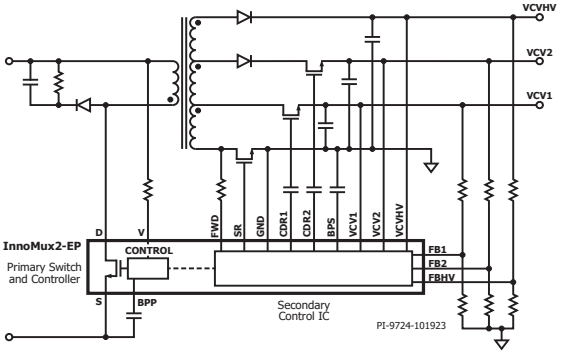


Figure 3. Typical Application with Three Constant Voltages.

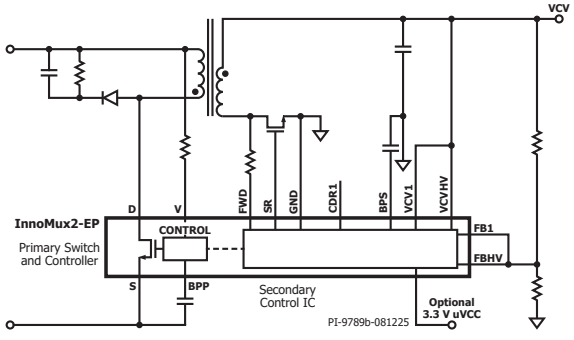


Figure 4. Typical Application with One Output.

Output Power Table

Product	1 CV & 1 CC Output[6]		
	230 VAC ±15%[1]	**85-265 VAC[1]**	**385 VDC (PFC Input)**
650 V MOSFET			
IMX2267C[2]	40 W	36 W	
IMX2268C[2]	55 W	50 W	
750 V PowiGaN Switch		**Up to 3 CV Outputs[6]**	
IMX2278F[4]	77 W	60 W	85 W
IMX2279F[4]	88 W	70 W	97 W
IMX2270F[4]	100 W	80 W	110 W
725 V MOSFET			
IMX2174F[3]	20 W	15 W	
IMX2175F[3]	25 W	20 W	
IMX2176F[3]	35 W	27 W	
IMX2177F[3]	40 W	36 W	
750 V PowiGaN Switch			
IMX2378F[3]	70 W	55 W	77 W
IMX2379F[3]	80 W	65 W	88 W
IMX2370F[3]	90 W	75 W	100 W
1700 V PowiGaN Switch			
	85-670 VAC Peak or Open Frame[1]		**300-1000 VDC Peak or Open Frame[1]**
IMX2353F[5]	55 W		100 W

Table 1. InnoMux2-EP Controller Part Numbers.

1. Continuous power using nominal primary current limit in a typical open frame application at +50 °C ambient with adequate PCB thermal design to ensure package temperature <125 °C.
2. InSOP-24B (C) exposed pad.
3. InSOP-T28D (F).
4. InSOP-T28B (F) exposed pad.
5. InSOP-T28G (F).
6. Use Feature Code table on page 39 when selecting parts with 1 or 2 CV outputs. Parts with no feature code are configured to support 3 CV output designs.
7. Contact PI for Information on UL, TUV, CQC and DIN EN IEC 60747-17.

Description

The InnoMux™2-EP IC dramatically improves power conversion efficiency. By independently regulating and protecting each output the InnoMux2-EP family eliminates multiple downstream conversion stages. InnoMux2-EP IC-based designs have low BOM count and small size. The family incorporates both primary and secondary-side controllers, with protection, sense elements and a safety-rated feedback mechanism (FluxLink) into a single IC. The InnoMux2-EP IC also includes an LED backlight controller that supports multi-mode dimming making it ideal for monitors, TVs and appliances with lighting or display requirements.

The InnoMux2-EP IC contains enhanced features for maximizing conversion efficiency including quasi-resonant switching in DCM operation, accurate SR control and minimum-threshold-regulation for the LED driver.

Configuration Options

Part No.	Switch Rating	Continuous Power	Peak Power[1]	Output	CV1[2]	Maximum V_{LED}[2]	V_{SENSE} Voltage[2]	SR MOSFET Driver	Dimming Interface[2]	Package
IMX2267C	650 V	36 W[1]	57 W	1 CV, 1 CC	12 V	80 V	0.8 V	No	2-Pin Filtered PWM/ Hybrid Dimming	InSOP-24B
IMX2268C	650 V	50 W[1]	80 W	1 CV, 1 CC	12 V	80 V	0.8 V	No	2-Pin Filtered PWM/ Hybrid Dimming	InSOP-24B
IMX2278F	750 V	60 W[1]	94 W	1 CV, 1 CC	12 V	140 V	0.9 V	Yes	2-Pin Filtered PWM/ Hybrid Dimming	InSOP-T28B
IMX2279F	750 V	70 W[1]	110 W	1 CV, 1 CC	12 V	150 V	1.0 V	Yes	2-Pin Filtered PWM/ Hybrid Dimming	InSOP-T28B
IMX2270F	750 V	80 W[1]	130 W	1 CV, 1 CC	12 V	170 V	1.0 V	Yes	2-Pin Filtered PWM/ Hybrid Dimming	InSOP-T28B
IMX2174F	725 V	15 W[1]		2 CV[3]				Yes		InSOP-T28D
IMX2175F	725 V	22 W[1]		2 CV[3]				Yes		InSOP-T28D
IMX2176F	725 V	27 W[1]		2 CV[3]				Yes		InSOP-T28D
IMX2177F	725 V	36 W[1]		2 CV[3]				Yes		InSOP-T28D
IMX2378F	750 V	55 W[1]		3 CV[4]				Yes		InSOP-T28D
IMX2379F	750 V	65 W[1]		3 CV[4]				Yes		InSOP-T28D
IMX2370F	750 V	75 W[1]		3 CV[4]				Yes		InSOP-T28D
IMX2353F	1700 V	100 W[5]		3 CV[6]				Yes		InSOP-T28G

Table 2. Configuration Options.

1. 85 – 265 VAC.
2. These parameters can be configured to other values.
3. Can be configured to 3 CV.
4. Can be configured to 2 CV.
5. 300 – 1000 VDC.
6. Also available on 2 CV. See Feature Code Table.

Block Diagrams

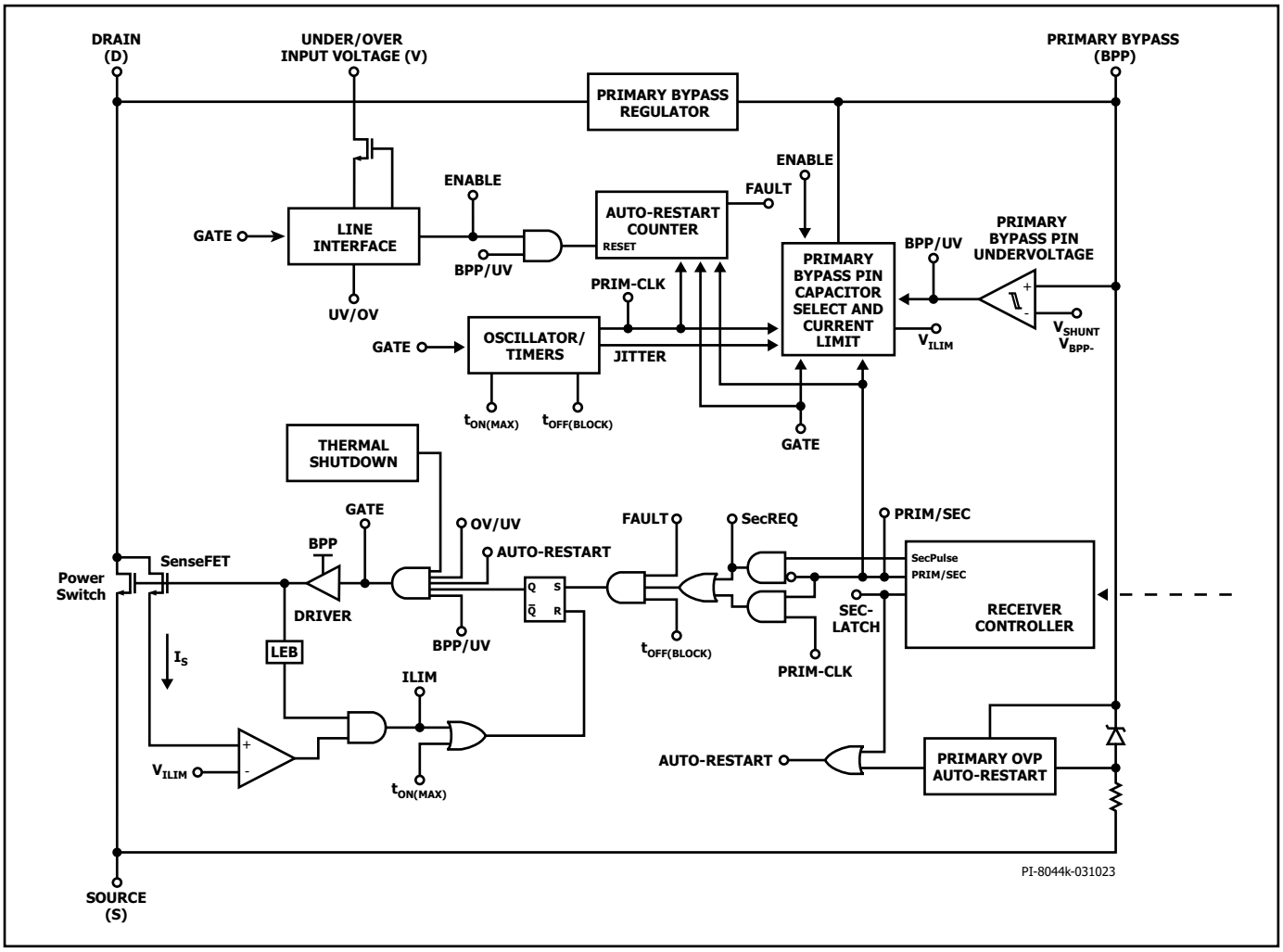


Figure 6. InnoMux2-EP Primary Block Diagram.

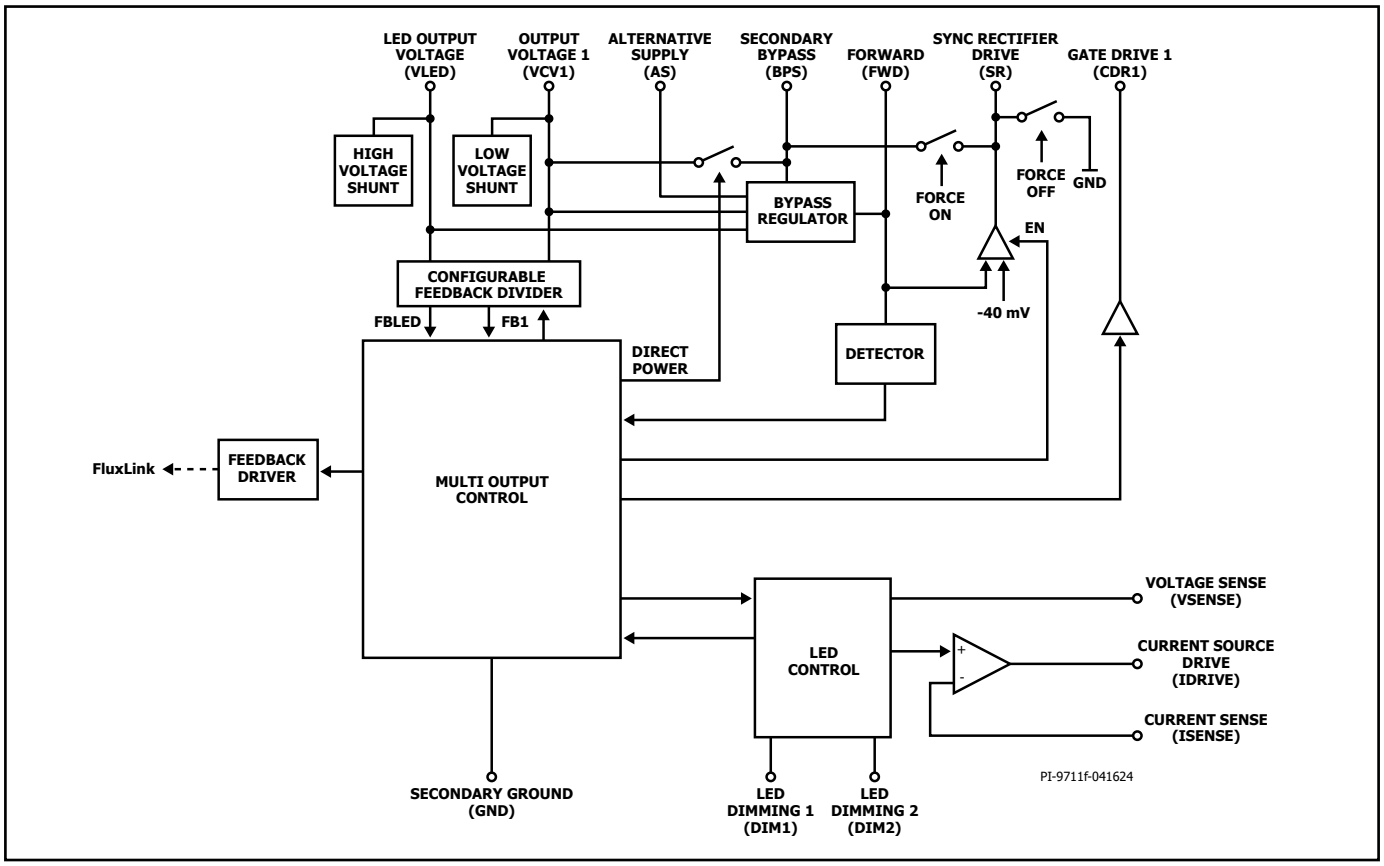


Figure 7. InnoMux2-EP Secondary Block Diagram LED Configuration. (Not applicable for IMX2353F)

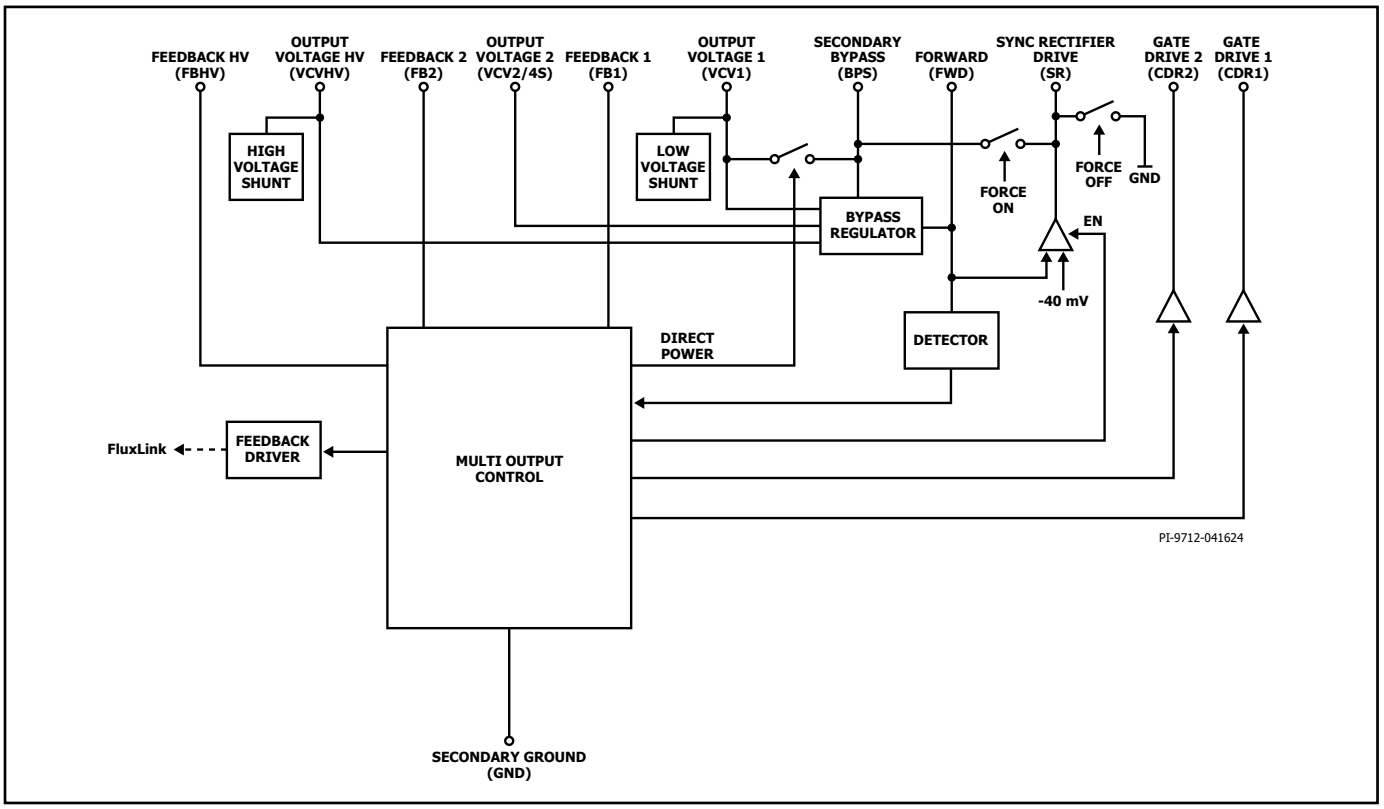


Figure 8. InnoMux2-EP Secondary Block Diagram CV Configuration.

Pin Functional Description IMX226xC

InnoMux2-EP InSOP-24B 1CV+1LED Dual Dimming Pin Configuration

CURRENT SENSE (ISENSE) Pin (Pin 1)
Connection to external LED driver MOSFET source terminal for sensing LED current. An external current sense resistor should be connected between this and the GND pin.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

CURRENT SOURCE DRIVE (IDRIVE) Pin (Pin 3)
Connection to external LED driver MOSFET gate terminal for controlling LED current.

VOLTAGE SENSE (VSENSE) Pin (Pin 4)
Connection to external LED driver MOSFET Drain terminal for regulation of voltage to minimise MOSFET power dissipation.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for the V_{CV1} output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor which supplies power to the secondary side of the IC.

LED DIMMING 2 (DIM2) Pin (Pin 7)
LED dimming control input.

LED DIMMING 1 (DIM1) Pin (Pin 8)
LED dimming control input.

FORWARD (FWD) Pin (Pin 9)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 10)
Connected directly to the V_{CV1} output voltage, to provide current for the controller on the secondary-side and provide sensing for output voltage regulation and protection.

LED OUTPUT VOLTAGE (VLED) Pin (Pin 11)
Connected directly to the LED output voltage, to provide current for the controller on the secondary-side and provide sensing of LED voltage for overvoltage protection.

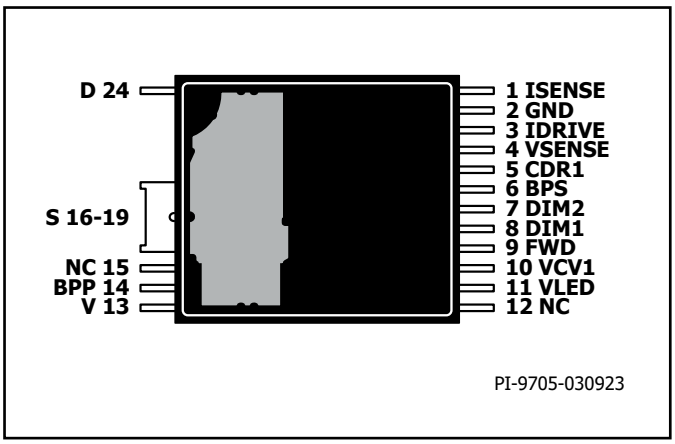


Figure 9. InnoMux2-EP InSOP-24B 1CV+1LED Dual Dimming Pin Configuration (Bottom View).

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to the SOURCE pin to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor of the primary-side supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

NC Pin (Pin 15)
Leave open or connect to the SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch SOURCE connection. Also ground reference for the primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power switch Drain connection.

SOURCE (S) Exposed Pad (InSOP-24B Only)
Power switch SOURCE connection. Also ground reference for the primary BYPASS pin. Connect all SOURCE pins together. Used to enhance thermal management.

InnoMux2-EP InSOP-T28B 1CV+1LED Dual Dimming with SR Pin Configuration IMX227xF

CURRENT SENSE (ISENSE) Pin (Pin 1)
Connection external LED driver MOSFET source terminal for sensing LED current. An external current sense resistor should be connected between this and the GND pin.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

CURRENT SOURCE DRIVE (IDRIVE) Pin (Pin 3)
Connection to external LED driver MOSFET gate terminal for controlling LED current.

VOLTAGE SENSE (VSENSE) Pin (Pin 4)
Connection to external LED driver MOSFET Drain terminal for regulation of voltage to minimise MOSFET power dissipation.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for V_{CV1} output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor which supplies power to the secondary side of the IC.

LED DIMMING 2 (DIM2) Pin (Pin 7)
LED dimming control input.

LED DIMMING 1 (DIM1) Pin (Pin 8)
LED dimming control input.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver for external SR MOSFET.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 11)
Connected directly to the V_{CV1} output voltage, to provide current for the controller on the secondary-side and provide sensing for output voltage regulation and protection.

ALTERNATIVE SUPPLY (AS) (Pin 12)
Alternative supply input for the controller on the secondary-side. Can be left open if not in use

LED OUTPUT VOLTAGE (VLED) Pin (Pin 13)
Connected directly to the LED output voltage, to provide current for the controller on the secondary-side and provide sensing of LED voltage for overvoltage protection.

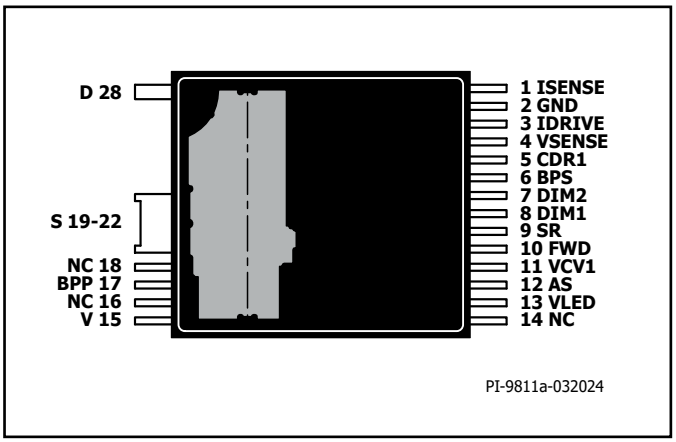


Figure 10. InnoMux2-EP InSOP-T28B 1CV+1LED Dual Dimming with SR Pin Configuration (Bottom View).

NC Pin (Pin 14)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 15)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

NC Pin (Pin 16)
Leave open or connect to SOURCE pin or BPP pin.

PRIMARY BYPASS (BPP) (Pin 17)
The connection point for an external bypass capacitor of the primary-side supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

NC Pin (Pin 18)
Leave open. Should not be connected to any other pins.

SOURCE (S) Exposed Pad (InSOP-T28B Only)
Power switch SOURCE connection. Also ground reference for primary BYPASS pin. Connect all SOURCE pins together. Used to enhance thermal management.

DRAIN (D) Pin (Pin 28)
Power switch Drain connection.

InnoMux2-EP InSOP-T28D 3CV / 2CV Pin Configuration IMX217xF, IMX237xF

FEEDBACK 1 (FB1) Pin (Pin 1)
Connection to an external resistor divider to set the power supply output voltage of V_{CV1}.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

FEEDBACK 2 (FB2) Pin (Pin 3) / NC for 2CV output
Connection to an external resistor divider to set the power supply output voltage of V_{CV2}. Not used for 2CV, leave open should not be connected to any other pins.

NC Pin (Pin 4)
Leave open. Should not be connected to any other pins.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for V_{CV1} output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor for the secondary IC supply.

GATE DRIVE 2 (CDR2) Pin (Pin 7) / NC for 2 CV Output
Gate driver for external selection MOSFET for V_{CV2} output. Not used for 2CV output, leave open, should not be connected to any other pins.

FEEDBACK HV (FBHV) Pin (Pin 8)
Connection to an external resistor divider to set the power supply output voltage of V_{CVHV}.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver for external SR MOSFET.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 11)
Connected directly to the V_{CV1} output voltage, to provide current for the controller on the secondary-side and for protection.

OUTPUT VOLTAGE 2 (VCV2/AS) Pin (Pin 12)
Connected directly to the V_{CV2} output voltage, to provide current for the controller on the secondary-side. Alternative supply as input for 2CV configuration. Can be left open if not in use.

OUTPUT VOLTAGE HV (VCVHV) Pin (Pin 13)
Connected directly to the V_{CVHV} output voltage, to provide current for the controller on the secondary-side and for protection.

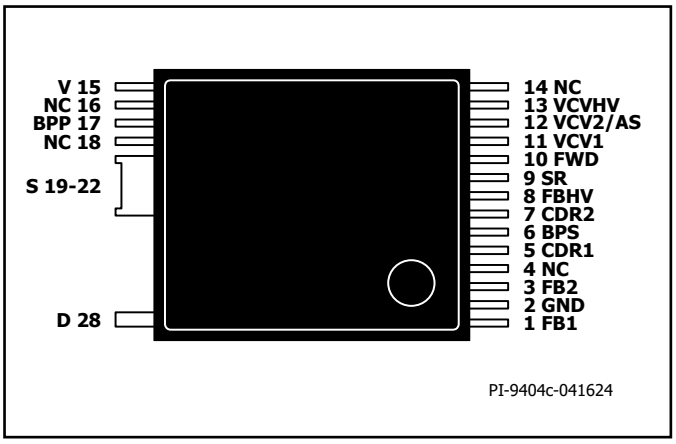


Figure 11. InnoMux2-EP InSOP-T28D 3CV / 2CV Pin Configuration.

NC Pin (Pin 14)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 15)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

NC Pin (Pin 16)
Leave open or connect to SOURCE pin or BPP pin.

PRIMARY BYPASS (BPP) (Pin 17)
The connection point for an external bypass capacitor of the primary-side supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

NC Pin (Pin 18)
Leave open. Should not be connected to any other pins.

SOURCE (S) Pin (Pin 19-22)
These pins are the power switch SOURCE connection. Also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 28)
Power switch Drain connection.

InnoMux2-EP 2CV/3CV Pin Configuration IMX2353F

FEEDBACK 1 (FB1) Pin (Pin 1)
Connection to an external resistor divider to set the power supply output voltage of VCV1. Not used with internal feedback*.

SECONDARY GROUND (GND) Pin (Pin 2)
GND for the secondary IC.

FEEDBACK 2 (FB2) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage of VCV2. Not used in 2CV configuration or in combination with internal feedback*.

NC Pin (Pin 4)
Leave open. Should not be connected to any other pins.

GATE DRIVE 1 (CDR1) Pin (Pin 5)
Gate driver for external selection MOSFET for VCV1 output.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Connection for external bypass capacitor for the secondary IC supply.

GATE DRIVE 2 (CDR2) Pin (Pin 7)
Gate driver for external selection MOSFET for VCV2 output. Not used in 2CV configuration.

FEEDBACK HV (FBHV) Pin (Pin 8)
Connection to an external resistor divider to set the power supply output voltage of VCVHV.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver for external SR MOSFET.

FORWARD (FWD) Pin (Pin 10)
The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller during start-up.

OUTPUT VOLTAGE 1 (VCV1) Pin (Pin 11)
Connected directly to the VCV1 output voltage, to provide current for the controller on the secondary-side and for protection.

OUTPUT VOLTAGE 2 (VCV2/AS) Pin (Pin 12)
Connected directly to the V_{CV2} output voltage, to provide current for the controller on the secondary-side. Alternative supply as input for 2CV configuration. Can be left open if not in use.

OUTPUT VOLTAGE HV (VCVHV) Pin (Pin 13)
Connected directly to the VCVHV output voltage, to provide current for the controller on the secondary-side and for protection.

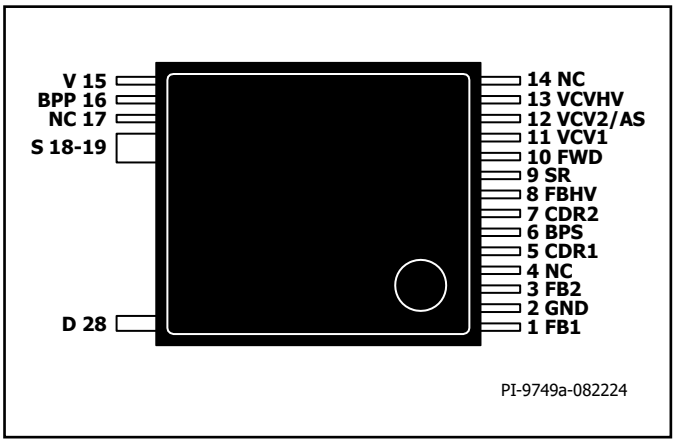


Figure 12. InnoMux2-EP InSOP-T28G 3CV Pin Configuration.

NC Pin (Pin 14)
Leave open. Should not be connected to any other pins.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 15)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting undervoltage and overvoltage conditions at the power supply input. This pin should be tied to SOURCE pin to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 16)
The connection point for an external bypass capacitor of the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 17)
Leave open. Should not be connected to any other pins.

SOURCE (S) Pin (Pin 18-19)
These Pins are the power switch source connection. Also ground reference for primary BYPASS pin..

DRAIN (D) Pin (Pin 28)
Power switch drain connection.

InnoMux2-EP Functional Description

The InnoMux2-EP combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device. The InnoMux2-EP architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to accurately communicate power requests from the secondary controller to the primary controller.

The primary controller on InnoMux2-EP is a quasi-resonant (QR) flyback controller to operate in continuous conduction mode (CCM) or discontinous conduction mode (DCM) with Zero voltage switching (ZVS) using advanced SR FET control. The controller uses a variable current control scheme. The primary consists of a jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, overvoltage protection, leading edge blanking, secondary output diode / SR MOSFET short protection circuit and a 650 V / 725 V / 750 V and 1700 V power switch.

The secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, multi-output controller for regulating up to three outputs independently, 5 V regulator on the SECONDARY BYPASS pin, synchronous rectifier (SR) MOSFET driver, high-side MOSFET drivers, shunts to prevent individual outputs from rising in abnormal loading conditions, single string LED driver, timing functions and a host of integrated protection features.

Figures 4, 5 and 6 show the functional block diagrams of the primary and secondary controllers with the most important features.

Primary Controller

The InnoMux2-EP IC has variable frequency CCM / CrM / DCM controller plus ZVS operation in DCM for enhanced efficiency and extended output power capability.

For high-voltage input, the 1700 V InnoMUX2-EP (IMX2353F) has a variable frequency DCM only controller plus SR ZVS operation. This DCM ZVS operation achieves zero voltage switching on the primary switch using SR MOSFET. This reduces the capacitive turn on loss and improves efficiency.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoMux2-EP IC to be powered externally through a bias winding, decreasing the no-load consumption and enhancing low-standby-power operation.

Primary Bypass I_{LIM} Programming

InnoMux2-EP ICs allow the user to adjust primary current limit (I_{LIM}) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used. There are 2 selectable capacitor sizes – 0.47 µF and 4.7 µF for setting standard and increased I_{LIM} settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (= $V_{BPP} – V_{BPP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to $V_{BPP(SHUNT)}$ to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has an OV protection feature with either a latching or an auto-reset response. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

Output OV protection is also included as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin $UV_{(IUV-)}$ threshold.

Over-temperature protection is also included as an integrated feature on the secondary controller.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle) to the next switching request.

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 12).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current per cycle approaches 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to prevent audible noise). The time between switching cycles will continue to increase as load reduces.

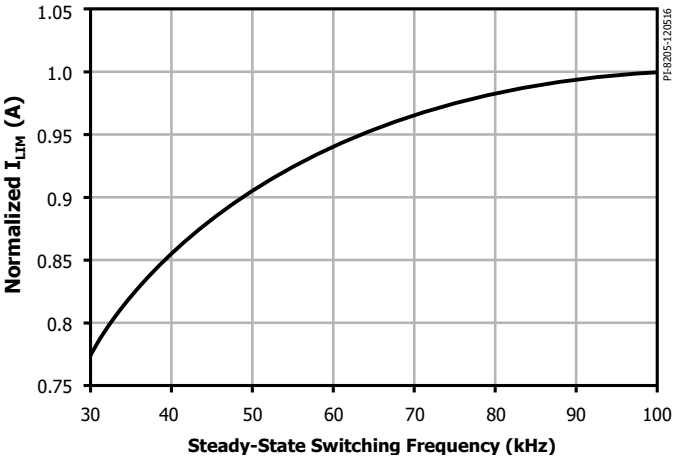


Figure 13. Normalized Primary Current vs. Switching Frequency.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M; this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoMux2-EP enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~3 V or by going below the UNDER/OVER INPUT VOLTAGE pin $UV_{(IUV-)}$ threshold.

During the first auto-restart after initial power up, switching of the power MOSFET is disabled for $t_{AR(OFF)SH}$. During subsequent auto-restart events, switching of the power MOSFET is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests received at a rate that is above the overload detection frequency (f_{OVL}) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for >$t_{AR(SK)}$.

The secondary controller can initiate an auto-restart by not sending switching request cycles to the primary controller. The primary controller will then restart.

It is also possible that communication is lost, in which case the primary will also try to restart. Although this should never be the case in normal operation, it can be useful when system ESD events(for example) cause a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where the I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs. This provides sufficient time for the transformer to reset when operating with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND. Please note the maximum voltage for this UNDER/OVER INPUT VOLTAGE pin is 650 V; for above 650 V input DC voltage, an additional external clamp circuit is needed to clamp this pin voltage below 650 V.

At power-up, after the primary bypass capacitor is charged and the I_{LIM} state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-out for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of an internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage MOSFET will disconnect the external sense resistor from the internal sense circuits to eliminate current drawn through the sense resistor. The line sensing function will reactivate at the beginning of the next switching cycle.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™, LinkSwitch™ and other InnoSwitch™ controllers).

If no feedback signals are received during the auto-restart time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up from the FORWARD pin or output voltage and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests, or if the secondary detects that the primary is switching without cycle requests, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoMux2-EP IC features an active audible noise reduction mode where by the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz – 142 µs and 83 µs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

The secondary controller includes an audible-noise-reduction engine.

Frequency Soft-Start

At start-up (before handshake) the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

Secondary Controller

The IC is powered by the 5 V (V_{BPS}) regulator which is supplied by either an output or FORWARD pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the detection block used for both handshaking and timing circuit to turn on and regulate the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation.

In continuous conduction mode (CCM) the SR FET is turned off when a feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The FORWARD detector also measures the FORWARD pin voltage during the primary on time, this feeds into the SR zero voltage switching control function.

BPS Regulator

The regulator limits the BPS pin to V_{BPS}. The BP regulator can use V_{CV1} or $V_{CV2/AS}$ as its source. The source is automatically selected as follows:

- V_{CV1} is used if VCV1 pin > V_{BPS_VCV1}, otherwise
- $V_{CV2/AS}$ is used if VCV2 pin > V_{BPS_VCV2}

V_{CVHV}/V_{LED} can only be used as a source for BPS during start-up.During start-up, the FORWARD pin is also used as a source for BPS. This is provided to support start-up into heavy load and is not intended for continuous operation. The FORWARD pin needs to be a minimum of ≈8 V when the primary is on in order for this to function correctly.

A 2.2 µF or 4.7 µF ceramic capacitor on the BPS pin is required. There are no stability requirements on the capacitor; the BPS regulator is unconditionally stable.

BPS Regulator – Direct Power

When V_{CV1} is 5 V (V_{CV5V_BPS}) the BPS pin is automatically connected internally to the VCV1 pin, directly powering BPS instead of using the BPS linear regulator. This reduces power loss in the secondary controller and reduces standby power. This is automatically selected when V_{CV1} is V_{CV5V_BPS}.

High-Side MOSFET Drive

The high-side selection MOSFETs are driven with a drive voltage that is 5 V above the given output using a capacitive drive approach. The capacitive drive approach benefits from easy level translation by use of a capacitor CDR capacitor-drive (CDR) . A regular refresh cycle to top up the charge on the CDR is needed when one of the switches has been on for a long time, as the charge on the CDR will otherwise slowly leak away. Refresh is also needed during start-up to allow the CDR to follow the output voltage when the output is being pulled up. The controller will perform refresh cycles when necessary by turning the selection MOSFET off and then back on.

The default refresh time is $T_{REFRESH}$, which is doubled to 2 × $T_{REFRESH}$ during start-up. The longer the refresh time the better, but the MOSFET needs to be turned back on before the end of the primary on time. Once the CV outputs are in regulation the refresh time is reduced to $T_{REFRESH}$. Because the output is no longer changing, the refresh is only needed to top up CDR and by reducing the refresh time the risk of the primary on time finishing before the refresh is reduced.

A diode is required to be placed between the gate-source of each selection MOSFET to provide a path for charging the capacitor. A low forward voltage diode such as a Schottky diode should be used.

The optimal capacitor value for CDR depends on the gate charge of the selection MOSFET. The selection MOSFET on-level gate voltage is determined by $V_{BPS} \times (C_{DR}/(C_G + C_{DR})$, so it is essential that the gate charge (at 5 V gate voltage) is much smaller than the charge in the CDR capacitor. A typical value for the CDR capacitor is 100 nF. For higher CDR capacitor values, the refresh time might be insufficient and the capacitor will not be able to follow the output during start-up. It is therefore important to select low gate-charge devices for the selection MOSFETs to minimise the required CDR capacitor value as well as to minimise energy required to drive the MOSFETs.

High-Side MOSFET Static Pull-Down

To ensure that the selection MOSFET gates are held low when the secondary is not in control, the CDR1 and CDR2 pins have an internal pull down circuit "ON" feature to pull the pin low and reduce any voltage on the gate due to capacitive coupling.

Synchronous Rectifier Driver

The SR driver on the InnoMux2-EP IC is not an "on/off" driver. The SR MOSFET's gate-source voltage is modulated to regulate the FORWARD pin voltage to roughly -40 mV while the discharge current is flowing in the SR MOSFET. The regulated approach allows for improved noise immunity, removing the possibility of the MOSFET being turned off too early causing increased power loss.

A force-on signal provides a boost when turning on the SR MOSFET to charge the gate-source capacitance quickly. A force off signal is used to quickly discharge the gate-source capacitance when operating in CCM and also ensure the MOSFET is held off when the secondary is not conducting.

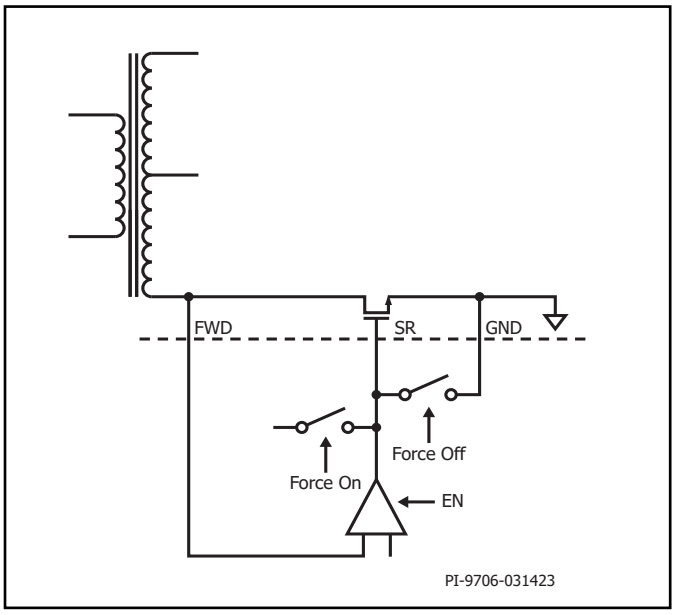


Figure 14. Synchronous Rectifier Driver Diagram.

For optimum performance, an SR MOSFET with a gate-source capacitance of less than 10 nF is recommended.

SR Disable Protection

In each cycle the SR is only engaged if a new cycle is requested by the secondary controller and the negative edge is detected on the FORWARD pin.

SR Static Pull-Down

To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has internal pull down circuit "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Short/Open SR Protection

In order to protect against the SYNCHRONOUS RECTIFIER DRIVE pin system faults, (an SR pin short to ground or SR pin open), the secondary controller has a protection mode that ensures that the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is less than 200 pF, the device will assume that the SYNCHRONOUS RECTIFIER DRIVE pin is "open". If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is above 20 nF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "short". In either of these two cases a fault is detected otherwise the controller will assume an SR FET is connected.

In the event SYNCHRONOUS RECTIFIER DRIVE pin fault is detected the secondary controller will stop requesting pulses from the primary and initiate auto-restart.

Multi-Output Control

The multi-output control regulates each output independently by requesting pulses from the primary based on the FB pin voltages of each output. The transformer energy is then directed to the output that needs the energy on a cycle-by-cycle basis. This is accomplished by turning on the appropriate selection MOSFET in series with either the CV1 or the CV2 output. The transformer shall be designed such that the V_{OR} increases between V_{CV1} and V_{CV2} and between V_{CVHV}/V_{LED}. This guarantees that the current through the V_{LED} diode is negligible when the selection MOSFET for either V_{CV1} or V_{CV2} is turned on, disabling both MOSFETs will direct the energy delivery to the LED output.

InnoMux2-EP Enhanced Audible Noise Reduction

The InnoMux2-EP IC has enhanced features for audible noise reduction.

Multi-output control can create sub-harmonic frequencies of the switching frequency in the flux of the transformer. These sub-harmonics can fall in the audible range. THE InnoMux2-EP IC avoids such conditions by sharing fractions of discharge pulses between outputs.

This is achieved by allowing the first part of the discharge pulse to the V_{CVHV}/V_{LED} output and then turning on the selection MOSFET part way through the discharge and allowing the second part of the discharge to flow via the V_{CV1} or V_{CV2} output. The point at which the MOSFET is turned on to switch over from the L_{ED}/C_{VHV} output to the CV1 or CV2 output is dependent on the relative loading of the outputs.

This provides an added benefit of reducing the RMS currents in the secondary windings, reducing power loss. The operating frequency of each output is increased (while the power switch frequency remains the same) reducing the output ripple for a given filter capacitance.

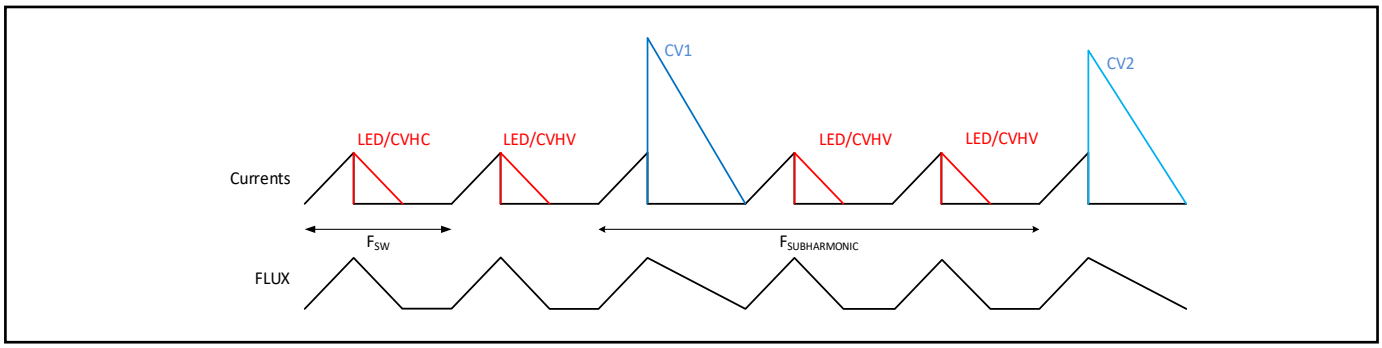


Figure 15. Multi-Output Control Switching Pattern.

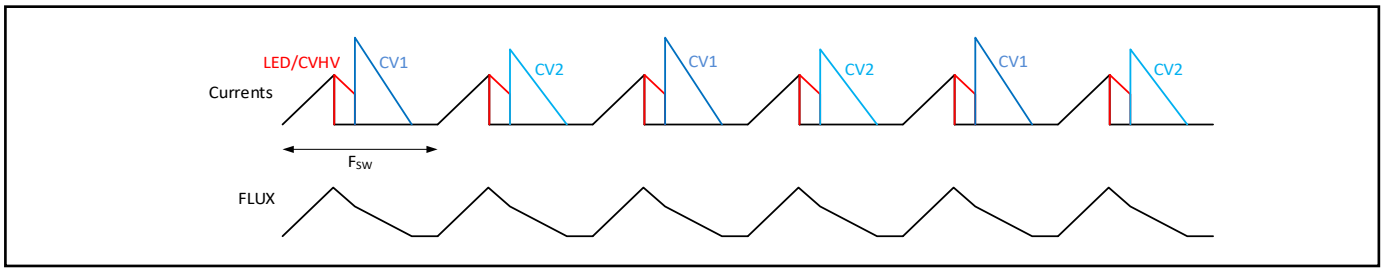


Figure 16. InnoMux2-EP Switching Pattern.

Output Capacitance Requirement

The InnoMux2-EP IC has a minimum output capacitance requirement for each output to ensure optimum operation. This is given by the following equation:

$$C_{OUTmin} = \frac{L_{PRI} \times I_{LIMIT}^2}{4 \times \frac{V_{OUT}^2}{V_{FB(REG)}} \times V_{SHTHR}}$$

Where:

L_{PRI} is the primary inductance
I_{LIMIT} is the primary peak current
V_{OUT} is the output voltage for the given output
V_{SHTHR} is 10 mV for CV outputs and 5 mV for V_{LED} output
$V_{FB(REG)}$ internal voltage comparator reference voltage

Minimum Off-Time

The secondary controller initiates a cycle request using the FluxLink magneto-inductive connection to the primary. The maximum frequency of secondary cycle requests is limited by the minimum cycle off-time of $t_{OFF(MIN)}$. This ensures that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency

The maximum switch-request frequency from the secondary controller is f_{SREQ}.

Maximum Secondary Inhibit Period

Secondary requests to initiate primary switching are inhibited when necessary to maintain operation below maximum frequency and ensure minimum off-time. Secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle request is ~30 µs.

Feedback

For applications with CV only outputs, output voltage feedback is provided by the FEEDBACK pins (FB1, FB2, FBHV) and is used for output voltage regulation of each output. The internal voltage comparator reference voltage is $V_{FB(REG)}$.

The FB pins are noise sensitive so the feedback resistor networks need to be placed close to the IC. The FORWARD pin signal path must not be placed near the FB nodes. The resistor between the FB pins and GND should be 1-5 kΩ. A 100 pF capacitor may also be placed between the FB pins and GND to reduce noise.

FEEDBACK Pin Short/Open Detection

At start-up the sensed FB pin voltage is below $V_{FB(OFF)}$ after a number switching cycles, the secondary controller will complete the hand-shake to take control but will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

A weak internal pull-down for the FB pins allows FB pin-open to be detected.

When using the internal feedback (as is the case for applications with the LED output), this protection mechanism also applies. This protects against faults with the VCV1 and VLED pins.

Output Voltage Protection

If the output voltage is 12% higher than the regulation threshold for V_{CV1} or V_{CV2}, 20% higher than the regulation threshold for V_{CVHV} or 16% higher than the regulation threshold for V_{LED} a command is sent to the primary to either latch-off or begin an auto-restart sequence. This integrated output OVP can be used in conjunction or independently to the primary sensed OVP.

Shunts

The LV shunt is designed to limit the voltage lift on the V_{CV1} output. Voltage lift on the V_{CV1} output will typically occur due to its lower V_{OR}. At turn-on of the V_{CV1} selection MOSFET after delivery of a pulse to one of the other outputs, a small amount of energy is delivered to the V_{CV1} output from the higher idle ring voltage. The LV shunt is turned on when the sensed voltage exceeds $V_{LV(SHUNT)}$.

In practical applications it is unlikely that the V_{CV1} output will lift; V_{CV1} output lift typically only occurs when the V_{CV1} output is unloaded while the other outputs are running at high load. It is likely V_{CV1} is powering the secondary controller and this alone is sufficient to prevent lift.

The HV shunt is used to limit the voltage on the V_{CVHV}/V_{LED} rail to the maximum allowed voltage in case of peak-charging of the V_{CVHV}/V_{LED} output when the V_{CVHV}/V_{LED} output is not loaded. This peak charging is predominantly caused by leakage in the transformer; the V_{CVHV}/V_{LED} output typically has lowest leakage and thus will receive a small amount of energy from switching cycles that are destined for V_{CV1} or V_{CV2}. The HV shunt is turned on when the sensed voltage exceeds $V_{HV(SHUNT)}$.

Note that the V_{CV2} output does not need a shunt as this output is not susceptible to peak charging or unintended energy delivery.

Overload / Short-Circuit Protection

The V_{CV1}, V_{CV2} and V_{CVHV}/V_{LED} outputs have a maximum power protection feature. The controller determines whether the output is more than 10% (CV outputs) or more than 1% (V_{LED} output) below the set point. If this condition persists for multiple switching cycles, then the output is assumed to be overloaded – either the output has a short-circuit, or the output power capability of the power supply has been exceeded and it cannot maintain regulation.

Over-Temperature Latch-Off

The thermal shutdown circuitry senses the secondary die temperature. The threshold is set to $T_{SD(SEC)}$.

Primary control over-temperature is the main temperature protection feature and includes hysteresis. The secondary controller also has over temperature protection but once reached creates a latch-off condition as hysteresis is not available.

DCM ZVS Mode Switching

The InnoMux2-EP IC features Zero Voltage Switching (ZVS) in the primary switch while the converter is operating in discontinuous conduction mode (DCM). This is achieved using the synchronous rectifier (SR) MOSFET. This mode of operation is disabled in continuous conduction mode (CCM). IMX2353F (1700 V) exclusively operates in DCM ZVS mode.

Before turning on the primary switch, the SR MOSFET is turned on at the valley of the idle ring on the FORWARD Pin. The SR MOSFET is kept on to charge the transformer's magnetizing inductance. The SR MOSFET is turned off and the voltage on the primary is allowed to ring down to near zero volts at which point the primary switch is turned on.

The SR MOSFET on-time for achieving ZVS is automatically calculated by the InnoMux2-EP controller. This corrects for design parameters, input voltage and output voltage. The calculation is based on the FORWARD Pin voltage during the primary on-time. To sample the FORWARD Pin voltage correctly the primary on-time needs to be at least 500 ns and FORWARD Pin voltage needs to be less than 100 V.

ZVS is not available when the LED is disabled or when operating below 15 kHz for output IMX2267 – IMX2268. In this case quasi-resonant switching is used.

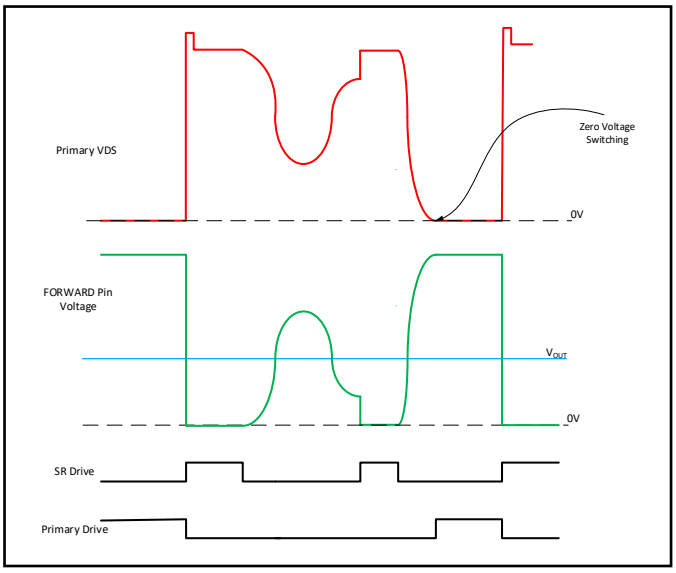


Figure 17. DCM ZVS Mode Switching.

DCM Only Mode

With PFC input or for a high-line (only) input design, DCM is always preferred due to the lower SR voltage spike when the primary turns on. The InnoMux2-EP IC has an option to only allow DCM switching. To ensure power delivery in a corner case condition, a K_p > 1.2 is recommended to enable this feature. This DCM ZVS mode is applied to IMX2353F (1700 V).

LED Current Control Operation

The InnoMux2-EP IC features an LED driver for controlling the current through an LED string. To provide application flexibility with regard to voltage and current, an extra MOSFET and sense resistor are used.

The LED driver uses the sense resistor to monitor LED current and adjusts the MOSFET gate voltage to control it. The maximum LED current is given by:

$$I_{LED(MAX)} = \frac{V_{ISENSE(MAX)}}{R_{ISENSE}}$$

The external MOSFET must be a logic level type with a low gate-source threshold voltage. The maximum drive voltage is $V_{IDRIVE(SAT)}$.

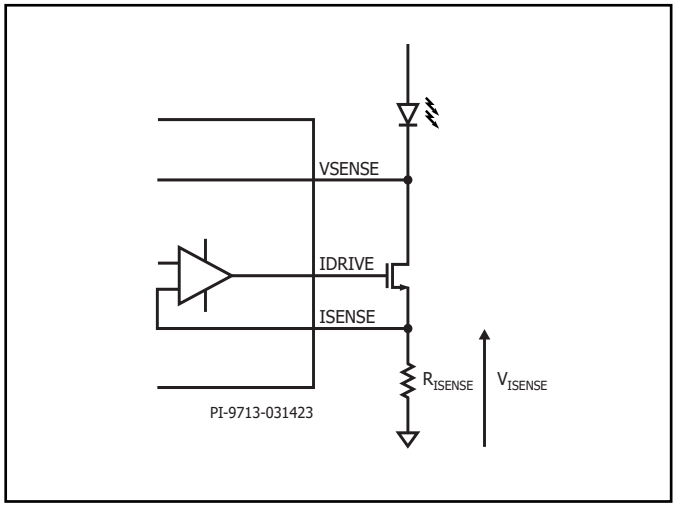


Figure 18. InnoMux2-EP LED Driver.

Output Voltage Regulation for V_{LED} Output

To maximize efficiency the InnoMux2-EP IC keeps the voltage drop across the current source as low as possible. The output voltage for driving the LED string (V_{LED}) is therefore regulated according to the minimum required voltage drop across the current source. The low voltage drop across the current source is maintained for any LED current by changing the V_{LED} output voltage set point.

The minimum voltage setting is configurable to accommodate a range of LED requirements and MOSFET characteristics.

To ensure stability of the LED voltage regulation a maximum V_{LED} output capacitance is recommended which depends on the maximum LED voltage and the maximum LED current.

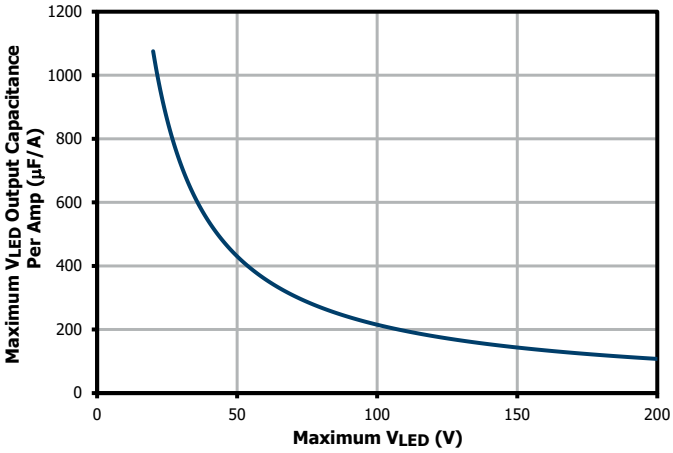


Figure 19. Maximum LED Output Capacitance.

LED Dimming

The current through the LED strings can be varied to change the LED brightness.

The InnoMux2-EP IC supports multiple dimming modes, the choice of which depends on whether 1 or 2 dimming pins are available. The dimming mode is also configurable.

Figure 19 provides an overview of the available dimming modes in the InnoMux2-EP IC.

PWM Dimming

In this mode, the LED current steps from zero to $I_{LED(MAX)}$ at a frequency given by the PWM input. The LED average current is controlled by the duty cycle of the PWM input.

PWM dimming is supported by applying a PWM signal with desired duty cycle to the DIM1 pin. The allowed PWM frequency range is given by $PWM_{F(RANGE)}$. Pulling the DIM1 pin low disables the LEDs.

When the DIM2 pin is available this also acts as an enable/disable signal, pulling the DIM2 pin low disables the LEDs. In this case both DIM1 and DIM2 need to be high to enable the LEDs.

Pulling DIM1 or DIM2 low is intended to disable the LEDs during a 'screen-off' mode. Disabling the LED regulator will reduce the InnoMux2-EP IC current consumption.

The LED driver is limited to a minimum on-time ($t_{LED(ON)MIN}$) which limits the minimum duty cycle and a minimum off time $t_{LED(OFF)MIN}$ which limits the maximum duty cycle before reaching 100%. 100% duty is achievable.

Analog Dimming
In this mode, the LED current is continuous and is proportional to the DIM1 pin voltage. $V_{ADIM(MAX)}$ on DIM1 pin corresponds to $I_{LED(MAX)}$, reducing the DIM1 pin voltage reduces the LED current in a linear fashion. Pulling DIM1 pin below $V_{ADIM(DISABLE)}$ disables the LEDs and they remain disabled until DIM1 pin is above $V_{ADIM(ENABLE)}$.

When the DIM2 pin is available this also acts as an enable/disable signal, pulling the DIM2 pin low disables the LEDs. In this case both DIM1 and DIM2 need to be high to enable the LEDs.

Additionally, when the DIM2 pin is available this pin can be used as a PWM input. This allows the LED brightness to be controlled by adjusting both the current duty cycle and the current level. This is described further in the Hybrid Dimming section.

Filtered PWM Dimming
In this mode, the LED current is continuous (as in Analog Dimming). The LED current level is proportional to the DIM1 pin duty cycle. This avoids the need for generating an accurate analog voltage, instead a regular PWM signal can be used and the controller converts the duty cycle to an analog current level.

100% duty cycle on the DIM1 pin corresponds to $I_{LED(MAX)}$, reducing the DIM1 pin duty cycle reduces the LED current in a linear fashion from 100% down to 3%. The allowed PWM frequency range is $FPWM_{F(RANGE)}$. Pulling DIM1 pin low disables the LEDs.

When the DIM2 pin is available this also acts as an enable/disabled signal, pulling the DIM2 pin low disables the LEDs. In this case both DIM1 and DIM2 need to be high to enable the LEDs.

Additionally, when the DIM2 pin is available this pin can be used as a PWM input. This allows the LED brightness to be controlled by adjusting both the current duty cycle and the current level. Described further in the Hybrid Dimming section.

Hybrid Dimming
Hybrid dimming combines adjusting the LED current by adjusting the peak level in an analog fashion and by pulsing the LED current where by the duty cycle is adjusted.

Hybrid dimming is only possible when both DIM1 and DIM2 pins are available. DIM1 is either an analog voltage input or a PWM input which is internally converted to an analog level. DIM2 is a PWM input. The analog, filtered PWM and PWM inputs behave as described in previous sections.

The combined LED dimming level from both inputs is not intended to go below 1% of $I_{LED(MAX)}$ (i.e. 10% analog and 10% PWM).

LED Faults
The InnoMux2-EP IC features LED fault protection. LED open, LED driver MOSFET Drain short to V_{LED} and LED short to ground are all protected against.

If LED open is detected, the power supply will continue to operate but with the LED output disabled until restart. The other faults result in restart or latch-off.

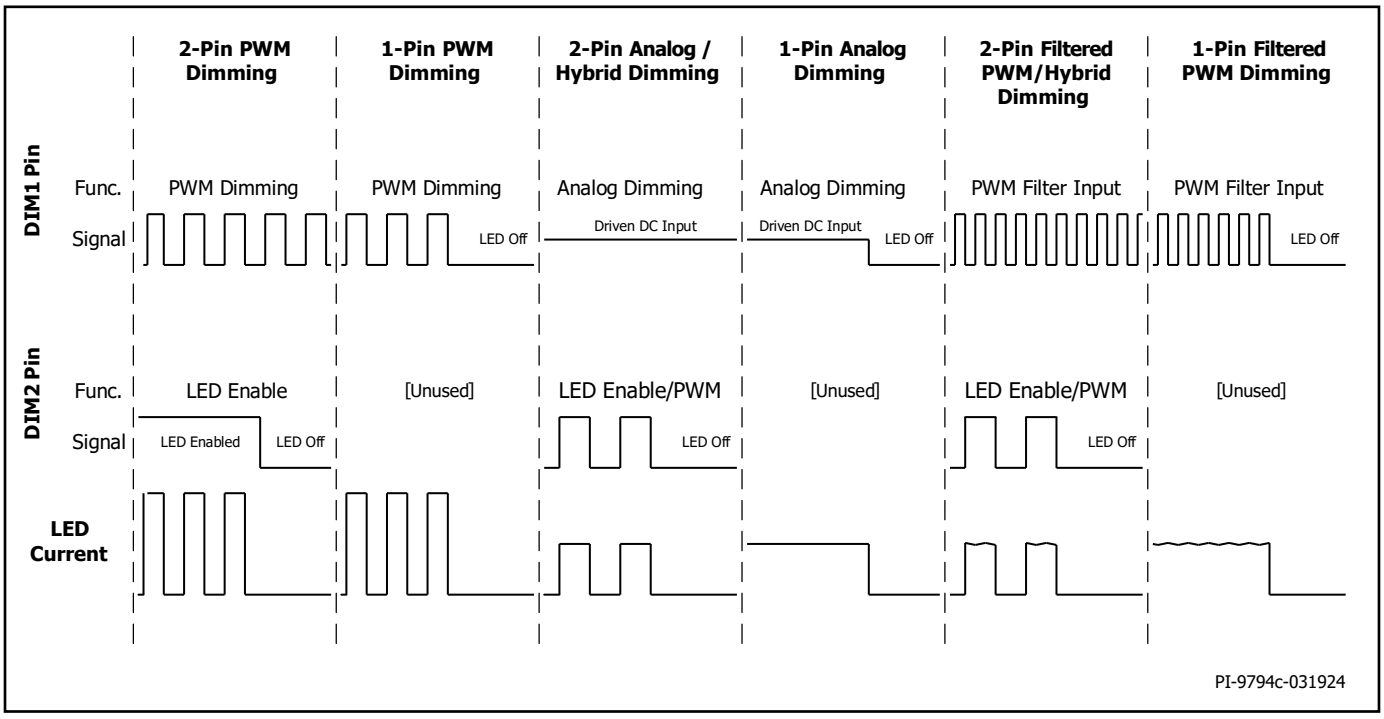


Figure 20. InnoMux2-EP Dimming Modes.

Design Considerations When Using PowiGaN Devices (IMX2353F)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 20. VOR is the reflected output voltage across the primary winding when the secondary is conducting. VBUS is the DC voltage connected to one end of the transformer primary winding. In addition to VBUS+VOR, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch.

VCLM in Figure 20 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of VBUS, VOR and VCLM. VOR and the clamp voltage VCLM should be selected such that the peak drain voltage is lower than 1450 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during input transients will maintain the peak drain voltage well below 1700 V.

Due to DCM operation only for IMX2353F, set reflected output voltage (VOR) to main $K_p \geq 1$ for all input range conditions.

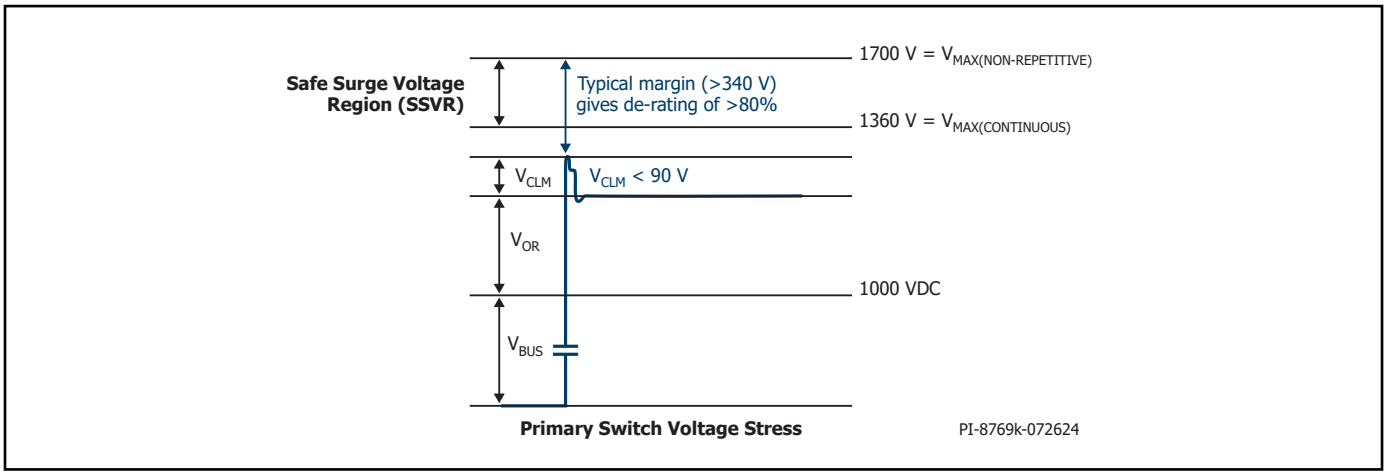


Figure 21. Peak Drain Voltage for 1000 VDC Input Voltage.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: IMX2267-IMX2268 ..... -0.3 to 650 V
DRAIN Pin Voltage: IMX2174-IMX2177 ..... -0.3 to 725 V
DRAIN Pin Voltage: IMX2x78, IMX2x79, IMX2x70 ..... -0.3 to 750 V[5]
DRAIN Pin Voltage: IMX2353 ..... -0.3 to 1700 V[6]
DRAIN Pin Peak Current: IMX2174 ..... 3.47 A[7]
IMX2175 ..... 4.11 A[7]
IMX2176 ..... 5.19 A[7]
IMX2177 ..... 5.57 A[7]
IMX2267 ..... 5.92 A[7]
IMX2268 ..... 6.24 A[7]
PowiGaN device IMX2x78 ..... 6.5 A[8]
PowiGaN device IMX2x79 ..... 10 A[8]
PowiGaN device IMX2x70 ..... 14 A[8]
PowiGaN device IMX2353 ..... 6.5 A[8]
V Pin Voltage ..... -0.3 V to 650 V
BPP/BPS Pin Voltage ..... -0.3 V to 6 V
BPP Pin Current ..... 100 mA
FWD Pin Voltage ..... -1.5 V to 250 V
SR Pin Voltage ..... -0.3 V to 6 V
VCV1, VCV2/AS Pin Voltage ..... -0.3 V to 30 V
VCVHV/VLED Pin Voltage ..... -0.3 V to 250 V
CDR1, CDR2 Pin Voltage ..... -0.3 V to 6 V
DIM1, DIM2 Pin Voltage ..... -0.3 V to 6 V
ISENSE Pin Voltage ..... -0.3 V to 6 V
IDRIVE Pin Voltage ..... -0.3 V to 6 V
VSENSE Pin Voltage ..... -0.3 V to 250 V

Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3] ..... -40 to 150 °C
Operating Ambient Temperature ..... -40 to 105 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Maximum Drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V
   Maximum continuous Drain voltage ..... -0.3 V to 650 V
6. Maximum Drain voltage (non-repetitive pulse) ... -0.3 V to 1700 V
   Maximum continuous Drain voltage ..... -0.3 V to 1360 V
7. Higher peak Drain current is allowed while Drain voltage is simultaneously less than 400 V. Please refer to Figure 21 and Figure 26.
8. Please refer to Figure 33 and Figure 37 about maximum voltage and current combinations.

Thermal Resistance

Thermal Resistance: IMX2267 – IMX2268 InSOP-24B
(θ_{JA}) ..... 48 °C/W[2], 43 °C/W[3]
(θ_{JC}) ..... 1 °C/W[4,5]

IMX2278 – IMX2270 InSOP-T28B
(θ_{JA}) ..... 71-60 °C/W[2,4], 63-55 °C/W[3,4]
(θ_{JC}) ..... 8-3 °C/W[2,4,5]

IMX2174 – IMX2177 InSOP-T28D
(θ_{JA}) ..... 55-52 °C/W[2,4], 50-42 °C/W[3,4]
(θ_{JC}) ..... 10-7 °C/W[2,4,5]

IMX2378 – IMX2370 InSOP-T28D
(θ_{JA}) ..... 71-68 °C/W[2,4], 65-57 °C/W[3,4]
(θ_{JC}) ..... 19-9 °C/W[2,4,5]

IMX2353 InSOP-T28G
(θ_{JA}) ..... 71-68 °C/W[2], 65-57 °C/W[3]
(θ_{JC}) ..... 19-9 °C/W[2]

Notes:
1. The case temperature is measured on the top of the package.
2. Soldered to 0.36 sq. inch (232 mm²), 2 oz. (610 g/m²) copper clad.
3. Soldered to 1.0 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
4. Highest thermal resistance corresponds to controllers with highest primary switch $R_{DS(ON)}$ and then reduces for controllers with lower $R_{DS(ON)}$ due to the larger device size.
5. The θ_{JC} is measured to the bottom of the package for exposed pad packages (InSOP-24B, InSOP-T28B) and to the top of the package for overmolded packages (InSOP-24D, InSOP-T28D, InSOP-T28G).

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C		23	25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz		0.8	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (MOSFET not Switching) T_J = 25 °C	IMX2174 – IMX2177, IMX2267 – IMX2268		200	300	µA
			IMX2x78, IMX2x79, IMX2x70, IMX2353		375	460	
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (MOSFET Switching at f_{SREC}) T_J = 25 °C	IMX2174	0.44	0.58	0.83	mA
			IMX2175	0.59	0.79	1.10	
			IMX2176	0.77	1.02	1.38	
			IMX2177	0.90	1.20	1.73	
			IMX2267	0.77	1.03	1.38	
			IMX2268	0.90	1.20	1.75	
			IMX2x78 IMX2353		2.10		
			IMX2x79		2.95		
			IMX2x70		2.96		
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.8	5	5.16	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.80	3.15	3.50	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.6	25.8	28	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	IMX2x6x, IMX217x, IMX227x, IMX237x T_J = 25 °C		20	23	24.5	µA
		IMX235x T_J = 25 °C		19	21	23.5	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		106	115	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			7		µA

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100			µA
Line Fault Protection							
UV/OV Pin Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C			3		µs
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT}	di/dt = 500 mA/µs T_J = 25 °C	IMX2267C	1.84	2.0	2.16	A
		di/dt = 575 mA/µs T_J = 25 °C	IMX2268C	2.08	2.3	2.52	
		di/dt = 650 mA/µs T_J = 25 °C	IMX2278F	2.39	2.6	2.81	
		di/dt = 725 mA/µs T_J = 25 °C	IMX2279F	2.63	2.9	3.19	
		di/dt = 848 mA/µs T_J = 25 °C	IMX2270F	3.13	3.39	3.67	
		di/dt = 188 mA/µs T_J = 25 °C	IMX2174F	0.697	0.750	0.803	
		di/dt = 288 mA/µs T_J = 25 °C	IMX2175F	1.06	1.15	1.24	
		di/dt = 363 mA/µs T_J = 25 °C	IMX2176F	1.33	1.45	1.57	
		di/dt = 400 mA/µs T_J = 25 °C	IMX2177F	1.46	1.6	1.74	
		di/dt = 475 mA/µs T_J = 25 °C	IMX2378F	1.77	1.9	2.03	
		di/dt = 550 mA/µs T_J = 25 °C	IMX2379F	2.02	2.2	2.38	
		di/dt = 650 mA/µs T_J = 25 °C	IMX2370F	2.35	2.6	2.85	
		di/dt = 475 mA/µs T_J = 25 °C	IMX2353F	1.67	1.85	2.04	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$	di/dt = 575 mA/µs T_J = 25 °C	IMX2267C	2.10	2.3	2.50	A
		di/dt = 650 mA/µs T_J = 25 °C	IMX2268C	2.39	2.6	2.81	
		di/dt = 728 mA/µs T_J = 25 °C	IMX2278F	2.63	2.91	3.19	
		di/dt = 813 mA/µs T_J = 25 °C	IMX2279F	2.97	3.25	3.53	
		di/dt = 950 mA/µs T_J = 25 °C	IMX2270F	3.48	3.8	4.12	
		di/dt = 238 mA/µs T_J = 25 °C	IMX2174F	0.86	0.95	1.04	
		di/dt = 350 mA/µs T_J = 25 °C	IMX2175F	1.27	1.4	1.53	
		di/dt = 413 mA/µs T_J = 25 °C	IMX2176F	1.51	1.65	1.79	
		di/dt = 463 mA/µs T_J = 25 °C	IMX2177F	1.69	1.85	2.01	
		di/dt = 525 mA/µs T_J = 25 °C	IMX2378F	1.92	2.1	2.28	
		di/dt = 613 mA/µs T_J = 25 °C	IMX2379F	2.24	2.45	2.66	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$	di/dt = 725 mA/µs T_J = 25 °C	IMX2370F	2.65	2.9	3.15	A
		di/dt = 475 mA/µs T_J = 25 °C	IMX2353F	1.86	2.05	2.23	
Overload Frequency	f_{OVL}	T_J = 25 °C	IMX2174 – IMX2177 IMX2267 – IMX2268 IMX2353	102	110	118	kHz
			IMX2x78, IMX2x79, IMX2x70	148	155	161	
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6	7.5	11.3	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7	2	2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note B			0.2		sec
Output							
On-State Resistance	$R_{DS(ON)}$	IMX2174 $I_D = I_{LIMIT+1}$	T_J = 25 °C		3.22	3.70	Ω
			T_J = 100 °C		4.99	5.74	
		IMX2175 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		IMX2176 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.34	1.54	
			T_J = 100 °C		2.08	2.39	
		IMX2177 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
		IMX2267 $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.02	1.17	
			T_J = 100 °C		1.58	1.82	
		IMX2268 $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.86	0.99	
			T_J = 100 °C		1.34	1.55	
		IMX2x78 $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		IMX2x79 $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		IMX2x70 $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		IMX2353 $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.73	1.02	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output (cont.)							
Off-State Drain Leakage Current	I_{DSS1}	V_{BPP} = V_{BPP} + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C	IMX2x6x IMX2x7x			200	µA
			IMX2353			200	
	I_{DSS2}	V_{BPP} = V_{BPP} + 0.1 V V_{DS} = 325 V T_J = 25 °C	IMX2x6x IMX2x7x		15		
			IMX2353		15		
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$				70		°C
Secondary							
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	IMX2174 – IMX2177 IMX2267 – IMX2268 IMX2353	118	130	145	kHz
			IMX2x78, IMX2x79, IMX2x70	164	180	194	
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			3.2		mA
BPS Pin Voltage	V_{BPS}			4.9	5.0	5.15	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)}$				3.0	3.3	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(HYS)}$	T_J = 25 °C			1.0		V
Start-Up Ramp Time	$t_{SS(RAMP)}$				76		ms
Minimum Off-Time	$t_{OFF(MIN)}$		IMX2174 – IMX2177 IMX2267 – IMX2268 IMX2353		3.2		µs
			IMX2x78, IMX2x79, IMX2x70		2.5		
BPS Direct Power VCV1 Range	$V_{CV5V(BPS)}$			4.75	5.0	5.4	V
BPS Source Threshold VCV1	$V_{BPS(VCV1)}$				7.9	9.3	V
BPS Source Threshold VCV2/AS	$V_{BPS(VCV2)}$			5.3	5.5	5.8	V
Minimum Voltage VCVHV/VLED	$V_{STAYALIVE}$			6.55	8.0	9	V
Threshold Shutdown	$T_{SD(SEC)}$	See Note B			140		°C
Recommended Output Voltage Range							
VCV1 Recommended Voltage Range	V_{CV1}			3		25	V
VCV2 Recommended Voltage Range	V_{CV2}			5		25	V
VCVHV Recommended Voltage Range	V_{CVHV}			9		53	V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Recommended Output Voltage Range (cont.)							
VLED Recommended Voltage Range	V_{LED}			9		200	V
Feedback							
FEEDBACK Pin Regulation Voltage	$V_{FB(REG)}$	T_J = 25 °C		1.208	1.220	1.234	V
Overvoltage Threshold VCV1, VCV2	$V_{FB(OVP)}$	T_J = 25 °C			112% of $V_{FB(REG)}$		V
Overvoltage Threshold VCVHV	$V_{FB(OVP)VCVHV}$	T_J = 25 °C			120% of $V_{FB(REG)}$		V
Overvoltage Threshold VLED	$V_{FB(OVP)VLED}$	T_J = 25 °C			116% of $V_{FB(REG)}$		V
LV Shunt Threshold	$V_{LV(SHUNT)}$	T_J = 25 °C			104% of $V_{FB(REG)}$		V
Maximum LV Shunt Current	$I_{LV(SHUNT)}$				30		mA
HV Shunt Threshold	$V_{HV(SHUNT)}$		V_{CVHV}		104% of $V_{FB(REG)}$		
			V_{LED}		108% of $V_{FB(REG)}$		
Maximum HV Shunt Current	$I_{HV(SHUNT)}$		V_{CVHV}		9		mA
			V_{LED} < 50 V		8		mA
			V_{LED} < 100 V		4.1		mA
			V_{LED} < 150 V		3.3		mA
			V_{LED} > 150 V		2.1		mA
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$	T_J = 25 °C			48		mV
Led Control							
Frequency Range PWM Dimming	$PWM_{F(RANGE)}$			90		1,000	Hz
Frequency Range Filtered PWM Dimming	$FPWM_{F(RANGE)}$			90		30,000	HZ
Minimum On-Time PWM Dimming	$t_{LED(ON)MIN}$				12		µs
Minimum Off-Time PWM Dimming	$t_{LED(OFF)MIN}$	Limits the maximum duty cycle before reach 100%			1		µs
DIM1, DIM2 Pin Digital Input Thresholds	V_{IL}					0.8	V
	V_{IH}			2.0			V
DIM1 Pin Maximum Analog Dimming Voltage	$V_{ADIM(MAX)}$				3.0		V
DIM1 Pin Analog Dimming Enable Threshold	$V_{ADIM(ENABLE)}$				100	120	mV

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Led Control (cont.)						
DIM1 Pin Analog Dimming Disable Threshold	$V_{ADIM(DISABLE)}$		40	50		mV
ISENSE Pin Voltage	V_{ISENSE}	DIM1 Pin = $V_{ADIM(MAX)}$ (ADIM) DIM1 Pin = 100% Duty (FPWM) T_J = 25 °C	98	100	102	mV
		DIM1 Pin = 10% of $V_{ADIM(MAX)}$ (ADIM) DIM1 Pin = 10% Duty (FPWM) T_J = 25 °C	8	10	12	mV
IDRIVE Pin Saturation Detection	$V_{IDRIVE(SAT)}$	T_J = 25 °C		85% of BPS		V
VSENSE Pin Short to VLED Pin Detection Threshold	$V_{SENSE(FAULT)}$	T_J = 25 °C		97% of V_{LED}		V
Selection MOSFET						
CDR1, CDR2 Pin Drive Voltage	V_{CDR}			BPS		V
CDR1, CDR2 Pin Pull-Up Resistance		T_J = 25 °C	4.75	5.4	5.8	Ω
CDR1, CDR2 Pin Pull-Down Resistance		T_J = 25 °C	4.75	5.4	6.5	Ω
Refresh Pulse Width	$T_{REFRESH}$	Note: Doubled during start-up		500		ns
Synchronous Rectifier						
SR Pin Drive Voltage	V_{SR}			BPS		V
SR FWD Pin Regulation Target	$V_{FWD(REG)}$			-40	-85	mV
SR Pin Pull-Up Speed	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF $V_{FWD(REG)} - V_{FWD}$ = +40 mV		10		V/µs
SR Pin Pull-Down Speed	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF $V_{FWD(REG)} - V_{FWD}$ = -30 mV		-10		V/µs
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF 10-90%		50		ns
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF 10-90%		25		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 5.0 V I_{SR} = 5 mA	6	7.9	9	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 5.0 V I_{SR} = 5 mA	6	7.8	9	Ω

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Minimum	Value Tolerance Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

Typical Performance Curves (650 V MOSFET)

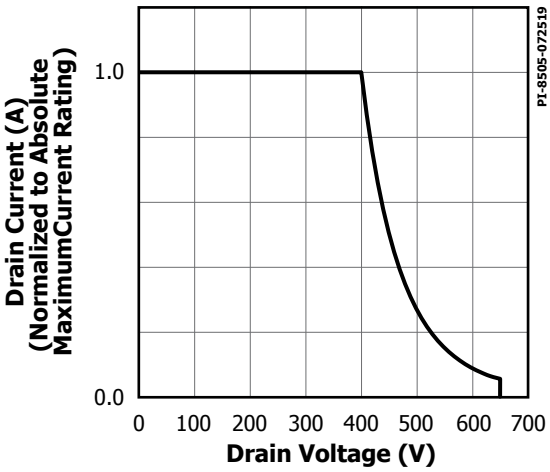


Figure 22. Maximum Allowable Drain Current vs. Drain Voltage

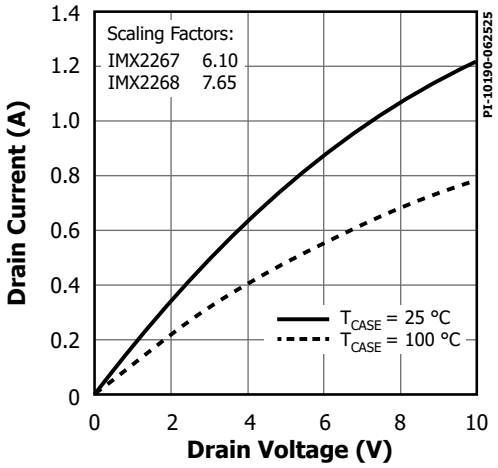


Figure 23. Output Characteristics.

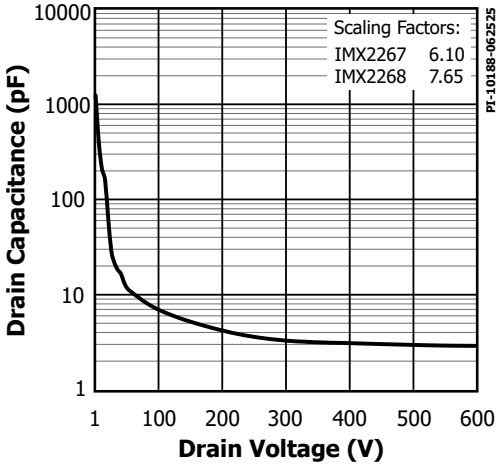


Figure 24. C_{OSS} vs. Drain Voltage.

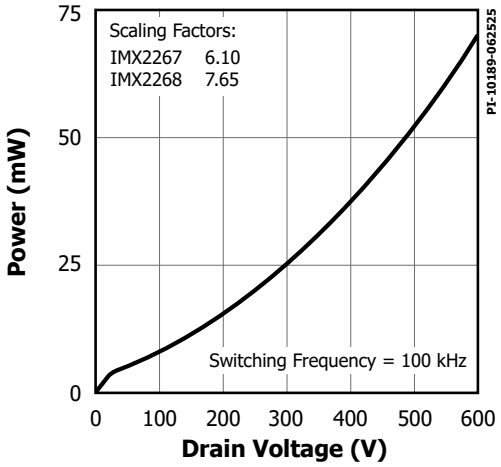


Figure 25. Drain Capacitance Power.

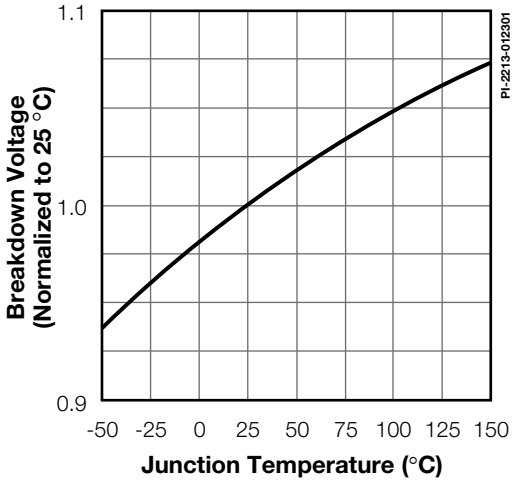


Figure 26. Breakdown vs. Temperature.

Typical Performance Curves (725 V MOSFET)

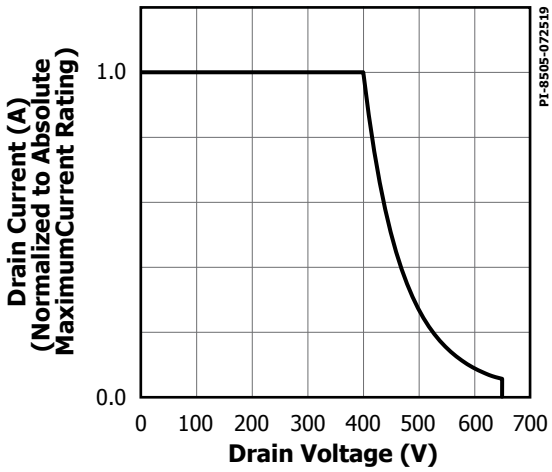


Figure 27. Maximum Allowable Drain Current vs. Drain Voltage.

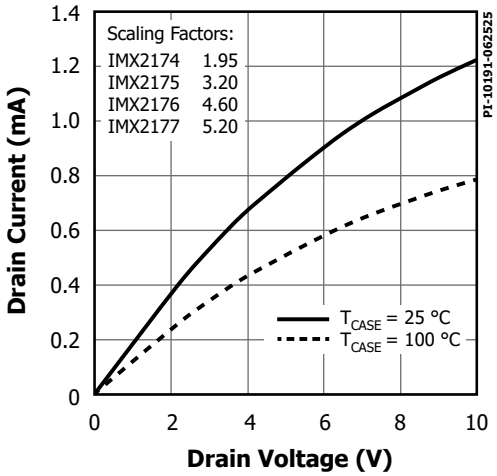


Figure 28. Output Characteristics.

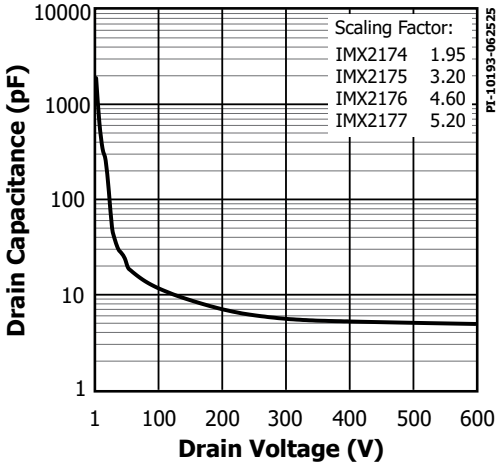


Figure 29. COSS vs. Drain Voltage.

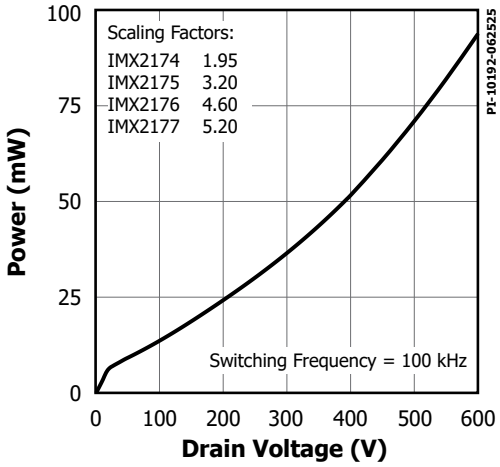


Figure 30. Drain Capacitance Power.

Typical Performance Curves (750 V MOSFET)

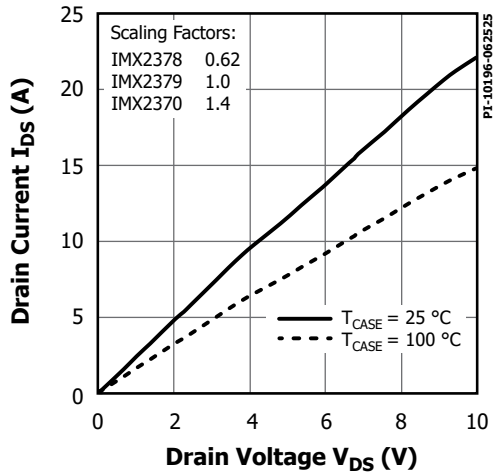


Figure 31. Output Characteristics.

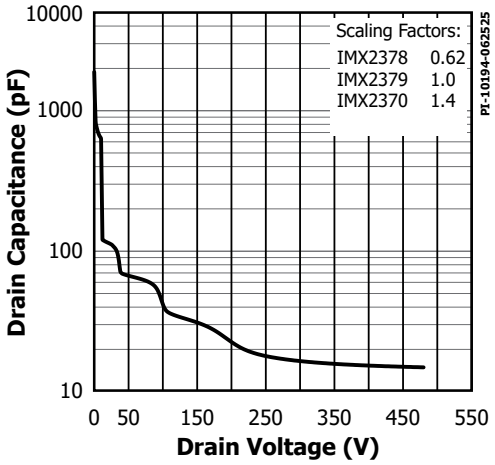


Figure 32. COSS vs. Drain Voltage.

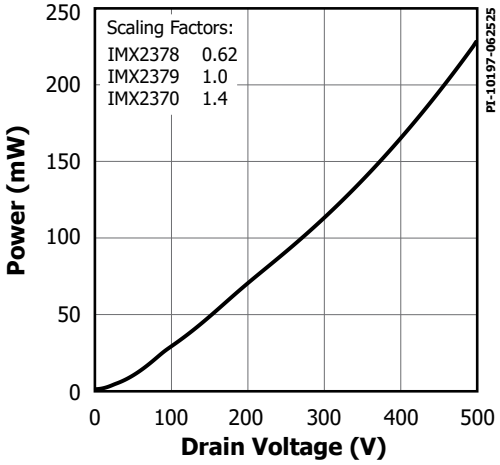


Figure 33. Drain Capacitance Power.

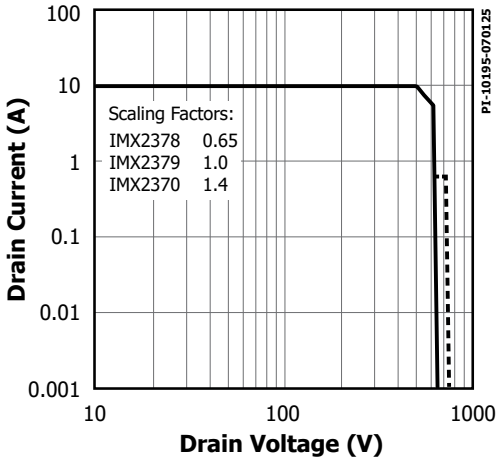


Figure 34. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices IMX2378 / IMX2379 / IMX2370).

Typical Performance Curves (1700 V MOSFET)

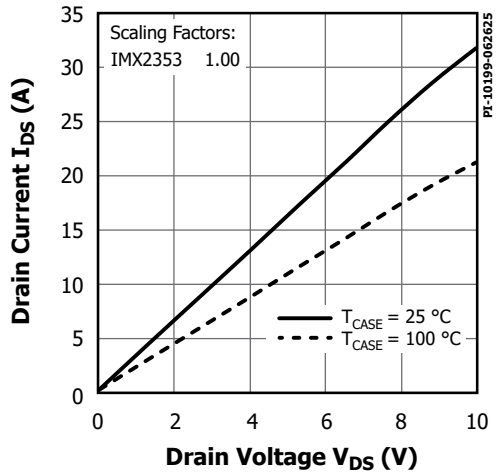


Figure 35. Output Characteristics.

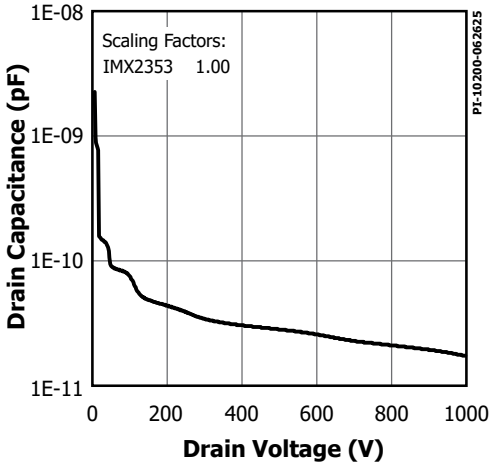


Figure 36. COSS vs. Drain Voltage.

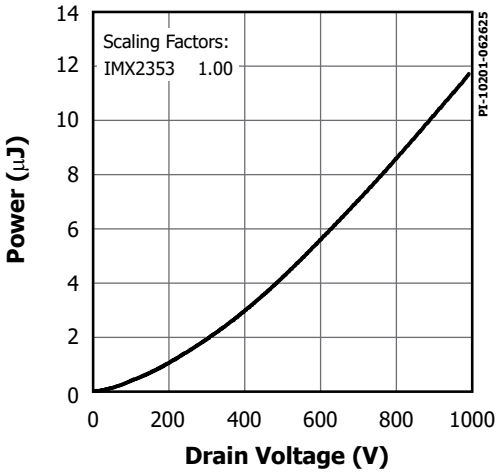


Figure 37. Drain Capacitance Power.

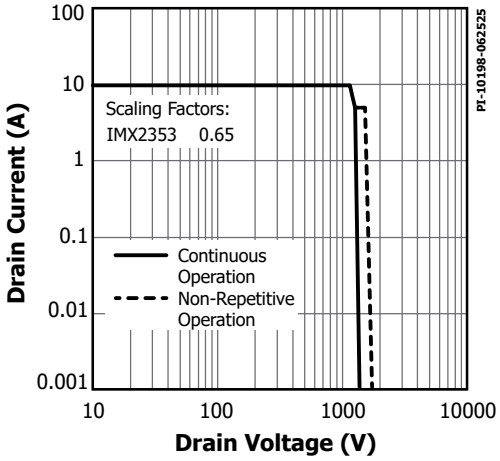
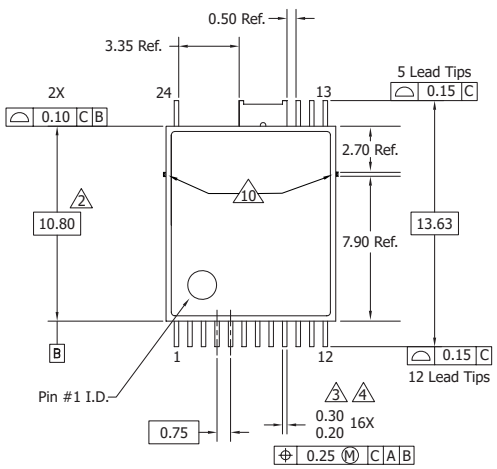
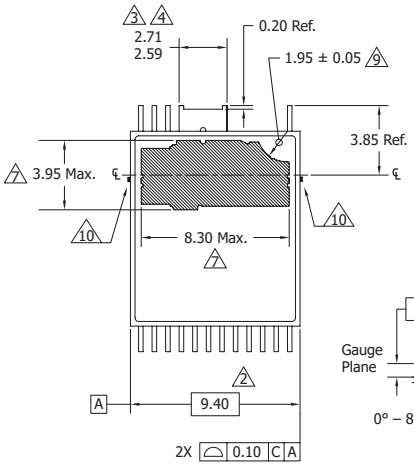


Figure 38. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Device IMX2353).

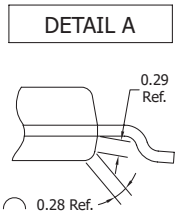
InSOP-24B (C Package)

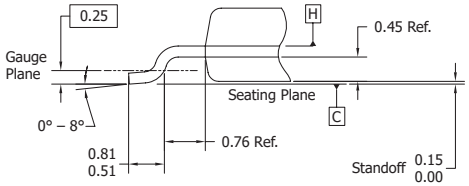


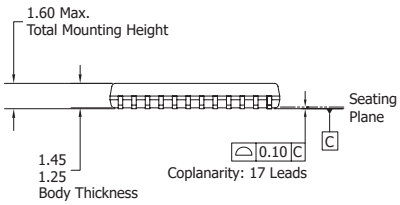
TOP VIEW



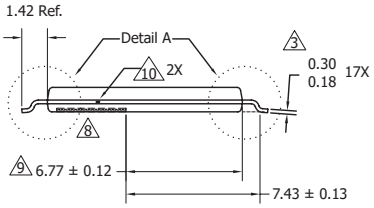
BOTTOM VIEW







SIDE VIEW



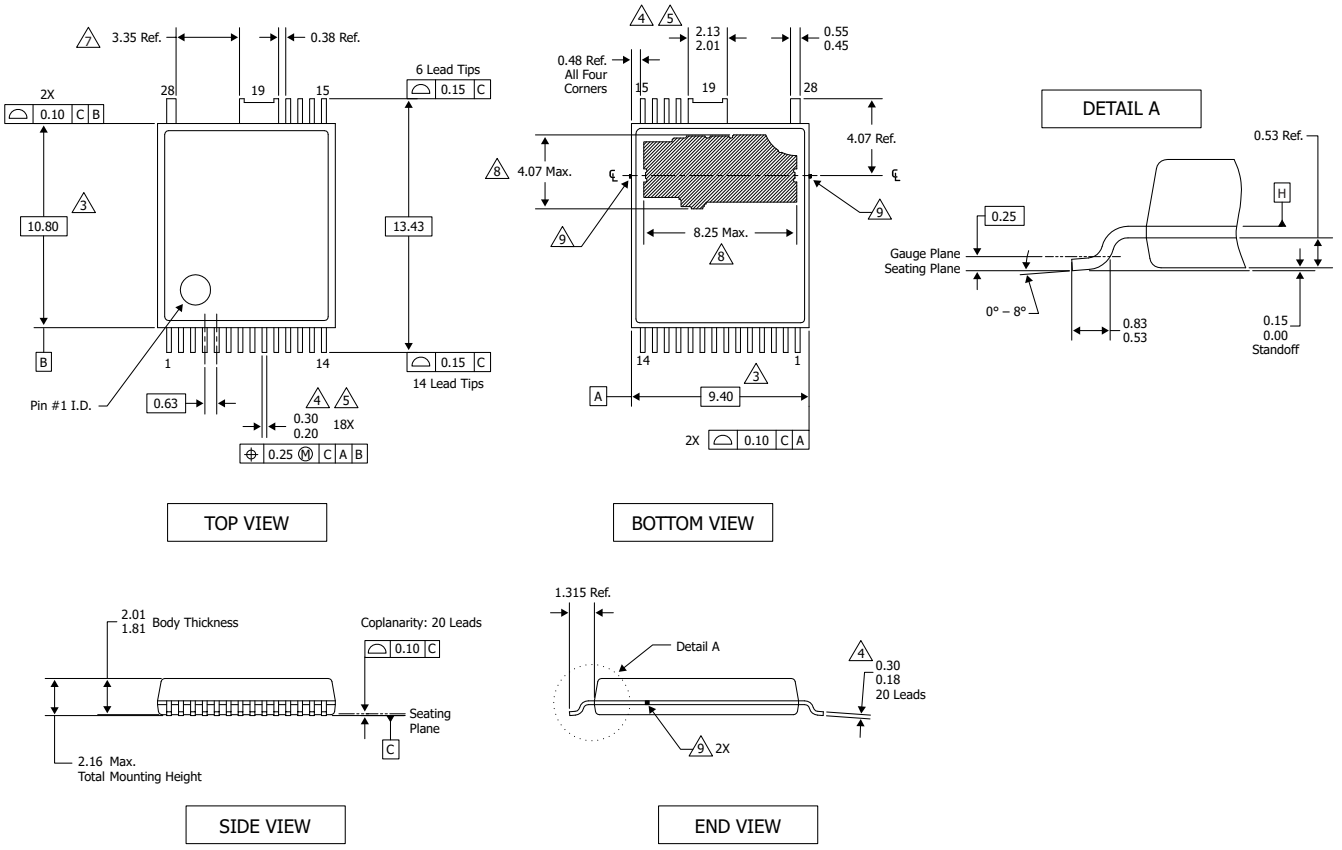
END VIEW

Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exculsive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. Exposed pad Min and Max dimensions include both size and positional tolerances.
8. Exposed pad hidden end-view shown for illustrative purposes to dimension creepage.
9. Creepage dimension includes package body side-contour dimensions as shown in Detail A.
10. Location of exposed metal tiebars: One at each end of package as shown. Electrically connected to the exposed pad and wide lead.

PI-8105-122720
POD-InSOP-24B Rev D

InSOP-T28B (F Package)



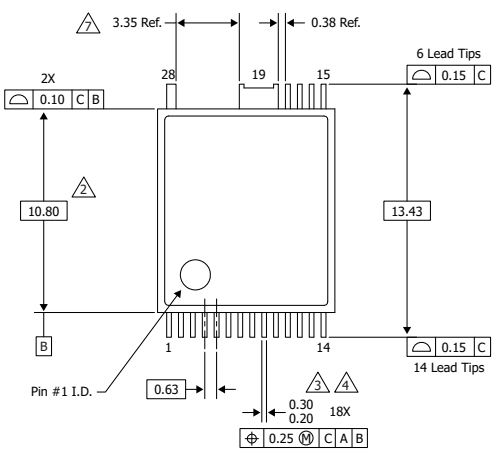
NOTES:

1. Dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
4. Dimensions noted are inclusive of plating thickness.
5. Does not include inter-lead flash or protrusions.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-Metal distance (Creepage) is 3.20 mm minimum.
8. Exposed pad max dimensions include both size and positional tolerances.
9. Location of exposed metal tiebars: One at each end of package as shown. Electrically connected to the exposed pad and wide lead.

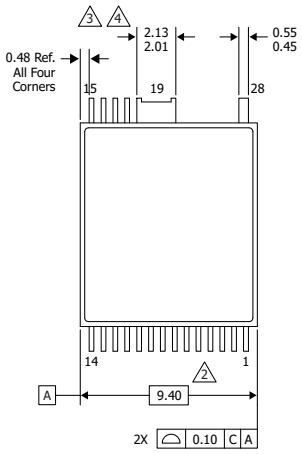
PI-9730-031224
POD-inSOP-T28B Rev A

POD-inSOP-T28B_A_032823

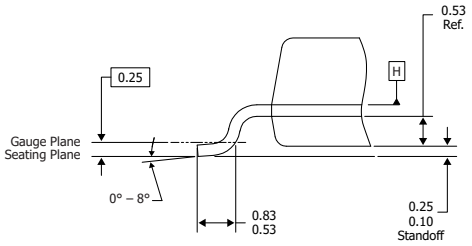
InSOP-T28D (F Package)



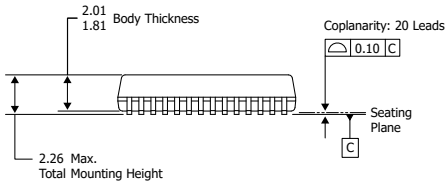
TOP VIEW



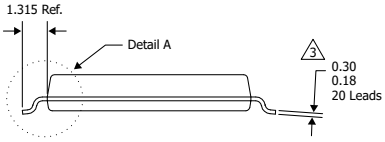
BOTTOM VIEW



DETAIL A



SIDE VIEW



END VIEW

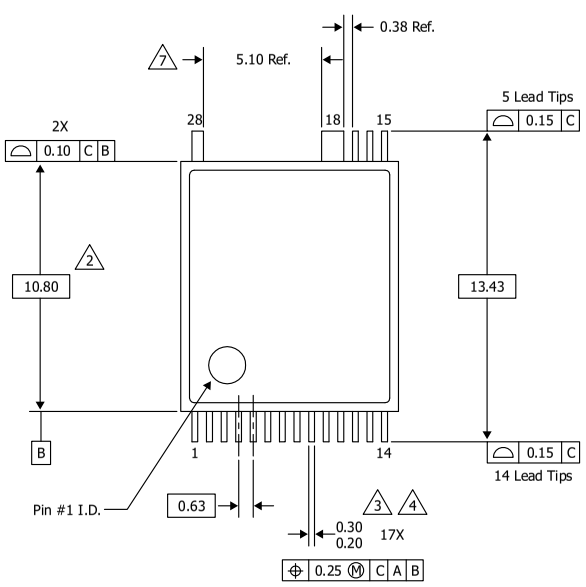
NOTES:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-Metal distance (Creepage) is 3.20 mm minimum.

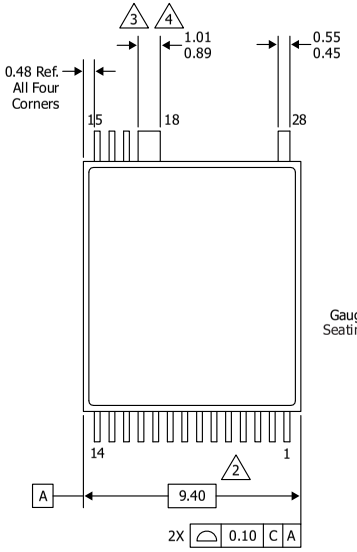
PI-9406-031224
POD-inSOP-T28D Rev B

POD-inSOP-T28D_B_032623

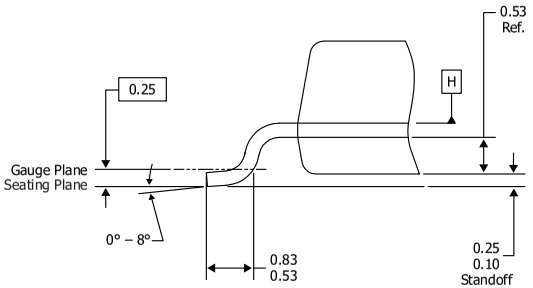
InSOP-T28G



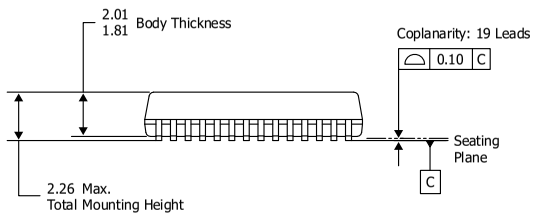
TOP VIEW



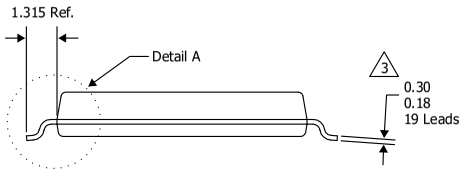
BOTTOM VIEW



DETAIL A



SIDE VIEW



END VIEW

NOTES:

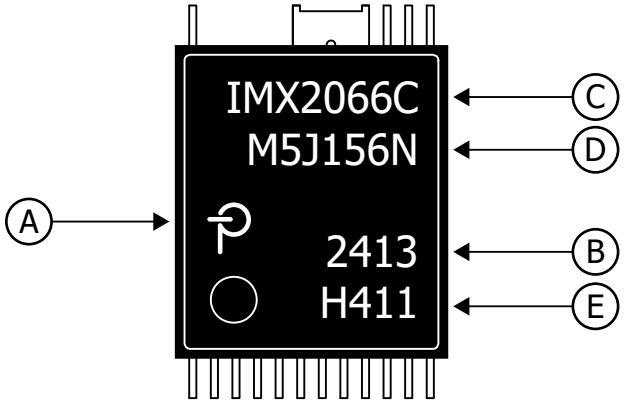
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-Metal distance (Creepage) is 4.95 mm minimum.

PI-9731-042123
POD-inSOP-T28G Rev C

POD-inSOP-T28G_C_040423

PACKAGE MARKING

InSOP-24B

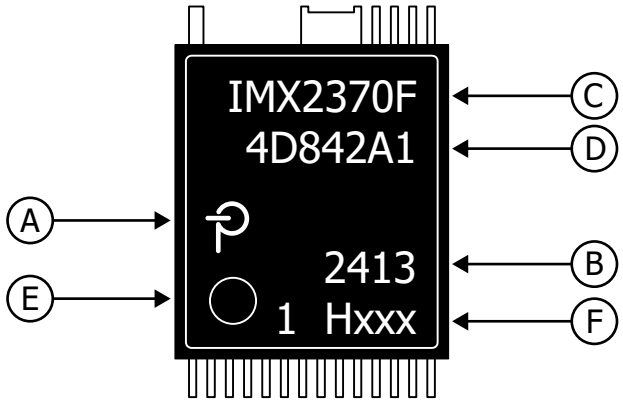


A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8617a-032824

PACKAGE MARKING

InSOP-T28B
InSOP-T28D

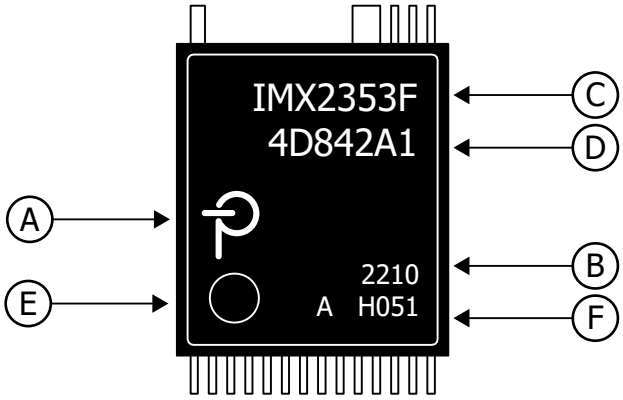


A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Supply Chain Flow (Foundry / Assembly Location (X))

PI-9756a-102424

PACKAGE MARKING

InSOP-T28G



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW))
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Supply Chain Flow (Foundry / Assembly Location (X)) and Feature Code

PI-9750b-062725

Feature Code Table IMX2353F Only

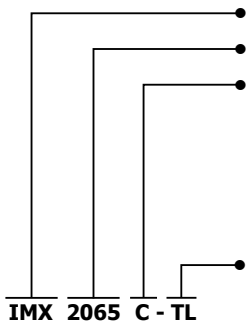
Feature Code	H415	H418
Output Configurations	2 CV	1 CV
Feedback Resistors	External	External
I_{LIM} Selectable	YES	YES
Primary Fault Response	Auto-Restart	Auto-Restart
Secondary Fault Response	Auto-Restart	Auto-Restart
Auto-Restart	$V_{OUT(AR)}$ = 90% of $V_{OUT(NOM)}$	$V_{OUT(AR)}$ = 90% of $V_{OUT(NOM)}$
Over Power Protection	No	No

Part Number	MSL Rating
IMX2267C	3
IMX2268C	3
IMX2278F	3
IMX2279F	3
IMX2270F	3
IMX2174F	3
IMX2175F	3
IMX2176F	3
IMX2177F	3
IMX2378F	3
IMX2379F	3
IMX2370F	3
IMX2353F	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



- **InnoMux2 Family**
- **InnoMux2-EP Series Number**
- **Package Identifier**
  - C — InSOP-24B
  - F — InSOP-T28B
  - F — InSOP-T28D
  - F — InSOP-T28G
- **Tape & Reel and Other Options**
  - TL — Tape & Reel, 2 k pcs per reel InSOP-24B, 1.8 k pcs per reel InSOP-T28B, InSOP-T28D and InSOP-T28G

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24 or from pin (19-22) to pin 28	1.5	A
Primary-Side Current Rating	Current from pin (16-19) to pin 24 or from pin (19-22) to pin 28 for IMX2x78 to IMX2x70	1.0	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W

Parameter	Symbol	Conditions		Rating	Units
Package Characteristics					
Clearance	CLR	InSOP-24D, inSOP-28D, inSOP-28G		11.4	mm (min)
		inSOP-28B		6.83	mm (min)
Creepage	CPG	InSOP-24D, InSOP-28D		11.4	mm (min)
		InSOP-28B		6.83	mm (min)
Distance Through Insulation	DTI			0.4	mm
Comparative Tracking Index	CTI			>600	-
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C (See Note 1)		10^{12}	Ω (min)
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ 125 °C (See Note 1)		10^{11}	
Isolation Capacitance, Input to Output	C_{IO}	(See Note 1)		1	pF
Package Insulation Characteristics					
Maximum RMS Working Isolation Voltage	$V_{IORM(RMS)}$	IMX2378F to IMX2370F		530	V_{RMS} (max)
		IMX2353F		1202	
Maximum Repetitive Peak Isolation Voltage	$V_{IORM(PK)}$	IMX2378F to IMX2370F		750	V_{PK} (max)
		IMX2353F		1700	
Maximum Transient Peak Isolation Voltage	V_{IOTM}	Test Voltage = V_{IOTM}, t = 60 s (Qualification)		6.6	kV_{PK} (max)
		t = 1 s (100% Production)		8	
Maximum Surge Isolation Voltage	V_{IOSM}	Surge Test 1.2/50 usec Table 2 IEC 60747-17		10.4	kV_{PK} (max)
Input to Output Test Peak Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PD} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC	IMX2378F to IMX2370F	1200	V_{PEAK}(min)
			IMX2353F	2720	
		Method A, After Input / Output Safety Test Subgroup 2/3, V_{PD} = 1.2 × V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC	IMX2378F to IMX2370F	900	
			IMX2353F	2040	
		Method B1, 100% Production Test, V_{PD} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC	IMX2378F to IMX2370F	1406	
			IMX2353F	3188	
Insulation Resistance	R_S	V_{IO} = 500 V at T_J = 150 °C		>10^9	Ω
Climatic Category				40/125/21	
IEC 60664-1 Rating Table					
Basic Isolation Group		Material Group		I	
Insulation Classification		Rated Mains RMS voltage ≤ 150 V		I - IV	
		Rated Mains RMS voltage ≤ 300 V		I - IV	
		Rated Mains RMS voltage ≤ 600V		I - IV	
		Rated Mains RMS voltage ≤ 1000 V		I - III	

Note 1: All pins on each side of the barrier tied together creating a two-terminal device.
Note 2: VDE 0884-17 (IEC/EN 60747-17) only applies to IMX2378F to IMX2370F and IMX2353F devices with following H-Codes: -H235, H607, H608, H609, H610, H611, H612, H613, H614, H615.

Revision	Notes	Date
B	Production release. Power table on page 2 has been updated to include O/P power for PFC input and Table 2 to include option features.	06/24
C	Added IMX2353F 1700 V part.	10/24
D	Added H Code H415 and updated power output 1700 V PN.	12/24
E	Added graphs, Safety table and new Figure 4 on page 1. Updated $R_{DS(ON)}$ room and hot MAX value.	11/25
F	Update made to page 11 under Auto-Restart, 2nd paragraph. Updates made to $t_{AR(OFF)SH}$, I_{UV-}, $V_{BPS(VCV1)}$ and $V_{C5V(BPS)}$ parameters. Update made to page 40 Table to include IMX2357F.	05/26

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

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