HiperPFS-5 Family

Power Factor Correction (PFC) Controller with Integrated 750 V PowiGaN Switch

Product Highlights

- High efficiency and power factor across load range
  - >98% efficient from 10% to 100% load
  - 0.96 PF at 20% load
- Quasi-resonant Discontinuous Conduction Mode (DCM) control
  - Up to 250 W output without heat sink
  - PFC stages can be paralleled for increased output power
  - Smallest boost inductor and simple boost diode
  - Low switching loss
  - PF enhancement compensates for EMI filter and bridge rectifier distortion
  - Operates with distorted input voltage signature of UPS or generators
- <40 mW no-load consumption at 230 VAC
  - Integrated automatic X capacitor discharge
- 750 V PowiGaN™ switch
  - High power factor at 305 VAC with 80% derating
  - Easily withstands 460 VAC line swells
- Highly integrated, compact footprint
  - Self-bias for high-voltage start-up
  - Source-potential cooling reduces EMI
- Programmable Power Good (PG) signal for active inrush control
- Selectable power limit enables rapid prototyping
- Safety certified to IEC62368

Applications

- PC
- Printer
- LCD TV
- Video game consoles
- 80 Plus™ Platinum
- High-power adaptors and USB PD 3.1 rapid charging
- High-power LED lighting
- Industrial and appliance
- Generic PFC converters

Description

The HiperPFS™-5 family of advanced power factor correction ICs leverages the low switching losses of the 750 V PowiGaN switch to optimize efficiency. High integration and advanced control minimizes system footprint by reducing component count and inductor size. Mounted in the low profile, surface mount InSOP-T28F package, HiperPFS-5 ICs pass heat directly to the PCB, eliminating the need for bulky heat sinks.

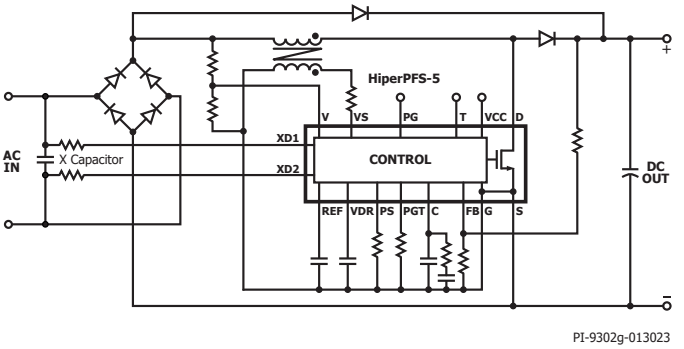


Figure 1. Typical Application Circuit.

Output Power Table

Maximum Continuous Output Power at 90 VAC	
Product[1,2]	**Self Biased**
PFS5173F	77 W
PFS5174F	115 W
PFS5175F	130 W
PFS5176F	165 W
PFS5177F	185 W
PFS5178F	250 W
Product[1,2]	**Non Self-Biased (USB PD)**
PFS5274F	115 W
PFS5275F	130 W
PFS5276F	165 W
PFS5277F	185 W
PFS5278F	250 W

Table 1. Output Power Table.

Notes:
1. Maximum output power is dependent on the design. With condition that package temperature < 125 ºC.
2. Package: InSOP-T28F.

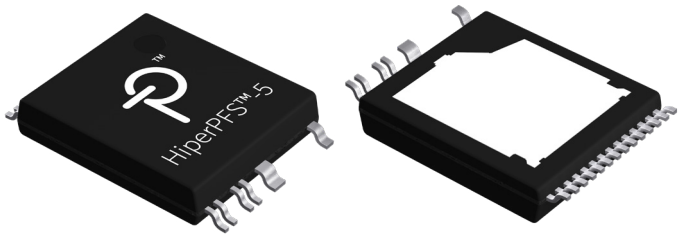


Figure 2. InSOP-T28F Package.

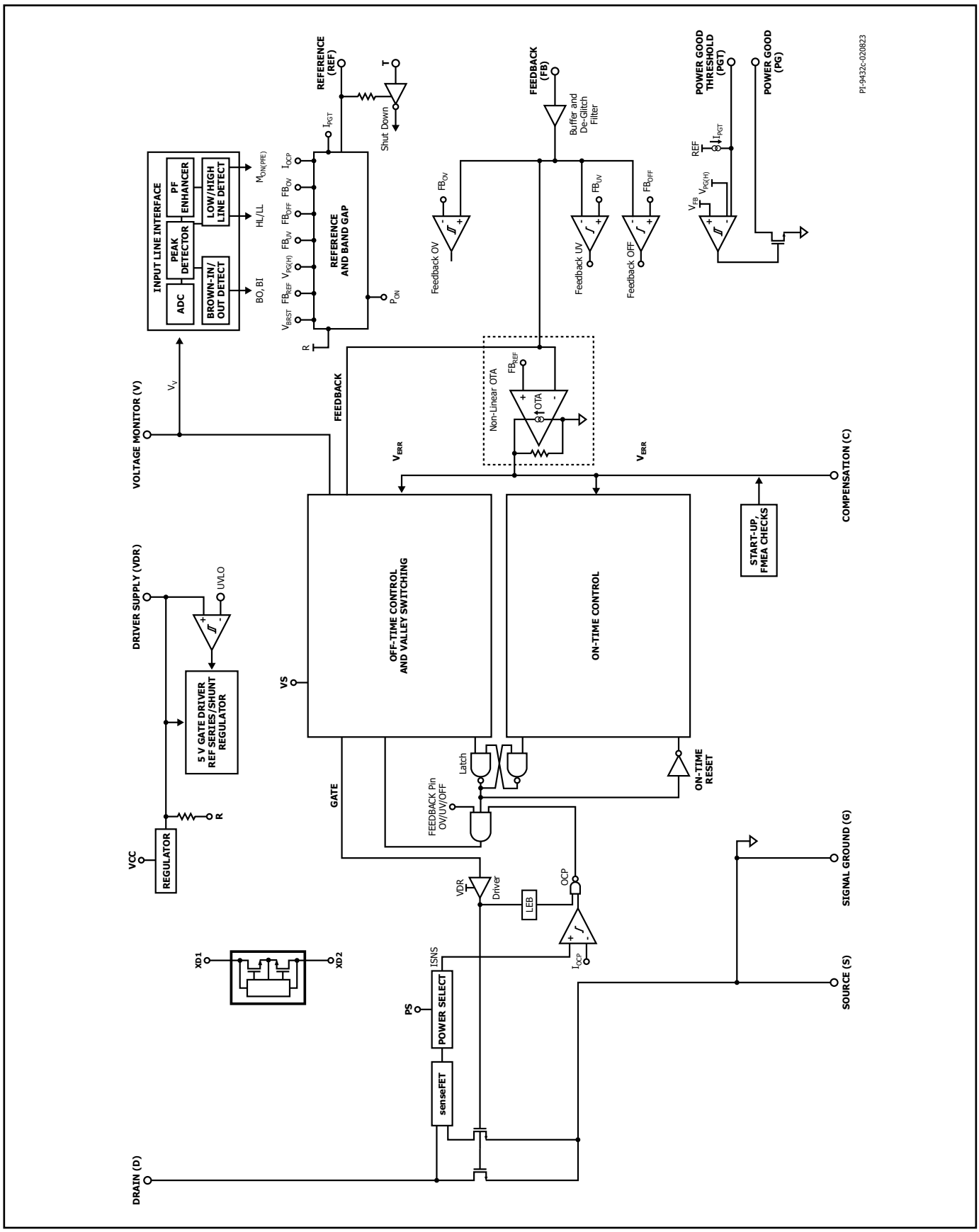


Figure 3. Functional Block Diagram.

Pin Functional Description

VALLEY SENSING (VS) Pin (Pin 1)
This pin is used to sense voltage on the auxiliary winding of the PFC inductor. The VS pin is connected to the auxiliary winding on a PFC inductor through an external resistor. The voltage on the auxiliary winding on a PFC inductor provides the controller information about the drain voltage. The external resistor is used to limit the current through VS pin and for fine adjustment of timing for valley switching.

SIGNAL GROUND (G) Pin (Pin 2, 13)
Discrete components used in the feedback circuit, including loop compensation, decoupling capacitors for the BIAS POWER (VCC), REFERENCE (REF) and VOLTAGE MONITOR (V) must be referenced to the SIGNAL GROUND (G) pin. The SIGNAL GROUND pin is also connected to the exposed pad of the device. The SIGNAL GROUND pin should not be tied directly to the SOURCE pin external to the IC.

T Pin (Pin 3)
This pin is used to shut down the HiperPFS-5 IC when it is pulled down (to SIGNAL GROUND potential). This can be used to turn off the PFC stage which improves overall system efficiency at light load. When an external bias is not applied, an internal resistor pulls the T pin up (to REF pin voltage). The T pin can be left floating during normal circuit operation, however, an external pull-up resistor (e.g. 50 kΩ, the value depends on the type of transistor used to pull down the T pin) from the VDR pin is recommended when the shut down mode is used for this device.

VOLTAGE MONITOR (V) Pin (Pin 4)
The VOLTAGE MONITOR pin is tied to the rectified high-voltage DC rail through a 100:1, 1% high-impedance resistor divider to minimize power consumption in standby. The recommended resistance value is between 8 MΩ and 16 MΩ. Changing this divider ratio affects the input current waveform, reduces power factor and increases THD. A small ceramic capacitor forming an 80 μs time constant must be connected between the VOLTAGE MONITOR pin and the SIGNAL GROUND pin to bypass any switching noise present on the rectified DC bus. This pin also features brown-in/out detection thresholds and incorporates a weak current source that acts as a pull-down in the event of an open-circuit condition.

COMPENSATION (C) Pin (Pin 5)
This pin is used for loop pole/zero compensation of the OTA error amplifier via a network of capacitors and a resistor between the COMPENSATION pin and SIGNAL GROUND pin.

Two or more PFC stages can be connected together via the C pin (and the outputs) to enable parallel operation. The trace connecting the C pins together should be routed to avoid noise pickup, as this is a high impedance node. (See Figure 4)

FEEDBACK (FB) Pin (Pin 6)
This pin is connected to the main voltage regulation feedback resistor divider network and is also used for fast over and undervoltage protection. This pin also detects the presence of the feedback voltage divider network at start-up. The divider ratio should be the 400/3.85 to ensure that nominal PFC output voltage is 400 V. Positioning a large upper resistor between 8 MΩ and 16 MΩ ±1% is recommended. A small ceramic capacitor between FEEDBACK and SIGNAL GROUND, forming a 80 μs time-constant with the bottom resistor, is required.

POWER GOOD (PG) Pin (Pin 7)
Use of the PG function is optional for PFS517xF. The POWER GOOD pin is an active low, open-drain connection which sinks current when the output voltage is in regulation. At start-up, once the FEEDBACK pin voltage has risen to ~95% of the internal reference voltage, the POWER GOOD pin is asserted low. After start-up, the output voltage threshold at which the PG signal becomes high-impedance and depends on the threshold programmed by the POWER GOOD THRESHOLD pin resistor. When not used, the POWER GOOD pin should be left floating.

For PFS527xF this pin is used to implement the boost follower feature. This is an active low, open-drain connection which sinks current when the peak detected input voltage is determined to be high-line. Connect an additional feedback resistor R_{BF} between PG pin and the FB pin to change the output voltage between low-line and high-line inputs. This feature improves efficiency particularly at low-line AC input.

POWER GOOD THRESHOLD (PGT) Pin (Pin 8)
This pin is used to program the output voltage threshold at which the PG signal becomes high-impedance representing the PFC stage falling out of regulation. The low threshold for the PG signal is programmed with a resistor between the POWER GOOD THRESHOLD and SIGNAL GROUND pins. Tying the POWER GOOD THRESHOLD to the REFERENCE pin disables the power good function (i.e. POWER GOOD pin remains high impedance). In boost follower mode, the PGT pin has no function and should be connected to REFERENCE pin.

POWER SELECTION (PS) Pin (Pin 9)
This pin is used to program the output power of the HiperPFS-5. The power is programmed with a resistor connected to the SIGNAL GROUND pin. The power is programmed in 10% steps, between 70% to 100% of nominal power.

VPP Pin (Pin 10)
Should be connected to REF pin or left open.

REFERENCE (REF) Pin (Pin 11)
This pin is connected to an external bypass capacitor. The voltage on this pin is nominally 5 V and is used to supply the control circuitry inside PFS PowiGaN.

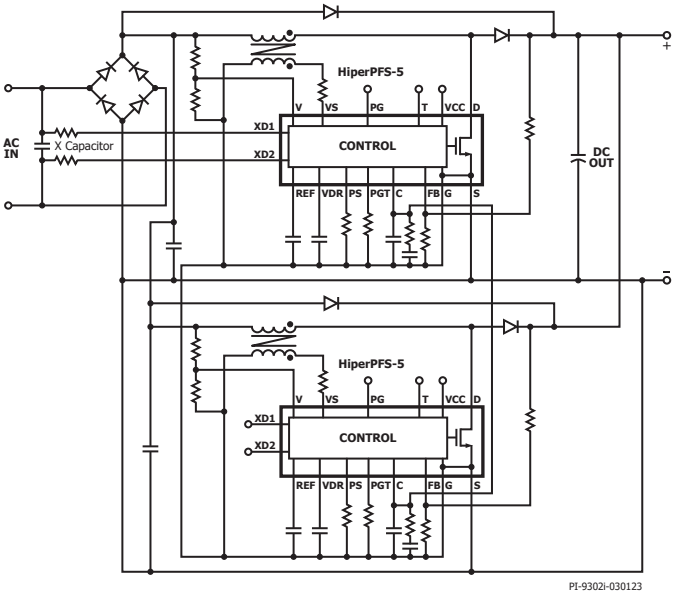


Figure 4. Compensation Pin Connection for Parallel Operation.

DRIVER VCC DECOUPLING (VDR) Pin (Pin 12)
This pin is connected to an external bypass capacitor. There is an internal linear regulator which supplies the VDR pin with a regulated voltage of (5.25 V nominally). This voltage is used to supply the driver section of the PFS PowiGaN controller.

BIAS POWER (VCC) Pin (Pin 14)
This is the input for the 7-35 VDC bias supply used to power the IC. The maximum operating voltage must be externally clamped to prevent the BIAS POWER pin from exceeding 35 VDC.

X CAPACITOR DISCHARGE TERMINAL XD1 (Pin 15-16)
Connected together internally to one terminal of the X capacitor. These two pins are connected together with a bond wire inside package. For selection of the discharge resistors follow the recommendations in CAPZero-2 data sheet.

X CAPACITOR DISCHARGE TERMINAL XD2 (Pin 18-19)
Connect one pair of pins via a series resistor to each side of the X capacitor. These two pins are connected together internally with a bond wire inside package. To select the values for the discharge resistors follow the recommendations in the CAPZero-2 data sheet.

SOURCE (S) Pin (Pin 21)
This pin is the source connection for the power switch as well as the negative bulk capacitor terminal connection.

DRAIN (D) Pin (Pin 28)
This is the drain connection for the internal power switch.

SOURCE (S) Exposed Pad
The exposed pad is the source connection for the power switch as well as the negative bulk capacitor terminal connection. It also provides a thermal path for cooling of the power switch.

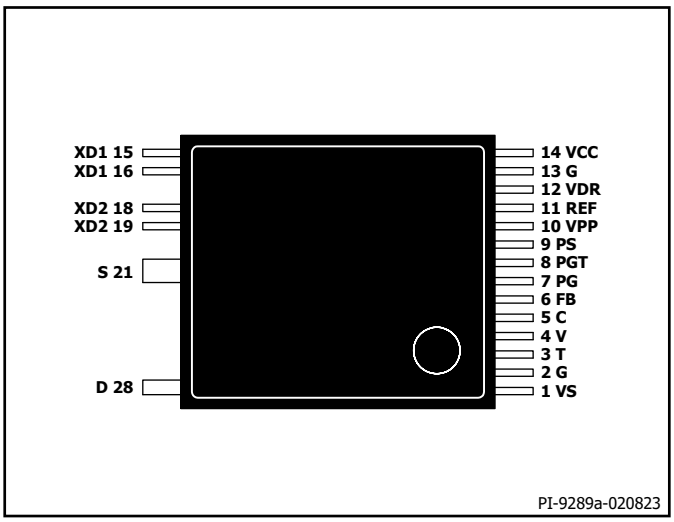


Figure 5. Pin Configuration.

Functional Description

The HiperPFS-5 family are variable switching frequency boost PFC devices. It employs a constant amp-second on-time and constant volt-second off-time control algorithm. This algorithm is used to regulate the output voltage and shape the input current to comply with regulatory harmonic current limits and (high power factor). Integrating the switch current and controlling it to have a constant amp-second product over the on-time of the switch allows the average input current to follow the input voltage. Integrating the difference between the output and input voltage maintains a constant volt-second balance dictated by the boost inductance, regulated output voltage and power. The controller sets the amount of charge delivered during each on-cycle. The charge per cycle is altered gradually over many switching cycles in response to load changes and can be considered constant across a given half line cycle. With this constant charge (or amp-second) control:

$$I_{IN} \times t_{ON} = K_2 \quad (1)$$

The control technique also sets constant volt-second for the off-time (t_{OFF}). The off-time is controlled such that:

$$(V_O - V_{IN}) \times t_{OFF} = K_1 \quad (2)$$

Since the volt-seconds during the on-time must equal the volt-second during the off-time, (to maintain flux equilibrium in the PFC choke), the on-time (t_{ON}) is controlled such that:

$$V_{IN} \times t_{ON} = K_1 \quad (3)$$

Substituting t_{ON} from (3) into (1) gives:

$$I_{IN} = V_{IN} \times K_2/K_1 \quad (4)$$

The relationship of (4) demonstrates that by controlling a constant amp-second on-time and constant volt-second off-time, the input current I_{IN} is proportional to the input voltage V_{IN}, satisfying the fundamental requirement for power factor correction.

At the end of volt-second integration for the off-time, the control engine waits for the valley of the Drain voltage, and turns on the PowiGaN at the minimum. In order to compensate for this delay, the HiperPFS-5 IC also measures the difference between desired OFF-time (controlled by volt-second integration) and actual OFF-time (synchronized with Drain voltage valley). The control engine then adjusts the next On-time period to account for this difference. This valley-correction ensures the same average current in each switching cycle.

This control produces a discontinuous mode power-switch current waveform (during normal operation) that varies both in frequency and peak current value across a line half-cycle to produce an input current proportional to the input voltage.

Control Engine

The controller features a low bandwidth, high gain OTA error-amplifier of the non-inverting terminal of which is connected to an internal voltage reference of 3.85 V. The inverting terminal of the error-amplifier is fed from the external FEEDBACK pin which connects to the output voltage divider network with a divider ratio of 3.85:400 to regulate the output voltage to 400 V (nominal). The FEEDBACK pin connects directly to the divider network to ensure fast transient load response.

The difference between the input and output voltage is derived internally, and the result is scaled, integrated, and compared to a voltage reference (V_{OFF}) to determine the point of off-time termination. The controller delays this request and terminates the off-time at a point to coincide with the nearest valley of the ring on the drain voltage.

The internally sensed FET switch current is scaled by the input-voltage peak detector current-sense gain (M_{ON}) then integrated and compared with the error-amplifier signal (V_{ERR}) to determine the on-time termination point. The valley correction block adjusts this to compensate for the delay imposed by the valley switching adjustment in the off-time.

Line Feed-Forward Scaling Factor (M_{ON}) and PF Enhancer

The VOLTAGE MONITOR (V) pin voltage is sampled and converted by a Δ-Σ ADC to a quantized digital value. A digital line-cycle peak detector, with dynamic time constants and multi-cycle filtering, derives and averages the peak of the input line voltage. This peak is used internally to scale the gain of the current sense signal through the M_{ON} variable. This contribution is required to reduce the dynamic range of the control feedback signal as well as flatten the loop gain over the operating input line voltage. The line-sense feed-forward gain adjustment is proportional to the square of the peak rectified AC line voltage and is adjusted as a function of the VOLTAGE MONITOR pin voltage.

At high-line, the feed-forward M_{ON} variable is dynamically adjusted across the line cycle in order to compensate for the line current distortion caused by the EMI filter and full bridge network, and improve power factor.

The line-sense feed-forward gain is also important in providing a switch power limit over the input line range.

Beyond the specified maximum power rating of the device, the internal power limit will regulate the output voltage below the set regulation threshold as a function of output overload to maintain constant output power.

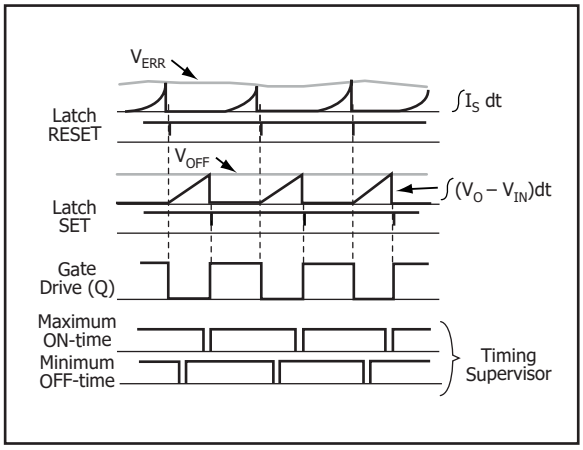


Figure 6. Idealized Converter Waveforms.

Valley Synchronization

In a normal operation, the PowiGaN switch is turned-on at the valley of the drain voltage of the PowiGaN power switch. The Valley Synchronisation Block ensures turn-on in the valley to minimize turn-on losses.

The voltage measured across the auxiliary (sense) winding of the PFC inductor is connected to the VALLEY SENSING (VS) pin through an external resistor. This voltage of auxiliary (sense) winding of the PFC inductor represents the difference between of the voltage on the drain of the PowiGaN switch and the rectified voltage. The valleys of this voltage coincide with valleys of the voltage on the drain of the PowiGaN switch.

In certain cases, where valley switching is not possible, such as during operation in CCM, or when the amplitude of oscillations of the drain voltage becomes too small, the controller enables the No Valley Switching (NVS) mode. In this condition, the controller does not wait for the valley to appear. When the volt-second integration circuit requests a turn-on, it immediately turns on the PowiGaN switch.

Valley Correction

Valley correction reduces the input current distortion coming from the valley switching operation in discontinuous mode (DCM) and critical mode (CrM). Valley correction is enabled in DCM and CrM operation when more than one valley is detected.

In a DCM PFC converter with valley switching, the PowiGaN switch can be turned on only at the V_{DS} valley instants. The relaxation frequency of the V_{DS} voltage ring is ≤ 1 MHz, which means that the time between two valleys are more than 1 µs apart. There is a delay between the instant when the OFF controller requests the turn-on and the point when the PowiGaN power switch is actually turned on.

This delay changes the average input current from what was originally requested by the controller, and the input current becomes distorted. The deviation in average cycle current from the desired current is proportional to this delay. In such cases, the switching period instantly changes by a significant value (could be in the range of 1 µs) and distortion of the input current is the most pronounced.

Controller Supplying Circuitry

Parts Without Self-Supply Circuit

Parts without the self-supply circuit are supplied only through the BIAS POWER (VCC) pin. Inside the IC there is a linear regulator between the VCC pin and the VDR pin. This linear regulator regulates the voltage on the VDR pin to 5.25 V.

The voltage on the VDR pin is used to supply the internal controller. A decoupling capacitor is connected to the VDR pin to provide a low high-frequency impedance path to ground.

Parts With the Self-Supply Circuit

Parts with the self-supply feature generate the internal supply voltage for the control circuitry. The converter operates with the control circuitry being supplied through the internal PowiGaN until the voltage on the VCC pin form the external bias circuit is established.

Once the voltage on the VCC pin appears, and is greater than the minimum voltage needed to operate the internal linear regulator (VCC > 7 V), the internal linear regulator will start supplying the control circuitry and disable the self-supply circuit.

Start-Up With Pin-to-Pin Short-Circuit Protection

At start-up and prior to the commencement of switching, the engine performs a sequence of operational pin short/open checks, as shown in Figure 7. If no faults are detected, when the input voltage peak is above the brown-in threshold, the engine enables switching.

The OTA error amplifier provides a non-linear amplifier (NLA) mechanism to overcome the inherently slow feedback loop response when the sensed output voltage on the FEEDBACK pin is outside its regulation window. This allows the error amplifier function to limit the maximum overshoot and undershoot during load transient events.

To reduce switch and output diode current stress at start-up, the HiperPFS-5 calculates the off-time based on the output voltage (V_O) during start-up, resulting in a soft controlled start-up.

Additionally, the Over-Current Protection (OCP) threshold is ramped up from 60% to 100% of its nominal value. This reduces flux swing in the PFC inductor if the control loop requires larger duty cycle.

At power-up, the controller first determines whether the appropriate supply voltage is applied by checking that the voltage on the VDR pin is greater than the $VDR_{VDR(UV+)}$ threshold. Once the voltage on the VDR pin is above the $V_{VDR(UV+)}$ threshold, pin open/short tests are performed, and if the FEEDBACK pin voltage is valid, the over-temperature status is confirmed to be false.

Once these checks are confirmed, the input voltage is monitored via the VOLTAGE MONITOR pin until it exceeds the V_{BR+} threshold (but the peak detector is not saturated). This is the point at which the value of the resistor on the POWER SELECTION (PS) pin is determined and the maximum output power is set. After the maximum power is determined the switching is enabled.

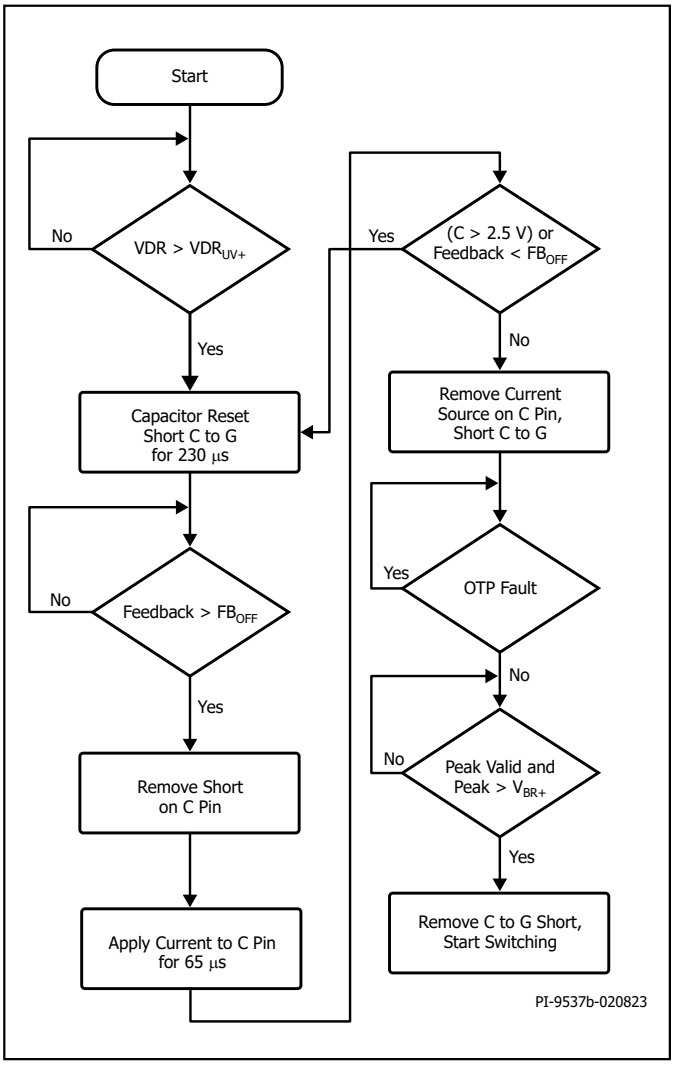


Figure 7. Start-Up Flow Chart.

Timing Supervisor and Operating Frequency Range

The controller operates with a variable switching frequency over the line frequency half-cycle, typically spanning a range of 22 – 145 kHz. The controller also features a timing supervisor function which monitors and limits the maximum switch on-time and off-time as well and ensures minimum cycle on-time. Figure 8 shows the typical half-line frequency profile of the device switching frequency as a function of input voltage at maximum load.

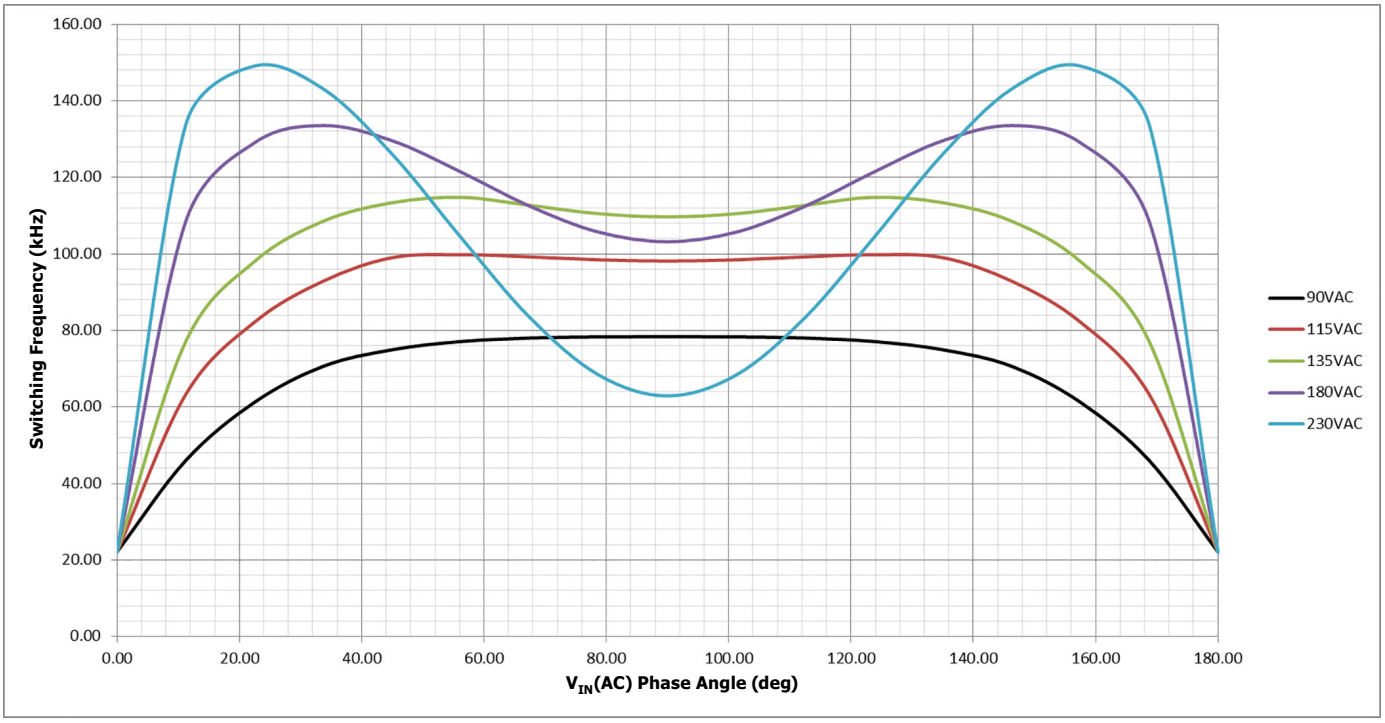


Figure 8. Frequency Variation Over Line Half-Cycle as a Function of Input Voltage.

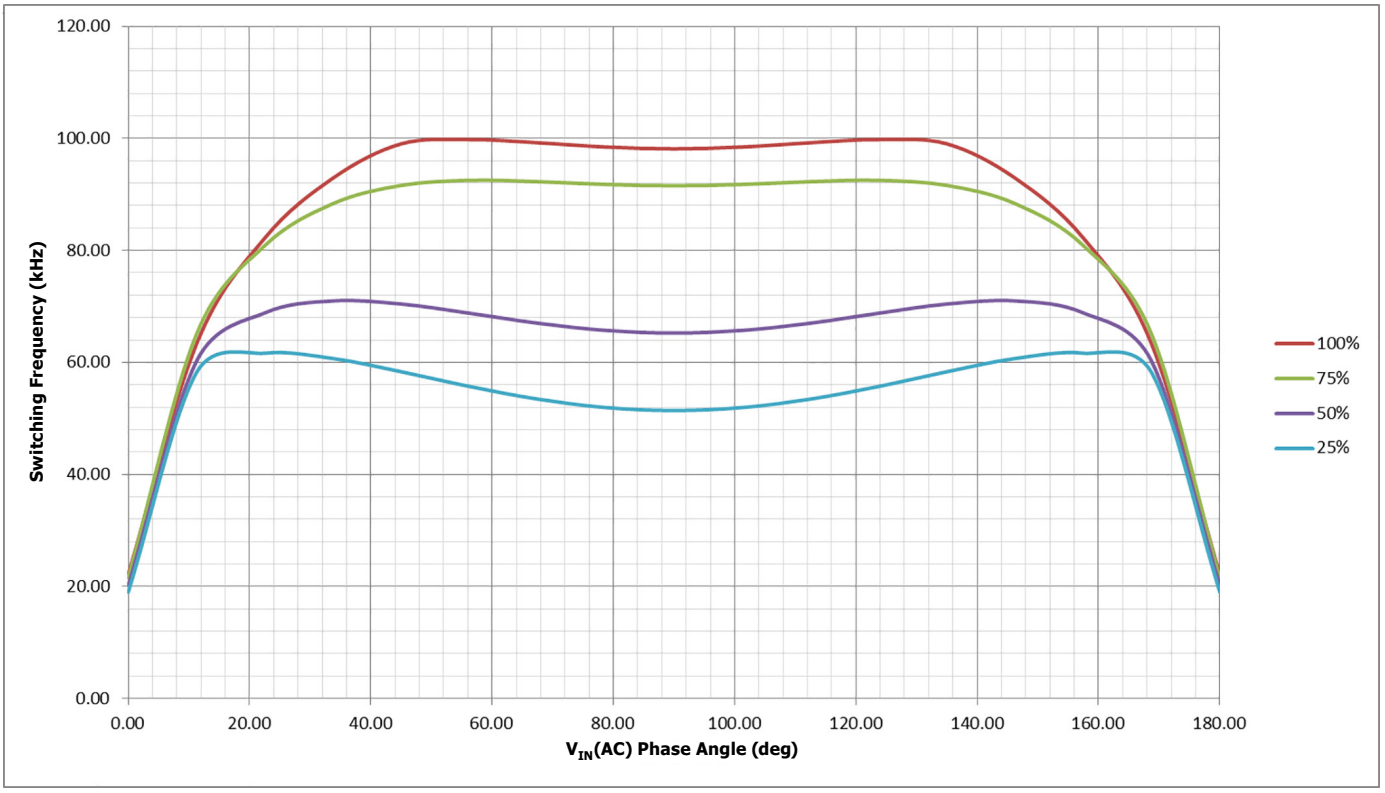


Figure 9. Frequency Variation Over Line Half-Cycle as a Function of load (V_{IN} = 115 VAC).

EcoSmart (Frequency Sliding and Spread-Spectrum Switching)

The HiperPFS-5 IC's include an EcoSmart function whereby the internal error signal (V_{ERR}) is used to detect the converter output power. This is used to set the average switching frequency as a function of output power.

As shown in the Figure 10 below, the off-time integrator control reference (V_{OFF}) is set by the internal error-voltage level (output power) to allow the converter to maintain output voltage regulation and flat conversion efficiency from 20% to 100% of rated load, which is essential to meet many efficiency directives. The degree of frequency slide is also controlled which is a function of input line voltage. The lower V_{OFF} slope as a function of input voltage reduces the average frequency range for high input line operation. Using this approach, the HiperPFS-5 IC enables the use of a smaller PFC inductor, while still keeping the switching frequency below 150 kHz across line and load to minimize the burden on EMI components.

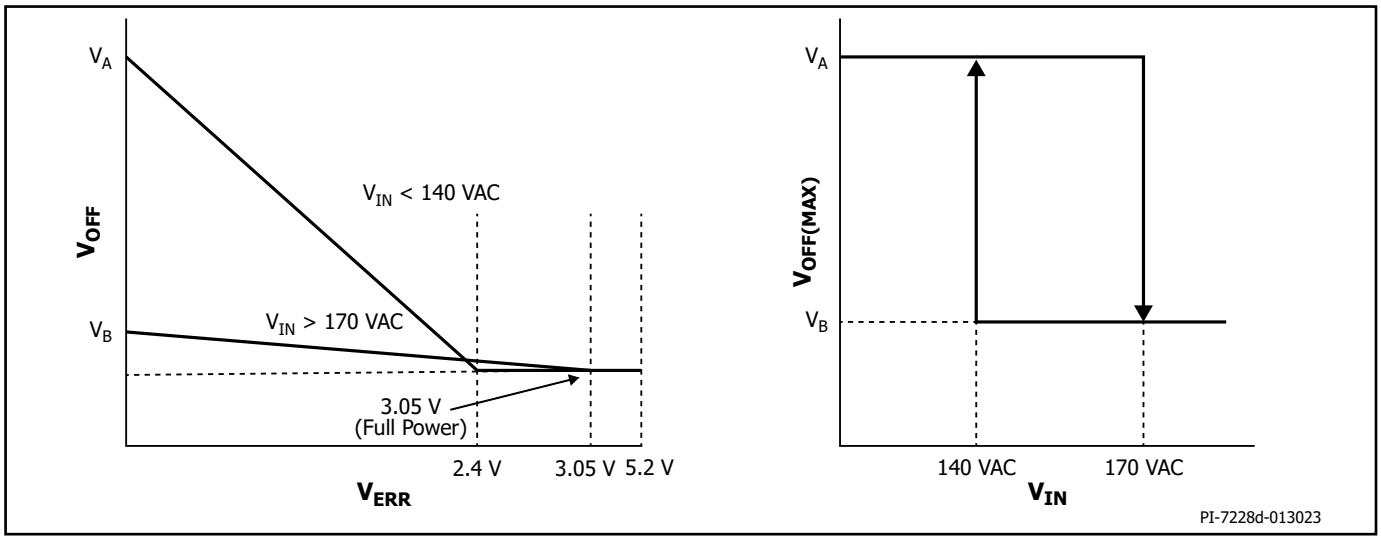


Figure 10. EcoSmart Frequency Sliding V_{OFF} vs. V_{ERR} and $V_{OFF(MAX)}$ vs. Input Voltage.

Power Good Signal For PFS517xF

The HiperPFS-5 features a power good (PG) circuit which comprises an internal comparator that turns an open-drain switch on during start-up when the sensed output voltage on the FEEDBACK pin rises to ~95% (V_{PG+}) of the output voltage threshold. During start-up, prior to the output voltage reaching V_{PG+}, the PG signal is in a high-impedance state (internal switch is in off-state).

The power good signal transitions from on to off-state when the sensed output voltage on the FEEDBACK pin falls to a user selected threshold, programmed via resistor on the POWER GOOD THRESHOLD (PGT) pin. The POWER GOOD THRESHOLD pin sources a fixed current $I_{PG(T)}$. This current in combination with the power good threshold resistor sets the threshold at which the power good signal transitions from the on-state to the high-impedance off-state as the PFC output falls out of regulation.

The power good comparator has an internal 81 µs de-glitch filter (t_{PGD}) to prevent noise events from falsely triggering the programmed VPG-threshold.

In the event a load fault prevents the boost from achieving regulation (above ~95% of the set output voltage threshold) the PG function will remain in the high-impedance state and so will not indicate when an output voltage has fallen below the user programmed V_{PG-} threshold. The V_{PG-} user programmed threshold is only enabled once the V_{PG+} threshold has been reached.

If the POWER GOOD THRESHOLD programming pin is tied to REFERENCE pin, the power good function is disabled and PG remains in the high-impedance (off) state. This is the preferred configuration when PG is not used. If the POWER GOOD THRESHOLD pin is shorted to the SIGNAL GROUND pin, the PG signal will transition to the on-state at V_{PG+} and remain low (on) until the PFC output voltage has fallen below the $V_{FB(UV)}$ threshold for greater than $t_{FB(UV)}$ seconds.

Similar to the disable condition described above, if the value of the PGT resistor is such that the V_{PG-} threshold is greater than the V_{PG+} threshold, the PG signal will latch off and remain in the high-impedance off-state.

The Power Good function is not valid under the following conditions:

A. VCC or VDR are not in a valid range of operation. VCC below UVLO- or VDR below $V_{VDR(UV-)}$ the power good function is not valid with the POWER GOOD pin in a high-impedance state.
B. POWER GOOD pin will go to high-impedance state when a soft shutdown is initiated by an over-temperature fault to provide early indication to secondary circuits of an OT (over-temperature) fault.
C. PGT is outside the valid programming range of between 225 V and 360 V. PGT voltages above this range, including PGT floating, will prevent PG from transitioning to active pull-down. PGT voltages below this range result in PG de-assertion at the output under-voltage ($V_{FB(UV)}$) threshold.
D. Once the start-up sequence check has passed and the converter goes into start-up, if PGT is opened, then the PG signal will remain latched in the high-impedance state until the controller is reset.

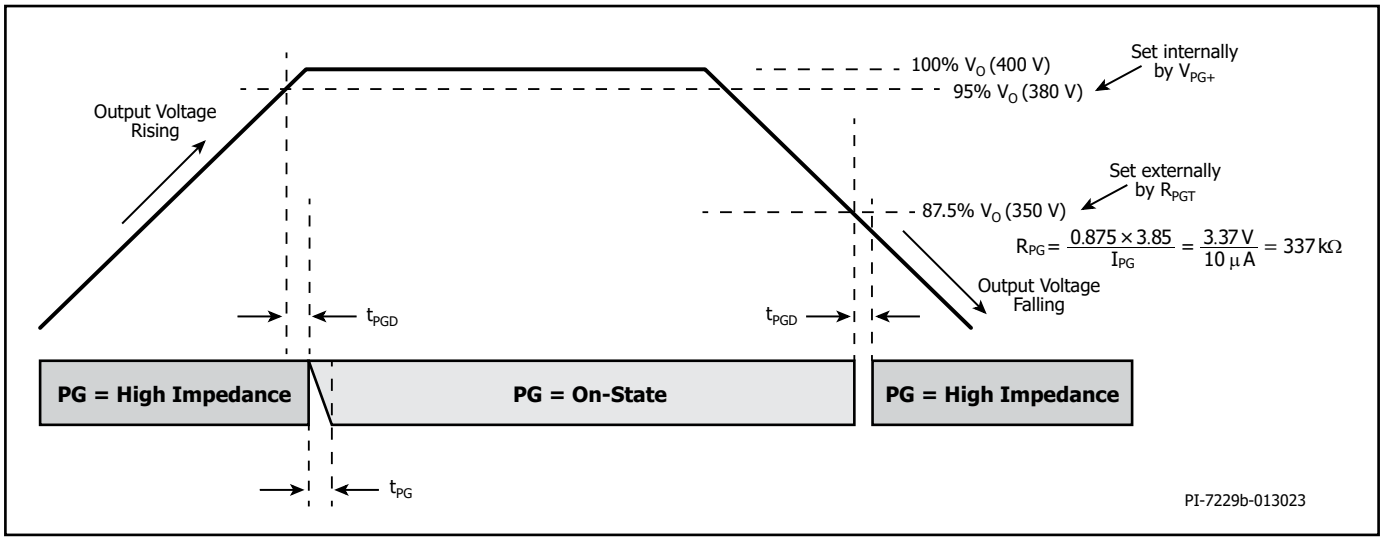


Figure 11. Power Good Function Description.

Boost-Follower For PFS527xF

The HiperPFS-5 IC's feature a Boost Follower (BF) circuit which controls the output voltage as a function of input voltage. This feature improves efficiency at low-line by reducing the target output voltage. When the input peak voltage indicates low-line, the PG/BF pin is in a high impedance state (internal switch is in off-state). When the input peak voltage is sensed to be in high-line, the PG/BF pin is turned on (low impedance state) (internal switch is switched to ground). The low-line and high-line hysteresis is set at 140 VAC and 170 VAC.

As shown in Figure 13, at high-line input, the output voltage is equal to:

$$V_O = V_{FB} \times \left(\frac{R_{UPP} + R_{BF} // R_{DWN}}{R_{BF} // R_{DWN}} \right)$$

and at low-line input, the output voltage is equal to:

$$V_O = V_{FB} \times \left(\frac{R_{UPP} + R_{DWN}}{R_{DWN}} \right)$$

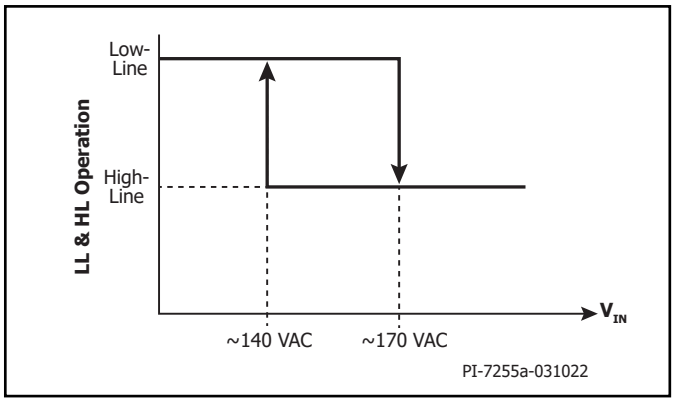


Figure 12. Boost Follower Low-Line and High-Line operation vs. Input Voltage.

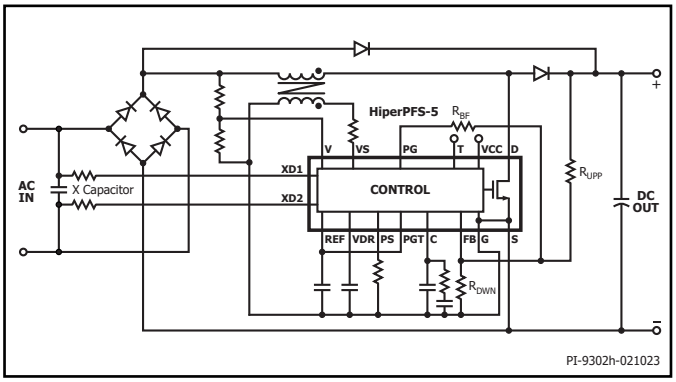


Figure 13. System Schematic with a Line Dependent V_{OUT} (Boost Follower).

Selectable Power Limit

The PS (Power Selection) pin is used to program the output power of the HiperPFS-5. The power is programmed with a resistor connected to the G pin, in 10% steps, between 70% to 100% of the nominal output power.

Turns Ratio For Auxiliary Winding

The VS pin is connected to the auxiliary winding of the PFC inductor through a resistor to detect the valley switching. This resistor can adjust the proper delay for a given application so that the turn-on of the PowiGaN happens at the valley of the voltage on the DRAIN pin. The delay depends on the resistance of this resistor and the effective capacitance on the VS pin. If the resistor is closer to the VS pin, the effective capacitance on the VS pin is smaller with a shorter delay.

Oppositely, if the resistor is put far from the VS pin, then the effective capacitance on the VS pin is larger with a longer delay. The initial design recommended value for the resistor is 10 kΩ and put this resistor close to VS pin.

The maximum turns ratio (N_{MAX}) of auxiliary winding is calculated as $N_{MAX} = (V_{OMIN} – V_{ACPEAK})/ V_{VS1}$. Here, the V_{OMIN} is minimum output voltage considering the ripple tolerance. If V_O = 400 V and assuming 3% tolerance, the V_{OMIN} is 388 V; V_{ACPEAK} is the peak voltage of maximum high-line input. For universal AC input, $V_{ACPEAK} = \sqrt{2} \times 265 \approx 375$ V; V_{VS1} is the valley sensing positive threshold with typical value 0.88 V. From the above equation, it can calculate the maximum turn ratio (N_{MAX}) is about 15. The recommended turns ratio for auxiliary winding is ranged from 10 to 15.

Resistor (Ohms)	Power Selection	Comments
>400 k	100%	Leaving pin open is acceptable
100 k – 200 k	90%	
25 k – 50 k	80%	
<6 k	70%	Connecting pin short to G node is acceptable

Table 2. Power Programming Resistances (Resistor Between PS Pin and G Pin).

Protection Modes

Brown-In Protection

The VOLTAGE MONITOR pin has an input line undervoltage detection feature to limit the minimum start-up voltage. This detection threshold will inhibit the device from starting at input voltages below brown-in point and above input peak voltages of 400 V_{PK}.

Brown-Out Protection

The VOLTAGE MONITOR pin features a brown-out protection mode whereby the HiperPFS-5 will turn-off when the VOLTAGE MONITOR pin voltage is below the line undervoltage threshold (VBR-) for a period exceeding $t_{BROWN-OUT}$ (brown-out debounce period). In the event that a single half-line cycle is missing (normal operating line frequency is in the range of 47 Hz to 63 Hz) the brown-out protection feature will not be activated.

Once brown-out has been triggered, the HiperPFS-5 IC's soft-shutdown gradually reduces the internal error-voltage to zero over a period of 1 ms which ramps the power PowiGaN on-time to zero. The onset of this soft-shutdown is aligned to the next line cycle zero crossing to minimize reactive component di/dt transients and allow time for the energy stored within the boost choke as well as the input EMI filter to dissipate. This helps minimize voltage transients after the bridge rectifier and prevent false restarts.

The device will enter an auto-restart, including FMEA pin fault checks and other start-up qualifications prior to checking that the line voltage is above the brown-in threshold (VOLTAGE MONITOR pin voltage above V_{BR+}).

After a brown-in event, and once the $t_{START-UP}$ timer expires, the line voltage brown-out threshold is reduced to $V_{BR(NTC)}$ and the brown-out timer is extended to $t_{BROWN-OUT(NTC)}$ to allow for the drop in line voltage caused by the voltage drop across the in-rush limiting negative temperature coefficient (NTC) thermistor in series with the input line.

If the $t_{BROWN-OUT(NTC)}$ debounce timer is triggered by the sensed line voltage dropping below the $V_{BR(NTC)}$ threshold but the line voltage recovers to above the $V_{BR(NTC)}$ threshold before the $t_{BROWN-OUT(NTC)}$ expires, then the $t_{START-UP}$ timer will be re-started. If the line does not recover above the $V_{BR(NTC)}$ threshold before the $t_{BROWN-OUT(NTC)}$ debounce timer expires a shutdown will occur.

After the $t_{STARTUP}$ timer has expired, if the VOLTAGE MONITOR pin voltage rises above V_{BR-NTC}, the brown-out debounce timer will switch to normal period (t_{BRWN_OUT}) and the brown-out threshold will switch to V_{BR-}. If the VOLTAGE MONITOR pin voltage is not above V_{BR-} after the subsequent t_{BRWN_OUT} timer has expired then a brown-out shutdown will occur.

HiperPFS-5 IC's incorporates input waveform discrimination to determine if the line signal peak-to-average voltage ratio is representative of a sine wave or a high-duty-cycle square wave. The brown-out threshold is reduced to $V_{BR(SQ)}$ when a high duty cycle (UPS) square wave is detected.

VCC Undervoltage Protection (UVLO) for PFS527x Parts

The BIAS POWER (VCC) pin has an undervoltage lock-out protection which inhibits the IC from starting unless the applied VCC voltage is above the VCC_{UVLO+} threshold.

The IC initiates a start-up once the BIAS POWER pin voltage exceeds the VCC_{UVLO+} threshold. After start-up the IC will continue to operate until the BIAS POWER pin voltage has fallen below the VCC_{UVLO-} level.

PFS517x parts are using VDR for UVLO protection.

Line Dependent Over-Current Protection (OCP)

The device includes a cycle-by-cycle over-current protection mechanism which protects the device in the event of a fault. The OCP circuit protects the internal power switch. This intends to protect the converter from output short-circuit or overload fault conditions.

The OCP limit is set as a function of the input line voltage. This helps to restrict power limit due to short-circuits as well as minimize the stress on the switch due to current overloads at higher input line conditions.

Figure 14 below illustrates the hysteretic adjustment of the OCP levels as a function of VOLTAGE MONITOR pin line sense.

The low-line OCP (the greater of the two settings) is selected when the peak of the input line voltage drops below 140 VAC for 3 less consecutive half-cycles and the high-line OCP level (the less of the two settings)is selected when the input line voltage rises above 170 VAC for 1 half-cycle, (except in follower mode, as described in the subsequent sections).

The HiperPFS-5 IC implements a high input line OCP after detecting the VOLTAGE MONITOR pin voltage being above the high-line threshold, $V_{V(HIGH+)}$. The controller reverts back to low-line OCP (as well as low-line frequency slide) only after 3 consecutive half-line cycle peak values that are below the low-line threshold $V_{V(HIGH-)}$. In the event of a line drop-out, the controller may revert from high-line to low-line set-points if the drop-out exceeds 37 ms (nominal).

A feed-forward feature updates the controller to high-line status rapidly, as soon as the input voltage exceeds V_{HIGH+}. This feature has particular benefit for high-line hard-start conditions after a long AC line drop-out where the peak detector may initially indicate a low input line condition.

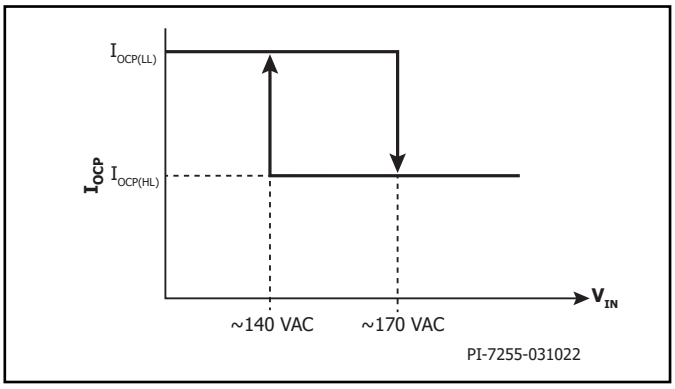


Figure 14. Line Dependent OCP.

Safe Operating (SOA) mode

Since the cycle-by-cycle OCP mechanism described above does not prevent the possibility of inductor current 'stair-casing', and an SOA mode is also featured.

Rapid build-up of the switch current can occur in the event of inductor saturation or when the input and output voltage differential is small resulting in too little inductor reset time.

The SOA mode is triggered whenever the switch current reaches current limit (I_{OCP}) and the on-time is less than $t_{ON(SOA)}$. The SOA mode forces an off-time equal to $t_{OFF(SOA)}$ and pulls the internal error-voltage (V_{ERR}) down by 1/2 of its maximum value in order to ensure the switch remains within its SOA.

Fast Output Voltage Overvoltage Protection

The HiperPFS-5 features a voltage feedback threshold comparator on the FEEDBACK pin which detects an output overvoltage condition to allow rapid response, (independent of the COMPENSATION pin response), to prevent hazardous voltage conditions from occurring. The overvoltage protection is hysteretic – the voltage on the FEEDBACK pin must drop by 0.1 V (equating to an output voltage drop of 10 V) before switching is re-started.

FEEDBACK to COMPENSATION Pin Short Detection Safeguard

The PFC controller continuously monitors the FEEDBACK and COMPENSATION pins to ensure that there are no potential short conditions between the adjacent FEEDBACK and COMPENSATION pins, which could result in output overvoltage conditions. In the event a potential short is detected, a rapid short check is performed and a shutdown is executed in the event that a suspected short is validated.

Open FEEDBACK Pin Protection

The FEEDBACK pin continuously sinks a static current of I_{FBPD} ([VCC >VCC_{UVLO+}]) to protect against a fault related to an open FEEDBACK pin or invalid feedback divider network. The internal current sink introduces a small static offset to the output regulation which can be accounted for in selecting the output feedback regulation components (FEEDBACK pin divider).

Hysteretic Thermal Protection

The thermal shutdown circuit senses the controller die temperature which is well coupled to the power switch through the exposed, source pad and PCB copper cooling plane. The OTP (over-temperature protection) threshold is set at 130 °C typical with 49 °C hysteresis.

When the controller die temperature rises above this threshold (OTP), the controller initiates a soft-shutdown and remains disabled until the controller die temperature falls by ~49 °C, at which point the device will re-initiate the start-up sequence.

Safety of X Capacitor Discharge

X capacitor discharge function can be implemented by connecting XD1 to one AC line input through an external series resistor and XD2 to the other AC input line input through a separate external resistor.

X capacitor discharge function meets safety requirements even if connection is placed before the system input fuse. If a short-circuit is placed between XD1 and XD2 terminals, the system is identical to existing systems where X capacitor discharge function is not used.

With regard to open circuit tests, it is not possible to create a fault condition through a single pin fault (for example lifted pin test) since there are two pins connected to both XD1 and XD2. If several pins are lifted to create an open-circuit, the condition is identical to an open circuit X capacitor discharge resistor in existing systems where X capacitor discharge function is not disabled.

Total X Capacitance	Total Series Resistance
100 nF to 6 µF	7.5 MΩ to 142 kΩ

Table 3. X Capacitance and Discharge Resistance.

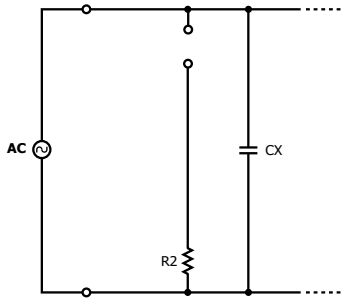
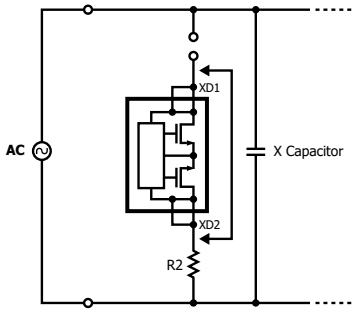
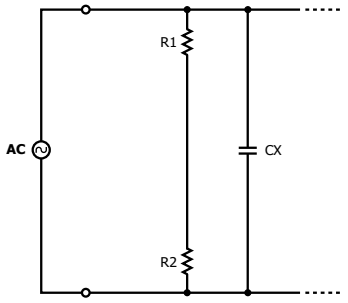
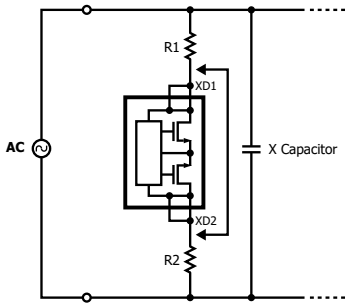
Test	Test With Existing System	CAPZero Equivalent	Comments
Open Circuit: Disconnect one pin of any device to see effect on system			**Open Circuit:** Lifting any one pin of XD1 and XD2 pins has no effect as 2 pins are connected to each drain terminal. The only way to create an open circuit is by lifting the leads of one of the discharge resistors. This is equivalent to an existing system without the active capacitor discharge function.
Short-Circuit: Short any two adjacent pins to see effect on system			**Short-Circuit:** Shorting XD1 and XD2 pins creates a condition equivalent to an existing system not using an active X capacitor discharge function.

Table 4. Single Point of Failure (SPOF) Tests as Pertaining to Failure Modes of the X Capacitor Discharge. HiperPFS-5 Device Passes Both Tests.

Application Example 1

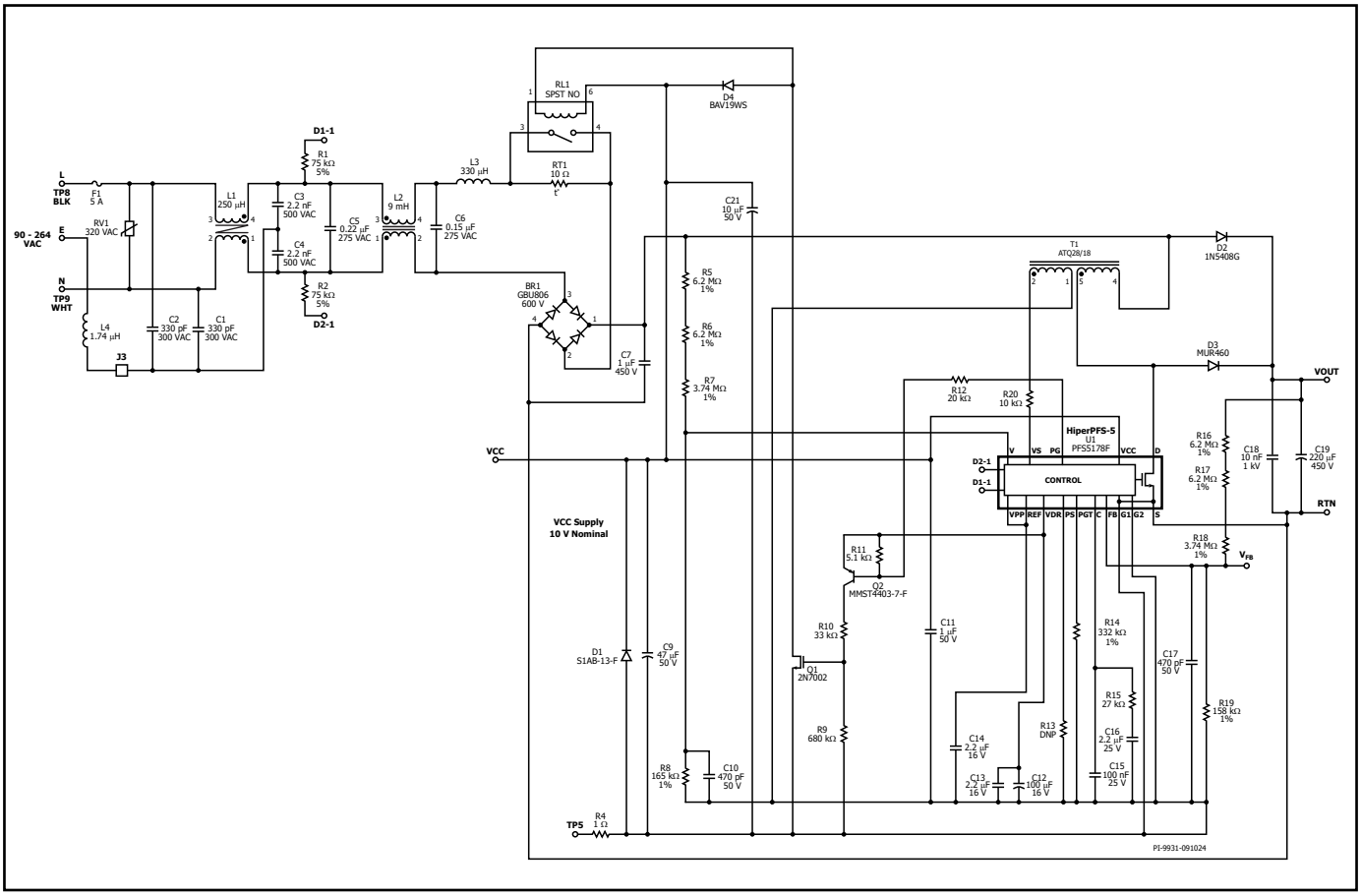


Figure 15. Schematic of a 250 W, 400 VDC Output PFC Circuit using PFS5178F Device.

The circuit shown in Figure 15 is a power factor correction circuit that uses a PFS5178F IC. This design delivers a continuous output power of 250 W with a regulated nominal output voltage of 400 V. It maintains a high input power factor and system efficiency across line and load without the need for external heatsinking.

Fuse F1 provides input over-current protection and isolates the circuit from the AC line in the event of a fault. Metal oxide varistor RV1 protects the circuit during surge events by clamping the input voltage. Diode bridge BR1 rectifies the AC input voltage. Capacitors C1, C2, C3, C4, C5, and C6 and inductors L1, L2, L3, and L4 form the EMI filter. Resistors R1 and R2 are used to discharge the X capacitors via the integrated automatic X capacitor discharge feature of the HiperPFS-5 controller U1. The discharge resistors are connected across the X capacitors only when the AC line is disconnected, eliminating the losses that would occur with conventional circuits.

Thermistor RT1 limits the inrush input current at startup. The electromechanical relay RL1 is used to bypass the thermistor once the output voltage reaches nominal (indicated by the POWER GOOD signal from the PG pin of integrated controller U1). Resistors R9, R10, R11, and R12 along with transistors Q1 and Q2, drive the relay RL1. Diode D4 clamps the voltage when the relay is turned off. Resistor R14 sets the POWER GOOD signal threshold via the PGT pin.

Film capacitor C7 provides input decoupling and charge storage to reduce input current ripple. The boost converter is formed by inductor T1, boost diode D3, output capacitor C19, and the integrated 750 V PowiGaN switch. The HiperPFS-5 device controls the input current to the power supply and maintains regulation of the output DC voltage. Diode D2 provides an inrush current bypass path when AC line is first applied before PFC operation starts. An auxiliary winding on the inductor T1 is used to sense the voltage difference between the Drain of the PowiGaN switch and the rectified voltage, providing the information necessary for valley switching. Resistor R20 limits the current through the VS pin, providing fine timing adjustment for the valley-switching circuit. Capacitor C18 provides a bypass path to the ground for high frequency switching noise.

Capacitors C9 and C11 provide bypass and filtering for the VCC pin of the HiperPFS-5 controller while diode D1 provides reverse polarity protection. Capacitors C12 and C13 provide bypass and filtering for the internal regulator on the VDR pin used to supply the driver circuitry of the HiperPFS-5 controller. Capacitor C14 provides bypass and filtering for the internal regulator on the REF pin used to supply the control circuitry of the HiperPFS-5 controller.

Resistor R13 sets the maximum continuous output power of the HiperPFS-5 and is left unpopulated for full power operation. Resistors R5, R6, R7, and R8 along with capacitor C10 provide input voltage information to the V pin. Resistors R16, R17, R18, and R19 along with capacitor C17 provide output voltage information to the FB pin. Capacitors C15 and C16 along with resistor R15 shape the loop response of the PFC circuit.

Application Example 2

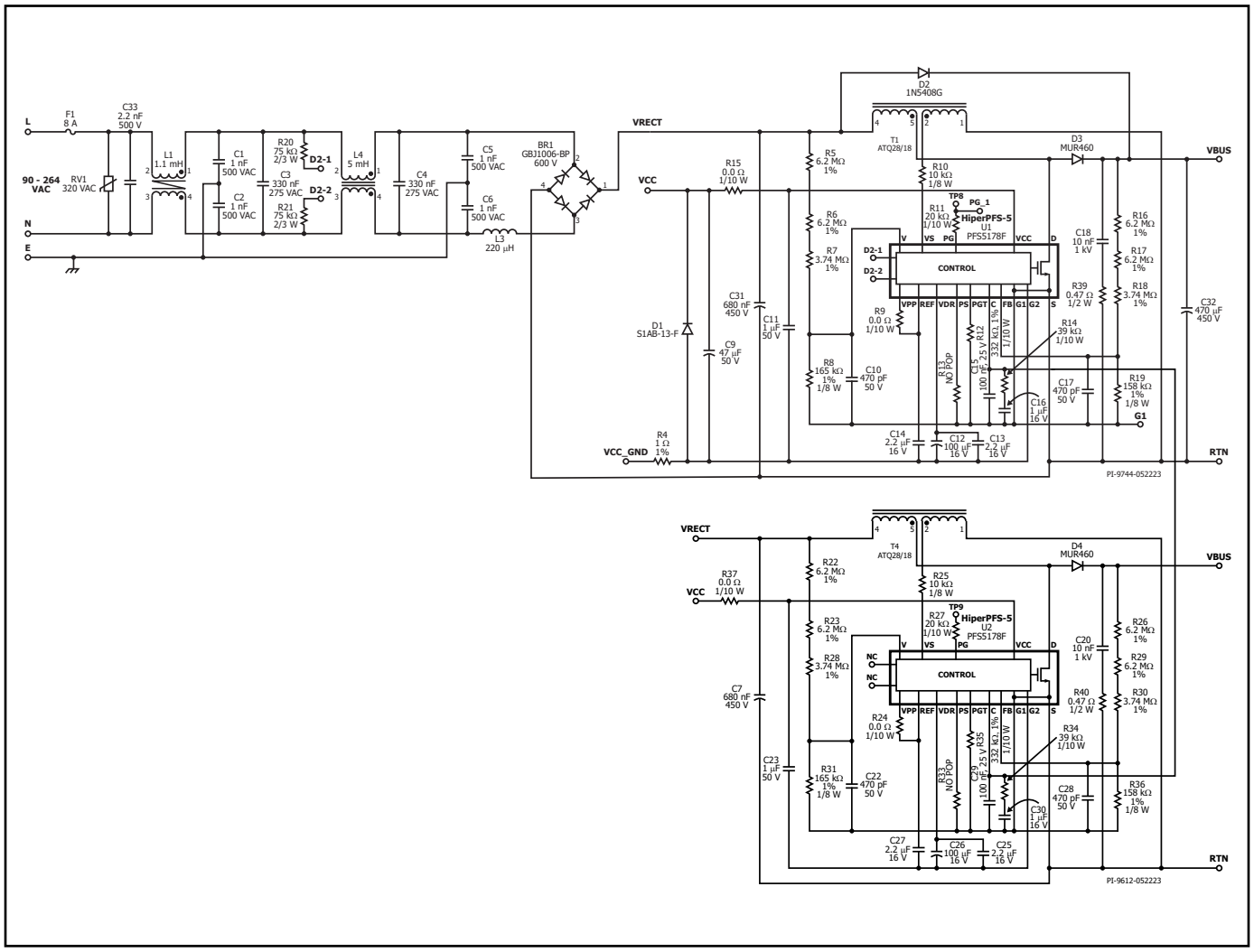


Figure 16. Schematic of a 500 W, 400 VDC Output Parallel PFC Circuit using PFS5178F Devices.

The circuit shown in Figure 16 is a power factor correction circuit using 2 PFS5178F devices in parallel. This design delivers a continuous output power of 500 W with a regulated nominal output voltage of 400 V, maintaining a high input power factor and system efficiency across line voltages and load without external heatsinking.

Fuse F1 provides input over-current protection to the circuit and isolates it from the AC line in the event of a fault. Metal oxide varistor RV1 protects the circuit during surge events by clamping the input voltage. Diode bridge BR1 rectifies the AC input voltage. Capacitors C1, C2, C3, C4, C5, C6, and C33 and inductors L1, L3, and L4 form the EMI filter. Resistors R20 and R21 are used to discharge the X capacitors via the integrated automatic X capacitor discharge feature of the HiperPFS-5 controller U1. The discharge resistors are connected across the X capacitors only when the AC line is disconnected, eliminating the losses that would occur with conventional circuits.

Film capacitors C7 and C31 provide input decoupling and charge storage to reduce input current ripple. Two boost converters are formed by inductors T1 and T2, boost diodes D3 and D4, output capacitor C32, and the integrated 750 V PowiGaN switches. The HiperPFS-5 devices control the input current to the power supply and maintain regulation of the output DC voltage. Diode D2 provides an inrush current bypass path when AC line is first applied before PFC operation starts. Auxiliary windings on the inductors T1 and T2 are used to sense the voltage difference between the Drain of the PowiGaN switches and the rectified voltage, providing information for valley switching. Resistors R10 and R25 limit the current through the VS pins of the HiperPFS-5 controllers U1 and U2 respectively, providing fine timing adjustment for the valley-switching circuit. Capacitor C18 and C20 along with resistors R39 and R40 provide bypass paths to the ground for high frequency switching noise.

Capacitors C11 and C23 provide bypass and filtering for the VCC pins of the respective HiperPFS-5 controllers while diode D1 provides reverse polarity protection for the VCC pins. Capacitors C12, C13, C25, and C26 provide bypass and filtering for the internal regulators on the VDR pins used to supply the driver circuitry. Capacitors C14 and C27 provide bypass and filtering for the internal regulator on the REF pins used to supply the control circuitry for the respective HiperPFS-5 controllers.

Resistors R13 and R33 set the maximum continuous output power for each of the HiperPFS-5 devices and are left unpopulated for full power operation. Resistors R5, R6, R7, R8, R22, R23, R28, and R31 along with capacitors C10 and C22 provide the rectified input voltage

information to the V pins. Resistors R16, R17, R18, R19, R26, R29, R30, and R36 along with capacitors C17 and C28 provide output voltage information to the FB pins. Capacitors C15, C16, C29, and C30 along with resistors R14 and R34 shape the loop response of each PFC circuit. Resistor R12 and R35 sets the POWER GOOD signal threshold via the PGT pins.

Parallel operation and power sharing are accomplished by connecting the C pins of the U1 and U2 together. The C pin is used to scale the output power of the PFC circuit. By connecting the C pins together, output power information is shared between the two PFC circuits.

Recommended Compensation Values

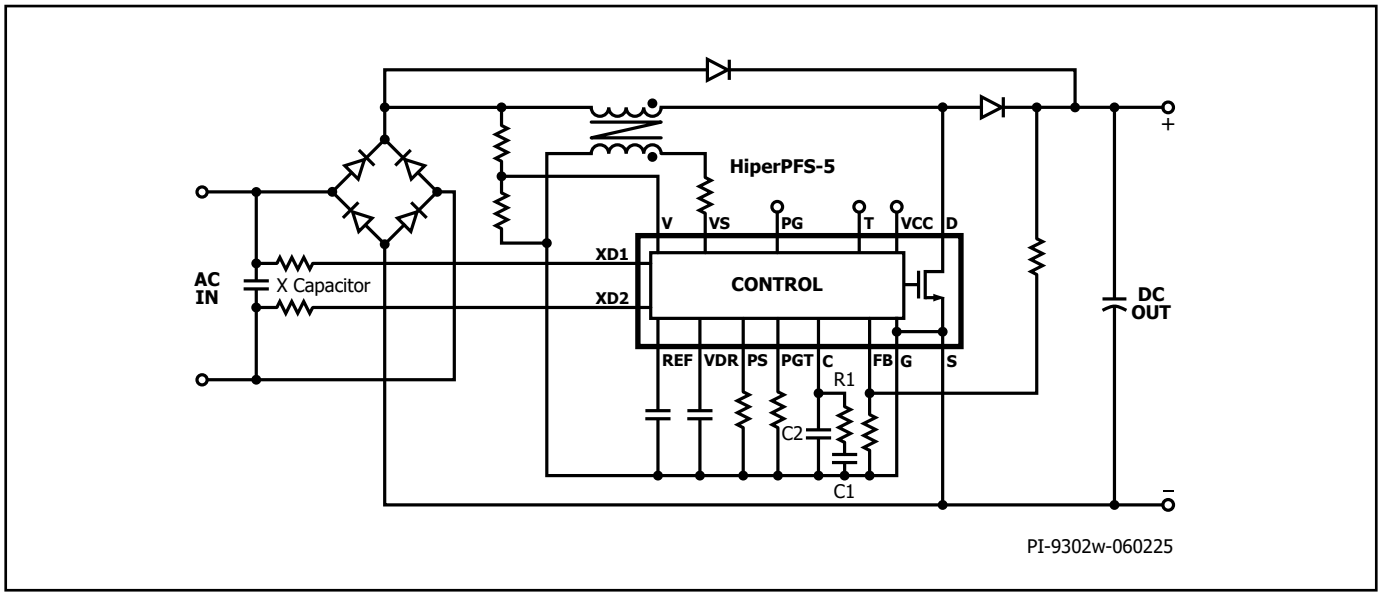


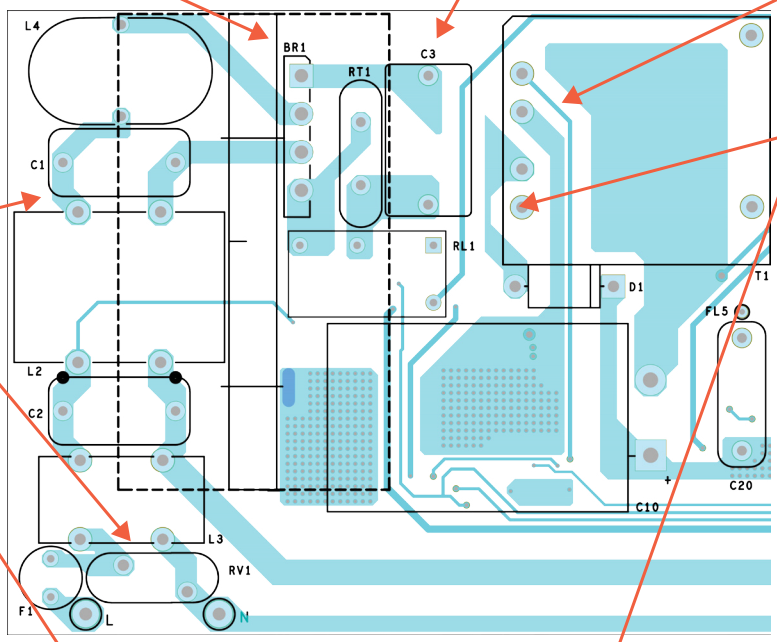
Figure 17. Typical Application Circuit.

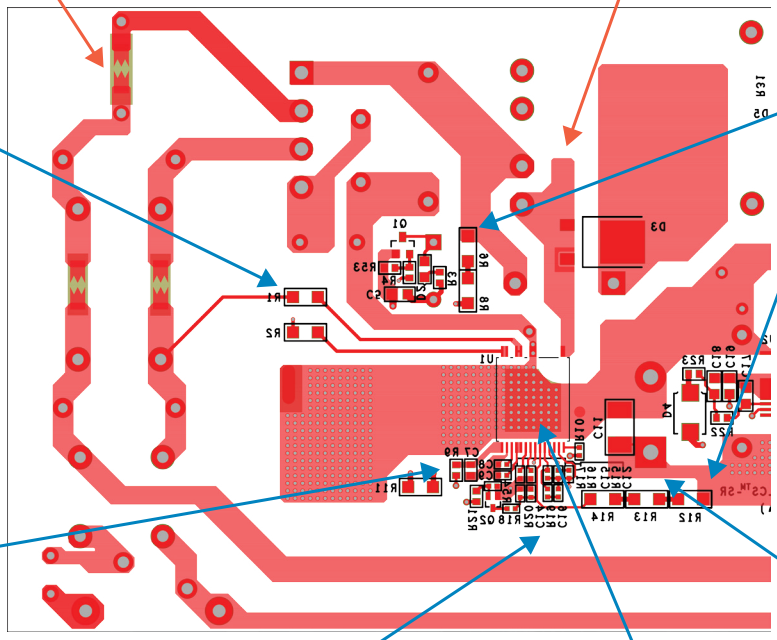
For most designs, to achieve an appropriate phase margin with a gain crossover frequency of < 10 Hz, the recommended compensation values are: R1 = 27 kΩ, C1 = 2.2 μF, C2 = 100 nF. These values were chosen for a 250 W design using an output capacitance of 220 μF.

For boost follower configurations, the recommended compensation values are: R1 = 18 kΩ, C1 = 4.7 μF, C2 = 470 nF. These values were chosen for a 250 W design using an output capacitance of 220 μF.

Adjusting output capacitance will necessitate changes to compensation values in order achieve the desired gain crossover frequency and phase margin at low input voltages.

Layout Example





Diode bridge BR1 heatsink is connected to the ground and acts a shield to prevent noise coupling between BR1, relay RL1, and the EMI components.

Capacitor C3 is placed directly after the bridge diode BR1 through planes for effective decoupling.

Inductor T1 pin 3 (return node of the sense winding) is directly connected to the power ground plane (connected to S-pin) of the HiperPFS-5 device.

Inductor T1 pins 4 and 5 (main winding), boost diode D3, HiperPFS-5 Drain pin are placed tightly together and connected through planes to minimize the switching loop.

EMI filter components L2, L3, L4, C1, and C2 are placed away from any switching nodes with high dv/dt or di/dt.

Fuse F1 and varistor RV1 are placed directly at the input terminals.

Spark gaps are added across inductive EMI components to provide a discharge path during ESD/surge.

Input voltage sensing resistor R6 is connected directly to the positive plane from the decoupling capacitor C3 for accurate sensing.

Output voltage sensing resistor R12 is connected directly to the positive plane from the output capacitor C10 for accurate sensing.

Discharge resistors R1 and R2 are placed away from the EMI components and routed away from any switching nodes with high dv/dt or di/dt.

Capacitors C7, C8, and C9 are placed adjacent to the VCC, VDR, and REF pins of the HiperPFS-5 device and are connected to the nearest G pin (pin 13).

Valley sensing resistor R10 and voltage monitor components R15 and C12 are placed adjacent to the respective VS and V pins of the HiperPFS-5 device.

Compensation components R19, C15, and C16 are placed adjacent to the C pin while feedback components R20 and C14 are placed adjacent to the FB pin of the HiperPFS-5 device. Resistor R16 and R17 are also placed close to their respective PGT and PS pins. The corresponding ground nodes are connected to nearest G pin (pin 2).

Maximize PCB heatsinking by soldering the exposed thermal pad on the bottom side of the HiperPFS-5 package, extending the ground plane, and by using thermal relief vias.

Figure 18. Typical Application Circuit.

Quick Design Checklist

As with any power supply design, all HiperPFS-5 family designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that peak VDS does not exceed 650 V at lowest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level above the highest rated load and before the power supply output voltage starts falling out of regulation. When measuring Drain-Source voltage of the PowiGaN switch, a high-voltage probe should be used. When the probe's sprung hook is removed, a metallic ring surrounding the probe tip can be seen. This ring is at ground potential and the best ground connection point for making noise-free measurements. Wrapping bare wire around the ground ring and then connecting that ground wire into the circuit with the shortest possible wire length, then connecting the probe tip to the point being measured, ensures error-free measurement. Probe should be compensated according to probe manufacturer's guidelines to ensure error-free measurement.
2. Maximum Drain Current – Drain current can be measured indirectly by monitoring inductor current. A current probe should be inserted between the bridge rectifier and inductor connection. At maximum ambient temperature, minimum input voltage and maximum output load, verify Drain current waveforms at start-up for any signs of inductor saturation. When performing this measurement with Sendust inductor, it is typical to see inductor waveforms that show exponential increase in current due to permeability drop. This should not be confused with hard saturation.
3. Thermal Check – At maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the HiperPFS-5 device, PFC inductor, output diodes and output capacitors. Thermal margin should be enough to allow for the part-to-part variation of the RDS(ON) of HiperPFS-5 device, as specified in the data sheet. A maximum package temperature of 100 °C is recommended to allow for these variations.
4. Input PF should improve with load, if performance is found to progressively deteriorate with loading, it is a sign of possible noise pick-up by the VOLTAGE MONITOR pin circuit, the FEEDBACK pin circuit, and the COMPENSATION pin circuit.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage (non-repetitive pulse) ..... -0.3 V to 750 V[6]
DRAIN Pin Voltage (continuous) ..... -0.3 V to 650[3] V
DRAIN Pin Peak Current: PFS5x73F .....6.5 A[8]
PFS5x74F ..... 10.0 A[8]
PFS5x75F ..... 14.0 A[8]
PFS5x76F ..... 17.0 A[8]
PFS5x77F .....24.0 A[8]
PFS5x78F .....33.0 A[8]
VCC Pin .....-0.3 V to 35 V
V_S, V, FB, PG, PGT, PS, REF, VDR, C Pins .....-0.3 V to 5.6 V
XD1/XD2 Pin Voltage[7] ..... 1000 V
XD1/XD2 Pin Current[8].....5 mA
Storage Temperature .....-65 to 150 °C
Operating Junction Temperature[4]..... -40 to 150 °C
Ambient Temperature.....-40 to 105 °C
Lead Temperature[5]..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Self-supply not active.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Non-repetitive pulse.
7. Voltage of XD1 pin relative to XD2 pin in either polarity.
8. The peak current is allowed while the XD1/XD2 voltage is simultaneously less than 400 V.

Thermal Resistance

Thermal Resistance: PFS5x73F
(θ_{JA})..... 61 °C/W[1], 53 °C/W[2]
(θ_{JC}).....7 °C/W[3]
PFS5x78F
(θ_{JA}).....51 °C/W[1], 43 °C/W[2]
(θ_{JC}).....1.1 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm2) 2 oz. (610 g/m2) copper clad.
2. Soldered to 1 sq. inch (645 mm2), 2 oz. (610 g/m2) copper clad.
3. The case temperature is measured at the bottom of the package body on the exposed pad.

Parameter	Symbol	Conditions SOURCE = 0 V, T_J = -40 to +125 °C (See Note C)	Pin	Min	Typ	Max	Units
Currents							
Current Consumption – In Burst Mode No Switching	$I_{CC(BURST)}$	VCC = 12 V, V_{FB} = 3.85 V, C < $V_{ERR(MIN)}$ 0 °C < T_J < 100 °C V = 1.414 V	VCC		700	850	µA
Leakage Current in UVLO State	I_{oz}	0 V < Pin Voltage < REF T_J = 25 °C V_{DR} < $V_{DR(UV+)}$	V, FB, C, PGT		±10		nA
		V_{PG} = REF T_J = 25 °C V_{PG} = V	PG		±0.1		µA
Pull-Down Current on Feedback	$I_{FB(PD)}$	0 °C < T_J < 100 °C V_{FB} = 5 V	FB		100	150	nA

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)		Min	Typ	Max	Units
Control Functions							
Maximum Operating "On-Time" Controller	$t_{ON(MAX)}$				34		µs
Maximum Operating "Off-Time" Controller	$t_{OFF(MAX)}$	No valleys detected on the VS pin (operation in CCM mode)			250	300	µs
Feedback							
Internal Feedback Error Voltage Reference	$V_{FB(REF)}$	T_J = 25 °C		3.82	3.85	3.88	V
Feedback Error-Amplifier Transconductance Gain	Gm	3.75 V < V_{FB} < 3.95 V 0 °C < T_J < 100 °C C = 4 V		75	90		µA/V
Soft Shutdown Time	$t_{SHUTDWN}$	See Note A			1.00		ms
FEEDBACK Pin Start-Up/ Fault Threshold	$V_{FB(OFF)}$	0 °C < T_J < 100 °C			0.64	0.71	V
FEEDBACK Pin Undervoltage Assertion Threshold	$V_{FB(UV)}$	0 °C < T_J < 100 °C		2.09	2.25	2.36	V
FEEDBACK Pin Overvoltage Assertion Threshold	$V_{FB(OV+)}$	0 °C < T_J < 100 °C		4.00	4.10		V
FEEDBACK Pin Overvoltage Deassertion Threshold	$V_{FB(OV-)}$	0 °C < T_J < 100 °C			4.00	4.10	V
FEEDBACK Pin Overvoltage Hysteresis	$V_{FB(OVHYST)}$	0 °C < T_J < 100 °C			0.1		V
Voltage on C Pin That Triggers Switching During a Burst-Mode Recovery, or When Commencing Soft-Start (COMPENSATION Pin Burst Disable Threshold)	$V_{ERR(MIN+)}$	0 °C < T_J < 100 °C	V_{IN} < 140 VAC		0.39		V
			V_{IN} > 170 VAC		0.19		
Voltage on C Pin That Suppresses Switching, Causing the Device to Enter Burst-Mode (Burst Enable Threshold)	$V_{ERR(MIN-)}$	0 °C < T_J ≤ 100 °C	V_{IN} < 140 VAC		0.34		V
			V_{IN} > 170 VAC		0.13		
Hysteresis of $V_{ERR(MIN)}$ (COMPENSATION Pin Burst Threshold Hysteresis)	$V_{ERR(HYST)}$	$V_{ERR(MIN+)}$ - $V_{ERR(MIN-)}$ 0 °C < T_J < 100 °C	V_{IN} < 140 VAC		0.05		V
			V_{IN} > 170 VAC		0.06		

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)	Min	Typ	Max	Units
Line Sense / Peak Detector						
Line Sense and Peak Detector Input Voltage (Line-Sense Input Voltage Range)	$V_{V(RANGE)}$	The voltage on V may exceed the upper specification, however the line sense function is saturated at its full scale. Not tested.			4	V
Brown-In Threshold Voltage	V_{BR+}	0 ºC < T_J < 100 °C		1.102		V
Brown-Out Threshold Voltage	V_{BR-}	0 ºC < T_J < 100 °C	0.86	0.895	1.12	V
Brown-Out Threshold for Square Wave (Brown-Out Threshold for High Duty Cycle Square Wave)	$V_{BR(SQ)}$	0 ºC < T_J < 100 °C See Note A		0.86		V
Soft-Start Brown-Out Threshold Voltage (Start-Up Brown-Out Threshold Voltage (During NTC Warm-Up Time))	$V_{BR(NTC)}$	0 ºC < T_J < 100 °C See Note A		0.74		V
Brown-In/Out Hysteresis (V_{BR+} - V_{BR-}) (Brown-In / Out Hysteresis (After NTC Warm-Up Time)	$V_{BR(HYST)}$	0 ºC < T_J < 100 °C	190	207	220	mV
Brown-Out Debounce Timer	$t_{BROWN-OUT}$	See Note A		54		ms
Brown-Out Debounce Timer During Start-Up with VBR_NTC Threshold	$t_{BROWN-OUT(NTC)}$	Triggered during startup (while $t_{STARTUP}$ is active) if the peak of the V pin is lower than V_{BR-NTC}. See Note A		1000		ms
Start-Up Timer for Using Lower Brown-Out Threshold (V_{BR-NTC})	$t_{START-UP}$	The timer is triggered when switching starts. The timer aborts when a peak < V_{BR-NTC}. The timer restarts at zero when a peak > V_{BR-NTC}. When timer expires, the higher brown-out threshold V_{BR-} is applied. See Note A		1000		ms
VOLTAGE MONITOR Pin High-Line Threshold	$V_{V(HIGH+)}$	(170 VAC) See Note A		2.42		V
VOLTAGE MONITOR Pin High-Line Deassertion Threshold	$V_{V(HIGH-)}$	(140 VAC) See Note A		2.00		V

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)			Min	Typ	Max	Units
Current Limit / Circuit Protection								
Over-Current Protection Limit[1]	I_{OCP} T_J = 25 °C	**Full Power**						A
		di/dt = 293 mA/µs	PFS5x73F	V_V < 2 V	2.8	3.1	3.3	
				V_V > 2.42 V		2.1		
		di/dt = 437 mA/µs	PFS5x74F	V_V < 2 V	4.5	4.8	5.1	
				V_V > 2.42 V		3.3		
		di/dt = 494 mA/µs	PFS5x75F	V_V < 2 V	5.0	5.3	5.6	
				V_V > 2.42 V		3.6		
		di/dt = 627 mA/µs	PFS5x76F	V_V < 2 V	6.0	6.4	6.8	
				V_V > 2.42 V		4.3		
		di/dt = 703 mA/µs	PFS5x77F	V_V < 2 V	7.0	7.5	7.9	
				V_V > 2.42 V		5.0		
		di/dt = 836 mA/µs	PFS5x78F	V_V < 2 V	8.5	9.0	9.5	
				V_V > 2.42 V		6.1		
Over-Current Protection Limit[1]	I_{OCP} T_J = 25 °C	**90% Full Power**						A
		di/dt = 263 mA/µs	PFS5x73F	V_V < 2 V	2.6	2.8	3.1	
				V_V > 2.42 V		1.9		
		di/dt = 393 mA/µs	PFS5x74F	V_V < 2 V	4.1	4.4	4.8	
				V_V > 2.42 V		3.0		
		di/dt = 445 mA/µs	PFS5x75F	V_V < 2 V	4.5	4.9	5.3	
				V_V > 2.42 V		3.3		
		di/dt = 564 mA/µs	PFS5x76F	V_V < 2 V	5.4	5.9	6.4	
				V_V > 2.42 V		4.0		
		di/dt = 633 mA/µs	PFS5x77F	V_V < 2 V	6.3	6.9	7.4	
				V_V > 2.42 V		4.6		
		di/dt = 752 mA/µs	PFS5x78F	V_V < 2 V	7.6	8.3	8.9	
				V_V > 2.42 V		5.6		

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)			Min	Typ	Max	Units
Current Limit / Circuit Protection (cont.)								
Over-Current Protection Limit[1]	I_{OCP} T_J = 25 °C	**80% Full Power**						A
		di/dt = 234 mA/µs	PFS5x73F	V_V < 2 V	2.4	2.6	2.8	
				V_V > 2.42 V		1.7		
		di/dt = 350 mA/µs	PFS5x74F	V_V < 2 V	3.7	4.1	4.4	
				V_V > 2.42 V		2.7		
		di/dt = 395 mA/µs	PFS5x75F	V_V < 2 V	4.1	4.5	4.8	
				V_V > 2.42 V		3.0		
		di/dt = 500 mA/µs	PFS5x76F	V_V < 2 V	4.9	5.4	5.8	
				V_V > 2.42 V		3.6		
		di/dt = 562 mA/µs	PFS5x77F	V_V < 2 V	5.8	6.3	6.7	
				VV > 2.42 V		4.2		
		di/dt = 669 mA/µs	PFS5x78F	V_V < 2 V	7.0	7.6	8.1	
				V_V > 2.42 V		5.1		
Over-Current Protection Limit[1]	I_{OCP} T_J = 25 °C	**70% Full Power**						A
		di/dt = 205 mA/µs	PFS5x73F	V_V < 2 V	2.2	2.3	2.5	
				V_V > 2.42 V		1.6		
		di/dt = 306 mA/µs	PFS5x74F	V_V < 2 V	3.4	3.7	4.0	
				V_V > 2.42 V		2.5		
		di/dt = 346 mA/µs	PFS5x75F	V_V < 2 V	3.7	4.0	4.3	
				V_V > 2.42 V		2.7		
		di/dt = 439 mA/µs	PFS5x76F	V_V < 2 V	4.6	4.9	5.3	
				V_V > 2.42 V		3.3		
		di/dt = 492 mA/µs	PFS5x77F	V_V < 2 V	5.4	5.8	6.2	
				V_V > 2.42 V		3.9		
		di/dt = 585 mA/µs	PFS5x78F	V_V < 2 V	6.3	6.8	7.3	
				V_V > 2.42 V		4.6		
SOA Protection Fixed Off-Time	$t_{OFF(SOA)}$	T_J = 25 °C See Note A			200	250	300	µs
SOA Protection Fixed On-Time	$t_{ON(SOA)}$	T_J = 25 °C See Note A				700		ns
Leading Edge Blanking (LEB) Time Period	t_{LEB}	T_J = 25 °C See Note A				550		ns
Minimum On-Time in I_{OCP}	$t_{ON\_OCP(MIN)}$	T_J = 25 °C See Note A			600	800		ns

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)	Min	Typ	Max	Units
VCC Parameters PFS527xF Parts (Parts without high voltage start-up power supply circuit)						
VCC Operating Range	VCC	0 °C < T_J < 100 °C	7.0	12.0	35.0	V
VCC Start-Up Threshold	VCC_{UV+}	0 °C < T_J < 100 °C		8.7	8.9	V
VCC Shutdown Threshold	VCC_{UV-}	0 °C < T_J < 100 °C	6.08	6.2		V
VCC UVLO Hysteresis	VCC_{HYST}	0 °C < T_J < 100 °C		2.5		V
Series Regulator PFS527XF Parts						
REFERENCE Pin Voltage VDR Pin Voltage	V_{REF} V_{VDR}	VCC > 6.3 V 0°C < T_J < 100 °C No external load applied on REF and VDR		5.25		V
VDR Pin Start-Up Threshold	$V_{VDR(UV+)}$	0 °C < T_J < 100 °C			5.0	V
VDR UVLO Hysteresis	$V_{VDR(UV)(HYST)}$	See Note A	50			mV
VCC Parameters PFS517xF Parts (Parts with high voltage start-up power supply circuit)						
VCC Operating Range	VCC	0 °C < T_J < 100 °C	7.0	12.0	35.0	V
VCC Takes Over VDR and Reference Supply From High-Voltage Regulator From the D Pin	VCC_{TO+}	VD > 20 V, VCC rising from 0 V T_J = 25 °C		6.3		V
Series Regulator PFS517xF Parts						
REFERENCE Pin Voltage VDR Pin Voltage (VDR and REFERENCE pin Supplied From VCC Pin	$V_{REF(VCC)}$ $V_{VDR(VCC)}$	VCC > 6.3 V, VD = 0 V to 400 V 0 °C < T_J < 100 °C		5.25		V
REFERENCE Pin Voltage VDR Pin Voltage (VDR and REFERENCE Pin Supplied Through High-Voltage Regulator from the D pin)	$V_{REF(VD)}$ $V_{VDR(VD)}$	VCC = 0 V, VD > 20 V 0 °C < T_J < 100 °C		5.15		V
VDR and REFERENCE Pin Start-Up Threshold	$V_{VDR(UV+)}$ $V_{REF(UV+)}$	0 °C < T_J < 100°C See Note A			5.0	V
Reference VDR UVLO Hysteresis	$V_{VDR(VH)(HYST)}$	See Note A	50			mV
Time From V_{REF} > V_{REFUV+} Until Device Commences Switching	t_{RESET}	Assumes V pin is above brown-in threshold. See Note A		1.6	3	ms
Valley Sensing						
Valley Sensing Positive Threshold	V_{VS1}	Voltage on the VS pin rising T_J = 25 °C		0.88		V
Valley Sensing Negative Threshold	V_{VS2}	Voltage on the VS pin falling T_J = 25 °C		0.48		V

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)	Min	Typ	Max	Units
Power Good PFS517x Parts						
Power Good Threshold Set Reference Current (Power Good Deassertion Threshold Output Reference Current)	$I_{PG(T)}$	0 °C < T_J < 100 °C; V_{PGT} = 3.0 V		-10		µA
Power Good Delay Time (From FB > V_{PG+} to PG < 1 V)	t_{PG}	0 °C < T_J < 100 °C; PG = 20 kΩ pull-up to 12 V from FB > V_{PG+} to PG < 1 V See Note A		<15		µs
Power Good State Change Deglitch Time	$t_{PG(D)}$	T_J = 25 °C; Applies to rising and falling transitions on the power good comparator and detection of an open PGT pin. See Note A		81		µs
Power Good Internal Reference Threshold (Start-up Threshold) (Power Good Internal Assertion Threshold)	V_{PG+}	0 °C < T_J < 100 °C	3.55	3.65	3.75	V
Power Good Relative Threshold	$V_{PG+REL(FB)}$	0 °C < T_J < 100 °C		V_{FBREF} -0.2		V
Power Good Deassertion Threshold	$V_{PG(VOL)}$	V (PGT) = 3 V 0 °C < T_J < 100 °C		V (PGT) ±30 mV		V
Power Good Pin Leakage Current in Off-State	$I_{PG(OFF)}$	FB < $V_{PG(-)}$ 0 °C < T_J < 100 °C			100	nA
Power Good On-State Voltage	V_{PG-}	0 °C < T_J < 100 °C I_{PG} = 1.0 mA; FB = 3.85 V			2	V
Thermal Protection (OTP)						
Controller Junction Temperature for Shutdown	T_{OTP+}	Soft-shutdown is triggered when the silicon exceeds this temperature See Note A		130		°C
Controller Junction Temperature for Restart	T_{OTP-}	Restart occurs if OTP hysteresis is enabled when the silicon drops below this temperature See Note A		81		°C
Over-Temperature Hysteresis	$T_{OTP(HYST)}$	V > V_{BR+} See Note A		49		°C

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +125 °C (See Note C)		Min	Typ	Max	Units
PowiGaN Cascode							
On-State Resistance	$R_{DS(ON)}$ I_D = 0.5 X I_{OCP}	PFS5x73F	$T_{J(M)}$ = 25 °C		0.52	0.68	Ω
			$T_{J(M)}$ = 100 °C		0.78	1.02	
		PFS5x74F	$T_{J(M)}$ = 25 °C		0.35	0.44	
			$T_{J(M)}$ = 100 °C		0.49	0.62	
		PFS5x75F	$T_{J(M)}$ = 25 °C		0.29	0.39	
			$T_{J(M)}$ = 100 °C		0.41	0.54	
		PFS5x76F	$T_{J(M)}$ = 25 °C		0.18	0.28	
			$T_{J(M)}$ = 100 °C		0.27	0.37	
		PFS5x77F	$T_{J(M)}$ = 25 °C		0.145	0.21	
			$T_{J(M)}$ = 100 °C		0.23	0.29	
		PFS5x78F	$T_{J(M)}$ = 25 °C		0.11	0.16	
			$T_{J(M)}$ = 100 °C		0.18	0.22	
Charge Effective Output Capacitance	$C_{OSS(CH)}$	T_J = 25 °C V_{GS} = 0 V, V_{DS} = 0 to 400 V See Note A	PFS5x73F		26.1		pF
			PFS5x74F		39.5		
			PFS5x75F		51.3		
			PFS5x76F		67.1		
			PFS5x77F		89.5		
			PFS5x78F		123		
Energy Effective Output Capacitance	$C_{OSS(EN)}$	T_J = 25 °C V_{GS} = 0 V, V_{DS} = 0 to 400 V See Note A	PFS5x73F		18.1		pF
			PFS5x74F		26.4		
			PFS5x75F		35.6		
			PFS5x76F		46.4		
			PFS5x77F		62.4		
			PFS5x78F		92.5		
Off-State Drain Current Leakage	I_{DSS}	T_J = 1 00 °C V_{DS} = 80% V_{CC} = 12 V V_{FB} = V_V = V_C = 0	PFS517xF PFS527xF			100	µA

Parameter	Symbol	Conditions SOURCE = 0 V, V_{CC} = 12 V, T_J = -40 to +105 °C (See Note C)	Min	Typ	Max	Units
X Capacitor Discharge XD1/XD2 Function						
Supply Current	I_{SUPPLY}	T_J = 25 °C			21.7	µA
Saturation Current [A, D]	I_{DSAT}		2.5			mA
AC Removal Detection Time	t_{DET}	Line Cycle Frequency 47-63 Hz		22	31.4	ms

NOTES:
A. Not tested parameter. Guaranteed by design.
B. Tested in typical boost PFC application circuit.
C. Normally limited by internal circuitry.
D. Saturation current specifications ensure a natural RC discharge characteristic at all voltages up to 265 VAC peak with the external resistor values specified in component selection table.

Typical Performance Characteristics

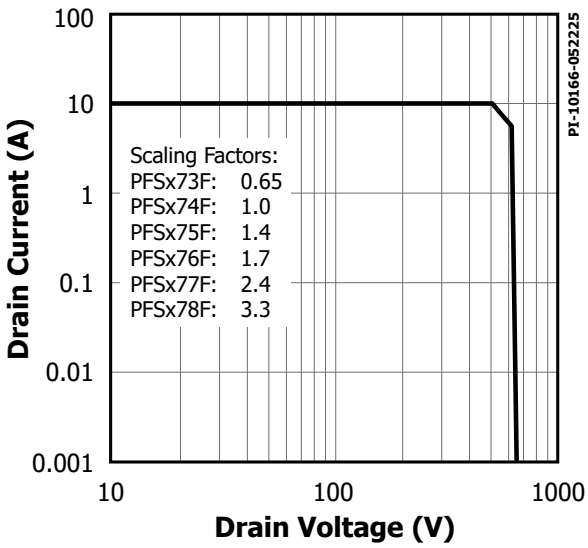
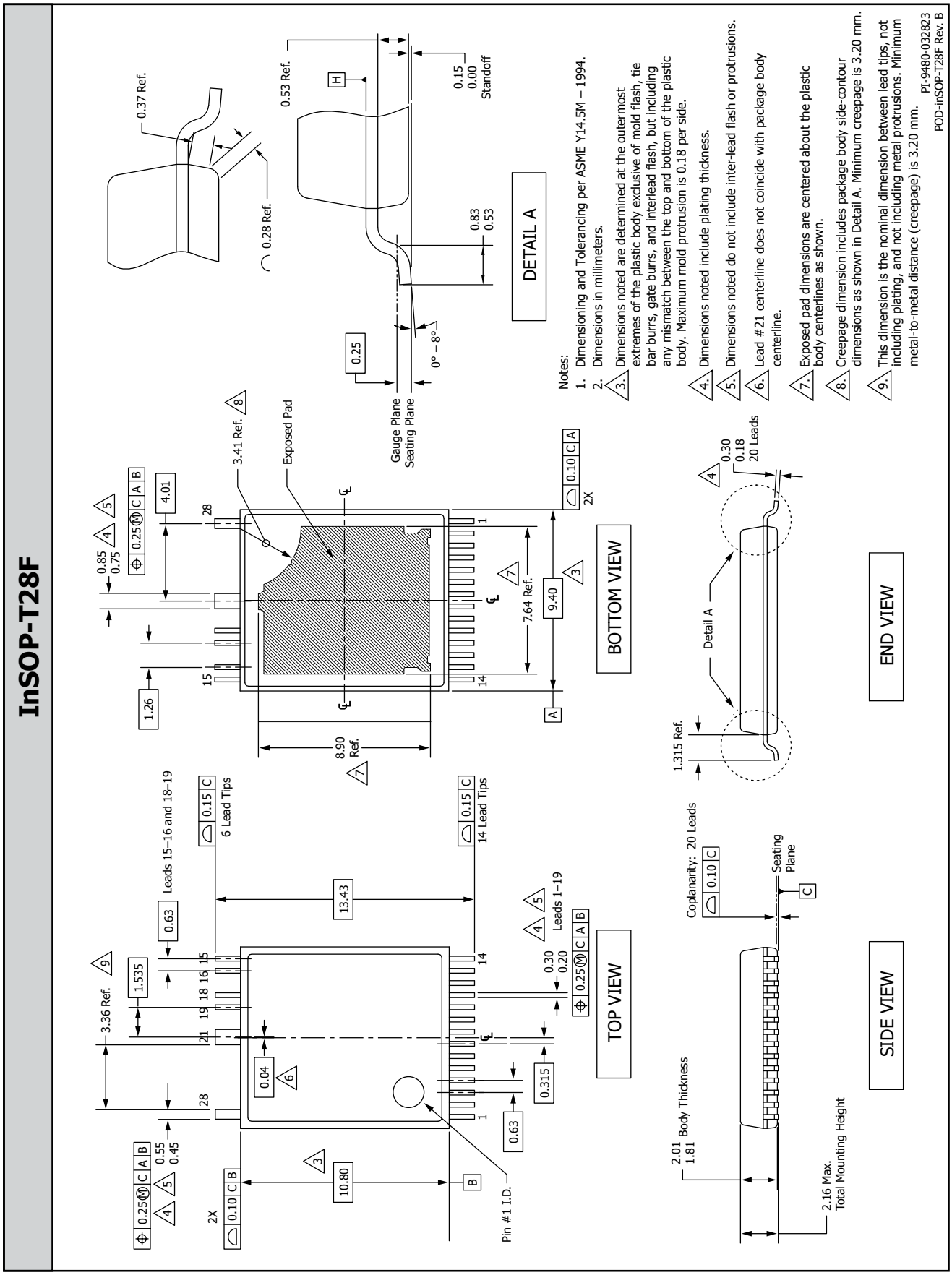


Figure 19. Output Characteristics.

InSOP-T28F



P1-9480-032823
POD-inSOP-T28F Rev. B
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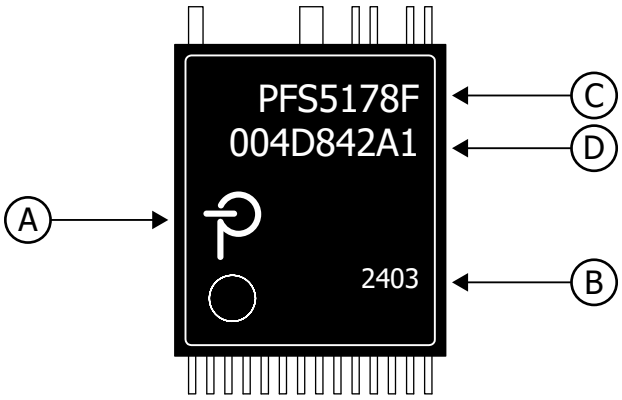
PACKAGE MARKING

InSOP-T28F



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW))
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-9436c-052225

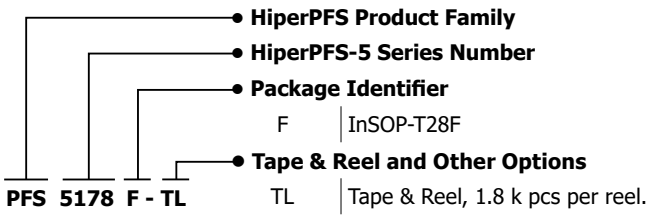
Part Ordering Table

Part Number	Option	Quantity
PFS5173F-TL	Reel	1800
PFS5x74F-TL	Reel	1800
PFS5x75F-TL	Reel	1800
PFS5x76F-TL	Reel	1800
PFS5x77F-TL	Reel	1800
PFS5x78F-TL	Reel	1800

MSL Table

Part Number	MSL Rating
PFS5173F-TL	3
PFS5x74F-TL	3
PFS5x75F-TL	3
PFS5x76F-TL	3
PFS5x77F-TL	3
PFS5x78F-TL	3

Part Ordering Information



Revision	Notes	Date
E	Production release.	07/23
F	Updated Over-Current Protection Limit (I_{OCP}) per PCN-24121.	03/24
G	Added Application section and Output Characteristics.	06/25

For the latest updates, visit our website: www.power.com

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