Title	***Engineering Prototype Report for EP-32 – TOPSwitch®-GX 25 W Multiple Output DVD, Set-top Box Power Supply Using TOP245P***
Specification	85 VAC to 265 VAC Input, 3.3 V, 5 V, 12 V, -24 V, 20 W continuous / 25 W peak output
Application	DVD player, Set-top box and other multiple output applications
Author	Power Integrations Applications Department
Document Number	EPR-32
Date	13-Jul-06
Revision	1.1

Summary and Features

- Low parts count, low cost design
- Excellent cross-regulation without linear post-regulators
- Simple input EMI filter
- Meets EN55022 B / CISPR22 B EMI with >20 dB margin
- Low no-load input power (<65 mW at 115 VAC, <90 mW at 230 VAC)
- High standby efficiency, <0.9 W input power with 0.5 W load
- High efficiency, >75%

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing the design of an AC-DC power supply with universal input and 4 outputs. The design, rated for 20 W (25 W peak), is implemented using a TOP245P device from the *TOPSwitch-GX* IC family and an EEL25 core in a flyback topology.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	100/115/230	265	VAC	2 Wire (No Protective Earth Ground)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				0.1	W	Measured at 265 VAC
Output						
Output Voltage 1	V_{OUT1}	3.20	3.30	3.45	V	±5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0.30	0.60	2.0	A	
Output Voltage 2	V_{OUT2}	4.75	5.00	5.25	V	±5%
Output Ripple Voltage 2	$V_{RIPPLE2}$			75	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}	0.30	1.20	2.5	A	
Output Voltage 3	V_{OUT3}	11.16	12.00	12.84	V	±7%
Output Ripple Voltage 3	$V_{RIPPLE3}$			100	mV	20 MHz Bandwidth
Output Current 3	I_{OUT3}	100	200	500	mA	
Output Voltage 4	V_{OUT4}	-21.62	-24.00	-26.9	V	-10% / +12%
Output Ripple Voltage 4	$V_{RIPPLE4}$			100	mV	20 MHz Bandwidth
Output Current 4	I_{OUT4}	30	50	50	mA	
Total Output Power						
Continuous	P_{OUT}	4.4	20		W	
Peak	P_{OUT_PEAK}			25	W	
Efficiency	η		75		%	Measured at P_{OUT} (26 W), 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950/UL1950 Class II				
Surge		2	3		kV	1.2 / 50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

Table 1 – Power Supply Specification.

3 Schematic

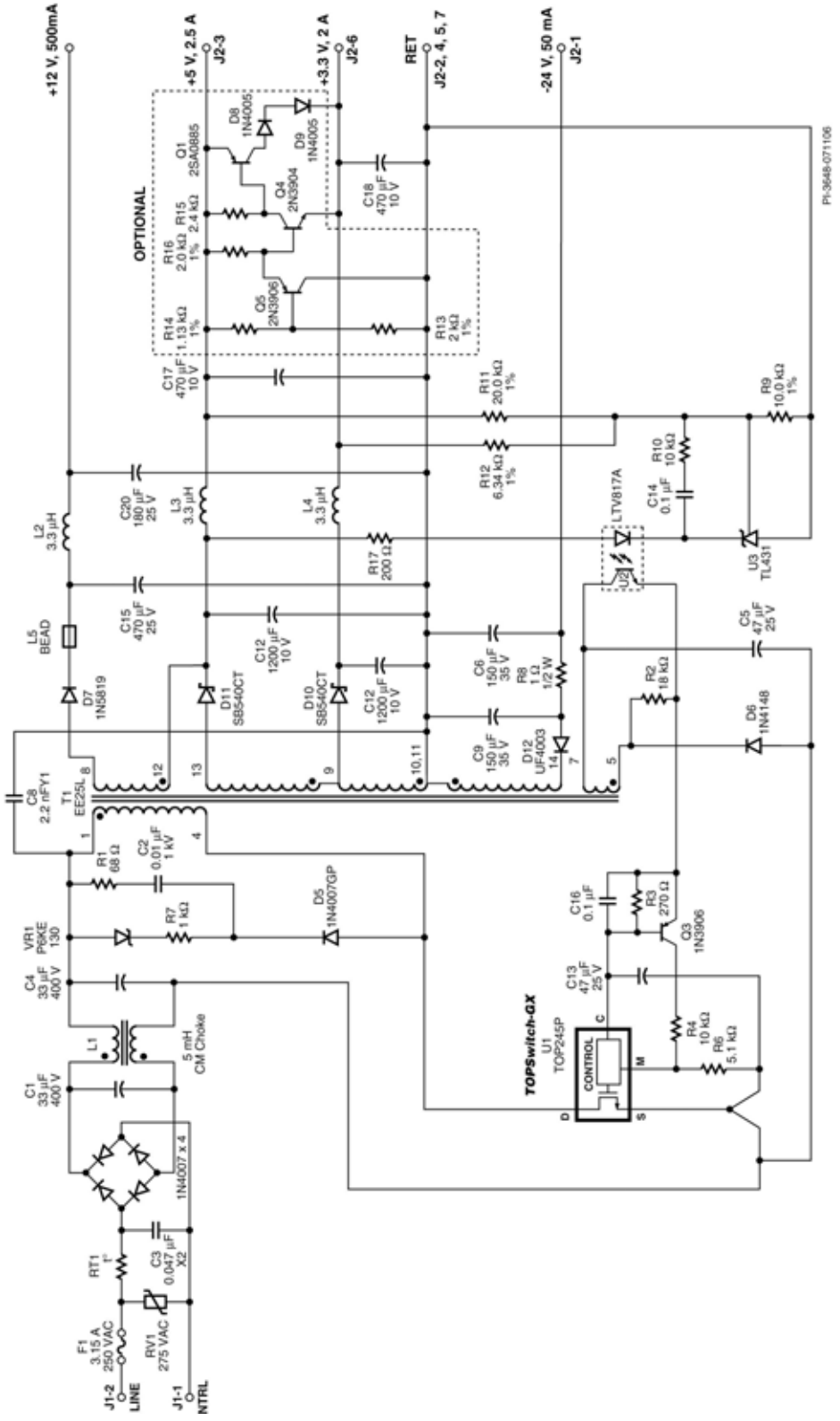

Figure 2 – Schematic.

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4 Circuit Description

This design features the TOP245P device from the *TOPSwitch-GX* IC family. By using the PC board to provide heatsinking, the need for an external heatsink is eliminated, removing the cost of the heatsink and associated assembly costs.

To provide <0.1 W no-load consumption, current mode control with variable frequency operation is implemented using the X pin feature of the *TOPSwitch-GX*. In designs where 0.5 W no-load is acceptable, the X pin control components can be removed, relying on the standard voltage mode control via the CONTROL pin. More details of this operation is provided below.

An optional secondary side discrete shunt regulator provides a low cost and efficient (no heatsink required) method of meeting the tight regulation requirements of maximum load on either the 5 V or 3.3 V outputs while the other is at minimum load. In designs where the minimum and maximum loads on the 3.3 V and 5 V output occur at the same time, this circuit can easily be removed.

4.1 Input EMI Filtering

Conducted EMI filtering is provided by C3, C1, L1, and C4. The switching frequency jitter feature of the *TOPSwitch-GX* family allows the use of a small, low cost common mode choke for L1 and reduces the value of C3 needed to meet EN55022 / CISPR22 Class B with good margin. A safety rated Y capacitor bridges the isolation barrier from the rectified DC rail to output return. This returns common mode EMI currents generated by the primary and secondary switching waveforms, reducing conducted EMI. EMI results are presented in a later section of this document. Returning the Y capacitor to the DC rail ensures high currents present during line transients are routed away from U1.

4.2 TOPSwitch-GX Primary

The universal AC input (85 VAC to 265 VAC) is rectified and filtered by D1-D4, C1 and C2. To limit inrush current and prevent damage to D1-D4, a thermistor RT1 is used. In addition, an MOV (or VDR), RV1, provides differential surge protection.

The rectified DC rail is applied to one end of the transformer primary, the other end being connected to the DRAIN pin of the integrated MOSFET of U1.

To keep the peak DRAIN voltage acceptably below the BV_{DSS} (700 V) of U1, diode D5, R7, VR1, C2, and R1 form a primary clamp. This network clamps the voltage spike seen on the DRAIN due to primary and secondary reflected leakage inductance. Capacitor C2 together with R1 form the main clamp with VR1 providing a hard limit for the maximum voltage seen across the primary. Resistor R7 ensures that VR1 only conducts at the end of the leakage inductance spike event, limiting dissipation. Diode D5 is deliberately selected as a slow recovery type, but must be a glass-passivated type to guarantee the reverse recovery time as defined by the manufacturer. Standard 1N4007 diodes should not be used as their potential for very long reverse recovery times can cause excessive

drain ringing. The slow recovery time, compared to fast or ultra-fast diodes, allows recovery of some of the clamp energy, improving efficiency.

4.3 Output Rectification

The secondary of the transformer is rectified and filtered by D7, C15, D11, C11, D10, C12, D12, and C9. For better voltage centering and regulation, the 12 V output is DC stacked on top of the 5 V output; the start of the 12 V winding is connected to the cathode of D11. A small ferrite bead, L5, was used to center the output and improve cross-regulation by reducing the effect of secondary leakage inductance.

Post-filters (L2, C20, L3, C17, L4, C16, R8, and C6) remove switching noise and further reduce switching ripple.

4.4 Output Feedback and Control

DC feedback to the output voltage regulator error amp (U3) comes from a combination of the 3.3 V output, via R12, and 5 V output, via R11. Together with resistor R9, these form a resistor divider, the center point that is tied to the 2.5 V REF pin of U3. Capacitor C14 and R10 roll off the high frequency gain of U3 while R17 sets the overall DC gain.

In a *TOPSwitch-GX* design, regulation of the output is normally provided by voltage mode PWM control. The current into the CONTROL pin sets the duty cycle of the internal MOSFET. The duty cycle control operates over a CONTROL pin current of 2 mA to 6 mA. Current below this level is used to supply power to the IC.

In this design control is accomplished by employing the externally programmable current limit function of the *TOPSwitch-GX* family, in this case via the M pin. This implements current mode control rather than using voltage mode PWM control via the CONTROL pin.

The first ~2 mA of feedback current is fed into the CONTROL pin. This provides the supply current for operation, but leaves the duty cycle at the internal device maximum.

Feedback current above ~2 mA forward biases Q3 and pulls up R6 via R4. The characteristic of the M pin is such that increasing sink current (current out of the pin) increases the primary current limit. Therefore, as the feedback current increases, the sink current decreases and the primary current limit reduces, thereby allowing the output voltage feedback loop to control the primary peak current. Resistor R6 sets the peak current limit (startup and overload) and R4 ensures that the maximum source current (current into the M pin) stays below 44 μA to prevent the device from operating in the line sensing mode of the M pin. As any current above 2 mA engages the M pin control, the current into the CONTROL pin is limited to this level and therefore, the PWM function of the CONTROL pin does not determine the duty cycle.

As the load is reduced, the primary current limit reduces until the remote ON/OFF (inhibit) threshold is reached at an M pin sink current of approximately 27 μA. The supply then operates with a fixed 25% current limit, but at a reduced and variable switching frequency,

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to maintain regulation as the load is further reduced. This greatly reduces switching losses, maintaining high standby efficiency and low no-load power consumption.

Current mode control above 50% duty cycle requires slope compensation and this is provided by a ramp signal generated from the bias winding via R2 and C16. Capacitor C16 also serves as a high frequency roll-off filter. The gain/phase results presented (Section 12) show excellent margin under all operating conditions.

4.5 Secondary 3.3 V and 5 V Shunt Regulator

To meet the cross-regulation requirement of the 3.3 V output at maximum load while the 5 V output is at minimum load or vice versa, a low cost secondary side shunt regulator was added between the 3.3 V and 5 V outputs. This is formed by R14, R13, Q5, R16, R15, Q4, Q1, D8, and D9. This provides current from the 5 V output into the 3.3 V output when the voltage difference between the two outputs becomes unacceptable. This threshold is set by R14, R15 and Q5, which in turn drive Q4 and Q1, providing current to the 3.3 V output via D8 and D9.

Unlike a linear regulator, this circuit dissipates very little power and the addition of D8 and D9 reduces the dissipation in Q1 such that no heatsink is required at all. The circuit configuration provides enough temperature compensation to meet the 0 °C to 50 °C ambient temperature specification.

In applications where the 3.3 V and 5 V loads track (the minimum and maximum loads on both outputs occur at the same time) then this circuit may be removed. Note that this circuit is not needed to meet no-load regulation.

5 PCB Layout

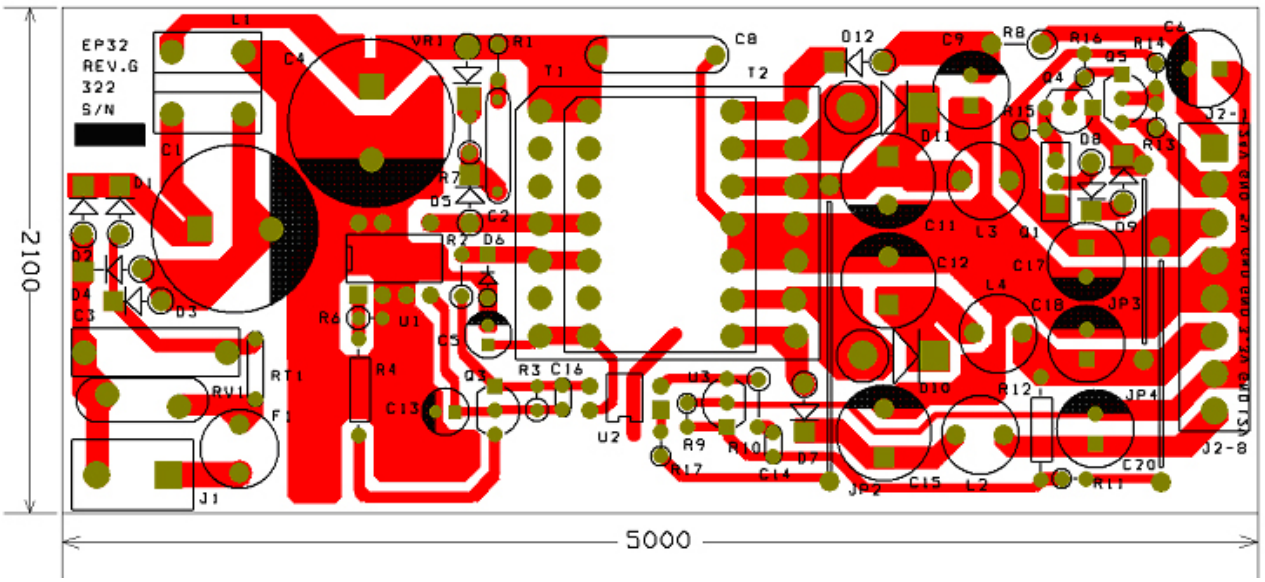

Figure 3 – Printed Circuit Layout (0.001 inches).

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6 Bill Of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	2	C1, C4	33 μF, 400 V 18 mm x 20 mm	EEU-EB2G330S	Panasonic
2	1	C3	0.047 μF, 250 VAC, X class	ECQ-U2A473MV	Any
3	1	C2	0.01 μF, 1 kV ceramic disc	5HKS10	Vishay / Cera-mite
4	2	C6, C9	150 μF, 35 V, low ESR 8 mm x 11.5 mm, 117 mΩ	EEU-FC1V151	Panasonic
5	1	C8	2.2 nF, Y1 Class	ECK-DNA222ME	Pansonic
6	2	C11, C12	1200 μF, 10 V 10 mm x 20 mm, 23 mΩ	KZE10VB122M10X20LL	United Chemi-con
7	2	C5, C13	47 μF, 25 V, general purpose 5 mm x 11 mm	ECA-1EHG470	Panasonic
8	2	C14, C16	0.1 μF, 50 V, ceramic	ECU-S1H104MEA	Panasonic
9	1	C15	470 μF, 25 V, low ESR 10 mm x 16 mm, 68 mΩ	EEU-FC1E471	Panasonic
10	2	C17, C18	470 μF, 10 V, low ESR 8 mm x 11.5 mm, 117 mΩ	EEU-FC1A471	Panasonic
11	1	C20	180 μF, 25 V, low ESR 8 mm x 11.5 mm, 117 mΩ	EEU-FC1E181	Panasonic
12	6	D1, D2, D3, D4, D8, D9	1 A, 600 V, rectifier	1N4005	Any
13	1	D5	1 A, 1000 V, trr = 2 μs glass passivated rectifier	1N4007GP	General Semiconductor (Vishay)
14	1	D6	1N4148, 75 V, signal	1N4148	Any
15	1	D7	1 A, 40 V, Schottky	1N5819	Any
16	1	D12	1 A, 200 V, ultra-fast	UF4003	Any
17	2	D10, D11	5 A, 40 V, Schottky	SB540	General Semiconductor
18	1	F1	3.15 A, 250 VAC	3721315041	Wickmann
19	1	L1	5 mH, 0.3 A common mode choke	HT9V03050	CUI
20	3	L2, L3, L4	5.5 A, 3.3 μH inductor	622LY-3R3M	Toko
21	1	L5	Ferrite bead	2643001501	Fair-Rite
22	1	Q1	2SA0885, PNP	2SA0885	Panasonic
23	2	Q3, Q5	TO-92 Transistor / PNP	2N3906_D26Z	Fairchild
24	1	Q4	TO-92 Transistor / NPN	2N3904_D26Z	Fairchild
25	1	R1	68 Ω, 1/2 W, 5%	CFR-50JB-68R	Yageo
26	1	R2	18 kΩ, 1/4 W, 5%	CFR-25JB-18K	Yageo
27	1	R3	270 Ω, 1/4 W, 5%	CFR-25JB-270R	Yageo
28	1	R4	10 kΩ, 1/4 W, 5%	CFR-25JB-10K	Yageo
29	1	R6	5.1 kΩ, 1/4 W, 5%	CFR-25JB-5K1	Yageo
30	1	R7	1 kΩ, 1/4 W, 5%	CFR-25JB-1K0	Yageo
31	1	R8	1 Ω, 1/2 W, 5%	CFR-50JB-1R0	Yageo
32	1	R9	10 kΩ, 1/4 W, 1%	MFR-25FBF-10K0	Yageo
33	1	R10	3.3 kΩ, 1/4 W, 5%	CFR-25JB-3K3	Yageo
34	1	R11	20 kΩ, 1/4 W, 1%	MFR-25FBF-20K0	Yageo
35	1	R12	6.34 kΩ, 1/4 W, 1%	MFR-25FBF-6K34	Yageo

36	2	R13, R16	2 kΩ, 1/4 W, 1%	MFR-25FBF-2K00	Yageo
37	1	R14	1.13 kΩ, 1/4 W, 1%	MFR-25FBF-1K13	Yageo
38	1	R15	2.4 kΩ, 1/4 W, 5%	CFR-25JB-2K4	Yageo
39	1	R17	200 Ω, 1/4 W, 5%	CFR-25JB-200R	Yageo
40	1	VR1	Zener / TVS, 3 W, 130 V	P6KE130A	Any
41	1	RV1	Varistor 430 VDC, 110 J (2 ms)	ERZ-V14D431	Panasonic
42	1	RT1	Thermistor	CL-120	Thermometrics
43	1	TI	EEL25 Flyback Transformer	SIL6025 LSPA11218 5450122600	Hical Li Shin Vogt
44	1	U1	*TOPSwitch-GX*, P package	TOP245P	Power Integrations
45	1	U3	Reference	TL431ALCP	Fairchild
46	1	U2	Opto coupler 80-160% CTR	LTV817A	Lite-On
47	1	J1	Input connector	26-48-1031	Molex
48	1	J2	Output connector	26-48-1081	Molex

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7 Transformer Specification

7.1 Electrical Diagram

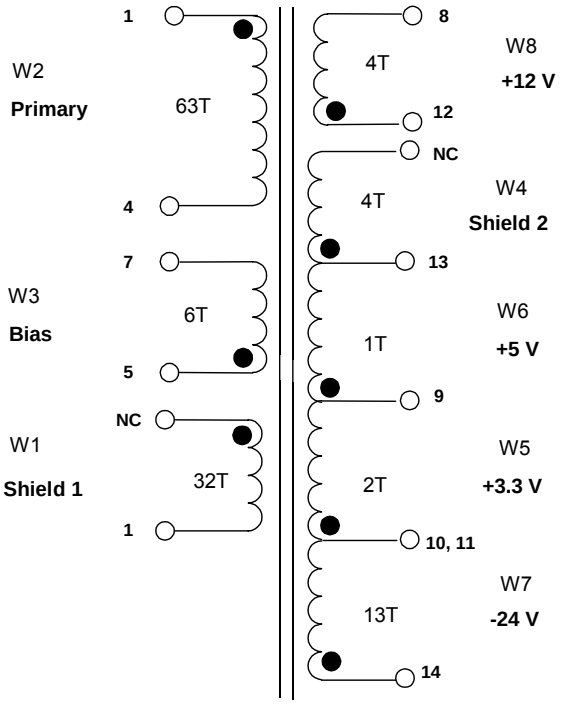

Figure 4 –Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1 through 7 to pins 8 through 14	3000 VAC
Primary Inductance	Pin 1 to pin 4, all other windings open, measured at 132 kHz, 1 V RMS excitation	800 μH, +/-10%
Resonant Frequency	Pin 1 to pin 4, all other windings open, 1 V RMS excitation	300 kHz (min.)
Primary Leakage Inductance	Pin 1 to pin 4, with pins 8 thru 14 shorted, measured at 132 kHz, 1 V RMS	80 μH (max.)

7.3 Materials

Item	Description
[1]	Core: EEL25, TDK gapped for AL of 202 nH/T^2
[2]	Bobbin: EEL25 14 pins
[3]	Magnet wire: # 32 AWG
[4]	Teflon tubing # 22
[5]	Copper foil 0.12 mm thick, 14 mm wide.
[6]	Tape: 3M 1298 polyester film, 16.1 mm wide
[7]	Tape: 3M 1298 polyester film, 22.1 mm wide
[8]	Tape: 3M # 44 polyester web, 3.0 mm wide
[9]	Varnish

7.4 Transformer Build Diagram

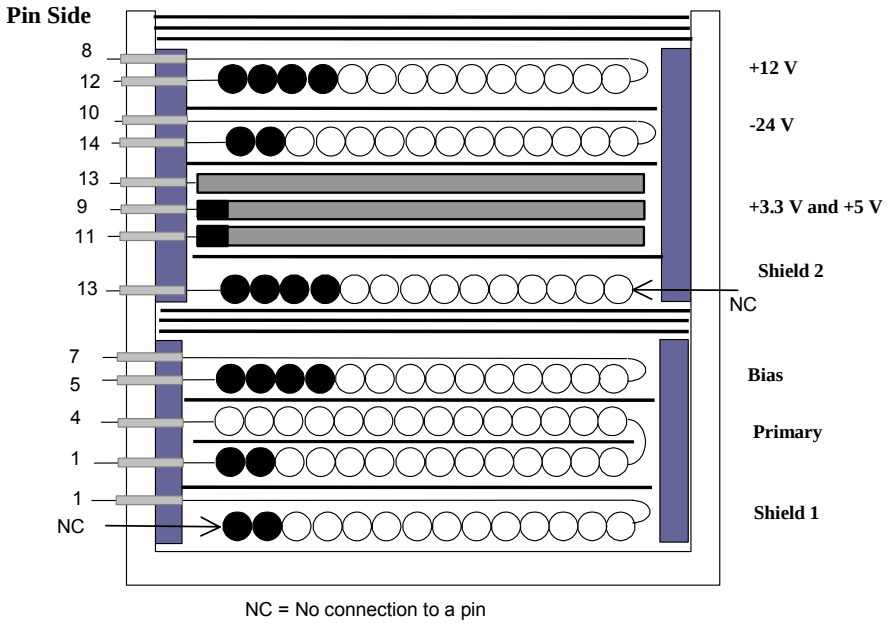

Figure 5 – Transformer Build Diagram.

The following figure shows the copper foils to be used for +3.3 V and +5 V outputs (W5 and W6)

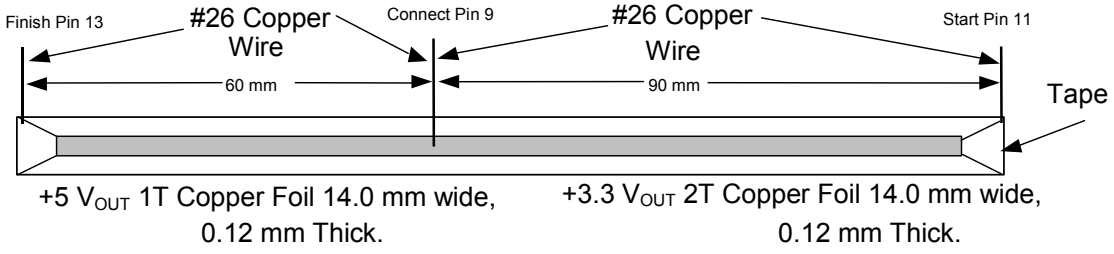

Figure 6 - Copper Foil Winding Information.

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7.5 Transformer Winding Construction

Margin Tape	Apply 3.0 mm margin at each side of bobbin using item [8]. Match combined height of primary, shield and bias windings.
W1 First Shield	Start with a floating lead. Wind 32 bifilar turns of item [3] from left to right. Wind tightly and uniformly across entire width of bobbin. Finish at pin 1 using item [4] at the finish leads. Cut the starting lead just at the start of the winding.
Basic Insulation	Apply one layer of tape item [6]
W2 Two Layers Primary	Start on pin 1 using item [4] at the start leads. Wind 32 bifilar turns of item [3] from left to right. Apply one layer of item [6]. Continue the same wire on second layer. Wind 31 turns from right to left. The two layers should be wound tightly with the turns uniformly distributed across entire width of bobbin. Finish on pin 4 using item [4] at the finish leads.
Basic Insulation	Apply one layer of tape item [6]
W3 Bias	Start on pin 5 using item [4] at the start leads. Wind 6 turns of 4 parallel wires of item [3]. Wind from left to right in a single layer. The wires should be tightly and uniformly wound. Finish on pin 7 using item [4] at the finish leads.
Insulation	3 Layers of tape [7] for insulation.
Margin Tape	Apply 3.0 mm margin at each side of bobbin using item [8]. Match combined height of secondary windings.
W4 Second shield.	Start on pin 13 using item [4] at the start leads. Wind 4 turns of 4 parallel wires of item [3]. Wind from right to left in a single tightly wound layer. Cut the ending lead to finish the winding.
Insulation	Apply one layer of tape item [6]
W5 and W6 +3.3 V and +5 V outputs.	Prepare copper foil item [5] and item [7] as shown in Figure 1. Start at pin 11 using item [4] at the start leads. Wind 2 turns. Connect the second lead to pin 9 using item [4] at the finish leads and wind 1 turn. Connect the end lead to pin 13 using item [4] at the finish leads.
Basic Insulation	Apply one layer of tape item [6]
W7 -24 V output.	Start at pin 14 using item [4] at the start leads. Wind 13 turns of 2 parallel wires of item [3]. Wind from right to left in a uniform and tightly wound layer. Finish on pin 10 using item [4] at the finish leads.
Basic Insulation	Apply one layer of tape item [6]
W8 +12 V output	Start on pin 12 using item [4] at the start leads. Wind 4 turns of 4 parallel wires of item [3]. Wind from right to left in a single tightly wound layer. Finish on pin 8 using item [4] at the finish leads.
Outer Insulation	3 layers of tape [7] for insulation.
Core Assembly	Assemble and secure core halves. Item [1]
Final Assembly	Dip varnish uniformly in item [9]. **Do not vacuum impregnate**.

7.6 Bobbin Drawing

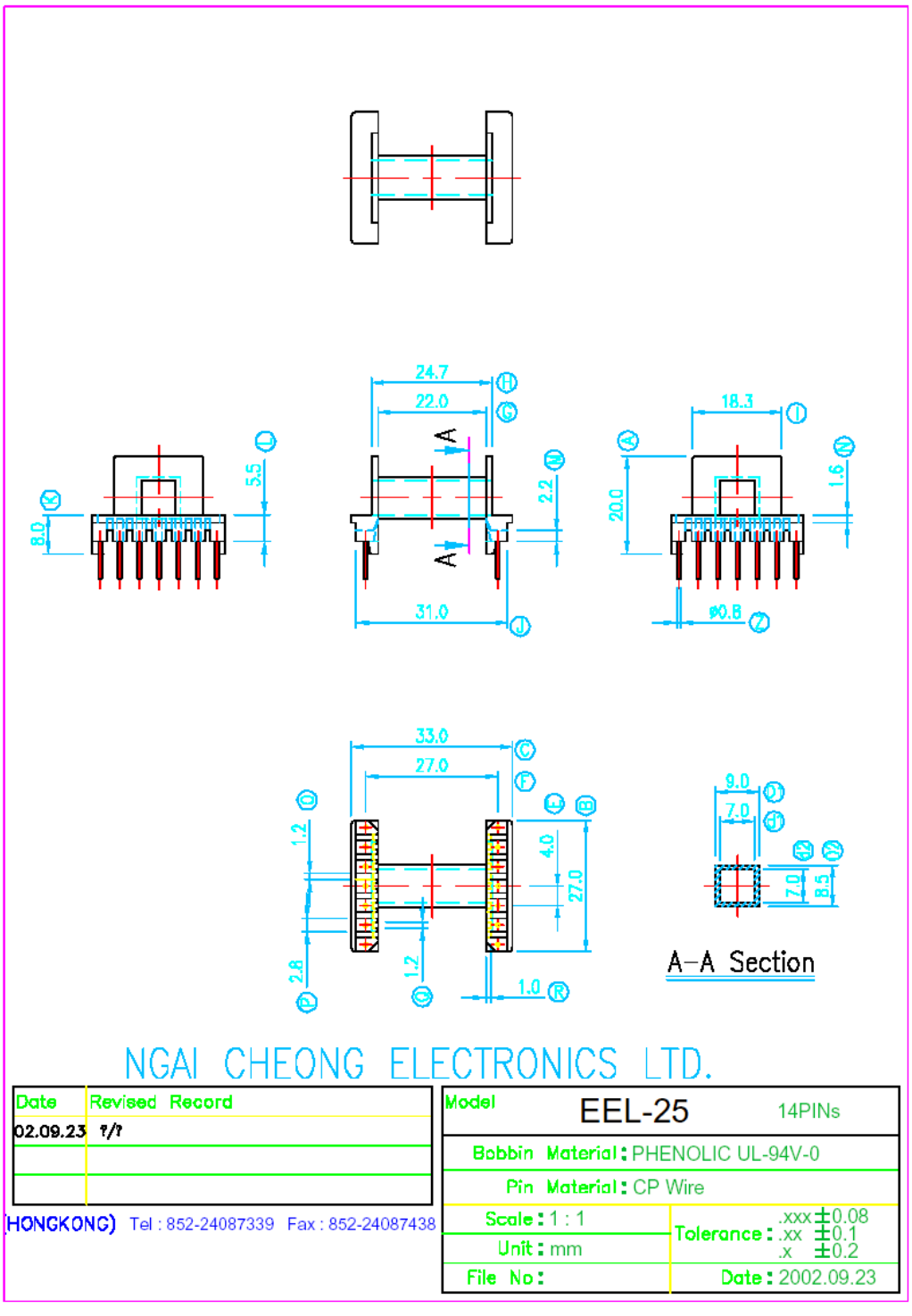

Figure 7 – EP-32 Transformer Bobbin Drawing.

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8 Transformer Spreadsheet

ACDC_TOPGX_Rev1.4_072403 Copyright Power Integrations Inc. 2003	INPUT	INFO	OUTPUT	UNIT	TOP_GX_072403.xls: TOPSwitch-GX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					**Customer**
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5			Volts	Output Voltage
PO	25	*Warning*		Watts	!!! For UNIVERSAL INPUT : REDUCE PO Cont.<22W (larger TOPSwitch-FX/GX,reduce input voltage range)
n	0.75				Efficiency Estimate
Z	0.5				Loss Allocation Factor
VB	15			Volts	Bias Voltage
tC	3			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	66			uFarads	Input Filter Capacitor
ENTER TOPSWITCH-GX VARIABLES					
TOP-GX	**TOP245P**			*Universal*	*115 Doubled/230V*
Chosen Device		*TOP245P*	*Power Out*	*22W*	*30W*
KI	1				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN			*1.023*	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX			*1.177*	Amps	Use 1% resistor in setting external ILIMIT
Frequency - (F)=132kHz, (H)=66kHz	f				Full (F) frequency option - 132kHz
fS	132000		*1.32E+05*	Hertz	TOPSwitch-GX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			*1.24E+05*	Hertz	TOPSwitch-GX Minimum Switching Frequency
fSmax			*1.40E+05*	Hertz	TOPSwitch-GX Maximum Switching Frequency
VOR	120			Volts	Reflected Output Voltage
VDS	10			Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.7			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KP	**0.54**				Ripple to Peak Current Ratio (0.4 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EEL25**				
Core		*EEL25*		*P/N:*	PC40EE25.4/32/6.4-Z
Bobbin		*EEL25_BOBBIN*		*P/N:*	*
AE			0.404	cm^2	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length
AL			1420	nH/T^2	Ungapped Core Effective Inductance
BW			22.3	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	**2**				Number of Primary Layers
NS	**3**				Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			86	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.61		Maximum Duty Cycle
IAVG			0.39	Amps	Average Primary Current
IP			0.87	Amps	Peak Primary Current
IR			0.46	Amps	Primary Ripple Current
IRMS			0.51	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			800	uHenries	Primary Inductance
NP			63		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			201	nH/T^2	Gapped Core Effective Inductance
BM			**2714**	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			**3690**	Gauss	Peak Flux Density (BP<4200)
BAC			728	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG			**0.22**	mm	Gap Length (Lg > 0.1 mm)
BWE			44.6	mm	Effective Bobbin Width
OD			0.71	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.63	mm	Bare conductor diameter
AWG			23	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			512	Cmils	Bare conductor effective area in circular mils
CMA		Warning	**1010**	Cmils/Amp	!!!! DECREASE CMA> (decrease L(primary layers),increase NS,smaller Core)

TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE		
Lumped parameters		
ISP	18.22 Amps	Peak Secondary Current
ISRMS	8.48 Amps	Secondary RMS Current
IO	5.00 Amps	Power Supply Output Current
IRIPPLE	6.86 Amps	Output Capacitor RMS Ripple Current
CMS	1697 Cmils	Secondary Bare Conductor minimum circular mils
AWGS	17 AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS	1.15 mm	Secondary Minimum Bare Conductor Diameter
ODS	7.43 mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS	3.14 mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS		
VDRAIN	647 Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS	23 Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB	64 Volts	Bias Rectifier Maximum Peak Inverse Voltage

The warning shown for PO is accepted as the 25 W specified power is a peak requirement (thermally limited). The warning shown for CMA (primary wire current density) is also accepted as it indicates the primary wire current density is low, and a smaller wire gauge could be used. The final design used bifilar 32 AWG wire.

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency

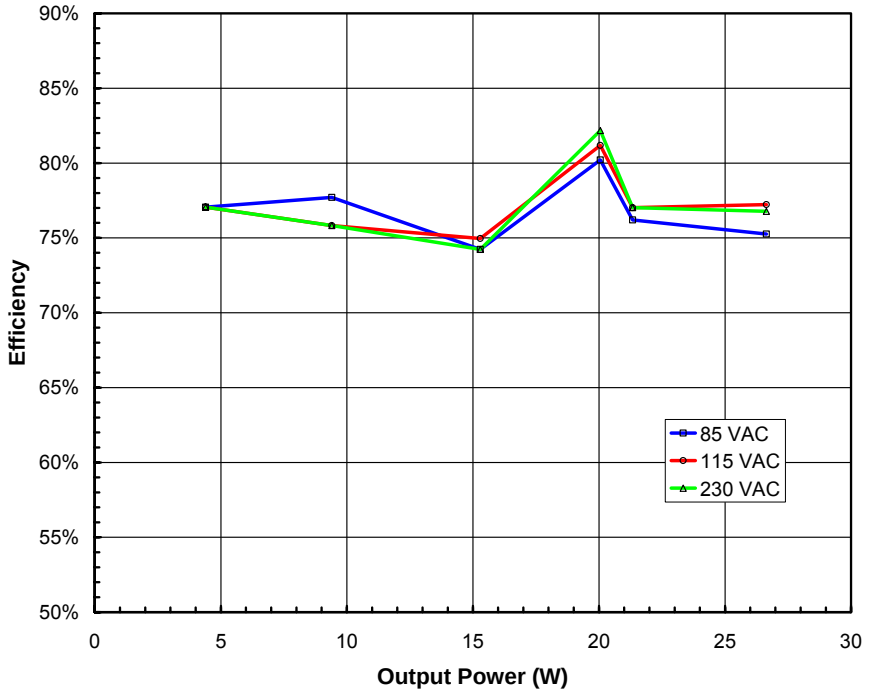

Figure 8 – Output Power vs. Efficiency, Room Temperature, 60 Hz.

9.2 No-load Input Power

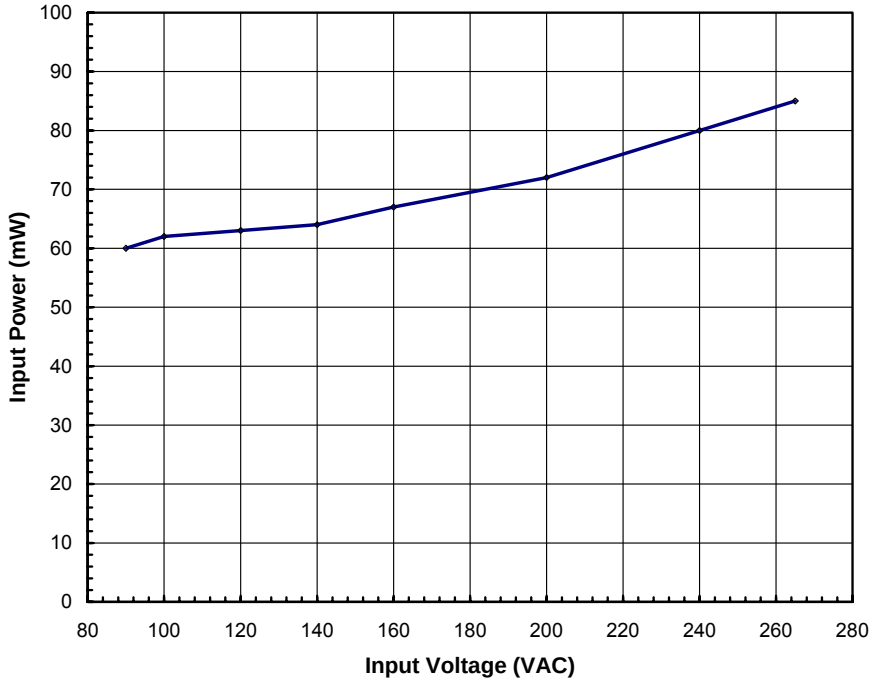

Figure 9 – No-Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

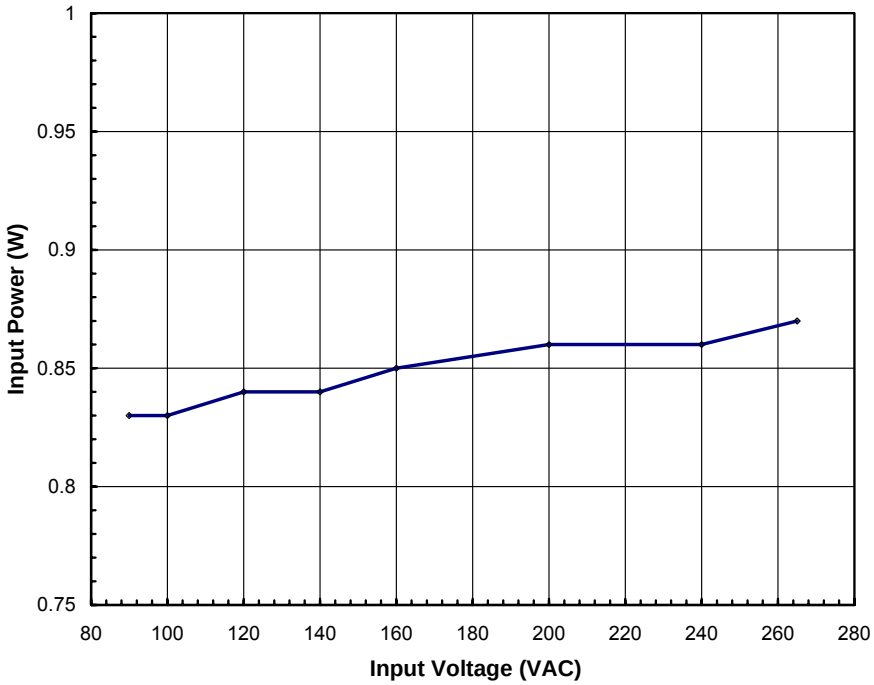

Figure 10 – Input Power vs. Input Voltage, 0.5 W Load, Room Temperature, 60 Hz.

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9.3 Regulation

All outputs were taken from minimum to maximum loads (per Table 1) according to the table below. The resultant overall variation in the output voltages is shown in Table 3.

-24 V	3.3 V	5 V	12 V
M	M	M	M
m	M	M	M
m	m	m	M
M	m	M	M
M	M	m	M
M	m	m	M
-	-	-	-
M = Max load, m = Min load, - = Unloaded			

Table 2 – Load Conditions for Cross-regulation Results.

		Regulation (% of nominal)															
Output	**Results**	**-5**	**-4**	**-3**	**-2**	**-1**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
3.3 V	-2.1% to -0.9%														
5 V	-3.6% to +2.2%														
12 V	-4.4% to +5%														
-24 V	-3.8% to +8%														

Table 3 – Cross-regulation Results.

10 Thermal Performance

The temperature of key components was measured at the maximum specified ambient of 50 °C. In addition to checking for hotspots, an infrared thermograph was taken at room ambient (as this is output as a color profile, please use the color version of this document, available at *www.powerint.com/epr.htm*, to review the temperatures).

Temperature (°C)			
Item	**90 VAC**	**115 VAC**	**230 VAC**
Ambient	51	51.4	51
Common Mode (L1)	90	82	67
Transformer (T1)	85	79	83
***TOPSwitch-GX* (U1)**	102	93	80
5 V Rectifier (D11)	112	112	113
3.3 V Rectifier (D10)	107	99	98

Table 4 – Temperature of Key Components, 50 °C Ambient.

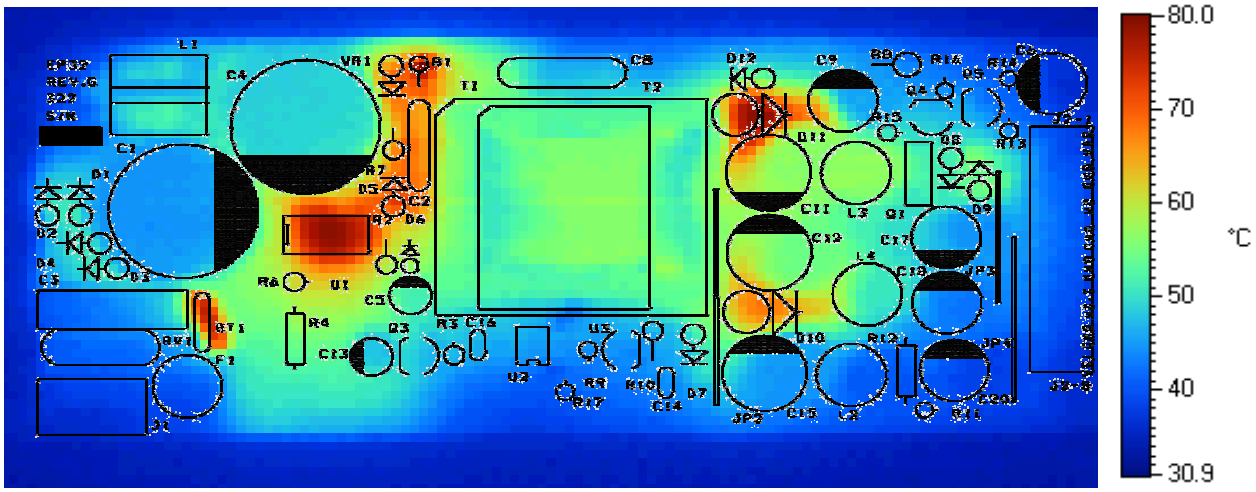

Figure 11 – Infrared Thermograph (with silk screen overlaid) of EP-32, 90 VAC Input, 20 W Load (5 V at 2 A, 3.3 V at 2 A, 12 V at 0.28 A, -24 V at 0 A), 23 °C Ambient.

In order to make the thermograph representative of the actual component temperatures, the entire board was spray painted black to give a uniform emissivity value.

The thermograph shows the hottest parts to be the input thermistor RT1, TOP245P, VR1, R1 in the clamp, and D11, the 5 V output diode. The highest temperature measured was 80 °C on R1, however, all components would remain acceptably less than 110 °C in an ambient of 50 °C.

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11 Waveforms

11.1 Drain Voltage and Current Waveforms

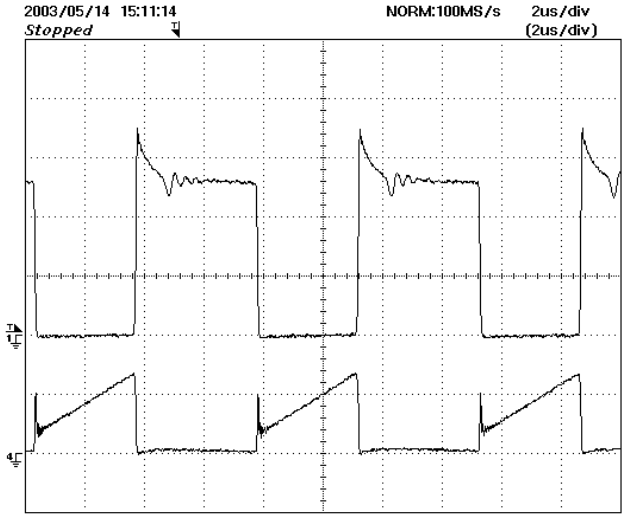

Figure 12 – 115 VAC, Full Load.
Upper: V_{DRAIN}, 100 V, 2 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

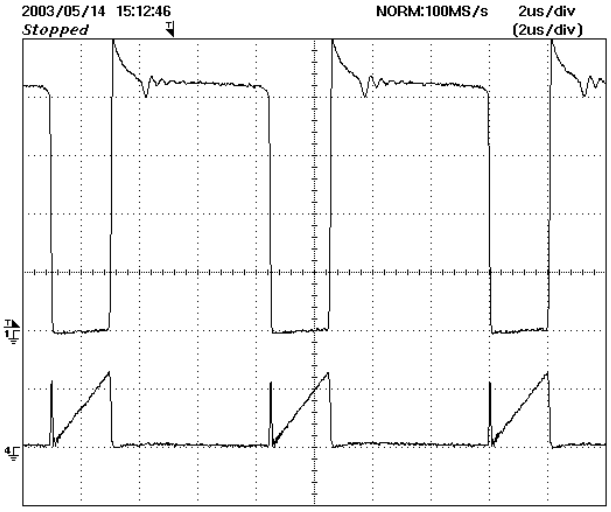

Figure 13 – 230 VAC, Full Load
Upper: V_{DRAIN}, 100 V, 2 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

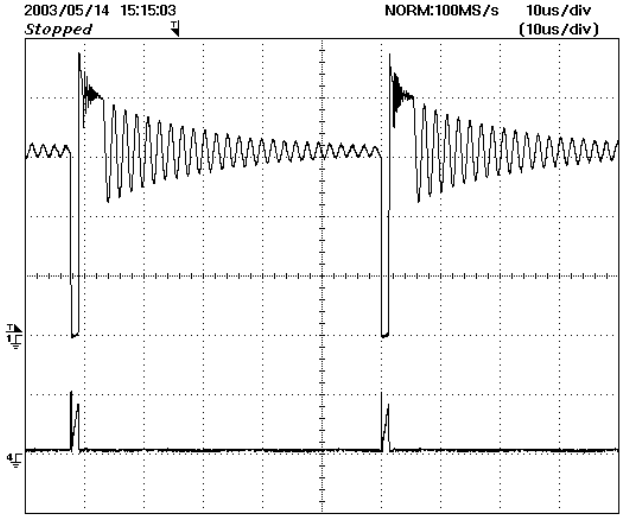

Figure 14 – 230 VAC, 0.5 W Load Showing Reduced Frequency Operation.
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

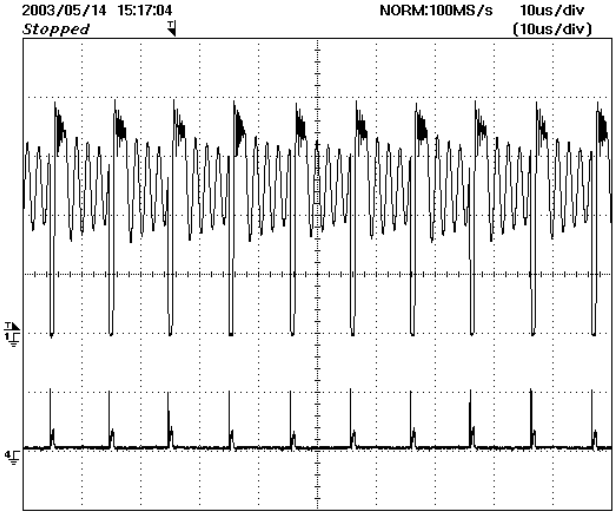

Figure 15 – 230 VAC, 1.5 W Load Showing Reduced Frequency Operation.
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

11.2 Output Voltage Start-up Profile

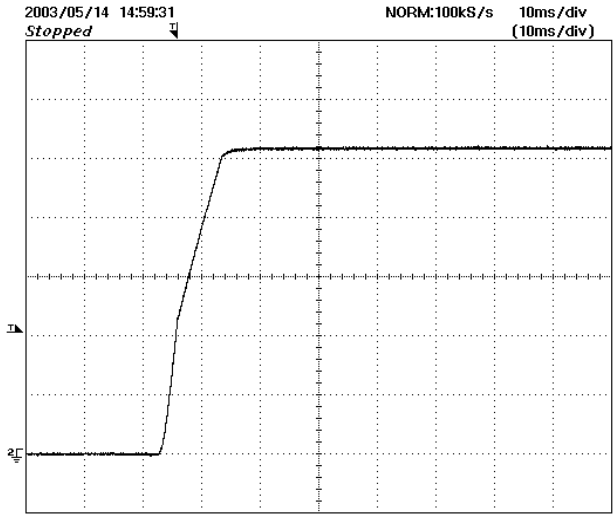

Figure 16 – 5 V output start-up Profile, 115 VAC,
Full load. 1 V, 10 ms / div.

11.3 Load Transient Response

Each output was step loaded according to the information below each of the transient response oscillograms below. All other outputs were set to maximum load.

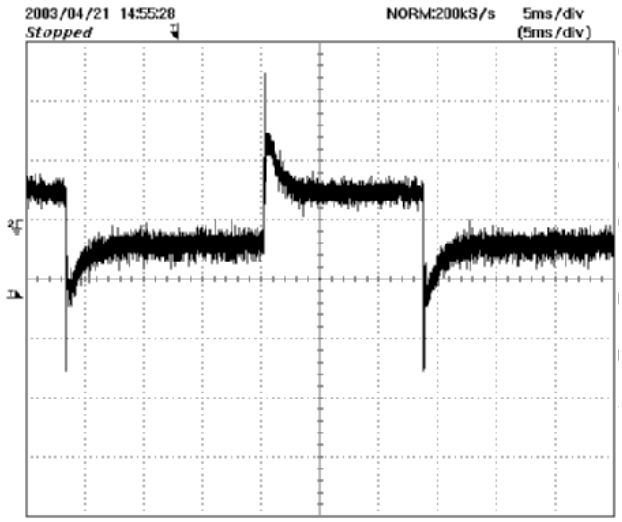

Figure 17 – Transient Response, 115 VAC,
50-100-50% Load Step, Max Load.
3.3 V Output Voltage,
20 mV, 5 ms / div.

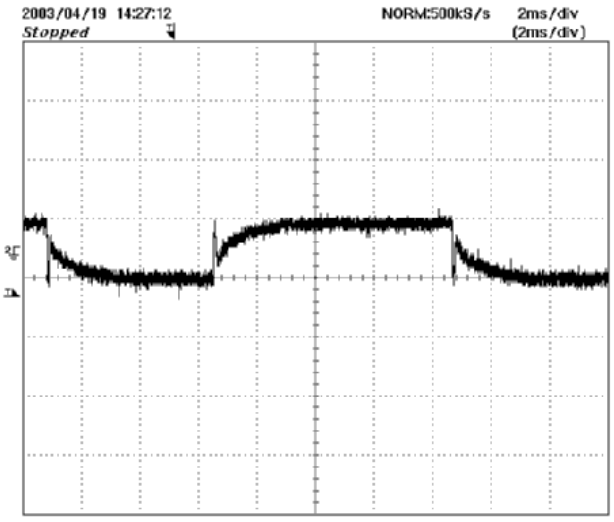

Figure 18 – Transient Response, 115 VAC,
60-100-60% Load Step, Max Load.
5 V Output Voltage
50 mV, 2 ms / div.

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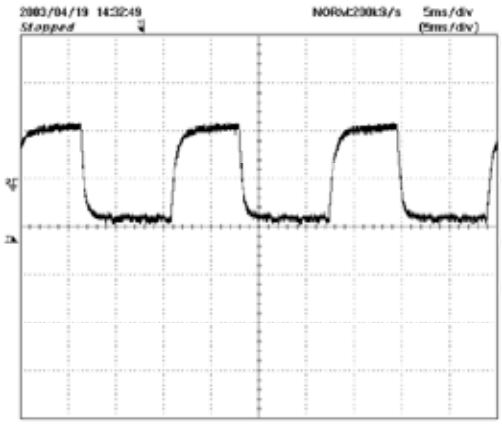

Figure 19 – Transient Response, 115 VAC,
40-100-40% Load Step, Max Load.
12 V Output Voltage
100 mV, 5 ms / div.

11.4 Output Ripple Measurements

All measurements were taken at maximum load on all outputs.

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 19 and Figure 20.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. *The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).*

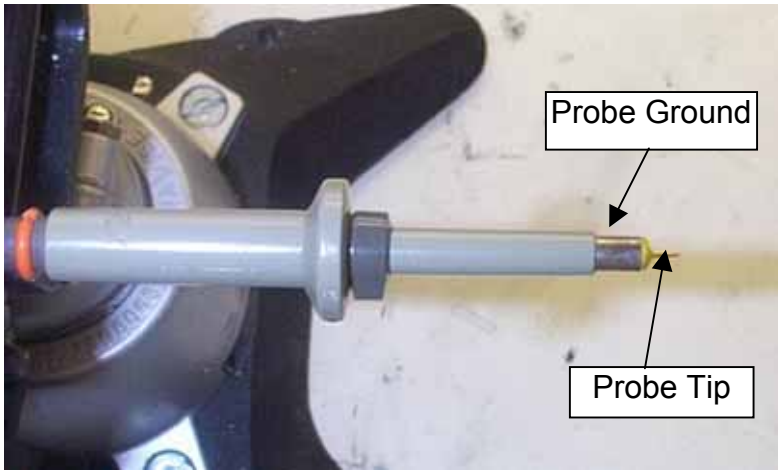

Figure 20 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

Figure 21 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

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11.4.2 Measurement Results

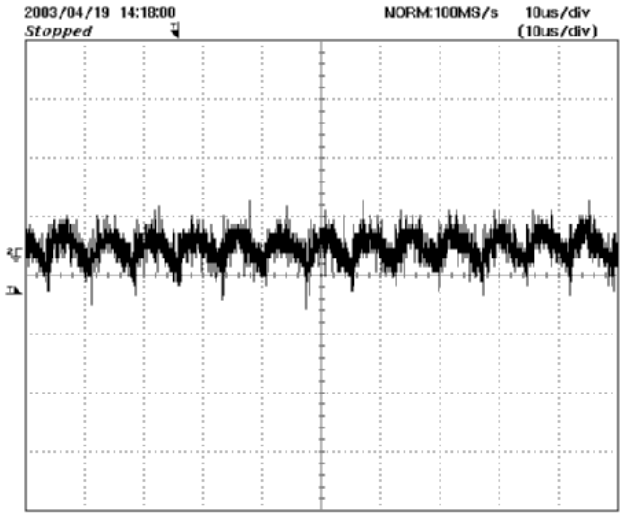

Figure 22 – 3.3 V Ripple, 115 VAC, Full Load, 10 μs, 10 mV / div.

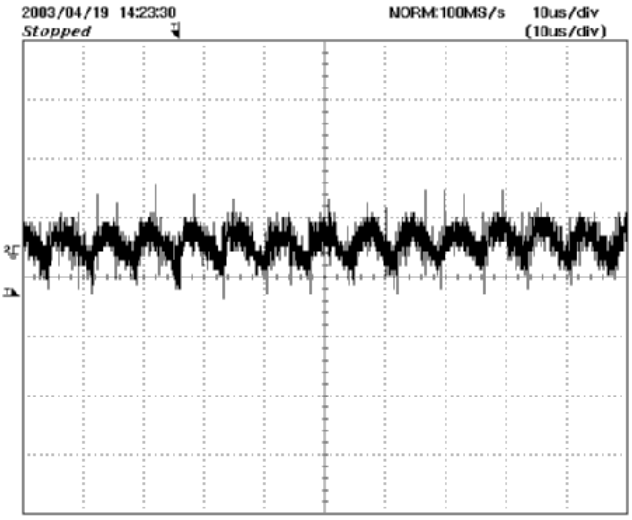

Figure 23 – 5 V Ripple, 115 VAC, Full Load, 10 μs, 10 mV / div.

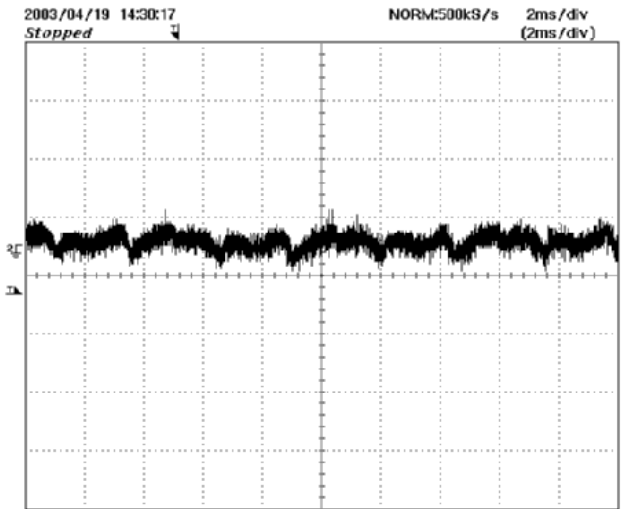

Figure 24 – 12 V Ripple, 115 VAC, Full Load, 2 ms, 20 mV /div.

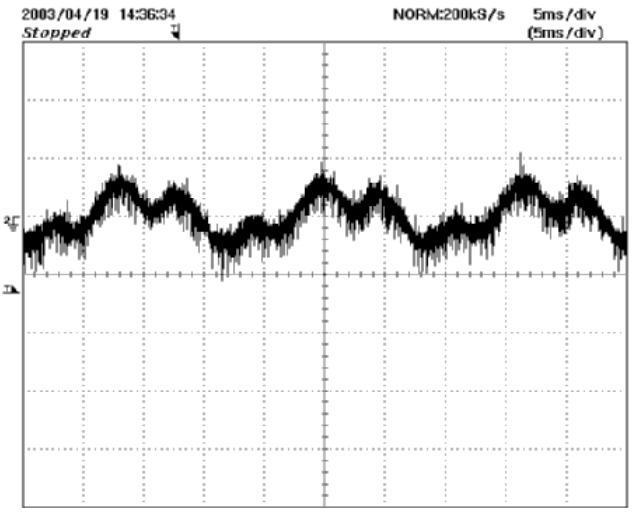

Figure 25 – -24 V Ripple, 115 VAC, Full Load, 5 ms, 20 mV /div.

12 Control Loop Gain/Phase Measurements

12.1 115 VAC Maximum Load

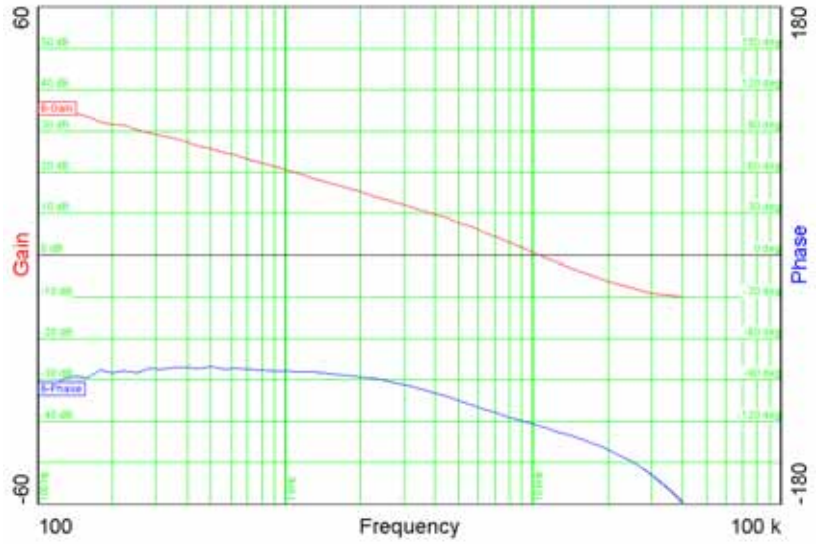

Figure 26 – Gain-Phase Plot, 180 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30°/div.
Crossover Frequency = 10 kHz, Phase Margin = 60°.

12.2 115 VAC 50% Load

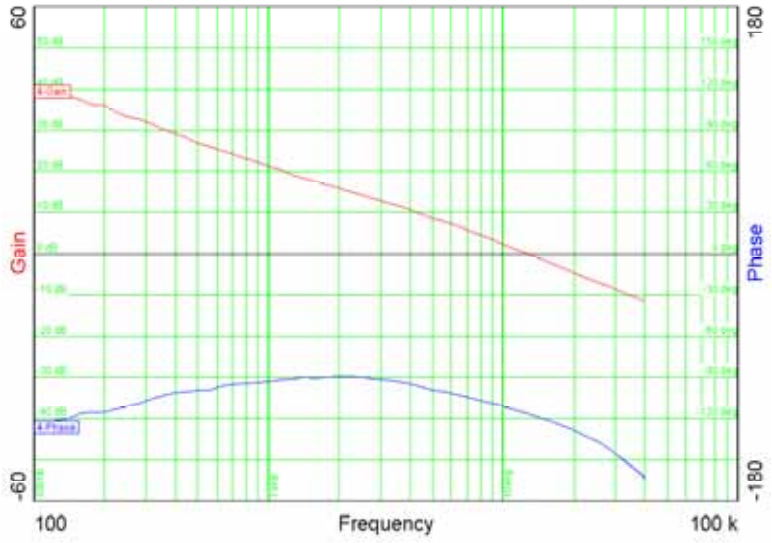

Figure 27 – Gain-Phase Plot, 180 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30°/div.
Crossover Frequency = 13 kHz, Phase Margin = 70°.

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12.3 115 VAC Minimum Load

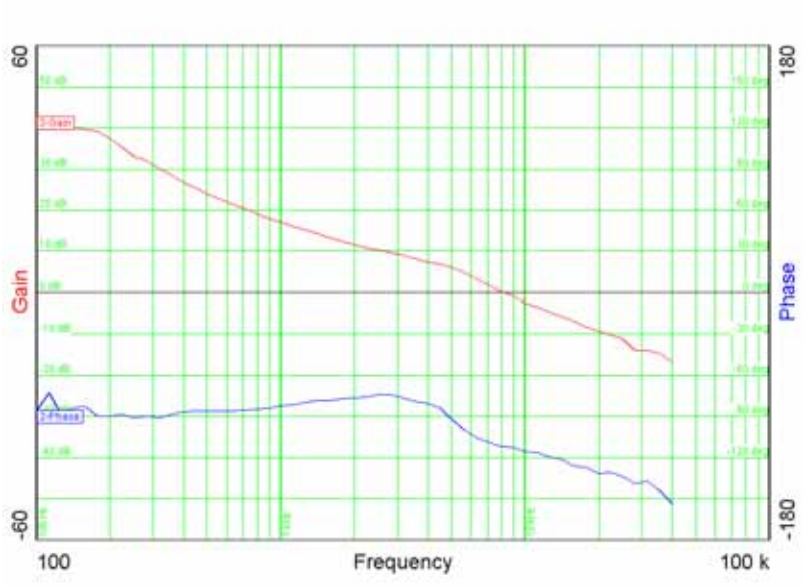

Figure 28 – Gain-Phase Plot, 180 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30°/div.
Crossover Frequency = 8 kHz, Phase Margin = 70°.

12.4 230 VAC Maximum Load

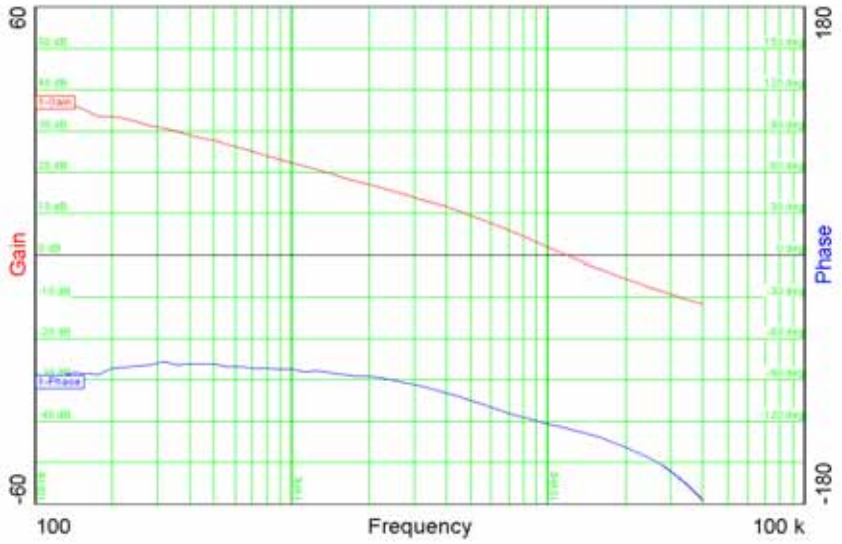

Figure 29 – Gain-Phase Plot, 230 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30 °/div.
Crossover Frequency = 12 kHz, Phase Margin = 50°.

12.5 230 VAC 50% Load

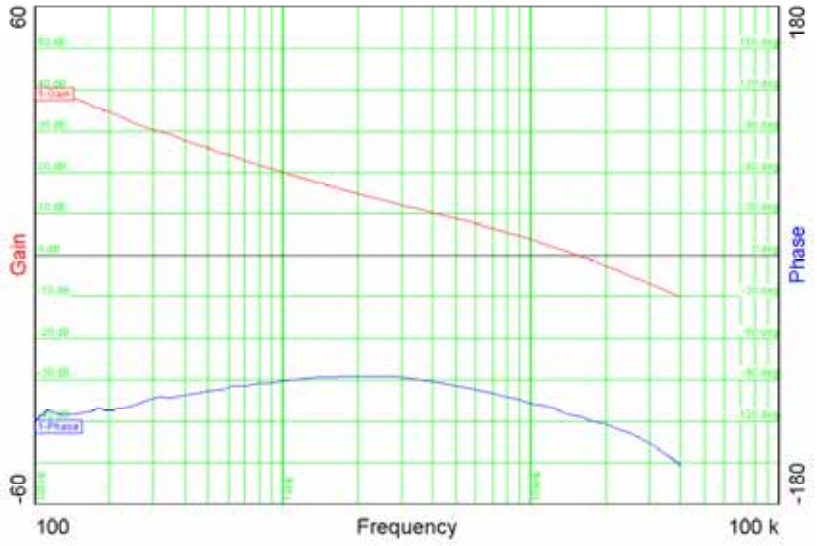

Figure 30 – Gain-Phase Plot, 230 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30°/div.
Crossover Frequency = 17 kHz, Phase Margin = 62°.

12.6 230 VAC Minimum Load

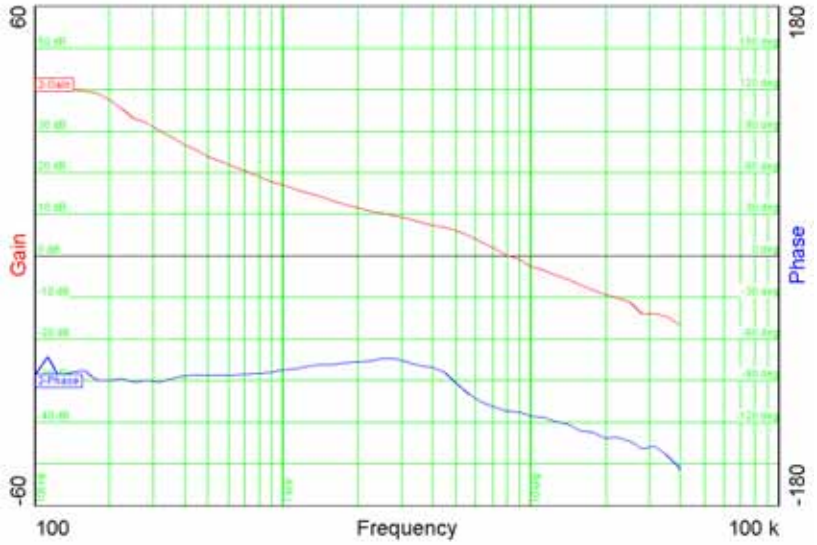

Figure 31 – Gain-Phase Plot, 230 VAC, Maximum Steady State Load.
Vertical Scale: Gain = 10 dB/div, Phase = 30°/div.
Crossover Frequency = 8 kHz, Phase Margin = 70°.

These results show that the X pin current mode control provides excellent bandwidth and phase margin at gain cross-over under all operating conditions.

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13 Conducted EMI

The results below show excellent conducted and expected radiated EMI performance (the scans were extended to 100 MHz to indicate radiated performance). In all cases >20 dB margin was measured to both Quasi-Peak (upper red traces and red limit line) and Average (lower green traces and blue limit line) limits.

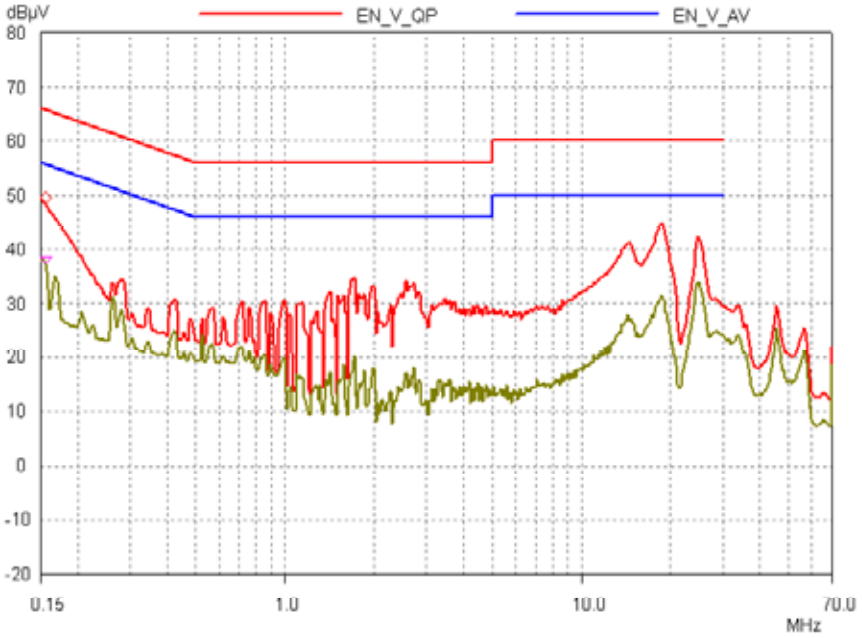

Figure 32 – Conducted EMI, Maximum Load, 115 VAC, Line, 60 Hz, and EN55022 B Limits.

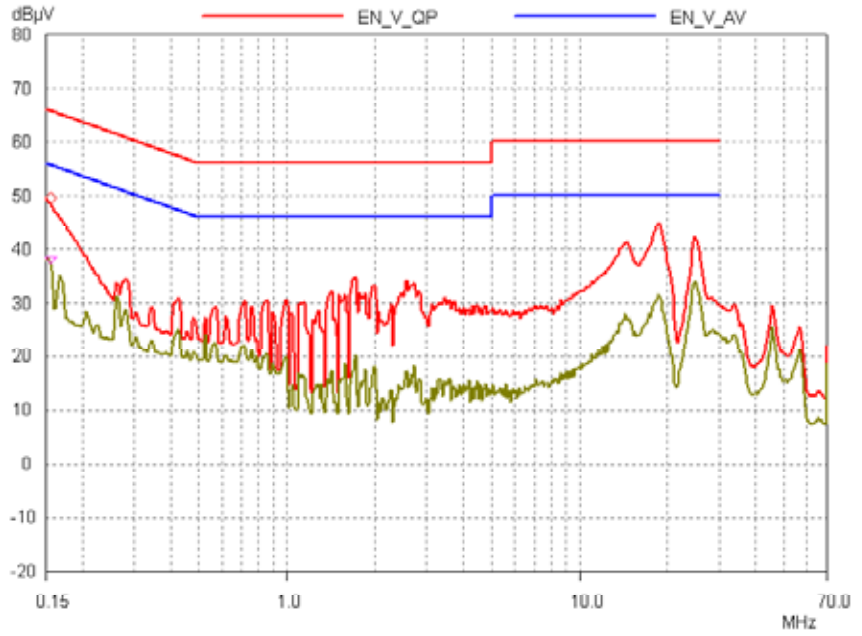

Figure 33 – Conducted EMI, Maximum Load, 115 VAC, Neutral, 60 Hz, and EN55022 B Limits.

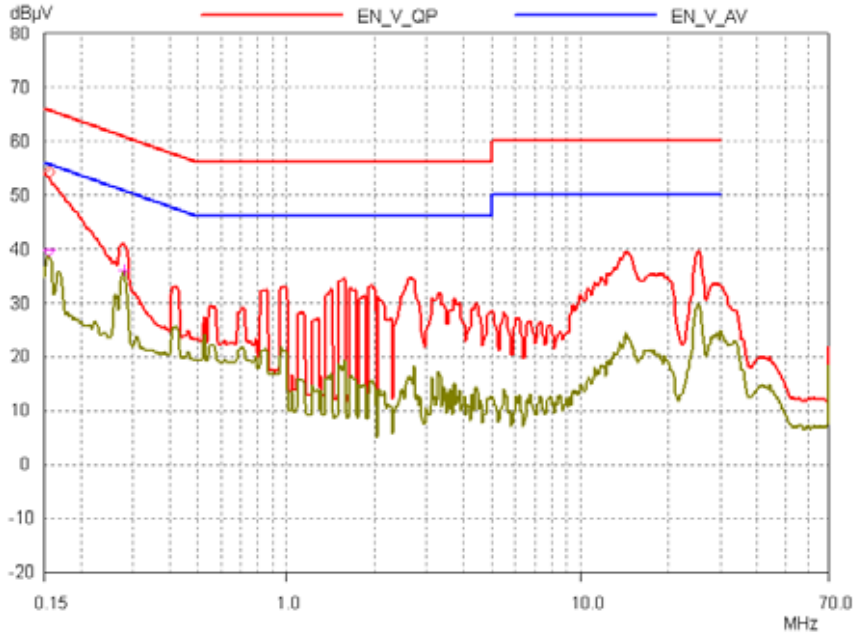

Figure 34 – Conducted EMI, Maximum Load, 230 VAC, Line, 60 Hz, and EN55022 B Limits.

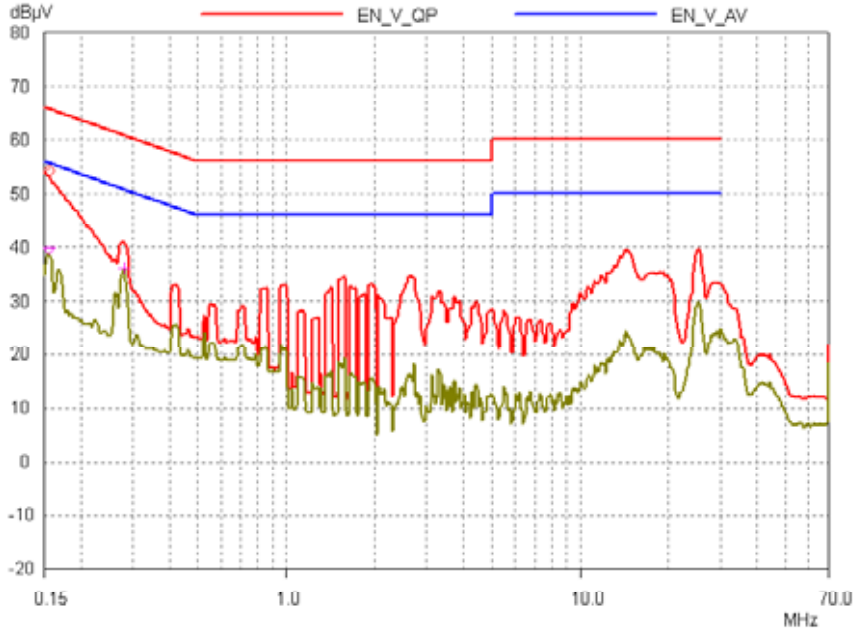

Figure 35 – Conducted EMI, Maximum Load, 230 VAC, Line, 60 Hz, and EN55022 B Limits.

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14 Revision History

Date	Author	Revision	Description & changes
10-May-03	AoD	0.1	First draft
07-July-03	AoD	0.2	Second draft – updated transformer spec
22-July-03	AoD	0.3	Third draft – thermal image and gain phase data added
06-Aug-03	PV	0.4	Fourth draft – formatting, circuit description added and final board photograph
08-Aug-03	IM	1.0	First release
13-Jul-06	PV	1.1	Updated Figure 2.

Notes

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