Reference Design Automotive

Title	**General Purpose Automotive Gate Driver Board for SCALE-iDriver™ SIC1182KQ**
Application	1200 V TO-247-4L Power Devices (IGBT/ SiC-MOSFET) in Half-Bridge Topology
Document Number	RDHP-2301Q
Author	System Engineering Automotive
Date	November 13, 2023
Revision	1.0

Feature Set

- Designed for 800 V_{DC} BEV automotive applications
- Low component count design
- Ambient operating temperature from -40°C to 105°C
- Reinforced isolation between high and low voltage domains (IEC-60664-1 and IEC-60664-4 compliant)
- Uses automotive qualified AEC-Q surface mount (SMD) components[1]
- SIC1182KQ specific features:
    - ±8 A gate drive current
    - PWM Input Interlocking
    - Ultrafast Short-circuit monitoring
    - AROC for transient overvoltage limitation
    - UVLO protection for primary and secondary-side
    - SO fault signaling

PATENT INFORMATION
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[1] AEC-Q200 transformer qualification belongs to final design

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1 Introduction

This document provides a detailed report on the results of tests performed on RDHP-2301Q as a gate driver board for On Semi's NVH4L020N120SC1 SiC MOSFET.

RDHP-2301Q is an automotive reference design board which features Power Integrations´ SIC1182KQ SCALE-iDriver^{TM}. This board is intended for driving two power devices (i.e., SiC-MOSFET/ IGBT) in a half-bridge configuration, each with a blocking voltage up to 1200 V and device package of TO-247-4L.

The goal of this test is to demonstrate the functionality of SIC1182KQ gate driver IC in safely turning on/off a 1200 V power device during normal operation and short-circuit condition. This is to enable potential end customers to evaluate Power Integrations' gate driver and power supply solutions for automotive applications.

Included in this document are the design specifications, schematic diagram, bill of materials (BOM), magnetics documentation, printed circuit board (PCB) layout and performance data.

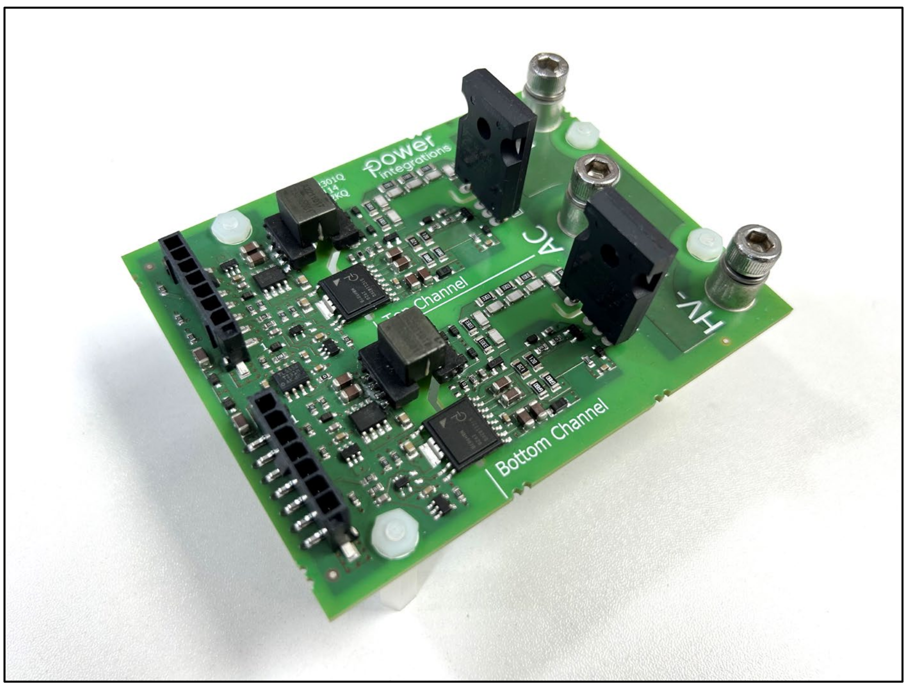

Figure 1 – Populated Circuit Board of RDHP-2301Q.

2 Design Specification

The table below represents the minimum acceptable performance of the design. The actual performance of the design is listed in the results section.

2.1 Electrical Specification

Description	Symbol	Min.	Typ.	Max.	Units
Low Voltage (LV) Side					
LV-side IC supply voltage referenced to GND for top and bottom channel driver	V_{VCC1} V_{VCC2}	4.75	5.00	5.25	V_{DC}
LV-side IC current consumption for top and bottom channel driver (f_{SW} = 75 kHz)	I_{VCC1} I_{VCC2}		25	35	mA
LV-side total power consumption of both channels (f_{SW} = 75 kHz)	$P_{VCC,\ TOTAL}$		250		mW
LV-side PWM command input referenced to GND for top and bottom channel driver	IN1 IN2	GND		5	V_{DC}
LV-side fault feedback referenced to GND for top and bottom channel driver	SO1 SO2	GND		5	
Primary-side reference ground	GND		0		V_{DC}
PWM command operating switching frequency	f_{sw}	5		75	kHz
High Voltage (HV) Side					
Positive DC Link input voltage referenced to HV-	HV+		800	850	V_{DC}
HV-side IC supply voltage referenced to V_{COM1}/ V_{COM2} for top and bottom channel driver	V_{VISO1} - V_{COM1} V_{VISO2} - V_{COM2}	18.00	20.00	21.00	V_{DC}
HV-side positive supply voltage referenced to V_{VEE1}/ V_{VEE2} for top and bottom channel driver	V_{VISO1} V_{VISO2}		15.00		V_{DC}
HV-side negative supply voltage referenced to V_{VEE1}/ V_{VEE2} for top and bottom channel driver	V_{COM1} V_{COM2}	-3.00	-5.00	-6.00	V_{DC}
HV-side IC current consumption for top and bottom channel driver (f_{SW} = 75 kHz)	I_{VISO1} I_{VISO2}		11	14	mA
HV-side supply power consumption per channel (f_{SW} = 75 kHz)	P_{VISO1} P_{VISO2}		220		mW
Gate power approximation for driving NVH4L020N120SC1 SiC MOSFET (ΔV = 20 V, f_{SW} = 75 kHz, $Q_g \approx$ 170 nC)	P_{GATE1} P_{GATE2}		255		mW
HV-side total power consumption of both channels [(P_{VISO1} + P_{GATE1}) + (P_{VISO2} + P_{GATE2})]	$P_{VISO,\ TOTAL}$		950		mW

Table 1 – Gate Drive Unit Electrical Requirements.

2.2 Isolation Coordination

Description	Symbol	Min.	Typ.	Max.	Units
Maximum blocking voltage of INN3947CQ	BV_{DSS}			1700	V
Maximum blocking voltage of NVH4L020N120SC1 SiC MOSFET	$V_{DS,max}$			1200	V
Working voltage	$V_{WORKING}$			850	V
System voltage	$V_{PK, SYSTEM}$			850	V
Rated impulse voltage	$V_{IMPULSE}$			2.5	kV
Comparative Tracking Index of FR4	CTI	175		399	
Pollution Degree	PD			2	
Altitude correction factor for h_a	Ch_a			1.29	
Technical cleanliness				1.0	mm
Basic clearance distance requirement	CLR_{BASIC}	3.0			mm
Reinforced clearance distance requirement	$CLR_{REINFORCED}$	4.9			mm
Basic creepage distance requirement	CPG_{BASIC}	5.8			mm
Reinforced creepage distance requirement	$CPG_{REINFORCED}$	9.5			mm
Isolation test voltage between low and high voltage side for 60s	V_{ISO}			4200	V_{PK}
Partial Discharge test voltage	V_{PD_TEST}			1800	V_{PK}

Table 2 – Isolation Requirements.

2.3 Environmental Specification

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_a	-40		105	V
Altitude of Operation	h_a			4000	m

Table 3 – Power Supply Unit Electrical Requirements.

3 Schematic

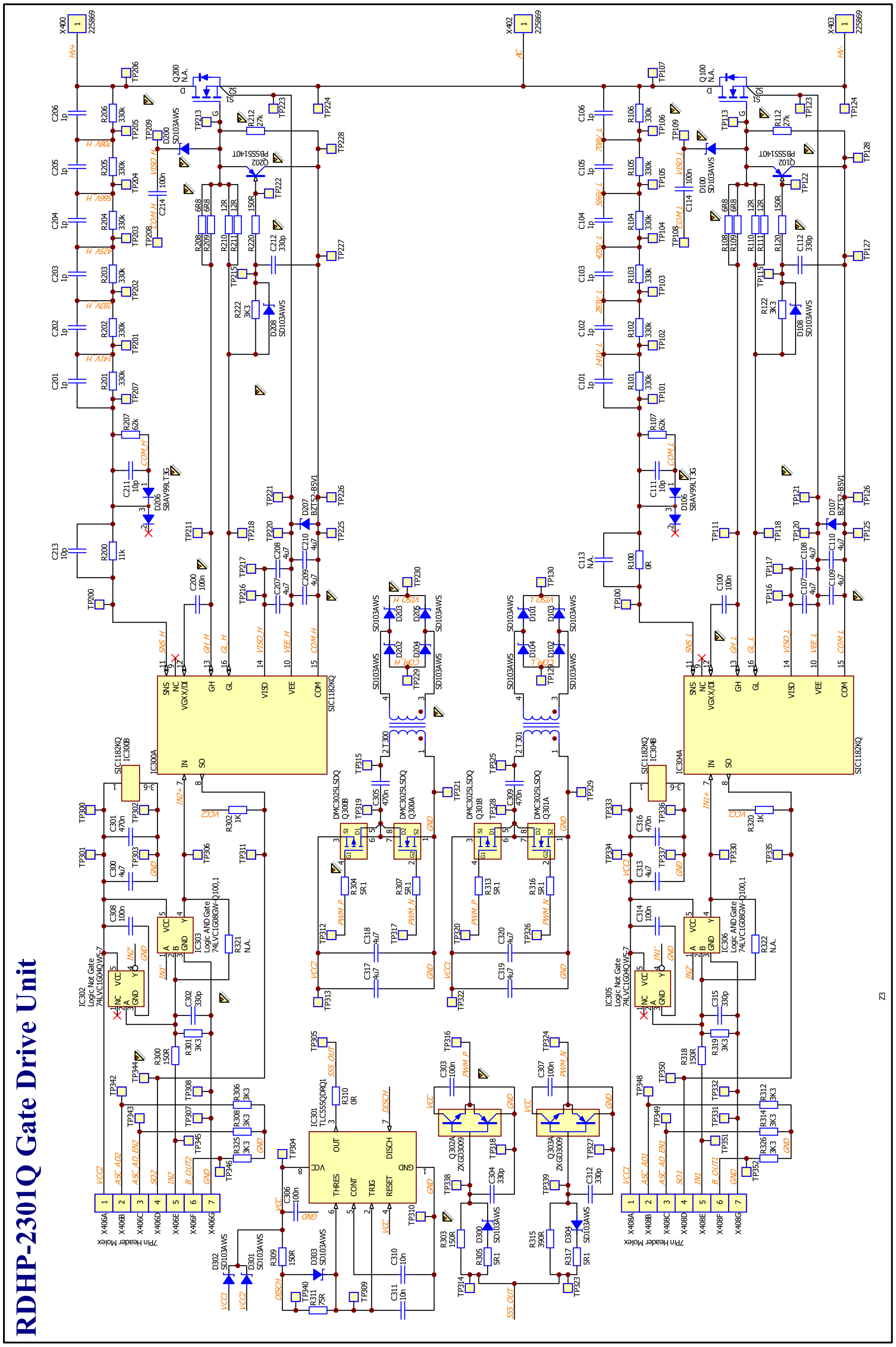

Figure 2 – Schematic Diagram (SCALE-iDriver).

4 PCB Layout

Layers: Six (6) (typical for traction inverter control board)
Board Material: FR4
Board Thickness: 2 mm
Copper Weight: 2 oz (outer layers), 3 oz (inner layers)

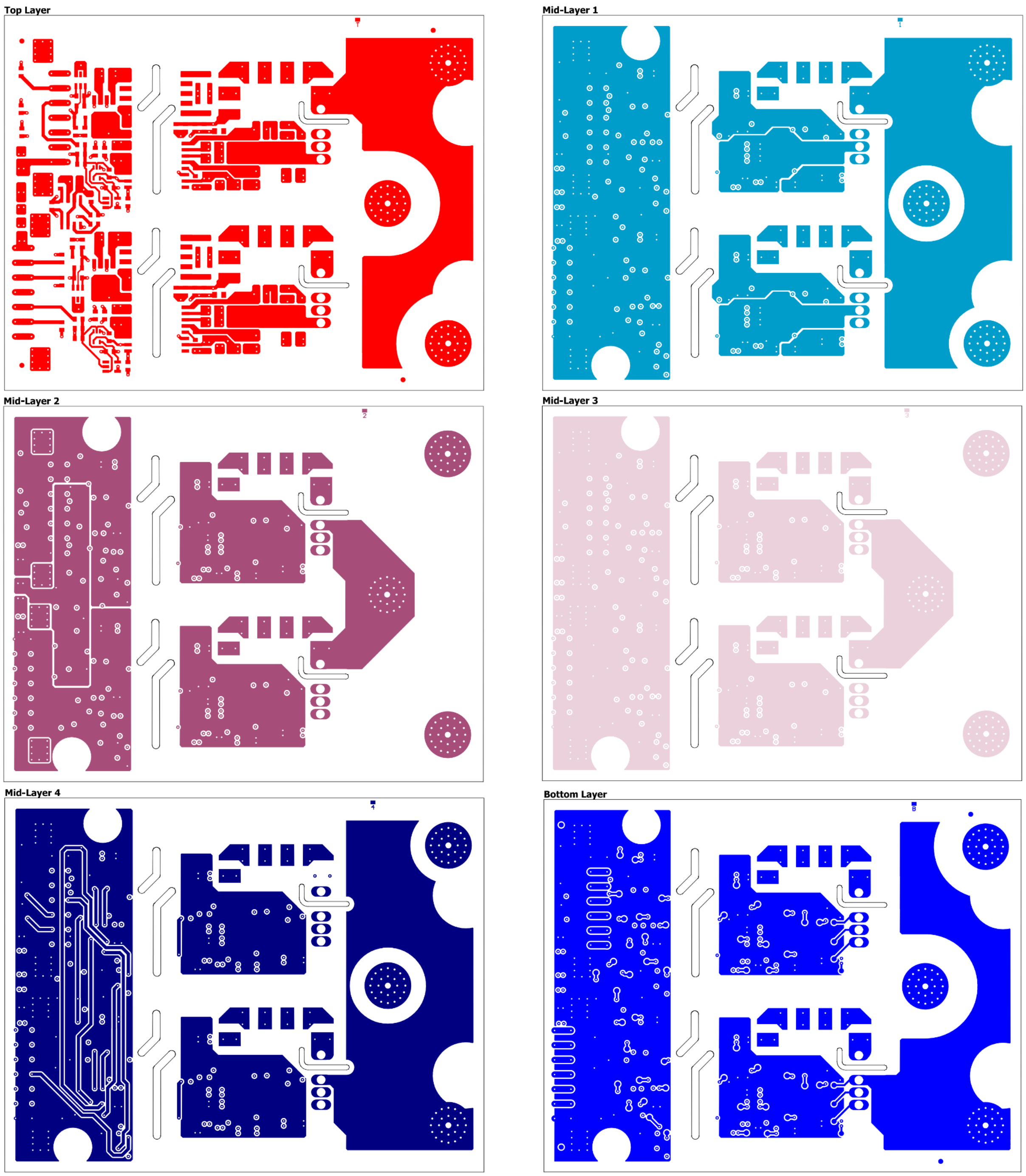

Figure 3 – RDHP-2301Q PCB Layout.

5 PCB 3D Image

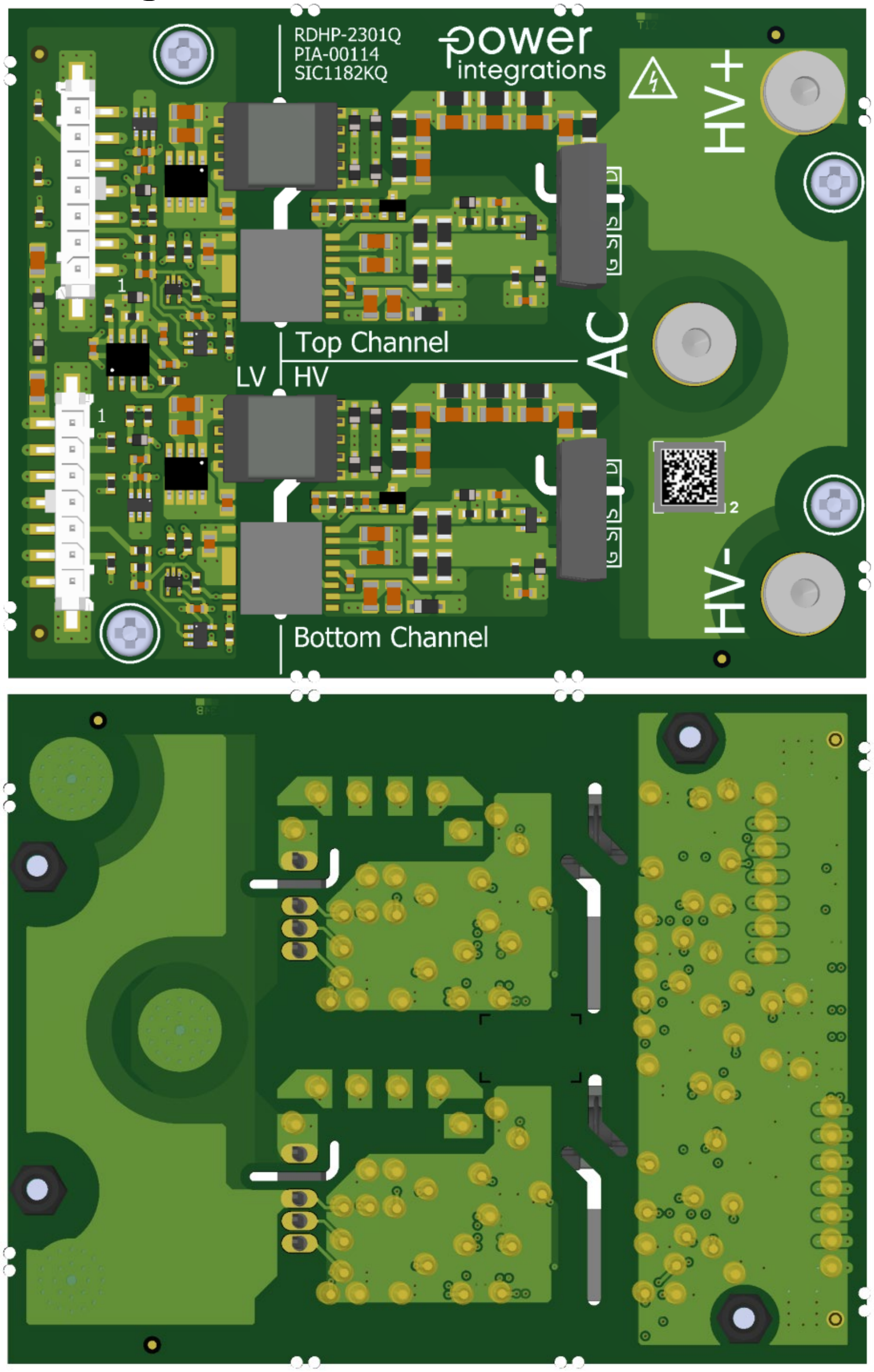

Figure 4 – RDHP-2301Q PCB 3D Render.

6 Board Assembly

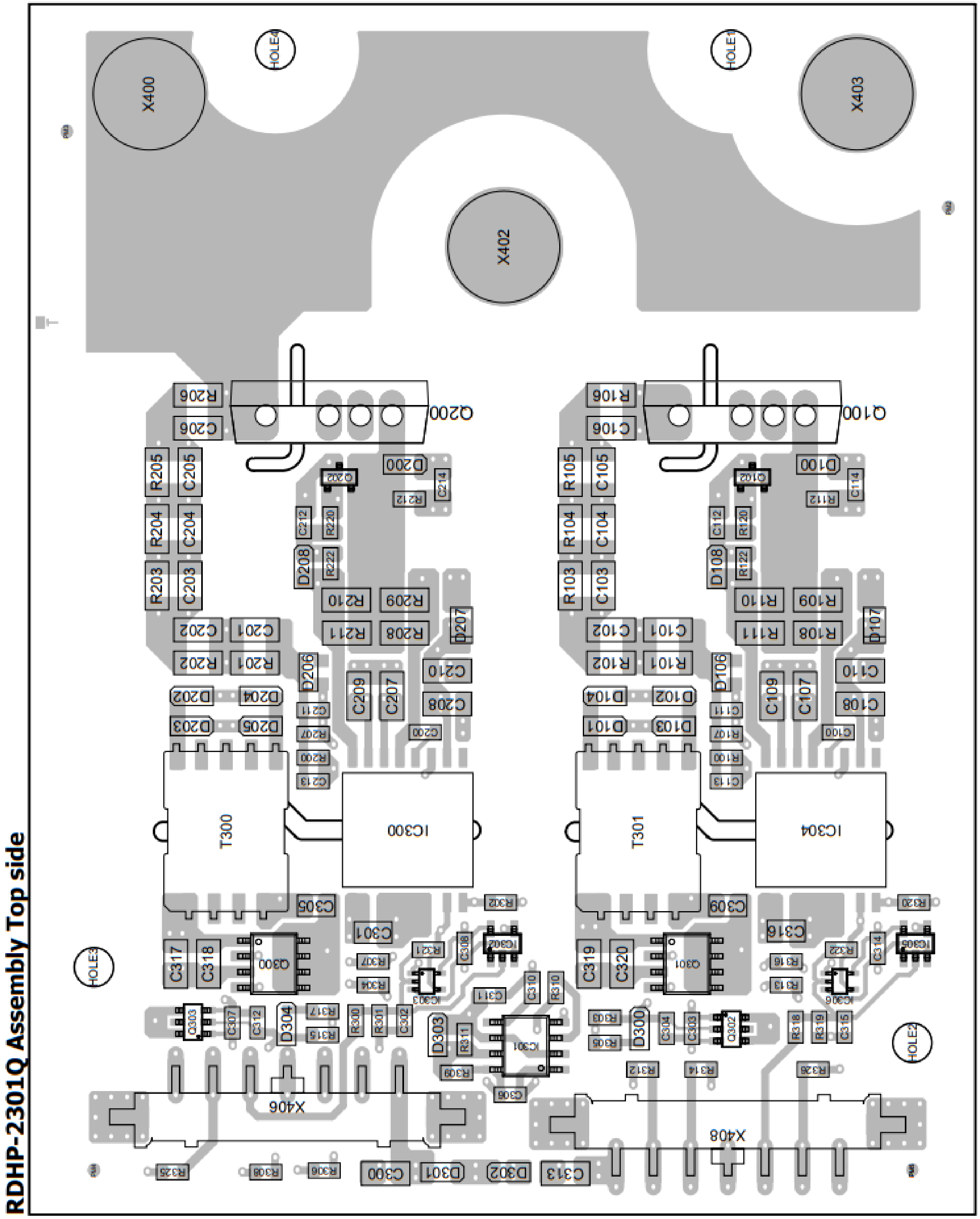

Figure 5 – Board Assembly.

7 Bill of Materials

Item	Qty	Designator	Value	MFR Part Number	Manufacturer
1	9	C100, C114, C200, C214, C303, C306, C307, C308, C314	100n	CL10B104KB8WPNC	Samsung
2	12	C101, C102, C103, C104, C105, C106, C201, C202, C203, C204, C205, C206	1p	GA1206D1R0BXLAT31M	Vishay
3	14	C107, C108, C109, C110, C207, C208, C209, C210, C300, C313, C317, C318, C319, C320	4u7	C1206X475K5RACAUTO	KEMET
4	3	C111, C211, C213	10p	CL10C100CB81PNC	Samsung
5	6	C112, C212, C302, C304, C312, C315	330p	CL10C331JB81PNC	Samsung
6	1	C113	N.A.		
7	4	C301, C305, C309, C316	470n	AC0805KKX7R7BB474	YAGEO
8	2	C310, C311	10n	C0603C103M5RACAUTO	KEMET
9	17	D100, D101, D102, D103, D104, D108, D200, D202, D203, D204, D205, D208, D300, D301, D302, D303, D304	SD103AWS	SD103AWS-AU_R1_000A1	Panjit
10	2	D106, D206	SBAV99LT3G	SBAV99LT3G	On Semi
11	2	D107, D207	BZT52-B5V1	BZT52-B5V1	NXP
12	2	IC300, IC304	SIC1182KQ	SIC1182KQ	Power Integrations
13	1	IC301	TLC555QDRQ1	TLC555QDRQ1	Texas Instruments
14	2	IC302, IC305	Logic Not Gate	74LVC1G04QW5-7	Diodes, Inc.
15	2	IC303, IC306	Logic AND Gate	74LVC1G08GW-Q100,1	Nexperia
16	2	Q100, Q200	N.A.	N.A.	N.A.
17	2	Q102, Q202	PBSS5140T	PBSS5140T,215	Nexperia
18	2	Q300, Q301	DMC3025LSDQ	DMC3025LSDQ-13	Diodes
19	2	Q302, Q303	ZXGD3009	ZXGD3009E6TA	DIODE
20	2	R100, R310	0R	AC0603FR-070RL	Yageo
21	12	R101, R102, R103, R104, R105, R106, R201, R202, R203, R204, R205, R206	330k	AC1206FR-07330KL	YAGEO
22	2	R107, R207	62k	ERJ-3GEYJ623V	Panasonic
23	4	R108, R109, R208, R209	6R8	AC1206FR-076R8L	YAGEO
24	4	R110, R111, R210, R211	12R	AC1206JR-0712RL	YAGEO
25	2	R112, R212	27k	AC0603JR-0727KL	YAGEO
26	6	R120, R220, R300, R303, R309, R318	150R	CRGCQ0603J150R	TE Connectivity
27	10	R122, R222, R301, R306, R308, R312, R314, R319, R325, R326	3K3	CRGCQ0603J3K3	TE Connectivity
28	1	R200	11k	ERJ-3EKF1102V	Panasonic
29	2	R302, R320	1K	CRGCQ0603J1K0	TE Connectivity
30	6	R304, R305, R307, R313, R316, R317	5R1	RMCF0603FT5R10	Stackpole
31	1	R311	75R	AC0603FR-0775RL	YAGEO
32	1	R315	390R	ERJ-3GEYJ391V	Panasonic
33	2	R321, R322	N.A.		
34	2	T300, T301	EP7	EP7	Power Integrations
35	3	X400, X402, X403	225869	225869	ERNI Electronics
36	2	X406, X408	7Pin Header Molex	436500724	Molex

Table 4 – Bill of Materials.

8 Test Set-up

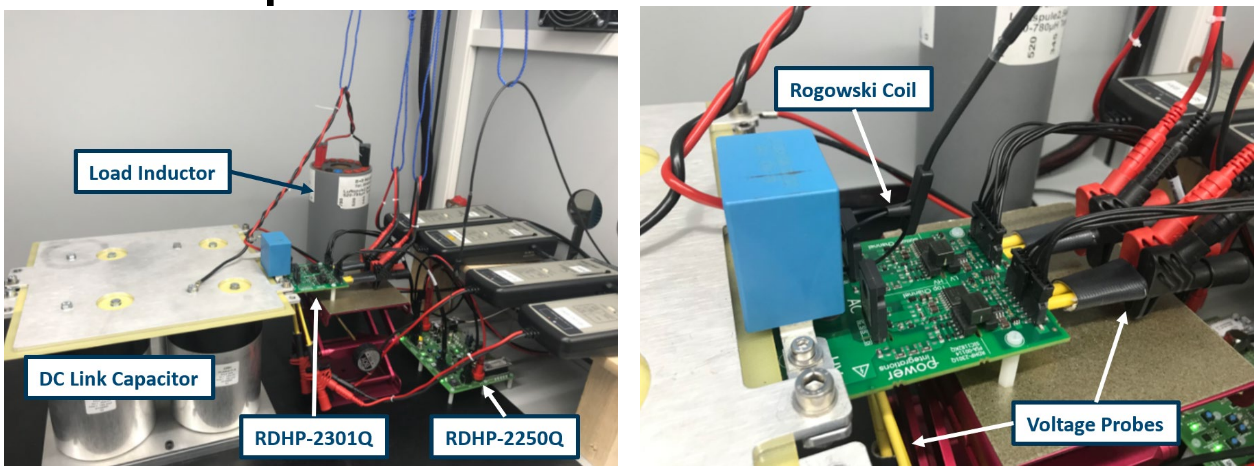

Figure 6 – Test Setup for HV Testing at T_J = 25 °C (configuration shown is for bottom channel testing)

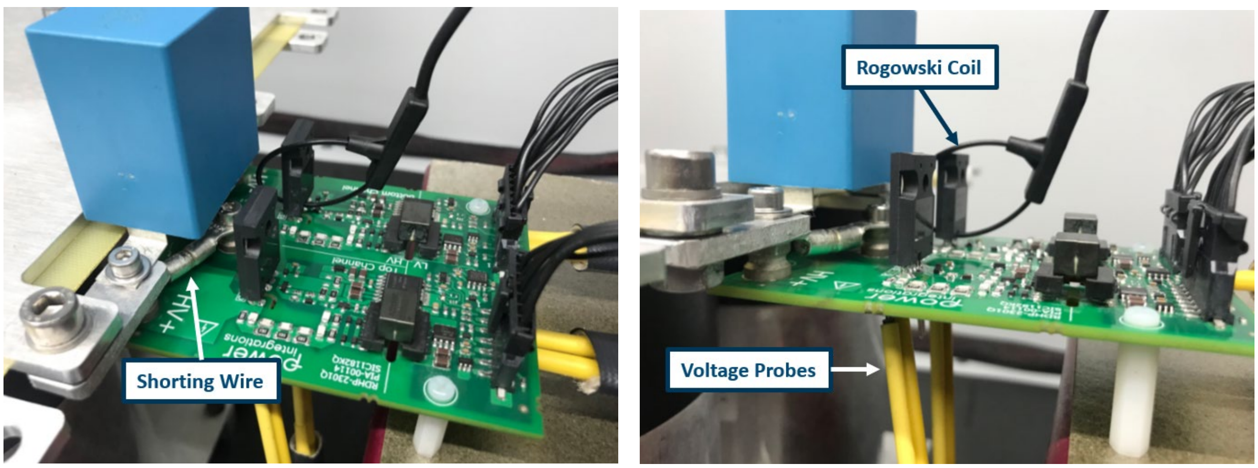

Figure 7 – Test Setup for HV Short-Circuit Testing at T_J = 25 °C (configuration shown is for bottom channel testing with top channel D-S shorted)

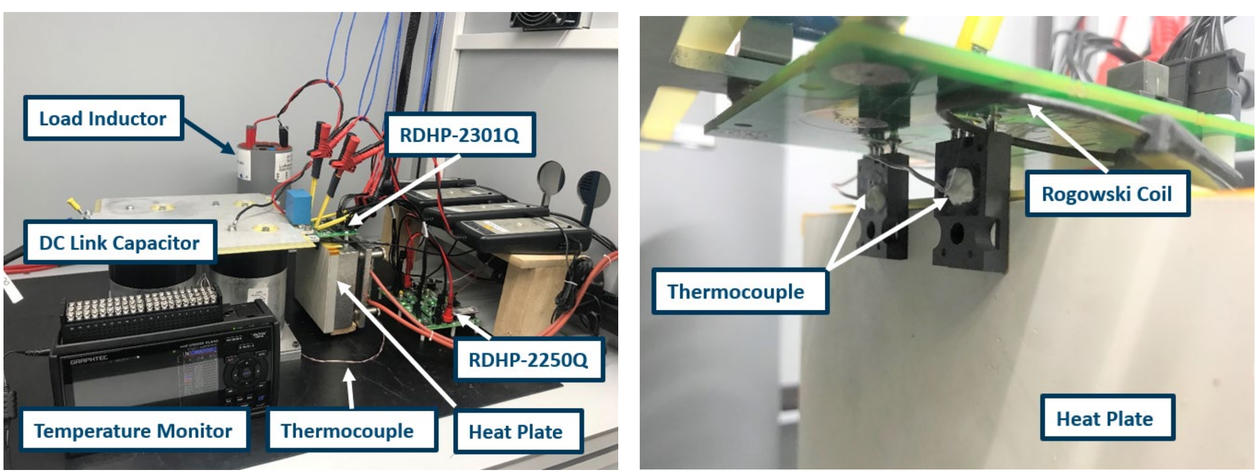

Figure 8 – Test Setup for HV Testing at T_J = 125 °C (configuration shown is for top channel testing).

For set-up verification of Figure 8, a thermal image was captured prior to each test to confirm the temperature of the SiC MOSFETs. Figure 9 confirms that both power devices are at 125°C.

Additionally, due to the heat plate's location being directly below the PCB, the surface temperature on the secondary side of board was increased to 80°C as shown in Figure 10.

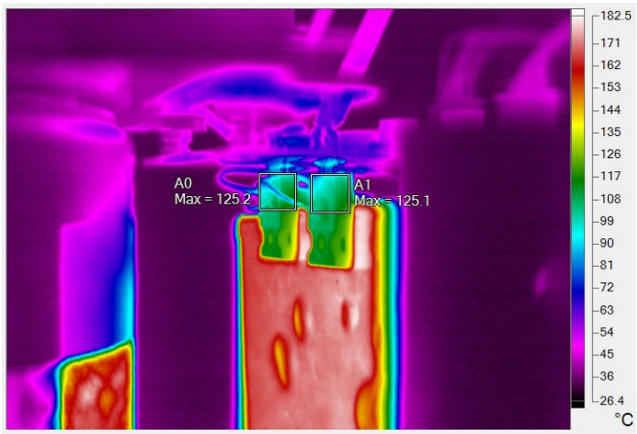

Figure 9 – SiC MOSFET Thermal Image during HV Testing at T_J = 125 ºC.

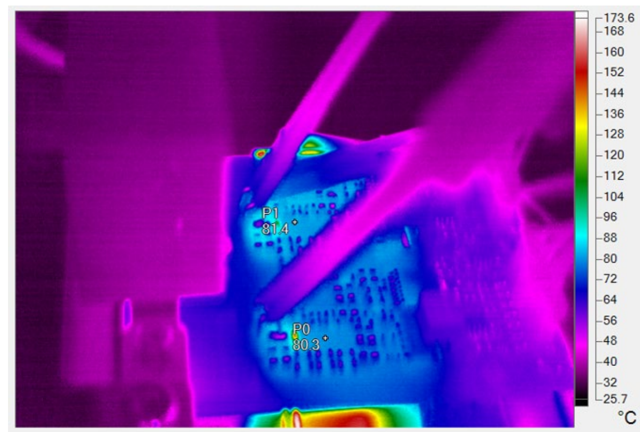

Figure 10 – PCB Secondary-side Thermal Image during HV Testing at T_J = 125 ºC.

9 Measurement Equipment

The following measurement equipment was used for the test(s):

Type	Supplier and Part Number	Identifier
Oscilloscope	Yokogawa DLM5058	LVB_OS_04
Differential Probe	Testec TT-SI9110	HVB_DP_05
Current Probe	PEM CWTUM/06/R, 50mV/A	ATV_CP_09
Current Probe	PEM CWTUM/6/B, 5mV/A	LVB_CP_02
Voltage Supply	Rohde & Schwarz HM 7042-5	LVB_PSU_03
High-Voltage Supply	Iseg HPp20 757 152	HVB_HVS_04
Frequency Generator	Tektronix AFG31000	LVB_SG_03
Thermal Camera	Fluke TiX580	059045

Table 5 – Measurement Equipment.

10 Transformer Specification

10.1 Electrical Diagram of SCALE-iDriver Transformer

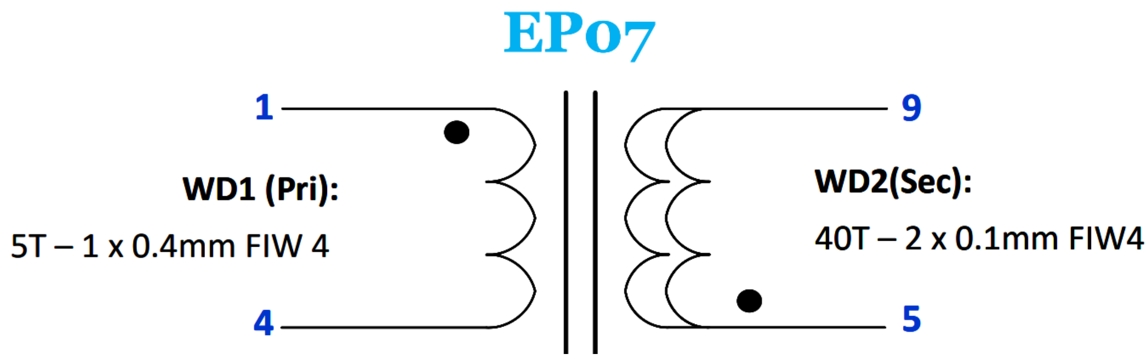

Figure 11 – SCALE-iDriver Transformers (T300 and T301) Electrical Diagram

10.2 Build Diagram of SCALE-iDriver Transformer

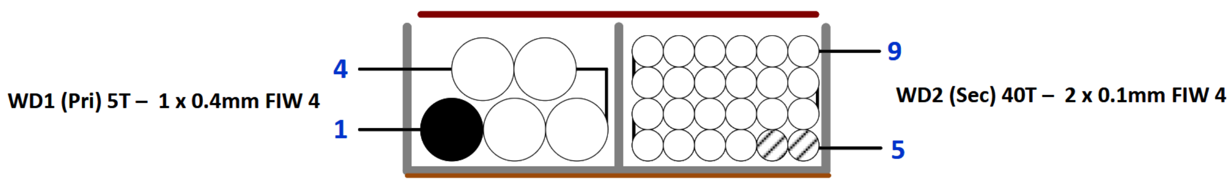

Figure 12 – SCALE-iDriver Transformer (T300 and T301) Build Diagram

10.3 Electrical Specification of SCALE-iDriver Transformer

Parameter	Conditions	Min	Typ	Max	Unit
Power	Output power secondary-side			1	W
Input Voltage VDC	LLC topology	4.75	5.00	5.25	V
Switching frequency	LLC topology	350	380	400	kHz
Duty cycle	LLC topology		50		%
Ns:Np			8		
Rdc	Primary-side			16	mΩ
Rdc	Secondary-side			880	mΩ
Coupling capacitance	Primary-side to secondary-side, Measured at 1 V_{PK-PK}, 400 kHz frequency, between pin 1 to pin 12, with pins 1 - 3 shorted and pins 12 - 8 shorted at 25 °C			5	pF
Primary inductance	Measured at 1 V_{PK-PK}, 400 kHz frequency, between pin 1 to pin 4, with all other Windings open at 25°C	20	28	36	µH
Primary Leakage inductance	Measured at 1 V_{PK-PK}, 400 kHz frequency, between pin 1 to pin 4, with all other Windings shorted	350	400	450	nH

Table 6 – SCALE-iDriver Transformer (T300 and T301) Electrical Specification.

10.4 Materials List of SCALE-iDriver Transformer

Item	Description	Qty	UOM	Material	Manufacturer	UL No.
[1]	Bobbin: EP07	1	PC	Phenolic	MyCoilTech	E150608
[2]	Core: EP07 3C95	2	PCS	N87 (or equivalent)	TDK	N.A.
[3]	WD1 (Pri): 0.4 mm FIW 4, Class F	120	mm	Copper Wire	Elektrisola	E467608
[4]	WD2 (sec): 0.1 mm FIW 4, Class F	1500	mm		Elektrisola	E467608
[6]	3M Polyimide 5413 Amber, width: 0.130in (3.3mm)	100	mm	3M157181 (or equivalent)	3M	E17385

Table 7 – SCALE-iDriver Transformer (T300 and T301) Materials List.

10.5 SCALE-iDriver Transformer

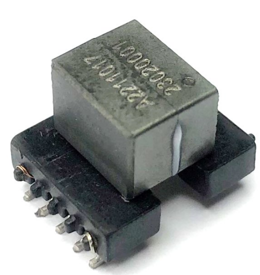

Figure 13 – SCALE-iDriver LLC Transformer (T300 and T301)

11 SCALE-iDriver SIC1182KQ Performance Data

11.1 General Conditions / Remarks

The following points should be considered:

- The test power device is onsemi's NVH4L020N120SC1 SiC MOSFET.
- The voltage class of the power devices is $V_{CE(MAX)}$ = 1200 V and is the absolute maximum rating.
- The allowed peak voltage during turn-off transient shall be $V_{CE(PK)}$ ≤ 1150 V for testing.
- The nominal load current of the power device is I_{NOM} = 60 A with $R_{DS(ON)}$ = 20 mΩ (typical value at 25 °C).
- The measured stray inductance of the entire test setup, including PCB trace and power device pin, during turn-off for the bottom-channel SiC-MOSFET is around $L_{\sigma(BOTTOM)}$ ≈ 98 nH.
- The measured stray inductance of the entire test setup, including PCB trace and power device pin, during turn-off for the top-channel SiC-MOSFET is around $L_{\sigma,top}$ ≈ 96 nH.
- The DC-link voltage is VDC = 800 V
- The primary-side supply voltage comes from a regulated flyback converter controlled by the InnoSwitch which has a nominal value of V_{CC} = 5 V.
- The secondary-side supply voltage of each gate driver ICs comes from an unregulated LLC converter which has a nominal value of $V_{VISO-COM}$ = 20 V.
- The gate driving voltage is set to V_{GE} = +15 V / -5 V (nominal value).
- All high voltage measurements on the power device have been carried out directly on its pins.
- All high voltage data presented in this report uses the secondary side setting (i.e., AROC Chain, Gate Resistor) given in chapter 11.2.

11.2 Secondary Side Gate Driver Settings

To achieve the shown test results within chapters 11.5 and 11.6, components on the secondary side should be adjusted as listed below.

Function	**Designator**	**Value**	**Change Reason**
DUT	Qx00	NVH4L020N120SC1	Power device to be tested
AMC BJT	Qx02	PBSS5140T	BJT for External Active Miller Clamping
$R_{G,OFF}$	Rx10, Rx11	12 Ω	Required for safe turn-off of power device
$R_{G,ON}$	Rx08, Rx19	6.8 Ω	Required for safe turn-on of power device
dv/dt Capacitor	Cx01 … Cx06	1 pF	Required for support of AROC function
R_{SENSE}	R200	11 kΩ	AROC adjustment on top channel power device
C_{SENSE}	C213	10 pF	Required for controlling the effects of the dv/dt capacitor on top channel power device

Table 8 – Summary of Component Temperature in at Different HVDC Input (105°C Ambient).

Note that the configuration listed in Table 8 is only applicable when using NVH4L020N120SC1 as the power device. These settings may not work for other power devices with different part numbers. HV testing should be repeated accordingly to confirm if the new power device will operate within its maximum ratings.

11.3 Equivalent Half-bridge Circuit for High Voltage Testing

Shown in Figure 14 and Figure 15 are the equivalent circuit for turn-on and turn-off measurement of the bottom and top channel, respectively. The snubber capacitor used for all high voltage tests is TDK's B32656S1684K563 (0.68 μF 1.6 kV 10%) film capacitor.

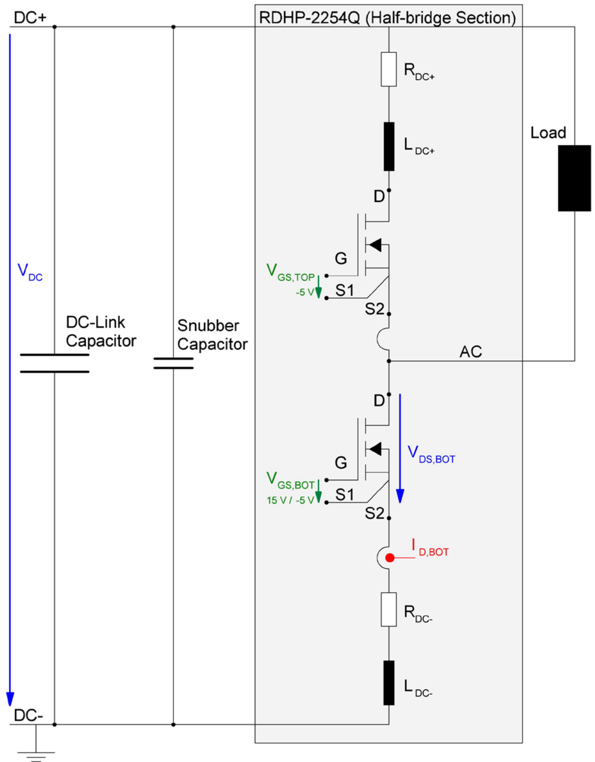

Figure 14 – Equivalent Circuit for Bottom Channel Measurements.

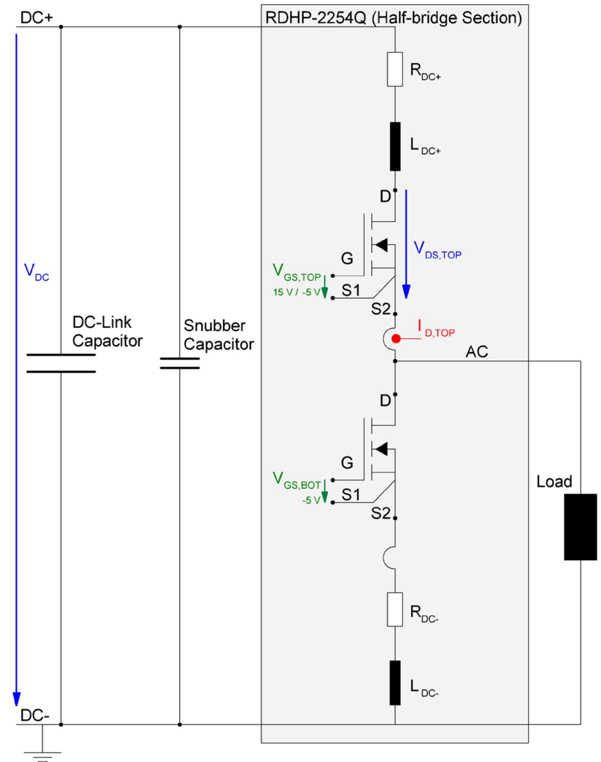

Figure 15 – Equivalent Circuit for Top Channel Measurements.

11.4 Low Voltage Measurements

The following low voltage measurements were carried out at T_A = 25 °C.

11.4.1 Efficiency and Voltage Output of DC/DC Converter of GDU

The secondary-side supply voltage comes from an unregulated LLC converter as shown in Figure 2. Each channel is using an LLC transformer shown in Figure 13 which can deliver up to 1 W of power capacity for each channel. and graphs the efficiency and VISO-COM voltage vs the total output power on the secondary-side. Note that, since this is an unregulated power supply, the VISO-COM voltage regulation may vary across boards. This will depend on the tolerances of the transformer. Nevertheless, VISO-COM voltage regulation shall be within 18 V to 21 V with a nominal value of 20 V.

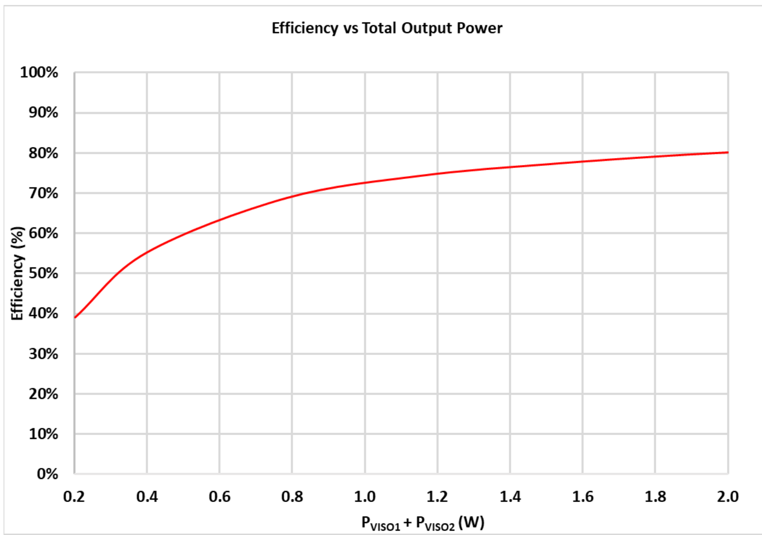

Figure 16 – Efficiency vs Total Output Power of LLC Converter.

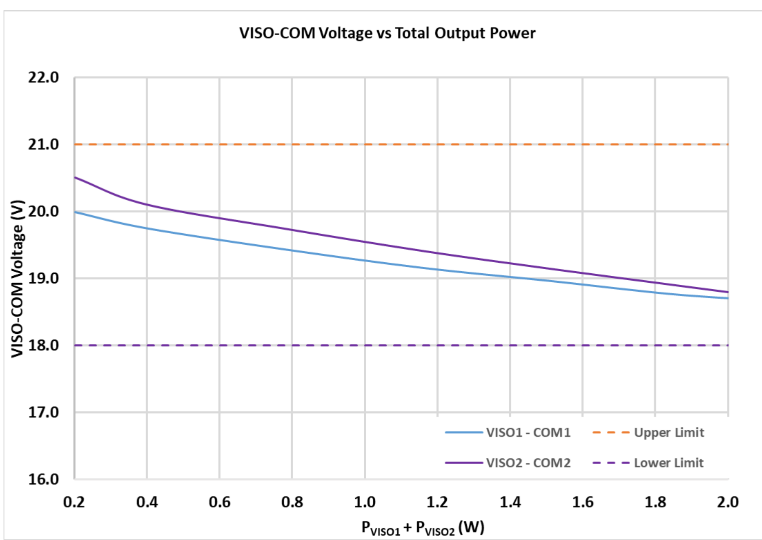

Figure 17 – VISO-COM Voltage vs Total Output Power.

11.4.2 PWM Input Interlocking

The waveform shown in Figure 18 features the interlocking function of RDHP-2301Q. The corresponding oscilloscope setting is listed in Table 9.

Oscilloscope Channel	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Signal Name	IN_{BOT}	n.a.	$V_{GS,BOT}$	n.a.	$V_{GS,TOP}$	n.a.		IN_{TOP}
Resolution	10 V / div.		10 V / div.		10 V / div.			10 V / div.
Time Base	10 μs / div.							

Table 9 – Oscilloscope Setting for Interlocking.

Each channel was fed with 20 kHz square wave that are 90° phase shifted from each other. When both input signals are 5 V logic high at the same time, both top and bottom gate signals are turned-off. This is to prevent cross-conduction between power devices.

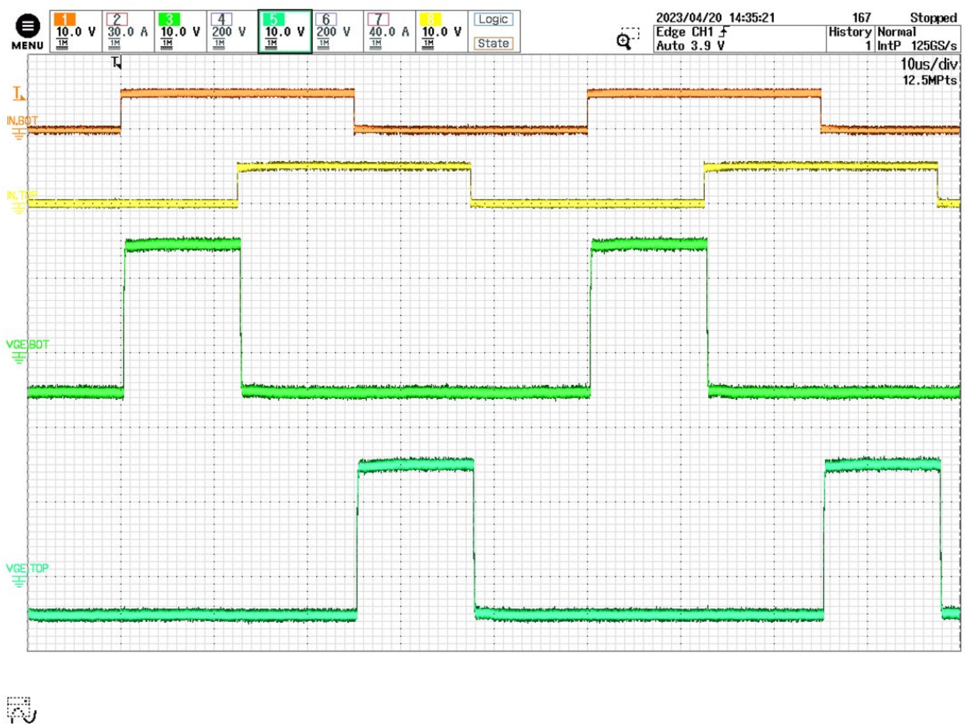

Figure 18 – PWM Interlocking Function.

11.5 High Voltage Double Pulse Tests of Half-Bridge

The data shown in the following sub-chapters are achievable using the secondary-side setting described in chapter 11.2.

The following signals were measured during the turn-on and turn-off measurements.

Oscilloscope Channel	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Signal Name	IN_X	$I_{D,X}$	$V_{GS,X}$	$V_{DS,X}$	N/A			
Resolution	10 V / div.	variable	5 V / div.	200 V / div.				
Time Base	100 ns / div.							

Table 10 – Oscilloscope Setting for Turn-on and Turn-off Measurements.

11.5.1 Testing at T_J = 25 °C

The following measurements were carried out with SiC MOSFETs at T_J = 25 °C using test set up shown in Figure 6.

11.5.1.1 Bottom Channel Turn-on Measurements

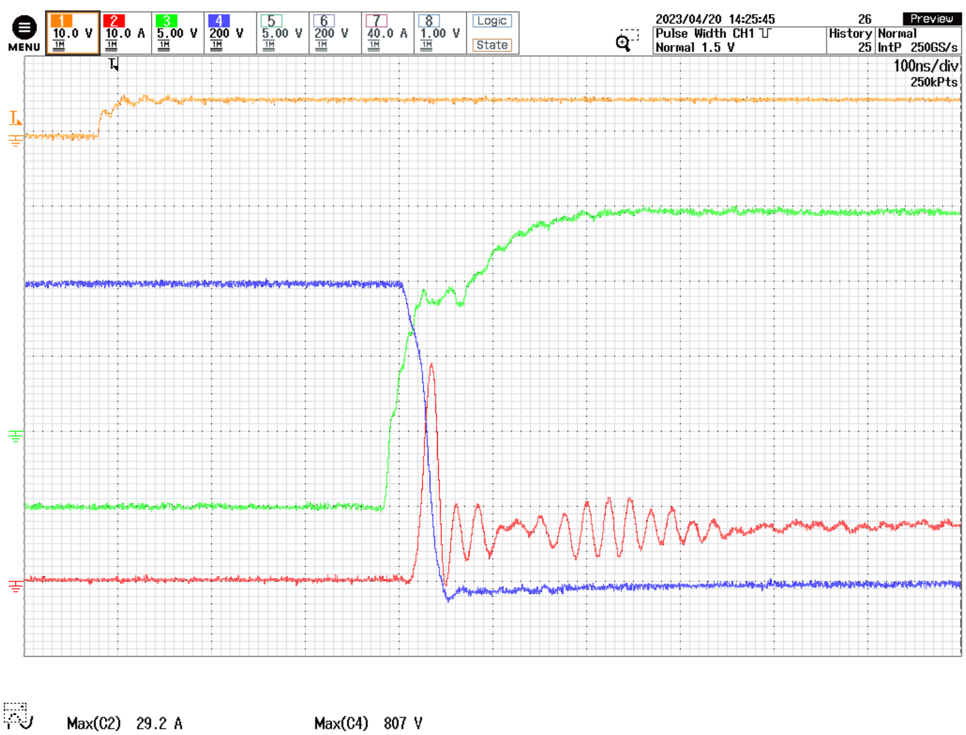

Figure 19 – Bottom Channel Turn-on, $I_{D,ON}$ = 0.1 · I_{NOM} at T_J = 25 °C.

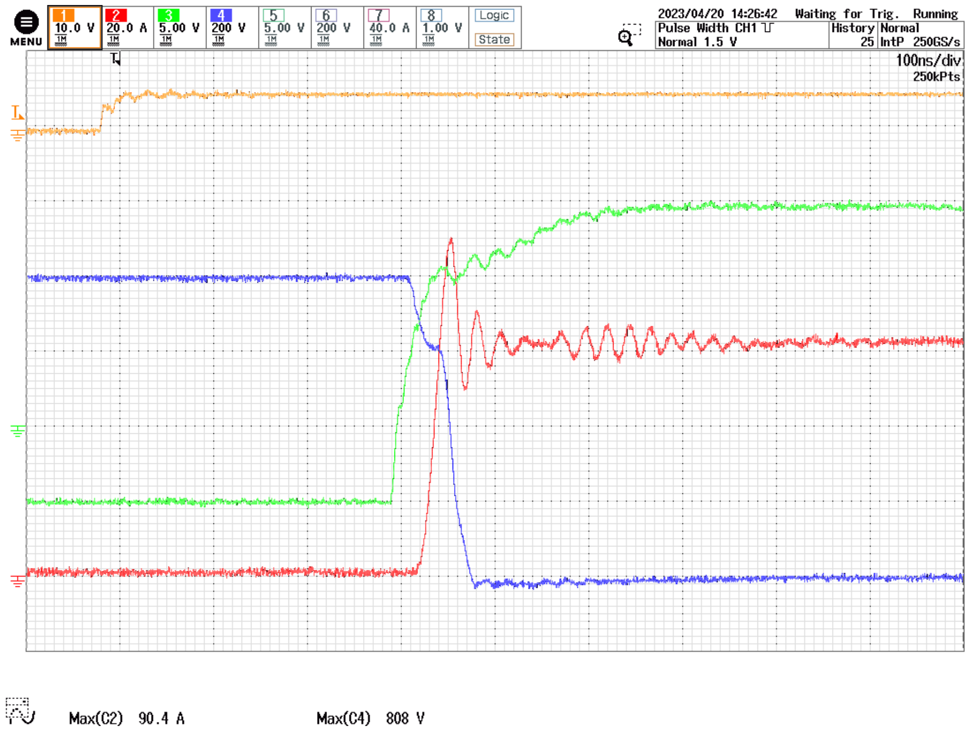

Figure 20 – Bottom Channel Turn-on, $I_{D,\,ON} = 1 \cdot I_{NOM}$ at $T_J = 25$ °C.

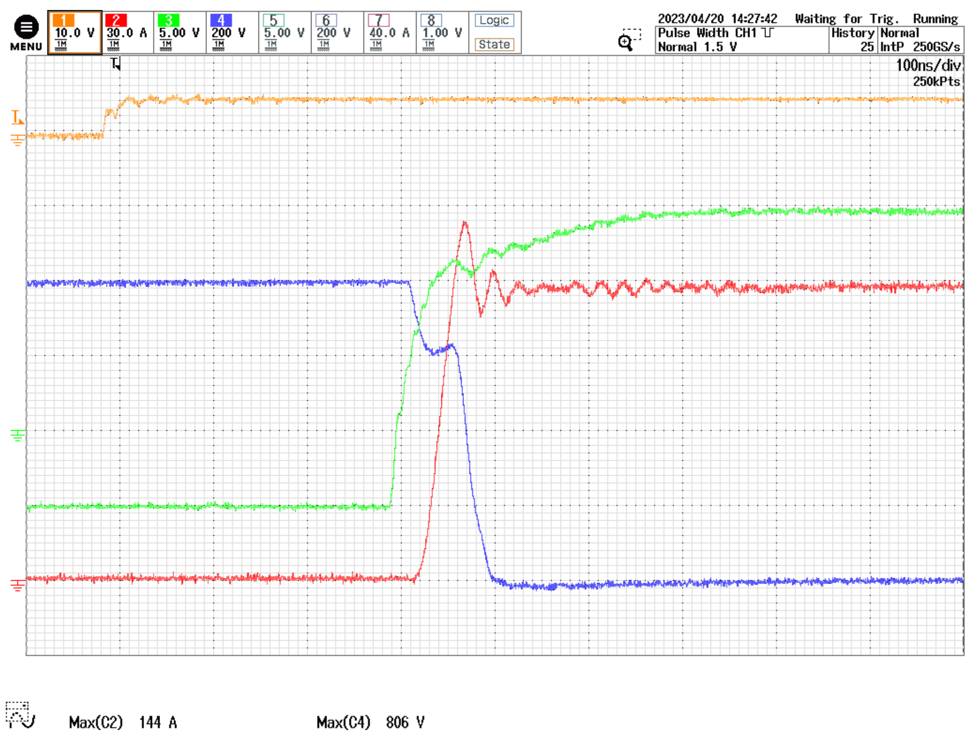

Figure 21 – Bottom Channel Turn-on, $I_{D,\,ON} = 2 \cdot I_{NOM}$ at $T_J = 25$ °C.

11.5.1.2 Bottom Channel Turn-off Measurements

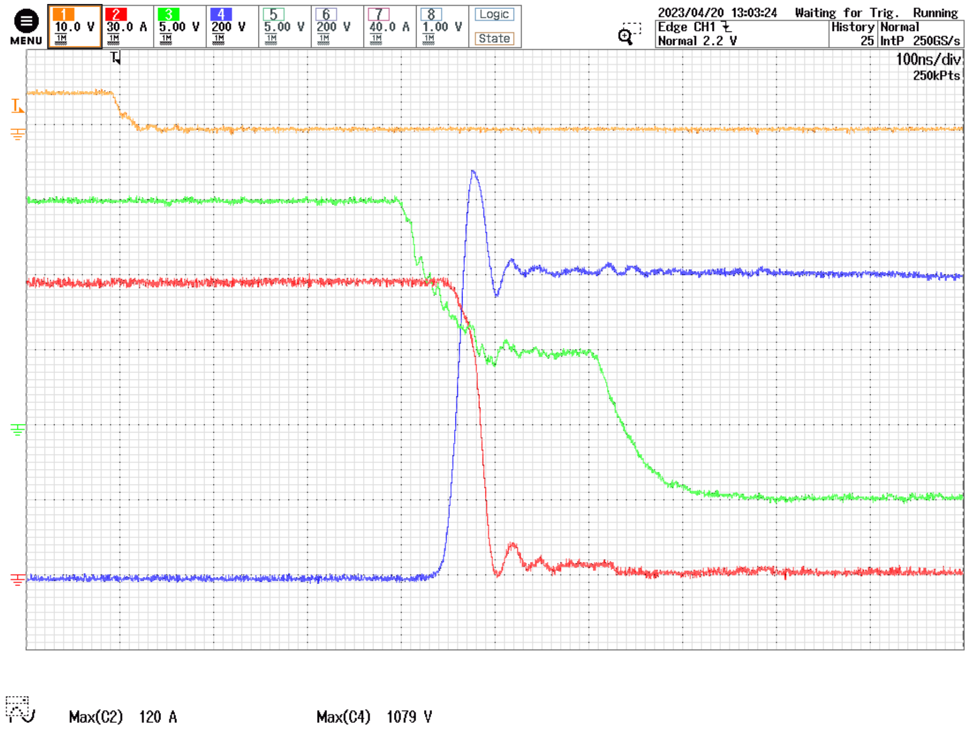

Figure 22 – Bottom Channel Turn-off, $I_{D,\ OFF} = 2 \cdot I_{NOM}$ at $T_J = 25$ °C.

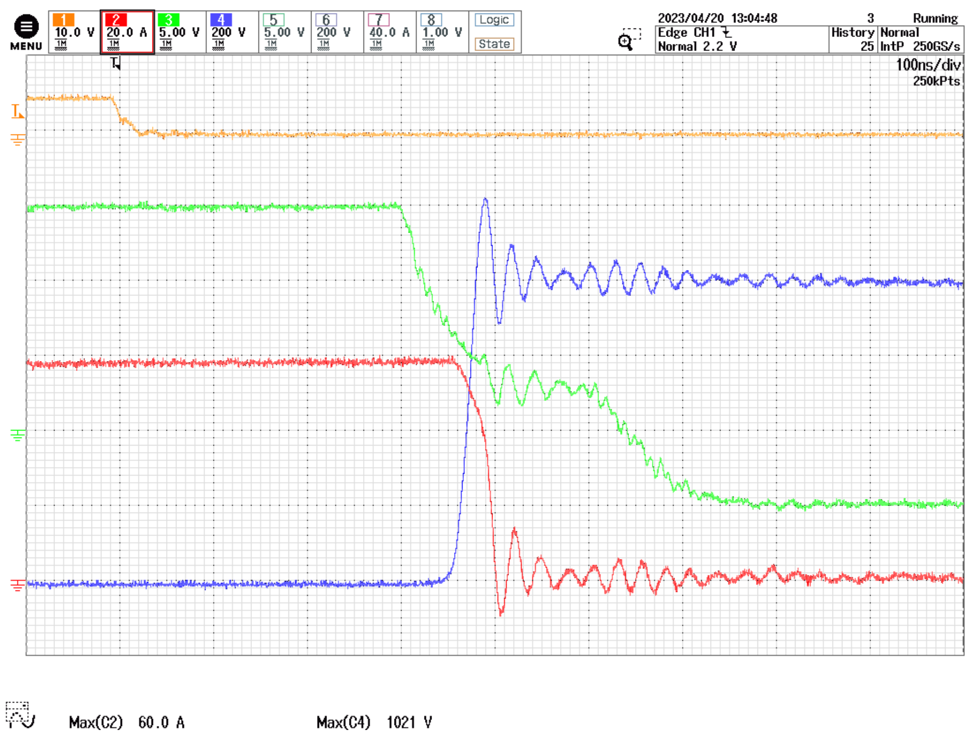

Figure 23 – Bottom Channel Turn-off, $I_{D,\ OFF} = 1 \cdot I_{NOM}$ at $T_J = 25$ °C.

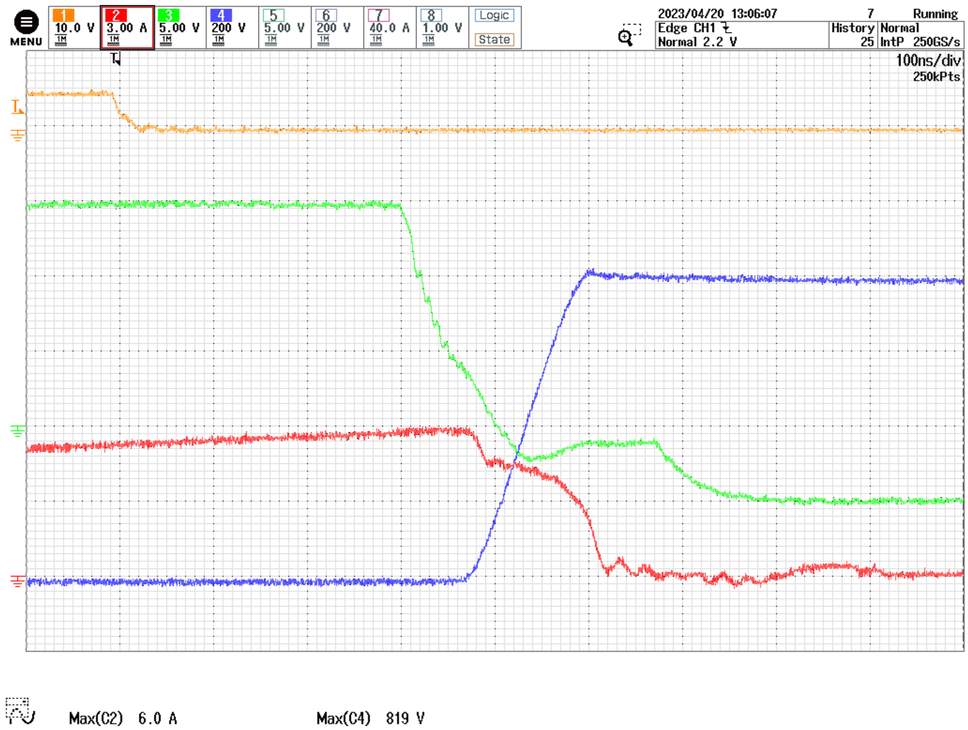

Figure 24 – Bottom Channel Turn-off, $I_{D,\ OFF}$ = 0.1 · I_{NOM} at T_J = 25 °C.

11.5.1.3 Top Channel Turn-on Measurements

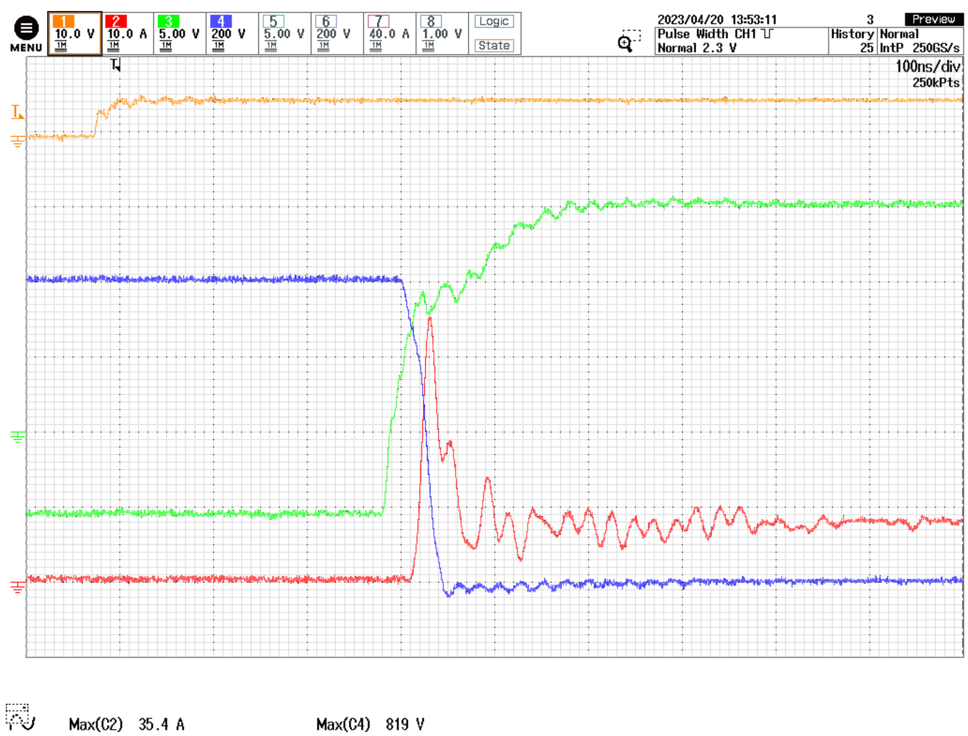

Figure 25 – Top Channel Turn-on, $I_{D,\ ON}$ = 0.1 · I_{NOM} at T_J = 25 °C.

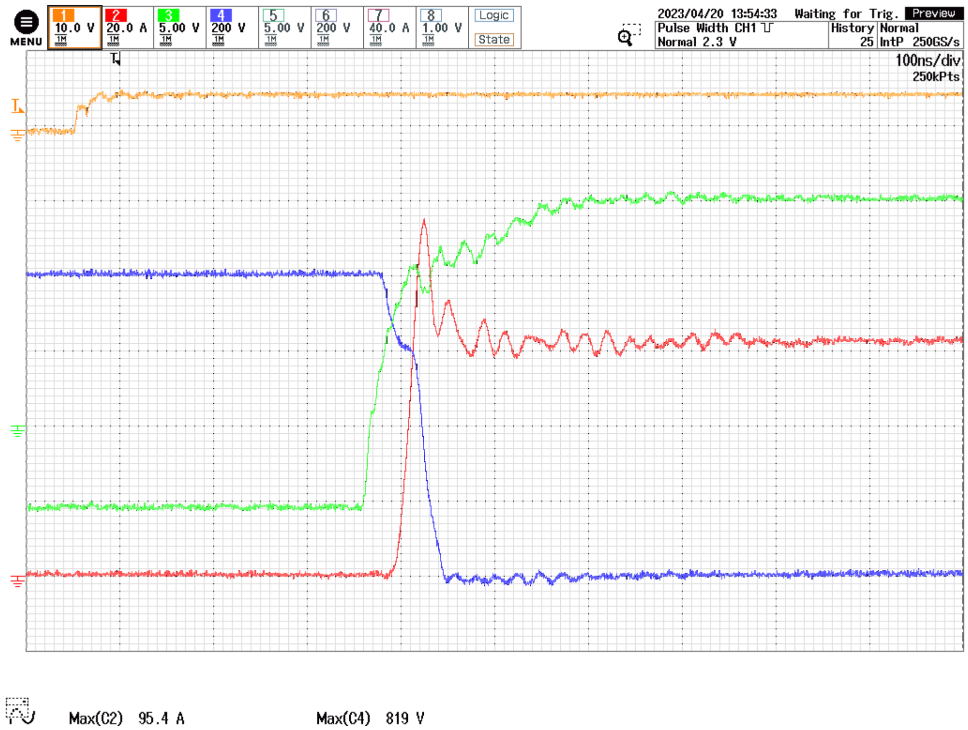

Figure 26 – Top Channel Turn-on, $I_{D,\,ON}$ = 1 · I_{NOM} at T_J = 25 °C.

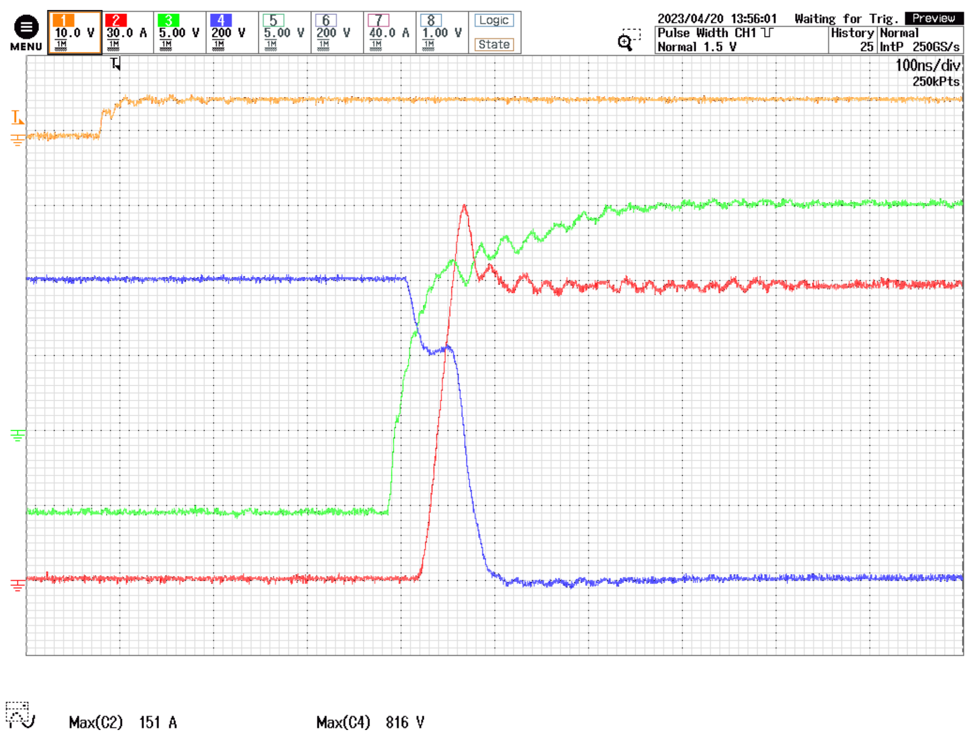

Figure 27 – Top Channel Turn-on, $I_{D,\,ON}$ = 2 · I_{NOM} at T_J = 25 °C.

11.5.1.4 Top Channel Turn-off Measurements

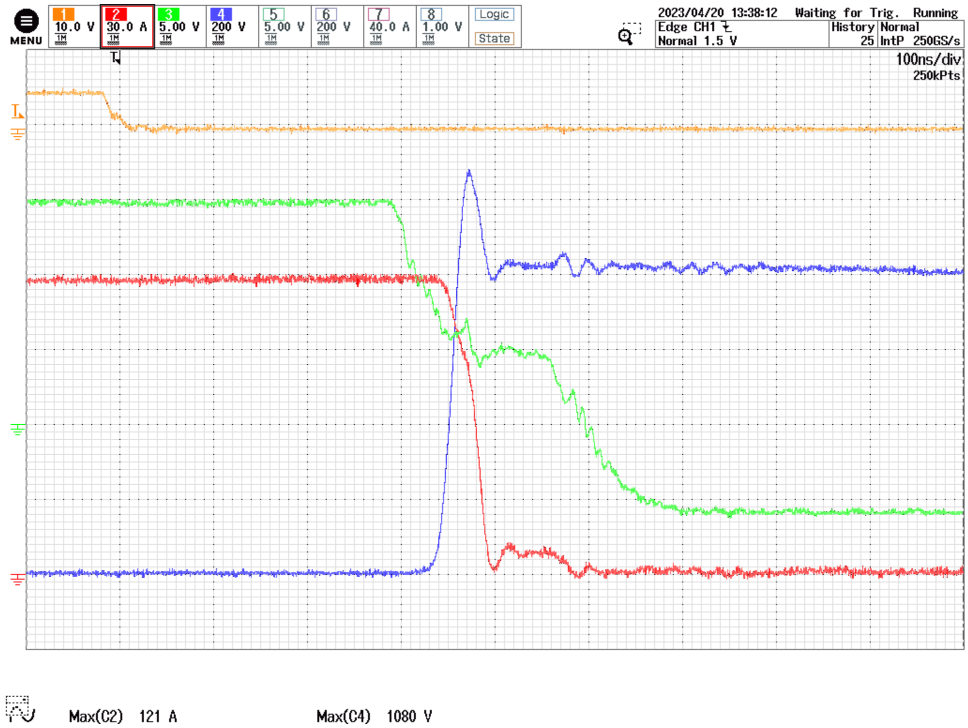

Figure 28 – Top Channel Turn-off, $I_{D,\,OFF} = 2 \cdot I_{NOM}$ at $T_J = 25$ °C.

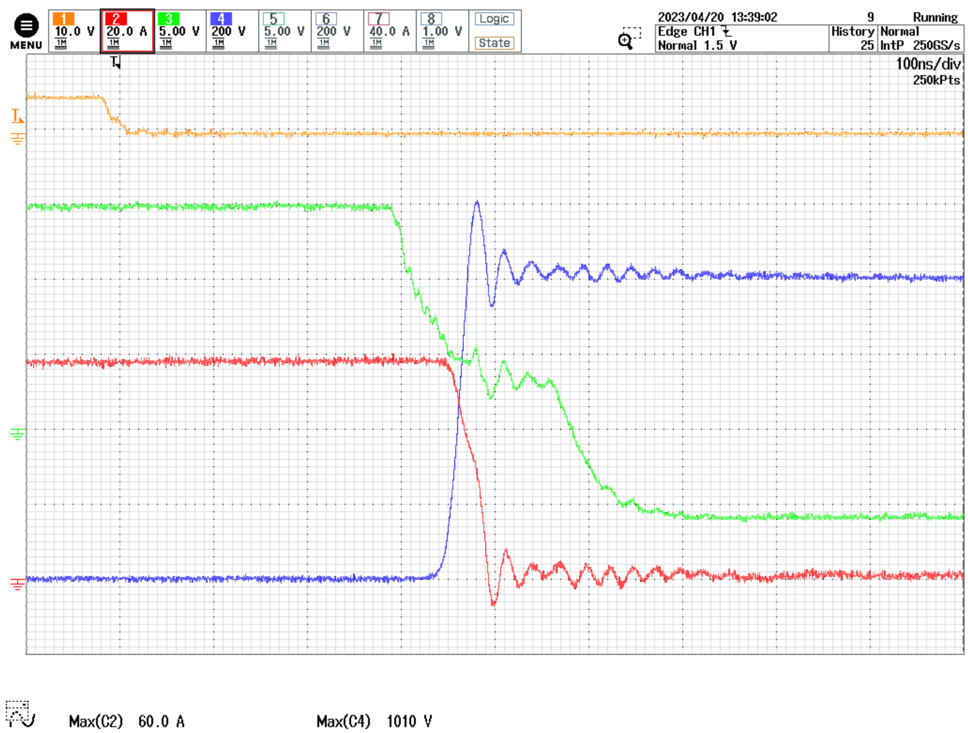

Figure 29 – Top Channel Turn-off, $I_{D,\,OFF} = 1 \cdot I_{NOM}$ at $T_J = 25$ °C.

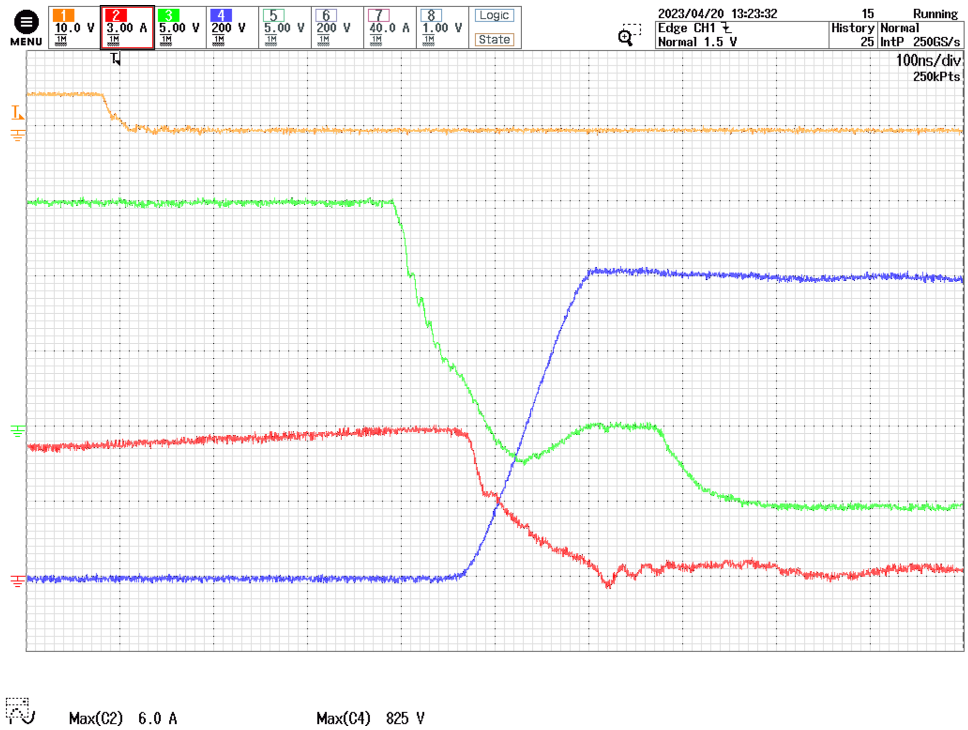

Figure 30 – Top Channel Turn-off, $I_{D,\,OFF} = 0.1 \cdot I_{NOM}$ at T_J = 25 °C.

11.5.2 Testing at T_J = 125 °C

The following measurements were carried out with SiC MOSFETs at T_J = 125 °C using test set up shown in Figure 8.

These signals were measured during the turn-on and turn-off measurements.

Oscilloscope Channel	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Signal Name	IN_x	$I_{D,x}$	$V_{GS,x}$	$V_{DS,x}$	N/A			
Resolution	10 V / div.	variable	5 V / div.	200 V / div.				
Time Base	100 ns / div.							

Table 11 – Oscilloscope Setting for Turn-on and Turn-off Measurements.

11.5.2.1 Bottom Channel Turn-on Measurements

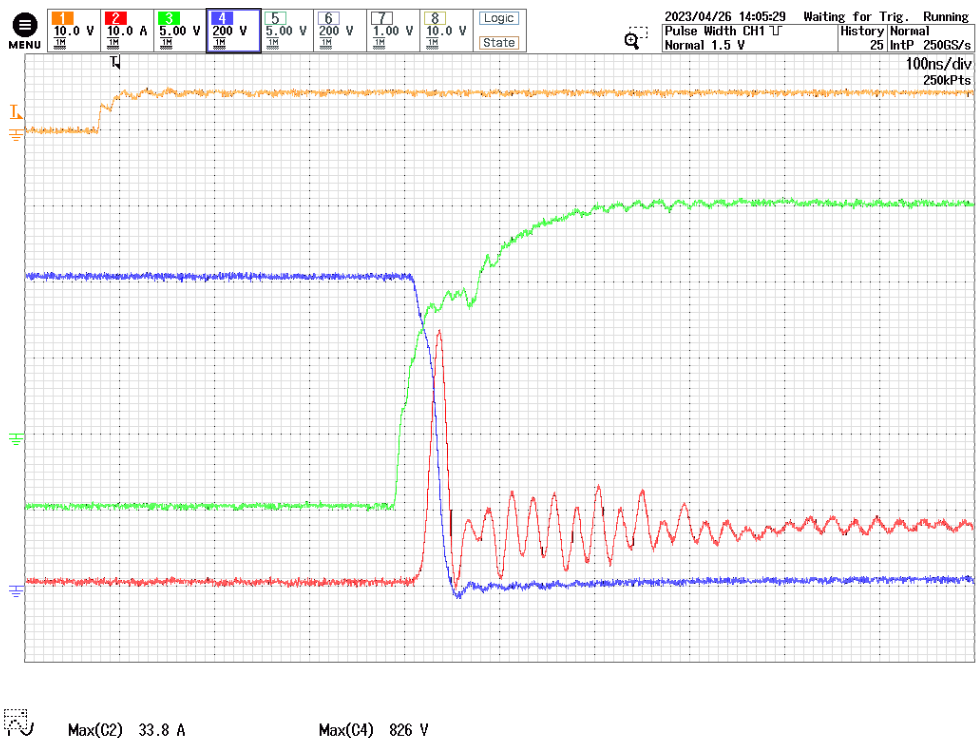

Figure 31 – Bottom Channel Turn-on, $I_{D,\,ON} = 0.1 \cdot I_{NOM}$ at T_J = 125 °C.

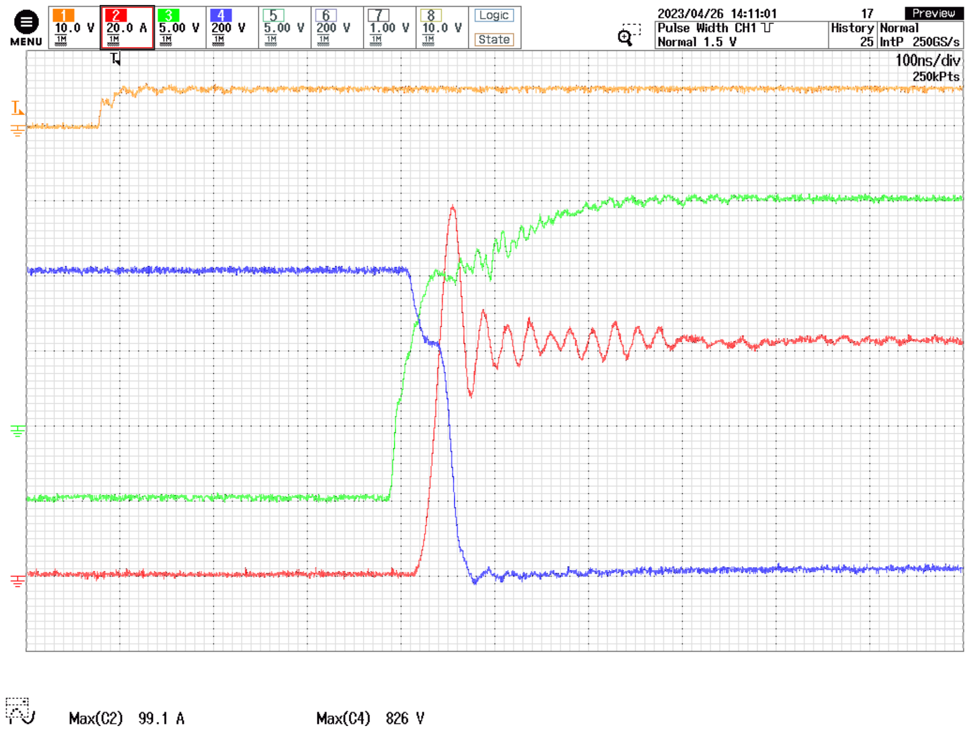

Figure 32 – Bottom Channel Turn-on, $I_{D,\,ON} = 1 \cdot I_{NOM}$ at T_J = 125 °C.

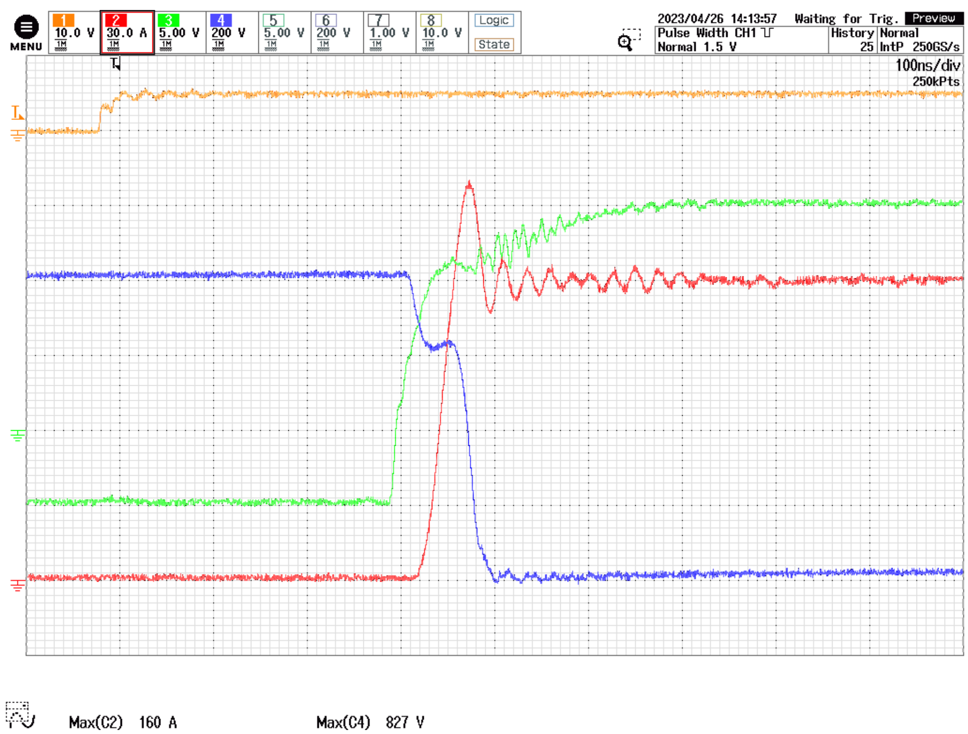

Figure 33 – Bottom Channel Turn-on, $I_{D,\,ON} = 2 \cdot I_{NOM}$ at T_j = 125 °C.

11.5.2.2 Bottom Channel Turn-off Measurements

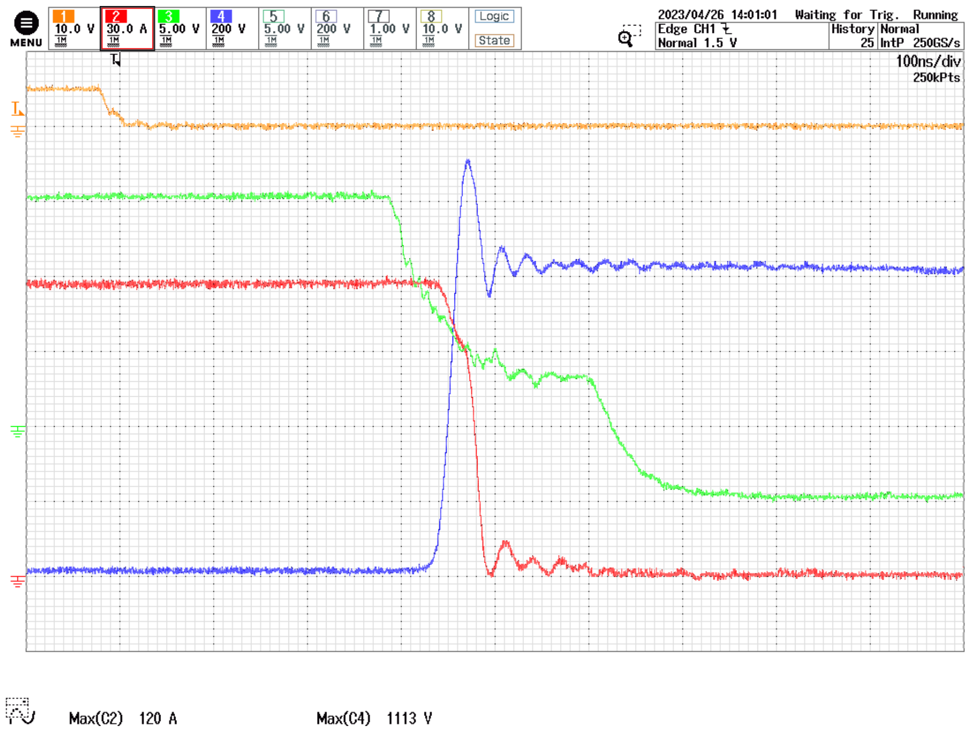

Figure 34 – Bottom Channel Turn-off, $I_{D,\,OFF} = 2 \cdot I_{NOM}$ at T_J = 125 °C.

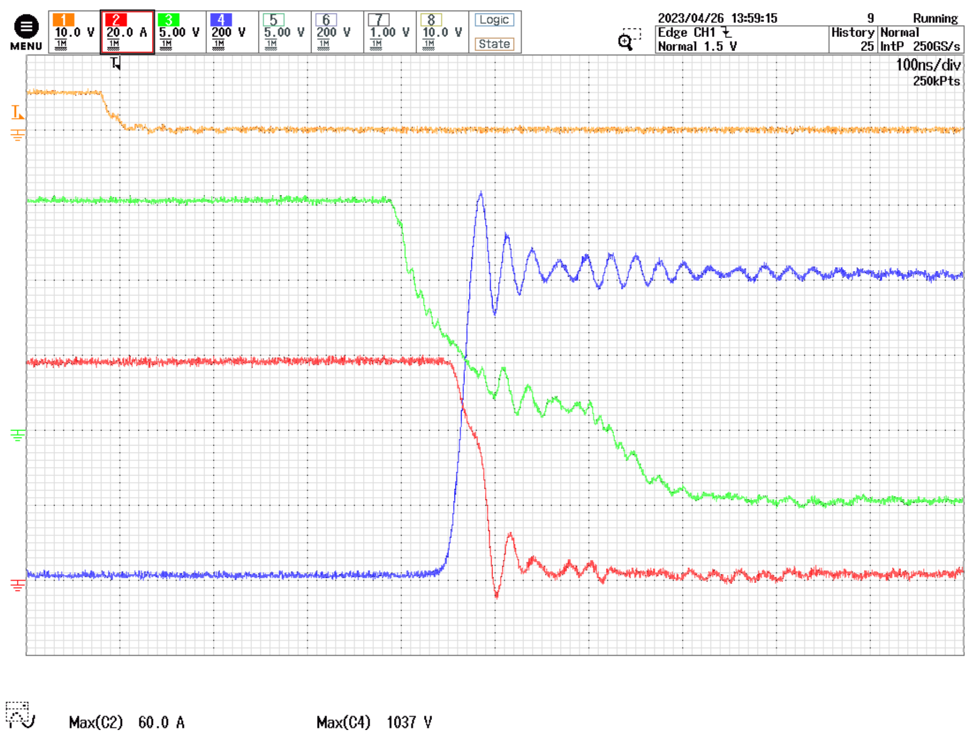

Figure 35 – Bottom Channel Turn-off, $I_{D,\,OFF} = 1 \cdot I_{NOM}$ at T_J = 125 °C.

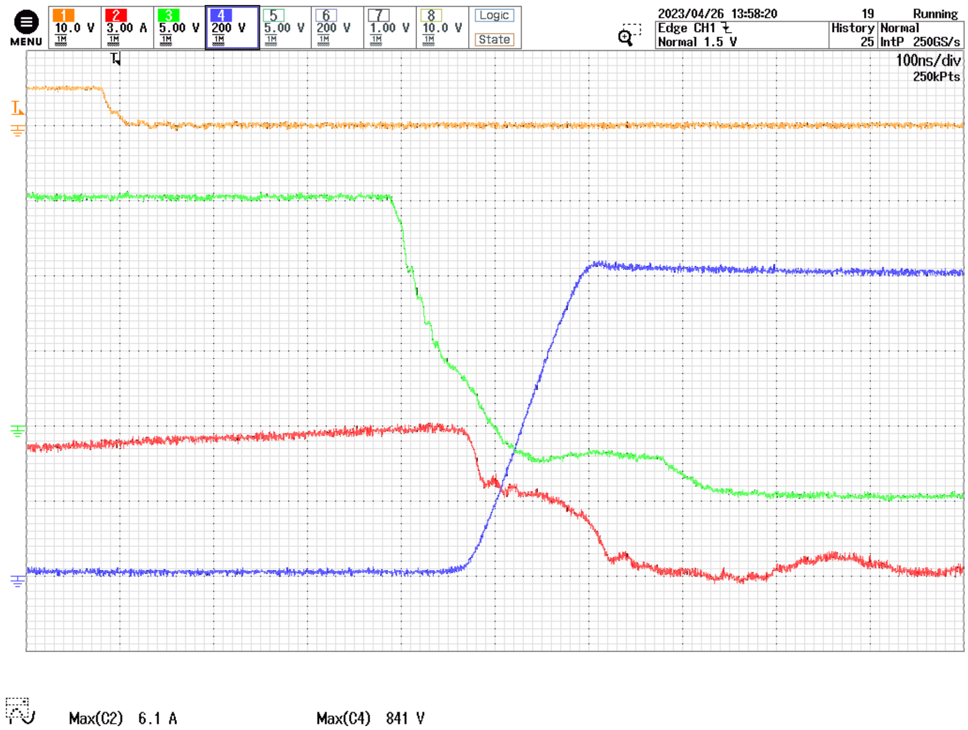

Figure 36 – Bottom Channel Turn-off, $I_{D,\,OFF} = 0.1 \cdot I_{NOM}$ at $T_J = 125$ °C.

11.5.2.3 Top Channel Turn-on Measurements

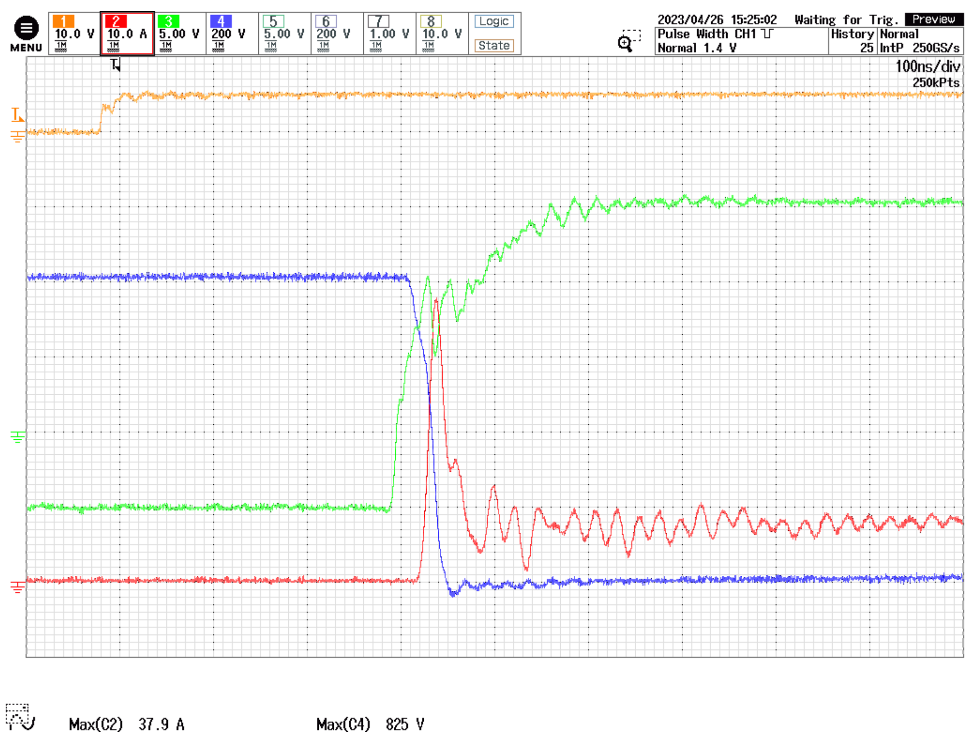

Figure 37 – Top Channel Turn-on, $I_{D,\,ON} = 0.1 \cdot I_{NOM}$ at $T_J = 125$ °C.

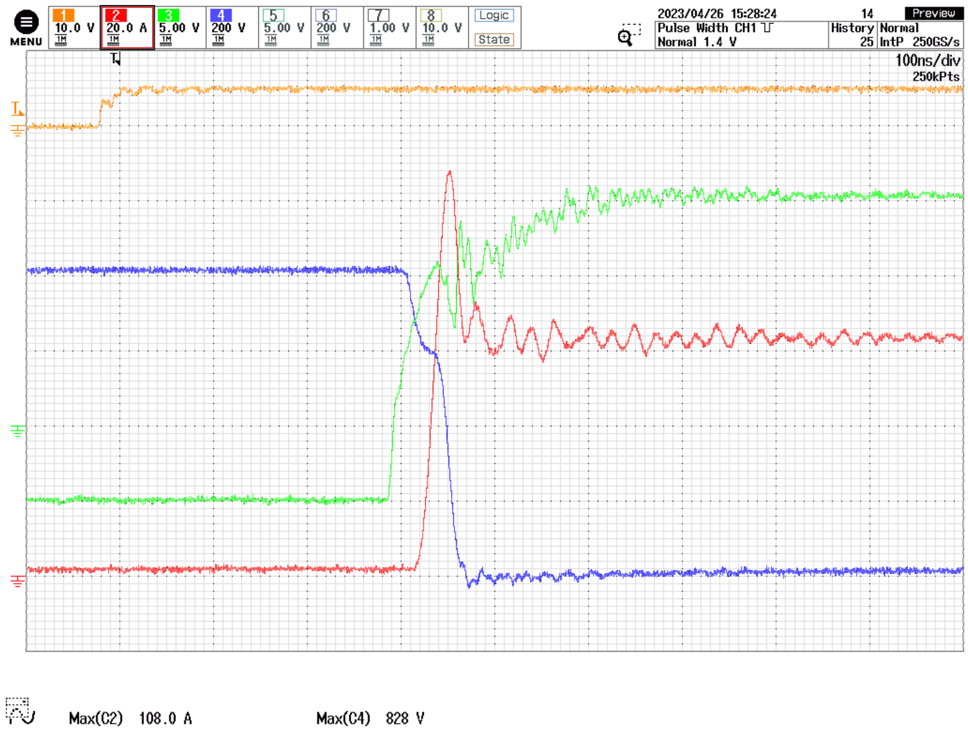

Figure 38 – Top Channel Turn-on, $I_{D,\,ON}$ = 1 · I_{NOM} at T_J = 125 °C.

Figure 39 – Top Channel Turn-on, $I_{D,\,ON}$ = 2 · I_{nom} at T_J = 125 °C.

11.5.2.4 Top Channel Turn-off Measurements

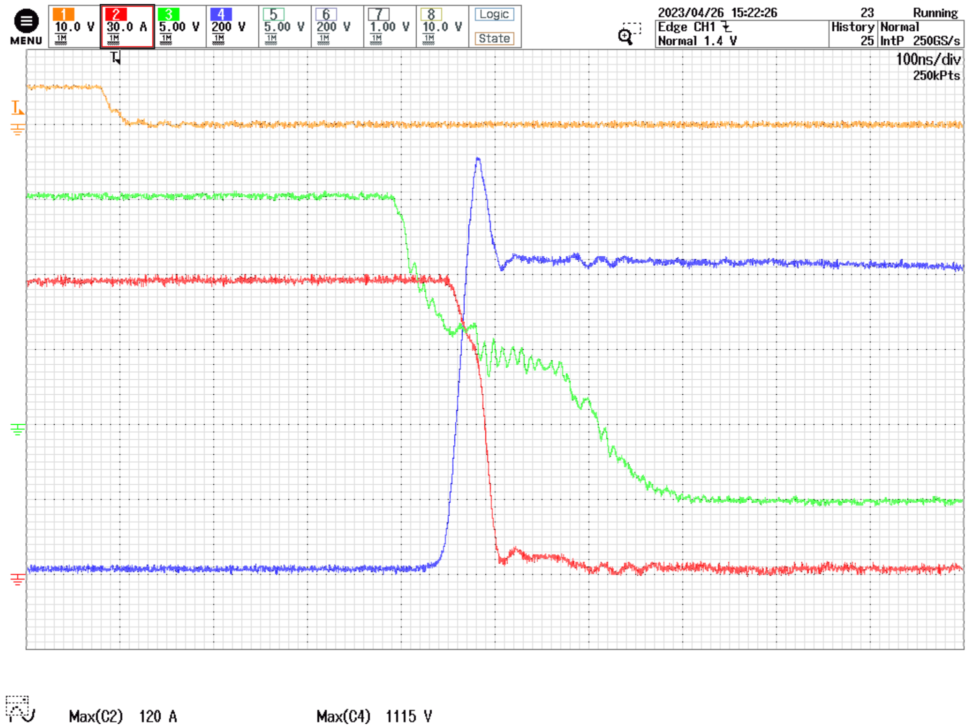

Figure 40 – Top Channel Turn-off, $I_{D,\,OFF} = 2 \cdot I_{NOM}$ at T_J = 125 °C.

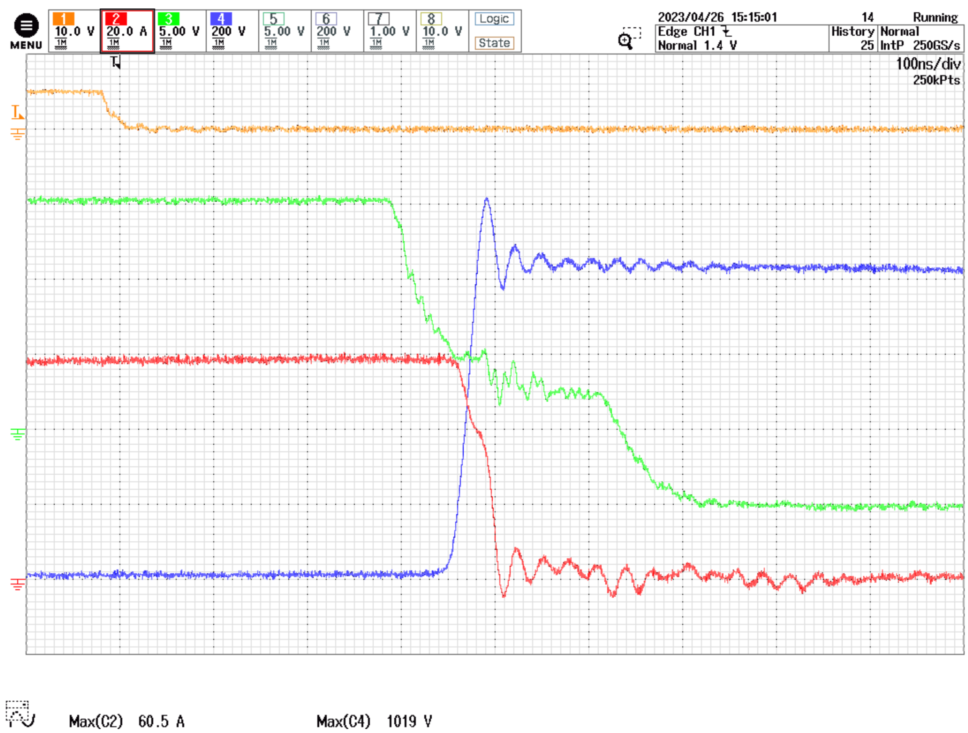

Figure 41 – Top Channel Turn-off, $I_{D,\,OFF} = 1 \cdot I_{NOM}$ at T_J = 125 °C.

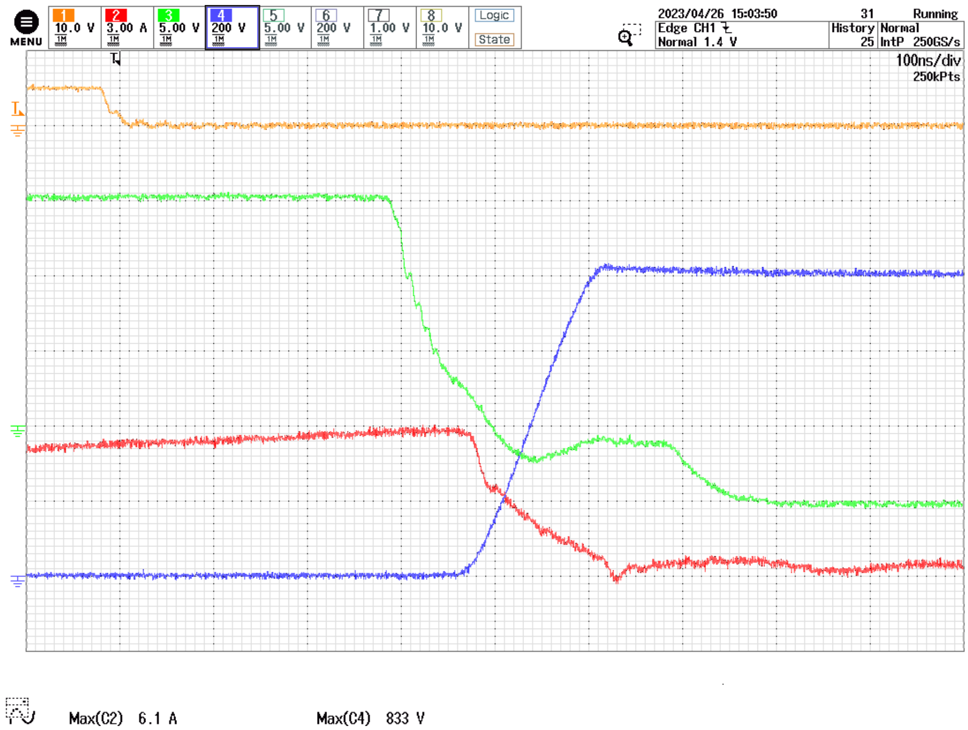

Figure 42 – Top Channel Turn-off, $I_{D,\ OFF}$ = 0.1 · I_{NOM} at T_J = 125 °C.

11.6 High Voltage Short-circuit Tests of Half-Bridge

The data shown in the following sub-chapters are achievable using the secondary side setting described in chapter 11.2.

The following signals were measured during short-circuit measurements.

Oscilloscope Channel	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Signal Name	IN_x	$I_{D,x}$	$V_{GS,x}$	$V_{DS,x}$	N/A		SO	N/A
Resolution	10 V / div.	200 A / div.	5 V / div.	200 V / div.			10 V / div.	
Time Base	500 ns / div.							

Table 12 – Oscilloscope Setting for Short-Circuit Measurements.

11.6.1 Testing at T_J= 25 °C

The following measurements were carried out with SiC MOSFETs at T_J = 25°C using test set up shown in Figure 7.

11.6.1.1 Short-Circuit Measurements

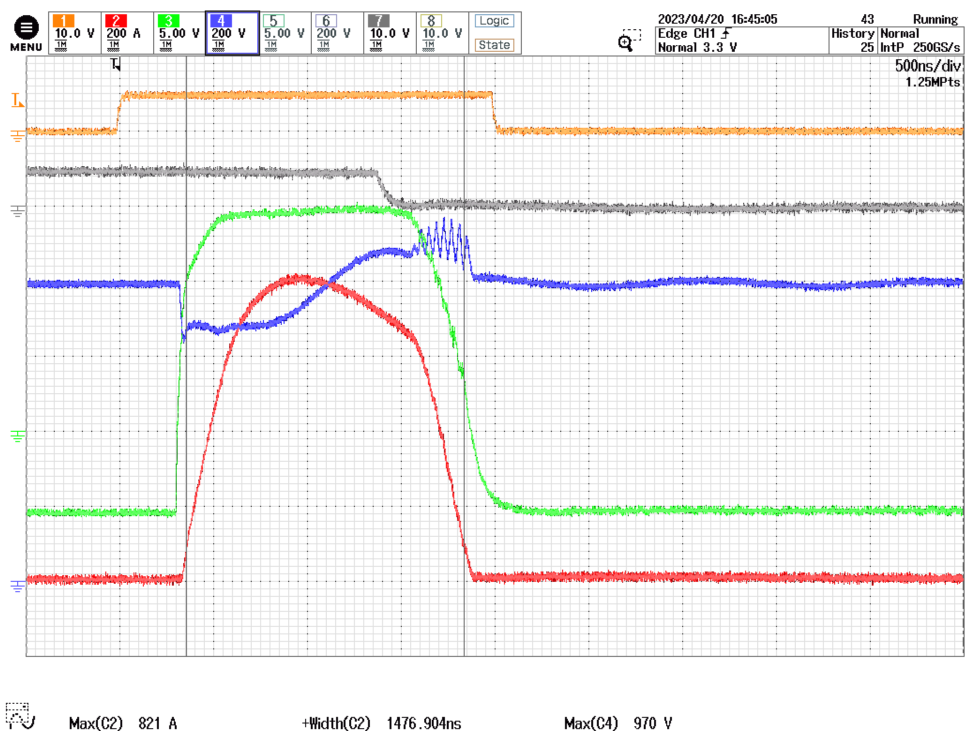

Figure 43 – Bottom Channel Short-Circuit Response at T_J = 25°C, measured t_{SC} = 1.476 µs.

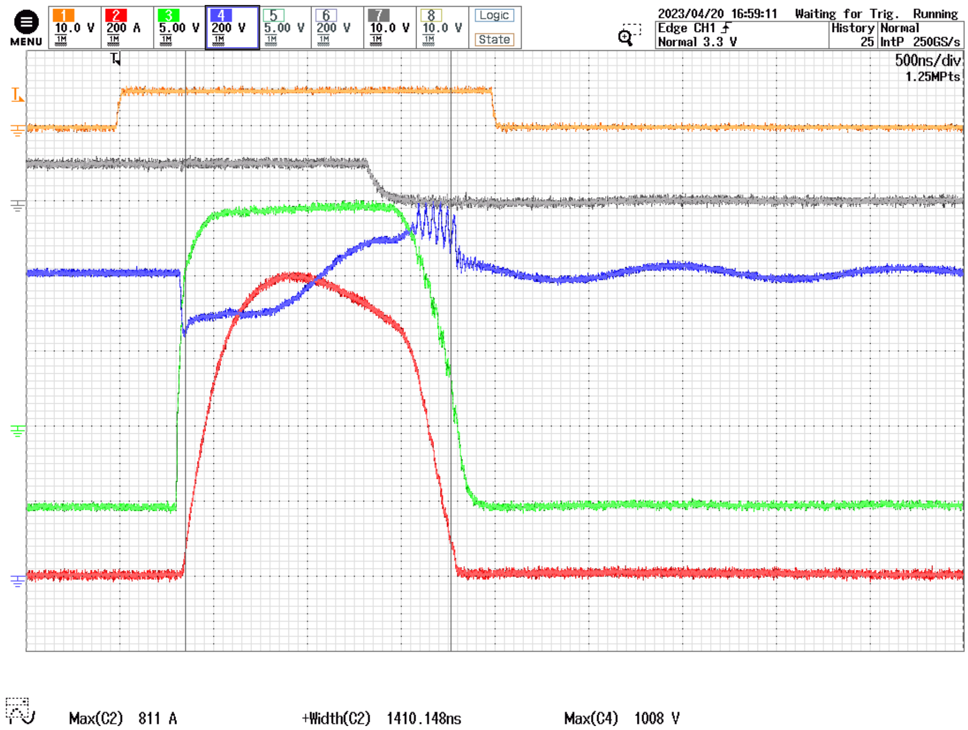

Figure 44 – Top Channel Short-circuit Response at T_J = 25 °C, measured t_{SC} = 1.410 μs.

11.6.2 Testing at T_J = 125 °C

The following measurements were carried out with SiC MOSFETs at T_J = 125 °C using test set up shown in Figure 8 with short-circuit simulation shown in Figure 7.

11.6.2.1 Short-circuit Measurements

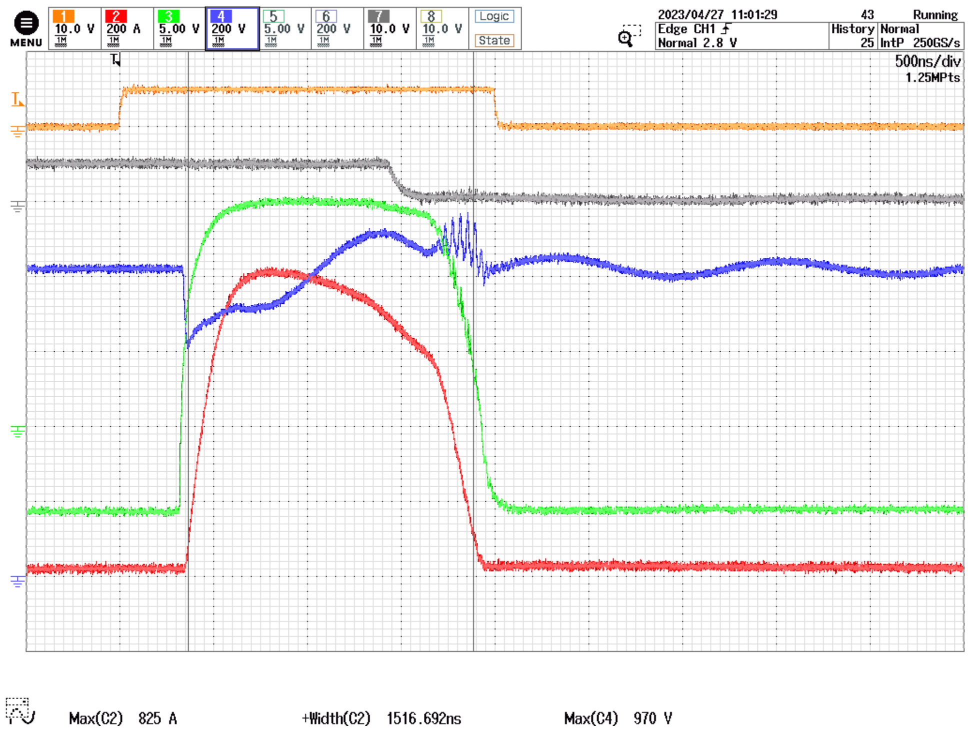

Figure 45 – Bottom Channel Short-circuit Response at T_J = 125 °C, measured t_{SC} = 1.516 μs.

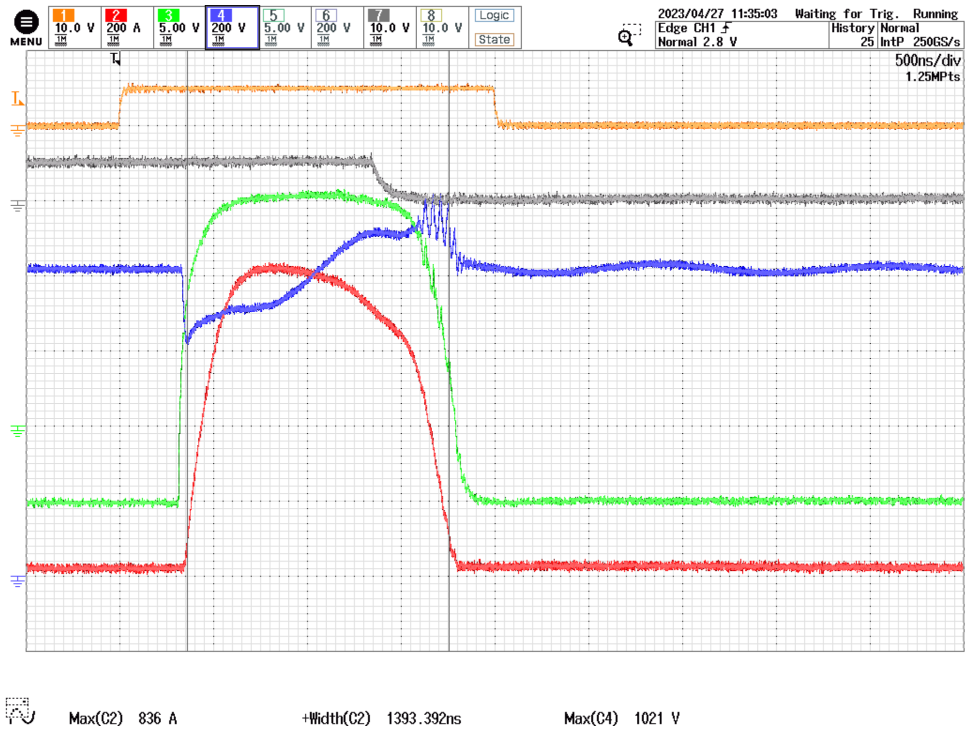

Figure 46 – Top Channel Short-circuit Response at T_J = 125 °C, measured t_{SC} = 1.393 μs.

12 Revision History

Date	Author	Revision	Description and changes	Approved
13-Nov-23	CO	1.0	Initial Release.	Apps & Mktg

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