

Design Example Report

Title	3 W Wide Range Flyback Power Supply using LNK304P					
Specification	Input: 57 VAC - 580 VAC; Output: 12 V, 250 mA					
Application	Utility Meter					
Author	Power Integrations Applications					
Document Number	DER-58					
Date	May 4, 2005					
Revision	1.0					

Summary and Features

- StackFETTM flyback topology delivers full load over extremely wide input AC voltage range
- LinkSwitch-TN feedback simplifies non-isolated voltage regulation 2 resistors precisely set the output voltage
- E-SHIELD[™] Transformer Construction for reduced common-mode EMI (>10dB margin)
- 66kHz Switching Frequency with jitter to reduce conducted EMI
- Simple ON/OFF controller no feedback compensation required
- Auto-restart function for automatic and self-resetting open-loop, overload and short-circuit protection
- Built-in hysteretic thermal shutdown at 135 °C
- EcoSmart for extremely low standby power consumption <200 mW at 265 VAC

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at <u>www.powerint.com</u>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.



1 Introduction

This document is an engineering report describing a wide-range non-isolated StackFET® Flyback converter employing the LNK304P.

The document contains the power supply specification, schematic, bill-of-materials, transformer documentation, printed circuit layout, and performance data.



Figure 1 – Populated Circuit Board Photograph.



2 Power Supply Specification

Description	Symbol	Min	Тур	Мах	Units	Comment
Input						
Voltage	V _{IN}	57		580	VAC	2 Wire – no P.E.
Frequency	f _{LINE}	47	50/60	64	Hz	
No-load Input Power (240 VAC)				0.2	W	
Output						
Output Voltage	V _{OUT}		12		V	± 5%
Output Ripple Voltage	VRIPPLE				mV	20 MHz Bandwidth
Output Current	Ι _{ουτ}			0.25	Α	
Total Output Power						
Continuous Output Power	Pout			3	W	
Efficiency	η	45			%	Measured at P _{OUT} (3 W), 25 °C
Environmental						
Conducted EMI		Mee	ts CISPR2	2B / EN55	022B	
Safety			Class I (no	on-Isolated	1)	
Ambient Temperature	T _{AMB}	0		60	°C	Free convection, sea level



3 Schematic







4 Circuit Description

RF1 is a fusible link resistor, which limits inrush current through the full-bridge rectifier comprised of D1 to D8. This resistor also complies with safety agency requirements to blow open in the event of a catastrophic failure in the power supply.

AC voltage is rectified through the full-bridge rectifier stage and filtered to produce a DC voltage across the series stacked high voltage electrolytic capacitors C1-C4. R1, R2 and R3, R4 help maintain voltage equalization across the series connected capacitors C1, C2 and C3, C4 respectively. L1, C1-C4 forms an input pi filter to reduce components of the switching frequency and its harmonics on the input line.

The rectified high voltage DC is applied to the transformer (T1) primary. The other end of the transformer primary winding is connected to a high-voltage (600V) MOSFET (Q1) that is cascode connected to the Drain of the LinkSwitch-TN Switch (U1). In this configuration the effective Drain-Source voltage rating of the primary is 1300Vpk.

D9-D11 clamps the maximum drain-source voltage across the LinkSwitch-TN (U1) to below 600V. D14 ensures that the maximum gate-source voltage of Q1 does not exceed 15V. R5 and R6 provide bias to enhance the gate of Q1 when its source is switched low by the drain of U1.

D12, D13 and R8 clamp the leakage inductance spike to limit the effective VDS (voltage across Q1 and U1) to about 980Vpk at high line (580VAC) input. C5 is the VCC storage capacitor for U1; this capacitor is charged to 5.8V from the internal high voltage current source, U1 derives its bias from this capacitor.

D15 and C7 rectify and filter the AC waveform produced from the transformer secondary winding to produce the desired DC voltage level. R10 and R11 form a potential divider that controls the output voltage. The midpoint of this divider is connected to the EN pin of U1 that is internally set at 1.63VDC. The simple ON/OFF controller integrated in the LinkSwitch-TN series switches the internal 700V MOSFET at 66kHz to maintain the output voltage set point. C8 is added across R11 to increase noise immunity in the event of transients caused by the load.

The transformer was wound with shields to counteract common-mode displacement currents generated by the windings in the transformer ($\mathsf{ESHIELD}^\mathsf{TM}$). This technique helps reduce conducted EMI and the burden on the input EMI filter. The primary winding was also wound with a Z-winding technique to reduce its self-capacitance and switching losses in the converter.



5 PCB Layout



Figure 3 – Printed Circuit Layout.



6 Bill of Materials

ltem	Qty	Ref Des	Value	Manufacturer	Part Number
1	4	C1, C2, C3, C4	22uF/450V		
2	2	C5, C8	0.1uF		
3	1	C7	100uF/25V		
4	9	D1, D2, D3, D4, D5, D6, D7, D8, D13	Stand. Rec. 1A/1000V		1N4007GP
5	3	D9, D10, D11	TVS 180V		P6KE180A
6	1	D12	TVS 150V		P6KE150A
7	1	D14	Zener 15V		1N4744A
8	1	D15	Ultrafast 1A/200V		UF4004
9	1	J4	JUMPER		
10	1	L1	1mH	Toko	8RB-102Y
11	1	Q1	N-Chan. MOSFET 1A/600V	International Rectifier	IRFU1N60A
12	4	R1, R2, R3, R4	470k 1/2W		
13	2	R5, R6	1M 1/2W		
14	1	R7	10 ohm		
15	1	R8	200 ohm		
16	1	R10	13k 1%		
17	1	R11	2.05k 1%		
18	1	RF1	10R 3W		
19	1	T1	EE13 Transformer		
20	1	U1	PWM + MOSFET	Power Integrations	LNK304P



7 Transformer Specification

7.1 Transformer Electrical Diagram



Figure 4 – Transformer Electrical Diagram

7.2 Electrical Specifications

Electrical Strength	60 Hz 1 second, from pins 1-4 to pins 7-8	N/A
Primary Inductance (Pin 1 to Pin 2)	All windings open.	2.7 mH ±10%
Resonant Frequency	All windings open.	500 kHz min.
Primary Leakage Inductance	L_{12} with pins 7-8 shorted.	100 µH max.

7.3 Materials

ltem	Description
[1]	Core: EE13, TDK Gapped for A _L = 57 nH/T ²
[2]	Bobbin: Horizontal 8 pins.
[3]	Magnet Wire: #36 AWG.
[4]	Magnet Wire: #39 AWG.
[5]	Magnet Wire: #31 AWG.
[6]	Tape: 3M 1298 Polyester Film (white) 0.311" x 2 mils.
[7]	Varnish.





7.4 Transformer Build Diagram

Figure 5 – Transformer Build Diagram

7.5 Transformer Construction

W1 (Core Cancellation Winding)	Start at pin 6 temporarily. Wind 30 turns of item [3] from left to right uniformly without any space between turns, in a single layer across the entire width of the bobbin. Finish on Pin 4. Move the start end from pin 6 to pin 3.
Insulation	Add 4 layers of tape [6] for insulation.
W2 (Primary Winding)	Start at pin 2. Wind 55 turns of item [4] from right to left. After finishing the first layer, return to the right and add one layer of tape [6]. Then wind 55 turns of item [4] from right to left, after finishing the second layer, return to the right and add one layer of tape [6]. Then wind 54 turns of item [4] from right to left, after finishing the second layer, return to the right and add one layer of tape [6]. Again, wind 54 turns of item [4] from right to left, after finishing the fourth layer, return to the right and finish on Pin 1. Wind all layers uniformly without any spaces between the turns.
Insulation	Add 3 layers of tape [6] for insulation.
W3 (Shield Winding)	Start of pin 1, wind 3 turns of quadfilar item [5]. Wind from right to left in a single layer across 60% of the bobbin width. Cut the wires after finishing the third turn.
Insulation	Add 1 layer of tape [6] for insulation.
W4 (Secondary Winding)	Temporarily start at pin 3. Wind 30T of item [3] from right to left in a single layer without any spaces between adjacent turns, across the entire width of the bobbin, finish on pin 7. Then move the Start lead to pin 8.
Outer Insulation	Add 2 layers of tape [6] for insulation.
Final Assembly	Use guidelines specified in AN-24 for audio noise suppression techniques in the transformer construction.



7.6 Design Notes

Power Integrations Device	LNK304P
Frequency of Operation	66 KHz
Mode	Continuous/ discontinuous
Peak Current	0.23 A
Reflected Voltage (Secondary to Primary)	92V
Maximum AC Input Voltage	580 V
Minimum AC Input Voltage	57 V



8 Transformer Spreadsheets

Rev 1.0	INPUT	OUTPUT		TinySwitch-II_022001.xls: TINYSwitch-II Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APP	LICATION VARIABLE	3		Sch
VACMIN	57		Volts	Minimum AC Input Voltage
VACMAX	580		Volts	Maximum AC Input Voltage
1L	50		Hertz	AC Mains Frequency
vo	12		Volts	Output Voltage
PO	3		Watts	Output Power
n	0.6			Efficiency Estimate
z	0.5			Loss Allocation Factor
VB	12		Volts	Bias Voltage
iC .	3		mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	22		uFarads	Input Filter Capacitor
ENTER Tiny	Switch-II VARIABLES			
TNY-II	Ink304		Universal	115/230V
Chosen				
Device	LNK304	Power Out	5.5W	8W
LIMITMIN		0.233	Amps	
ILIMITMAX		0.267	Amps	
fS	66000		Hertz	Typical Switching Frequency
fSmin		57000	Hertz	Minimum Switching Frequency (inc jitter deviation)
fSmax		74000	Hertz	Maximum Switching Frequency (inc jitter deviation)
VOR	92.1		Volts	Reflected Output Voltage
VDS	10		Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.7		Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7		Volts	Bias Winding Diode Forward Voltage Drop
KP	0.86			Bias Winding Diode Forward Voltage Drop
ENTER TR/	NSFORMER CORE/CO	INSTRUCTIO	N VARIABL	ES
Core Type	ee13			
Core	#N//		P/N:	#N/A
Bobbin	#N//		P/N:	#N/A
AE	0.17	1	cm^2	Core Effective Cross Sectional Area
LE	3.0	2	cm	Core Effective Path Length
AL	113	D	nH/T^2	Ungapped Core Effective Inductance
BW	7.	4	mm	Bobbin Physical Winding Width
M	0		mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4			Number of Primary Layers
NS	30			Number of Secondary Turns
DC INPUT V	OLTAGE PARAMETEI	28		
VMIN		58	Volts	Minimum DC Input Voltage
VMAX		820	Volts	Maximum DC Input Voltage
CURRENT	WAVEFORM SHAPE P	RAMETERS		
DMAX		0.66		Maximum Duty Cycle
IAVG		0.09	Amps	Average Primary Current
		0.23	Amps	Peak Primary Current
IP Effective		0.23		Actual ID forum - Device 1, 1947
P ACIUAL		0.000		ACIUAL IN TIQUINE E CIEVICE E CIMILE
10		0.233		Astron File allow Controlling Francesco
fSact		0.233		Actual Effective Switching Frequency
fSact IR		0.233	Amps	Actual Effective Switching Frequency Primary Ripple Current
fSact IR IRMS		0.233 0.20 0.12	Amps Amps	Actual Effective Switching Frequency Primary Ripple Current Primary RMS Current
fSact IR IRMS		0.233 0.20 0.12	Amps Amps	Actual Effective Switching Frequency Primary Ripple Current Primary RMS Current
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9 Performance Data



9.1 Efficiency and Standby Power Consumption

Figure 6 - Efficiency and Standby Power Consumption vs. Input Voltage, Room Temperature, 60 Hz



9.2 Regulation



Figure 7 – Load Regulation, Room Temperature.



10 Waveforms



10.1 Drain Voltage and Current, Normal Operation





Figure 9 – 265 VAC, Full Load *(LNK304)* Upper: I_{DRAIN}, 0.1 A / div. Lower: V_{DRAIN}, 200 V / div, 20 μs / div.

10.2 Output Voltage Start-up Profile at Full Load







10.3 Drain Voltage and Current Start-up Profile



Figure 11 - 57 VAC Input and Maximum Load. Upper: I_{DRAIN}, 0.1 A / div (*LNK304*) Lower: V_{DRAIN}, 100 V & 1 ms / div.



10.4 Load Transient Response at 120VAC (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.







10.5 Output Ripple Measurements

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 13 and Figure 14.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μ F/50 V ceramic type and one (1) 1.0 μ F/50 V aluminum electrolytic. *The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).*



Figure 13 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 14 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)



10.5.2 Measurement Results at Full Load



Figure 15 – +12 V Ripple @ 57 VAC 2 ms, 200 mV / div







11 Conducted EMI

A conducted EMI scan of the prototype was taken to determine the effectiveness of the input pi-filter and transformer ESHIELDTM construction. The following plots show the peak performance of the converter against quasi-peak (QP) and average (AVG) limits of EN55022 Class B. Both scans were taken at 120VAC/60Hz input with maximum load applied to the output (250mA). Since the peak scan is below the average limits, it is expected that the QP and Average scans would have greater than 10db of margin below the limits.



Figure 17 - Conducted EMI (Neutral).



Figure 18- Conducted EMI (LINE).



12 Revision History

Date	Author	Revision	Description & changes	Reviewed
04-May-05	RSP	1.0	Initial Release	VC /JC / AM



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