Design Example Report

Title	*10 W CV/CC Single-Sided USB Charger Using InnoSwitch™-CH INN2023K*
Specification	85 VAC – 265 VAC Input; 5 V, 2 A Output (end of USB Cable)
Application	Cell Phone / USB Charger
Author	Applications Engineering Department
Document Number	DER-518
Date	March 10, 2016
Revision	1.1

Summary and Features

- InnoSwitch-CH - Industry first AC/DC ICs with isolated, safety rated integrated feedback
- All the benefits of secondary side control with the simplicity of primary side regulation
  - ±3% CV, ±5% CC regulation
  - Insensitive to transformer variation
  - Transient response independent of load timing
  - Smaller, lower cost output capacitors
  - <10 mW no-load input power
  - Cable voltage drop compensation
- Built in synchronous rectification for high efficiency
- Single sided PCB

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

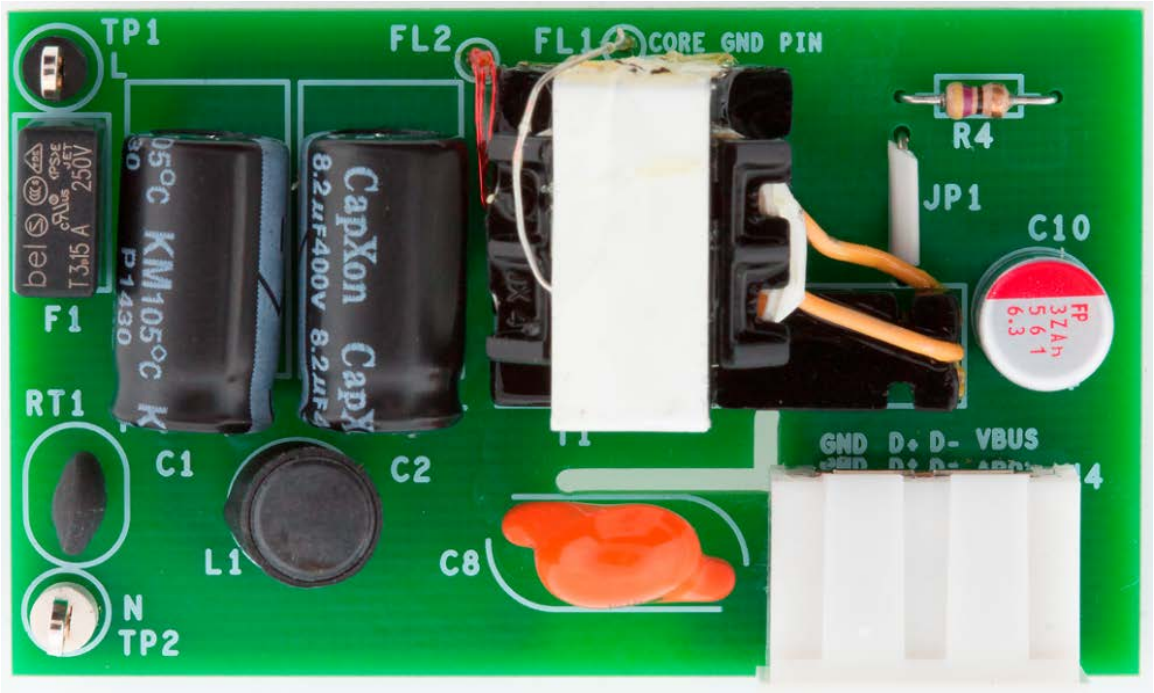

Figure 1 – Populated Circuit Board Photograph, Top.

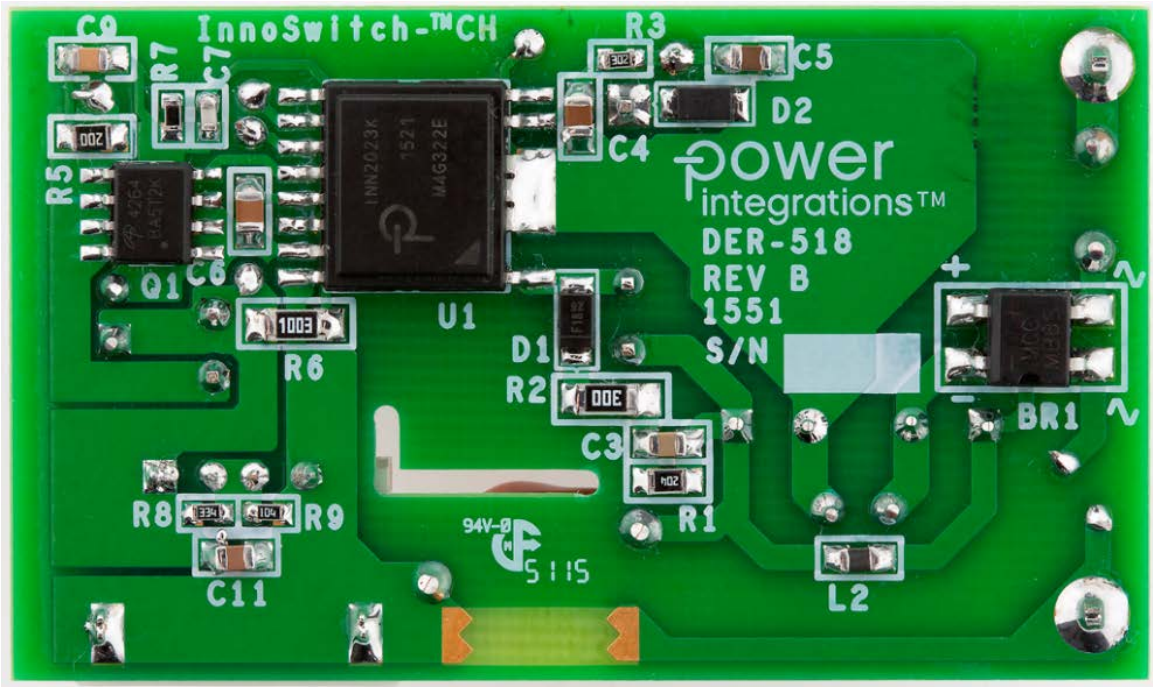

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				10	mW	230 VAC
Output						
Output Voltage	V_{OUT}	4.75	5.0	5.25	V	0.35 V cable resistance drop
Transient Output Voltage	$V_{OUT(T)}$	4.2		5.5	V	0 A - 2 A - 0 A load step end of cable At the end of the output cable
Output Ripple Voltage	V_{RIPPLE}			150	mV	At the end of the output cable
Output Cable Compensation	V_{CBL}	250	300	350	mV	At 2 A output current
Output Current CC point	I_{OUT}	2		2.5	A	
Auto-Restart Voltage	V_{AR}	2		3.5	V	At end of cable
Turn on Rise Time	t_R			20	ms	
Rated Output Power	P_{OUT}		10		W	
Efficiency						115 VAC, 230 VAC
Average	$\eta_{AVE[BRD]}$	84			%	Measured at USB socket
25%, 50%, 75%, and 100%	$\eta_{AVE[CBL]}$	80			%	With 0.38 V cable resistance drop
10%	$\eta_{10\%}$	79			%	
Environmental						
Output Cable Impedance	R_{CBL}		190		mΩ	
Conducted EMI		CISPR22B / EN55022B Load floating or grounded via artificial hand				Resistive load, 5 dB Margin
		Connected to mobile phone and TV (MHL connection enabled)				5 dB Margin
Safety		IEC950 / UL1950 Class II				Designed to meet
Audible noise				25	dB	Measured at 3 cm
Line Surge Common mode (L1/L2-PE)				6	kV	Ring Wave, Common Mode: 12 Ω
ESD		±16.5 ±8			kV kV	Contact Air discharge No degradation in performance
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level in sealed enclosure.

3 Schematic

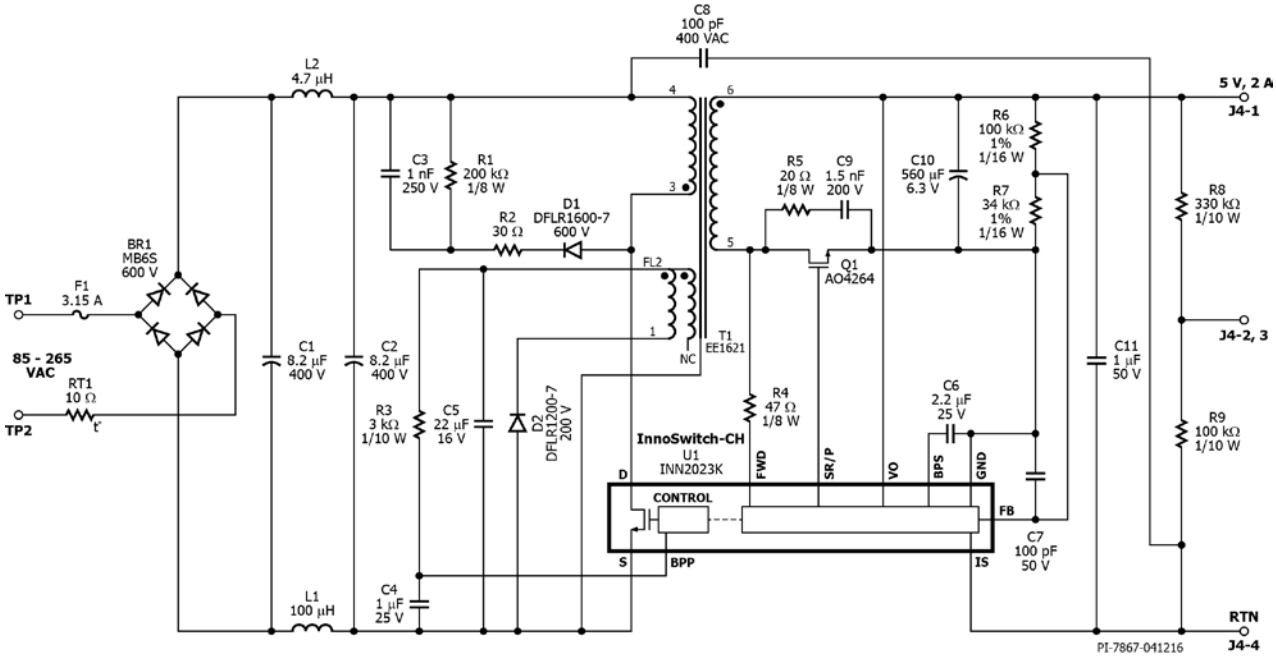

Figure 3 – Schematic.

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4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 provides protection against catastrophic failure of components on the primary side.

An inrush limiting thermistor (RT1) was necessary due to the low surge current rating of the rectifier bridge BR1 and the relatively high value and therefore low impedance of the bulk storage capacitors C1 and C2.

Physically small bridge rectifier BR1 was selected due to the limited space, specifically height from PCB to case.

Capacitor C1 and C2 provide filtering of the rectified AC input and together with L1 and L2 form a π (pi) filter to attenuate differential mode EMI. A low value Y capacitor (C8) reduces common mode EMI.

4.2 *InnoSwitch-CH IC Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 650 V power MOSFET inside the InnoSwitch-CH IC (U1).

A low cost RCD clamp formed by D1, R1, R2 and C3 limits the peak drain voltage due to the effects of transformer and output trace inductance.

The IC is self-starting, using an internal high voltage current source to charge the BPP pin capacitor (C4) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding, rectified and filtered (D2 and C5) and fed in the BPP pin via a current limiting resistor R3.

Output regulation is achieved using On/Off control, the number of enabled switching cycles are adjusted based on the output load. At high load most switching cycles are enabled, and at light load or no-load most cycled are disabled or skipped. Once a cycle is enabled, the power MOSFET remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arrange such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level.

4.3 *InnoSwitch-CH IC Secondary*

The secondary side of the InnoSwitch-CH provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by Q1 and filtered by C10. High frequency ringing during switching transients that would otherwise create high voltage across Q1 and radiated EMI is reduced via snubber components R5 and C9.

To reduce dissipation synchronous rectification (SR) is provided by Q1. The gate of Q1 is turned on based on the winding voltage sensed via R4 and the FWD pin of the IC. In continuous conduction mode operation the power MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold. Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. During CV operation the output voltage powers the device, fed into the VO pin.

During CC operation, when the output voltage falls the device will power itself from the secondary winding directly. During the on-time of the primary side MOSFET the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C6 via R4 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than the auto-restart voltage threshold which has a typical value of 3.45V.

Output current is sensed internally between the IS and GND pins with a threshold of 33 mV to minimize losses. Once the internal current sense threshold is exceeded, the device adjusts the number of enabled switching cycles to maintain a fixed output current.

Below the CC threshold the device operates in constant voltage mode. The output voltage is sensed via resistor divider R8 and R9 operation with a reference voltage of 1.265 V on the FB pin when at the regulation output voltage.

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5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

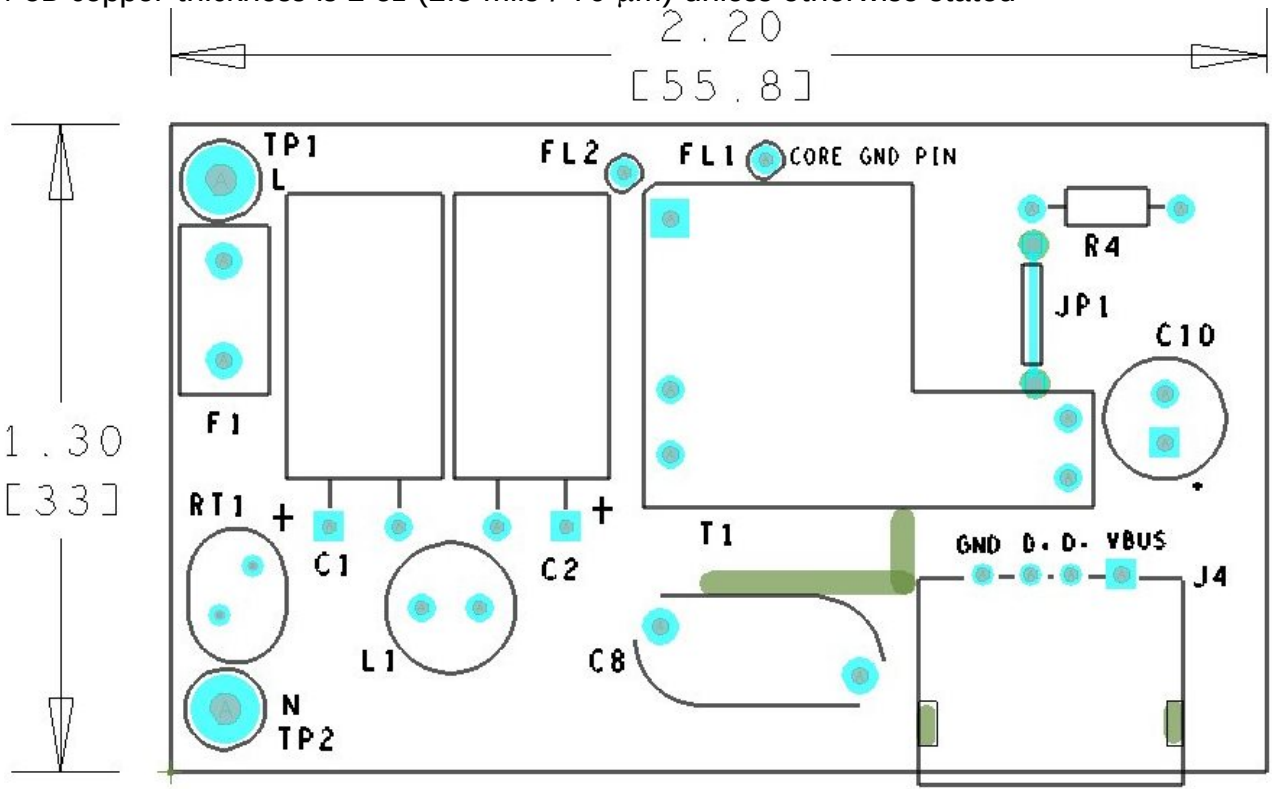

Figure 4 – Printed Circuit Layout, Top.

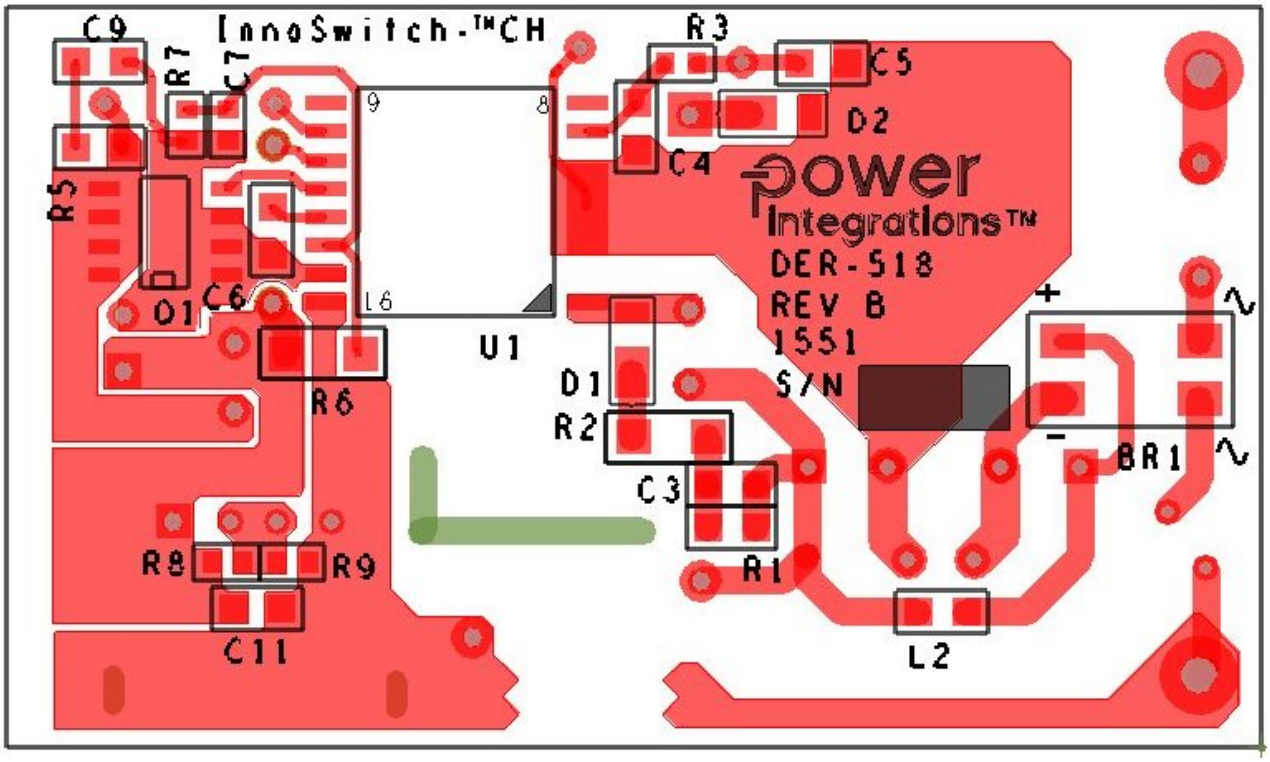

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	2	C1 C2	8.2 uF, 400 V, Electrolytic, (8 x 14)	KM8R2M400F140A	Capxon
3	1	C3	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
4	1	C4	1 uF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
5	1	C5	22 µF, 16 V, Ceramic, X5R, 0805	C2012X5R1C226K	TDK
6	1	C6	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
7	1	C7	100 pF 100V 10 % X7R 0805	08051C101JAT2A	AVX
8	1	C8	100 pF, Ceramic, Y1	440LT10-R	Vishay
9	1	C9	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
10	1	C10	560 µF, 6.3 V, Al Organic Polymer, Gen. Purpose, 20%	RS80J561MDN1JT	Nichicon
11	1	C11	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
12	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
13	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
14	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
15	2	FL1 FL2	Flying Lead, Hole size 30mils	N/A	N/A
16	1	J4	CONN USB FMALE REVERSE	USB AF DIP-318-HW	GOLDCONN
17	1	L1	100 µH, 0.490 A, 20%	RL-5480-2-100	Renco
18	1	L2	4.7 µH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
19	1	Q1	MOSFET, N-CH, 60V, 12A, 8SOIC	AO4264	Alpha & Omega Semiconductor
20	1	R1	200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
21	1	R2	30 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ300V	Panasonic
22	1	R3	3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
23	1	R4	47 Ω, 5%, 1/8 W, Carbon Film	CF18JT47R0	Stackpole
24	1	R5	20 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ200V	Panasonic
25	1	R6	100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
26	1	R7	34 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3402V	Panasonic
27	1	R8	330 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ334V	Panasonic
28	1	R9	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
29	1	RT1	NTC Thermistor, 10 Ohms, 0.7 A	MF72-010D5	Cantherm
30	1	T1	Bobbin, EE1621, Vertical, 8 pins, 4pri, 4sec	EE-1621	Shen Zhen Xin Yu Jia
31	1	TP1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
32	1	TP2	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
33	1	U1	InnoSwitch-CH	INN2023K	Power Integrations

7 Transformer Specification

7.1 *Electrical Diagram*

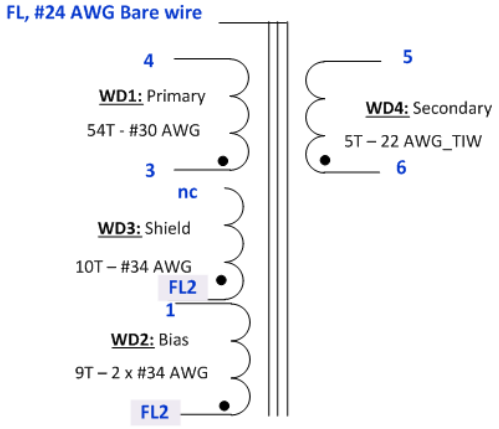

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	546 µH ±5%
Resonant Frequency	Pins 3-4, all other windings open.	1500 kHz (min)
Primary Leakage Inductance	Pins 3-4, with pins 5-6 shorted, measured at 100 kHz, 0.4 V_{RMS}.	25 µH (max)

7.3 *Transformer Build Diagram*

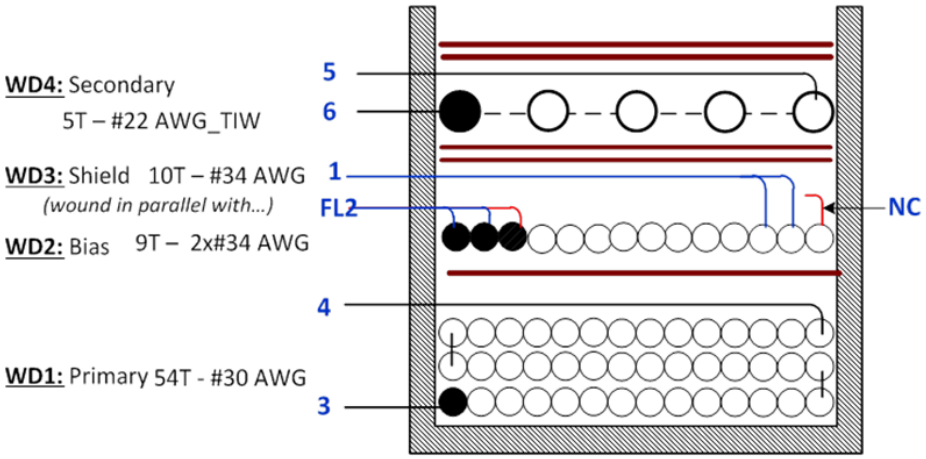

Figure 7 – Transformer Build Diagram.

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8 Transformer Design Spreadsheet

ACDC_InnoSwitch-CH_101614; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch_101614_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			85	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	5.00		5.00	V	Output Voltage (continuous power at the end of the cable)
IO	2.00		2.00	A	Power Supply Output Current (corresponding to peak power)
Power			10.6	W	Continuous Output Power, including cable drop compensation
n	0.82		0.82		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	16.40	Info	16.40	uFarad	!!! Input capacitor is too small. Recommnded to increase CIN above 19.05 uF to ensure VMIN>70 V
ENTER InnoSwitch VARIABLES					
InnoSwitch-CH	INN20x3		INN20x3		User defined InnoSwitch
Cable drop compensation	6%		6%		Select Cable Drop Compensation option
Complete Part Number			INN2023K		Final part number including package
Chose Configuration	INC		Increased Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.682	A	Minimum Current Limit
ILIMITTYP			0.75	A	Typical Current Limit
ILIMITMAX			0.818	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			47.25	A^2kHz	Worst case I2F parameter across the temperature range
VOR	58		58	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.80		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.46		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			9.32	V	Bias Winding Number of Turns
PIVB			102.59	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	Custom		Custom		Enter Transformer Core
Core	EE1621		EE1621		Enter core part number, if necessary
Bobbin			0		Enter bobbin part number, if necessary
AE	0.325		0.325	cm^2	Core Effective Cross Sectional Area

LE	3.93		3.93	cm	Core Effective Path Length
AL	2800		2800	nH/T^2	Ungapped Core Effective Inductance
BW	5.40		5.40	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3		Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	62	Warning	62	V	!!! Minimum DC Input Voltage < 70 Volts. Increase VACMIN or increase CIN
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.21	A	Average Primary Current
IP			0.682	A	Peak Primary Current assuming ILIMITMIN
IR			0.546	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.31	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			546	uHenry	Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 518 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			54		Primary Winding Number of Turns
ALG			187	nH/T^2	Gapped Core Effective Inductance
BM			2868	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1147	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2694		Relative Permeability of Ungapped Core
LG			0.20	mm	Gap Length (Lg > 0.1 mm)
BWE			16.2	mm	Effective Bobbin Width
OD			0.30	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.25	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			259	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			7.37	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			3.33	A	Secondary RMS Current
IRIPPLE			2.67	A	Output Capacitor RMS Ripple Current
CMS			667	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			517	V	Maximum Drain Voltage Estimate
PIVS			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.30	V	Main Output Voltage directly after output rectifier

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IO1			2.00	A	Output DC Current
PO1			10.60	W	Output Power
VD1			0.06	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			5.00	Turns	Output Winding Number of Turns
ISRMS1			3.33	A	Output Winding RMS Current
IRIPPLE1			2.67	A	Output Capacitor RMS Ripple Current
PIVS1			54	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			QM6006		Recommended SR FET for this output
RDSON_HOT			0.027	Ohm	RDSon at 100C
VRATED			60	V	Rated voltage of selected SR FET
CMS1			667	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.08	mm	Maximum Outside Diameter for Triple Insulated Wire

9 *Average Efficiency*

9.1.1 Efficiency Requirements

Test	Average	Average	Average	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
Effective	Now	2016	2016	2016
Power [W]	**Energy Star 2**	**New IESA2007**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
10	**74.2%**	**78.7%**	**79.0%**	**69.7%**

9.1.2 Average Efficiency Measured at the End of Cable

Load	85 VAC	115 VAC	230 VAC	265 VAC
100 %	77.6%	78.8%	79.9%	79.8%
75 %	79.1%	80.4%	81.3%	80.3%
50 %	80.5%	82.3%	81.2%	80.8%
25 %	81.0%	82.1%	81.6%	81.2%
10 %	79.8%	80.7%	80.4%	80.0%
Average	79.6%	80.9%	81.0%	80.5%

9.1.3 Average Efficiency Measured at the USB Socket on the Board

Load	85 VAC	115 VAC	230 VAC	265 VAC
100 %	83.1%	84.4%	85.5%	85.4%
75 %	83.2%	84.6%	85.5%	84.5%
50 %	83.3%	85.1%	84.1%	83.6%
25 %	82.5%	83.5%	83.0%	82.6%
10 %	80.3%	81.2%	80.9%	80.6%
Average	83.0%	84.4%	84.5%	84.0%

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10 Performance Data

10.1 *Efficiency Measured at Cable End*

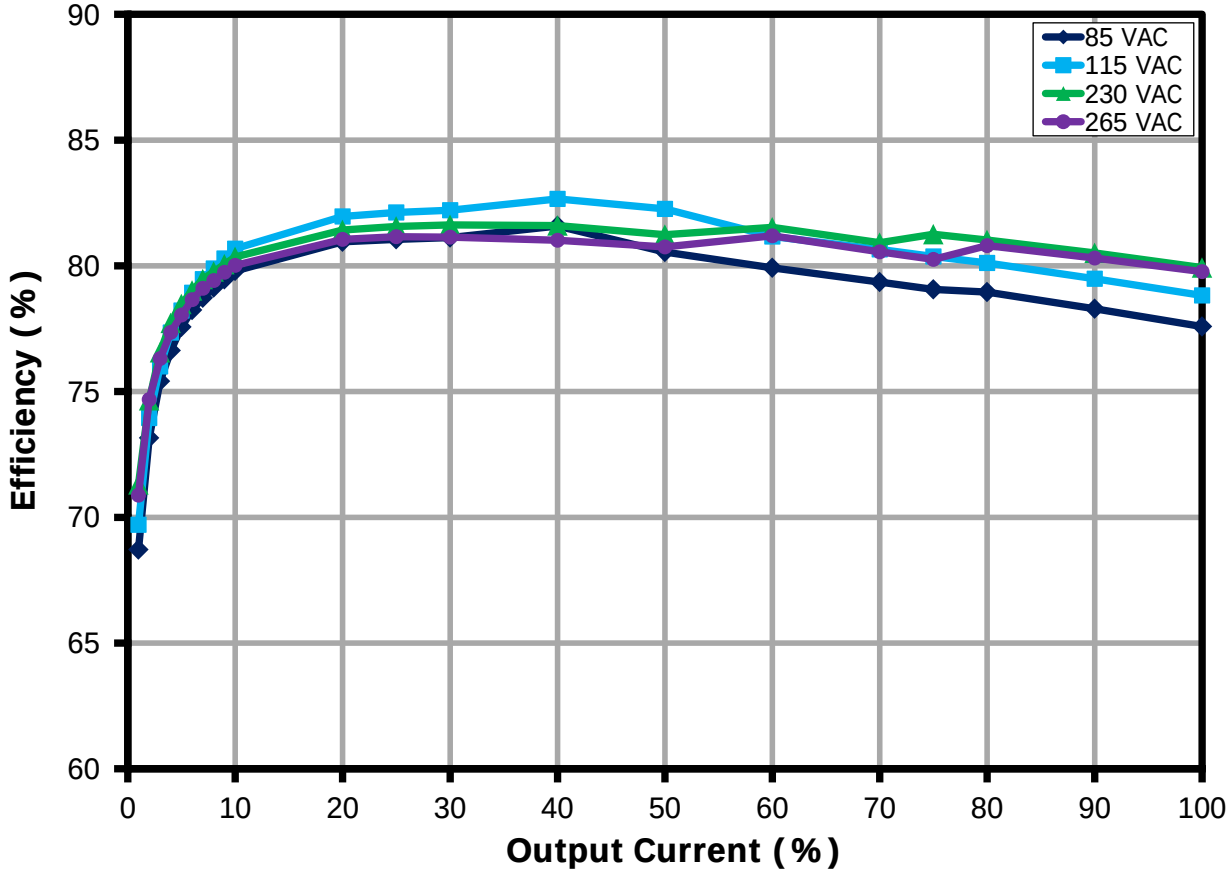

Figure 8 – Efficiency at Cable.

10.2 *Efficiency at Connector on the Board*

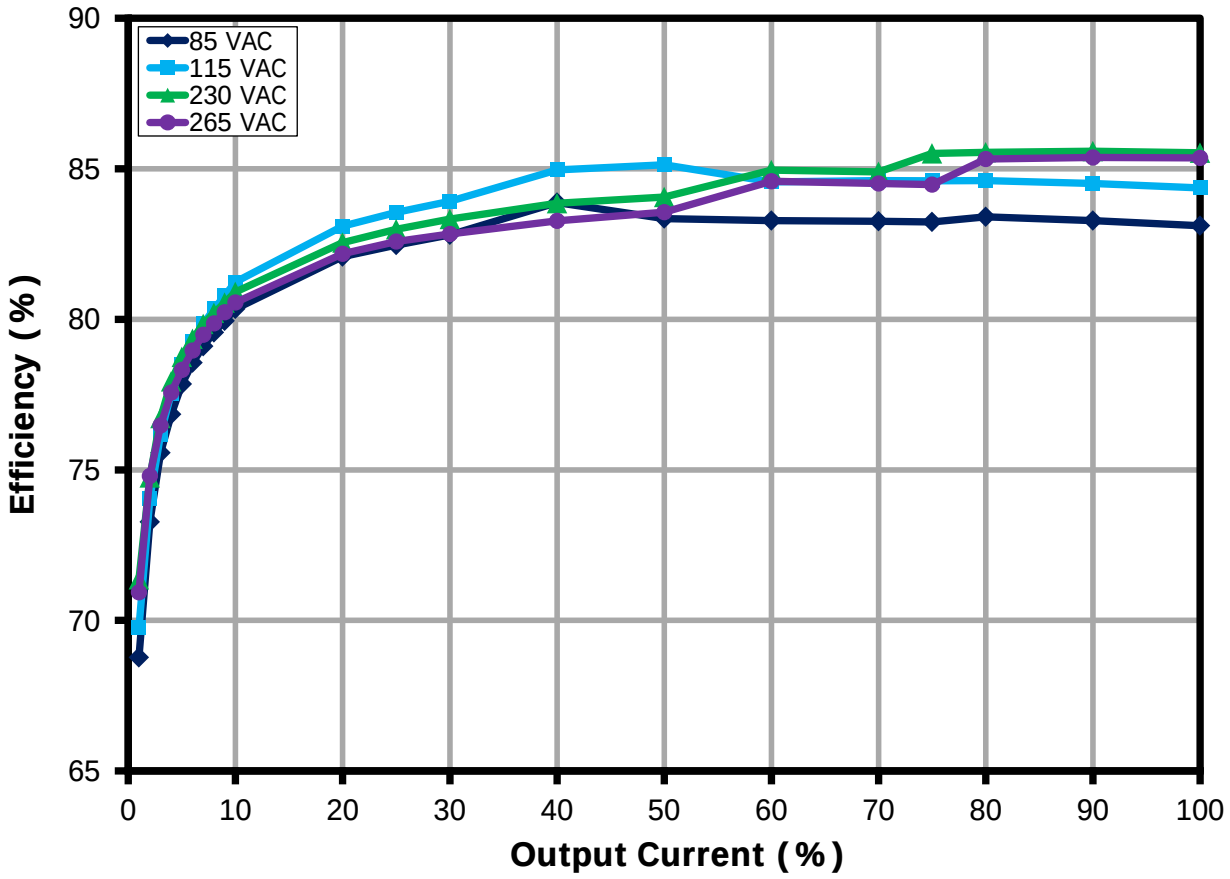

Figure 9 – Efficiency at Board.

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10.3 *CV/CC Regulation at Cable End*

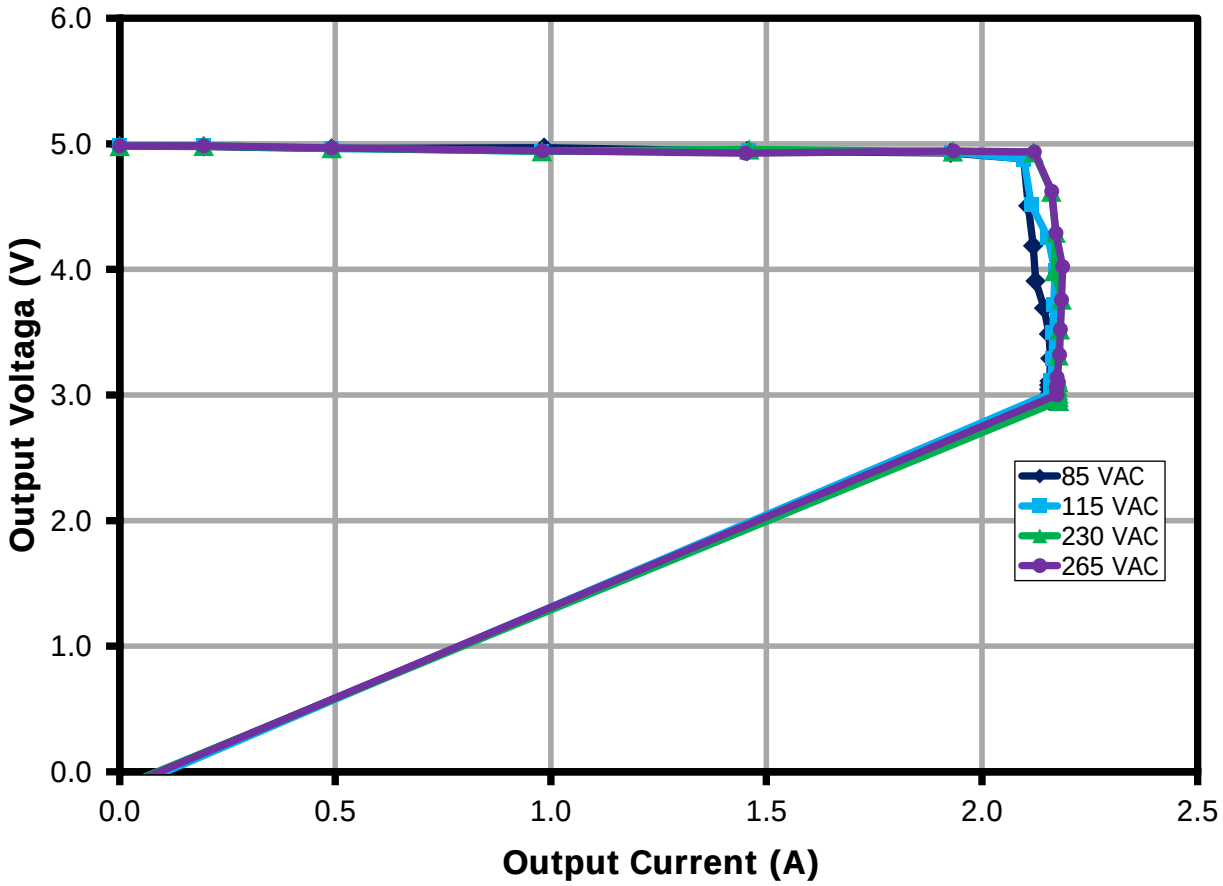

Figure 10 – CV/CC at Cable. Cable Drop = 0.32 V Max. Measured with 47 μF at the End of the Cable.

10.4 *CV/CC Regulation at Board*

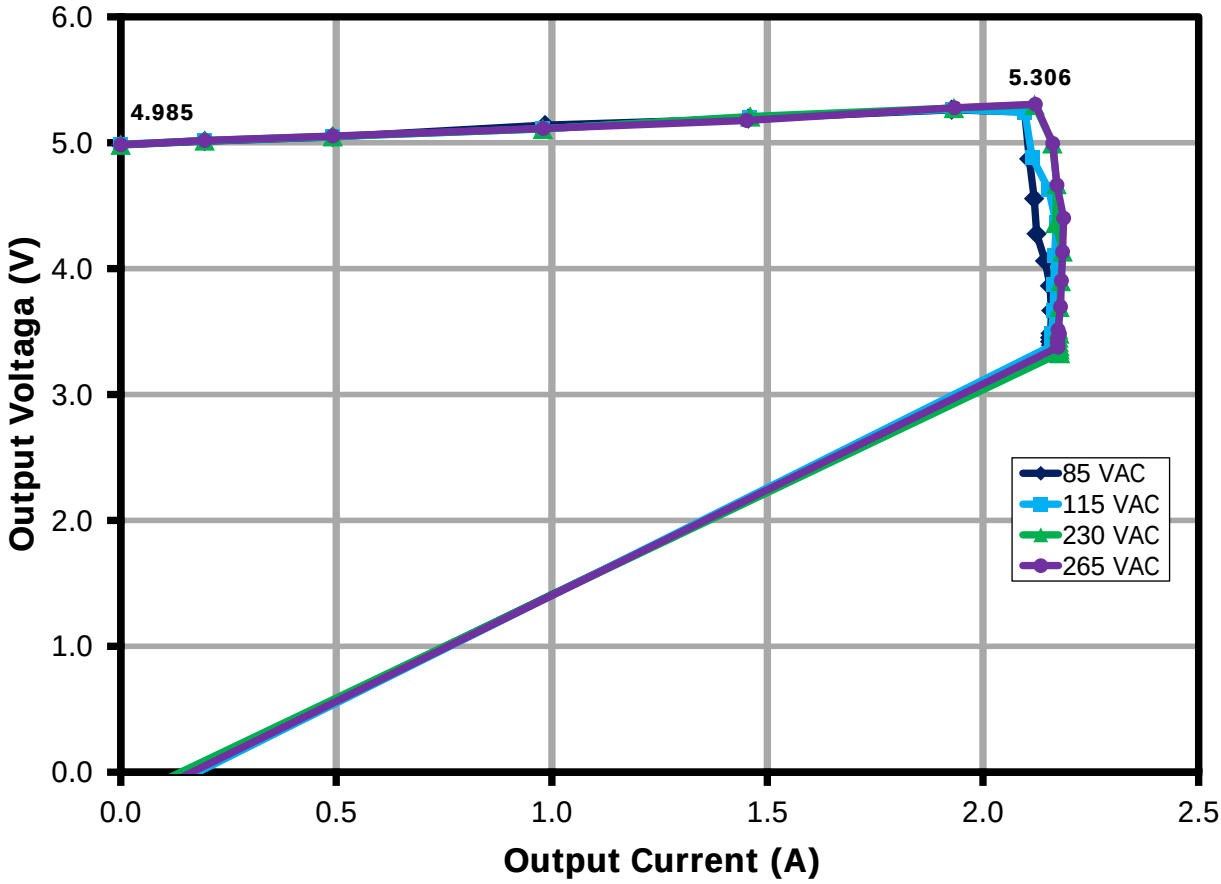

Figure 11 – CV/CC at Board, Room Temperature

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11 Thermal Performance

11.1 85 VAC

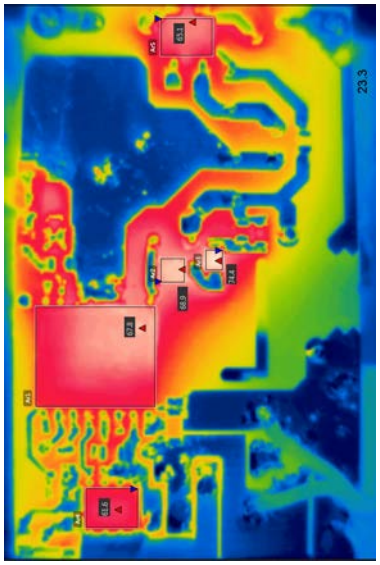

Figure 12 – Bottom Side.
5 V, 2 A Load.

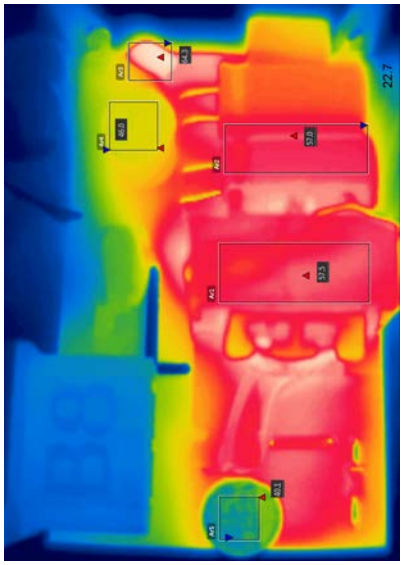

Figure 13 – Top Side.
5 V, 2 A Load.

Input Voltage		85 VAC (°C)
InnoSwitch-CH	U1	67.8
Clamp Diode	D1	68.9
Clamp Res. In series	R2	74.4
SR FET	Q1	61.6
Bridge Diode	BR1	65.1
Transformer	T1	57.5
Input Capacitor	C1	57.0
Thermistor	RT1	64.3
Output Capacitor	C10	40.1
Input Filter	L1	46
Ambient	$T_{AMBIENT}$	23.3

11.2 265 VAC

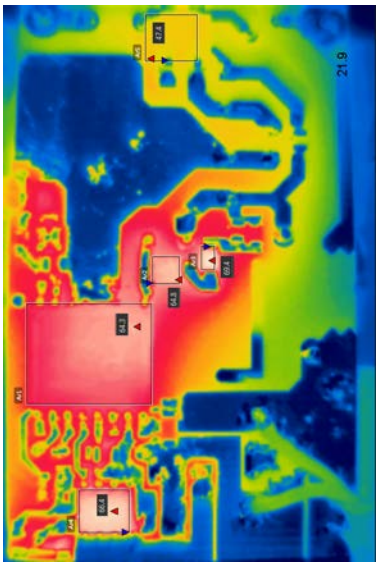

Figure 14 – Bottom Side.
5 V, 2 A Load.

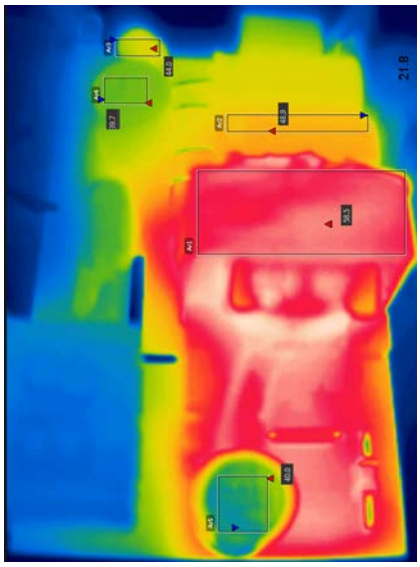

Figure 15 – Top Side.
5 V, 2 A Load.

Input Voltage		265 VAC (°C)
InnoSwitch-CH	U1	64.3
Clamp Diode	D1	64.8
Clamp Res. In series	R2	69.4
SR FET	Q1	66.4
Bridge Diode	BR1	47.4
Transformer	T1	58.5
Input Capacitor	C1	49.8
Thermistor	RT1	44
Output Capacitor	C10	40
Input Filter	L1	39.7
Ambient	$T_{AMBIENT}$	21.9

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12 Waveforms

12.1 *Load Transient Response (End of Cable)*

Results were measured with 47 µF at end of cable which is the typical specified measurement condition for mobile phone chargers.

Test Condition		
Cable Resistance		188 mΩ
Load	Slew Rate	0.25 A / µs
	T_{ON}	100 ms
	T_{OFF}	100 ms
	CC Mode	

Figure 16 – Transient Response
85 VAC, 0-2 A Load Step.
Min. V_{OUT}: 4.395 V,
Max. V_{OUT}: 5.318 V.
CH1(Olive): V_{OUT}, 0.2 V / div.
CH3(Blue): I_{OUT}, 1 A / div.
50 ms / div., 200 µs / div. (Zoom).

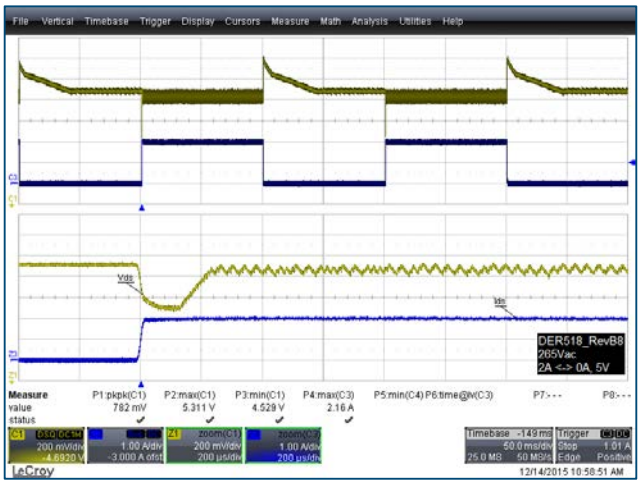

Figure 17 – Transient Response
265 VAC, 0-2 A Load Step.
Min. V_{OUT}: 4.529 V,
Max. V_{OUT}: 5.311 V.
CH1(Olive): V_{OUT}, 0.2 V / div.
CH3(Blue): I_{OUT}, 1 A / div.
50 ms / div., 200 µs / div. (Zoom).

12.2 *Start-up with 3000 µF, 85 VAC*

Test Condition	
V_{IN}	85 VAC
V_{OUT}	5 V
I_{OUT}	2 A

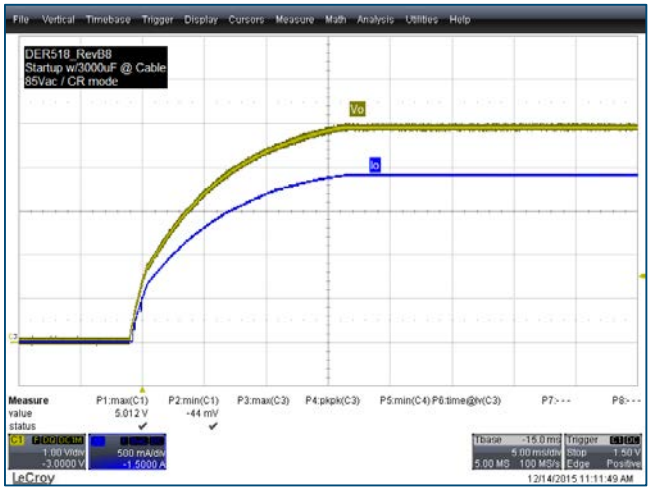

Figure 18 – Load in CR Mode.
CH1(Olive): V_{OUT}, 1 V / div.
CH3(Blue): I_{OUT}, 2 A / div., 5 ms / div.

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12.3 *Output Ripple Noise at USB Cable*

Test Condition	
USB Cable Resistance	188 mΩ
Electrolytic Capacitor	47 µF
Ceramic Capacitor	0.1 µF
Load	CC Mode

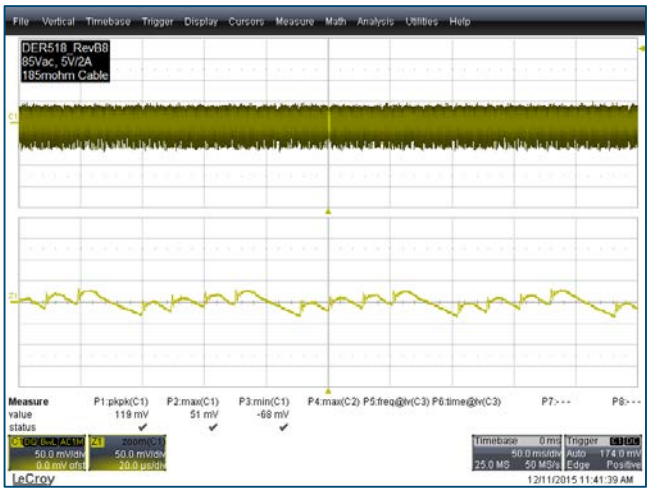

Figure 19 – 85VAC, 2A Load P-P Ripple: 0.119 V.
CH1(Olive): V_{OUT}, 50 mV / div.
50 µs / div., 20 µs / div. (Zoom).

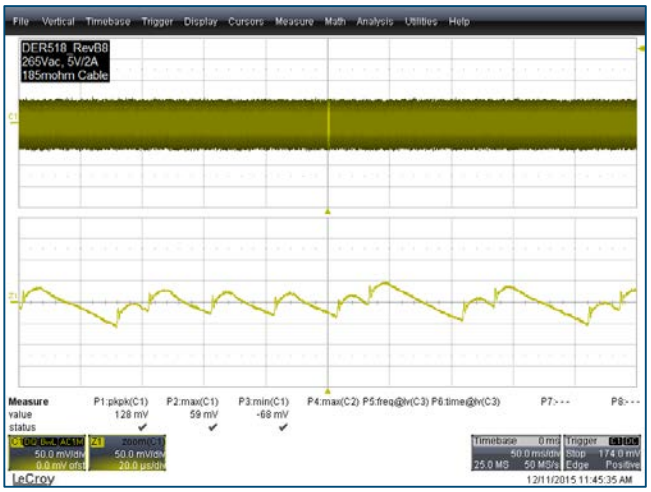

Figure 20 – 265VAC, 2A Load P-P Ripple: 0.128 V
CH1(Olive): V_{OUT}, 50 mV / div.
50 µs / div., 20 µs / div. (Zoom).

12.4 *InnoSwitch-CH Switching Waveforms:*

Test Condition	
V_{IN}	265 VAC
V_{OUT}	5 V
I_{OUT}	2 A

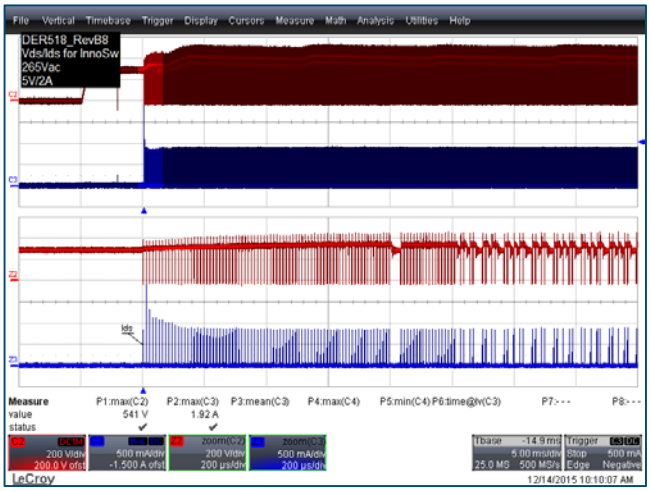

Figure 21 – Start-up.
$V_{DS(MAX)}$: 541 V
83.2% of BV_{DSS}.
5 µs / div., 200 µs / div. (Zoom).
CH2(Red): V_{DS}, 200 V / div.
CH3(Blue): I_{DS}, 0.5 A / div.

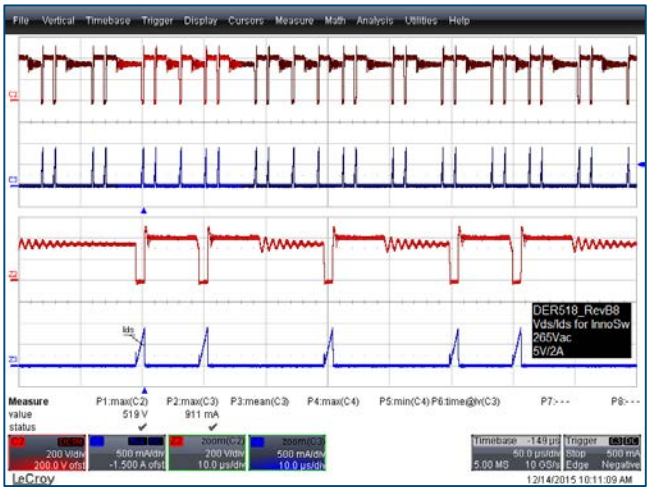

Figure 22 – Normal Operation.
$V_{VDS(MAX)}$: 519 V.
79.8% of BV_{DSS}.
50 µs / div., 10 µs / div. (Zoom).
CH2(Red): V_{DS}, 200 V / div.
CH3(Blue): I_{DS}, 0.5 A / div.

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12.5 *SR-MOSFET Switching Waveforms:*

Test Condition	
V_{IN}	265 VAC
V_{OUT}	5 V
I_{OUT}	2 A

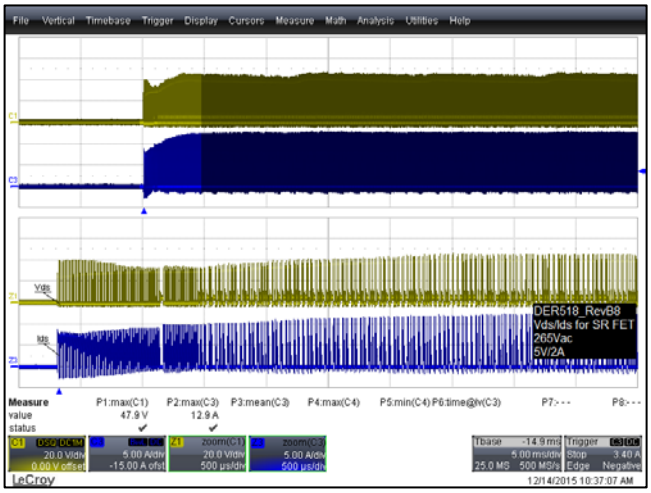

Figure 23 – Start-up.
$V_{DS(MAX)}$: 47.9 V
79.8% of BV_{DSS}.
5 µs / div., 500 µs / div. (Zoom).
CH1(Olive): V_{DS}, 20 V / div.
CH3(Blue): I_{DS}, 5 A / div.

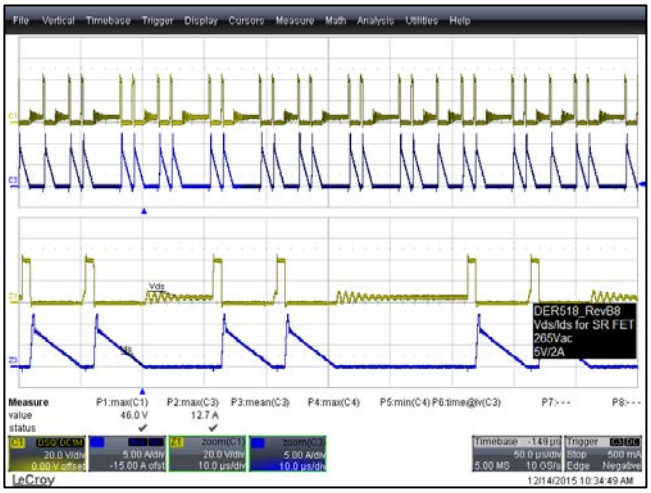

Figure 24 – Normal Operation.
$V_{VDS(MAX)}$: 46V.
76.7% of BV_{DSS}.
50 µs / div., 10 µs / div. (Zoom).
CH2(Red): V_{DS}, 200 V / div.
CH3(Blue): I_{DS}, 0.5 A / div.

13 Conductive EMI

13.1 *No Chassis Ground*

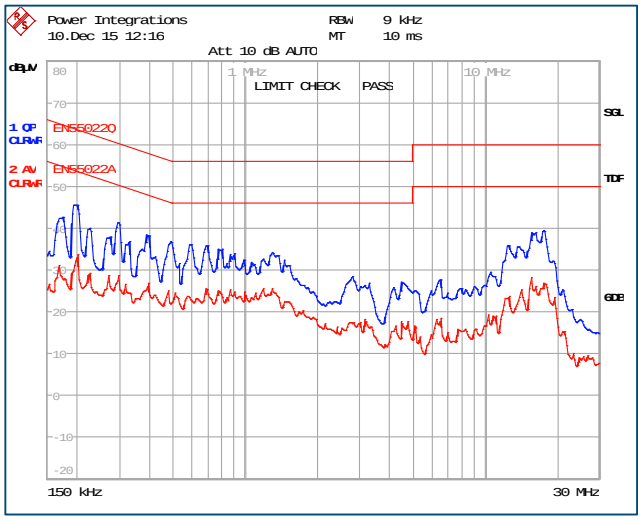

Figure 25 – Line. 230 VAC, 5 V, 2 A.
Margin:
- 18.08 dB @ 201 Hz, QP.
- 19.91 dB @ 201 kHz, AV.

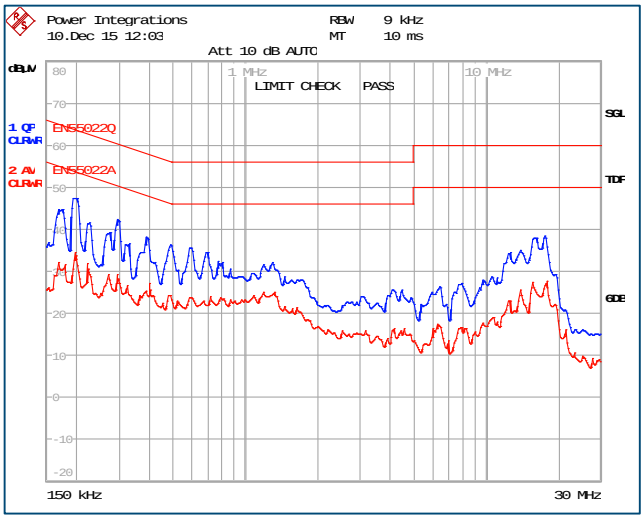

Figure 26 – Neutral. 230 VAC, 5 V, 2 A.
Margin:
- 16.28 dB @ 198 kHz, QP.
- 19.16 dB @ 198 kHz, AV.

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13.2 *Chassis Ground*

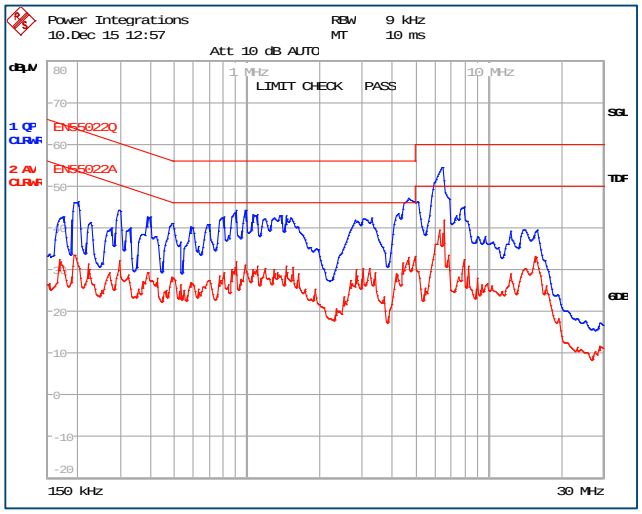

Figure 27 – Line. 230 VAC, 5 V, 2 A.
Margin:
- 18.08 dB @ 201 Hz, QP.
- 19.91 dB @ 201 kHz, AV.

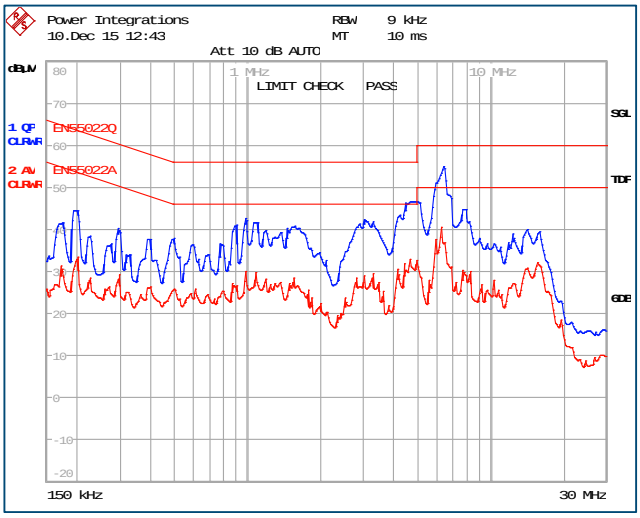

Figure 28 – Neutral. 230 VAC, 5 V, 2 A.
Margin:
- 16.28 dB @ 198 kHz, QP.
- 19.16 dB @ 198 kHz, AV.

13.3 *Artificial Hand Ground*

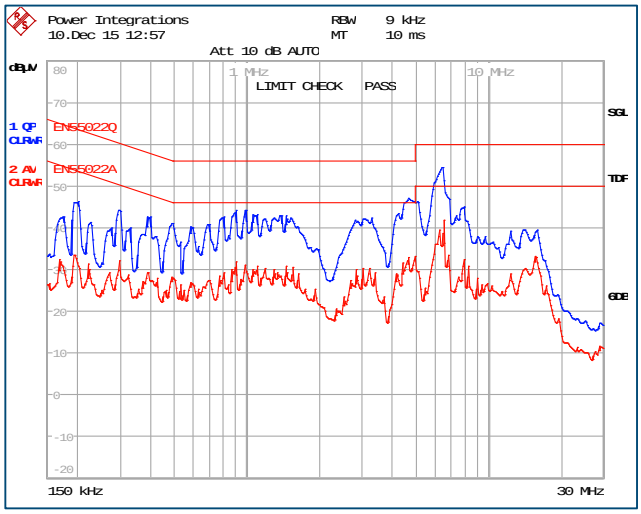

Figure 29 – Line. 230 VAC, 5 V, 2 A.
Margin:
- 14.6 dB @ 909 kHz, QP.
- 15.95 dB @ 909 kHz, AV.

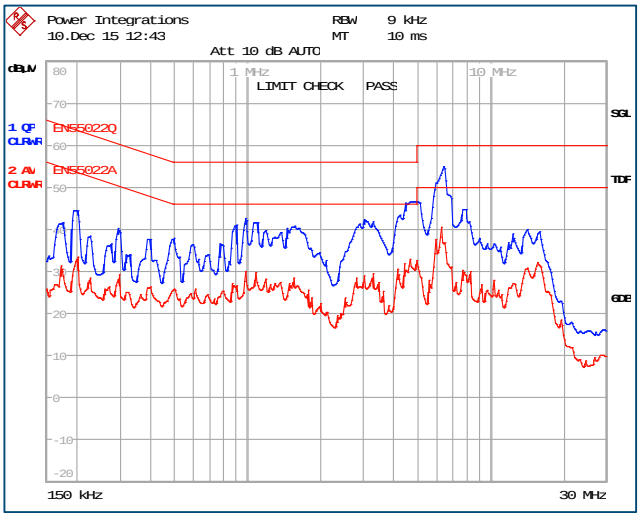

Figure 30 – Neutral. 230 VAC, 5 V, 2 A.
Margin:
- 18.18 dB @ 984 kHz, QP.
- 17.17 dB @ 420 kHz, AV.

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14 ESD and Line Surge Test

ESD			
Discharge		**Voltage**	**Result**
Air	±Pin	16.5 kV	Pass
Contact		8.8 kV	Pass
Line Surge			
	Mode	**Voltage**	**Result**
Combination	Differential	1 kV	Pass
Ring Wave	Common	6 kV	Pass

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
12-Feb-16	RJ	1.0	Initial Release	Mktg & Apps
10-Mar-16	RJ	1.1	Updates and corrections	Mktg & Apps

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