Design Example Report

Title	*25 W Dual Output Power Supply Using InnoSwitch™-EP INN2605K*
Specification	90 VAC – 265 VAC Input; 5 V, 1.5 A and 55 V, 0.32 A Outputs
Application	LED Monitors
Author	Applications Engineering Department
Document Number	DER-504
Date	June 29, 2016
Revision	1.2

Summary and Features

- InnoSwitch-EP - industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built in synchronous rectification for >89% efficiency without NTC at nominal AC input
- All the benefits of secondary side control with the simplicity of primary side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Meets output cross regulation requirements without linear regulators
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 1.5 A, 5 V and 0.32 A, 55 V dual output embedded power supply utilizing INN2605K from the InnoSwitch-EP family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

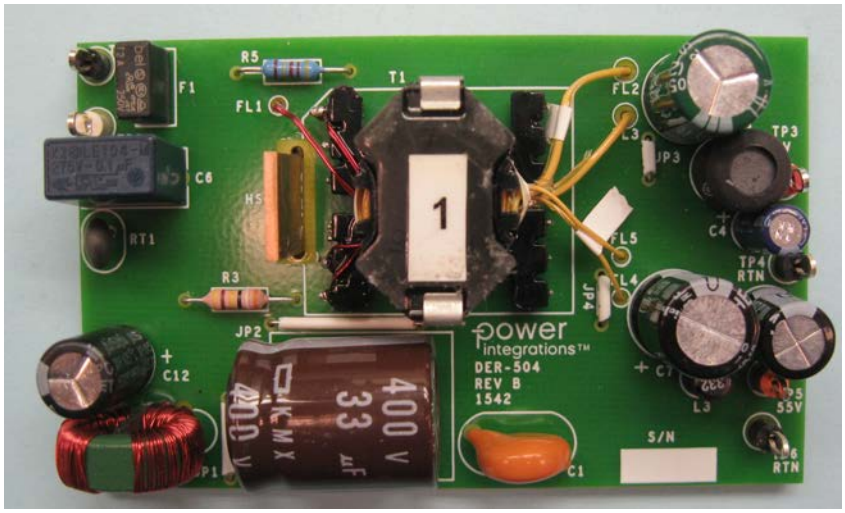

Figure 1 – Populated Circuit Board Photograph, Top.

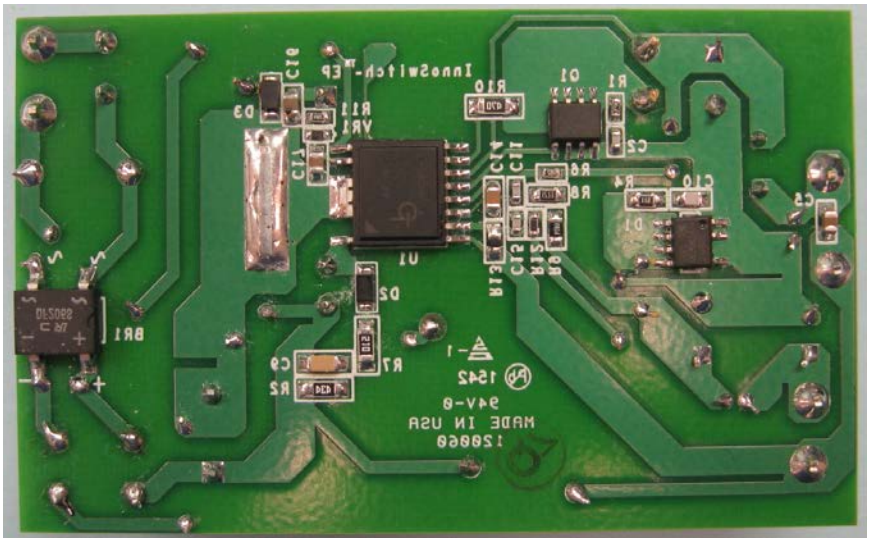

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			100	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		1.5	A	
Output Voltage 2	V_{OUT2}	50	55	65	V	±15%.
Output Ripple Voltage 2	$V_{RIPPLE2}$			500	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0.1		0.32	A	
Total Output Power						
Continuous Output Power	P_{OUT}		25		W	
Efficiency						
Full Load	η	88			%	Measured at 110 / 230 VAC, P_{OUT} 25 ºC.
No Load Input Power				35	mW	V_{IN} at 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 Schematic

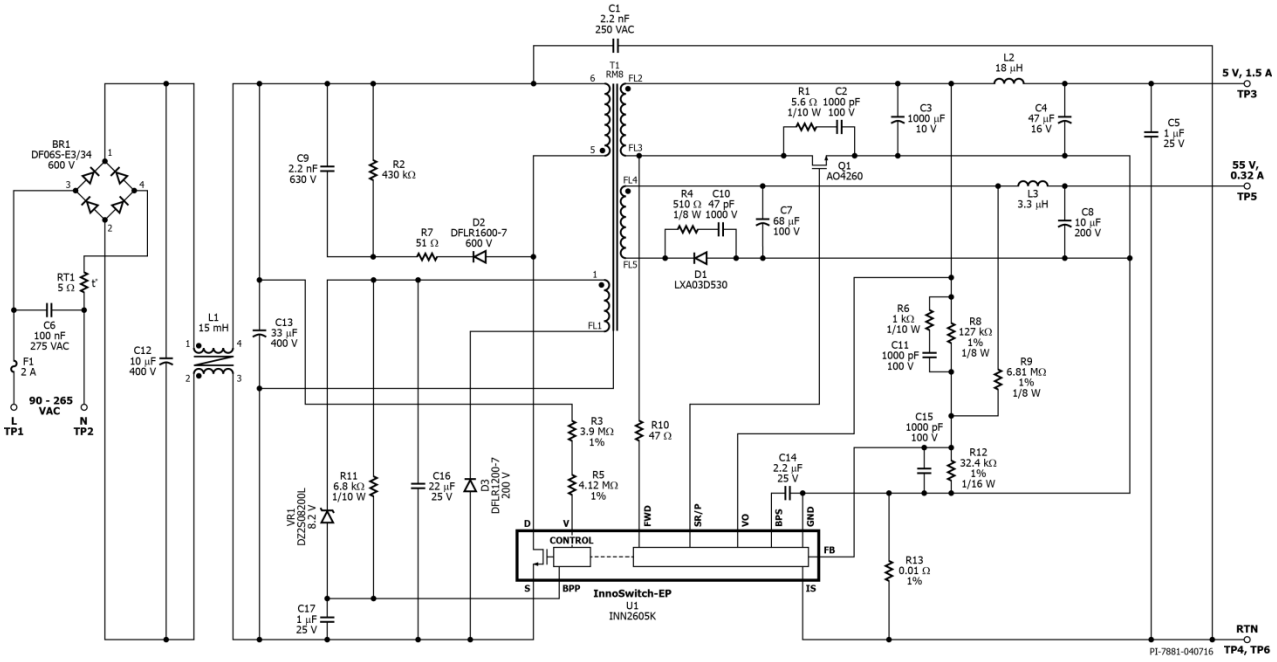

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and the common mode choke L1 with capacitors, C1 and C6, provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C12 and C13. Inrush current limiter RT1 limits the surge current into bridge rectifier. The differential inductance of common mode choke L1 with capacitors C12 and C13 provide differential noise filtering.

4.2 *InnoSwitch-EP Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the InnoSwitch-EP IC (U1).

A low cost RCD clamp formed by D2, R7, R2, and C9 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C17, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D3 and capacitor C16, and fed in the BPP pin via a current limiting resistor R11. The primary side overvoltage protection is obtained using Zener diode VR1. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR1 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch-EP IC.

Resistor R3 and R5 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C13. At approximately 100 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 460 V DC, the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1.

4.3 *InnoSwitch-EP Secondary*

The secondary side of the InnoSwitch-EP provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q1. Very low ESR capacitor C3 provides filtering, and inductor L2 and capacitor C4 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 55 V output is provided by Qspeed diode D1. Very low ESR capacitors C7 provides filtering, and inductor L3 and capacitor C8 form a second stage

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filter that significantly attenuates the high frequency ripple and noise at the 55 V output. Capacitor C5 reduces the radiation EMI noise.

RC snubber networks comprising R1 and C2 for Q1, R4 and C10 for D1 damp high frequency ringing across SR FET and diode, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 is turned on based on the winding voltage sensed via R10 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C14 via R10 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Resistor R8, R9 and R12 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. The InnoSwitch-EP IC has an internal reference of 1.265 V. Feedback compensation RC networks comprising capacitor C11 and resistor R6 reduce the output ripple voltage. Capacitor C15 provides decoupling from high frequency noise affecting power supply operation. Total output current is sensed by R13 with a threshold of approximately 33 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

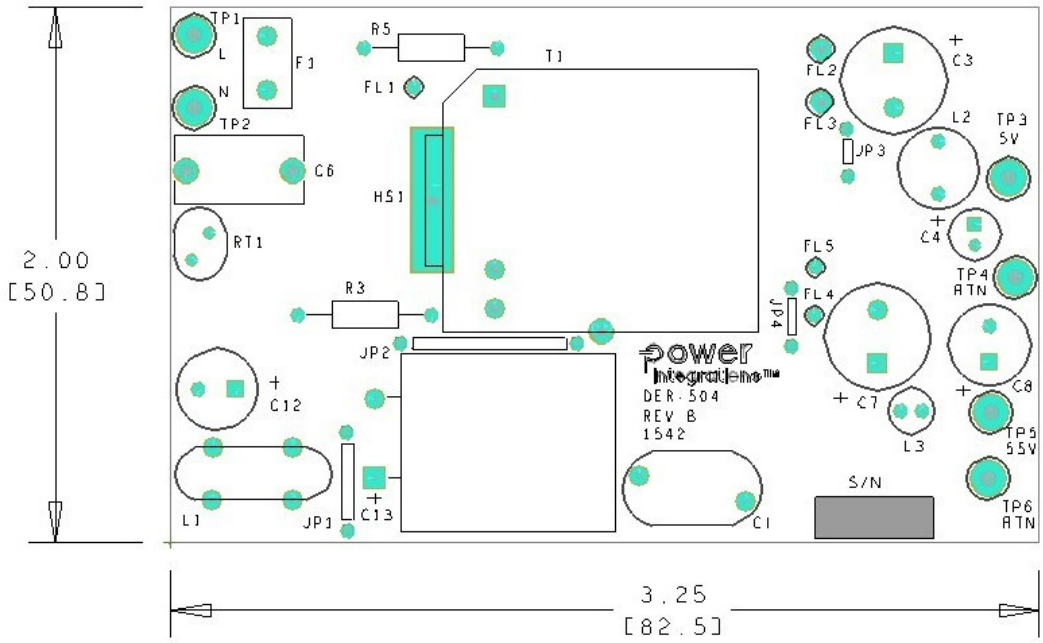

Figure 4 – Printed Circuit Layout, Top.

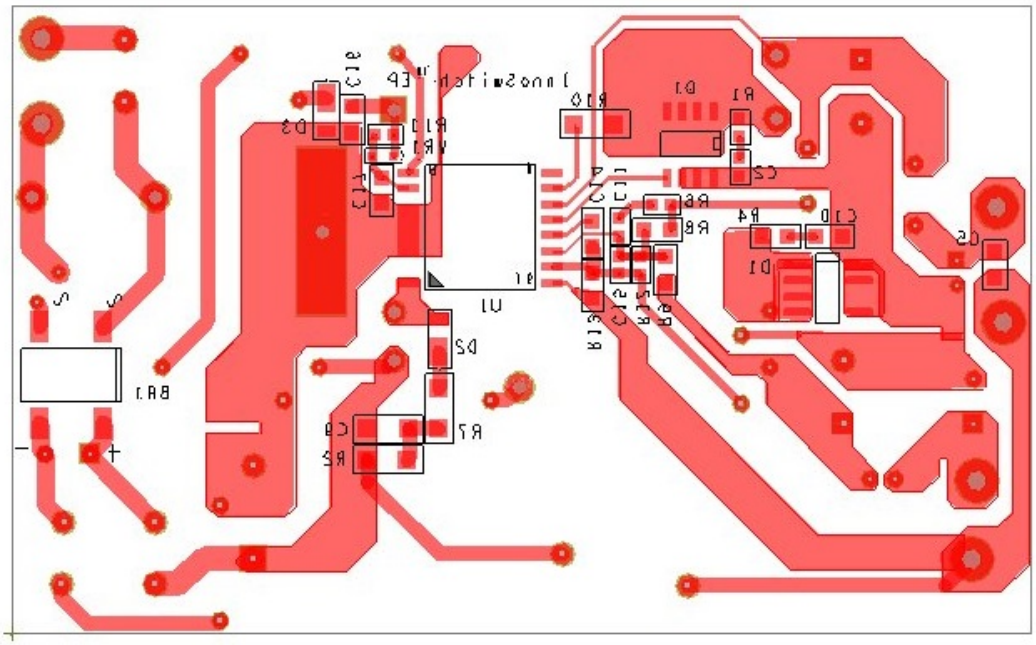

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, SMD, DFS	DF06S-E3/45	Vishay
2	1	C1	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
3	3	C2 C11 C15	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
4	1	C3	1000 µF, 10 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE100ELL102MJ16S	Nippon Chemi-Con
5	1	C4	47 µF, 16 V, Electrolytic, Low ESR, 500 mΩ, (5 x 11.5)	ELXZ160ELL470MEB5D	Nippon Chemi-Con
6	2	C5 C17	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
7	1	C6	100 nF, 275VAC, Film, X2	LE104-M	OKAYA
8	1	C7	68 µF, 100 V, Electrolytic, Gen. Purpose, (10 x 16)	UHE2A680MPD	Nichicon
9	1	C8	10 µF, 200 V, Electrolytic, (8 x 11)	UVY2D100MPD	Nichicon
10	1	C9	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
11	1	C10	47 pF, 1000 V, Ceramic, NPO, 0805	VJ0805A470JXGAT5Z	Vishay
12	1	C12	10 µF, 400 V, Electrolytic, (8 x 14)	EWH2GM100F14OT	Aishi
13	1	C13	33 µF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	EKMX401ELL330ML20S	Nippon Chemi-Con
14	1	C14	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
15	1	C16	22 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E226M125AC	TDK
16	1	D1	530 V, 3 A, D PACKAGE (SO-8C)	LXA03D530	Power Integrations
17	1	D2	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
18	1	D3	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
19	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
20	1	HS1	FAB, HEAT SINK, eSIP, DER504		Custom
21	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
22	1	JP2	Wire Jumper, Insulated, #24 AWG, 0.7 in	C2003A-12-02	Gen Cable
23	2	JP3 JP4	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
24	1	L1	15 mH, Common Mode Choke	TSD-3759	Premier Magnetics
25	1	L2	18 µH, 1.6 A, 9 x 12 mm H	AIUR-03-180K	Abracon
26	1	L3	3.3 µH, 1.5 A	11R332C	Murata
27	1	Q1	MOSFET, N-CH, 60V, 18A, 8SOIC	AO4260	Alpha & Omega Semi
28	1	R1	RES, 5.6 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ5R6V	Panasonic
29	1	R2	RES, 430 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ434V	Panasonic
30	1	R3	RES, 3.9 MΩ, 1%, 1/4 W, Metal Film	HHV-25FR-52-3M9	Yageo
31	1	R4	RES, 510 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ511V	Panasonic
32	1	R5	RES, 4.12 MΩ, 1%, 1/4 W, Metal Film	RNF14FTC4M12	Stackpole
33	1	R6	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
34	1	R7	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
35	1	R8	RES, 127 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1273V	Panasonic
36	1	R9	RES, 6.81 MΩ, 1%, 1/8 W, Thick Film, 0805	CRCW08056M81FKEA	Vishay-Dale
37	1	R10	RES, 47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
38	1	R11	RES, 6.8 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ682V	Panasonic
39	1	R12	RES, 32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
40	1	R13	RES, 0.01 Ω, 0.4 W, 1%, 0805	PF0805FRM7W0R01L	Yago
41	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
42	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer	P-803 POL-INN015	Pin Shine Premier Magnetics
43	1	U1	InnoSwitch-EP, Off-Line CV/CC Flyback Switcher	INN2605K	Power Integrations
44	1	VR1	8.2 V, 5%, 150 mW, SSMINI-2	DZ2S08200L	Panasonic

7 Transformer (T1) Specification

7.1 *Electrical Diagram*

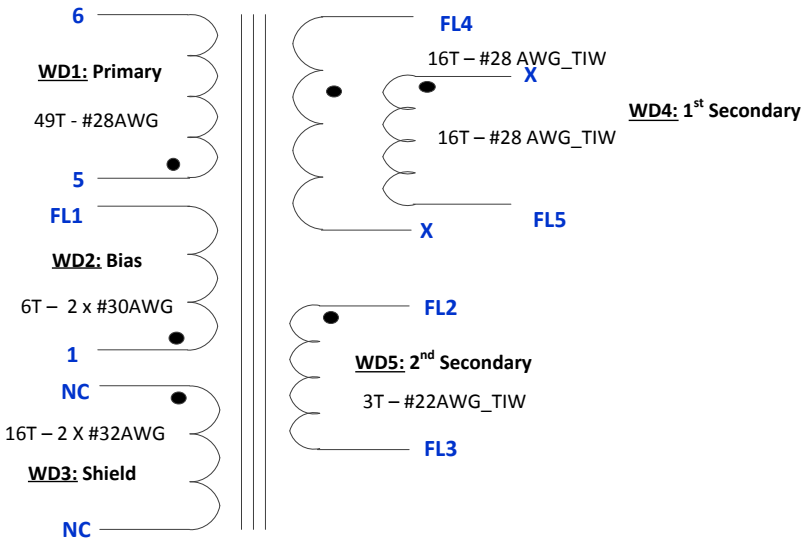

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 5 and 6, with all other windings open.	750 µH ±10%
Resonant Frequency	Between pin 5 and 6, other windings open.	1100 KHz (Min.)
Primary Leakage Inductance	Between pin 5 and 6, with FL1, FL2, FL4, FL5 shorted.	15 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: RM8, PC95 from TDK or DMR95 from DMEGC Magnetics.
[2]	Bobbin: RM8, Vertical,12 pins (6/6), In-line, (PI P/N: 25-00041-00).
[3]	Core Clip: Allstar Magnetic, P/N: CLI/P-RM8/I.
[4]	Magnet wire: #28 AWG, Double Coated.
[5]	Magnet wire: #30 AWG, Double Coated.
[6]	Magnet wire: #32 AWG, Double Coated.
[7]	Magnet wire: #22 AWG, Triple Insulated Wire.
[8]	Magnet wire: #28 AWG, Triple Insulated Wire.
[9]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 9.0 mm Wide.
[10]	Teflon tube: #26 AWG, Alpha Wire, P/N: TFT-20022.
[11]	Varnish: Dolph BC-359.

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7.4 *Transformer Build Diagram*

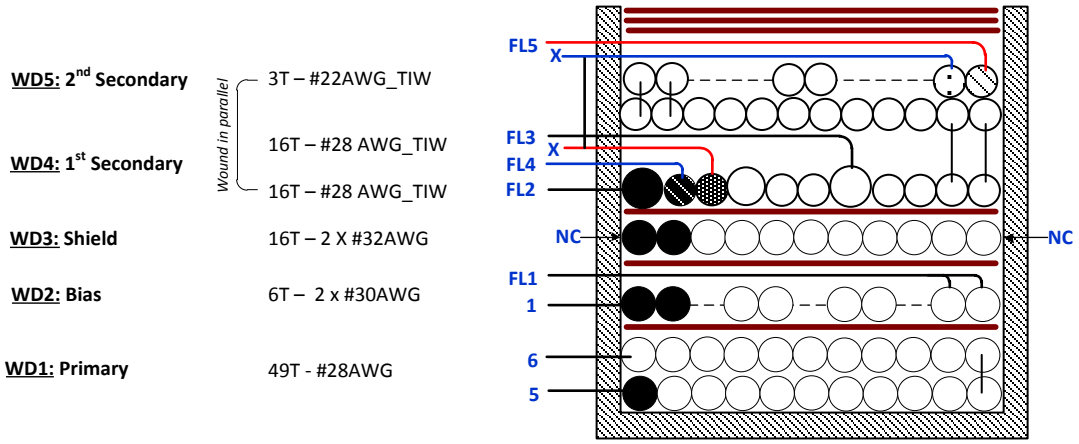
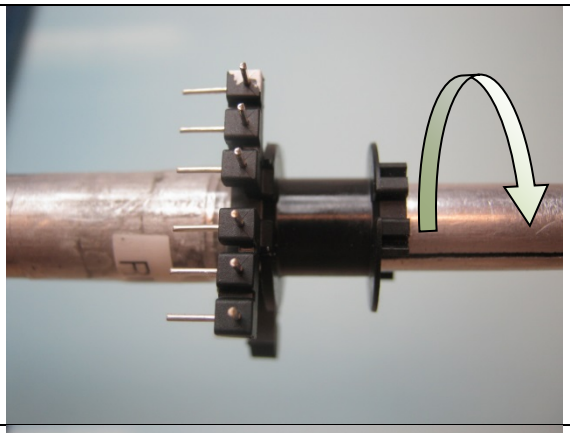
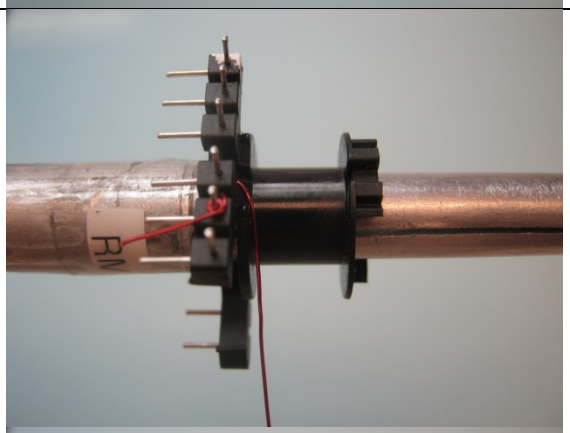
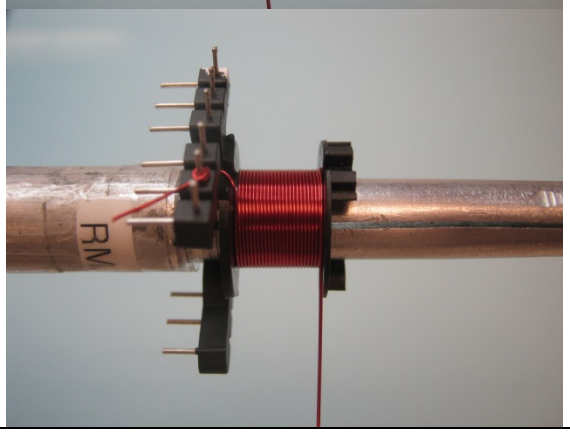


Figure 7 – Transformer Build Diagram.

7.5 *Winding Instructions*

Winding Preparation	Place the bobbin item [2] on the mandrel with the pin side is on the left side Winding direction is clockwise direction.
WD1 Primary	Start at pin 5, wind 49 turns of wire item [4] in 2 layers and finish at pin 6. It may have 1 or 2 turns on the 3rd layer.
Insulation	Place 1 layer of tape item [9] for insulation.
WD2 Bias	Start at pin 1, wind 6 bifilar turns of wire [5] in 1 layer, spread the wire evenly. At the last turn, bring the wire back to the left and leave ~1" floating and mark as FL1 for end lead.
Insulation	Place 1 layer of tape item [9] for insulation.
WD3 Shield	Use 2 wires item [6] temporarily hang on pin 3 as start lead, wind 16 bifilar turns. At the last turn cut short for no-connect, also cut short start lead for no-connect.
Insulation	Place 1 layer of tape item [9] for insulation.
WD4 & WD5 1st Secondary & 2nd Secondary	These windings will be wound in parallel, so prepare 3 wires as follow: - 1st wire, use wire item [7], start as FL2. - 2nd wire, use wire item [8], start as FL4. - 3rd wire, use wire item [8], start as X. Use these 3 wires, wind in parallel, at 3rd turn bring the 1st wire back to the left, leave ~1" floating and mark as FL3, then continue winding 13 turns in parallel for 2nd and 3rd wires approximately takes 2 ½ layers. At the last turn bring these wires to the left leave ~1" floating and mark as X and FL5 for 2nd and 3rd wire. Place 1 layer of tape item [9] for insulation. Solder to connect X to X from these wires, add Teflon tube item [10] for more insulation.
Insulation	Place 3 layers of tape item [9] for insulation and secure the windings.
Finish Assembly	Gap core halves to get 750 µH inductance and secure with clip item [3]. Cut short pins: 2, 3, 4 and all pins on secondary side. Varnish item [11].

7.6 *Winding Illustrations*

Winding Preparation		Place the bobbin item [2] on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**	 	Start at pin 5, wind 49 turns of wire item [4] in 2 layers and finish at pin 6. It may have 1 or 2 turns on the 3rd layer.

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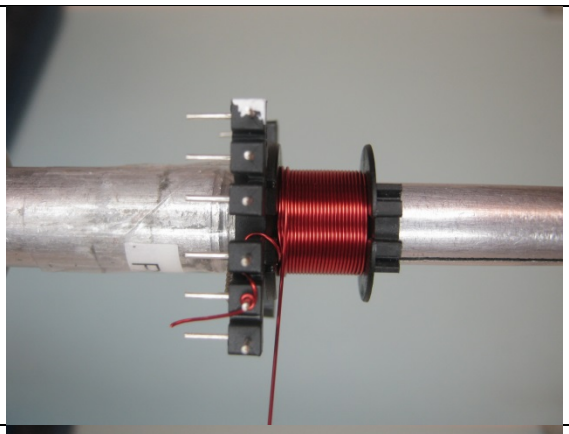
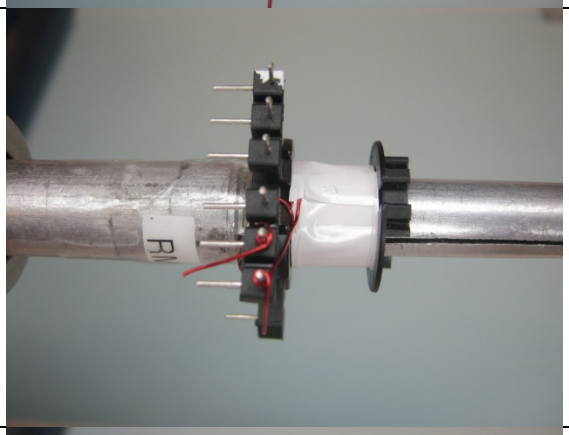
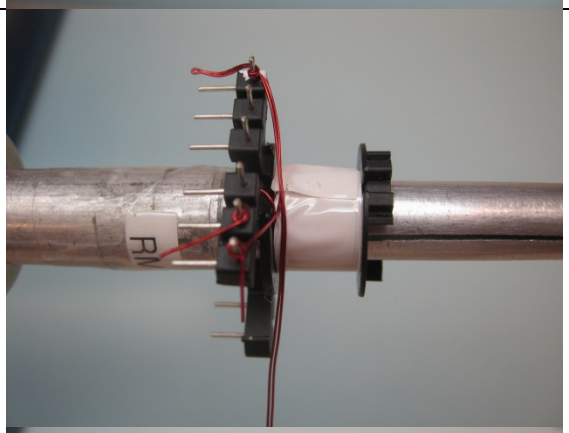
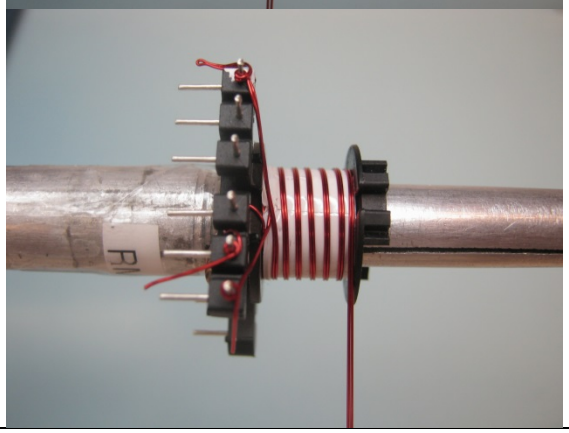
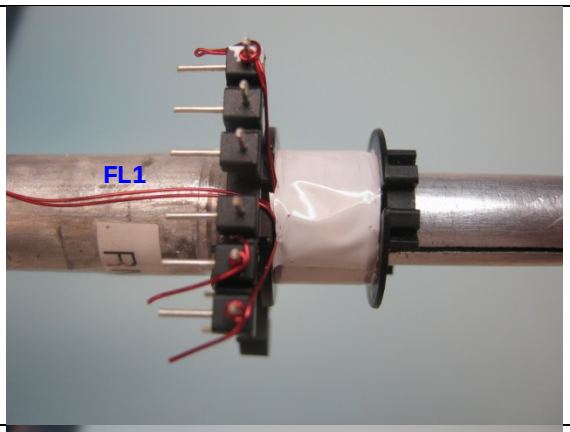
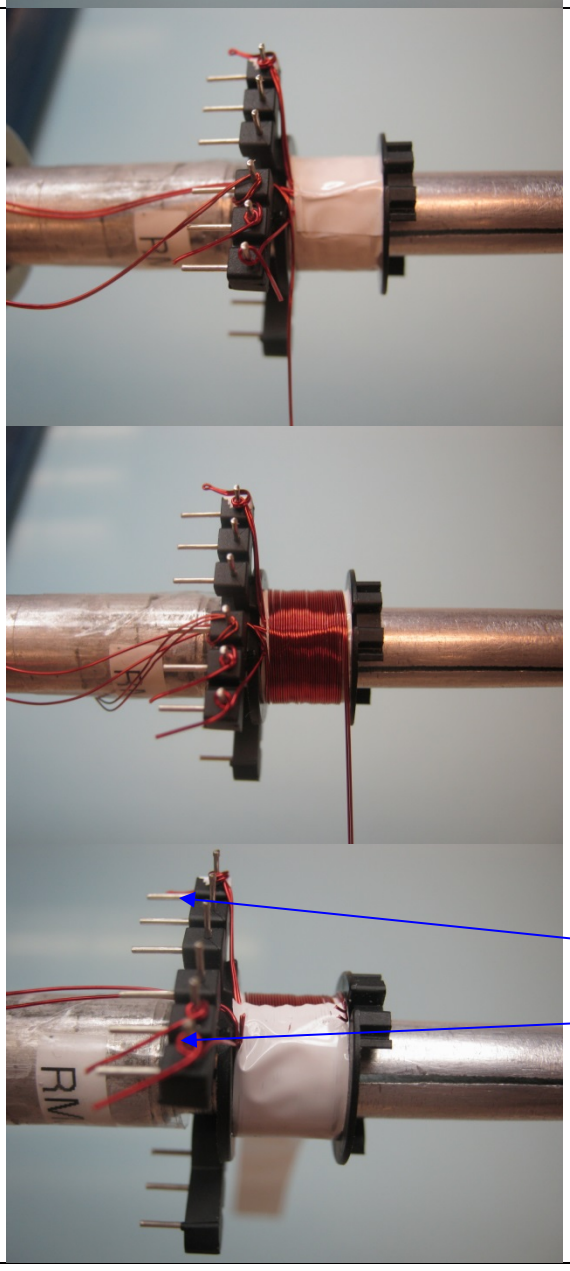
		
Insulation		Place 1 layer of tape item [9] for insulation.
WD2 **Bias**	 	Start at pin 1, wind 6 bifilar turns of wire [5] in 1 layer, spread the wire evenly. At the last turn, bring the wire back to the left and leave ~1” floating and mark as FL1 for end lead.

Insulation		Place 1 layer of tape item [9] for insulation.
WD3 Shield		Use 2 wires item [6] temporarily hang on pin 3 as start lead, wind 16 bifilar turns. <u>At the last turn cut short for no-connect, also cut short start lead for no-connect.</u>

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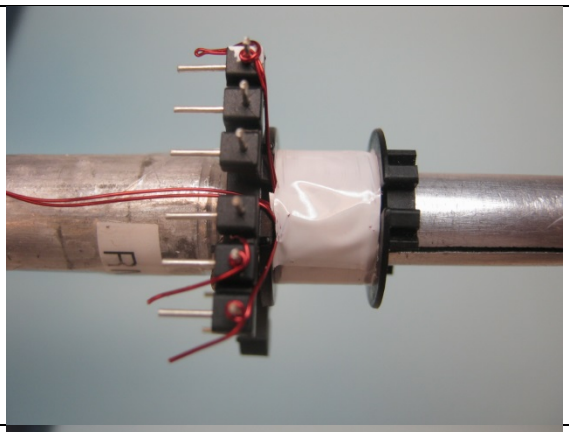
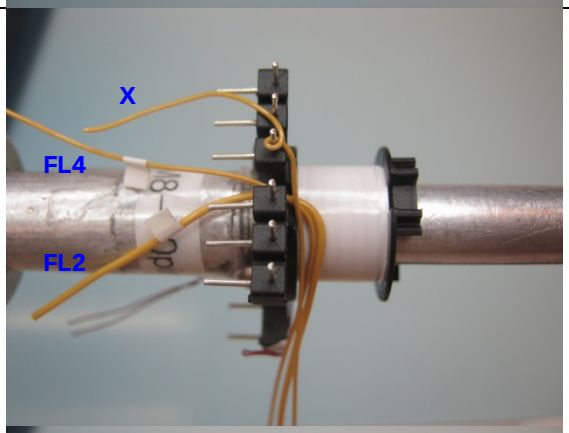
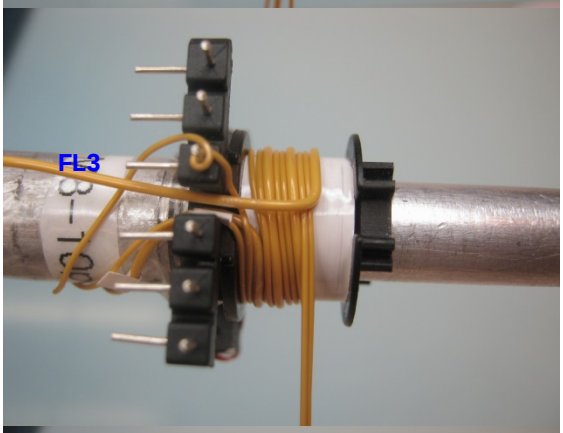
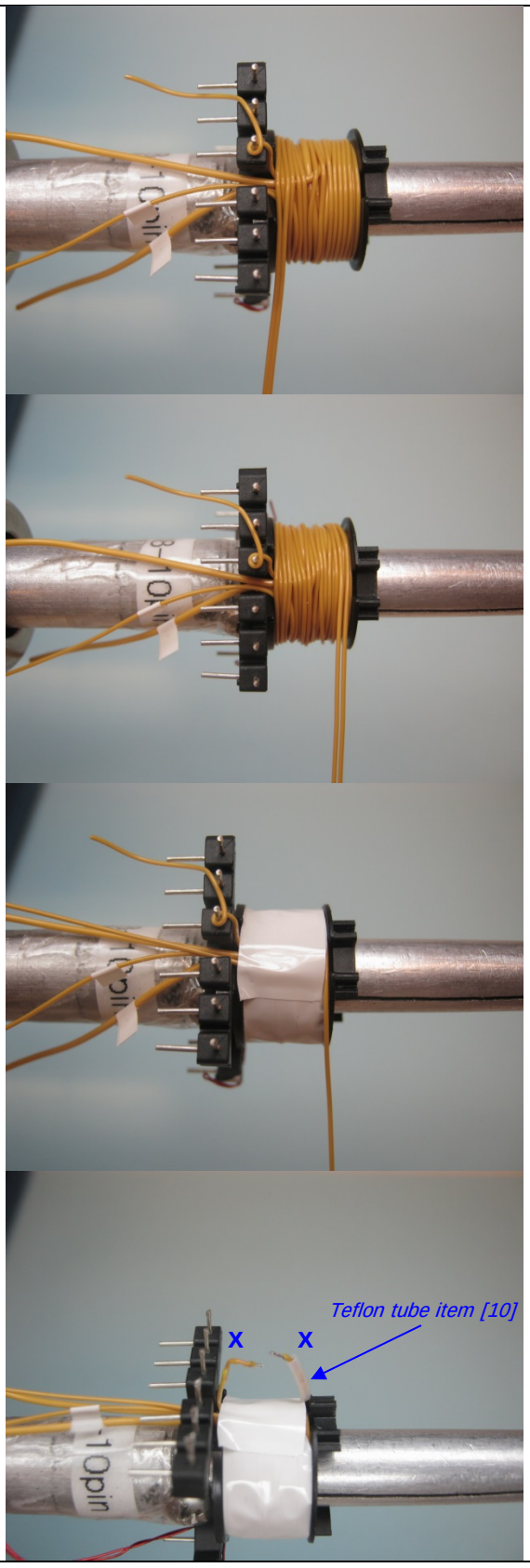
Insulation		Place 1 layer of tape item [9] for insulation.
WD4 & WD5 **1st Secondary & 2nd Secondary**	  	These windings will be wound in parallel, so prepare 3 wires as follow: - 1st wire, use wire item [7], start as FL2. - 2nd wire, use wire item [8], start as FL4. - 3rd wire, use wire item 8], start as X. Use these 3 wires, wind in parallel, at 3rd turn bring the 1st wire back to the left, leave ~1" floating and mark as FL3, then continue winding 13 turns in parallel for 2nd and 3rd wires approximately takes 2 ½ layers. At the last turn bring these wires to the left leave ~1" floating and mark as X and FL5 for 2nd and 3rd wire. Place 1 layer of tape item [9] for insulation. Solder to connect X to X from these wires, add Teflon tube item [10] for more insulation.



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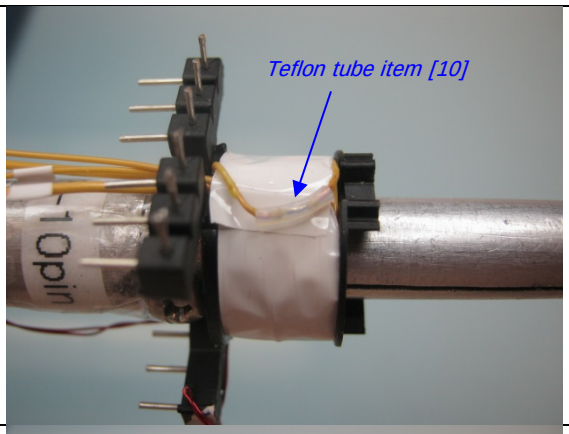
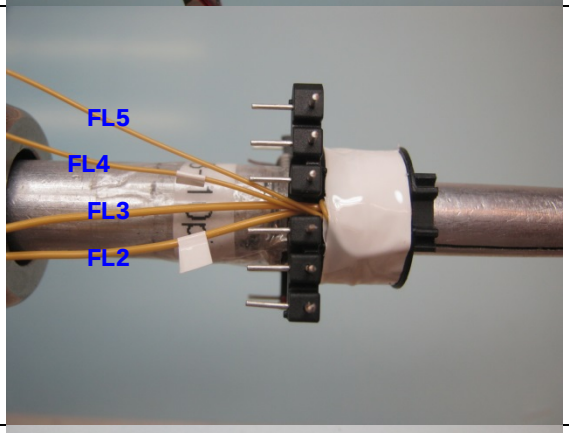
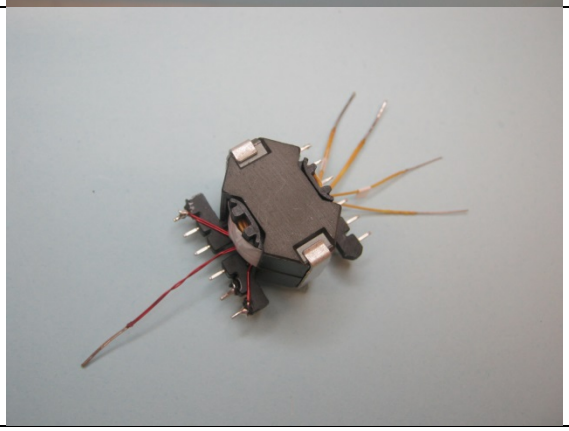
		
Insulation		Place 3 layers of tape item [9] for insulation and secure the windings.
Finish Assembly		Gap core halves to get 750 µH inductance and secure with clip item [3]. Cut short pins: 2, 3, 4 and all pins on secondary side. Varnish item [11].

8 15 mH Common Mode Choke (L1) Specification

8.1 *Electrical Diagram*

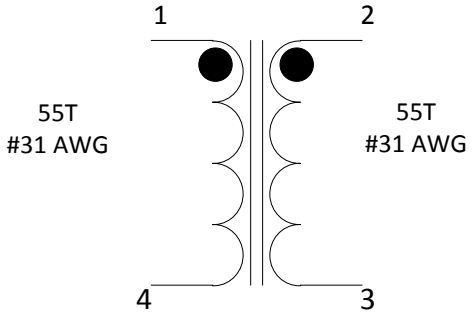


Figure 8 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	13 mH ±25%
Core Effective Inductance		4960 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	80 μH

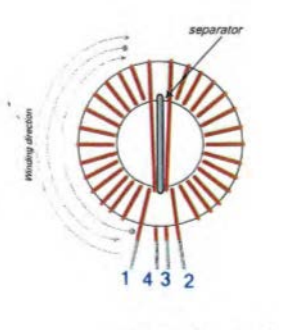
8.3 *Material List*

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID T14 x 8 x 5.5. PI Part number: #32-00286-00.
	Divider -- Fish paper, insulating cotton rag, 0.010” thick, PI #: 66-00042-00. Cut to size 8 mm x 5.5 mm.
[2]	Magnet Wire: #31 AWG Heavy Nyleze.

8.4 *Winding Instructions*

- Use 4 ft of item [2], start at pin 1 wind 55 turns end at pin 4.
- Do the same for another half of toroid, start at pin 2 and end at pin 3.

8.5 *Illustrations*



Top View.

Front View.

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch-CH_102014; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch-CH_101714_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	55.00		55.00	V	Output Voltage (continuous power at the end of the cable)
IO	0.46		0.46	A	Power Supply Output Current (corresponding to peak power)
Power		**Info**	25.3	W	Specified Output Power exceeds the value specified on the datasheet for universal input adapter. Please verify performance on bench
n	0.87		0.87		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	43.00		43.00	uFarad	Input Capacitance
ENTER InnoSwitch-CH VARIABLES					
InnoSwitch-CH	**Auto**		**INN20x5**		Recommended InnoSwitch-CH
Cable drop compensation	**0%**		**0%**		Select Cable Drop Compensation option
Complete Part Number			**INN2005K**		Final part number including package
Chose Configuration	**INC**		**Increased Current Limit**		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.955	A	Minimum Current Limit
ILIMITTYP			1.050	A	Typical Current Limit
ILIMITMAX			1.145	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			92.61	A^2kHz	Worst case I2F parameter across the temperature range
VOR	85		85	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.59		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.36		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			5.81	V	Bias Winding Number of Turns
PIVB			74.19	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM8**		**RM8**		Enter Transformer Core
Core			PC47RM8Z-12		Enter core part number, if necessary
Bobbin			BRM8-718CPFR		Enter bobbin part number, if necessary
AE			0.640	cm^2	Core Effective Cross Sectional Area
LE			3.80	cm	Core Effective Path Length
AL			1950	nH/T^2	Ungapped Core Effective Inductance
BW			9.05	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)

L	2		2		Number of Primary Layers
NS	32		32		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			82	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.35	A	Average Primary Current
IP			0.955	A	Peak Primary Current assuming ILIMITMIN
IR			0.564	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.50	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			742	uHenry	Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 705 uH
LP_TOLERANCE	5.0		5.0	%	Primary inductance tolerance
NP			49		Primary Winding Number of Turns
ALG			309	nH/T^2	Gapped Core Effective Inductance
BM			2965	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			876	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			921		Relative Permeability of Ungapped Core
LG			0.22	mm	Gap Length (Lg > 0.1 mm)
BWE			18.1	mm	Effective Bobbin Width
OD			0.37	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.31	mm	Bare conductor diameter
AWG			29	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			128	Cmils	Bare conductor effective area in circular mils
CMA			255	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.46	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			0.73	A	Secondary RMS Current
IRIPPLE			0.57	A	Output Capacitor RMS Ripple Current
CMS			146	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			28	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			573	V	Maximum Drain Voltage Estimate
PIVS			400	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			55.00	V	Main Output Voltage directly after output rectifier
IO1			0.46	A	Output DC Current
PO1			25.30	W	Output Power
VD1			0.10	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			32.00	Turns	Output Winding Number of Turns
ISRMS1			0.73	A	Output Winding RMS Current
IRIPPLE1			0.57	A	Output Capacitor RMS Ripple Current
PIVS1			400	V	Output Rectifier Maximum Peak Inverse Voltage,

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					assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
Recommended MOSFET			**Si7456**		Recommended SR FET for this output
RDSON_HOT			0.042	Ohm	RDSon at 100C
VRATED			100	V	Rated voltage of selected SR FET
CMS1			146	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			28	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.32	mm	Minimum Bare Conductor Diameter
ODS1			0.28	mm	Maximum Outside Diameter for Triple Insulated Wire

10 Performance Data

10.1 *Full Load Efficiency vs. Line*

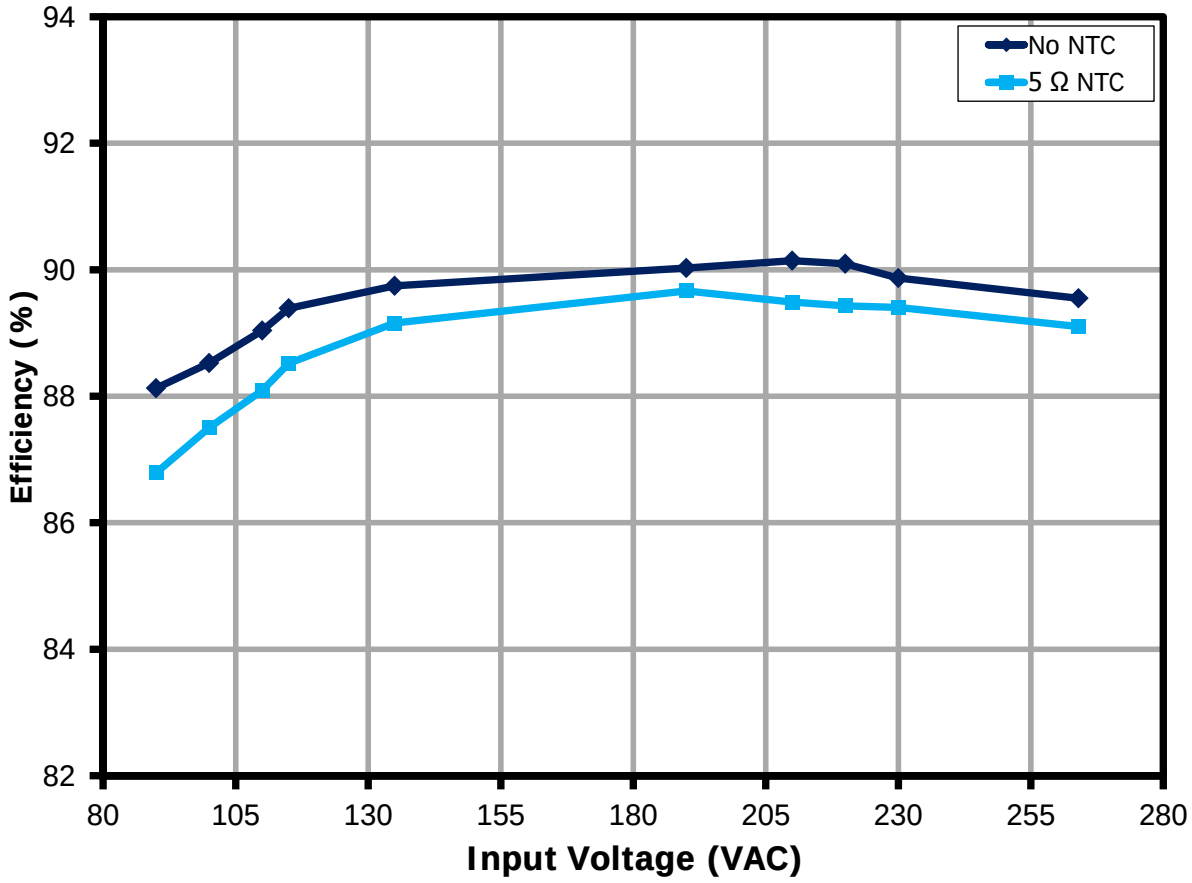

Figure 9 – Full load Efficiency vs. Line Voltage, Room Temperature.

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10.2 *Efficiency vs. Load (0.1 A – 0.32 A on 55 V, Full Load on 5 V)*

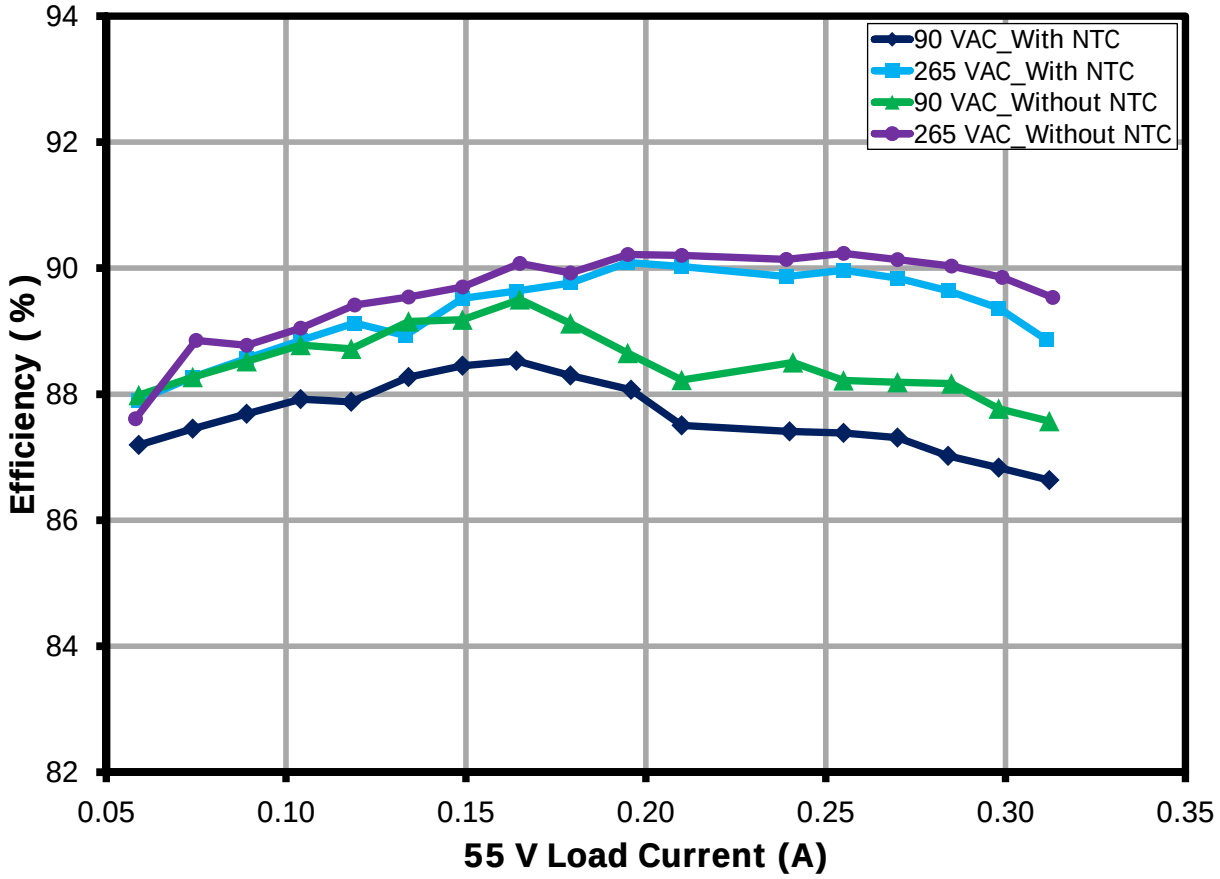

Figure 10 – Efficiency vs. Load, Room Ambient.

10.3 *Efficiency vs. Load (0.1 A – 0.32 A on 55 V, No-Load on 5 V)*

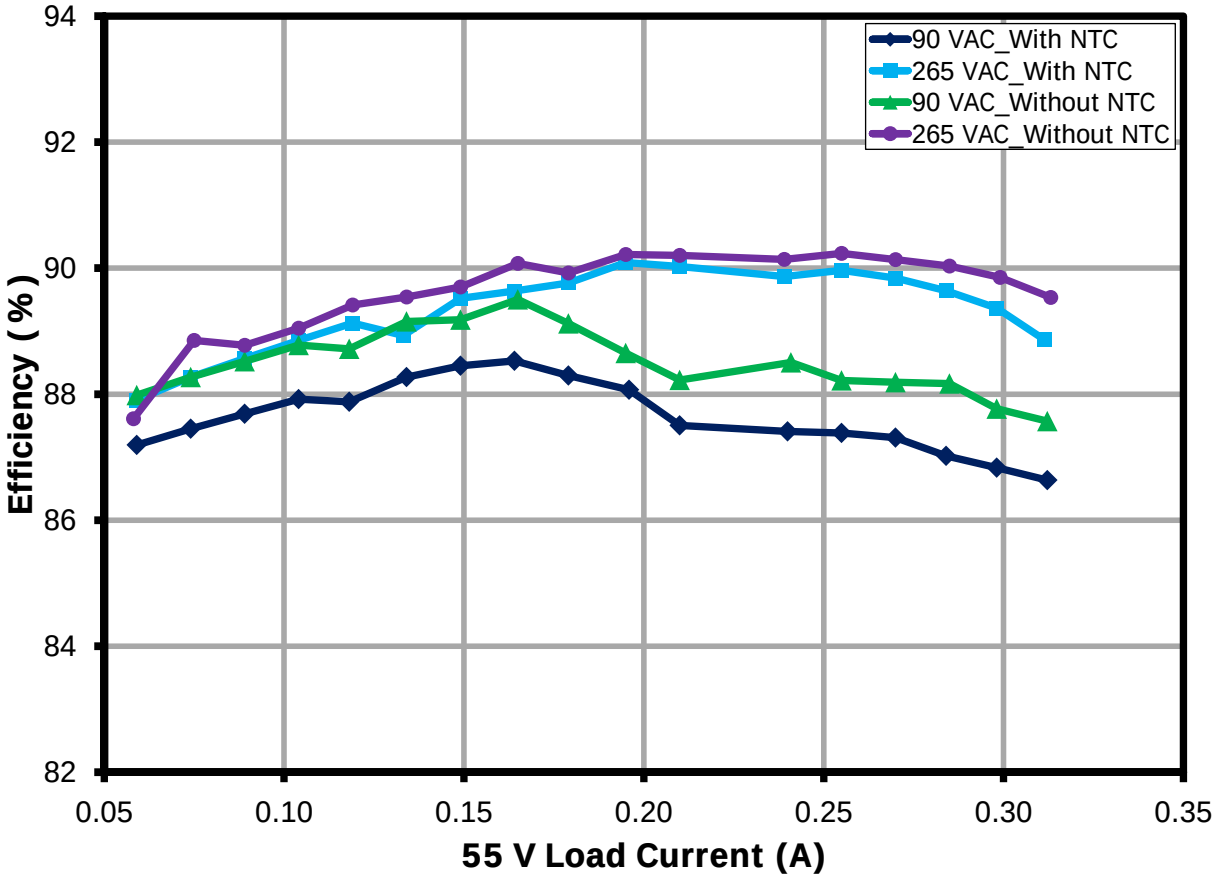

Figure 11 – Efficiency vs. Load.

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10.4 *No-Load Input Power*

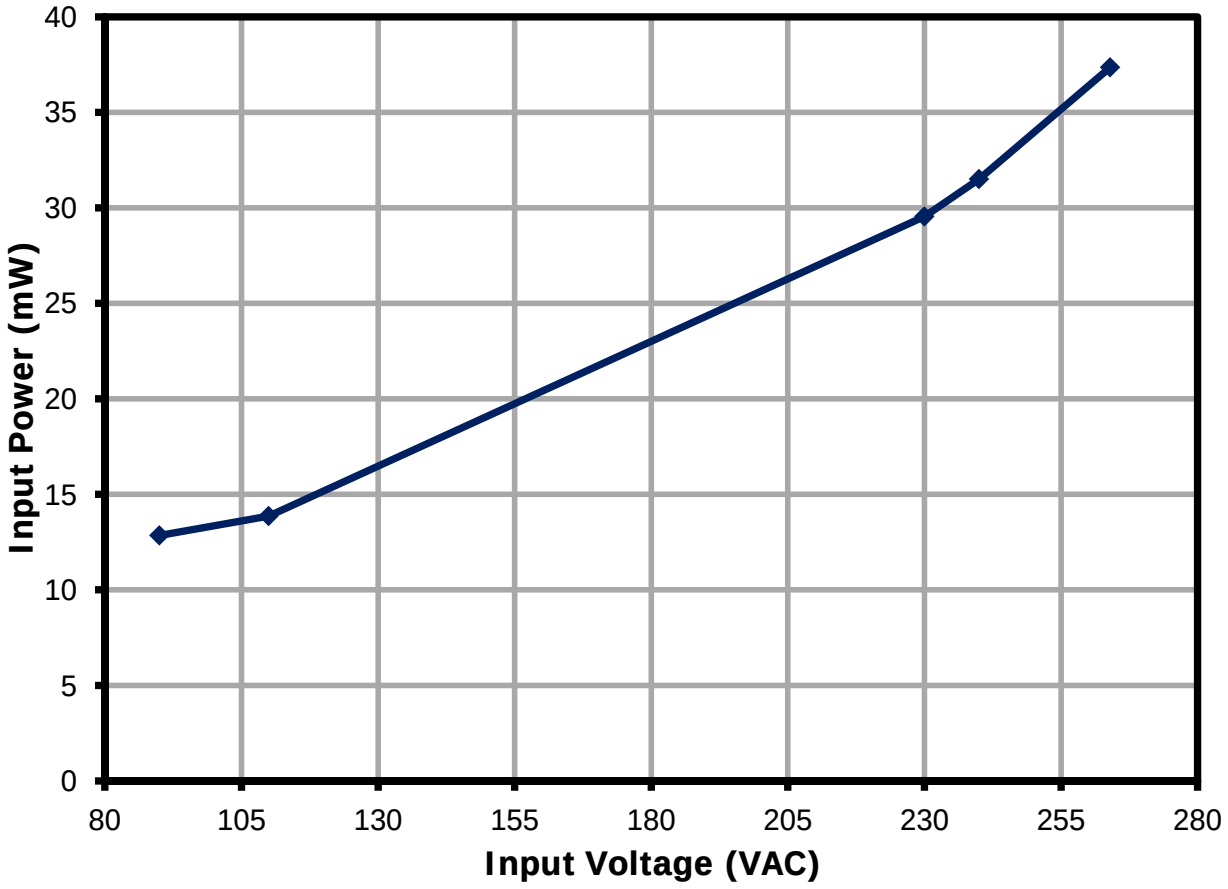
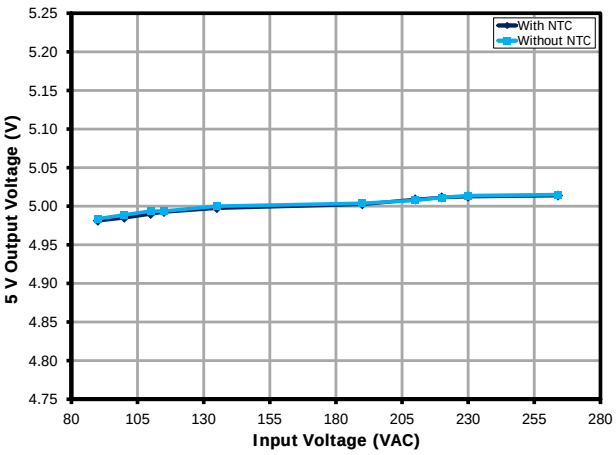
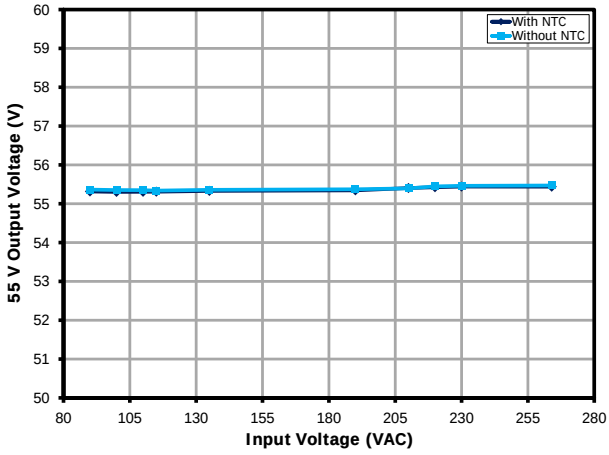


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.5 *Line and Load Regulation*

10.5.1 Line Regulation (Full Load)





	5 V	55 V
Min	4.98	55.30
Max	5.01	55.44

Figure 13 – Output Voltage vs. Input Line Voltage, Room Temperature.

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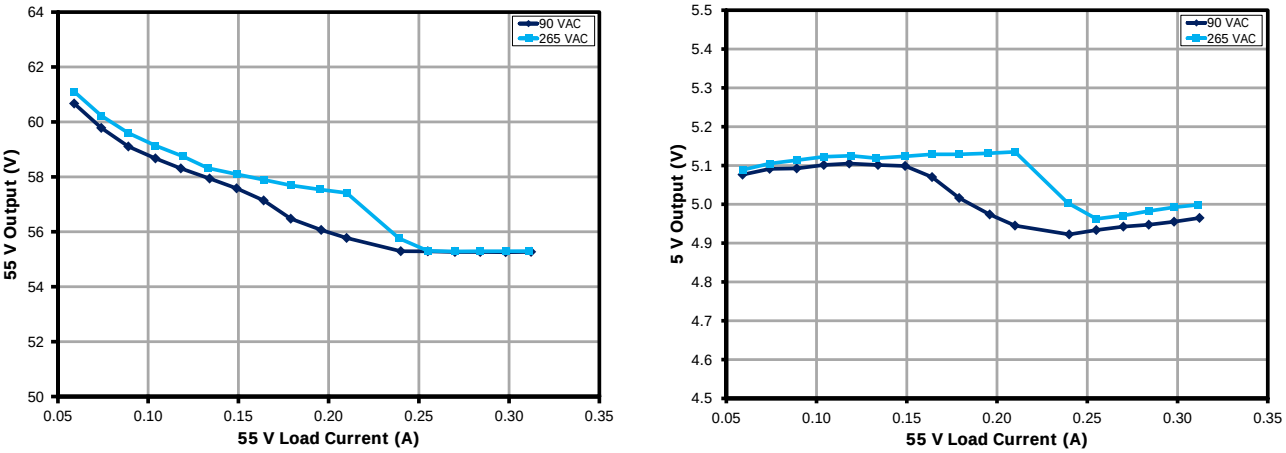
10.5.2 Cross Regulation

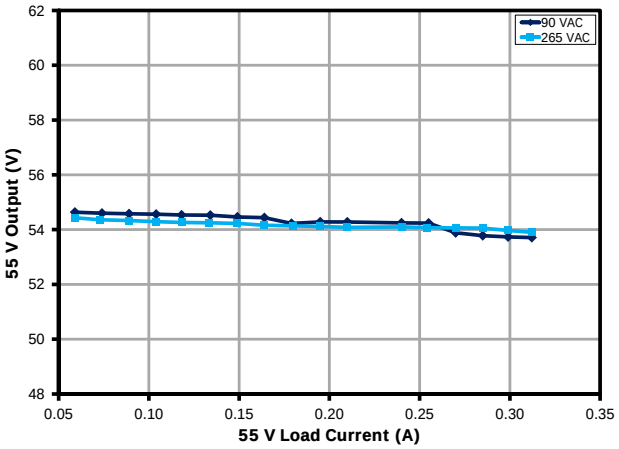
10.5.2.1 55 V Load Change with Full Load on 5 V

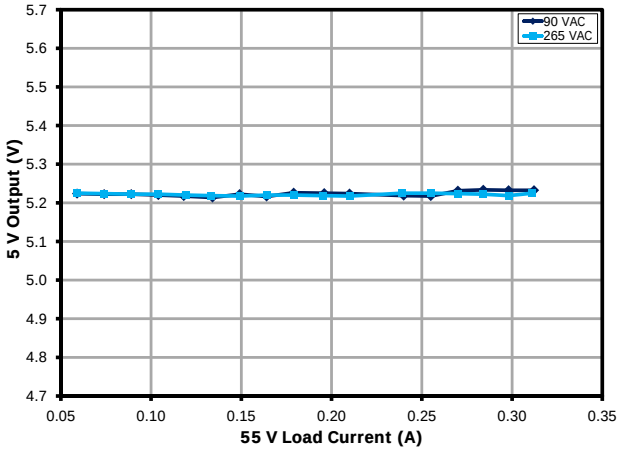


	55 V	5 V
Min	55.26	4.92
Max	61.10	5.14

Figure 14 – Output Voltages vs. 55 V Load, Room Temperature.

10.5.2.2 55 V Load Change with No Load on 5 V





	55 V	5 V
Min	53.71	5.21
Max	54.64	5.23

Figure 15 – Output Voltages vs. 55 V Load, Room Temperature.

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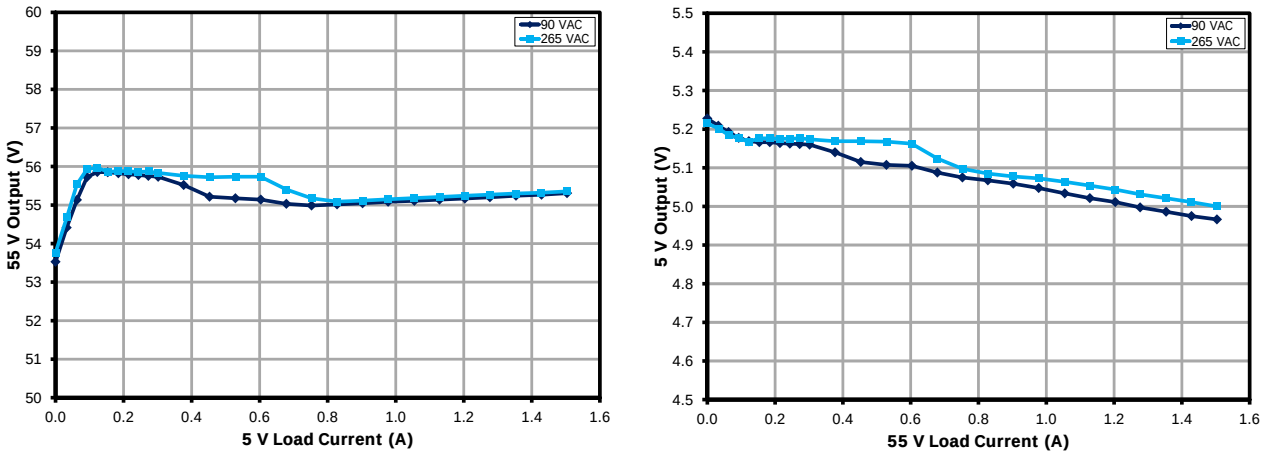
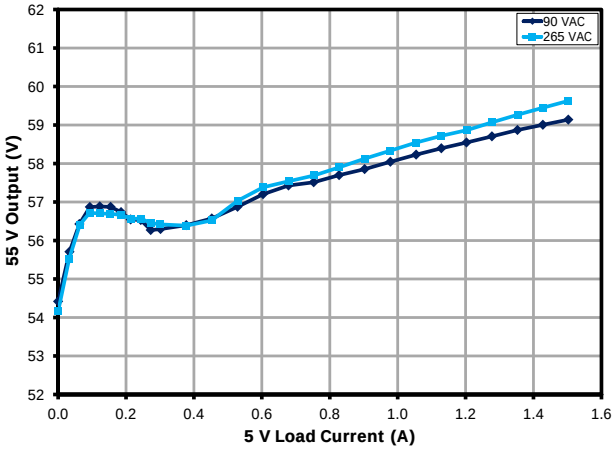
10.5.2.3 5 V Load Change with Full Load on 55 V

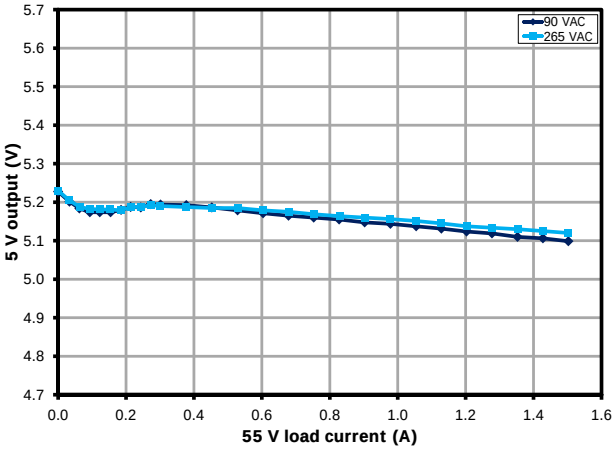


	55 V	5 V
Min	4.97	53.53
Max	5.23	55.97

Figure 16 – Output Voltages vs. 5 V Load, Room Temperature.

10.5.2.4 5 V Load Change with 0.1 A on 55 V





	55 V	5 V
Min	5.10	54.16
Max	5.23	59.45

Figure 17 – Output Voltages vs. 5 V Load, Room Temperature**.**

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11 Thermal Performance

11.1 *90 VAC*

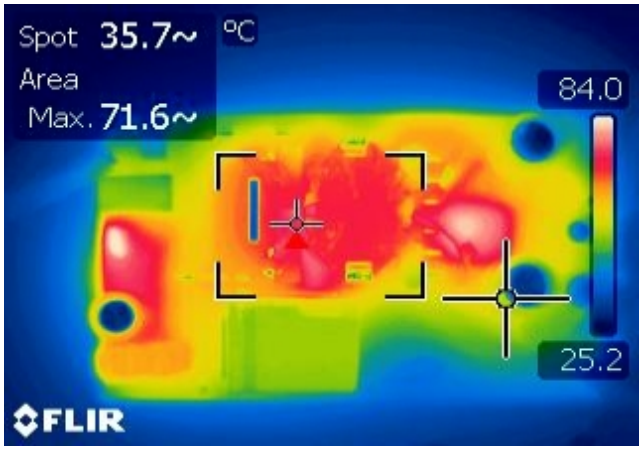

Figure 18 – Transformer Side. 85 VAC, Full Load.

	Reference	°C
Ambient		26.9
Transformer	T1	64.5
Input Capacitor	C13	47.3
55 V Choke	L2	44.9
5 V Choke	L3	52.8

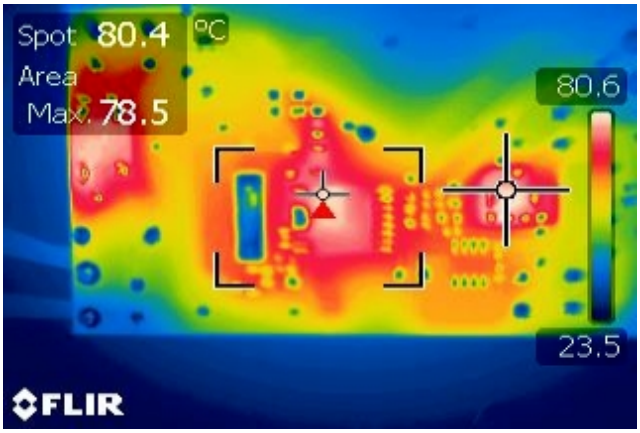

Figure 19 – InnoSwitch-EP Side. 85 VAC, Full Load.

	Reference	°C
Ambient		25
InnoSwitch-EP	U1	78.5
55V Rectifier	D1	80.4
SR FET Q1	Q2	60.5
Bridge	BR1	66.2

11.2 *110 VAC*

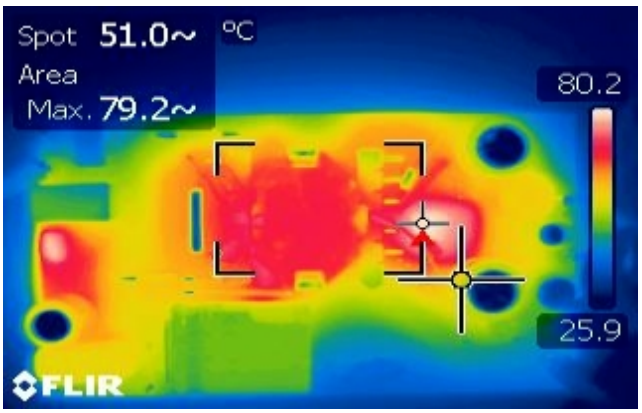

Figure 20 – Transformer Side. 110 VAC, Full Load.

	Reference	°C
Ambient		26.8
Transformer	T1	65.6
Input Capacitor	C13	45
55 V Choke	L2	42.2
5 V Choke	L3	52.8

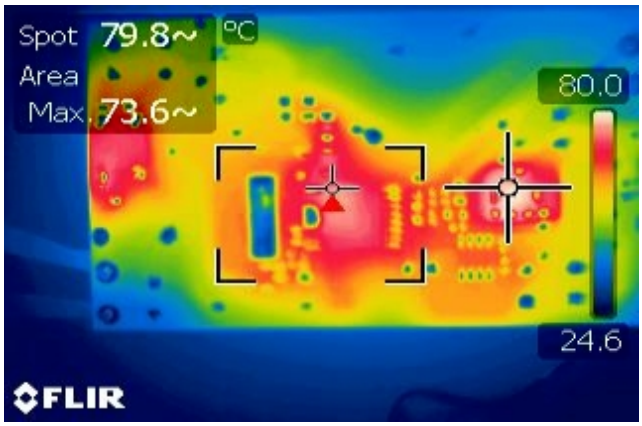

Figure 21– InnoSwitch-EP Side. 110 VAC, Full Load.

	Reference	°C
Ambient		25.2
InnoSwitch-EP	U1	73.6
55V Rectifier	D1	79.8
SR FET Q1	Q2	59.3
Bridge	BR1	58.8

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11.3 *230 VAC*

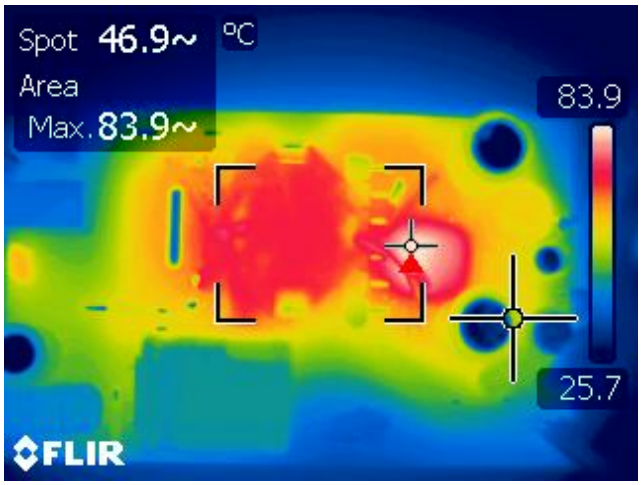

Figure 22 – Transformer Side. 230 VAC, Full Load.

	Reference	°C
Ambient		26.9
Transformer	T1	64
Input Capacitor	C13	40.8
55 V Choke	L2	42
5 V Choke	L3	50

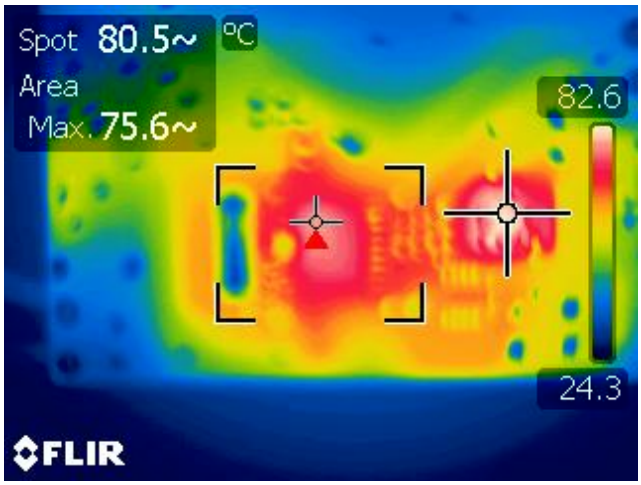

Figure 23 – InnoSwitch-EP Side. 230 VAC, Full Load.

	Reference	°C
Ambient		25.6
InnoSwitch-EP	U1	75.6
55V Rectifier	D1	80.5
SR FET Q1	Q2	60
Bridge	BR1	44.1

11.4 *265 VAC*

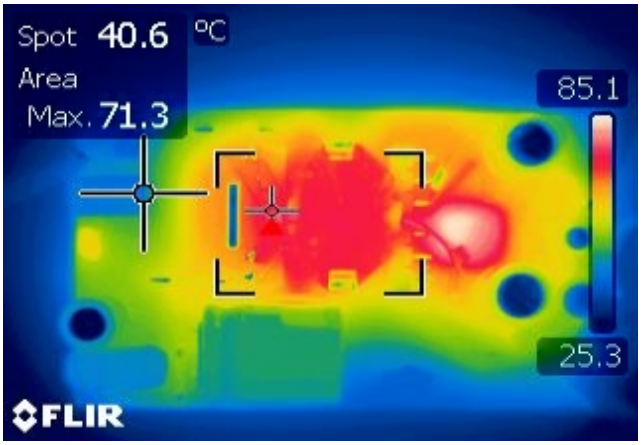

Figure 24 – Transformer Side. 265 VAC, Full Load.

	Reference	°C
Ambient		26.0
Transformer	T1	64.5
Input Capacitor	C13	40.5
55 V Choke	L2	42
5 V Choke	L3	52.6

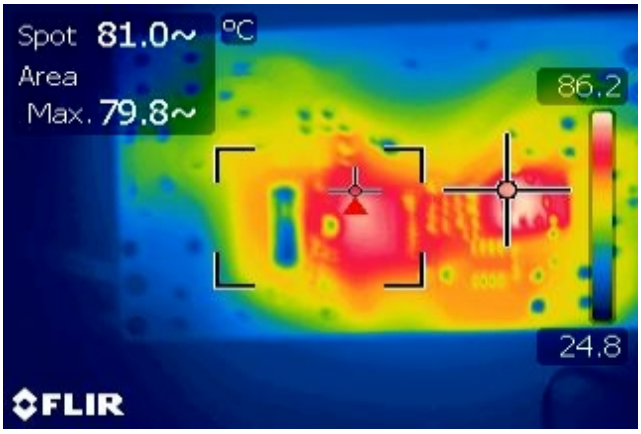

Figure 25 – InnoSwitch-EP Side. 265 VAC, Full Load.

	Reference	°C
Ambient		25.6
InnoSwitch-EP	U1	79.8
55V Rectifier	D1	81
SR FET Q1	Q2	60
Bridge	BR1	44

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12 Waveforms

12.1 *Load Transient Response*

12.1.1 55 V load Transient

Figure 26 – 0.1 A – 0.32 A, 55 V Load Step Transient Response, 90 VAC.
5 V_{MIN}: 4.86 V. 5 V_{MAX}: 5.09 V.
55 V_{MIN}: 54.3 V. 55 V_{MAX}: 59.7 V.
Upper: 55 V_{OUT}, 10 V / div.
Middle: 5 V_{OUT}, 0.5 V / div.
Lower: 55 V Load, 0.2 A, 100 ms / div.

Figure 27 – 0.1 A – 0.32 A, 55 V Load Step Transient Response. 265 VAC.
5 V_{MIN}: 4.91 V. 5 V_{MAX}: 5.11 V.
55 V_{MIN}: 54.3 V. 55 V_{MAX}: 60 V.
Upper: 55 V_{OUT},10 V / div.
Middle: 5 V_{OUT}, 0.5 V / div.
Lower: 55 V Load, 0.2 A, 100 ms / div.

12.2 *Switching Waveforms*

12.2.1 InnoSwitch-EP Drain and Current Waveforms

Figure 28 – Drain Voltage and Current Waveforms.
90 VAC Input, Full Load.
Upper: V_{DRAIN}, 200 V, 5 ms, 20 µs / div.
Lower: I_{DRAIN}, 1 A / div.

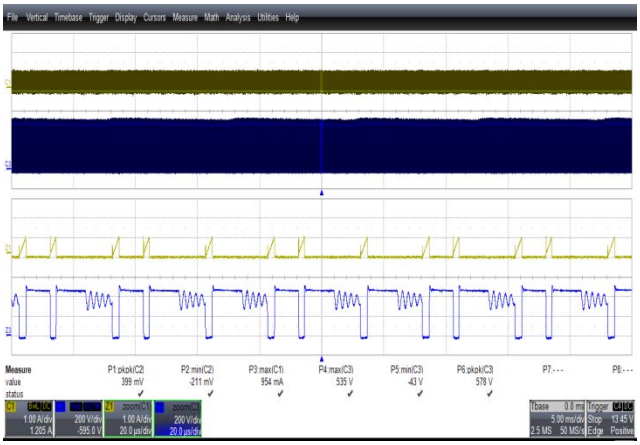

Figure 29 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (535 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 ms, 20 µs / div.
Lower: I_{DRAIN}, 1 A / div.

12.2.2 InnoSwitch-EP Drain and Current Waveforms Start-up and Shorted Output

Start-Up

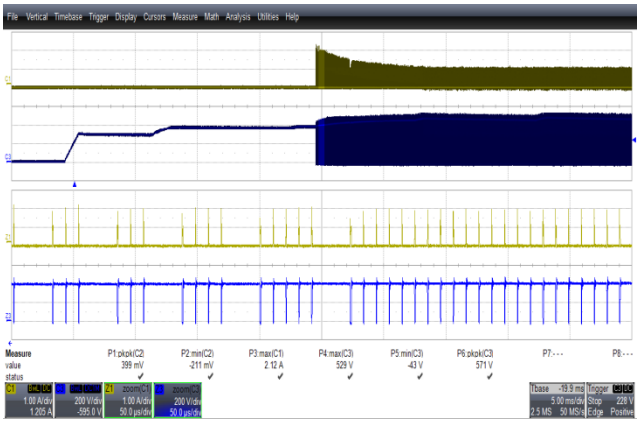

Figure 30 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (529 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 ms, 50 µs / div.
Lower: I_{DRAIN}, 1 A / div.

Shorted Output

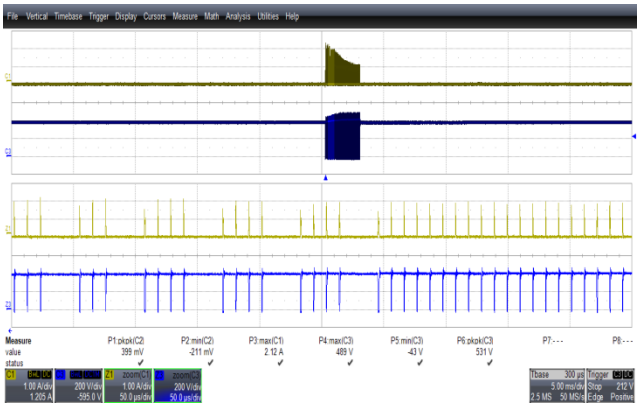

Figure 31 – Drain Voltage and Current Waveforms.
265 VAC Input, (489 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 ms, 50 µs / div.
Lower: I_{DRAIN}, 1 A / div.

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12.2.3 SR FET and Output Diode Waveforms

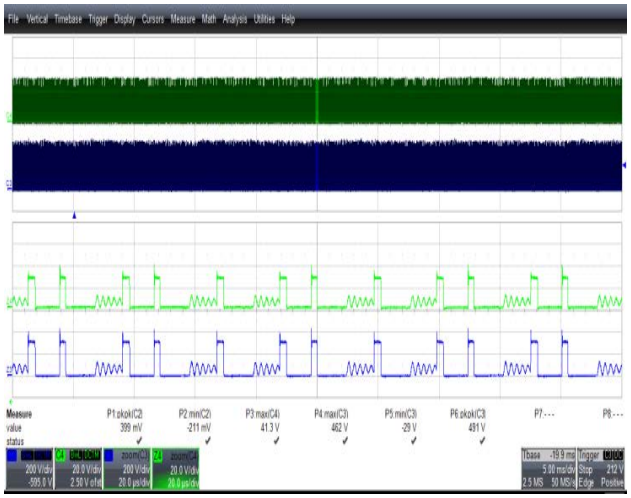

Figure 32 – SR FET and Output Diode Voltage Waveforms.
265 VAC Input, Full Load.
(462 V_{MAX} for 55 V, 41.3 V_{MAX} for 5 V.)
Upper: 5 V, 20 V /, 5 ms, 20 µs / div.
Lower: 55 V, 200 V / div.

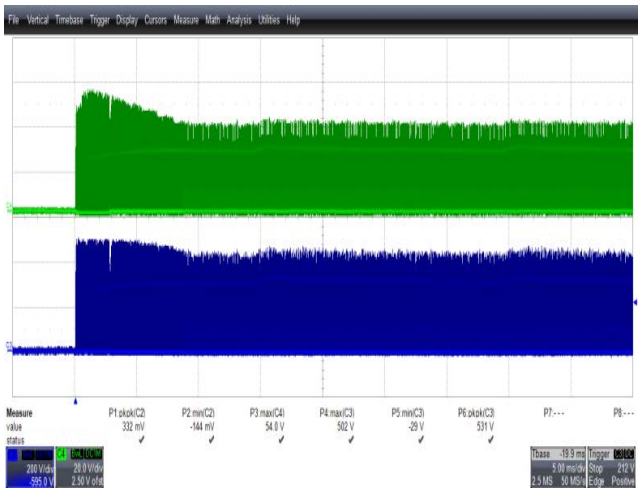

Figure 33 – SR FET and Output Diode Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
Upper: 5 V, 20 V /, 5 ms / div.
Lower: 55 V, 200 V / div.

12.2.4 Output Voltage and Current Waveforms at Start-up

12.2.4.1 Full load

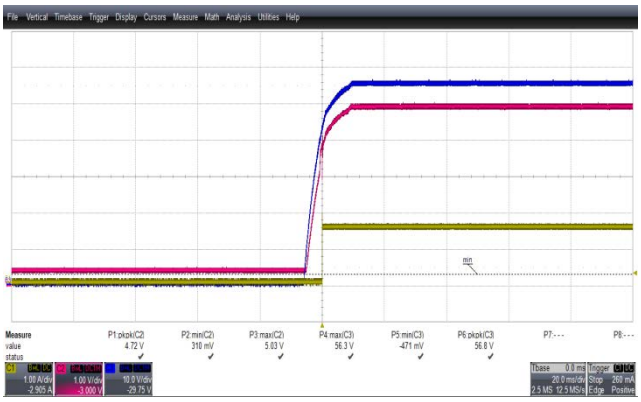

Figure 34 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V, 1 V / div.
Middle: 55 V, 10 V.
Lower: I_{OUT}, 1 A / div. 20 ms / div.

Figure 35 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V, 1 V / div.
Middle: 55 V, 10 V.
Lower: I_{OUT}, 1 A / div. 20 ms / div.

12.2.4.2 No-Load

Figure 36 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 5 V, 1 V / div.
Middle: 55 V, 10 V, / div.
Lower: I_{OUT}, 1 A, 20 ms / div.

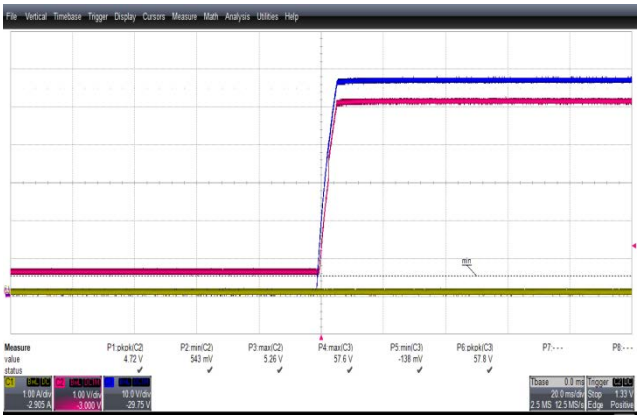

Figure 37 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V, 2 V / div.
Middle: 55 V, 10 V / div.
Lower: I_{OUT}, 1 A, 20 ms / div.

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12.2.5 Output Voltage and Current Waveforms with Shorted Output

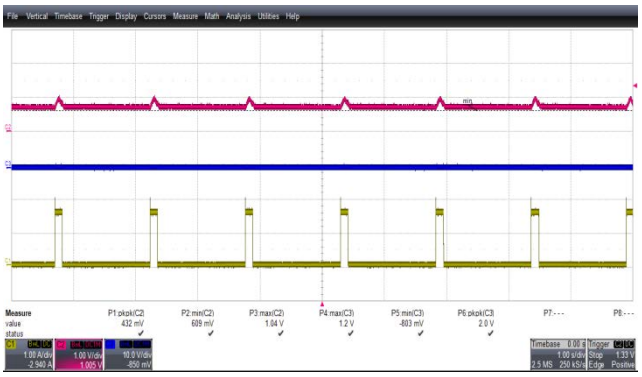

Figure 38 – Output Voltage and Current Waveforms.
90 VAC Input.
Upper: 5 V, 1 V, / div.
Middle: 55 V, 10 V / div.
Lower: I_{OUT}, 1 A , 1 s / div.

Figure 39 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V, 1 V, / div.
Middle: 55 V, 10 V / div.
Lower: I_{OUT}, 1 A , 1 s / div

12.2.6 Output Voltage and Current Waveforms with Open 5 V Feedback

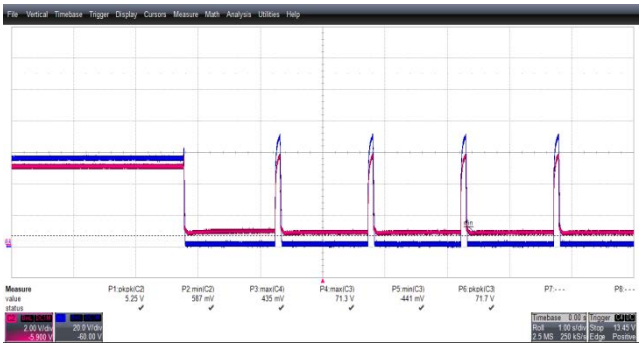

Figure 40 – Output Voltage Waveform.
90 VAC Input.
Upper: 55 V, 20 V / div.
Lower: 5 V, 2 V / 1 s / div.

Figure 41 – Output Voltage Waveform.
265 VAC Input.
Upper: 55 V, 20 V / div.
Lower: 5 V, 2 V / 1 s / div.

12.3 *Output Ripple Measurements*

12.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/100 V ceramic type and one (1) 1 μF/100 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

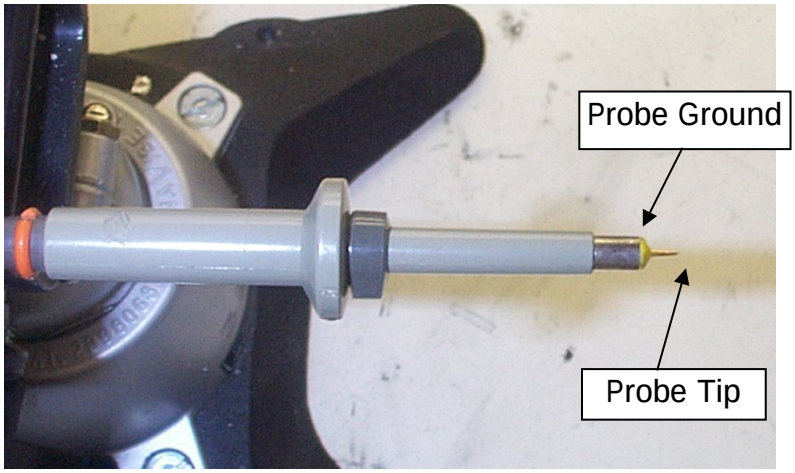

Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

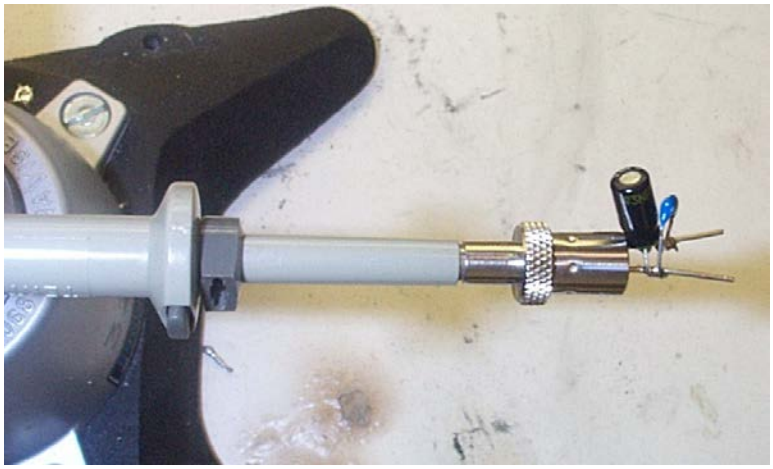

Figure 43 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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12.3.2 Ripple Voltage Waveforms

12.3.2.1 0.32 A Load on 55 V

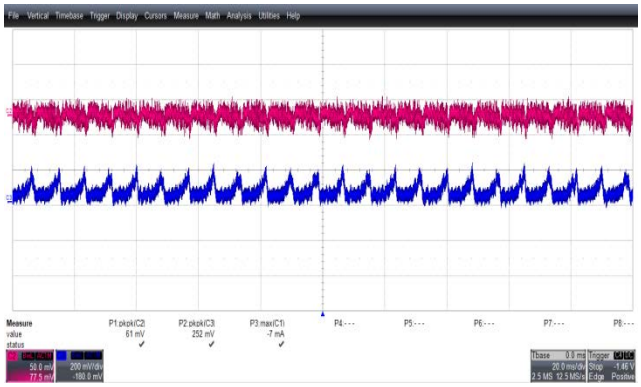

Figure 44 – Output Voltage ripple Waveforms.
90 VAC Input. 1.5 A on 5 V and 0.32 A on 55 V.
Upper: 5 V, 50 mV / div.
Lower: 55 V, 200 mV, 20 ms / div.

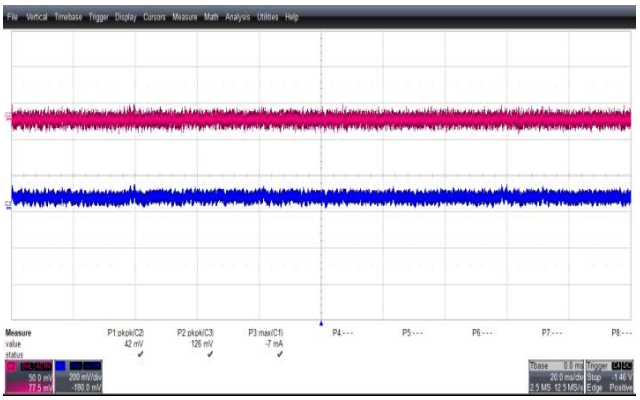

Figure 45 – Output Ripple Voltage Waveforms**.**
265 VAC Input. 1.5 A on 5 V and 0.32 A on 55 V.
Upper: 5 V, 50 mV / div.
Lower: 55 V, 200 mV , 20 ms / div.

12.3.2.2 0.1 A Load on 55 V

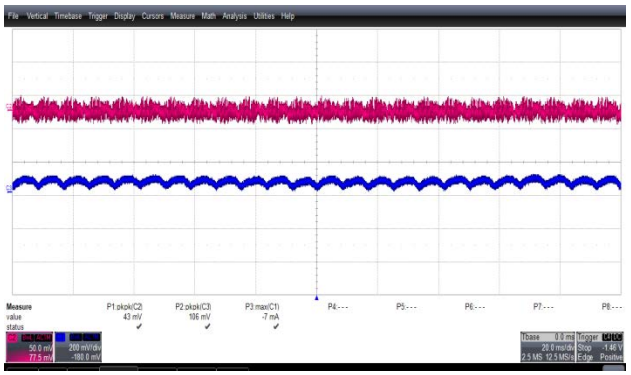

Figure 46 – Output Ripple Voltage Waveforms.
90 VAC Input. 1.5 A on 5 V and 0.1 A on 55 V.
Upper: 5 V, 50 mV / div.
Lower: 12 V, 200 mV, 20 ms / div.

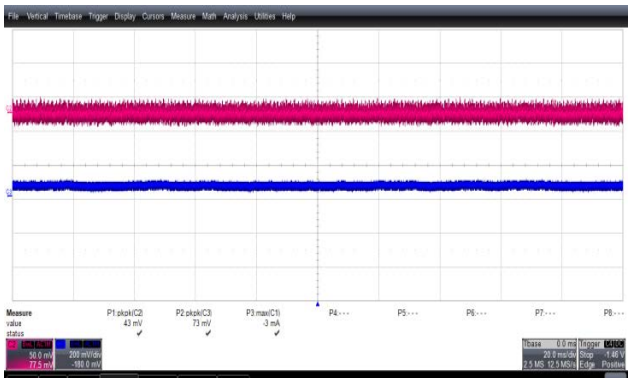

Figure 47 – Output Ripple Voltage Waveforms.
265 VAC Input. 1.5 A on 5 V and 0.1 A on 55 V.
Upper: 5 V, 50 mV / div.
Lower: 55 V, 200 mV, 20 ms / div.

12.3.2.3 Summary of Ripple Voltage with Different 5 V Load

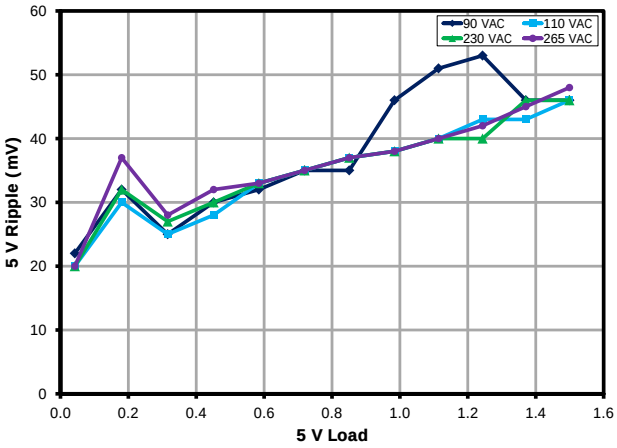

Figure 48 – With 0.1 A Load on 55 V.

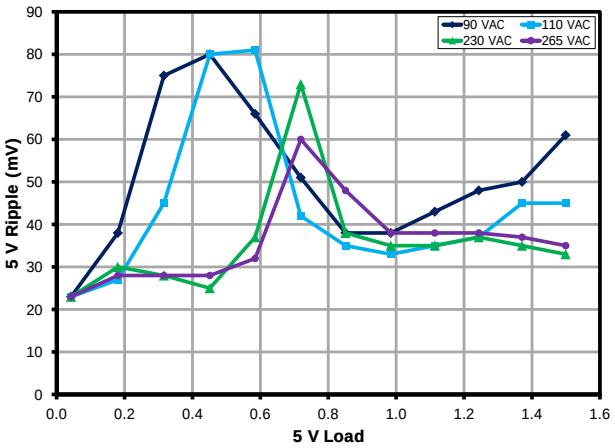

Figure 49 – With 0.32 A Load on 55 V.

12.4 *Line Undervoltage and Overvoltage (DC Input)*

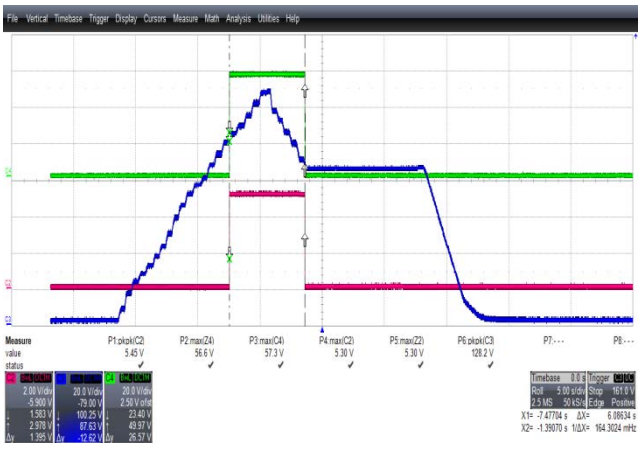

Figure 50 – Line Undervoltage.
DC Input.
V_{UV+}: 100.2 V, V_{UV-}: 87.6 V.
Upper: 55 V, 20 V / div.
Middle: 5 V, 2 V / div.
Lower: Input, 20 V, 5 s / div.

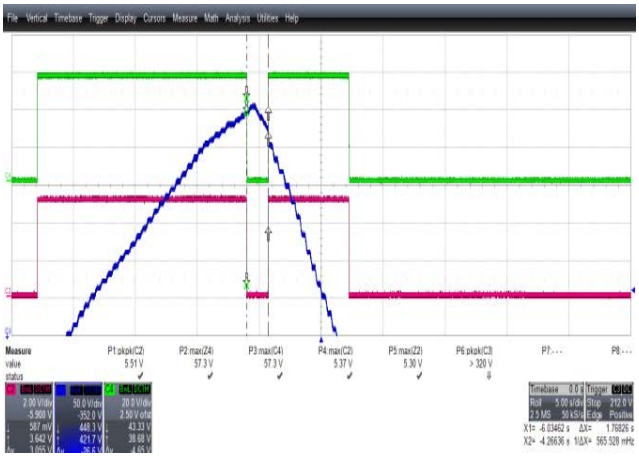

Figure 51 – Line Overvoltage.
DC Input, No-Load.
V_{OV+}: 443 V, V_{OV-}: 421 V.
Upper: 55 V, 20 V / div.
Middle: 5 V, 2 V / div.
Lower: Input, 50 V, 5 s / div.

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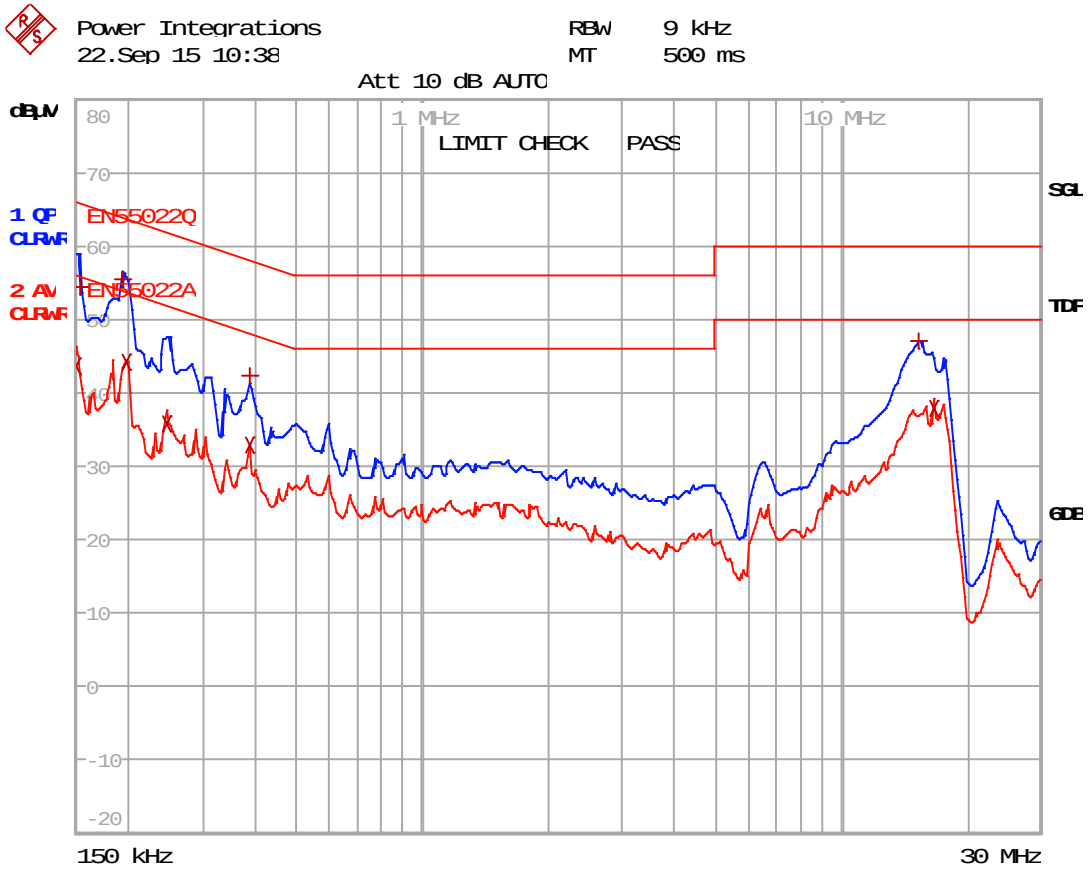
13 Conductive EMI - Earth Grounded Output (QP / AV)

13.1 *110 VAC Input*



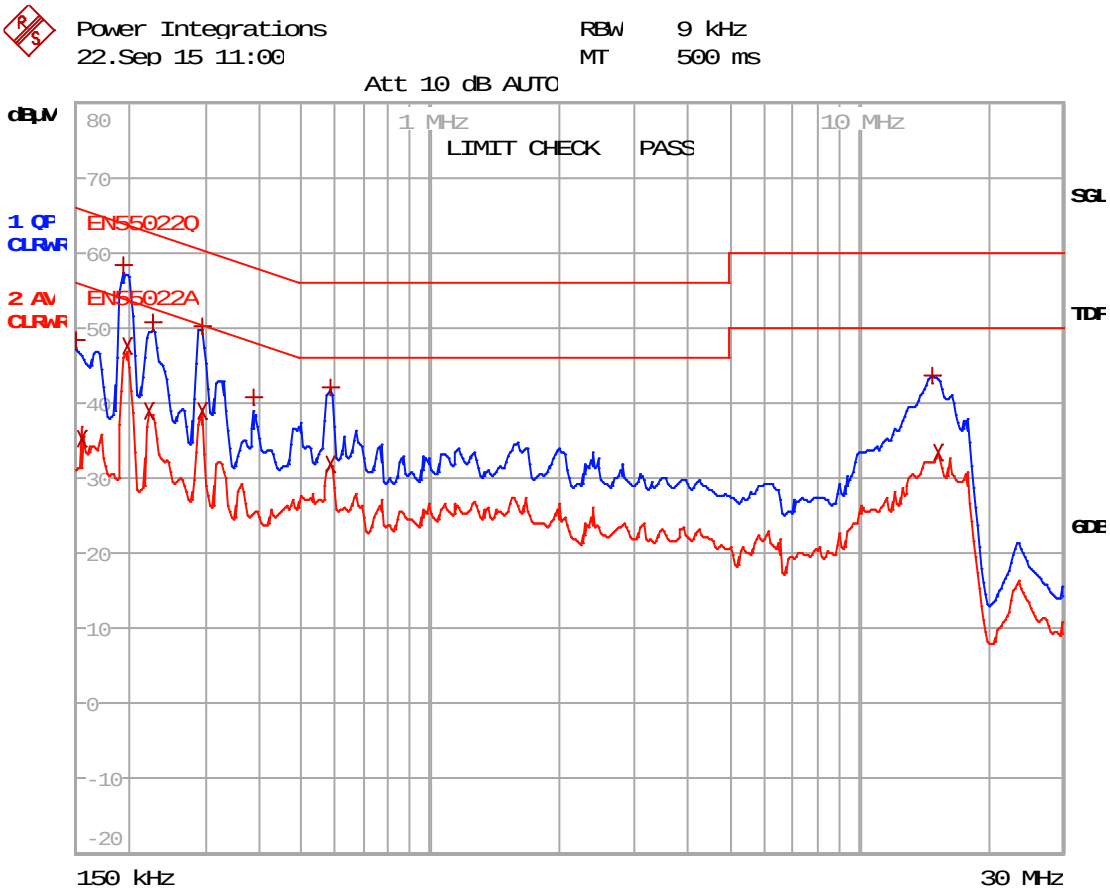
EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	150 kHz	43.63	L1 gnd	-12.36
1	Quasi Peak	153 kHz	54.32	L1 gnd	-11.50
1	Quasi Peak	194.040994568 kHz	55.55	L1 gnd	-8.31
2	Average	197.921814459 kHz	44.22	L1 gnd	-9.47
2	Average	246.09089917 kHz	35.69	L1 gnd	-16.19
1	Quasi Peak	388.060557825 kHz	42.40	L1 gnd	-15.70
2	Average	388.060557825 kHz	32.91	L1 gnd	-15.19
1	Quasi Peak	15.43588205 MHz	47.07	L1 gnd	-12.92
2	Average	16.7082951489 MHz	37.76	L1 gnd	-12.24

Figure 52 – Earth Ground at 110 VAC.

13.2 *230 VAC Input*



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	48.35	N gnd	-17.64
2	Average	156.06 kHz	35.27	L1 gnd	-20.40
1	Quasi Peak	194.040994568 kHz	58.38	N gnd	-5.47
2	Average	197.921814459 kHz	47.48	L1 gnd	-6.21
2	Average	222.892109397 kHz	38.97	L1 gnd	-13.73
1	Quasi Peak	227.349951585 kHz	50.64	N gnd	-11.90
1	Quasi Peak	294.101404803 kHz	50.32	N gnd	-10.08
2	Average	294.101404803 kHz	38.85	L1 gnd	-11.54
1	Quasi Peak	388.060557825 kHz	40.69	L1 gnd	-17.40
1	Quasi Peak	588.170326889 kHz	41.94	L1 gnd	-14.05
2	Average	588.170326889 kHz	31.95	L1 gnd	-14.04
1	Quasi Peak	14.8364879374 MHz	43.68	L1 gnd	-16.31
2	Average	15.43588205 MHz	33.34	L1 gnd	-16.65

Figure 53 – Earth Ground at 230 VAC.

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14 Lighting Surge Test

14.1 *Common Mode Test*

Passed ±6 kV, 500 A ring wave test.

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
6	90	12	10	PASS
-6	90	12	10	PASS
6	270	12	10	PASS
-6	270	12	10	PASS

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
22-Feb-16	DK	1.0	Initial Release	Apps & Mktg
29-Jun-16	KM	1.2	Added Magnetics Supplier.	

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