Design Example Report

Title	*7.8 W Isolated Flyback LED Driver Using LYTSwitch™-2 LYT2004D*
Specification	90 VAC – 270 VAC Input; 24 V to 60 V, 130 mA Output
Application	External Ballast LED Driver
Author	Applications Engineering Department
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Date	December 10, 2015
Revision	1.0

Summary and Features

- Accurate (primary-side control) constant current (CC)
  - Accurate CC, less than ±5% variation over load and line
- Provides ±5% constant voltage (CV)
- Wide LED load operating range (24 V to 60 V)
- Efficiency >85% at 230 VAC
- Low-cost, low component count (21), small size PCB
- Fast start-up time (<100 ms) – no perceptible delay
- No-load consumption <35 mW at nominal lines
- Integrated protection and reliability features
  - Output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis
  - No damage during brown-out conditions
  - Easily meets EN55015 and CISPR-22 Class B EMI standards

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a universal input design, 24 V to 60 V, 130 mA LED driver utilizing the LYT2004D device from the Power Integrations LYTSwitch-2 family.

This document contains the power supply and transformer specifications, schematics, bill of materials, and typical performance characteristics pertaining to this power supply.

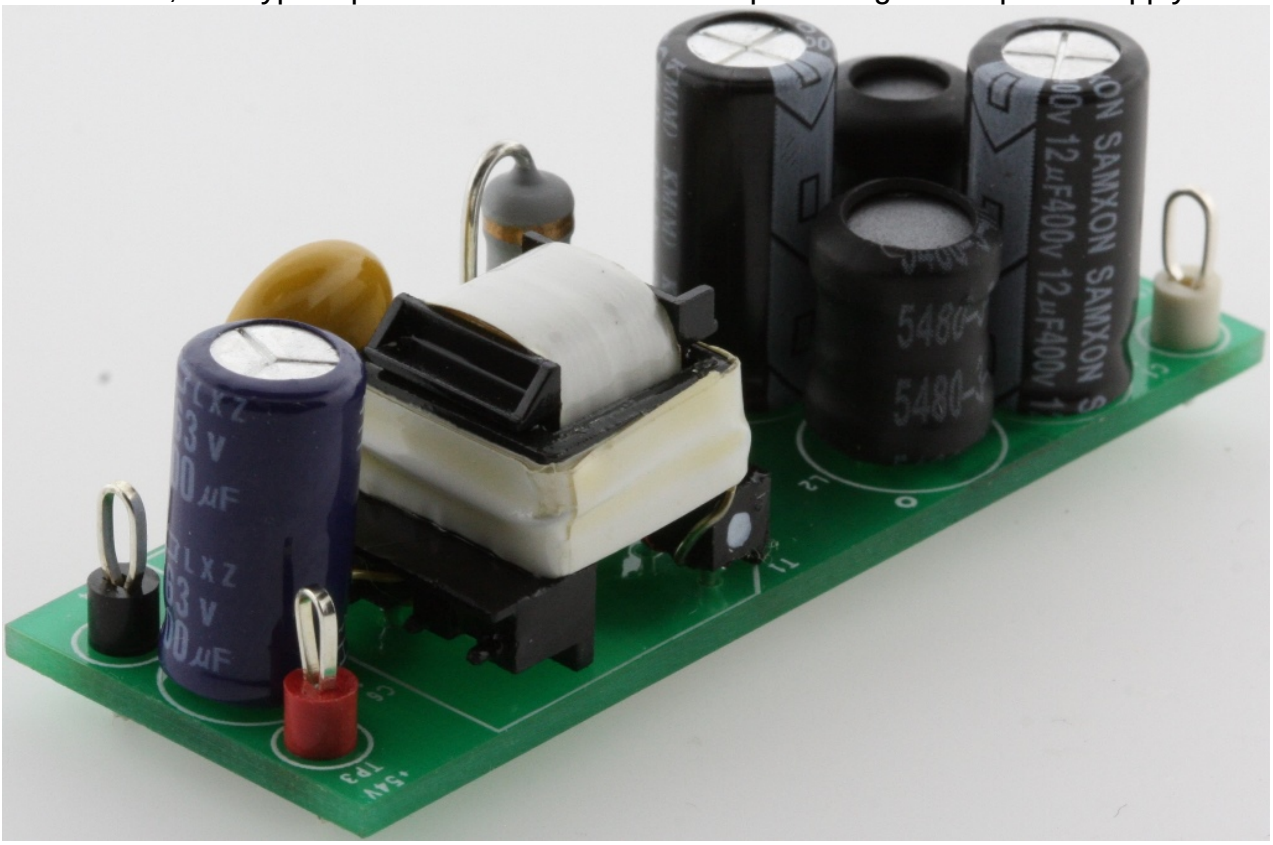


Figure 1 – Populated Circuit Board, Angle View.

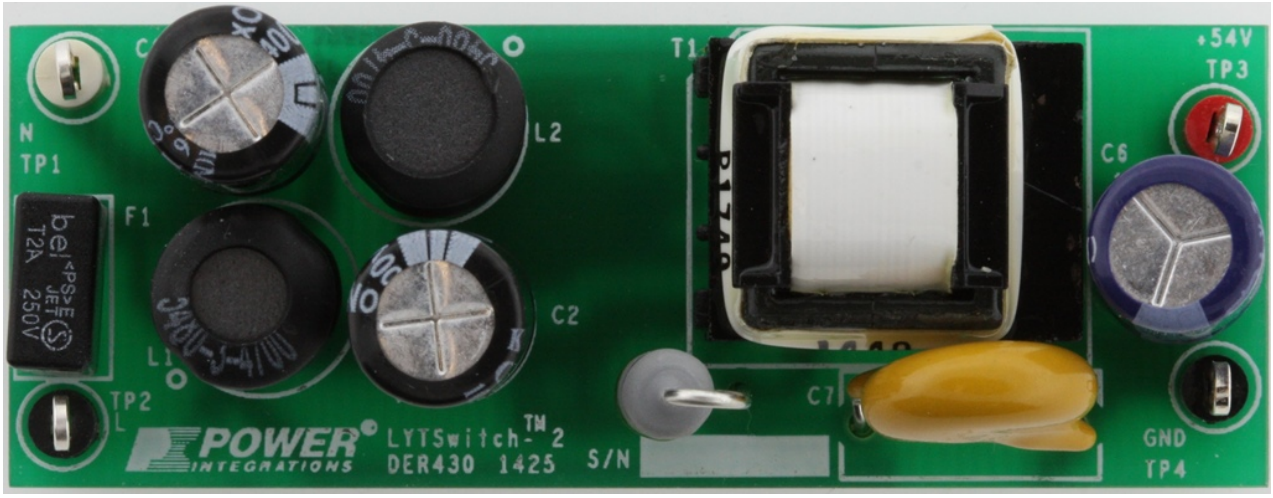


Figure 2 – Populated Circuit Board, Top View.

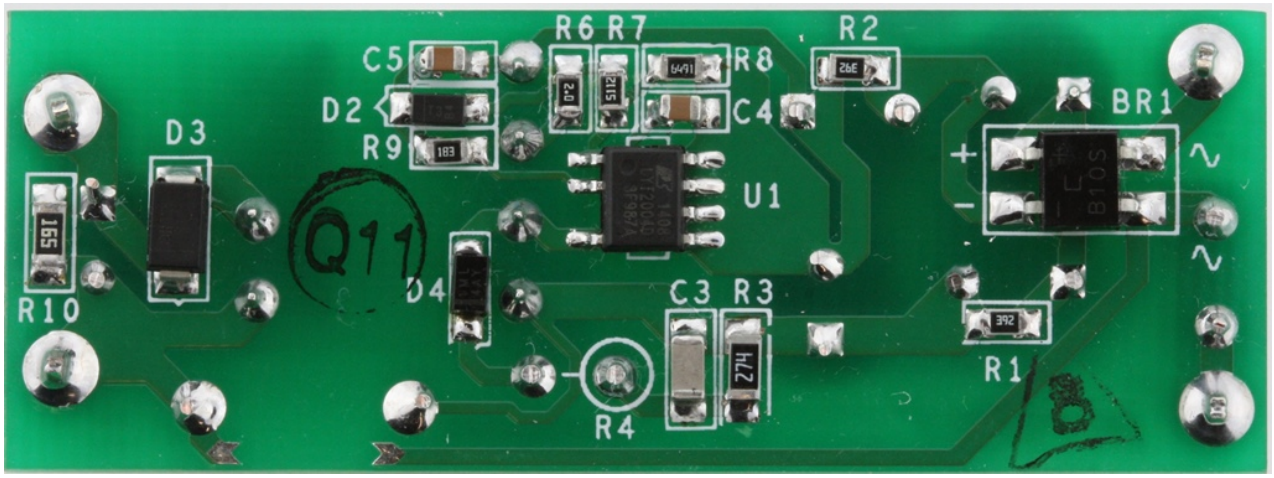


Figure 3 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		270	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
No-load Input Power	P_{NL}		30		mW	Measure at V_{IN} = 230 VAC.
Output						
Output Voltage	V_{OUT}	24		60	V	
Output Current	I_{OUT}		130		mA	25 ºC
Total Output Power						
Continuous Output Power	P_{OUT}			7.8	W	
Efficiency						
Full Load	η		85		%	Measured at P_{OUT} 25 ºC.
Environmental						
Conducted EMI		CISPR 15B / EN55015B				>6 dB Margin.
Safety		Designed to meet IEC950, UL1950 Class II				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	1.2//50 μs surge, IEC 1000-4-5, Series Impedance: 2 Ω.
Differential Surge			500		V	
ESD						
Contact Discharge		-8		+8	kV	IEC 61000-4-2.
Air Discharge		-15		+15	kV	
Ambient Temperature	T_{AMB}		40		ºC	

3 Schematic

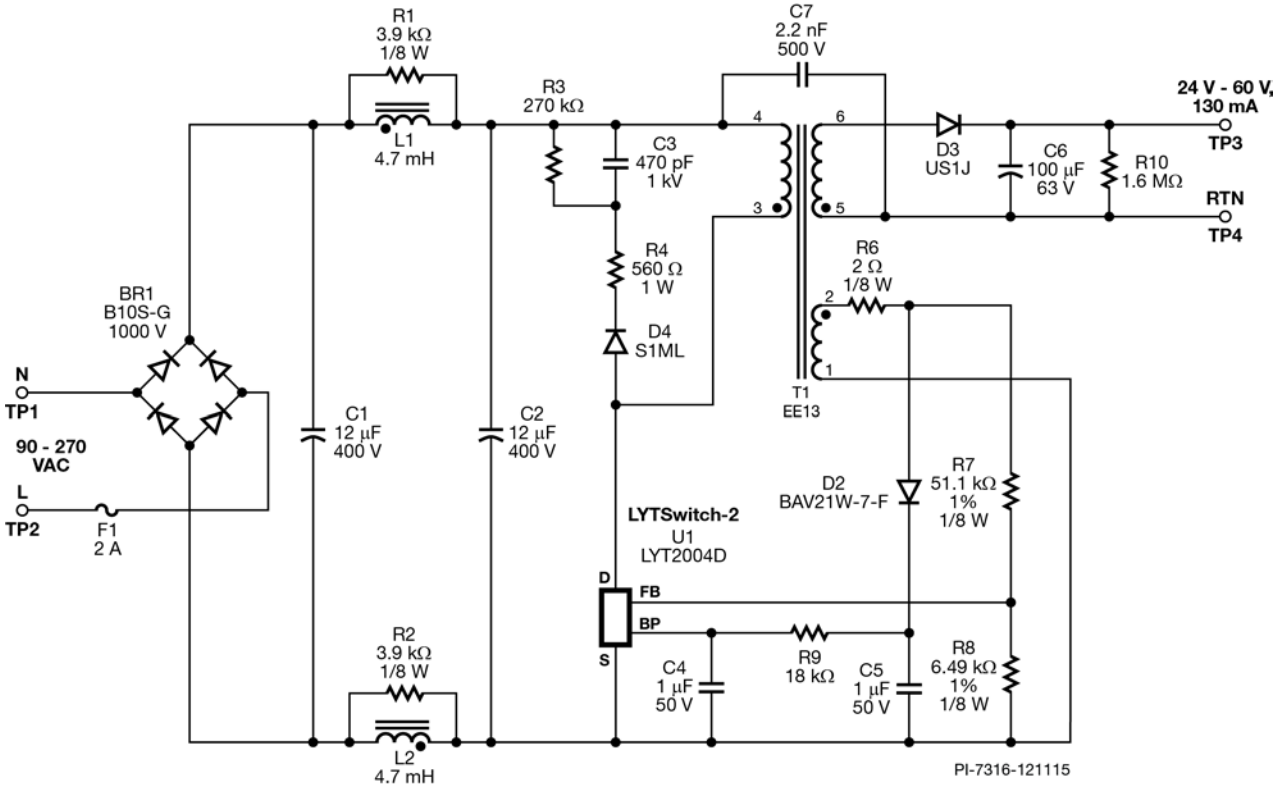


Figure 4 – Schematic.

4 Circuit Description

4.1 Input Filter

The AC input power is rectified by bridge rectifier BR1. The rectified DC is filtered by bulk storage capacitors C1 and C2. Inductors L1, L2, with capacitors C1 and C2, form pi (π) filters to attenuate conducted differential-mode EMI noise. This configuration, along with balance transformer design, grounding the core and adding Y capacitor C7, allows this design to meet EMI standard EN55022 class B with good margin, especially when there is a ground plane terminated to earth, which causes high common-mode noise. Resistors R1 and R2 damp the self-resonance of the inductors L1 and L2 to avoid noise peaking in the conducted EMI plot at their resonant frequency.

4.2 LYTSwitch-2 Primary

The LYTSwitch-2 device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and start-up and protection functions all on one IC. Its integrated 725 V power MOSFET allows sufficient voltage margins in universal input AC applications, including extended line swells.

The rectified and filtered input voltage is applied to one end of the transformer (T1) primary winding. The other side of the transformer's primary winding is driven by the internal MOSFET of U1. An RCD-R clamp consisting of C3, R3, R4 and D4 limits drain voltage spikes caused by leakage inductance. The clamp circuit is optimized in order to prevent any excessive ringing on the drain voltage waveform which may affect CC regulation load input power to less than 35 mW at nominal input voltage. Capacitor C4 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller.

4.3 Output Rectification

The transformer's secondary output is rectified by D3, and filtered by C6. The value the output capacitor C6 is selected to provide <30% output current ripple based on the available LED load in the lab. However, the ripple current may be different depending on the type of LED used due to different dynamic resistance values. The value of C6 must be adjusted accordingly.

4.4 Regulation

The LYTSwitch-2 device regulates the output using ON/OFF control for CV regulation, and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R7 and R8) were selected using standard 1% resistor values to center both the no-load output voltage and constant current regulation thresholds. Resistor R10 is providing a minimum load to maintain voltage regulation when the output is unloaded. Resistor R6 provides filtering of the feedback signals which is especially helpful at no-load in order to keep the output. The external bias supply, D2, C5, and R9 improves

efficiency and reduces no- voltage stable. The value must be kept low to prevent output voltage creeping up and to avoid adding heavier pre-load resistor which lowers efficiency.

5 PCB Layout

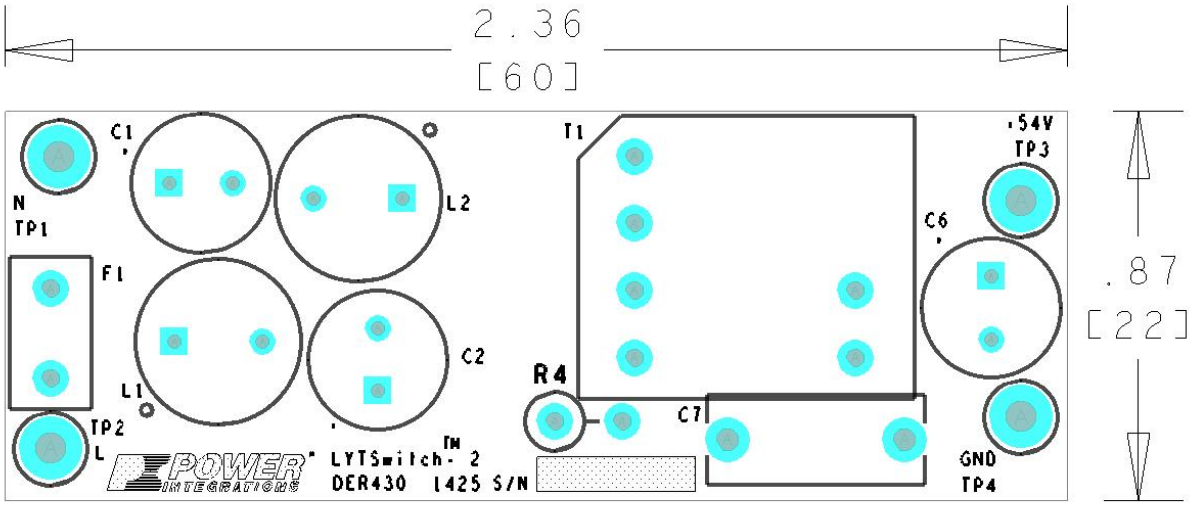


Figure 5 – Printed Circuit Board Layout, Top Side.

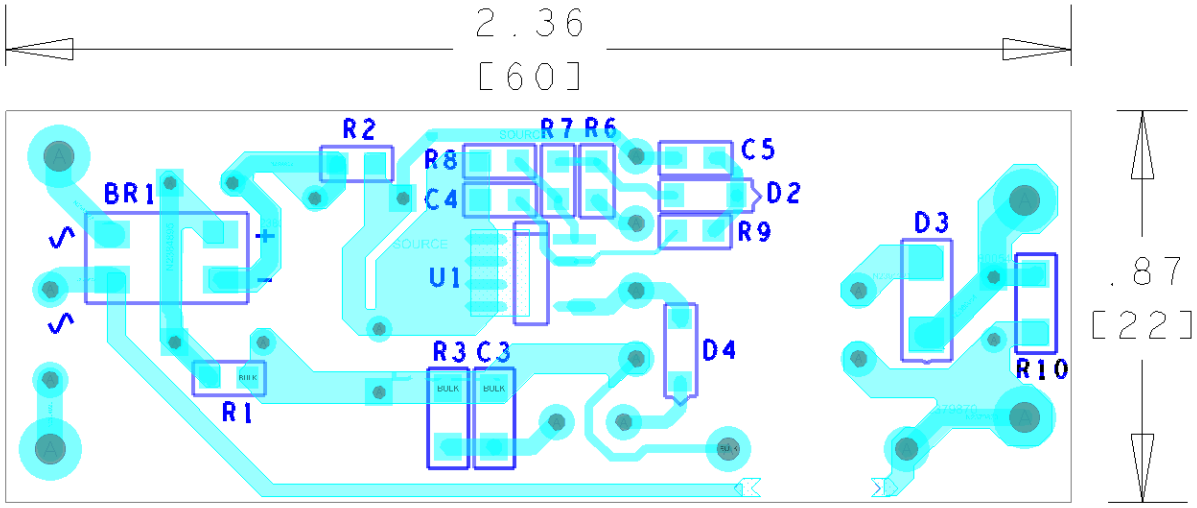


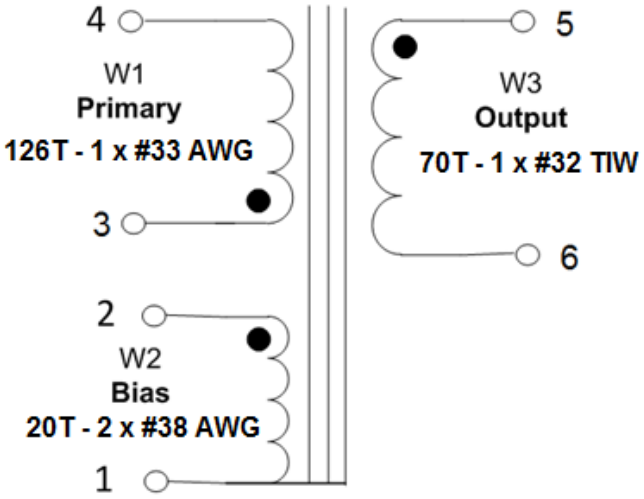
Figure 6 – Printed Circuit Board Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	P	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Tech
2	2	C1 C2	12 µF, 400 V, Electrolytic, (8 x 16)	EKM126M2GF16RRS1P	Man-Yue Electronics
3	1	C3	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay
4	2	C4 C5	1 µF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
5	1	C6	100 µF, 63 V, Electrolytic, Low ESR, 270 mΩ (8 x 15)	ELXZ630ELL101MH15D	Nippon Chemi-Con
6	1	C7	CAP Ceramic 2.2 nF 500 VAC	VY1222M47Y5UQ63V0	Vishay
7	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-123	BAV21W-7-F	Diodes, Inc.
8	1	D3	DIODE ULTRA FAST, SW 600 V, 1 A, SMA	US1J-FDICT-ND	Diodes, Inc.
9	1	D4	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
10	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
11	2	L1 L2	4.7 mH, 0.150 A, 10%	RL-5480-3-4700	Renco
12	2	R1 R2	3.9 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ392V	Panasonic
13	1	R3	270 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ274V	Panasonic
14	2	R4	560 Ω, 5%, 1 W, Metal Oxide	RSF100JB-560R	Yageo
15	1	R6	2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R0V	Panasonic
16	1	R7	51.1 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5112V	Panasonic
17	1	R8	6.49 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6491V	Panasonic
18	1	R9	18 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ183V	Panasonic
19	1	R10	1.6 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ165V	Panasonic
20	1	T1	Bobbin, EE13, Horizontal, 8 pins	548	Hical Magnetics
21	2	TP1 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
22	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
23	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
24	1	U1	LYTSwitch-2, CV/CC, SO-8D	LYT2004D	Power Integrations

7 Transformer Specification

7.1 Electrical Diagram



(Core is grounded through pin 1)

Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 3, 4 to 5, 6.	3000 VAC
Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1.264 mH ±3%
Primary Leakage Inductance	Pins 3-4, all other windings shorted, measured at 100 kHz, 0.4 V_{RMS}.	50 µH max

7.3 Material List

Item	Description
[1]	Core: EE13.
[2]	Bobbin: EE13 Horizontal, 8 pins. Hical Magnetics P/N: CPV-RM5-1S-6P-G. (PI P/N: 25-0002-00)
[3]	Magnet wire: #33 AWG - Double coated.
[4]	Magnet wire: #38 AWG - Double coated.
[5]	Triple Insulated: #32 AWG (0.20 mm).
[6]	Tape: 3M 1298 Polyester Film, 7.7 mm wide, 2.0 mils thick, or equivalent.
[7]	Tape: 3M 1298 Polyester Film, 6.0 mm wide, 2.0 mils thick, or equivalent.
[8]	Non-insulated bare wire: AWG# 31.
[9]	Varnish: Dolph BC-359 or equivalent.

7.4 Transformer Build Diagram

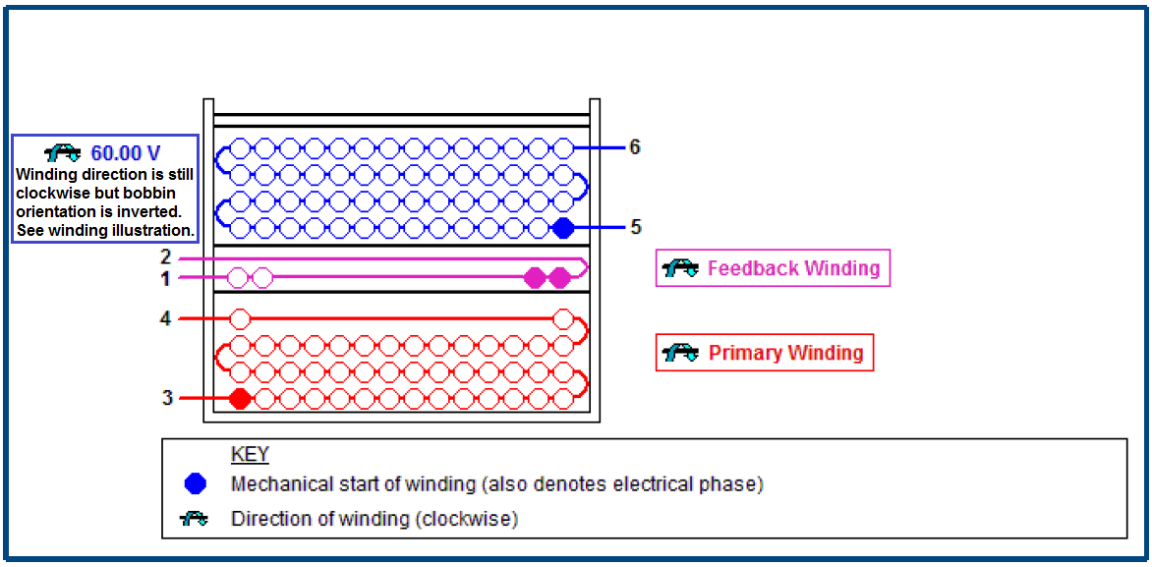
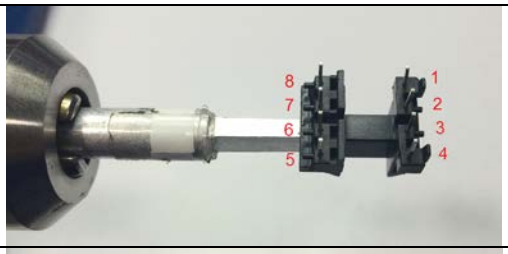
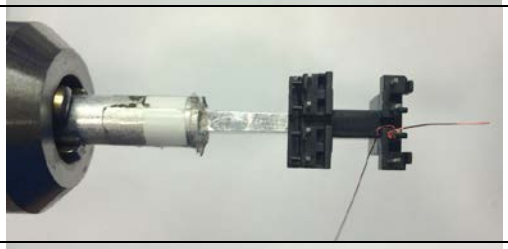
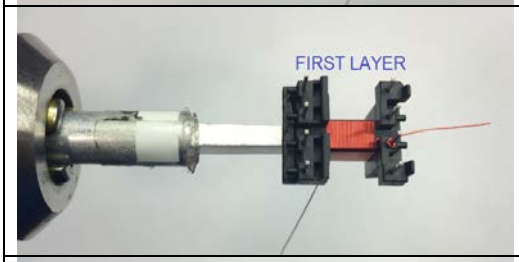
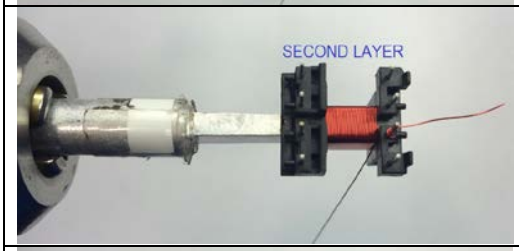
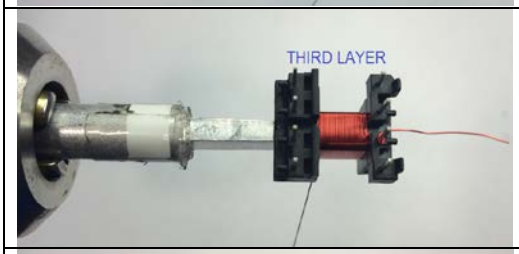
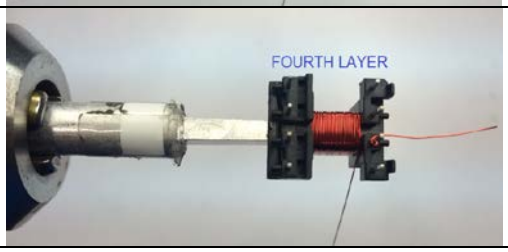


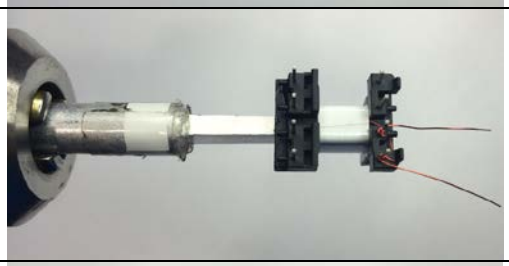
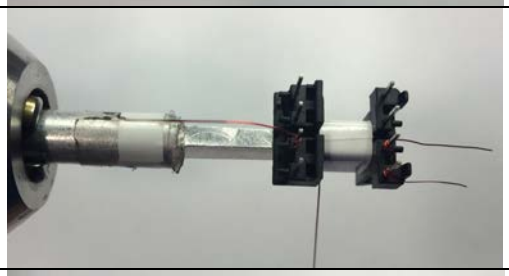
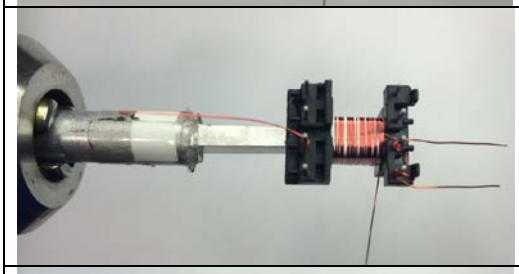
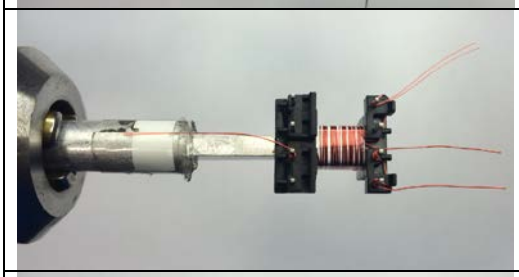
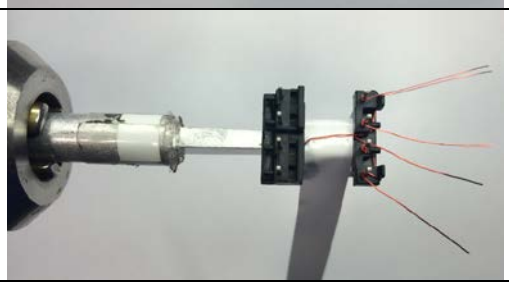
Figure 8 – Transformer Build Diagram.

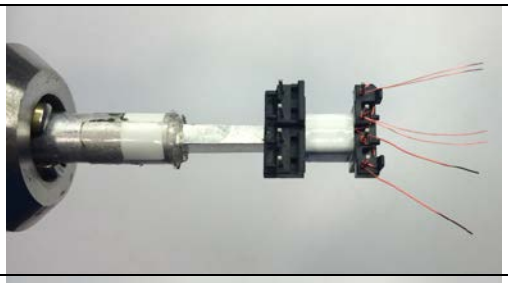
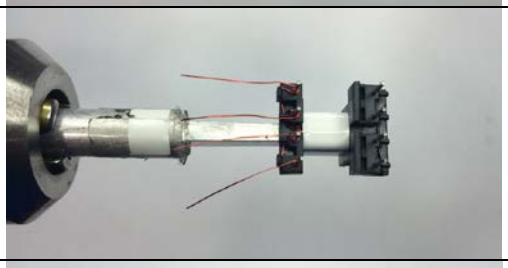
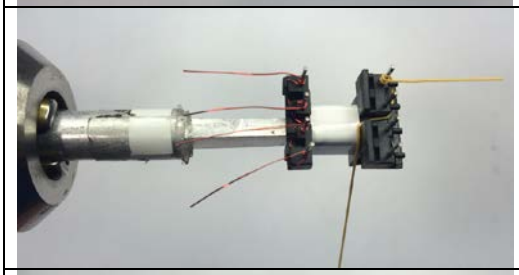
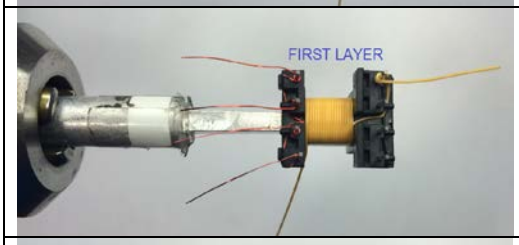
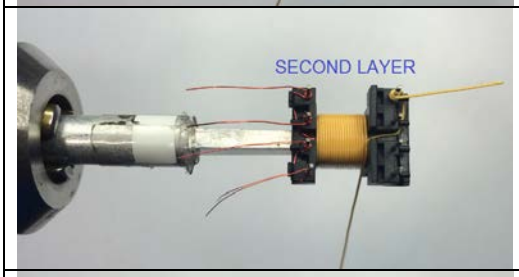
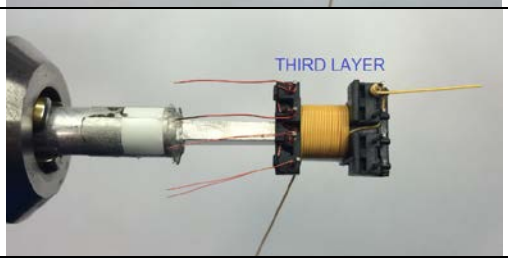
7.5 Winding Construction

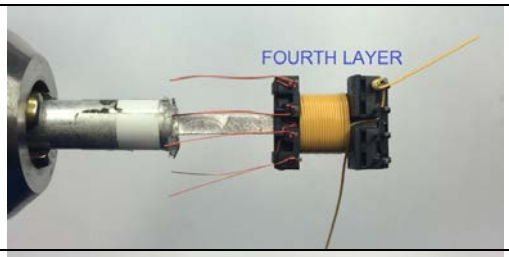
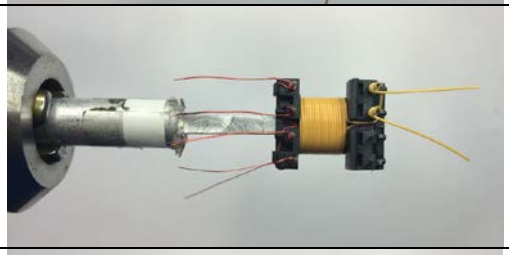
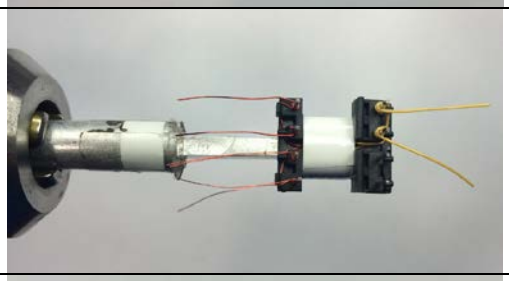
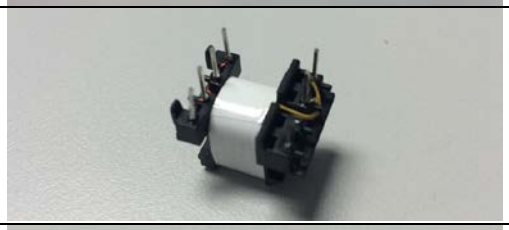
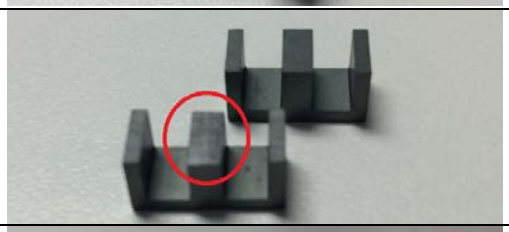
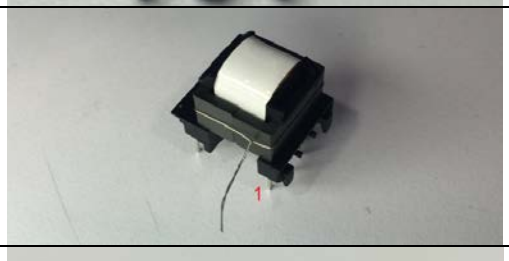
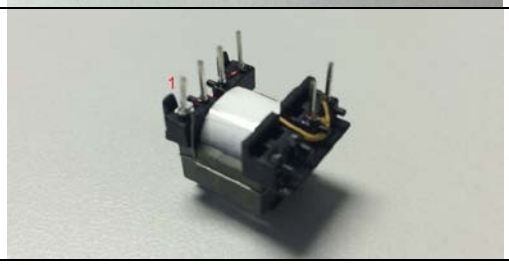
Winding Preparation	Item [2]. Place the bobbin on the mandrel with pins 1-4 on the right side. Winding direction is clockwise.
WD1 Primary	Item [3]: 1 x AWG #33. Start at pin 3, wind 126 turns of wire in 4 layers and finish at pin 4. See details in section 7.6 winding illustration.
Insulation1	Item [6]. Put single layer of tape to secure primary windings. See details in section 7.6 winding illustration.
WD2 Bias	Item [4]. 2 x AWG #38. Start 20 turns at pin 2 and finish at pin 1. See details in section 7.6 winding illustration.
Insulation2	Item [6]. Put 1 layer of tape to secure bias windings. See details in section 7.6 winding illustration.
WD3 Secondary	Invert bobbin orientation, pin 5-8 on the right side. Item [5]. Start 70 turns at pin 5 and finish with four layers at pin 6. See details in section 7.6 winding illustration.
Insulation3	Item [6]. Put 2 layers of tape to secure windings.
Finish	Grind core item [1] halves to get 1.264 mH inductance. Use wire item [8], wrap around both halves of core, twist both ends and connect to pin 1 for grounding. Put 3 layers of tape item [7] to secure wire ground and core. Pull out or cut pin 7 and 8. See details in section 7.6 winding illustration. Varnish with item [9].

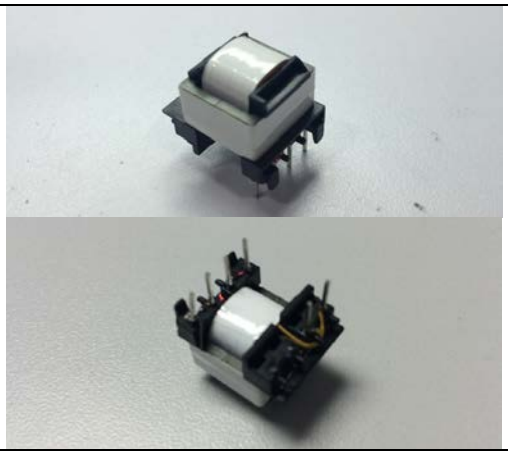
7.6 Winding Illustration

Winding Preparation		Put the bobbin item [2] in EE13 mandrel with pins 1-4 on the right side as illustrated on the figure.
WD 1 Primary Winding		Start primary winding item [3] at pin 3.
		Wind full width first layer of primary winding from right to left.
		Wind full width second layer of primary winding from left to right.
		Wind full width third layer of primary winding from right to left.
		Wind fourth layer of primary winding evenly from left to right completing 126 turns.

		Terminate end of primary winding in pin 4.
Insulation 1		Put single layer of tape item [6] for insulation.
WD 2 **Bias Winding**		Using Item [4], 2 x AWG#38. Temporarily terminate start of bias winding at any pin terminal on the left side.
		Wind 20 turns evenly distributed of bias winding from left to right.
		Terminate end of bias winding at pin 1.
		Place tape using item [6]. Remove temporary termination of start winding on the left side and terminate across the bobbin on the right side at pin 2 as shown.

Insulation 2		Continue putting 1 layer of tape covering the bias winding for insulation.
WD 3 **Secondary Winding**		Invert bobbin orientation. Take the bobbin out of the mandrel and put it back with primary pins 1 - 4 on the left side of the mandrel as shown.
		Start primary winding item [5] 1 x AWG32 TIW at pin 5.
		Wind full width first layer of secondary winding from right to left.
		Wind full width second layer of secondary winding from left to right.
		Wind full width third layer of secondary winding from right to left.

		Wind full width fourth layer of secondary winding from left to right completing 70 turns.
		Terminate end of secondary winding at pin 6.
Insulation 3		Put two layers of item [6] for insulation.
Termination		Terminate and solder each winding properly to its designated pin terminal.
Core Grinding		Grind center leg of one core halves to attain 1.264mH nominal inductance.
Core Grounding		Place the core in the bobbin. Wrap around core item [8] and twist tightly enough both ends to hold the core near pin1 for termination as shown.
		Terminate and solder end of ground wire at pin 1.

Finish		Tightly put 3 layers of tape item [7] to secure both halves of core and the ground wire. Varnish with item [9].

8 Transformer Design Spreadsheet

ACDC_LYTSwitch-2_081114; Rev.2.1; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LYTSwitch-2_080814_Rev2-1; Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			90	V	Minimum AC Input Voltage
VACMAX	270		270	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
Application Type	Ballast-CC		Ballast-CC		Choose application type
VO	60.00		60.00	V	Output Voltage. This value is recommended to be 10% higher than the maximum LED Voltage
IO	0.13		0.13	A	Power Supply Output Current (corresponding to peak power)
Power			7.80	W	Continuous Output Power
n	0.86		0.86		Efficiency Estimate at output terminals
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	24.00		24.00	uF	Input Capacitance
ENTER LYTSwitch-2 VARIABLES					
Chosen Device	Auto		LYT2004D		Chosen LYTSwitch-2 device
ILIMITMIN			0.41	A	Minimum Current Limit
ILIMITTYP			0.44	A	Typical Current Limit
ILIMITMAX			0.48	A	Maximum Current Limit
FS	68.00		68.00	kHz	Typical Device Switching Frequency at maximum power
VOR			108.90	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS	2.00		2.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			1.59		KP assuming minimum LP, VMIN, and average switching frequency. Ensure that this value is above 1.30 for optimal operation
FEEDBACK WINDING PARAMETERS					
NFB	20.00		20.00		Feedback winding turns
VFLY			17.29	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			16.58	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
BIAS	Ext. bias		Ext. bias		Select between self bias or external bias to supply the IC.
VB	0.00		0.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB	.	Info	N/A		Bias winding is disabled. Verify on the bench that current value of VFLY is enough to supply the IC under all operating conditions
REXT			1.80	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON	4.62		4.62	us	Desired output diode conduction time
DCON_FINAL			4.59	us	Final output conduction diode, assuming integer values for NP and NS
TON			4.79	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		Info	48.39	k-ohm	Upper resistor in Feedback resistor divider. Once the initial prototype is running, it may be necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER			6.12	k-ohm	Lower resistor in resistor divider

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	EE13		EE13		Enter Transformer Core.
Custom_Core					Enter Core name if selection on drop down menu is "Custom"
Bobbin			BE-13		Bobbin part number
AE			17.10	mm^2	Core Effective Cross Sectional Area
LE			30.20	mm	Core Effective Path Length
AL			1130.00	nH/turn ^2	Ungapped Core Effective Inductance
BW			7.40	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4.00		Number of Primary Layers
NS			70.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			104.45	V	Minimum DC bus voltage
VMAX			381.84	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.40		Maximum duty cycle measured at VMIN
IAVG			0.09	A	Input Average current
IP			0.41	A	Peak primary current
IR			0.41	A	Primary ripple current
IRMS			0.17	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1226.21	uH	Minimum Primary Inductance
LPTYP			1264.13	uH	Typical Primary inductance
LP_TOLERANCE	3.00		3.00	%	Tolerance in primary inductance
NP			126.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			79.63	nH/turn ^2	Gapped Core Effective Inductance
BM_TARGET			2600.00	Gauss	Target Flux Density
BM			2599.14	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2600 is recommended
BP			2888.63	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3100 is recommended
BAC			1299.57	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			158.81		Relative Permeability of Ungapped Core
LG			0.26	mm	Gap Length (LG > 0.1 mm)
BWE			29.60	mm	Effective Bobbin Width
OD			0.23	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.19	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			50.80	Cmils	Bare conductor effective area in circular mils
CMA			292.55	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			0.73	A	Peak Secondary Current
ISRMS			0.31	A	Secondary RMS Current
IRIPPLE			0.28	A	Output Capacitor RMS Ripple Current
CMS			61.22	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			32.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			630.53	V	Maximum Drain Voltage Estimate (Assumes 20% clamping

					voltage tolerance and an additional 10% temperature tolerance)
PIVS			272.13	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL	49.90		49.90	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL	6.19		6.19	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)	62.00		62.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)	0.12		0.12	Amps	Measured Output current from first prototype
RUPPER_FINE			52.32	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 52.3 k-ohms
RLOWER_FINE			6.73	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 6.81 k-ohms

9 Performance Data

All measurements were taken with the board at open frame, 25 ºC ambient.

9.1 Active Mode Efficiency

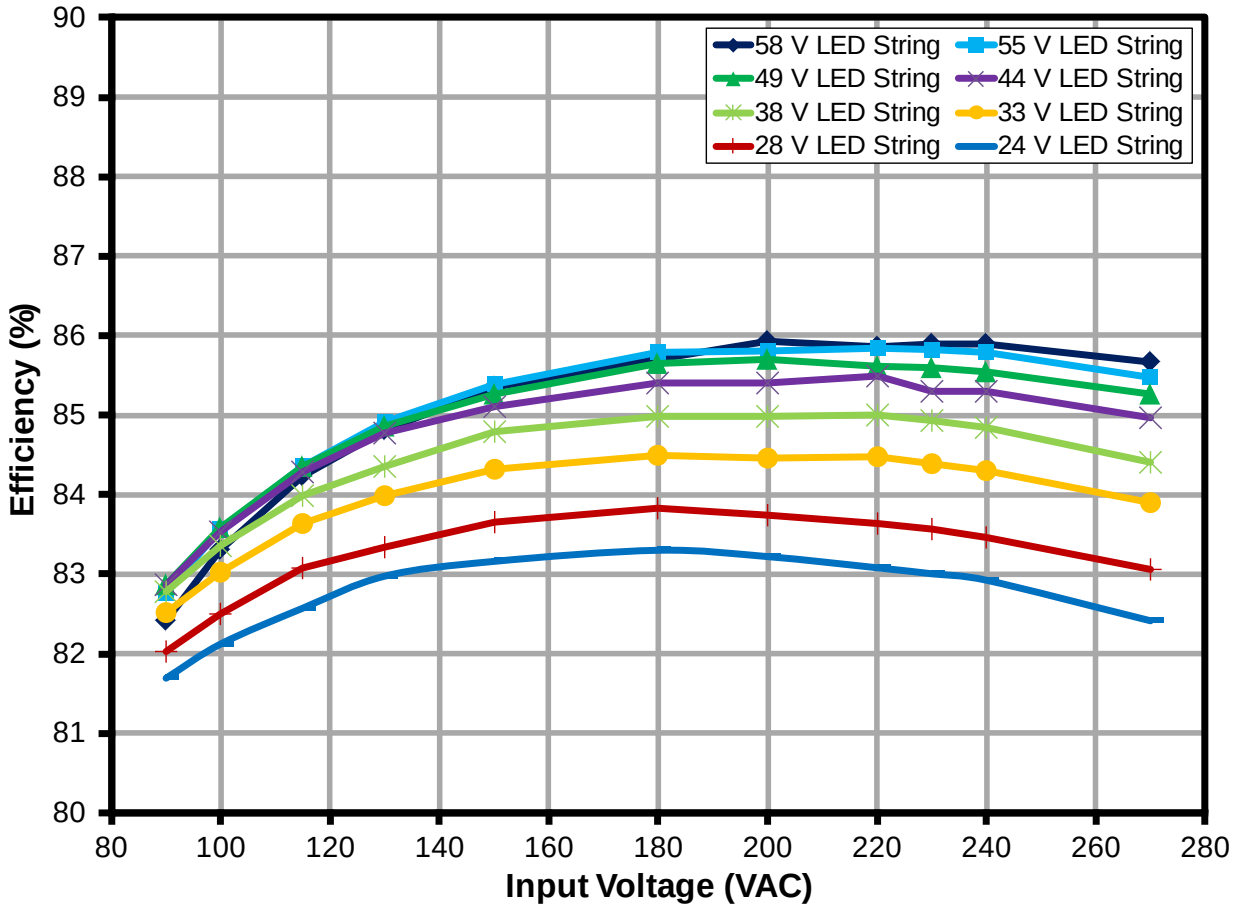


Figure 9 – Efficiency vs. Line and Load.

9.2 Average Efficiency

Input		Input Measurement					LED Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	130	114.98	147.29	9.35	0.55	82.28	60.73	129.88	7.89	84.36
75	97.5	114.99	115.06	7.07	0.53	83.78	61.05	97.87	5.9	84.57
50	65	115.01	80.99	4.71	0.51	85.68	61.37	64.90	3.98	84.49
25	32.5	115.02	46.08	2.42	0.46	88.46	61.86	32.40	2.00	82.98
							AVERAGE EFFICIENCY			84.10

Input		Input Measurement					LED Load Measurement			Efficiency (%)
LOAD (%)	LOAD (mA)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
100	130	229.96	88.18	9.19	0.45	88.87	60.72	129.88	7.89	85.82
75	97.5	229.97	69.46	6.95	0.44	89.78	60.98	97.38	5.94	85.45
50	65	229.97	50.91	4.80	0.4	90.94	61.43	64.90	3.99	83.06
25	32.5	229.99	29.55	2.46	0.36	92.85	61.93	32.41	2.0	81.75
							AVERAGE EFFICIENCY			84.02

9.3 Line and Load Regulation

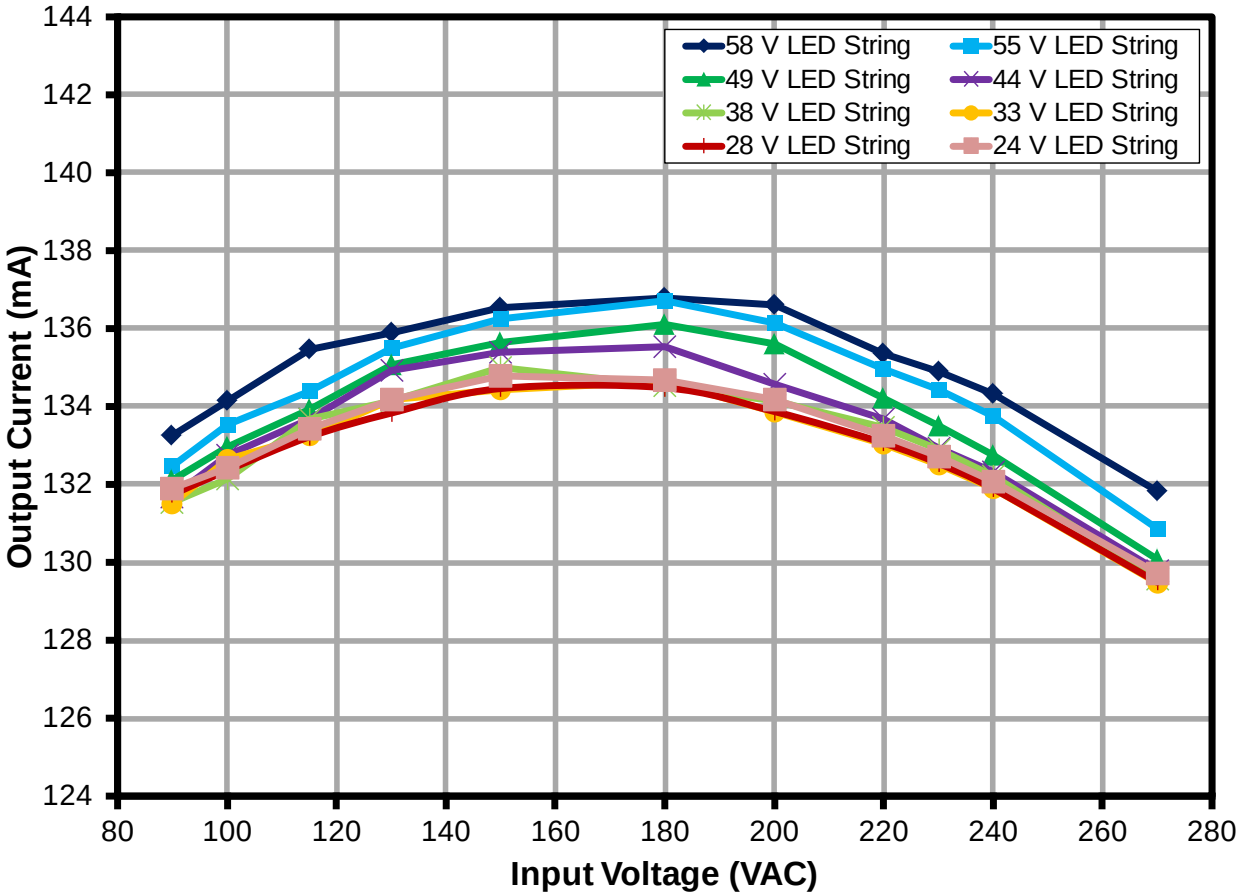


Figure 10 – Regulation vs. Line and Load.

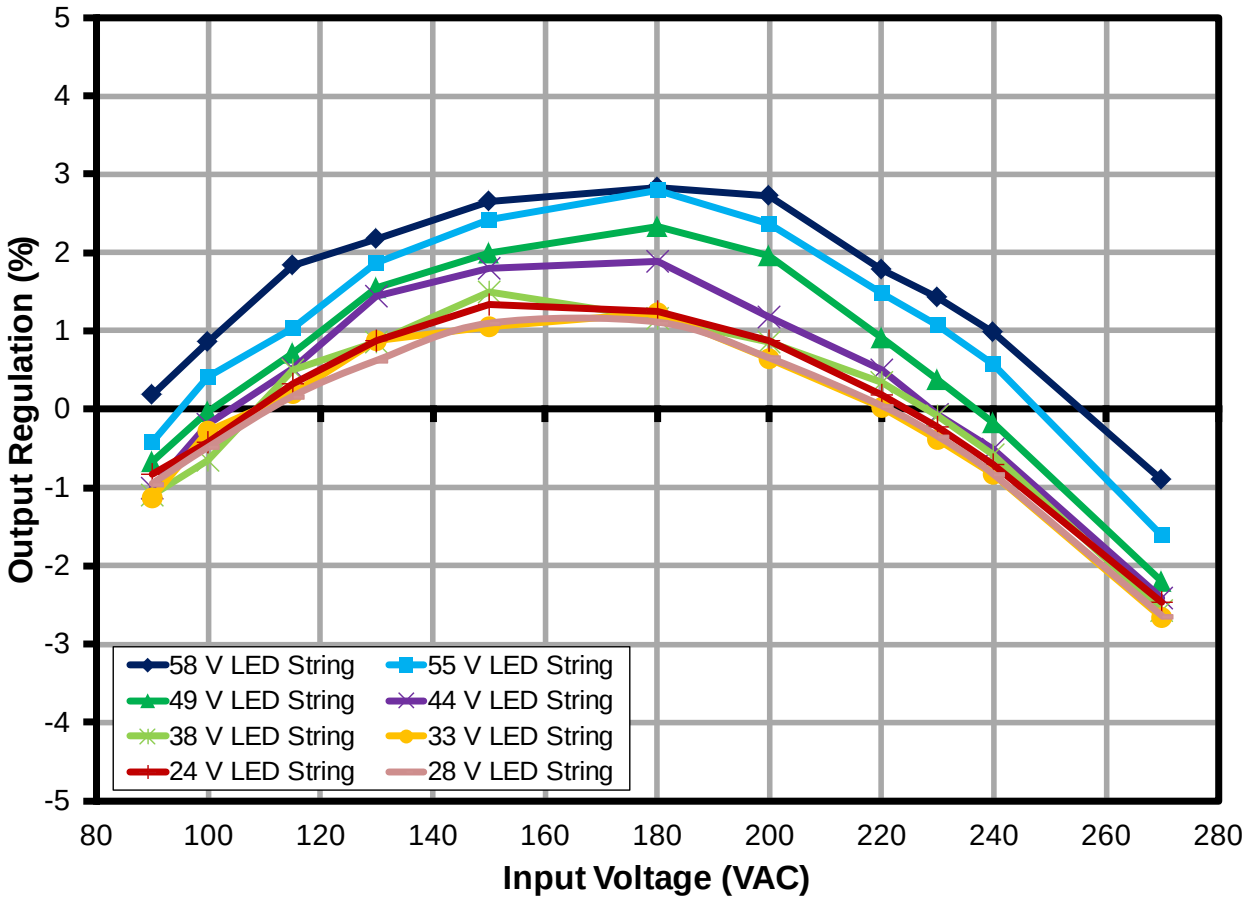


Figure 11 – % Regulation vs. Line and Load.

9.4 CV/CC Characteristics

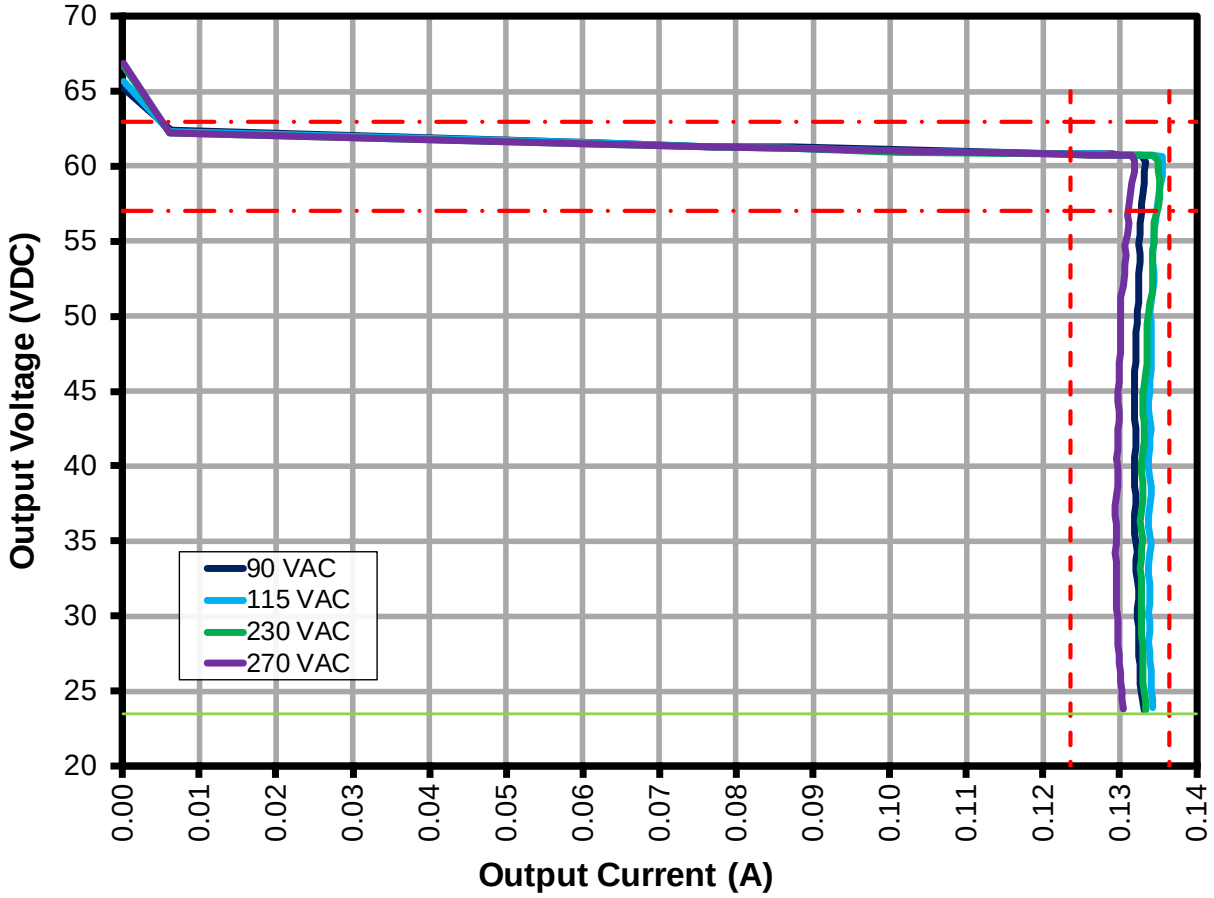


Figure 12 – CV/CC Characteristics.

9.5 No-Load Input Power

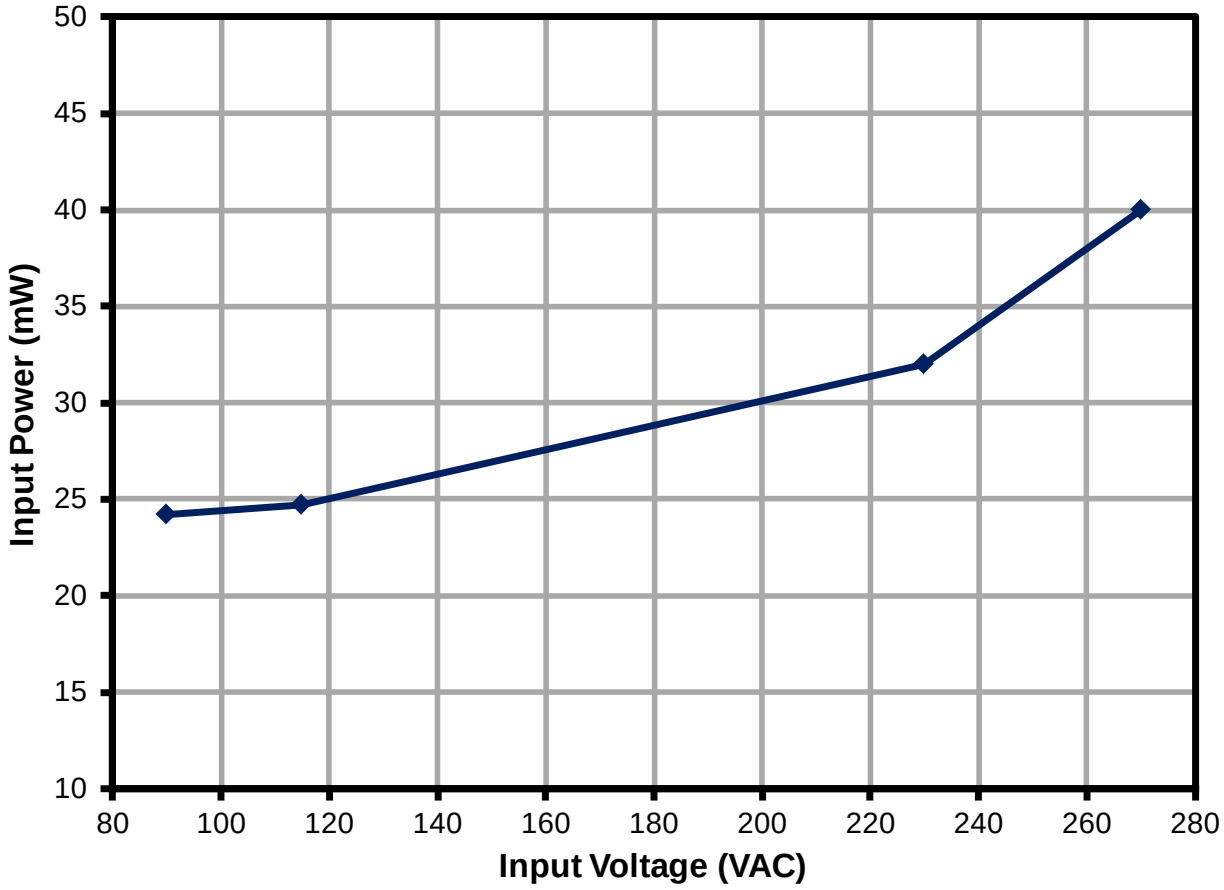


Figure 13 – No-Load Input Power.

10 Thermal Performance

Images captured after running for >30 minutes at enclosed compartment (30 °C ambient).

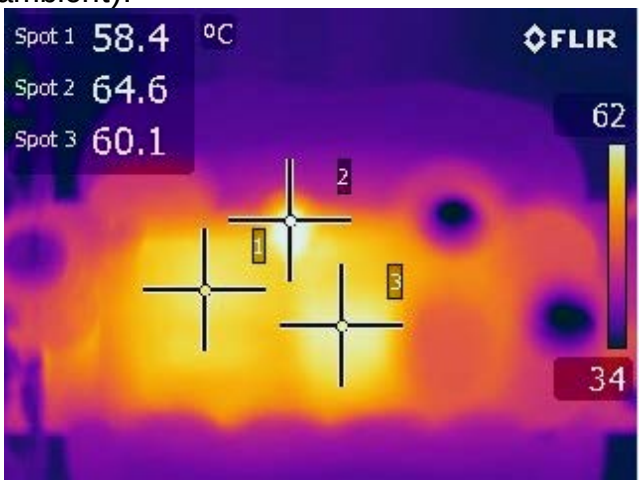


Figure 14 – 90 VAC, Thermal, Top Side.
SPOT1 (T1): 58.4 °C
SPOT2 (R4): 64.6 °C
SPOT3 (U1 Top Side): 60.1 °C

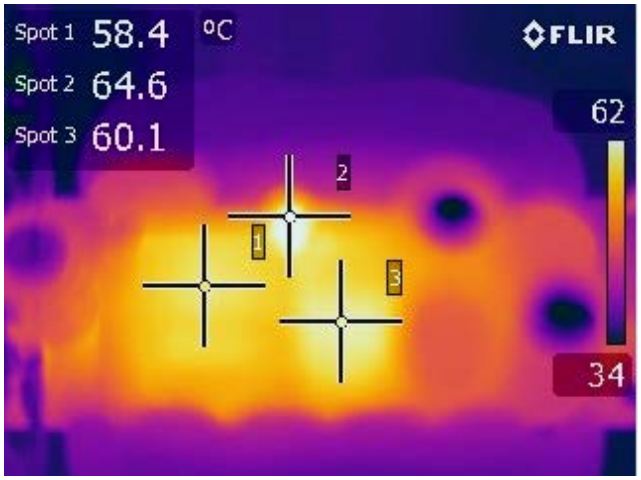


Figure 15 – 90 VAC, Thermal, Bottom Side.
SPOT1 (U1): 67.8 °C.
SPOT2 (D4): 65.1 °C.

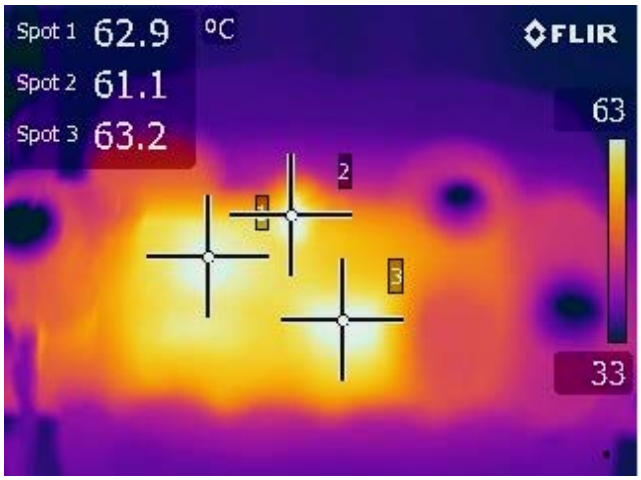


Figure 16 – 270 VAC, Thermal, Top Side.
SPOT1 (T1): 62.9 °C.
SPOT2 (R4): 61.1 °C.
SPOT3 (U1 Top Side): 63.2 °C.

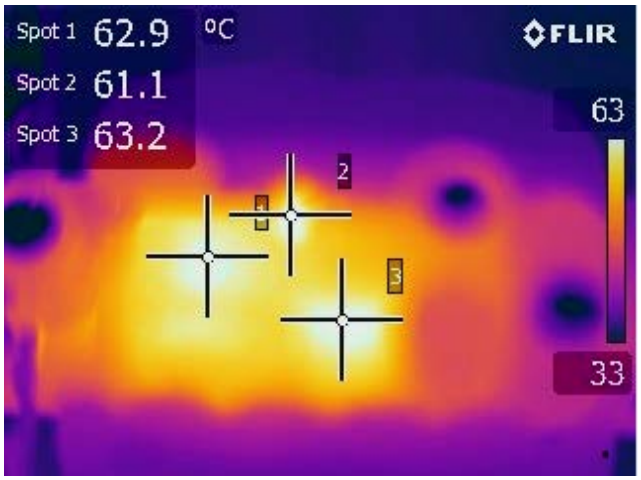


Figure 17 – 270 VAC, Thermal, Bottom Side.
SPOT1 (U1): 70.0 °C.
SPOT2 (D4): 64.2 °C.

11 Waveforms

11.1 Input Voltage and Input Current Waveforms

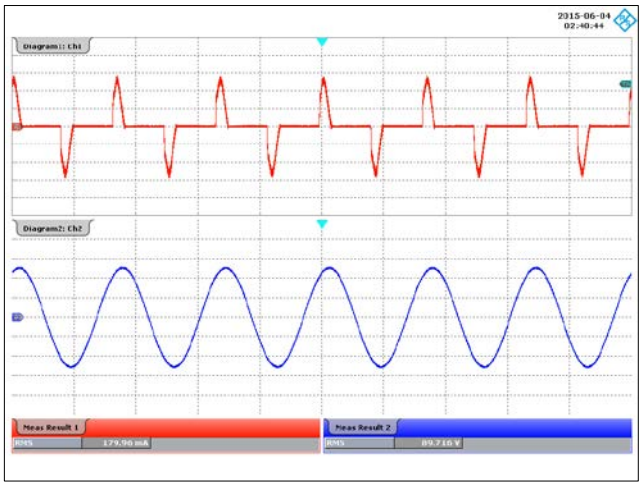


Figure 18 – 90 VAC, 60Hz Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 50 V / div, 10 ms / div.

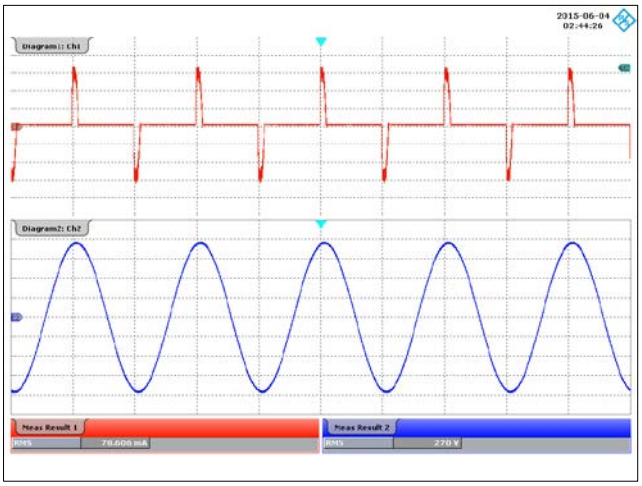


Figure 19 – 270 VAC, 50Hz Full Load.
Upper: I_{IN}, 100 mA / div.
Lower: V_{IN}, 100 V / div, 10 ms / div.

11.2 Output Current and Output Voltage at Normal Operation

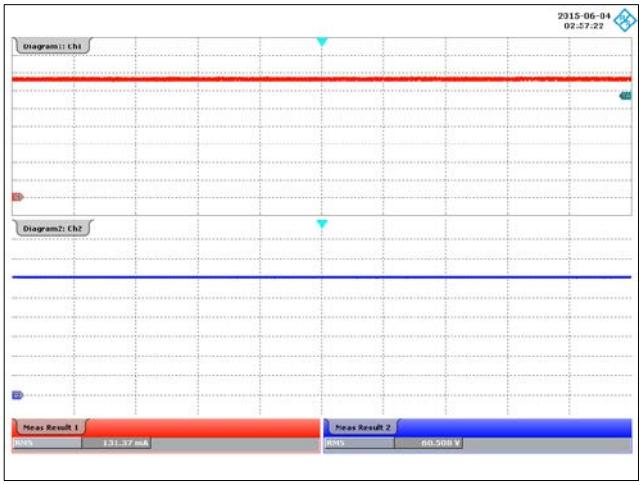


Figure 20 – 90 VAC, 60 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V / div, 10 ms / div.

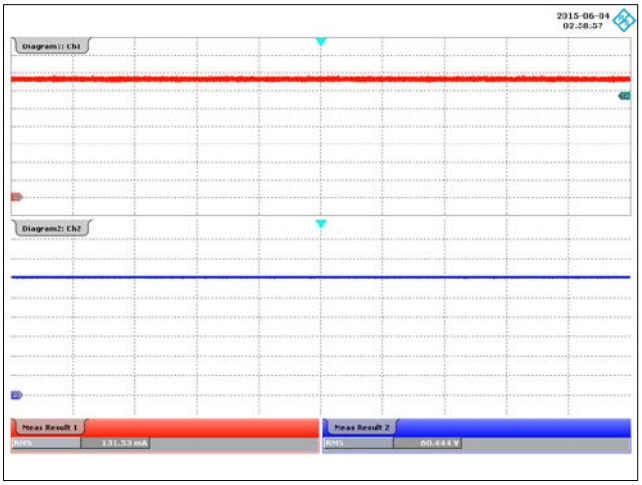


Figure 21 – 270 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V / div, 10 ms / div.

11.3 Output Voltage / Current Rise and Fall

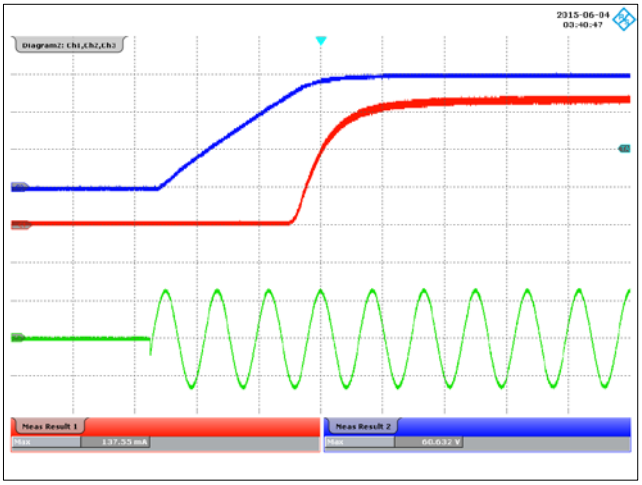


Figure 22 – 90 VAC, 60 Hz, Output Rise.
Upper: V_{OUT}, 20 V / div.
Middle: I_{OUT}, 40 mA / div.
Lower: V_{IN}, 100 V / div, 20 ms / div.

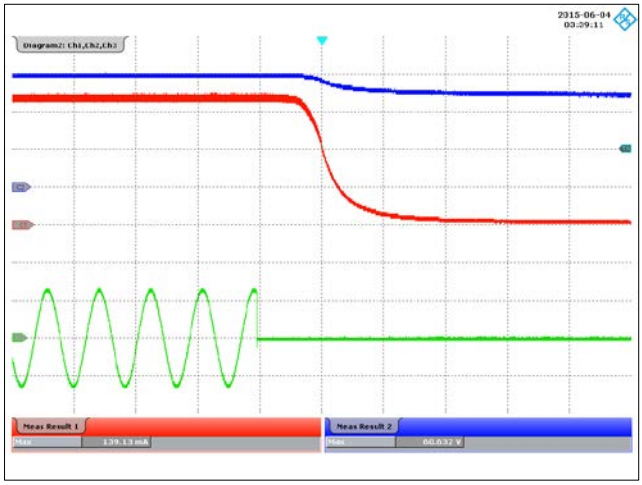


Figure 23 – 90 VAC, 60 Hz, Output Fall.
Upper: V_{OUT}, 20 V / div.
Middle: I_{OUT}, 40 mA / div.
Lower: V_{IN}, 100 V / div, 20 ms / div.

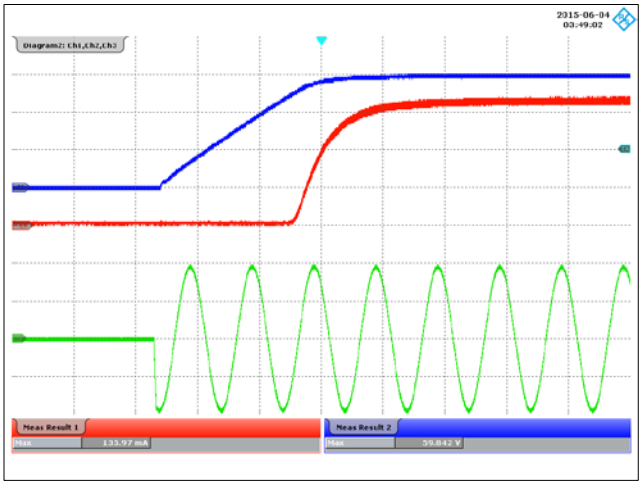


Figure 24 – 270 VAC, 50 Hz, Output Rise.
Upper: V_{OUT}, 20 V / div.
Middle: I_{OUT}, 40 mA / div.
Lower: V_{IN}, 200 V / div, 20 ms / div.

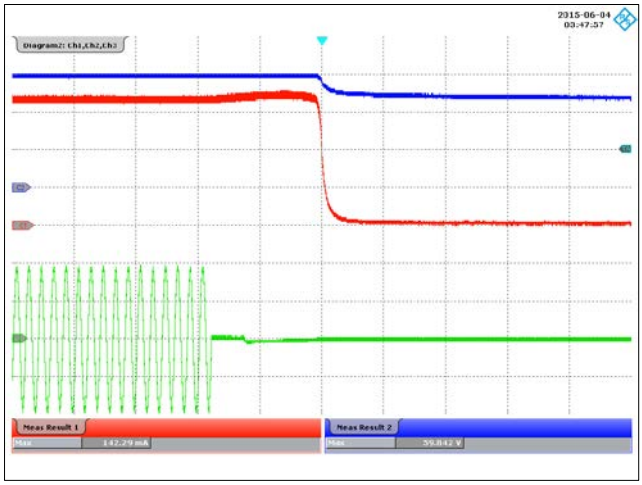


Figure 25 – 270 VAC, 50 Hz, Output Fall.
Upper: V_{OUT}, 20 V / div.
Middle: I_{OUT}, 40 mA / div.
Lower: V_{IN}, 200 V / div, 100 ms / div.

11.4 Voltage and Current Ripple

Only 0.1 μF ceramic cap was place at the voltage probe for pick-up noise filter. E-load set at CRH (Constant Resistance High) mode.

11.4.1 Constant Voltage Operation (CV)

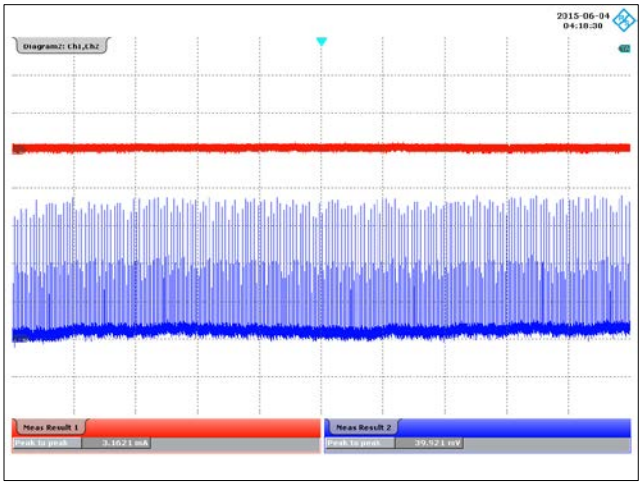


Figure 26 – 115 VAC, 60 Hz. No-load.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 10 mV, 50 ms / div.
I_{RIPPLE}: 3.1621 mA.
V_{RIPPLE}: 39.921 mV.

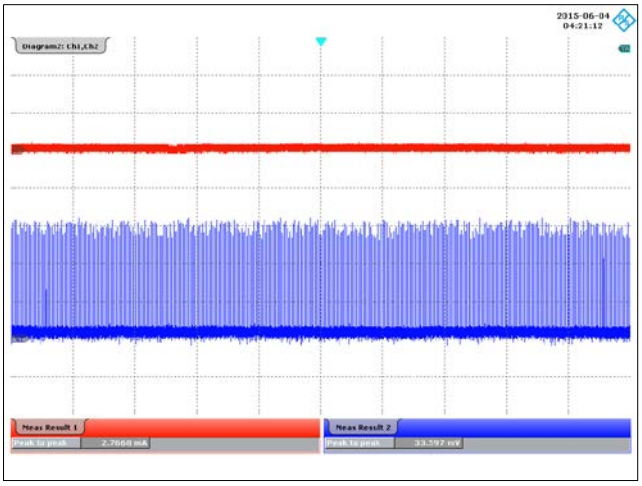


Figure 27 – 230 VAC, 60 Hz. No-load.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 10 mV, 50 ms / div.
I_{RIPPLE}: 2.7668 mA.
V_{RIPPLE}: 33.597 mV.

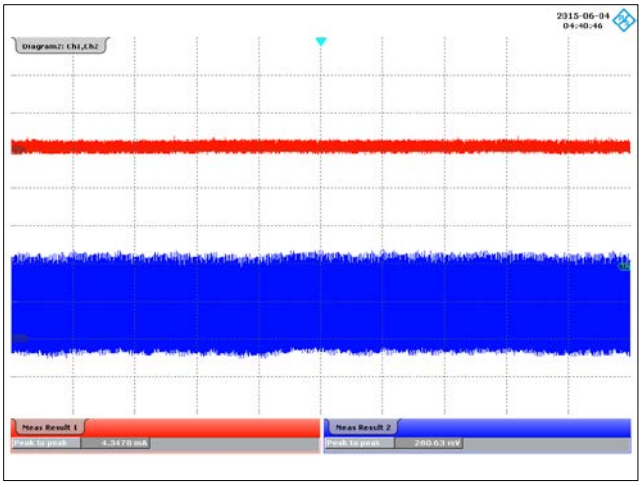


Figure 28 – 115 VAC, 50 Hz. 65 mA Load (50%).
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 4.3478 mA.
V_{RIPPLE}: 280.63 mV.

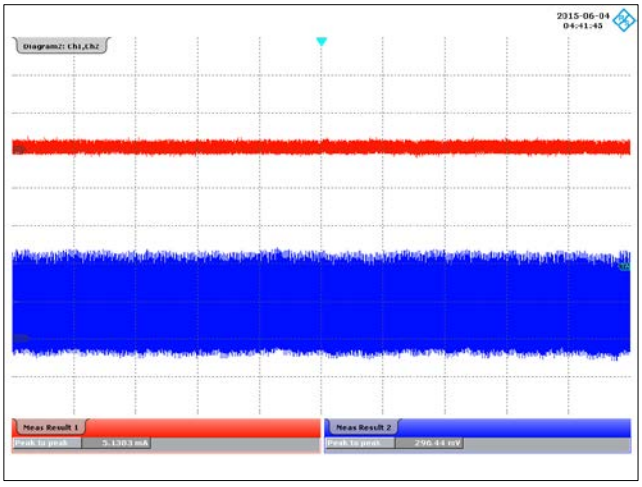


Figure 29 – 230 VAC, 60 Hz. 65 mA Load (50%).
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 500 mV, 5 ms / div.
I_{RIPPLE}: 5.1383 mA.
V_{RIPPLE}: 296.44 mV.

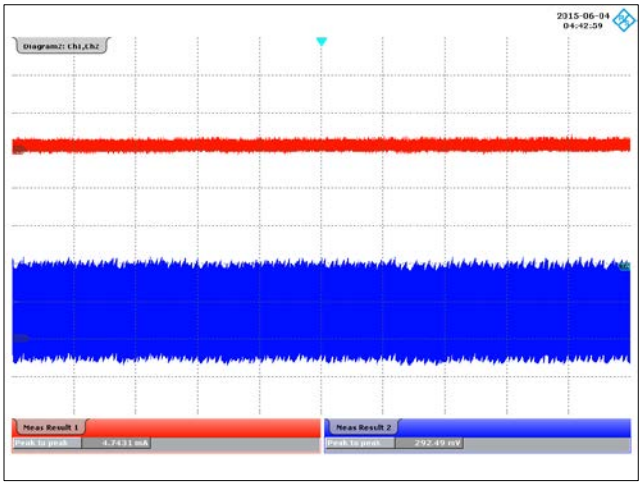


Figure 30 – 115 VAC, 50 Hz. 130 mA Load (100%).
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 4.7431 mA.
V_{RIPPLE}: 292.49 mV.

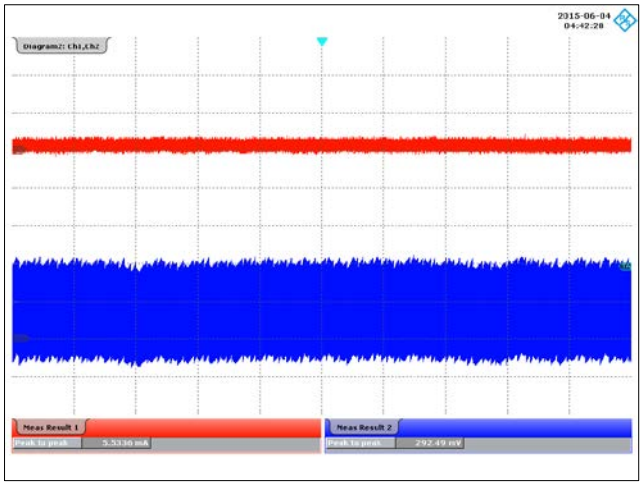


Figure 31 – 230 VAC, 60 Hz. 130 mA Load (100%).
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 5.5336 mA.
V_{RIPPLE}: 292.49 mV.

11.4.2 Constant Current Operation (CC)

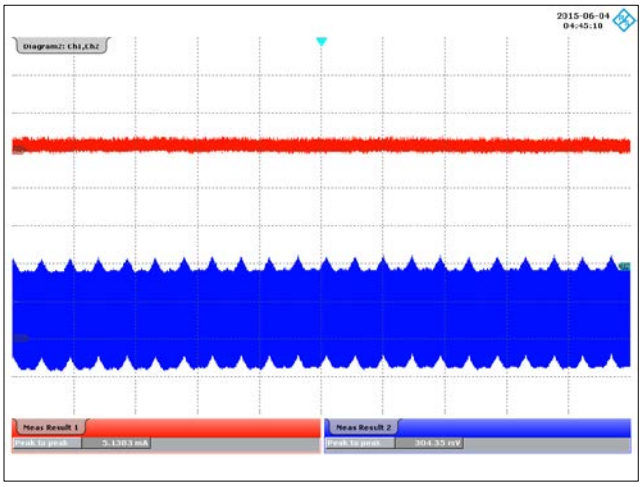


Figure 32 – 115 VAC, 60 Hz 24 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 5.1383 mA.
V_{RIPPLE}: 304.35 mV.

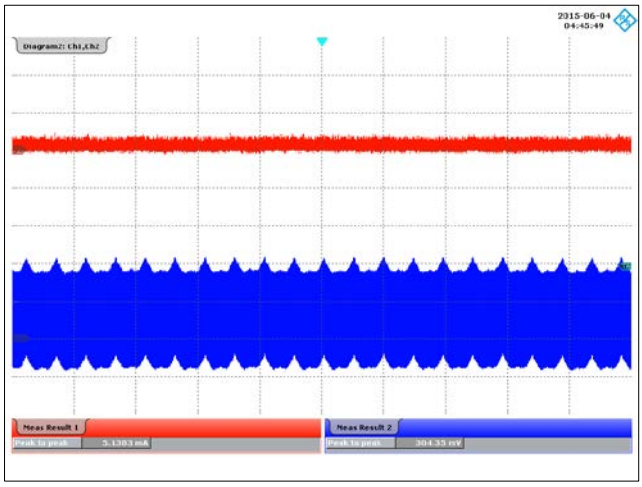


Figure 33 – 230 VAC, 50 Hz 24 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 5.1383 mA.
V_{RIPPLE}: 304.35 mV.

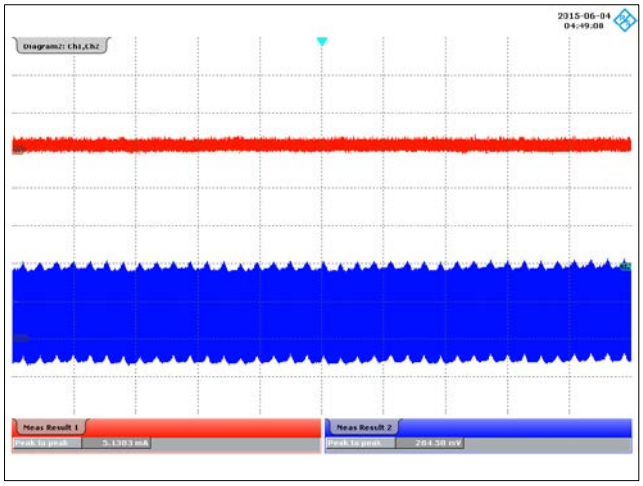


Figure 34 – 115 VAC, 50 Hz 42 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 5.1383 mA.
V_{RIPPLE}: 284.58 mV.

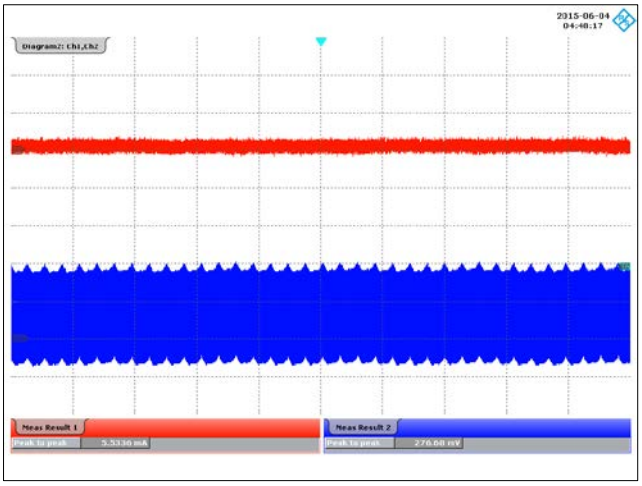


Figure 35 – 230 VAC, 60 Hz 42 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 100 mV, 5 ms / div.
I_{RIPPLE}: 5.5336 mA.
V_{RIPPLE}: 276.68 mV.

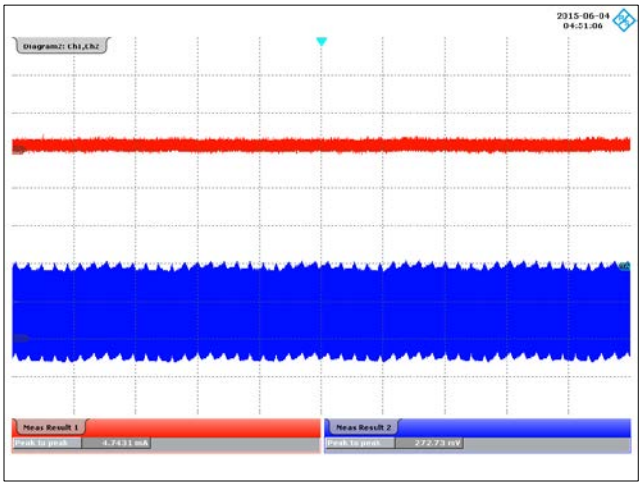


Figure 36 – 115 VAC, 50 Hz 54 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 50 mV, 5 ms / div.
I_{RIPPLE}: 4.7431 mA.
V_{RIPPLE}: 272.73 mV.

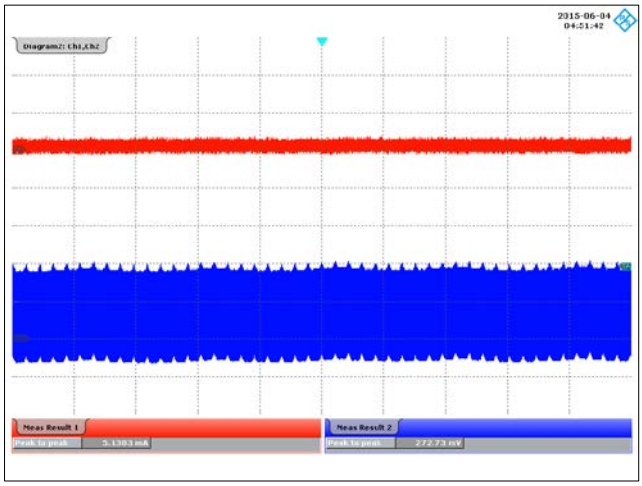


Figure 37 – 230 VAC, 60 Hz 54 V Output.
Upper: $I_{OUT(RIPPLE)}$, 10 mA / div.
Lower: $V_{OUT(RIPPLE)}$, 50 mV, 5 ms / div.
I_{RIPPLE}: 5.1383 mA.
V_{RIPPLE}: 272.73 mV.

11.5 Drain Voltage and Current at Normal Operation

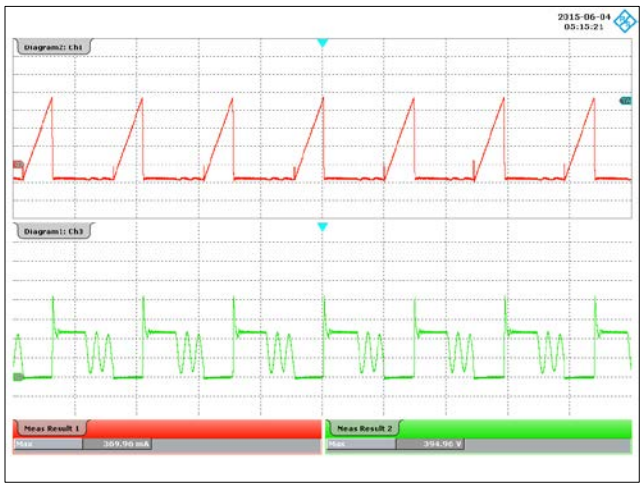


Figure 38 – 90 VAC 60 Hz, Full Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.
I_{PEAK}: 369.96 mA.
V_{DSMAX}: 394.96 V.

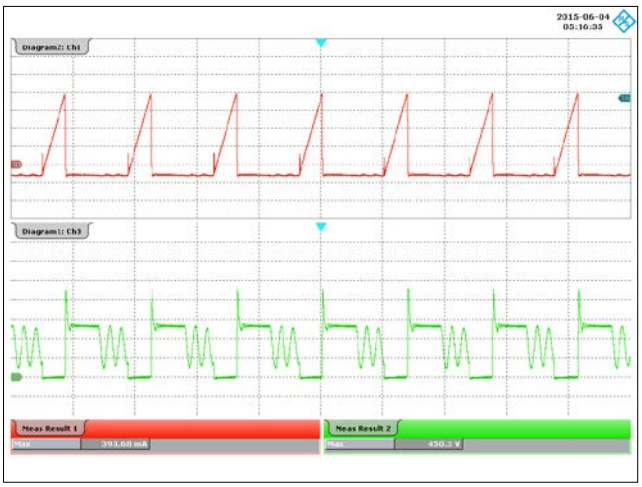


Figure 39 – 115 VAC 60 Hz, Full Load.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 200 V, 10 µs / div.
I_{PEAK}: 363.68 mA.
V_{DSMAX}: 450.3 V.

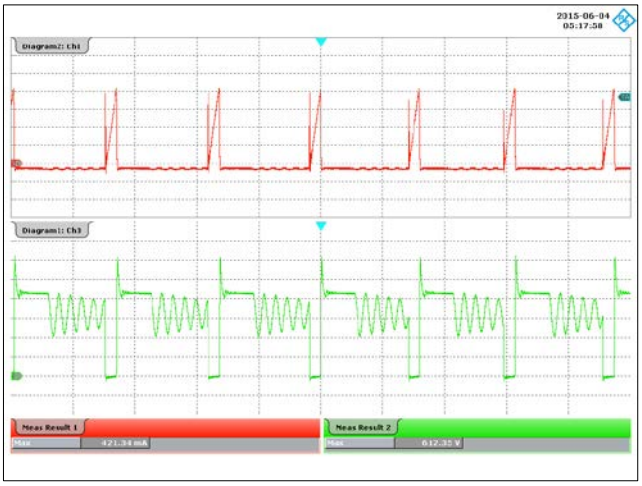


Figure 40 – 230 VAC, 50 Hz.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.
I_{PEAK}: 421.34 mA.
V_{DSMAX}: 612.35 V.

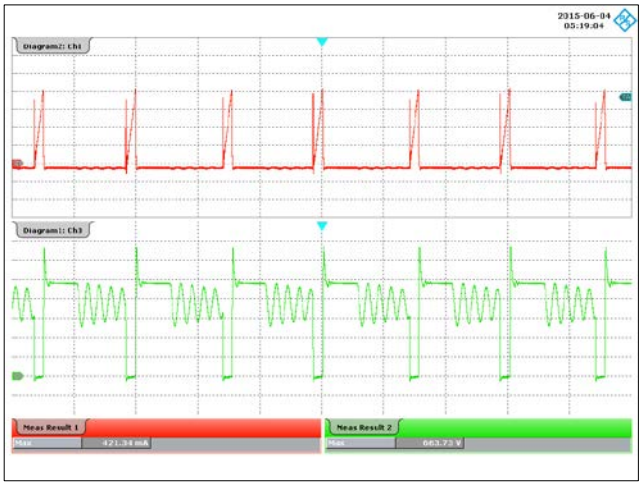


Figure 41 – 270 VAC, 50 Hz.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 10 µs / div.
I_{PEAK}: 421.34 mA.
V_{DSMAX}: 663.73 V

11.6 Start-up Drain Voltage and Current

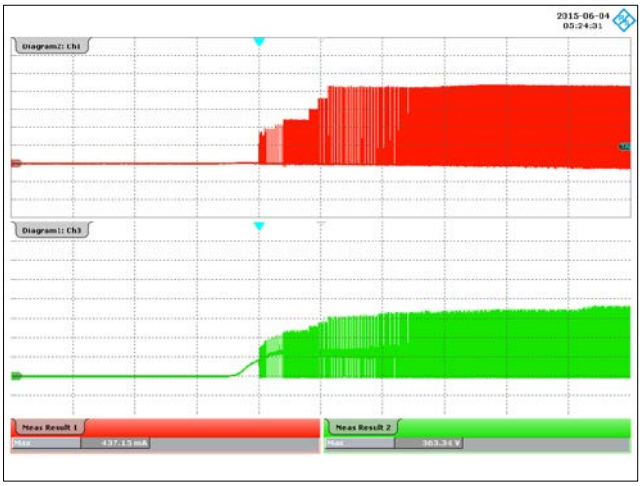


Figure 42 – 90 VAC 60 Hz, Full Load Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

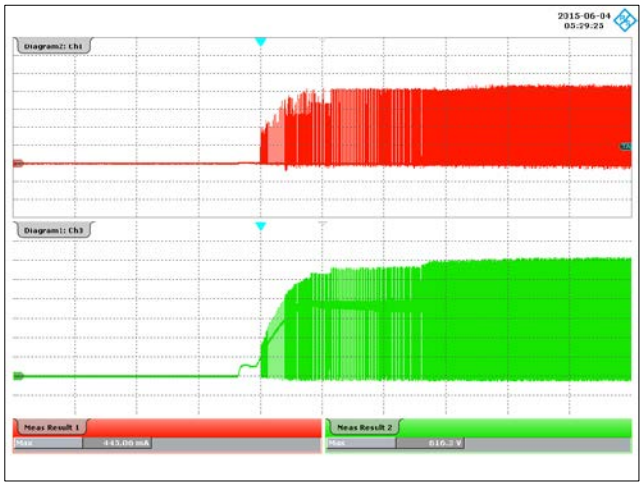


Figure 43 – 270 VAC 50 Hz, Full Load Start-up.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

11.7 Drain Current and Voltage during Output Short Condition

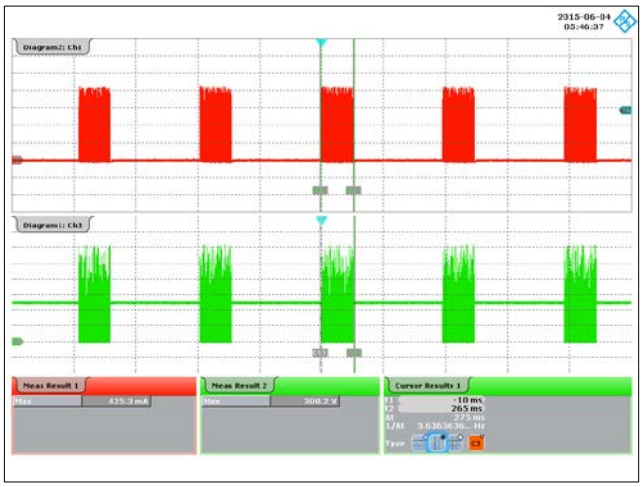


Figure 44 – 90 VAC 60 Hz, Output Short.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V, 500 ms / div.
T_{ON}: 275 ms

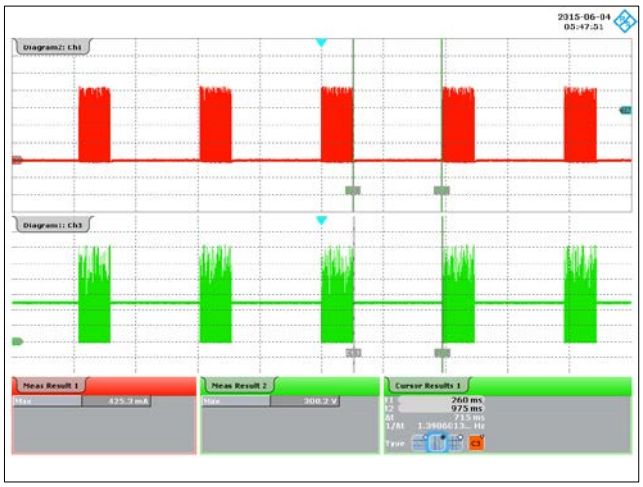


Figure 45 – 90 VAC 60 Hz, Output Short.
Upper: I_{DRAIN}, 100 mA / div.
Lower: V_{DRAIN}, 50 V, 500 ms / div.
Auto-restart Time: 715 ms

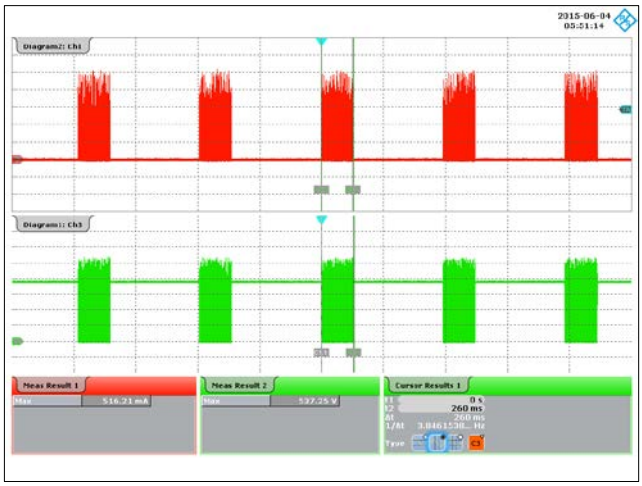


Figure 46 – 270 VAC 50 Hz, Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 500 ms / div.
T_{ON}: 260 ms

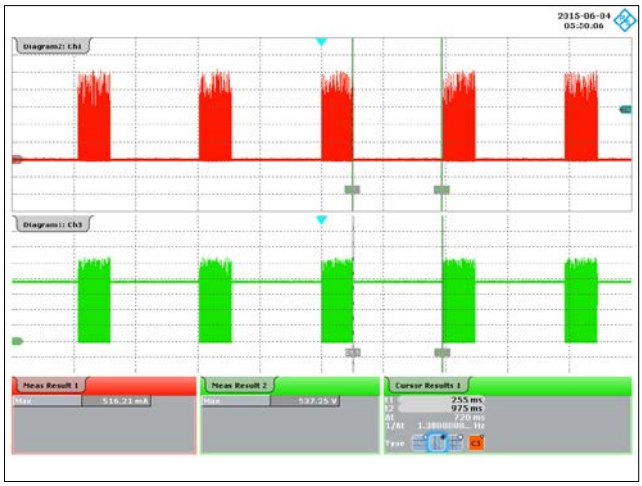


Figure 47 – 270 VAC 50 Hz, Output Short Condition.
Upper: I_{DRAIN}, 100 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 500 ms / div.
Auto-restart Time: 720 ms.

11.8 Drain Current and Voltage during Open-Loop Condition (R7 is Open)

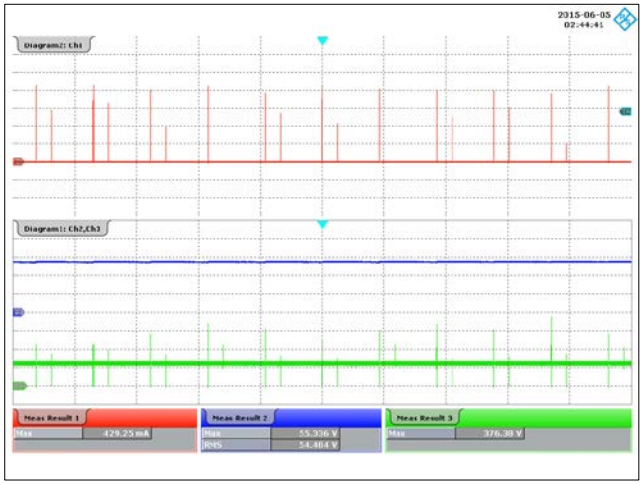


Figure 48 – 90 VAC 60 Hz, Open-loop Condition.
Upper: I_{DRAIN}, 100 mA / div.
Middle: $V_{OUT,}$ 20 V / div.
Lower: $V_{DRAIN,}$ 100 V, 1 s / div.

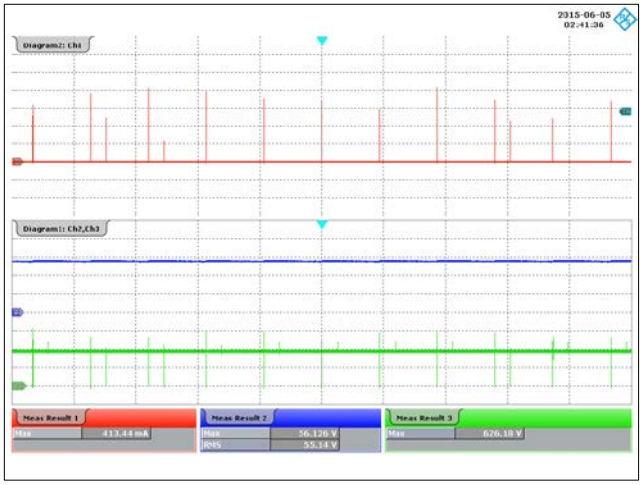


Figure 49 – 270 VAC 50 Hz, Open-loop Condition.
Upper: I_{DRAIN}, 100 mA / div.
Middle: $V_{OUT,}$ 20 V / div.
Lower: $V_{DRAIN,}$ 200 V, 1 s / div.

11.9 Output Diode Current and Voltage Waveforms Normal Operation

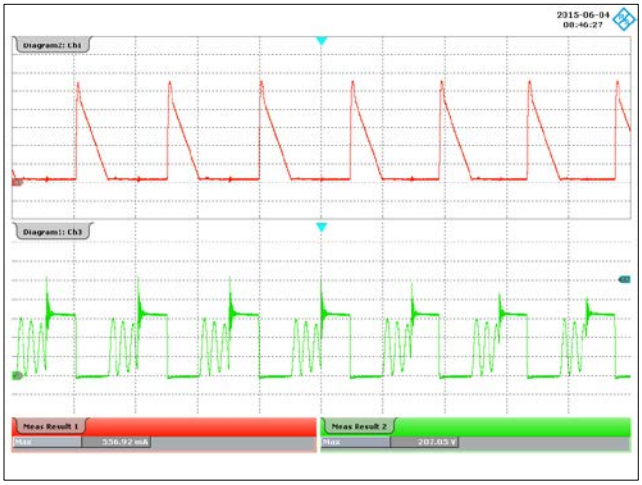


Figure 50 – 90 VAC 60 Hz, Full Load.
Upper: I_{D3}, 100 mA / div.
Lower: V_{D3}, 40 V, 10 µs / div.
I_{D3MAX}: 556.92 mA.
V_{D3MAX}: 207.05 V.

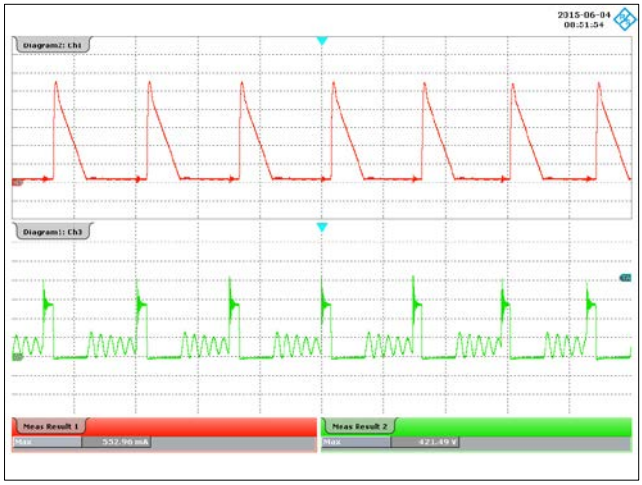


Figure 51 – 270 VAC 50 Hz, Full Load
Upper: I_{D3}, 100 mA / div.
Lower: V_{D3}, 100 V, 10 µs / div.
I_{D3MAX}: 588.54 mA.
V_{D3MAX}: 166.25 V.

11.10 Output Diode Current and Voltage Short-Circuit Waveforms

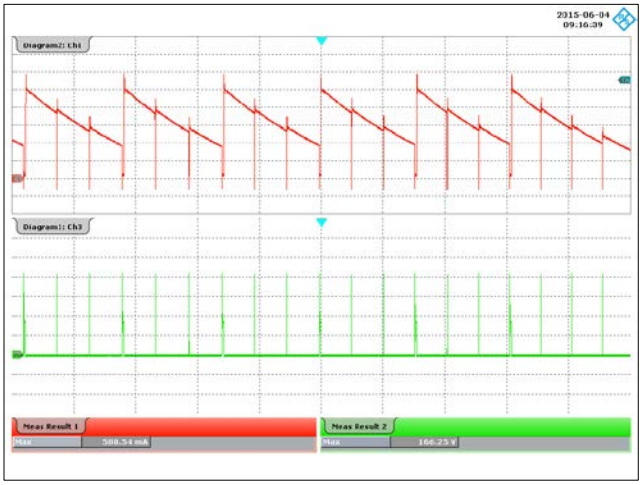


Figure 52 – 90 VAC, 60 Hz.
Upper: I_{D3}, 100 mA / div.
Lower: V_{D3}, 40 V / div, 100 µs / div.
I_{D3MAX}: 588.54 mA.
V_{D3MAX}: 166.25 V.

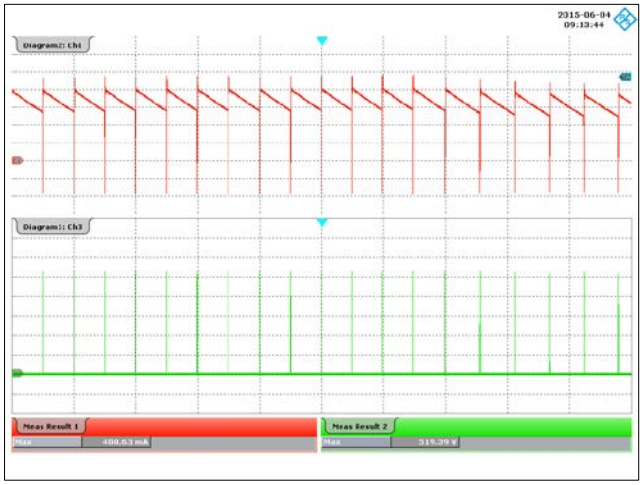


Figure 53 – 270 VAC, 50 Hz.
Upper: I_{D3}, 100 mA / div.
Lower: V_{D3}, 100 V, 100 µs / div.
I_{D3MAX}: 480.63 mA.
V_{D3MAX}: 519.39 V.

11.11 Brown-out / Brown-in

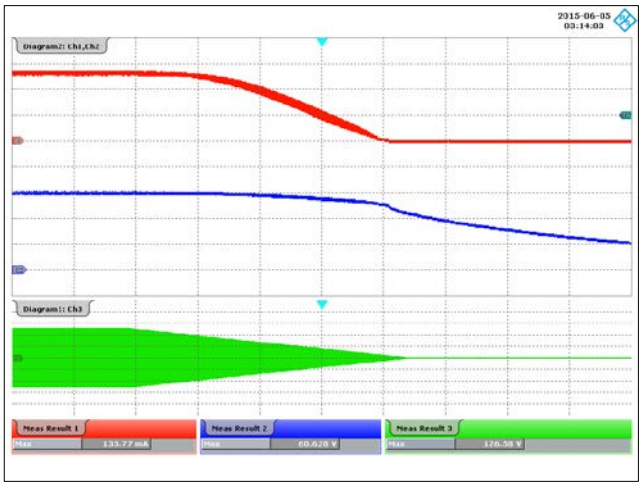


Figure 54 – 60 V Output, Brown-out Condition.
(1 V / s Decay Rate).
Upper: I_{OUT}, 50 mA / div.
Middle: V_{OUT}, 20 V / div.
Lower: V_{IN}, 50 V / div, 20 s / div.

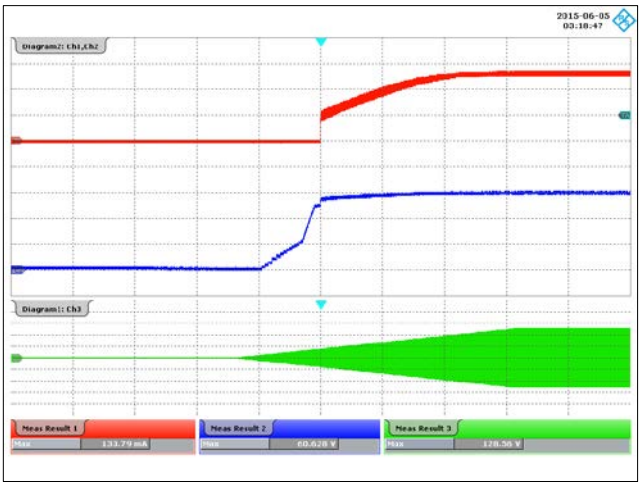


Figure 55 – 60 V Output, Brown-in Condition.
(1 V / s Ramp Rate).
Upper: I_{OUT}, 50 mA / div.
Middle: V_{OUT}, 20 V / div.
Lower: V_{IN}, 50 V / div, 20 s / div.

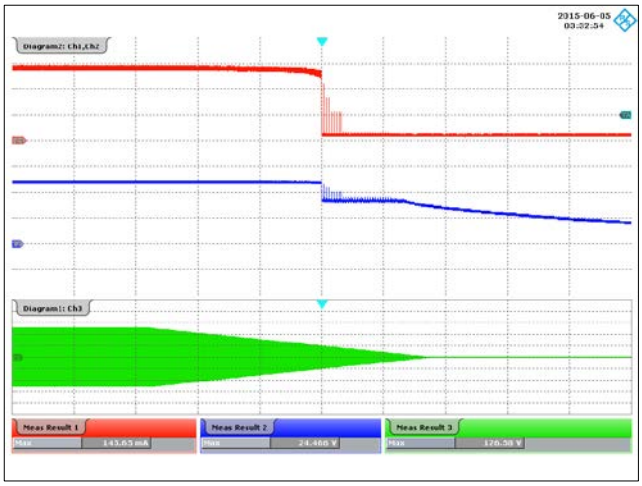


Figure 56 – 24 V Output, Brown-out Condition.
(1 V / s Decay Rate).
Upper: I_{OUT}, 50 mA / div.
Middle: V_{OUT}, 10 V / div.
Lower: V_{IN}, 50 V / div, 20 s / div.

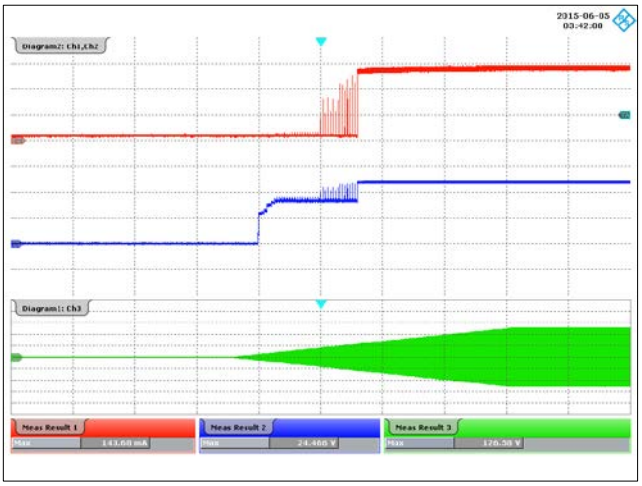


Figure 57 – 24 V Output, Brown-in Condition.
(1 V / s Ramp Rate).
Upper: I_{OUT}, 50 mA / div.
Middle: V_{OUT}, 10 V / div.
Lower: V_{IN}, 50 V / div, 20 s / div.

11.12 Line Transient

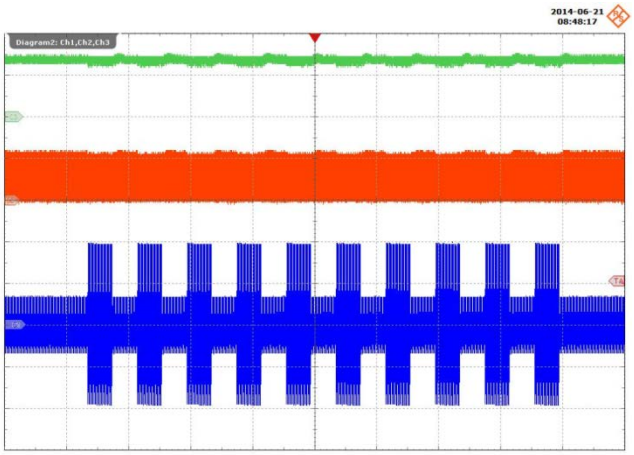


Figure 58 – 90 VAC to 270 VAC Line Transient.
Upper: I_{OUT}, 100 mA / div.
Middle: I_{DRAIN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 1 s/ div.

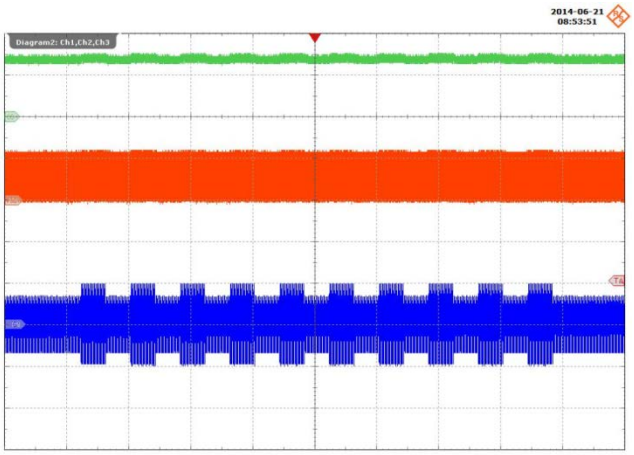


Figure 59 – 90 VAC to 132 VAC Line Transient.
Upper: I_{OUT}, 100 mA / div.
Middle: I_{DRAIN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 1 s/ div.

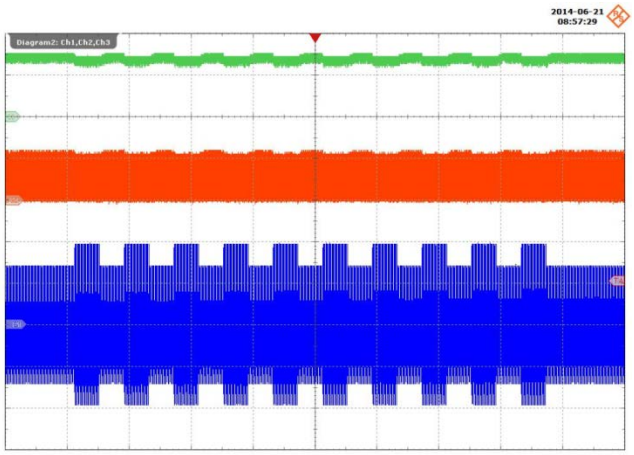


Figure 60 – 195 VAC to 270 VAC Line Transient.
Upper: I_{OUT}, 100 mA / div.
Middle: I_{DRAIN}, 400 mA / div.
Lower: V_{IN}, 200 V / div., 1 s/ div.

11.13 300 ms ON, 300 ms OFF AC Cycling

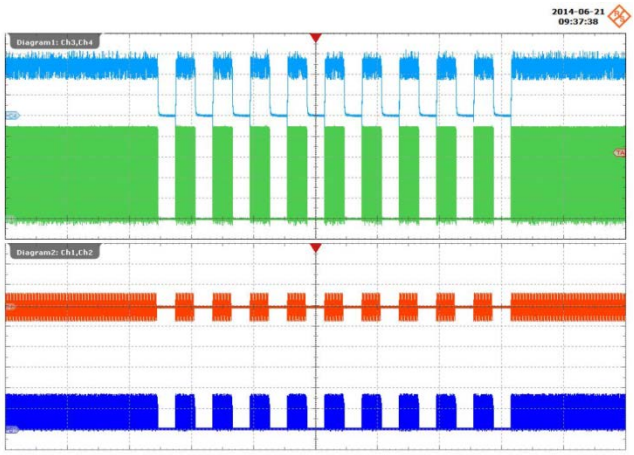


Figure 61 – 90 VAC, 300 ms ON-OFF Cycling.
Upper: I_{OUT}, 100 mA / div.
Upper Middle: I_{DRAIN}, 100 mA / div.
Lower Middle: V_{IN}, 200 V / div.
Lower: V_{DRAIN}, 200 V / div., 1 s / div.

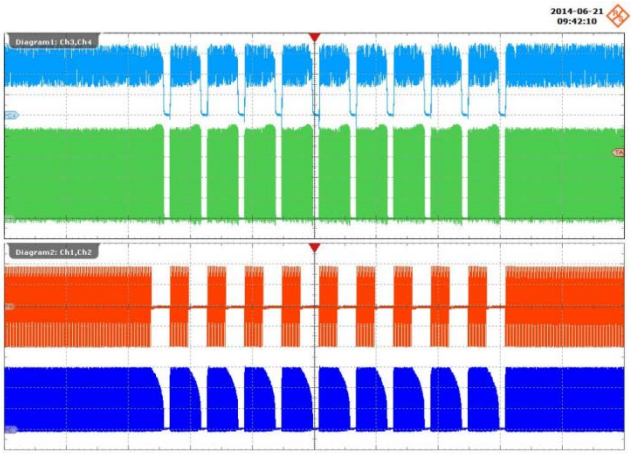


Figure 62 – 270 VAC, 300 ms ON-OFF Cycling.
Upper: I_{OUT}, 100 mA / div.
Upper Middle: I_{DRAIN}, 100 mA / div.
Lower Middle: V_{IN}, 200 V / div.
Lower: V_{DRAIN}, 200 V / div., 1 s / div.

12 Conducted EMI

The unit was tested using LED load (54 V, 130 mA) for CC and Resistor-LED load (60 V, 118 mA) for CV.

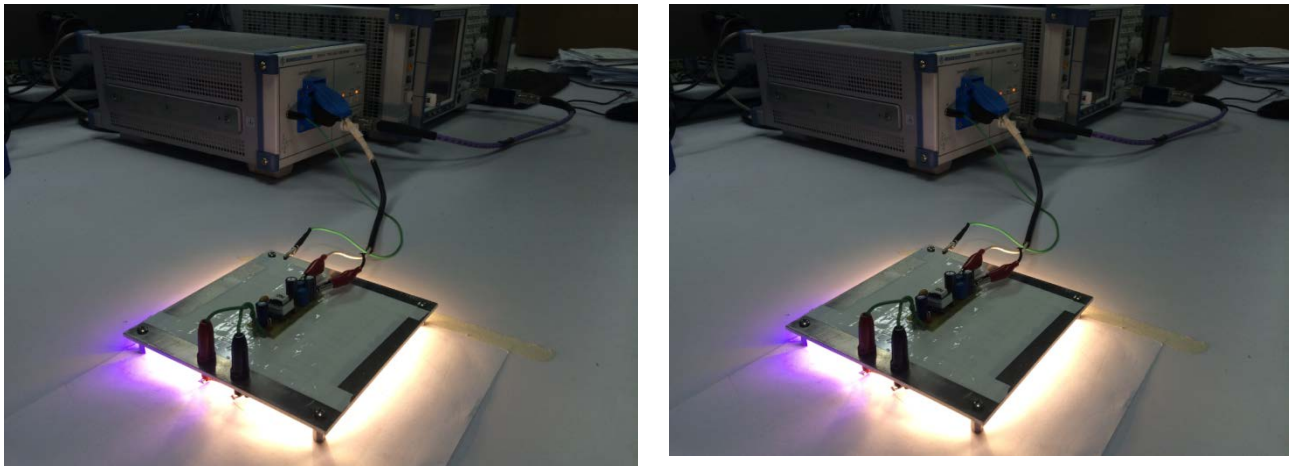


Figure 63 – Conducted EMI Set-up (With and Wwithout EARTH Connection).

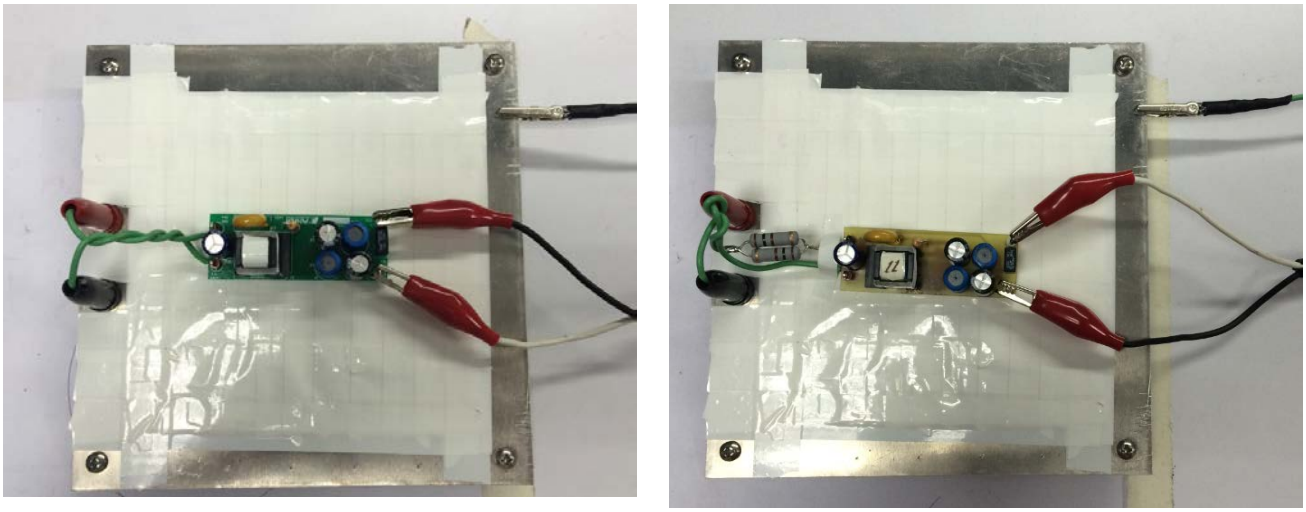
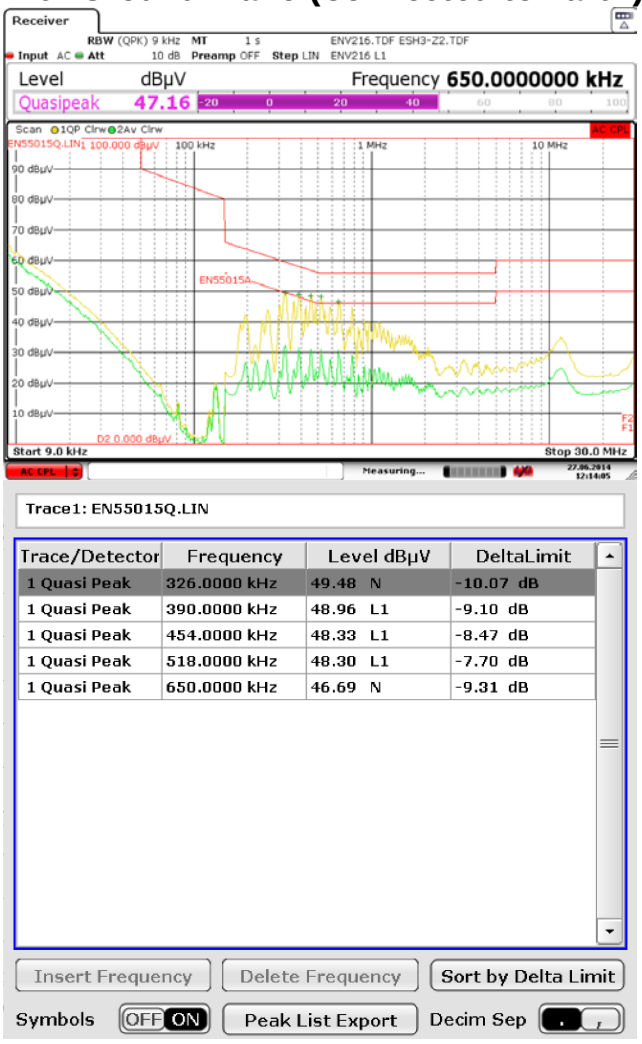


Figure 64 – CC (LED Load) and CV (Resistor-LED Load) Conducted EMI Set-up.

12.1 Conducted EMI at Constant Current

With Ground Plane (Connected to Earth)



With Ground Plane (Floating)

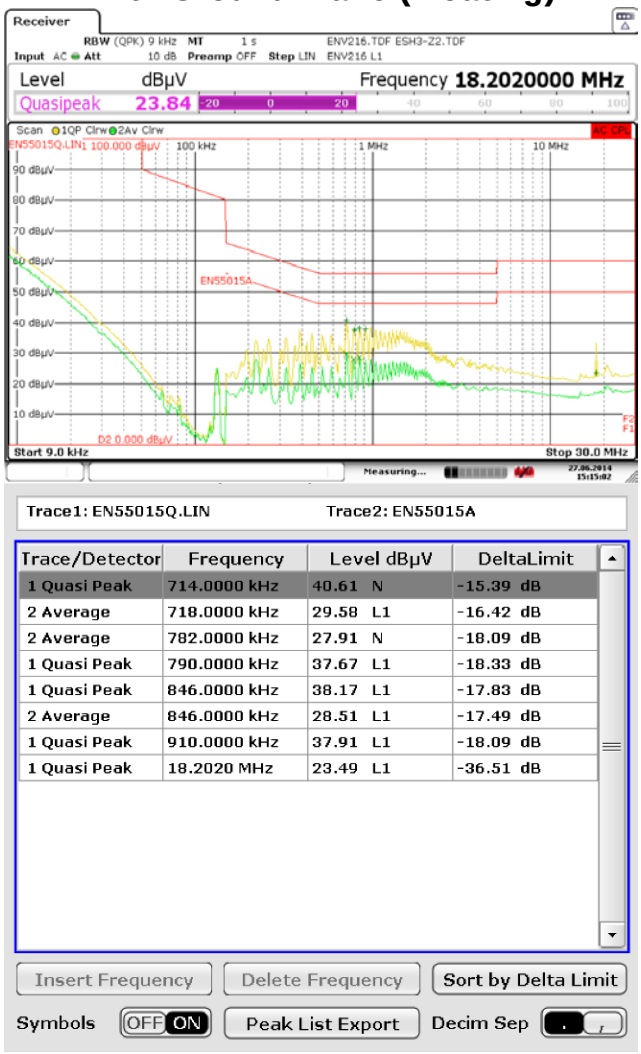
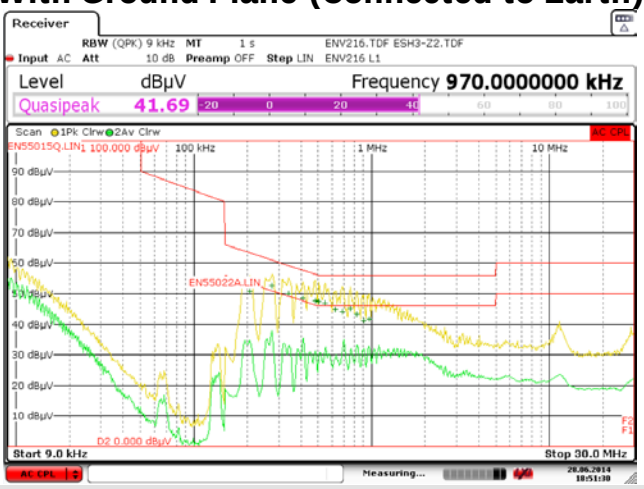


Figure 65 – 230 VAC, 60 Hz, 55 V 130 mA LED Load, EN55015 B Limits (Quasi-Peak Scan).

With Ground Plane (Connected to Earth)



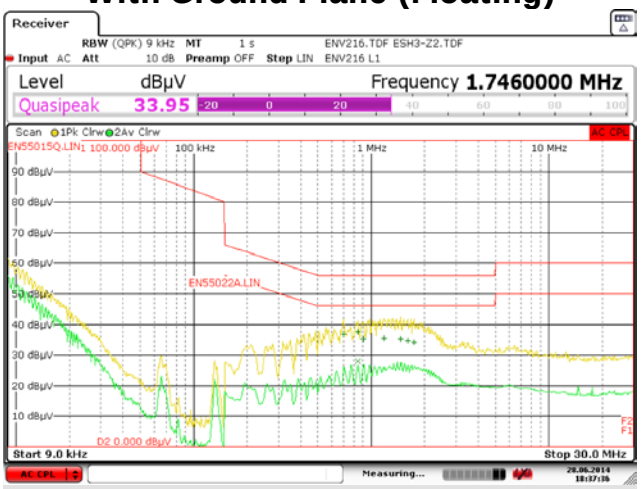
Trace1: EN55015Q.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	206.0000 kHz	50.69 N	-12.68 dB
1 Quasi Peak	274.0000 kHz	52.51 N	-8.49 dB
1 Quasi Peak	342.0000 kHz	50.07 L1	-9.08 dB
1 Quasi Peak	410.0000 kHz	48.47 L1	-9.18 dB
1 Quasi Peak	486.0000 kHz	47.78 L1	-8.46 dB
1 Quasi Peak	506.0000 kHz	47.41 L1	-8.59 dB
1 Quasi Peak	546.0000 kHz	46.85 L1	-9.15 dB
1 Quasi Peak	622.0000 kHz	44.80 L1	-11.20 dB
1 Quasi Peak	686.0000 kHz	44.08 N	-11.92 dB
1 Quasi Peak	762.0000 kHz	45.05 N	-10.95 dB
1 Quasi Peak	822.0000 kHz	43.37 N	-12.63 dB
1 Quasi Peak	902.0000 kHz	41.07 L1	-14.93 dB
1 Quasi Peak	970.0000 kHz	41.72 N	-14.28 dB

Insert Frequency | Delete Frequency | Sort by Delta Limit

Symbols OFF ON | Peak List Export | Decim Sep . ,

With Ground Plane (Floating)



Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	698.0000 kHz	36.87 L1	-19.13 dB
1 Quasi Peak	838.0000 kHz	37.60 L1	-18.40 dB
2 Average	838.0000 kHz	27.90 N	-18.10 dB
1 Quasi Peak	906.0000 kHz	35.32 N	-20.68 dB
1 Quasi Peak	1.1860 MHz	35.53 N	-20.47 dB
1 Quasi Peak	1.4660 MHz	35.27 N	-20.73 dB
1 Quasi Peak	1.6060 MHz	34.73 L1	-21.27 dB
1 Quasi Peak	1.7460 MHz	34.07 N	-21.93 dB

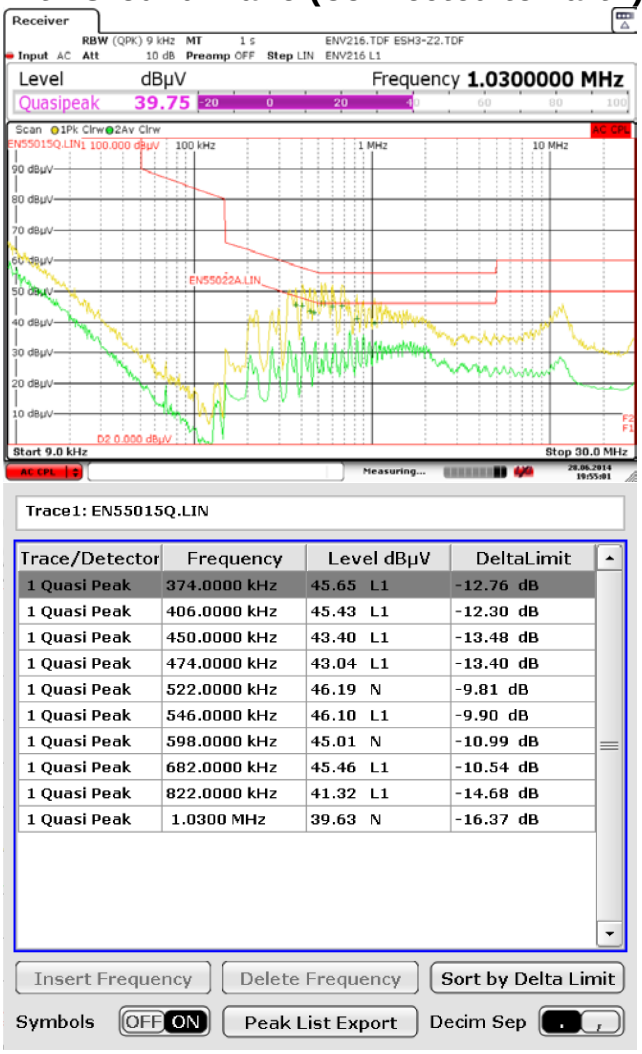
Insert Frequency | Delete Frequency | Sort by Delta Limit

Symbols OFF ON | Peak List Export | Decim Sep . ,

Figure 66 – 115 VAC, 60 Hz, 55 V 130 mA LED Load, EN55015 B Limits (Peak Scan).

12.2 Conducted EMI at Constant Voltage

With Ground Plane (Connected to Earth)



With Ground Plane (Floating)

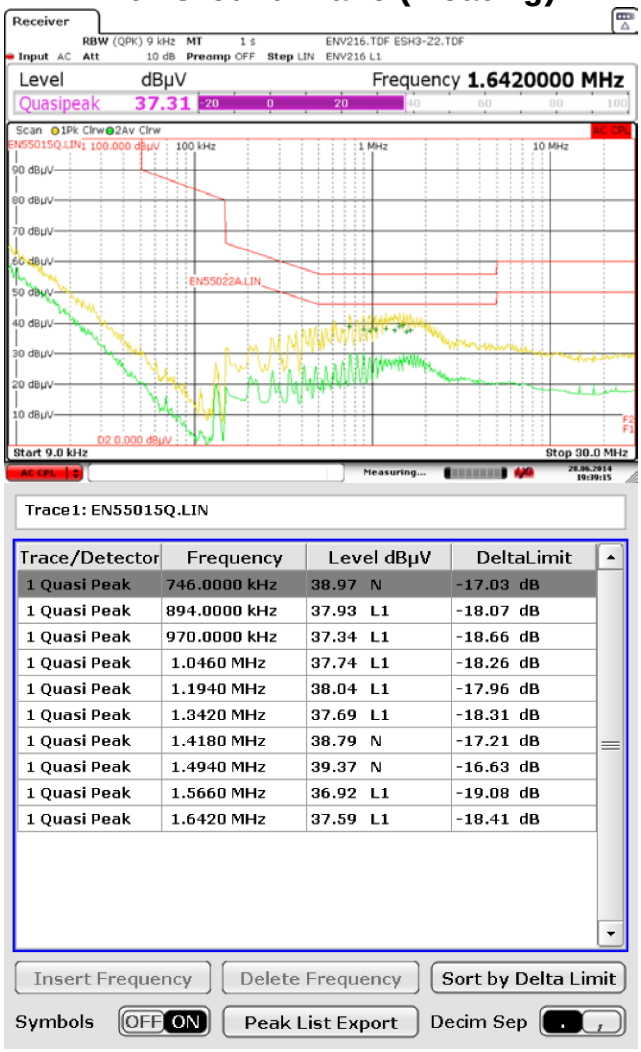
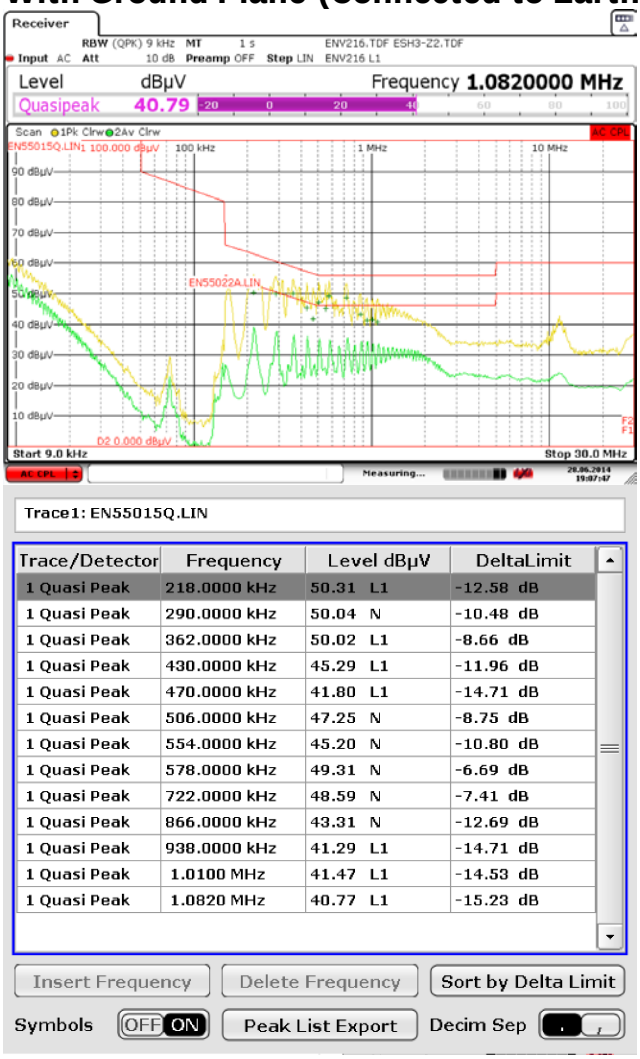


Figure 67 – 230 VAC, 60 Hz, 60 V 118 mA Resistor-LED Load, EN55015 B Limits (Peak Scan).

With Ground Plane (Connected to Earth)



With Ground Plane (Floating)

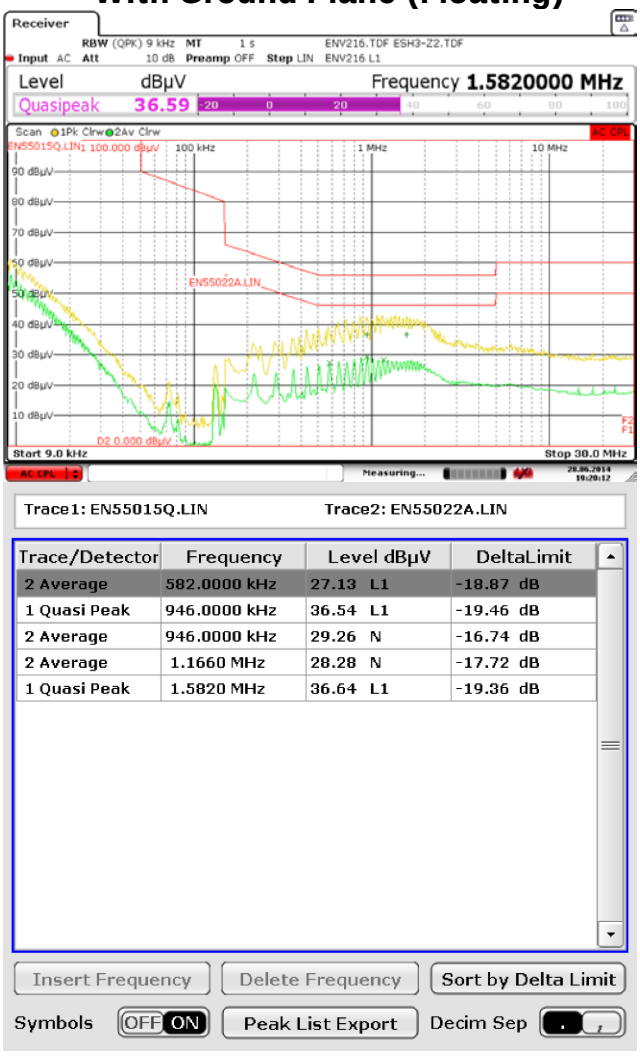


Figure 68 – 115 VAC, 60 Hz, 60 V 118 mA Resistor-LED Load, EN55015 B Limits (Peak Scan).

13 Line Surge Test

The unit was subjected to ±2500 V, 100 kHz ring wave and ±500 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

Figure 69 – (+) 500 V Differential Surge, 90°.
Upper: V_{DRAIN}, 500 V / div.
Lower: V_{C1}, 200 V, 100 µs / div.

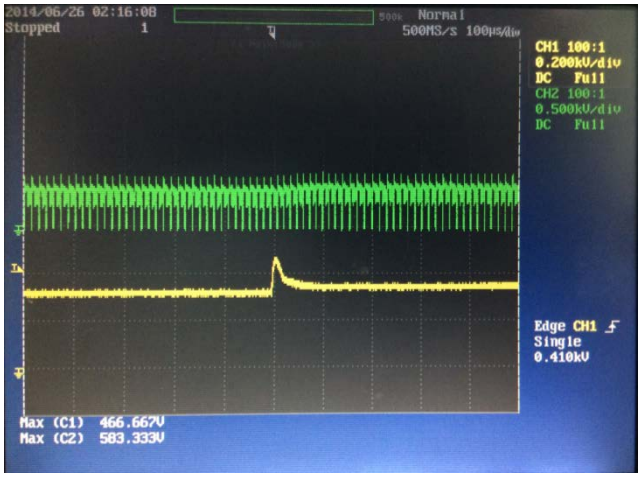


Figure 70 – (+) 500 V Differential Surge, 0°.
Upper: V_{DRAIN}, 500 V / div.
Lower: V_{C1}, 200 V, 100 µs / div.

13.1 1 kV Differential Line Surge Options

For 1 kV differential line surge requirements, C1 is still surviving but with excessive voltage stress as seen in figure below and with continuous repetition will damage the component. Replacement with 22 µF capacitor is recommended to limit the voltage stress. Alternatively, adding an MOV may also be used.

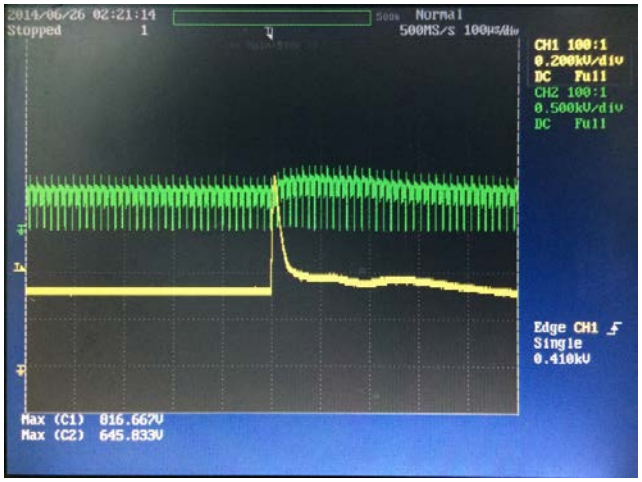


Figure 71 – (+) 1000 V Differential Surge, 90º.
Upper: V_{DRAIN}, 500 V / div.
Lower: V_{C1}, 200 V, 100 µs / div.

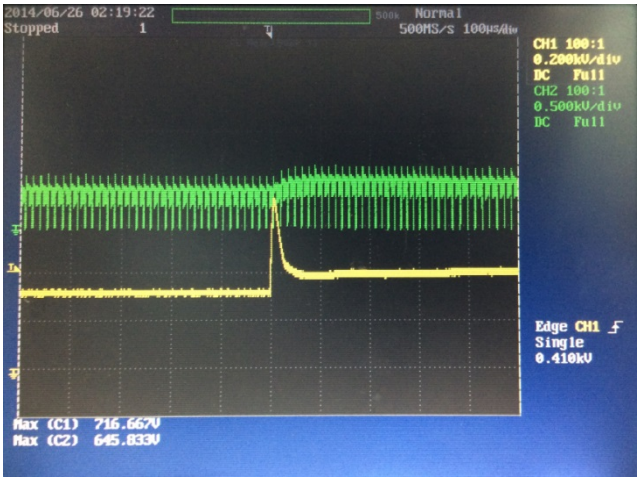


Figure 72 – (+) 1000 V Differential Surge, 0º.
Upper: V_{DRAIN}, 500 V / div.
Lower: V_{C1}, 200 V, 100 µs / div.

14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
01-July-14	AP	1.0	Initial Release	Apps & Mktg
05-June-15	AP	2.0	Redesign with new PIXls revision and LYTSwitch-2 update for ripple fix.	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

UK
Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5,
2nd Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com