Design Example Report

Title	***Universal Input, 22 V to 48 V Output, 180 mA, Isolated Flyback CC/CV LED Driver Using LYTSwitch™-2 LYT2004E***
Specification	90 VAC – 265 VAC Input; 22 V to 48 V, 180 mA Output
Application	External Ballast LED Driver
Author	Applications Engineering Department
Document Number	DER-424
Date	August 22, 2014
Revision	1.1

Summary and Features

- Accurate (primary-side control) constant current and constant voltage
  - Accurate constant current (CC) of less than ±5% variation over load and line
  - Accurate constant voltage (CV) of ±5% across line and load
- Wide operating load - voltage range (22 V to 48 V)
- Efficiency >86% at 230 VAC
- Low component count (21), small PCB
- Fast start-up time (<100 ms) – no perceptible delay
- No-load consumption <35 mW at 230 VAC
- Integrated protection and reliability features
  - Output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis
  - No damage during brown-out conditions
  - Easily meets EN55015 and CISPR-22 Class B EMI standards

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Table of Contents

Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a universal input, 22 V to 48 V, 180 mA LED driver. The power supply utilizes the LYT2004E device from the Power Integrations LYTSwitch-2 family.

This document contains the power supply and transformer specifications, schematics, bill of materials, and typical performance characteristics.

Figure 1 – Populated Circuit Board, Angle View.

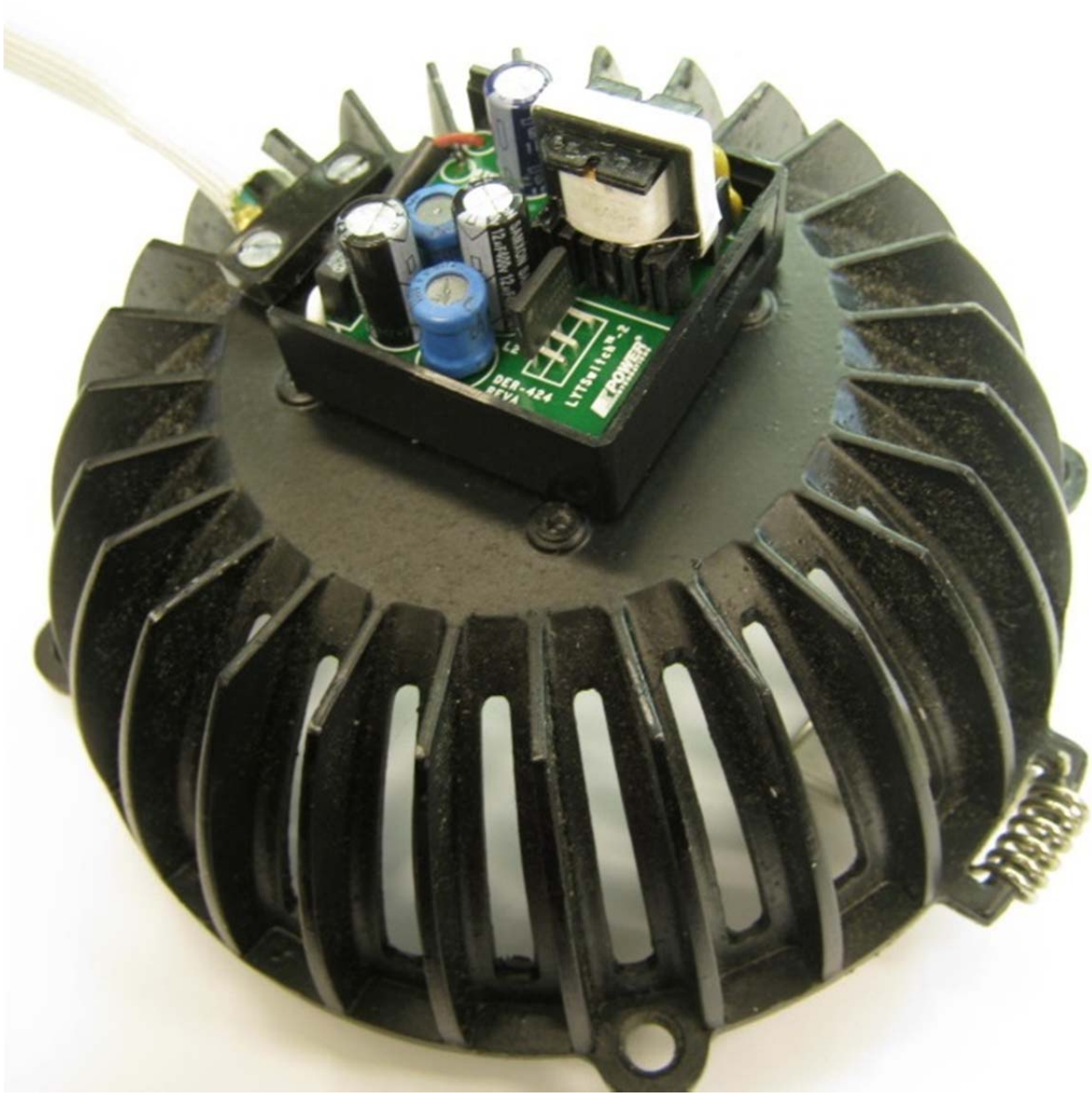

Figure 2 – Populated Circuit Board.

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Figure 3 – Populated Circuit Board, Top View.

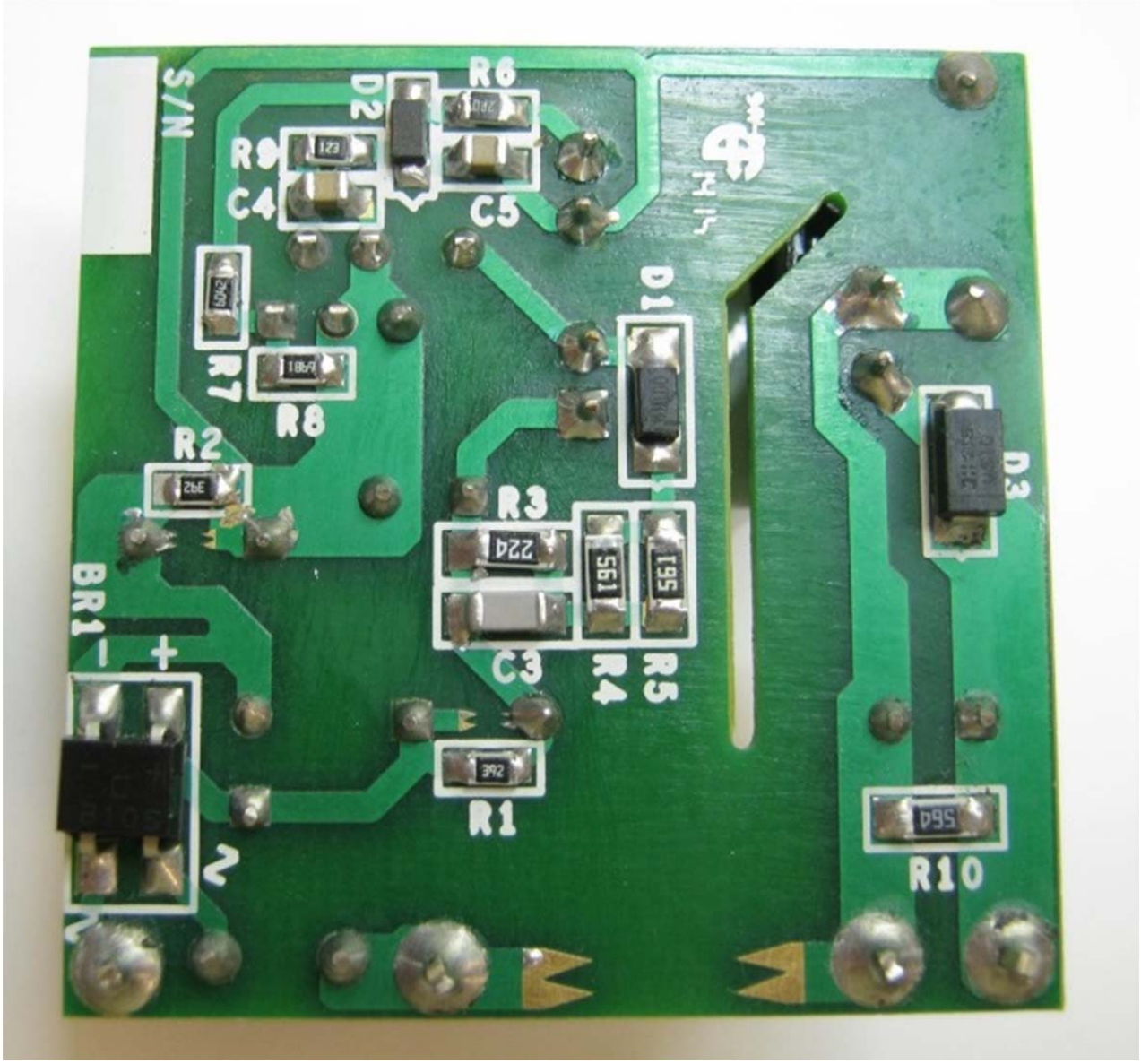

Figure 4 – Populated Circuit Board, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
No-load Input Power	P_{NL}		33		mW	Measure at V_{IN} = 230 VAC
Output						
Output Voltage	V_{OUT}	22		48	V	
Output Current	I_{OUT}		180		mA	25 ºC
Total Output Power						
Continuous Output Power	P_{OUT}			8.64	W	
Efficiency						
Full Load	η		86		%	Measured at P_{OUT} 25 ºC
Environmental						
Conducted EMI		CISPR 15B / EN55015B				>6 dB Margin
Safety		Designed to meet IEC950, UL1950 Class II				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	1.2//50 μs surge, IEC 1000-4-5, Series Impedance: 2 Ω
Differential Surge			500		V	
ESD						
Contact Discharge		-8		+8	kV	IEC 61000-4-2
Air Discharge		-15		+15	kV	
Ambient Temperature	T_{AMB}		40		°C	

3 Schematic

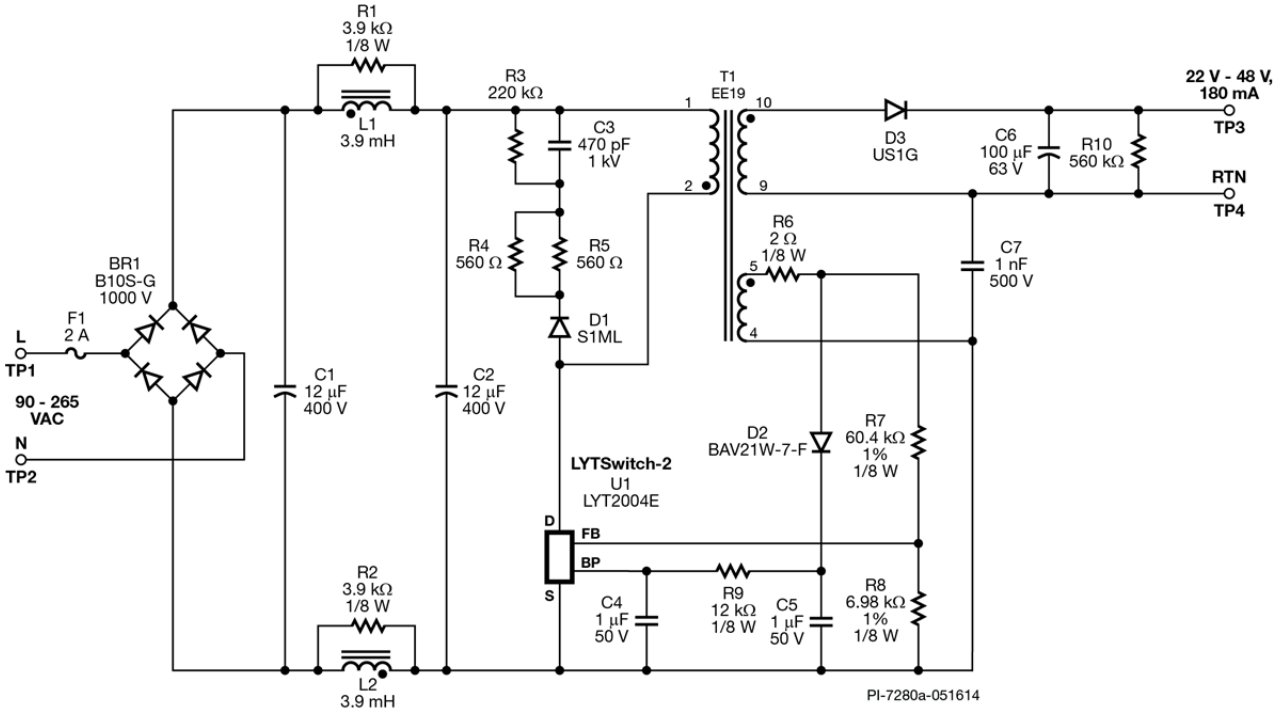

Figure 5 – Schematic.

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4 Circuit Description

4.1 Input Filter

AC power is rectified by bridge rectifier BR1. Inductors L1, L2, and capacitors C1, C2, form a pi (π) filter to attenuate conducted differential-mode EMI noise. This configuration, along with the transformer design, grounding of the transformer core and adding Y capacitor C7, allows the design to meet EMI EN55022 class B with good margin, even when there is a ground plane terminated to earth, (which typically causes high common-mode noise). Resistors R1 and R2 damp the self-resonance of the inductors L1 and L2 to avoid noise peaking at their resonant frequency.

The effect of magnetic coupling between L1 and L2 is controlled in order to yield consistent EMI performance. In this design, the start and finish of the windings are specified and indicated by a dot on the schematic and on the PCB. (See inductor manufacturer data sheet for information about the start and finish.)

4.2 LYTSwitch-2 Primary

The LYTSwitch-2 device (U1) incorporates the power switching MOSFET, oscillator, CV/CC control engine, and start-up and protection all on one IC. The integrated 700 V power MOSFET allows good voltage margin in universal input AC applications, including extended line swells.

The rectified and filtered input voltage is applied to one end of the transformer (T1) primary winding. The other side of the transformer's primary winding is driven by the internal MOSFET of U1. An RCD-R clamp consisting of D1, R3, R4, R5 and C3 limits drain voltage spikes caused by leakage inductance. The clamp circuit is optimized in order to prevent excessive ringing of the drain voltage which may affect CC regulation. R4 and R5 are connected in parallel for thermal management.

The external bias from the, D2, C5, and R9 combination improves efficiency and reduces no-load input power to less than 50 mW. Capacitor C4 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller.

4.3 Output Rectification

The secondary output from the transformer is rectified by D3, and filtered by C6. The value the output capacitor C6 is selected to provide <30% output current ripple based on a typical LED load. However, the ripple current may be different depending on the type of LEDs used due to different dynamic resistance values. The value of C6 should be adjusted according to the load.

4.4 Regulation

The LYTSwitch-2 device regulates the output using ON/OFF control for CV regulation, and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R7 and R8) were selected using standard 1% resistor values to center both the no-load output voltage and constant current regulation

thresholds. Resistor R10 provides a minimum load to maintain output regulation when the output is unloaded. Resistor R6 provides filtering of the feedback which is especially helpful at no-load in order to keep the output voltage stable. The value of R6 must be kept low to prevent output voltage creeping up and to avoid the need for a bigger pre-load resistor (R10), which lowers efficiency.

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5 PCB Layout

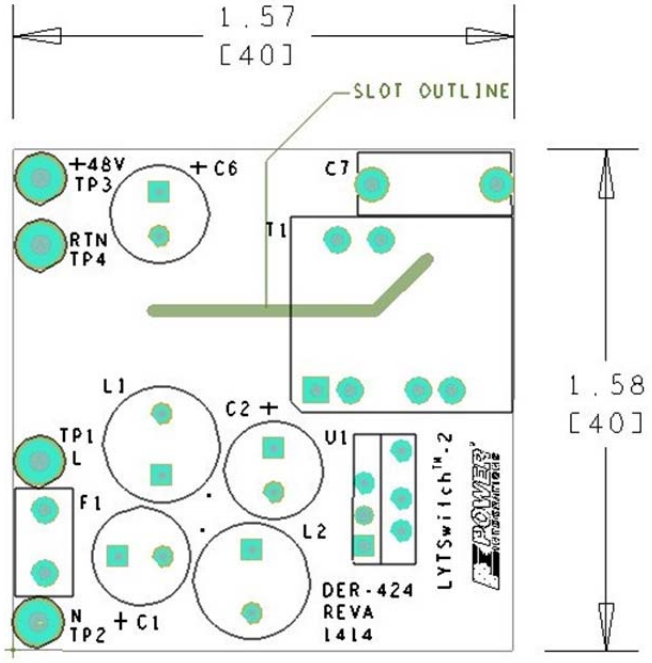

Figure 6 – Printed Circuit Board Layout, Top Side.

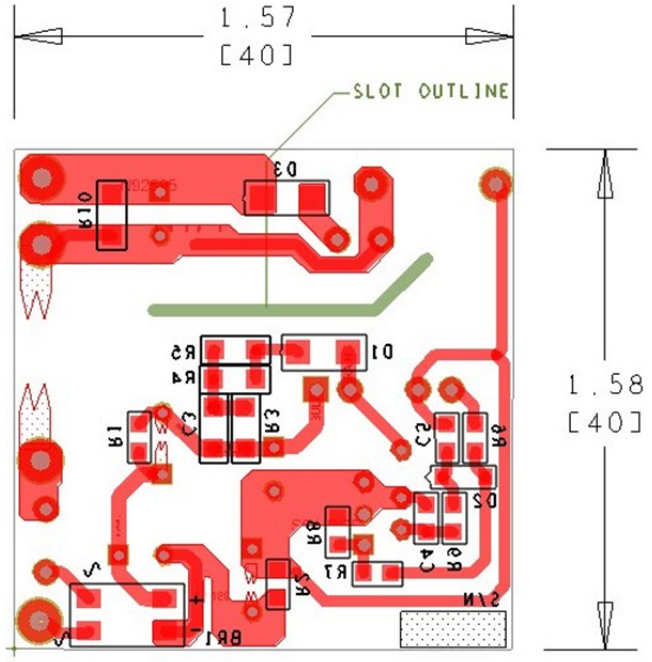

Figure 7 – Printed Circuit Board Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	2	C1 C2	12 μF, 400 V, Electrolytic, (8 x 16)	EKM126M2GF16RRS1P	Man-Yue Electronics
3	1	C3	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay
4	2	C4 C5	1 μF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
5	1	C6	100 μF, 63 V, Electrolytic, Low ESR, 270 mΩ, (8 x 15)	ELXZ630ELL101MH15D	Nippon Chemi-Con
6	1	C7	1 nF, 500 VAC, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
7	1	D1	1 kV, 1 A, Standard Recovery, SMA	S1ML	Taiwan Semi
8	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-123	BAV21W-7-F	Diodes, Inc.
9	1	D3	DIODE ULTRA FAST, GPP, 400 V, 1 A SMA	US1G-13-F	Diodes, Inc.
10	1	F1	2 A, 250 V, Slow, Long Time Lag,RST	RST 2	Belfuse
11	2	L1 L2	3.9 mH, 0.260 A, 10%	RL-5480HC-3-3900	Renco
12	2	R1 R2	3.9 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ392V	Panasonic
13	1	R3	220 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ224V	Panasonic
14	2	R4 R5	560 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ561V	Panasonic
15	1	R6	2 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R0V	Panasonic
16	1	R7	60.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6042V	Panasonic
17	1	R8	6.98 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6981V	Panasonic
18	1	R9	12 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ123V	Panasonic
19	1	R10	560 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ564V	Panasonic
20	1	T1	Bobbin, EE19, Vertical, 10 pins, 6pri, 4sec	TF-1939	Taiwan Shulin
21	2	TP1 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
22	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
23	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
24	1	U1	LYTSwitch-2, CV/CC, eSIP	LYT2004E	Power Integrations

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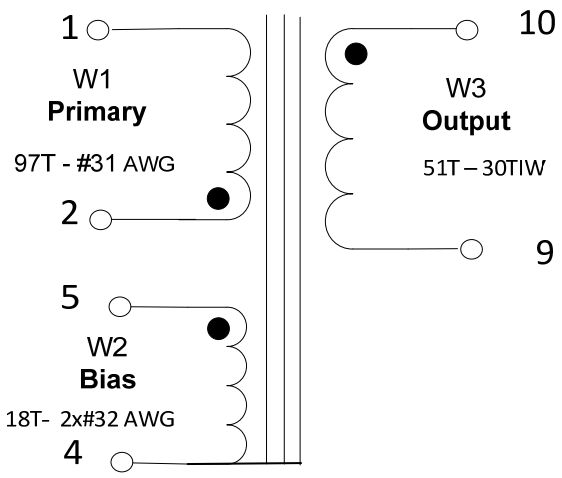
7 Transformer Specification

7.1 Electrical Diagram



(This is reversed winding for secondary transformer.)

Figure 8 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 4, 5 to 9, 10.	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1.1 mH ±3%
Resonant Frequency	Pins 1-2, all other windings open.	900 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with 9-10 shorted, measured at 100 kHz, 0.4 V_{RMS}.	50 μH max

7.3 Materials

Item	Description
[1]	Core: RM5/I-3F3 Ferrox Cube.
[2]	Bobbin: RM5-Vertical, 6 pins (3/3). AllStar Magnetics P/N: CPV-RM5-1S-6P-G.
[3]	Clip: AllStar Magnetics P/N: CLI/P-RM4/5/I.
[4]	Magnet wire: #33 AWG - Double coated.
[5]	Magnet wire: #29 AWG - Double coated.
[6]	Magnet wire: #34 AWG - Double coated.
[7]	Tape: 3M 1298 Polyester Film, 4.5 mm wide, 2.0 mils thick, or equivalent.
[8]	Varnish: Dolph BC-359 or equivalent.

7.4 Transformer Build Diagram

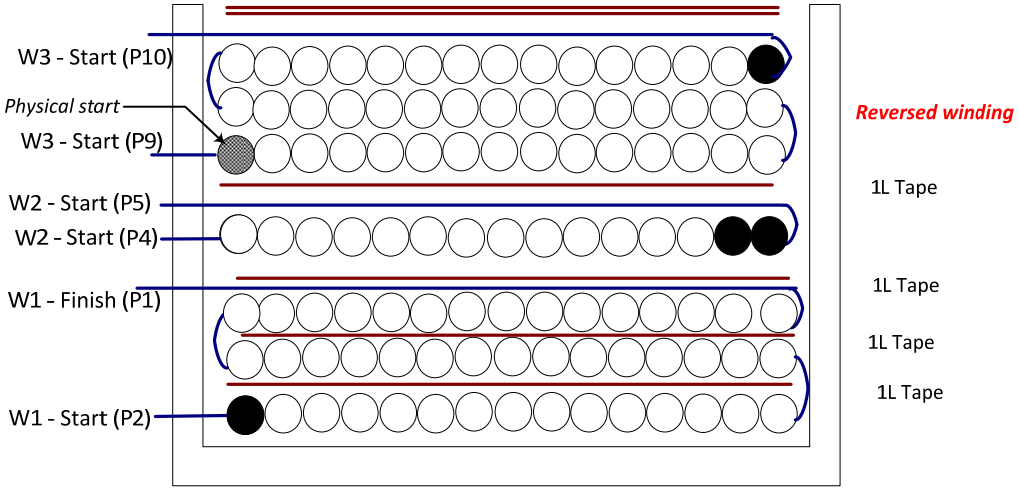


Figure 9 – Transformer Build Diagram.

7.5 Winding Construction

Winding Preparation	Place the bobbin on the mandrel with pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 2, wind 97 turns of wire item [4] in 3 layers, place 1 layer of tape item [3] between layers, and finish at pin 1.
Insulation	Place 1 layer of tape [3].
WD2 Bias	Take 2 wires item [5] leave floating (~1”), start from the right side of bobbin, then wind 18 bi-filar turns from right to left and finish at pin 4. Bring the floating ends to the left and finish at pin 5.
Insulation	Place 1 layer of tape [3].
WD3 Secondary	Because this winding is reversed winding so the bobbin is rotated with pin side is on the right side for easier winding. Start at pin 9, wind 51 turns of wire item [6] in 2 ¾ layers, and finish at pin 10.
Insulation	Place 2 layers of tape [3] to secure the windings.
Finish	Grind core halves to get 1.1 mH inductance. Use ~1.8” of wire item [7], connect to pin 4 and wrap along the bottom core halves then secure both of core halves with tape, see pictures below. Remove pins: 3, 6, 7, and 8. Vanish with item [8].

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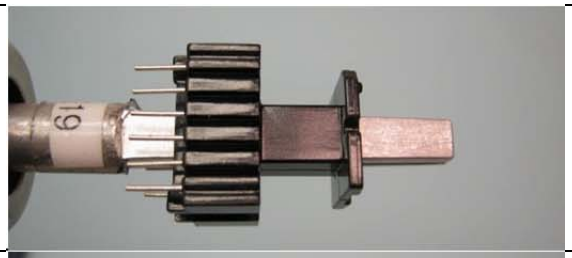
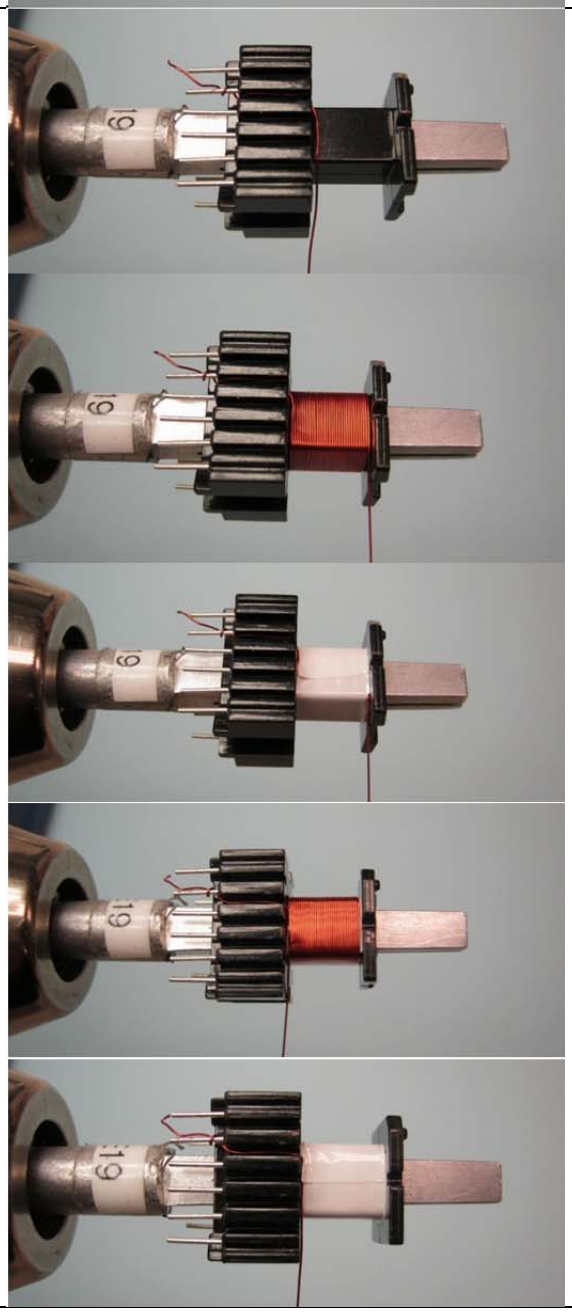
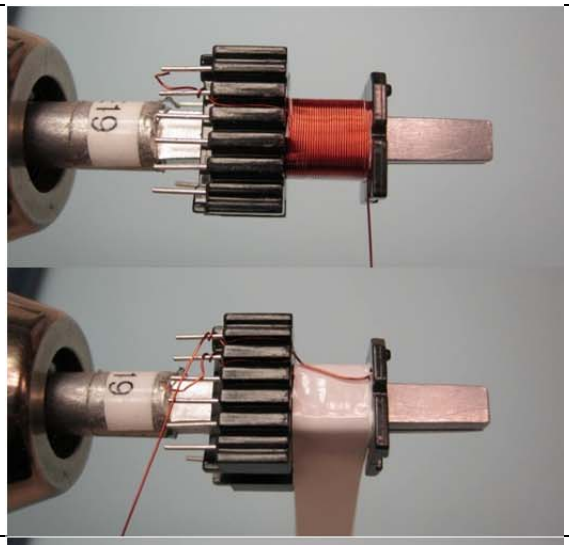
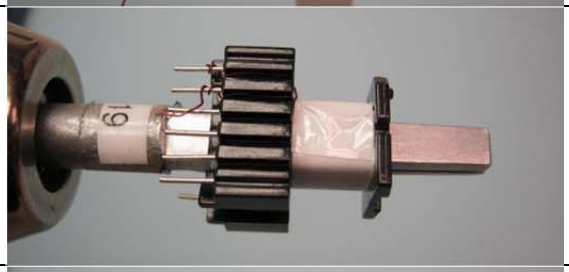
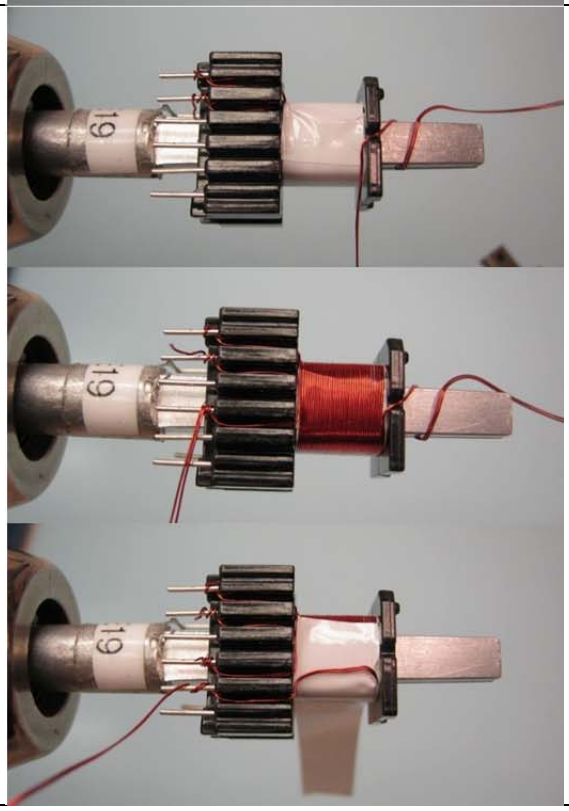
7.6 Winding Illustrations

Winding Preparation		Place the bobbin on the mandrel with pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**		Start at pin 2, wind 97 turns of wire item [4] in 3 layers, place 1 layer of tape item [3] between layers, and finish at pin 1.

		
Insulation		Place 1 layer of tape [3].
WD2 **Bias**		Take 2 wires item [5] leave floating (~1”), start from the right side of bobbin, then wind 18 bi-filar turns from right to left and finish at pin 4. Bring the floating ends to the left and finish at pin 5.

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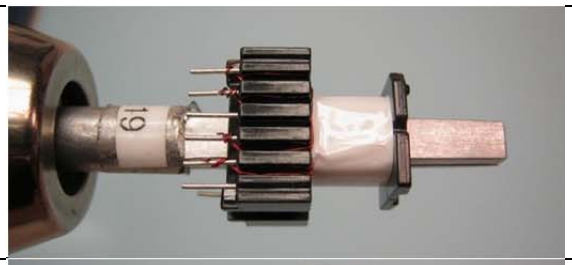
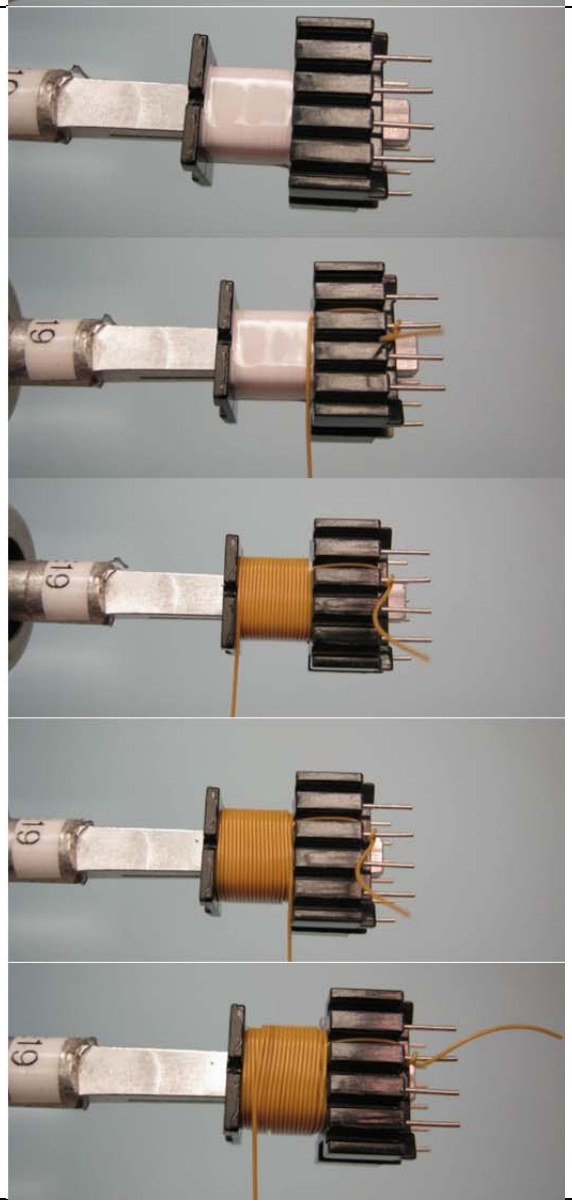
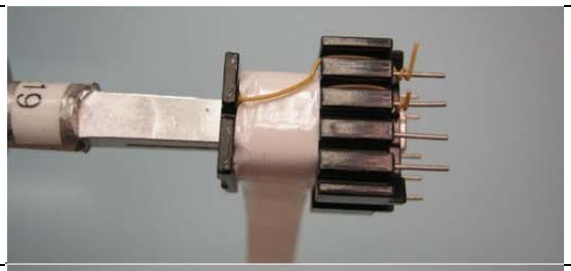
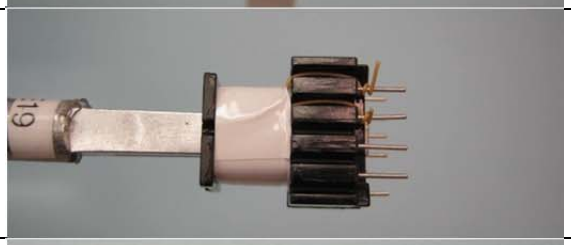
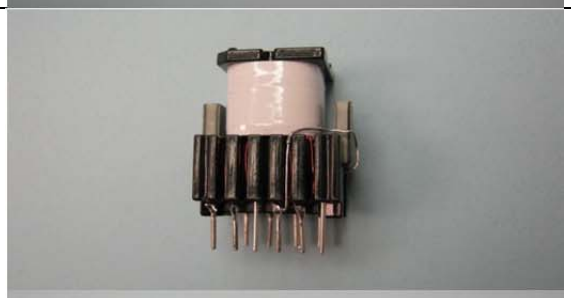
Insulation		Place 1 layer of tape [3].
WD3 **Secondary**		Because this winding is reversed winding so the bobbin is rotated with pin side is on the right side for easier winding. Start at pin 9, wind 51 turns of wire item [6] in 2 ¾ layers, and finish at pin 10.

		
Insulation		Place 2 layers of tape [3] to secure the windings.
Finish	   	Grind core halves to get 1.1mH inductance. Use ~1.8” of wire item [7], connect to pin 4 and wrap along the bottom core halves then secure both of core halves with tape, see pictures beside. Remove pins 3, 6, 7, and 8. Vanish with item [8].

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8 Transformer Design Spreadsheet

ACDC_LYTSwitch-2_050814; Rev.2.0; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LYTSwitch-2_050814_Rev2-0; Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			90	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
Application Type	**Ballast-CC**		Ballast-CC		Choose application type
VO	52.80		52.80	V	Output Voltage. This value is recommended to be 10% higher than the maximum LED Voltage
IO	0.18		0.18	A	Power Supply Output Current (corresponding to peak power)
Power			9.50	W	Continuous Output Power
n			0.85		Efficiency Estimate at output terminals
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	24.00		24.00	uF	Input Capacitance
ENTER LYTSwitch-2 VARIABLES					
Chosen Device	**Auto**		LYT2004K/E		Chosen LYTSwitch-2 device
ILIMITMIN			0.48	A	Minimum Current Limit
ILIMITTYP			0.52	A	Typical Current Limit
ILIMITMAX			0.56	A	Maximum Current Limit
FS	72.00		72.00	kHz	Typical Device Switching Frequency at maximum power
VOR			101.37	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			1.31		KP assuming minimum LP, VMIN, and average switching frequency. Ensure that this value is above 1.30 for optimal operation
FEEDBACK WINDING PARAMETERS					
NFB	18.00		18.00		Feedback winding turns
VFLY			18.81	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			18.26	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
BIAS	**Ext. bias**		Ext. bias		Select between self bias or external bias to supply the IC.
VB	0.00		0.00	V	Bias Winding Voltage. Ensure that VB > VFLY. Bias winding is assumed to be AC-STACKED on top of Feedback winding
NB	.	*Info*	N/A		Bias winding is disabled. Verify on the bench that current value of VFLY is enough to supply the IC under all operating conditions
REXT			3.20	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON	4.80		4.80	us	Desired output diode conduction time
DCON_FINAL			4.80	us	Final output conduction diode, assuming integer values for NP and NS
TON			4.95	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		*Info*	60.99	k-ohm	Upper resistor in Feedback resistor divider. Once the initial prototype is running, it may be

					necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER			7.01	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	**EE19**		EE19		Enter Transformer Core.
Custom_Core					Enter Core name if selection on drop down menu is "Custom"
Bobbin			BE-19-116-CP		Bobbin part number
AE			23.00	mm^2	Core Effective Cross Sectional Area
LE			39.40	mm	Core Effective Path Length
AL			1250.00	nH/turn^2	Ungapped Core Effective Inductance
BW			9.10	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3.00		Number of Primary Layers
NS			51.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			98.38	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.44		Maximum duty cycle measured at VMIN
IAVG			0.13	A	Input Average current
IP			0.48	A	Peak primary current
IR			0.48	A	Primary ripple current
IRMS			0.22	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1018.74	uH	Minimum Primary Inductance
LPTYP			1095.42	uH	Typical Primary inductance
LP_TOLERANCE			7.00	%	Tolerance in primary inductance
NP			97.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			116.42	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2560.00		2560.00	Gauss	Target Flux Density
BM			2553.19	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2600 is recommended
BP			2952.56	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3100 is recommended
BAC			1276.59	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			170.40		Relative Permeability of Ungapped Core
LG			0.24	mm	Gap Length (LG > 0.1 mm)
BWE			27.30	mm	Effective Bobbin Width
OD			0.28	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.23	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			80.63	Cmils	Bare conductor effective area in circular mils
CMA			374.69	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			0.91	A	Peak Secondary Current
ISRMS			0.40	A	Secondary RMS Current

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IRIPPLE			0.36	A	Output Capacitor RMS Ripple Current
CMS			80.64	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			31.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			607.65	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS			249.84	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL			60.99	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL			7.01	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)			52.80	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)			0.18	Amps	Measured Output current from first prototype
RUPPER_FINE			60.99	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 60.4 k-ohms
RLOWER_FINE			7.01	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 6.98 k-ohms

9 Performance Data

All measurements were taken with the board at open frame, 25 ºC ambient.

9.1 Efficiency

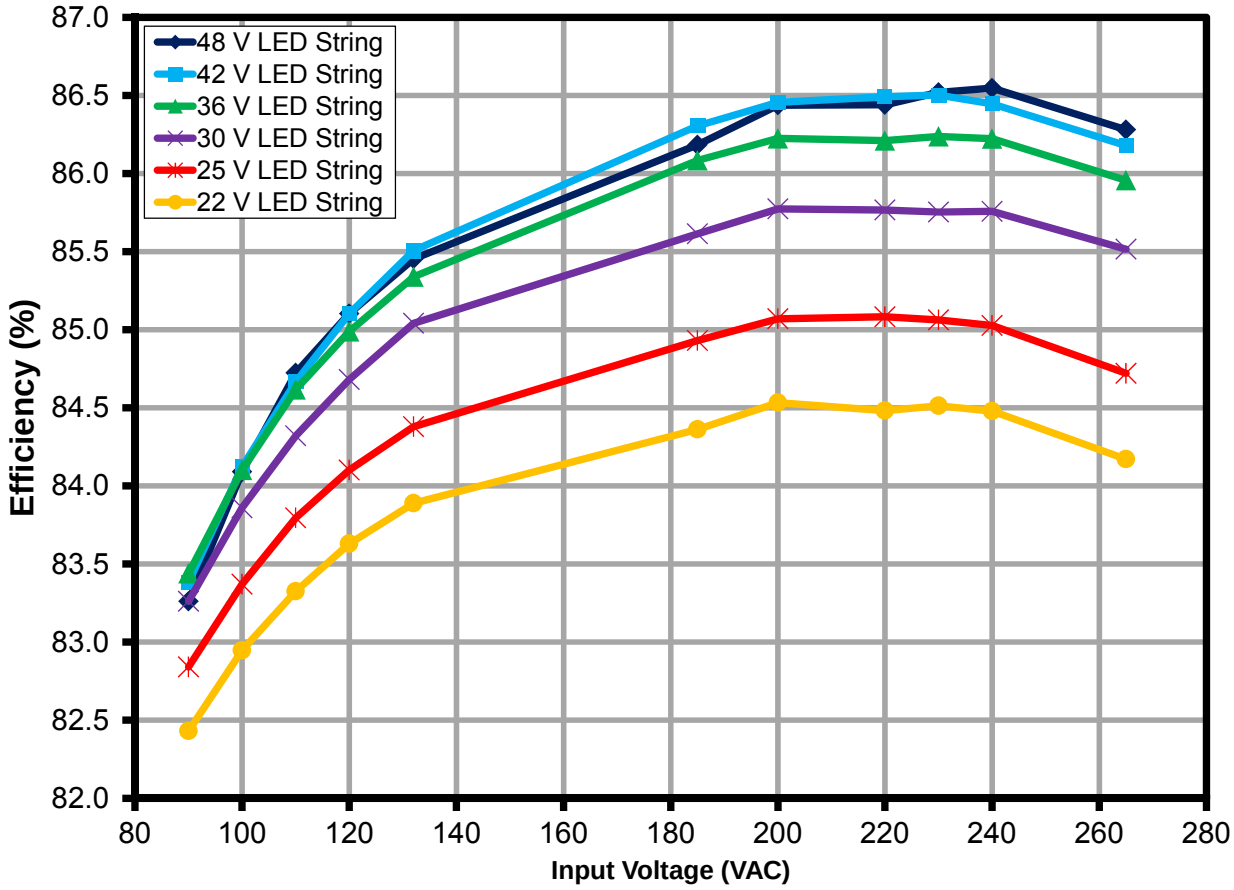

Figure 10 – Efficiency vs. Line and Load, 180 mA.

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9.2 Average Efficiency

Load Setting		Input Measurement				Load Measurement			
Load (%)	Load (A)	V (V_{RMS})	I (A_{RMS})	P (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	0.180	114.94	0.18	11.14	0.55	53.57	0.18	9.49	85.21
75	0.135	114.94	0.14	8.45	0.53	53.75	0.13	7.20	85.20
50	0.090	114.95	0.09	5.63	0.51	53.06	0.09	4.82	85.54
25	0.045	114.95	0.05	2.84	0.46	52.68	0.05	2.40	84.48
							Average Efficiency		**85.11**
Load Setting		**Input Measurement**				**Load Measurement**			
Load (%)	**Load (A)**	**V_{IN} (V_{RMS})**	**I_{IN} (A_{RMS})**	**P_{IN} (W)**	**PF**	**V_{OUT} (V_{DC})**	**I_{OUT} (A_{DC})**	**P_{OUT} (W)**	**Efficiency (%)**
100	0.180	229.92	0.10	10.91	0.46	53.55	0.18	9.51	87.15
75	0.135	229.92	0.08	8.29	0.44	53.70	0.13	7.21	87.00
50	0.090	229.92	0.06	5.56	0.41	53.02	0.09	4.83	86.78
25	0.045	229.92	0.03	2.79	0.37	52.59	0.05	2.36	84.38
							Average Efficiency		**86.33**

9.3 Line and Load Regulation

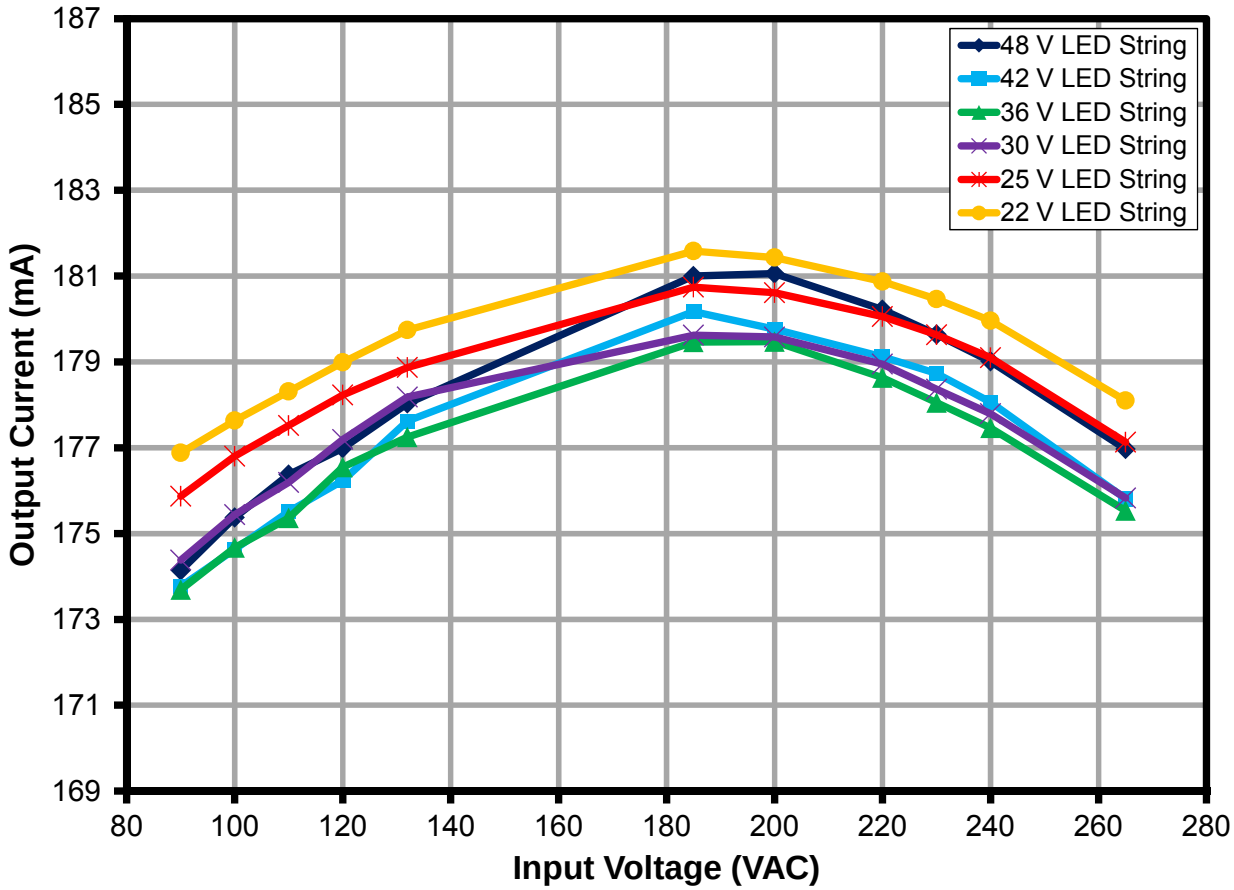

Figure 11 – Regulation vs. Line and Load.

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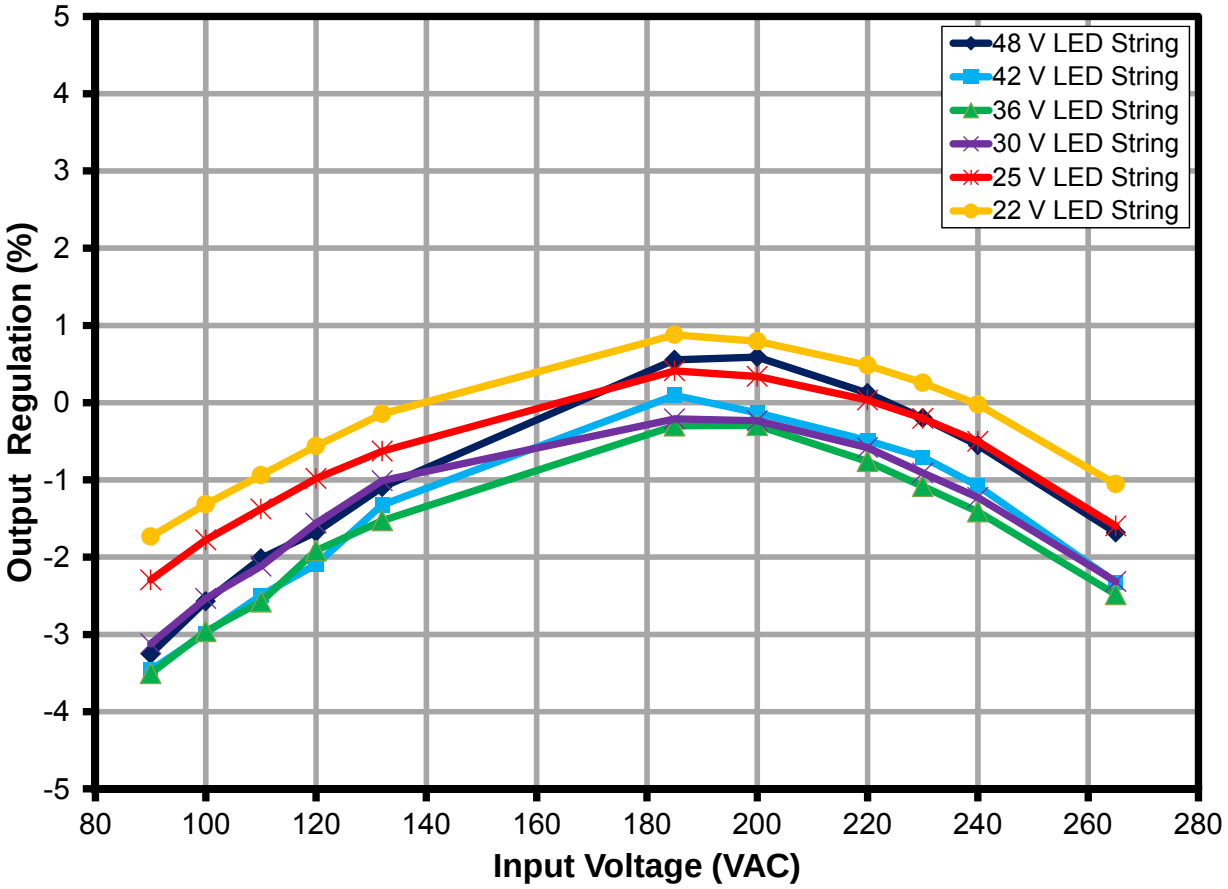

Figure 12 – % Regulation vs. Line and Load.

9.4 CV/CC Characteristics

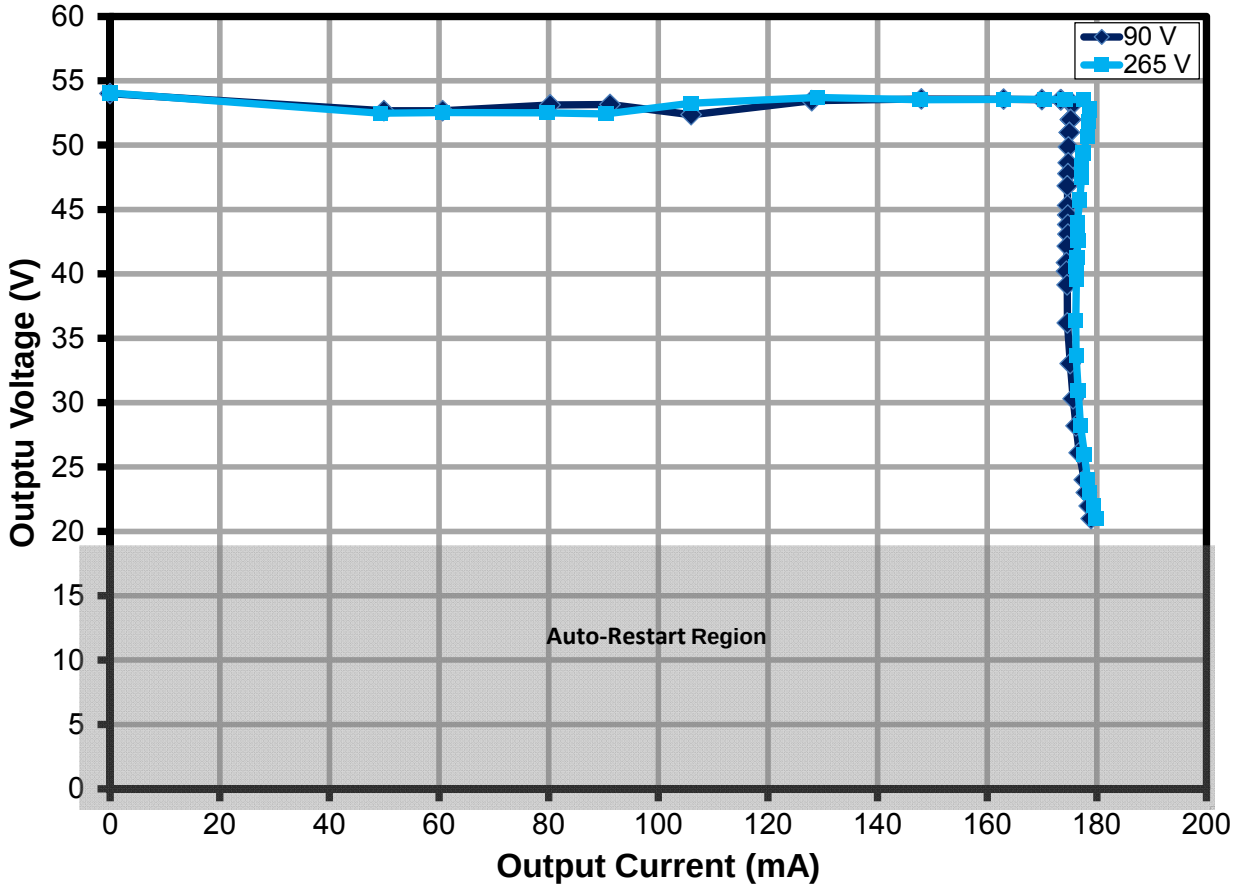

Figure 13 – CV/CC Characteristics.

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9.5 No-Load Input Power

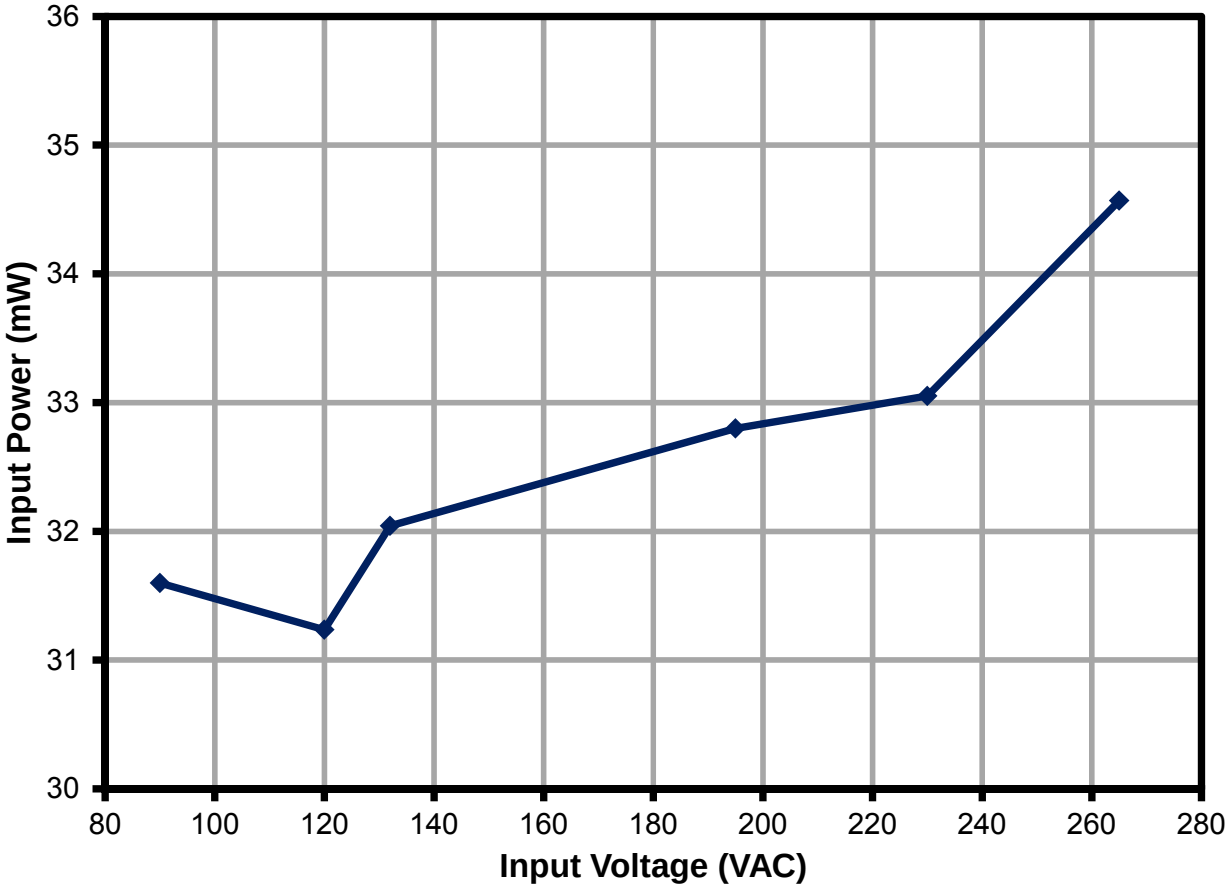

Figure 14 – No-Load Input Power.

10 Thermal Performance

Images captured after running for >30 minutes at room temperature (25 °C), open frame for the conditions specified.

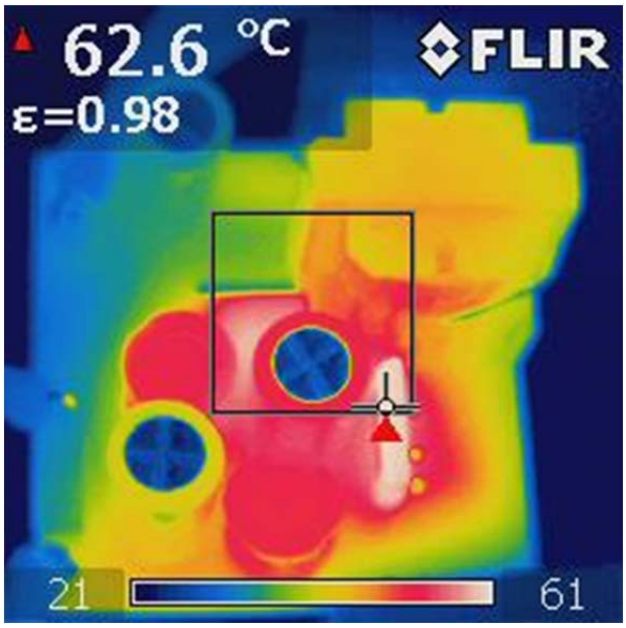

Figure 15 – 90 VAC, Thermal, Top Side**.**
LYT2004E: 62.6 ºC.

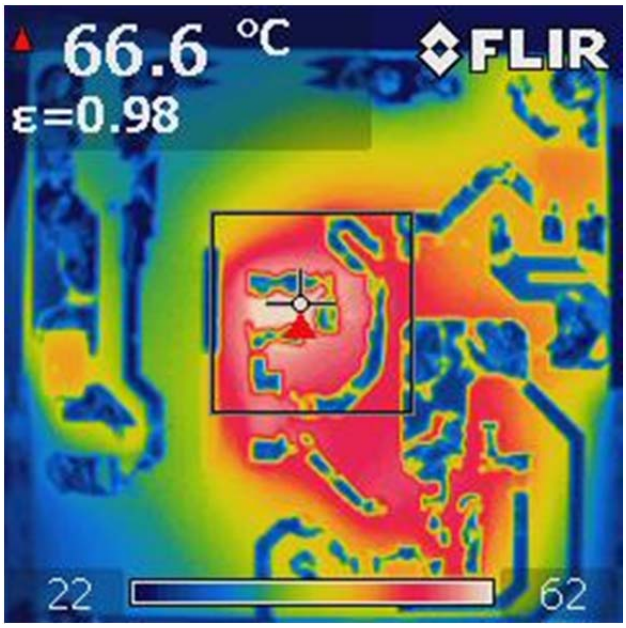

Figure 16 – 90 VAC, Thermal, Bottom Side**.**
R4 and R5: 66.6 ºC.

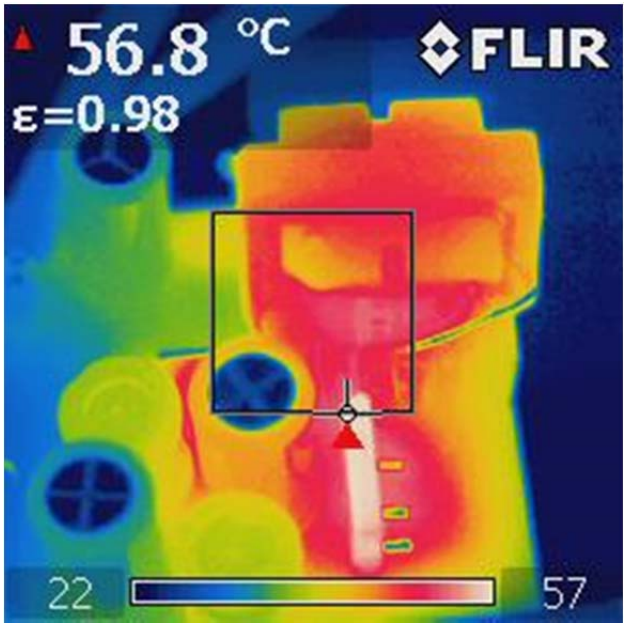

Figure 17 – 265 VAC, Thermal, Top Side.
LYT2004E: 56.8 ºC.

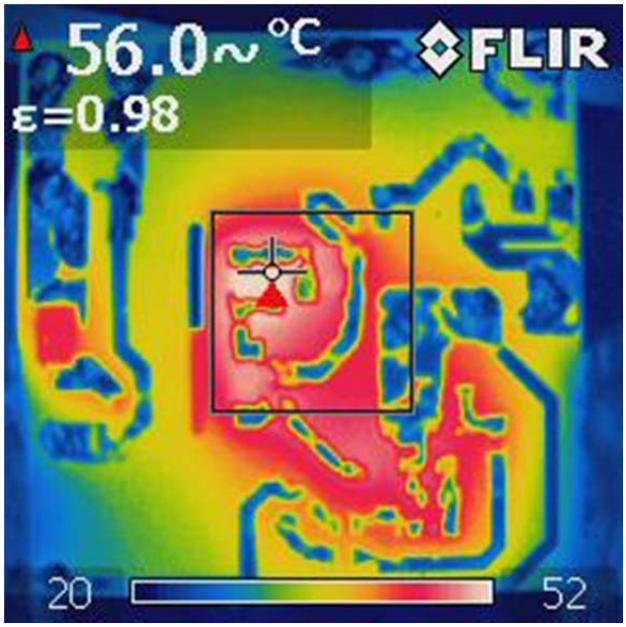

Figure 18 – 265 VAC, Thermal, Bottom Side.
R4 and R5: 56.0 ºC.

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11 Waveforms

11.1 Input Voltage and Input Current Waveforms

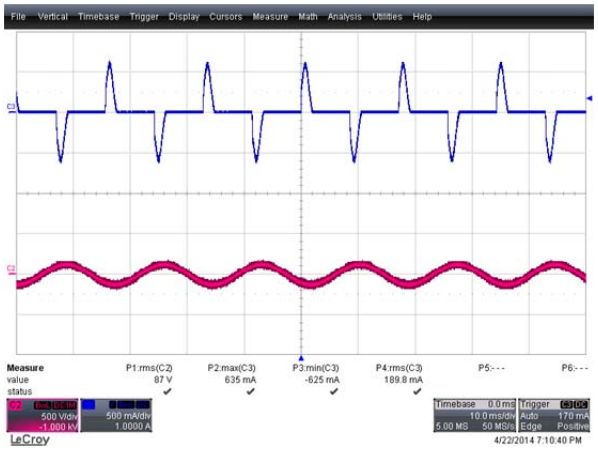

Figure 19 – 90 VAC, Full Load.
Upper: I_{IN}, 500 mA / div.
Lower: V_{IN}, 500 V, 10 ms / div.

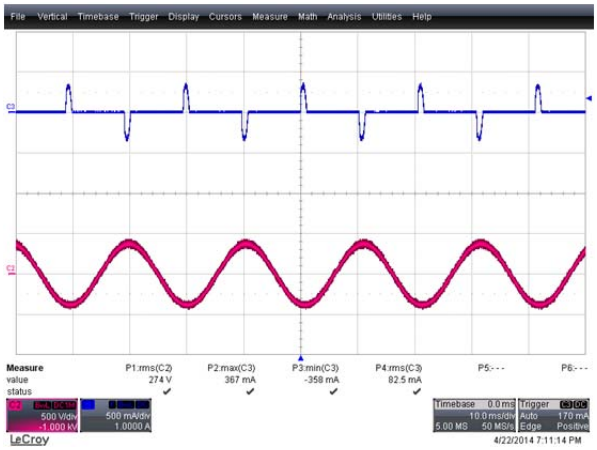

Figure 20 – 265 VAC, Full Load.
Upper: I_{IN}, 500 mA / div.
Lower: V_{IN}, 500 V, 10 ms / div.

11.2 Output Current and Output Voltage at Normal Operation

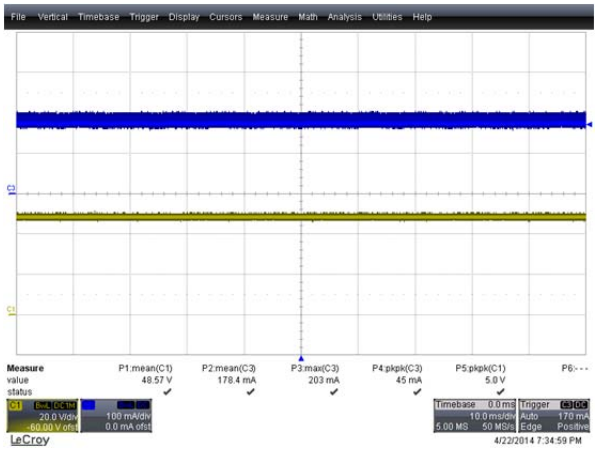

Figure 21 – 195 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

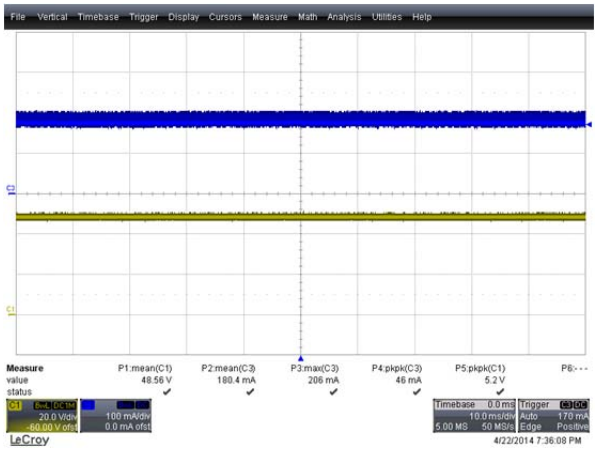

Figure 22 – 265 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{OUT}, 20 V, 10 ms / div.

11.3 Output Voltage Ripple (CV Mode)

The voltage ripple is measured in CV mode (VO ~ 53V) using a x1 probe with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic.

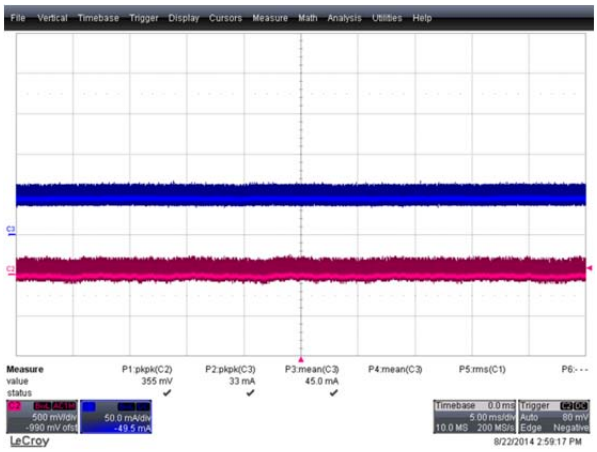

Figure 23 – 90 VAC, 60 Hz, Output Ripple, 25% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

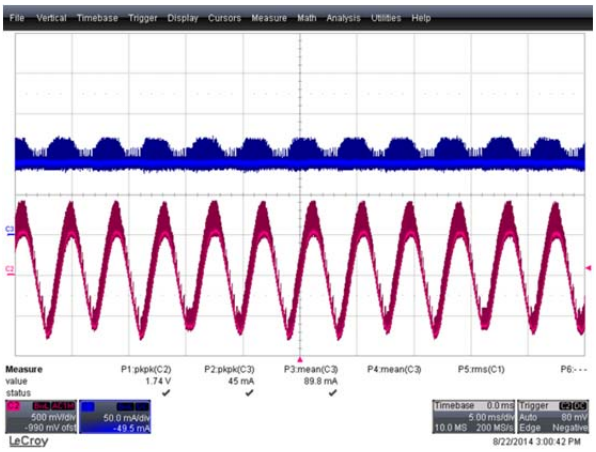

Figure 24 – 90 VAC, 60 Hz, Output Ripple, 50% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

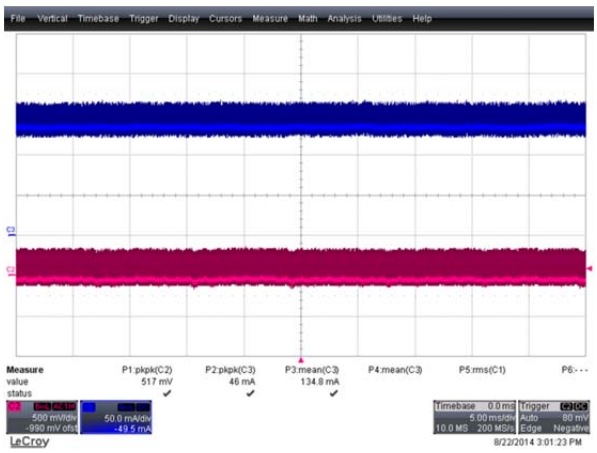

Figure 25 – 90 VAC, 60 Hz, Output Ripple, 75% Load,
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500mV, 5 ms / div.

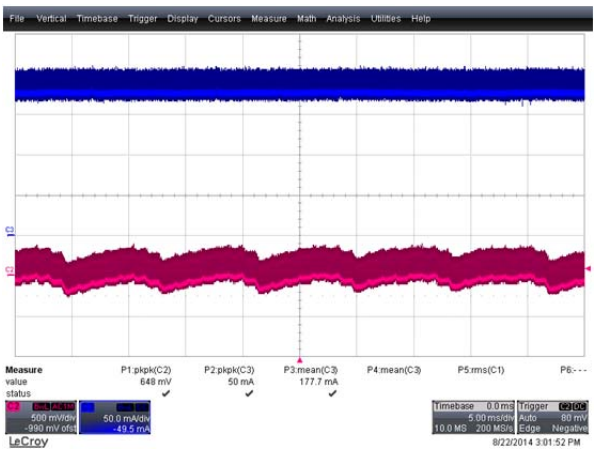

Figure 26 – 90 VAC, 60 Hz, Output Ripple, 100% Load,
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500mV, 5 ms / div.

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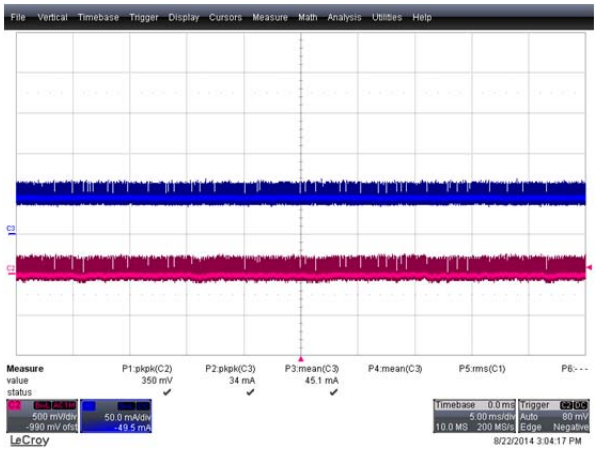

Figure 27 – 265 VAC, 50 Hz, Output Ripple, 25% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

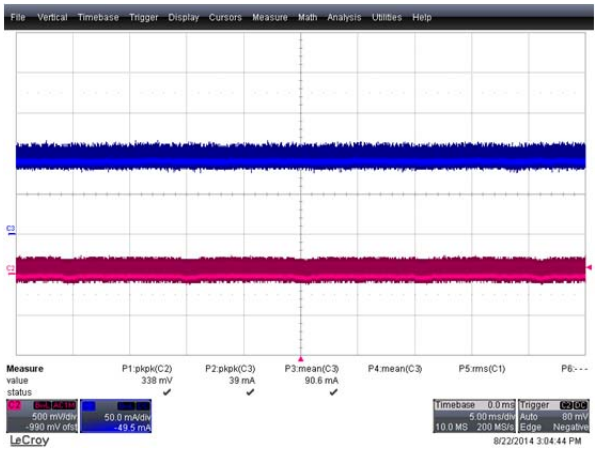

Figure 28 – 265 VAC, 50 Hz, Output Ripple, 50% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

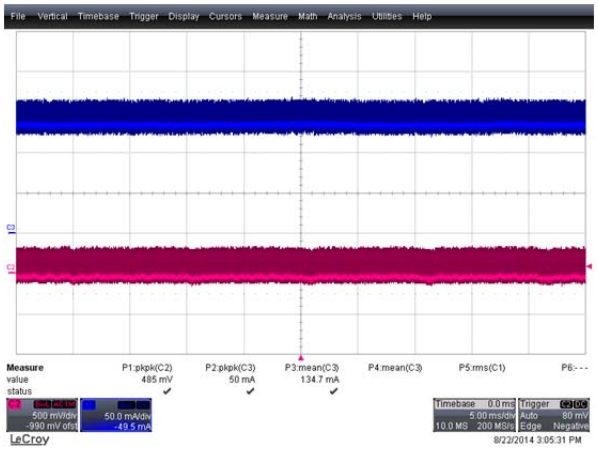

Figure 29 – 265 VAC, 50 Hz, Output Ripple, 75% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

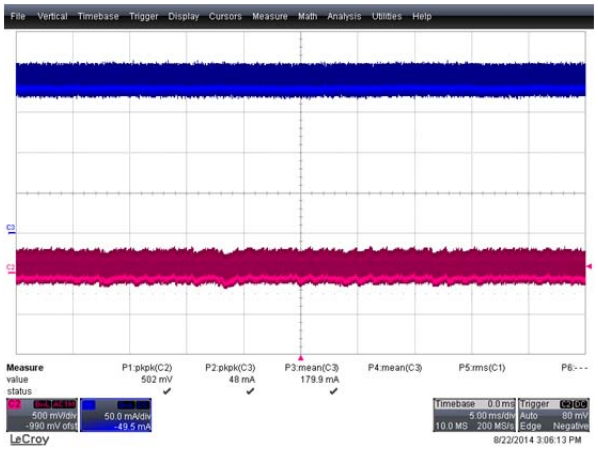

Figure 30 – 265 VAC, 50 Hz, Output Ripple, 100% Load.
Upper: I_{OUT}, 50 mA / div.
Lower: V_{RIPPLE}, 500 mV, 5 ms / div.

11.4 Output Voltage/ Current Rise and Fall

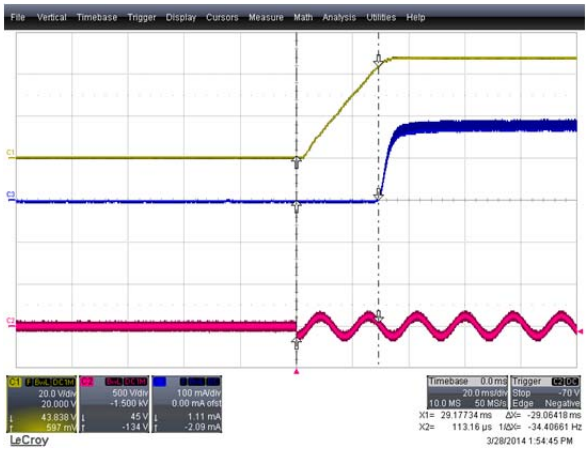

Figure 31 – 90 VAC, 60 Hz, Output Rise.
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{OUT}, 100 mA, 20 ms / div.
Start-up Time: 29 ms.

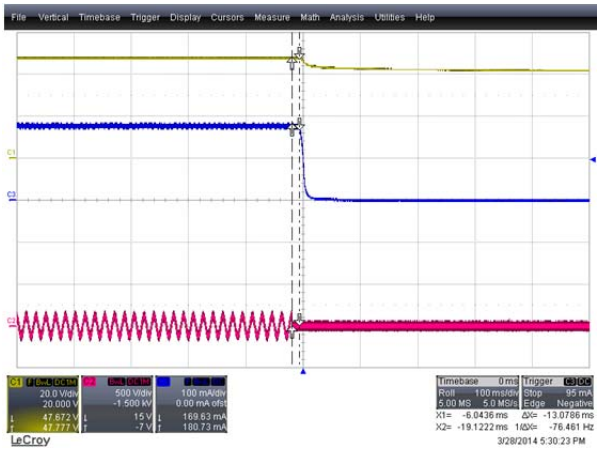

Figure 32 – 90 VAC, 60 Hz, Output Fall.
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{OUT}, 100 mA, 20 ms / div.
Hold-up Time: 13 ms.

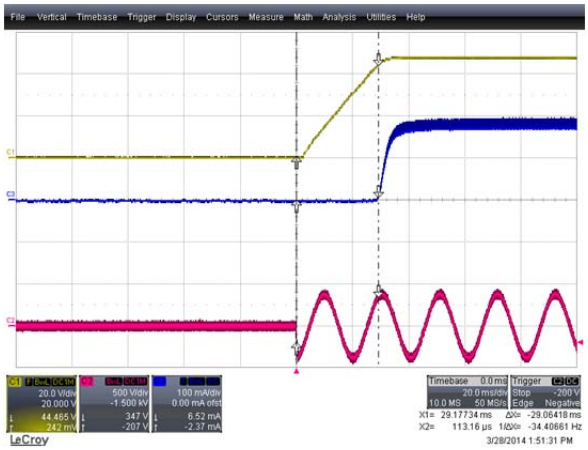

Figure 33 – 265 VAC, 50 Hz, Output Rise.
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{OUT}, 100 mA, 20 ms / div.
Start-up Time: 29 ms.

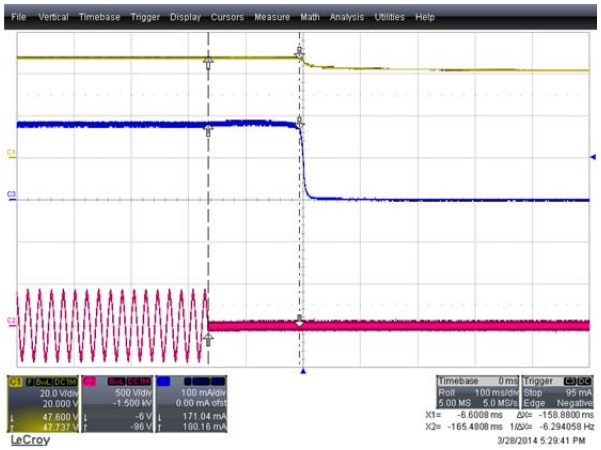

Figure 34 – 265 VAC, 50 Hz, Output Fall.
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{OUT}, 100 mA, 20 ms /div.
Hold-up Time: 159 ms.

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11.5 Drain Voltage and Current at Normal Operation

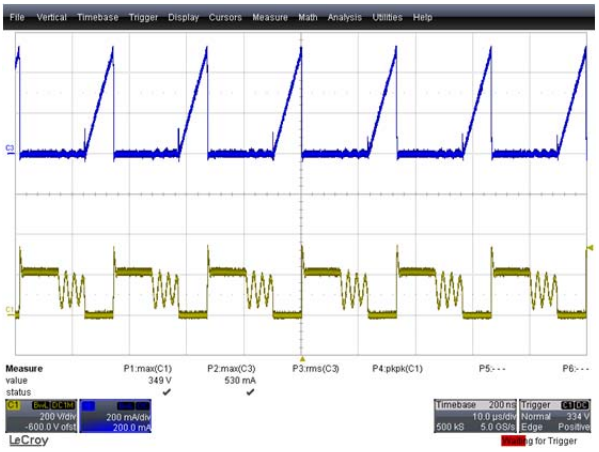

Figure 35 – 90 VAC, 60 Hz.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 10 μs / div.

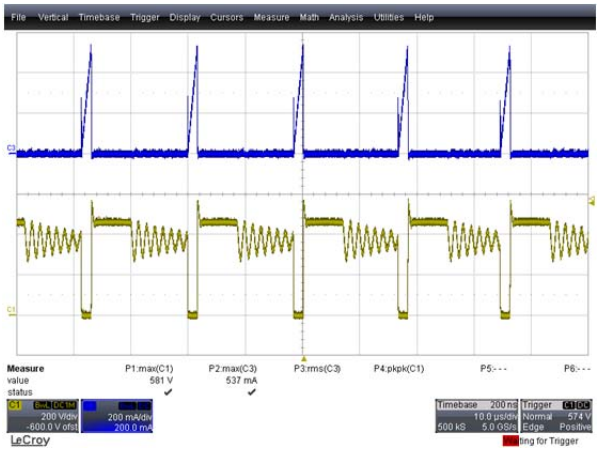

Figure 36 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 10 μs / div.

11.6 Start-up Drain Voltage and Current

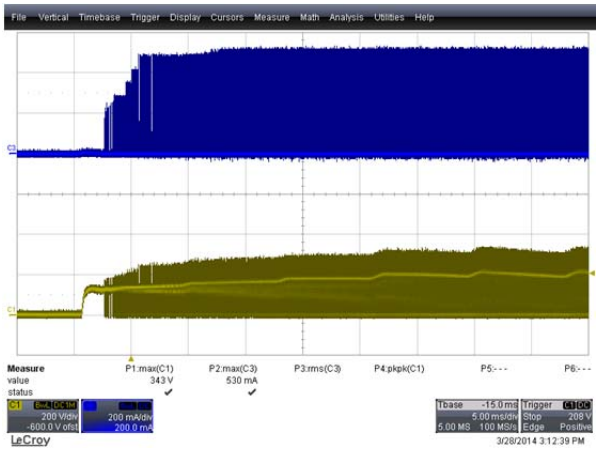

Figure 37 – 90 VAC, 60 Hz Start-up.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 5 ms / div.

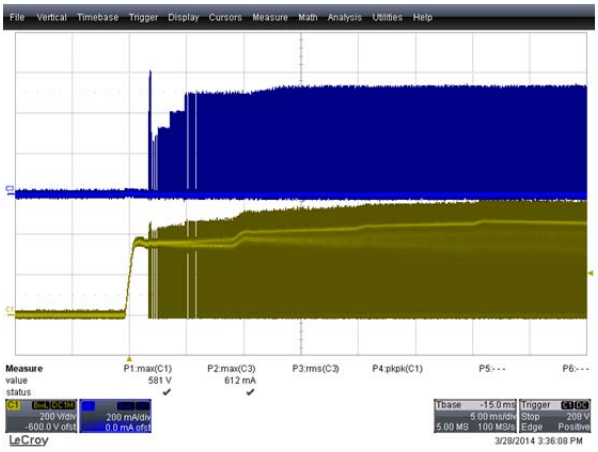

Figure 38 – 265 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 5 ms / div.

11.7 Drain Current and Drain Voltage during Output Short Condition

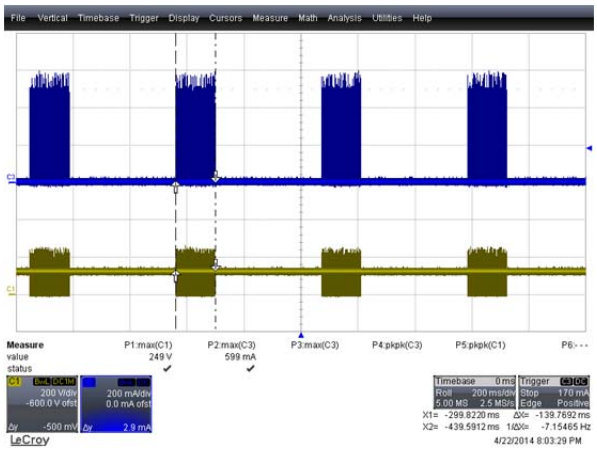

Figure 39 – 90 VAC, 60 Hz Output Short Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 200 ms / div.

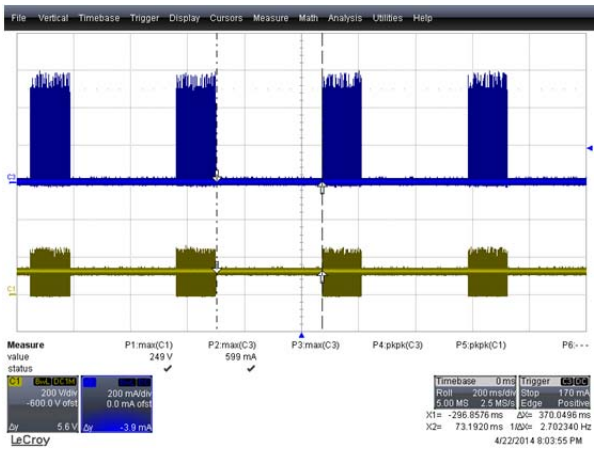

Figure 40 – 90 VAC, 60 Hz Output Short Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: V_{DRAIN}, 200 V, 200 ms / div.

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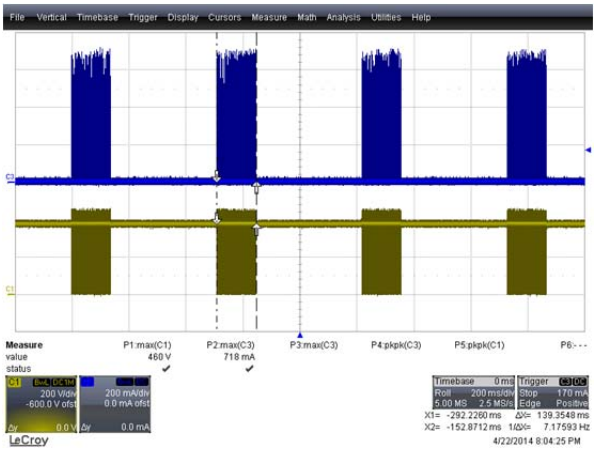

Figure 41 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

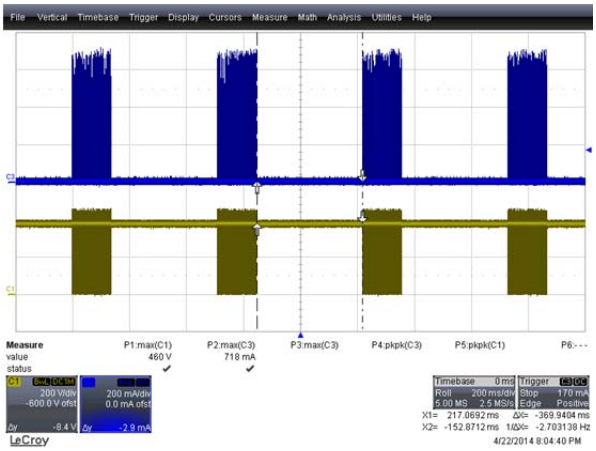

Figure 42 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

11.8 Drain Current and Drain Voltage During Open-Loop Condition (R7 is Open)

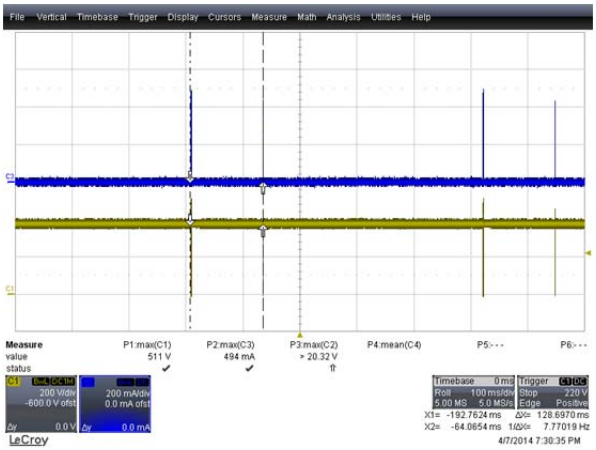

Figure 43 – 265 VAC, 50 Hz Open-loop Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 200 V, 100 ms / div.

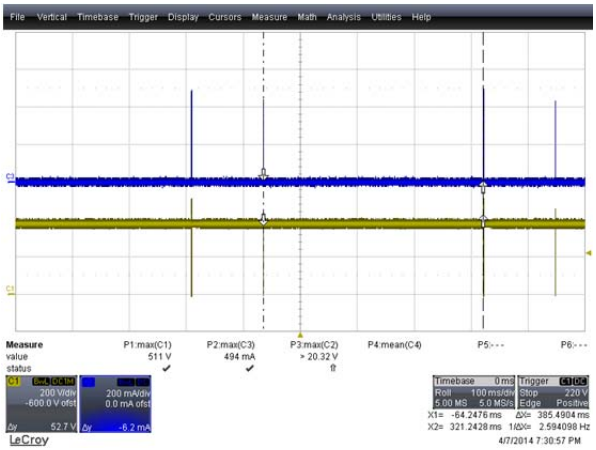

Figure 44 – 265 VAC, 50 Hz Open-loop Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 200 V, 100 ms / div.
OFF-time: 385 ms.

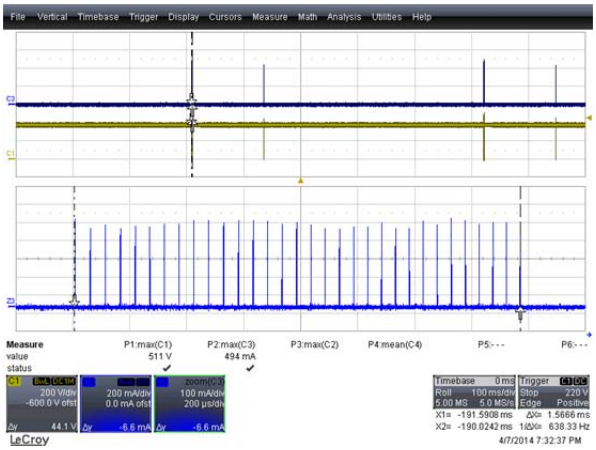

Figure 45 – 265 VAC, 50 Hz Open-loop Condition.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 200 V, 100 ms / div.
Z3: $I_{DRAIN(ZOOM),}$ 200 mA / div, 200 μs / div.
ON-time: 1.6 ms (32 pulses).

11.9 Output Diode Current and Voltage Waveforms

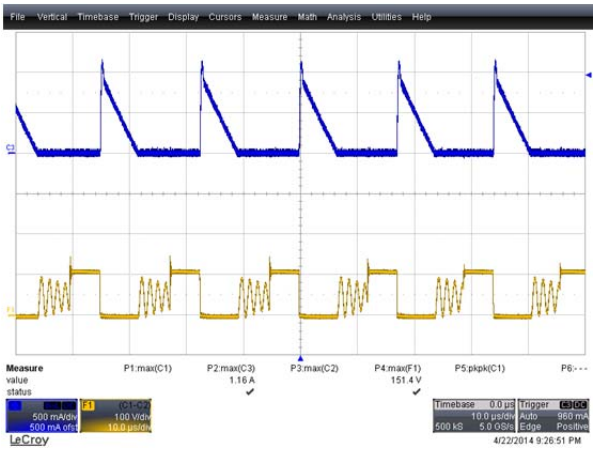

Figure 46 – 90 VAC, 60 Hz.
Upper: I_{D3}, 500 mA / div.
Lower: V_{D3}, 100 V, 10 μs / div.

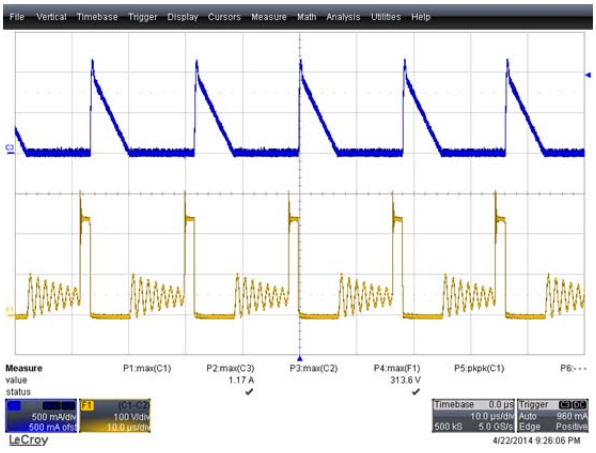

Figure 47 – 265 VAC, 50 Hz.
Upper: I_{D3}, 500 mA / div.
Lower: V_{D3}, 100 V, 10 μs / div.

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11.10 Output Diode Current and Voltage Short-Circuit Waveforms

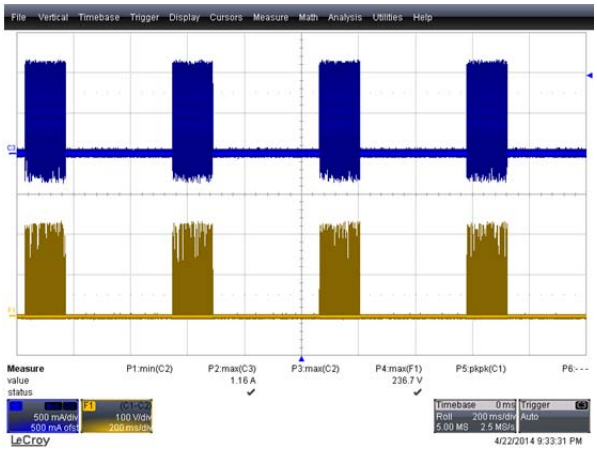

Figure 48 – 90 VAC, 60 Hz.
Upper: I_{D3}, 500 mA / div.
Lower: V_{D3}, 100 V, 200 ms / div.

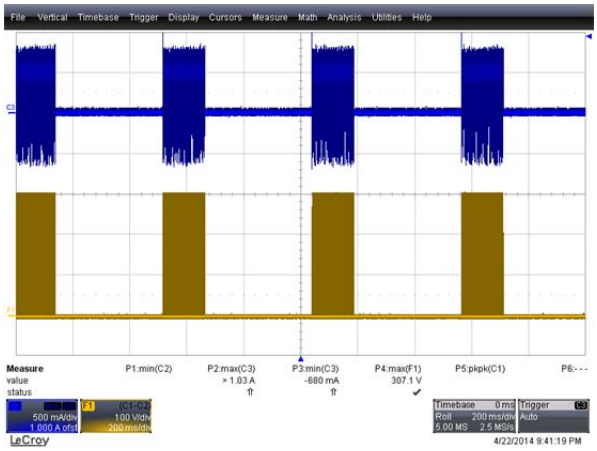

Figure 49 – 265 VAC, 50 Hz.
Upper: I_{D3}, 500 mA / div.
Lower: V_{D3}, 100 V, 200 ms / div.

11.11 Brown-out / Brown-in

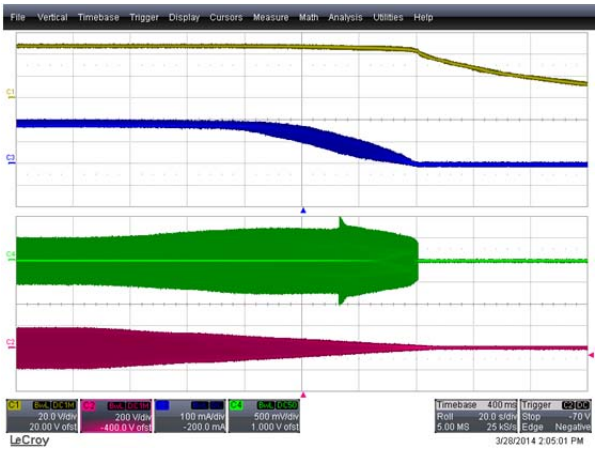

Figure 50 – 48 V Output, Brown-out Condition (1 V / s Decay Rate).
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 200 V / div.
CH3: I_{OUT}, 100 mA / div.
CH4: I_{IN}, 500 mA, 20 s / div.

Figure 51 – 48 V Output, Brown-in Condition (1 V / s Ramp Rate).
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 200 V / div.
CH3: I_{OUT}, 100 mA / div.
CH4: I_{IN}, 500 mA, 20 s / div.

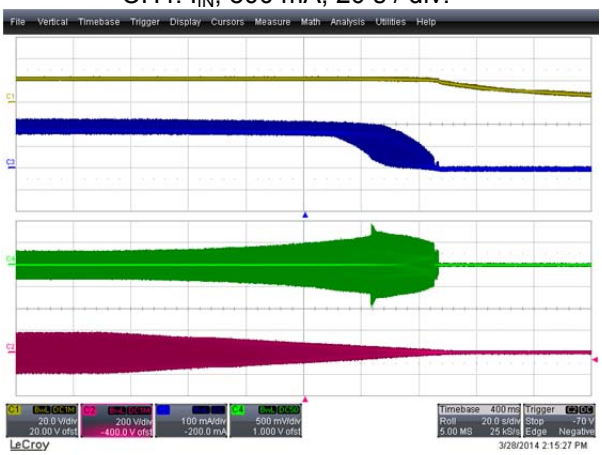

Figure 52 – 22 V Output, Brown-out Condition (1 V / s Decay Rate).
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 200 V / div.
CH3: I_{OUT}, 100 mA / div.
CH4: I_{IN}, 500 mA, 20 s / div.

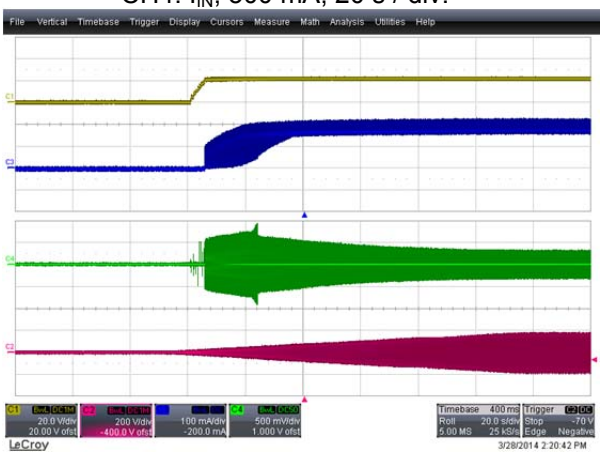

Figure 53 – 22 V Output, Brown-in Condition (1 V / s Ramp Rate).
CH1: V_{OUT}, 20 V / div.
CH2: V_{IN}, 200 V / div.
CH3: I_{OUT}, 100 mA / div.
CH4: I_{IN}, 500 mA, 20 s / div.

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11.12 Line Transient

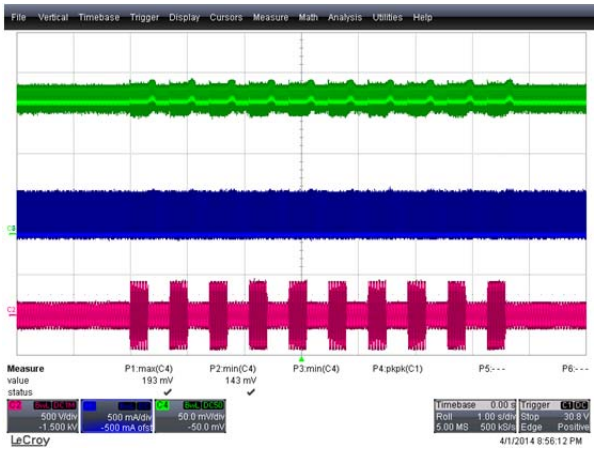

Figure 54 – 90 VAC to 265 VAC Line Transient.
CH2: V_{IN}, 500 V / div.
CH3: I_{DRAIN}, 500 mA / div.
CH4: I_{OUT}, 50 mA / div., 1 s / div.

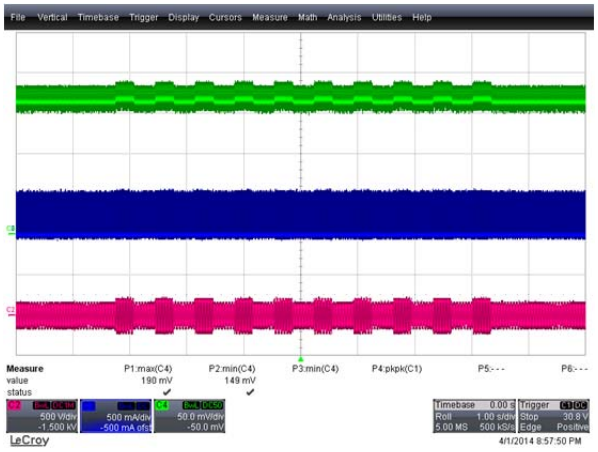

Figure 55 – 90 VAC to 132 VAC Line Transient.
CH2: V_{IN}, 500 V / div.
CH3: I_{DRAIN}, 500 mA / div.
CH4: I_{OUT}, 50 mA / div., 1 s / div.

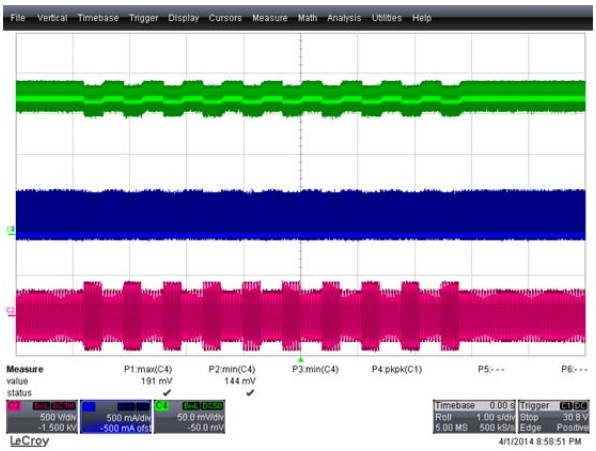

Figure 56 – 195 VAC to 265 VAC Line Transient.
CH2: V_{IN}, 500 V / div.
CH3: I_{DRAIN}, 500 mA / div.
CH4: I_{OUT}, 50 mA / div., 1 s / div.

11.13 300 ms ON, 300 ms OFF AC Cycling

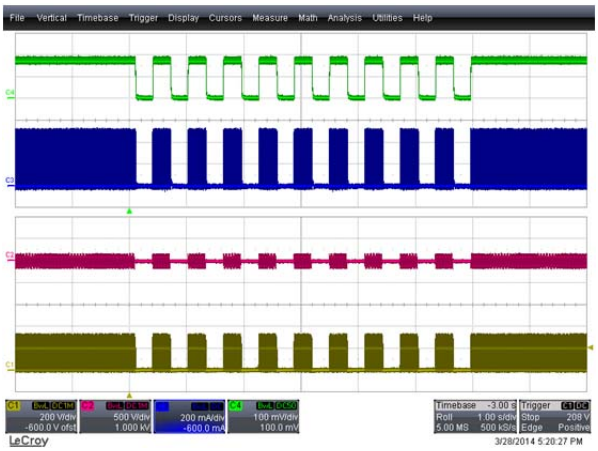

Figure 57 – 90 VAC, 300 ms ON-OFF Cycling.
CH1: V_{DRAIN}, 200 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{DRAIN}, 200 mA / div.
CH4: I_{OUT}, 100 mA / div., 1 s / div.

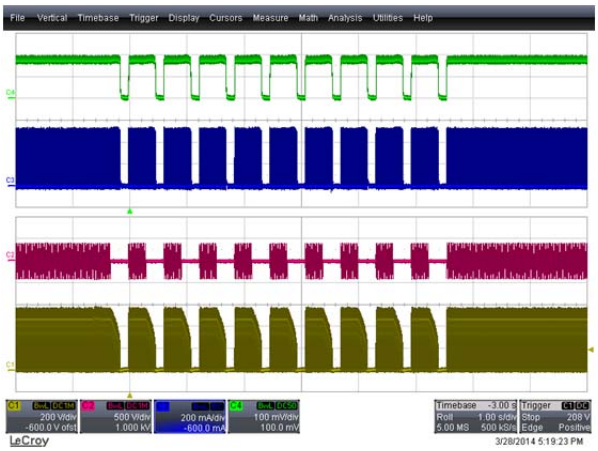

Figure 58 – 265 VAC, 300 ms ON-OFF Cycling.
CH1: V_{DRAIN}, 200 V / div.
CH2: V_{IN}, 500 V / div.
CH3: I_{DRAIN}, 200 mA / div.
CH4: I_{OUT}, 100 mA / div., 1 s / div.

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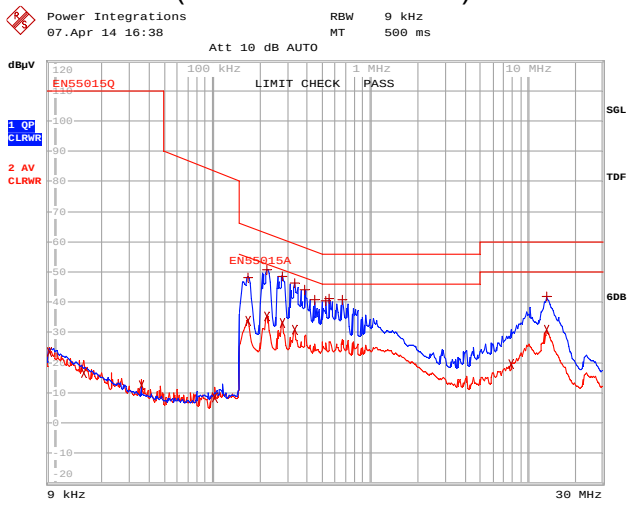
12 Conducted EMI

The unit was tested using LED load (~48 V V_{OUT}) with input voltage of 230 VAC, 60 Hz at room temperature.

Figure 59 – Conducted EMI Set-up.

Conducted EMI, With Ground Plane (Connected to Earth)

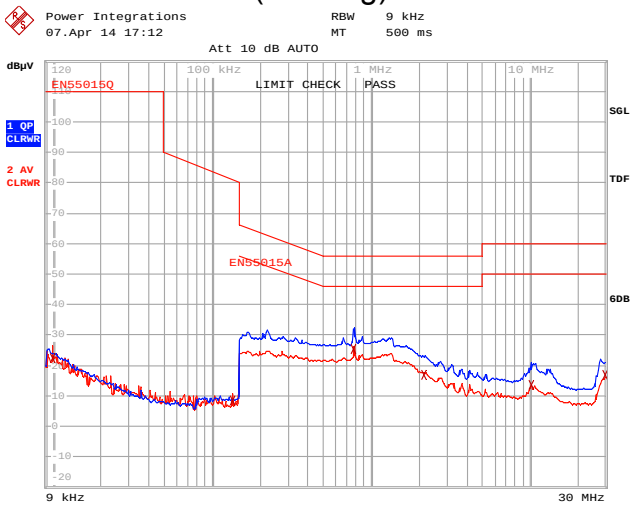


EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.1309 kHz	23.42	N gnd	
2	Average	15.2501922961 kHz	16.65	L1 gnd	
2	Average	35.5297450746 kHz	12.60	L1 gnd	
2	Average	104.063986756 kHz	8.59	L1 gnd	
1	Quasi Peak	167.350252 kHz	48.24	L1 gnd	-16.84
2	Average	167.350252 kHz	33.80	L1 gnd	-21.28
1	Quasi Peak	221.118376275 kHz	50.71	N gnd	-12.06
2	Average	221.118376275 kHz	35.27	N gnd	-17.50
1	Quasi Peak	277.981845331 kHz	48.55	L1 gnd	-12.31
2	Average	277.981845331 kHz	33.23	N gnd	-17.64
1	Quasi Peak	332.507282579 kHz	46.26	L1 gnd	-13.12
2	Average	332.507282579 kHz	30.96	N gnd	-18.42
1	Quasi Peak	386.030632509 kHz	44.13	L1 gnd	-14.01
1	Quasi Peak	443.732257589 kHz	40.77	L1 gnd	-16.22
1	Quasi Peak	520.310969312 kHz	40.48	L1 gnd	-15.51
1	Quasi Peak	552.320578504 kHz	41.36	L1 gnd	-14.63
1	Quasi Peak	667.263434405 kHz	40.64	N gnd	-15.36
2	Average	7.94912631806 MHz	19.51	N gnd	-30.48
1	Quasi Peak	13.2041199595 MHz	42.01	L1 gnd	-17.98
2	Average	13.2041199595 MHz	30.86	N gnd	-19.13

Conducted EMI, With Ground Plane (Floating)



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.74571035065 kHz	22.61	L1 gnd	
2	Average	133.454986145 kHz	8.44	N gnd	
2	Average	774.672132397 kHz	25.51	N gnd	-20.48
2	Average	2.1374603093 MHz	16.88	L1 gnd	-29.11
2	Average	10.1942139227 MHz	13.47	N gnd	-36.52
2	Average	29.8580960942 MHz	16.82	L1 gnd	-33.17

Figure 60 – Conducted EMI Scans, 48 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits**.**

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13 Line Surge Test

The unit was subjected to ±2500 V, 100 kHz ring wave and ±500 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

Figure 61 – (+)500 V Differential Surge, 90º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 µs / div.

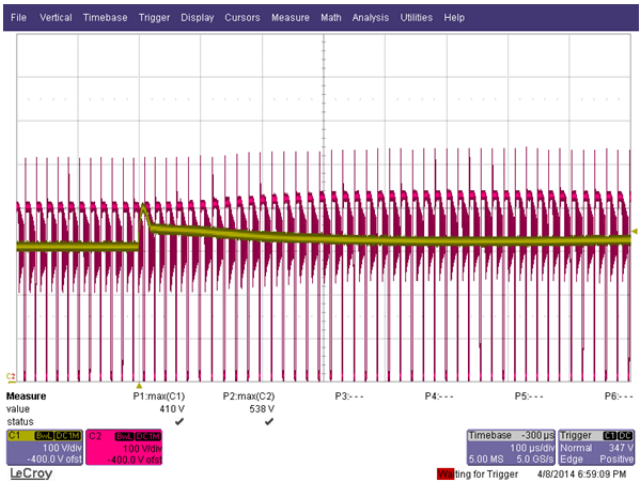

Figure 62 – (+)500 V Differential Surge, 0º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 µs / div.

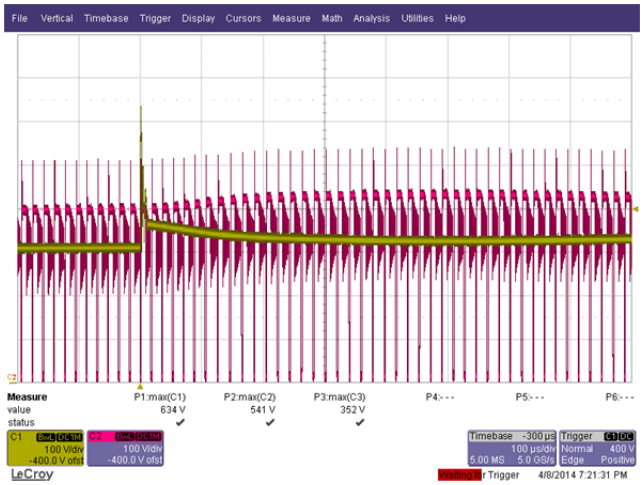

Figure 63 – (+)2.5 kV Ring Wave, 90º.
Upper: V_{BULK}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 μs / div.

Figure 64 – (-)2.5 kV Ring Wave, 270º.
Upper: V_{BULK}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 μs / div.

13.1 1 kV Differential Line Surge Options

For 1 kV differential line surge requirements, C1 may be replaced with a 22 μF capacitor to limit the voltage stress across C1. Alternatively, adding an MOV may also be used.

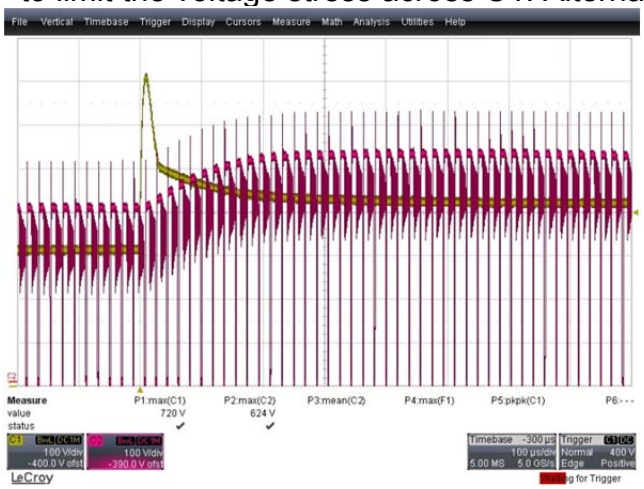

Figure 65 – C1 = 22 μF.
(+)1000 V Differential Surge, 90º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 μs / div.

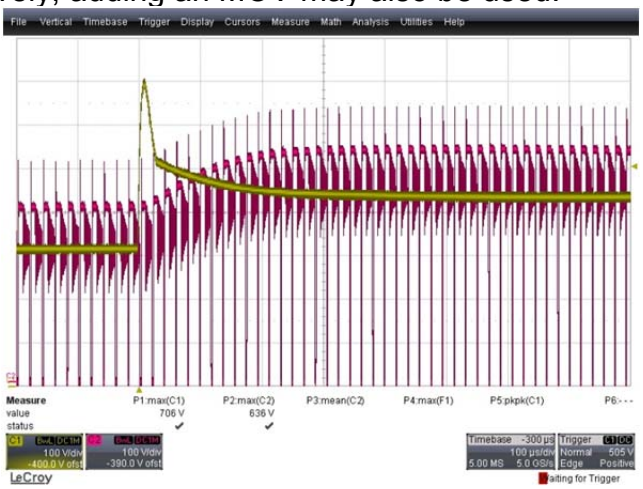

Figure 66 – C1 = 22 μF.
(-)1000 V Differential Surge, 270º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 μs / div.

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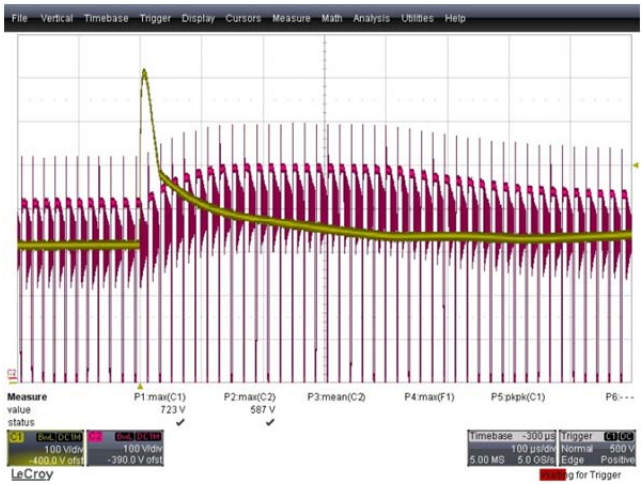

Figure 67 – With Additional 275 V MOV.
(+)1000 V Differential Surge, 90º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 µs / div.

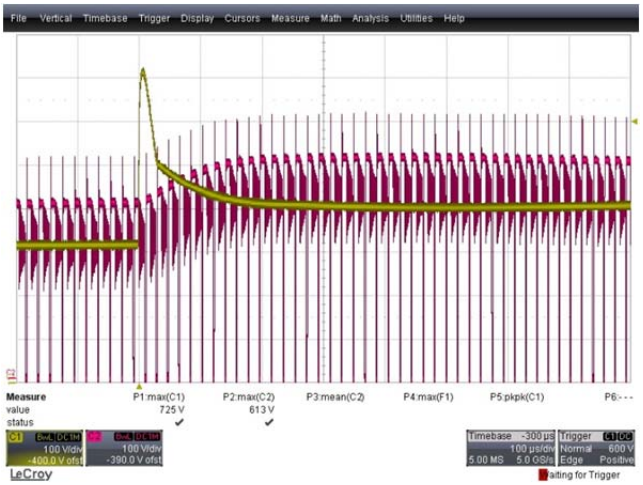

Figure 68 – With Additional 275 V MOV.
(-)1000 V Differential Surge, 270º.
Upper: V_{C1}, 100 V / div.
Lower: V_{DRAIN}, 100 V, 100 µs / div.

14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
20-May-14	DS	1.0	Initial Release	Apps & Mktg
22-Aug-14	DS	1.1	Added Voltage Ripple Measurements	

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