Design Example Report

Title	***4 W Power Factor Corrected (Valley Fill) Non-Dimmable Isolated Flyback, Constant Voltage LED Driver Using LYTSwitch™-2 LYT2003D***
Specification	Input: 190 VAC – 265 VAC (47 – 63 Hz); Output: 24 V, 167 mA
Application	Ballast LED Driver
Author	Applications Engineering Department
Document Number	DER-421
Date	August 20, 2014
Revision	1.2

Summary and Features

- Accurate primary side control constant voltage eliminates optocoupler and secondary control circuit.
- Combined CV/CC output characteristic
- Eliminates current sense resistors for better efficiency.
  - >80% active-mode efficiency.
- Easily meets CEC and ENERGY STAR 2.0 regulations
- No-load consumption <100 mW at 265 VAC
- Ultra-low leakage current: <5 μA at 265 VAC input.
- Easily meets EN550022 ,EN55015 and CISPR-22 Class B conducted EMI
- Auto-restart protection feature reduces power delivered to output by 95% during output short-circuit or open-loop fault conditions.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 4 W power supply that uses a LYTSwitch-2 IC, LYT2003D from the LYTSwitch-2 family, configured as a flyback. The power supply is specifically designed as an LED driver; however, it may also be used as a general evaluation platform for other applications that require constant voltage and constant current output.

This document contains the power supply specification, schematics, bill of materials, transformer documentation, printed circuit layout, and performance data.

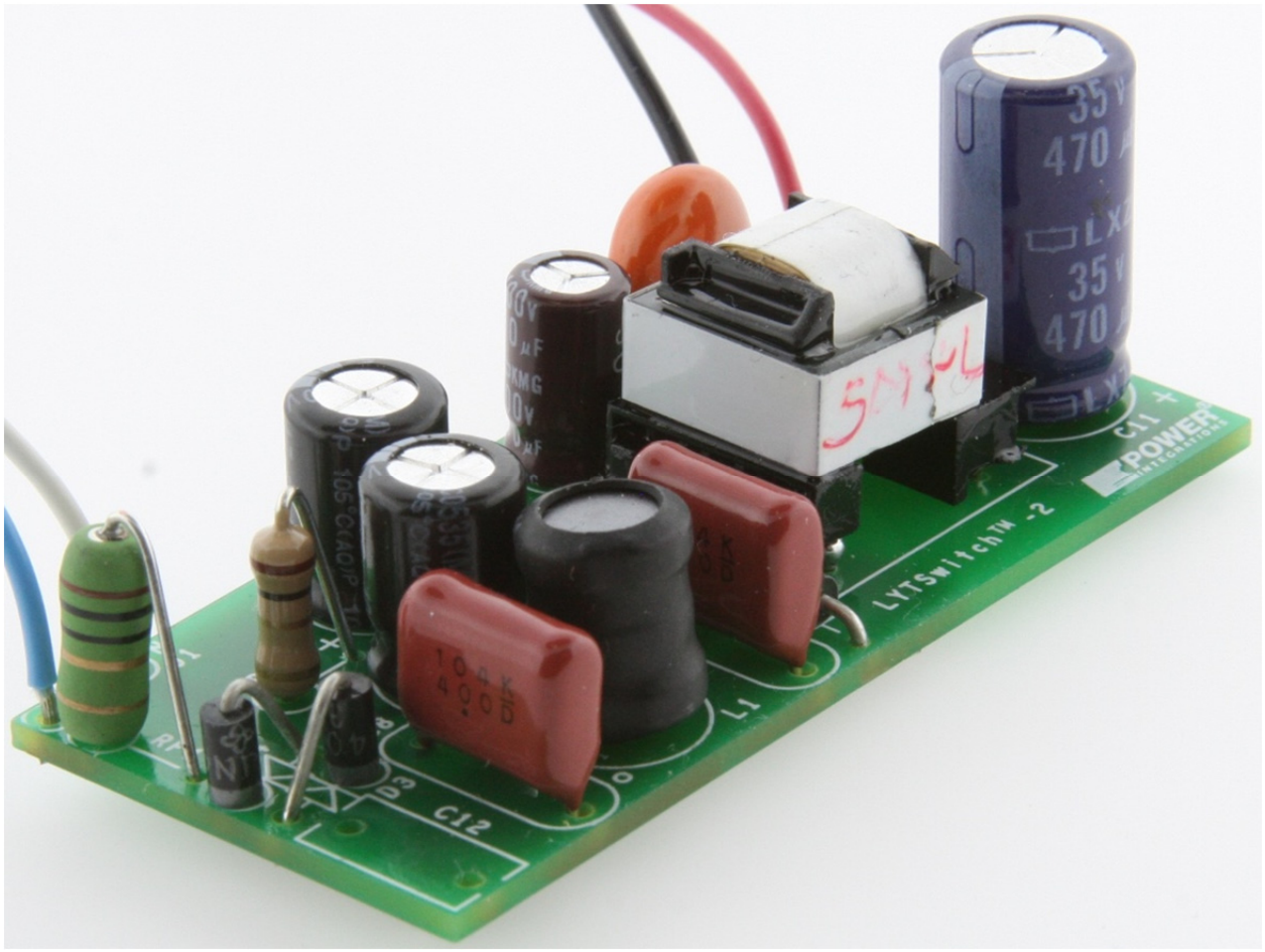

Figure 1 – Power Supply – Top Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power (230 VAC)				0.05	W	
In-rush Current (Cold start)	I_{RUSH}					269 V; 50 Hz – No damage will occur to the PSU nor should the fuse open
Power Factor		0.67				
Output						
CV Output Voltage	V_{OUT}	23	24	25	V	± 5%
CC Output Voltage Range		10		23	V	
Output Ripple Voltage	V_{RIPPLE}			1	V	Peak to peak, 20 MHz bandwidth-measured with 1 μF and 0.1 μF ceramic capacitor
Total Output Power						
Continuous Output Power	P_{OUT}			4	W	
Efficiency						
Required Average Efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{AVE}	75			%	Per Energy Star test method
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B/FCC Part 15				6 dBuV margin with grounded and ungrounded chassis
Safety		Designed to meet IEC950 / UL1950 Class II				
Leakage Current	I_{LEAK}	0.25 mA				Measured at 265 V_{RMS}, 50/60 Hz
Line Surge						
Differential Mode (L1-L2)				1	kV	IEC 61000-4-5/EN5504,
Common mode (L1/L2-PE)				2.5	kV	
Ring Wave (100 kHz)						500 A short-circuit Series Impedance:
Differential Mode (L1-L2)				2.5	kV	Differential Mode: 2 Ω
Common Mode (L1/L2-PE)					kV	Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		45	°C	Free convection, sea level

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3 Schematic

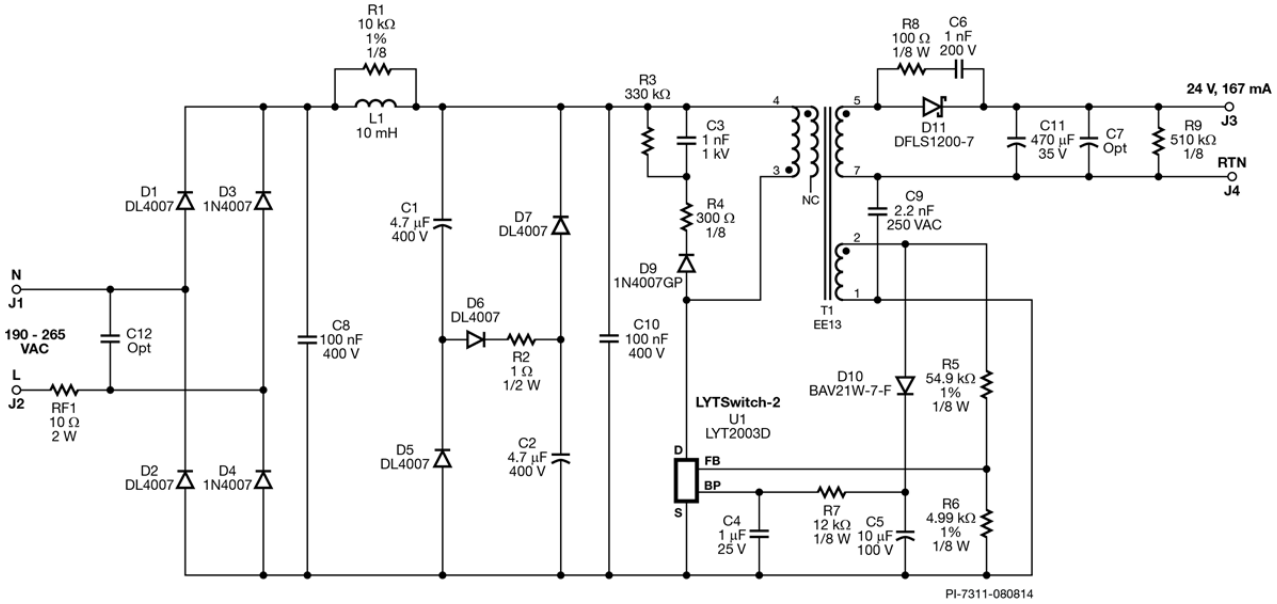

Figure 2 – Schematic.

4 Circuit Description

This LYTSwitch-2 based driver uses a flyback configuration to provide isolation between the primary and secondary. This converter provides 167 mA at 24 V over an input voltage range of 190 VAC to 265 VAC and is designed to drive LEDs in constant voltage or constant current operation. The LYTSwitch-2 IC controls the output using primary side regulation (PSR), reducing component count.

Being isolated, the user can dim by connecting a PWM converter, linear regulator or a DC-DC converter to the output.

This converter can also be used as an auxiliary supply for other types of lighting application.

4.1 Input Stage

Fusible resistor RF1 protects the power supply in the event that excessive input current is drawn. This fusible resistor aids in limiting the stress voltage during line transient and line surge as well as limiting the inrush current during a hot-plug.

The AC input is full wave rectified by diodes D1- D4 in full bridge configuration. The rectified DC is filtered by the bulk storage capacitors C8 and C10. Differential choke L1, C8 and C10 form the EMI filter which ensures compliance with Class B emission limits for conducted EMI. Resistor R1 damps the Q of L1, attenuating high frequency noise.

A passive (valley-fill) power factor correction circuit is employed to increase power factor to 0.74 at 230 VAC. This is composed of capacitors C1 and C2 and diodes D5, D6, D7 plus resistor R2. The valley-fill circuit also absorbs energy during differential line surges (IEC 61000-4-5/EN5504). At the point that the DC rectified voltage V_{IN} falls lower than the voltage across C1 and C2, they are effectively connected in parallel and supply power to the bulk capacitor (C10). Capacitors C1 and C2, which appear in series, are charged through D6 and R2 when V_{IN} DC is higher than the voltage across these capacitors. This forces input current to follow the input voltage, as shown in Figures 22 to 25, thus increasing PF.

4.2 LYTSwitch-2 - LYT2003D

The LYT2003D IC (U1) combines a power switching MOSFET, an oscillator, CV/CC control engine, as wells as start-up and protection circuits into one IC.

The control input regulates both the output voltage in CV mode and the output current in CC mode. Control is achieved by measuring forward and flyback voltages developed across the bias winding which is fed to the FB pin. Resistors R5 and R6 are 1% resistors to center the nominal (CV) V_{OUT} and to ensure accurate constant current regulation. The device uses an ON/OFF control technique with multiple states to minimize audible noise and to optimize efficiency in CV mode operation. Variable frequency control is used in CC mode.

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IC U1 is supplied from the BP (BYPASS) pin and the decoupling capacitor C4. IC U1 uses the energy stored in C4 when the MOSFET is on, and an internal 6 V regulator draws current from the MOSFET DRAIN pin when the MOSFET is off.

To minimize power consumption during no-load, especially at highest input voltage, the design employs the external supply voltage from the feedback/bias winding, through diode D10 and resistor R7 plus capacitor C5. Note that the bias winding return is directly connected to the bulk capacitor C10 ground point in the layout, which helps increase surge immunity.

This design used of a RCD-R clamp comprising of diode D9, capacitor C3 and resistors R3 and R4 to limit the MOSFET's drain voltage due to the leakage inductance of the transformer. The loop formed by this clamp and the primary winding of the transformer T1 is made small to reduce radiation EMI.

4.3 Output Rectification

Schotkky diode D11 rectifies the transformer secondary output and the rectified voltage is filtered by the output capacitor C11. Capacitor C11 has low ESR to reduce output voltage ripple. The output does not need an LC post filter.

Secondary RC-snubber (R8 and C6) is used across D11 to reduce radiated EMI.

4.4 Overvoltage Protection

In the event of a fault condition, the LYTSwitch-2 IC enters a protection mode. If the FEEDBACK pin voltage falls below 0.7 V during the flyback period ($t_{AR(ON)}$) the converter enters auto-restart. Subsequently, if the FEEDBACK pin current during the forward period of the conduction cycle falls below 120 μA, the converter infers an open-loop condition and inhibits switching. Refer to the data sheet for details of the auto-restart and open-loop protection features of the LYTSwitch-2 family of ICs.

4.5 PCB Layout

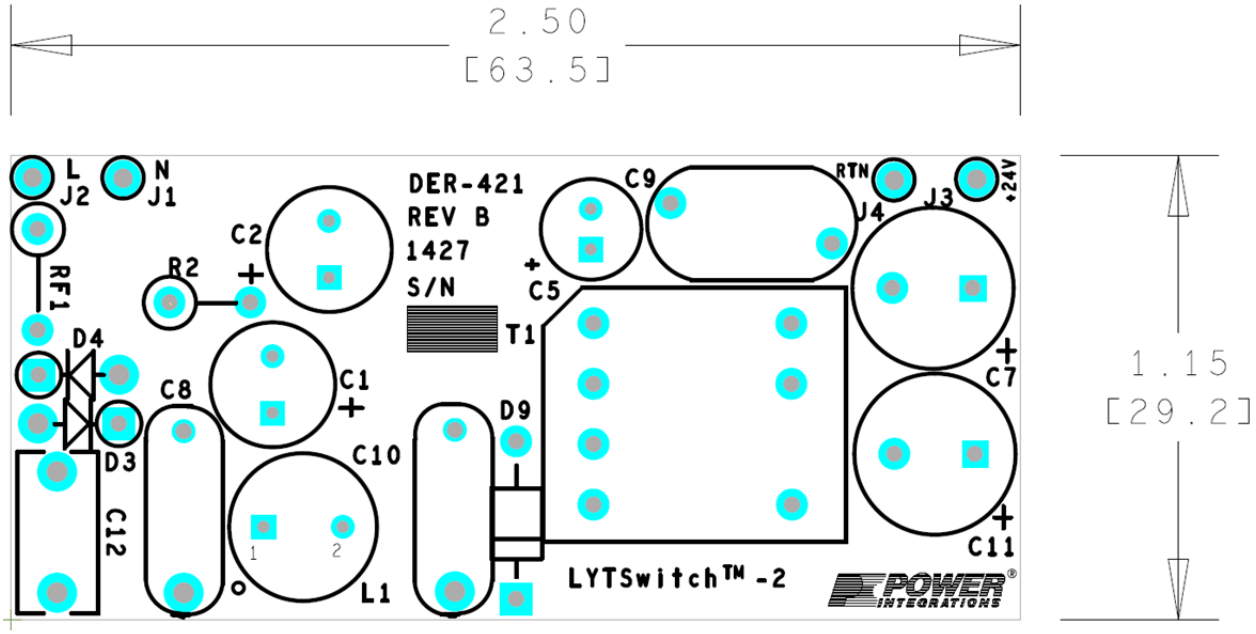

Figure 3 – Printed Circuit Layout, Top. (2.5 in [63.5 mm] L x 1.15 in [29.2 mm] W)

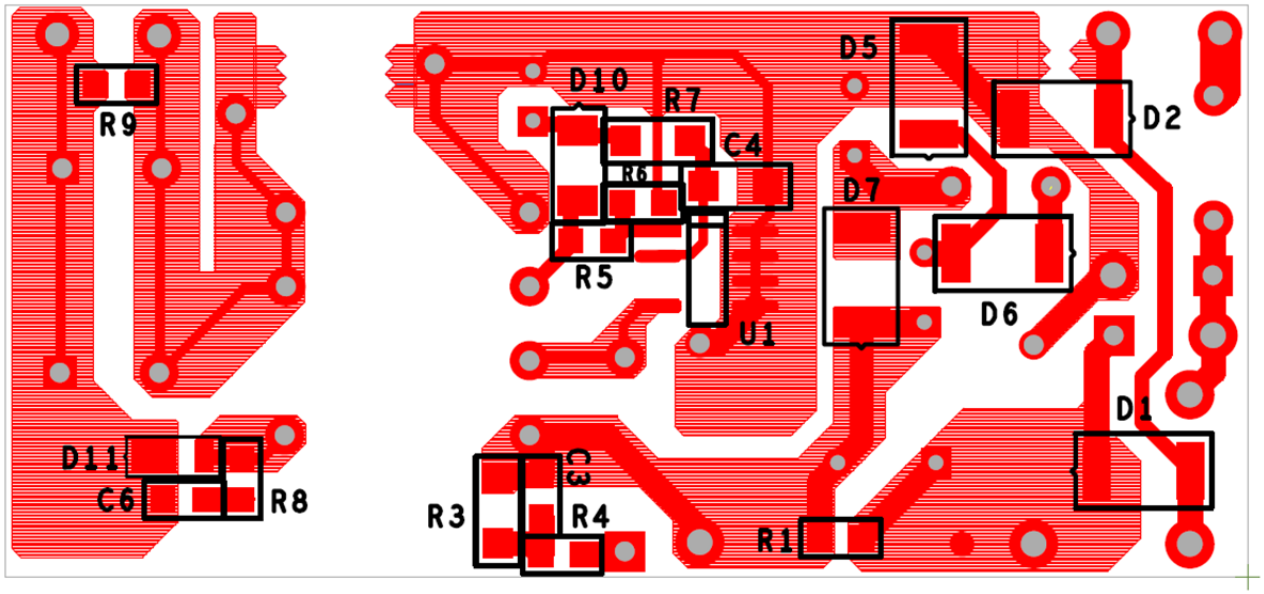

Figure 4 – Printed Circuit Layout, Bottom.

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5 PCB Assembly

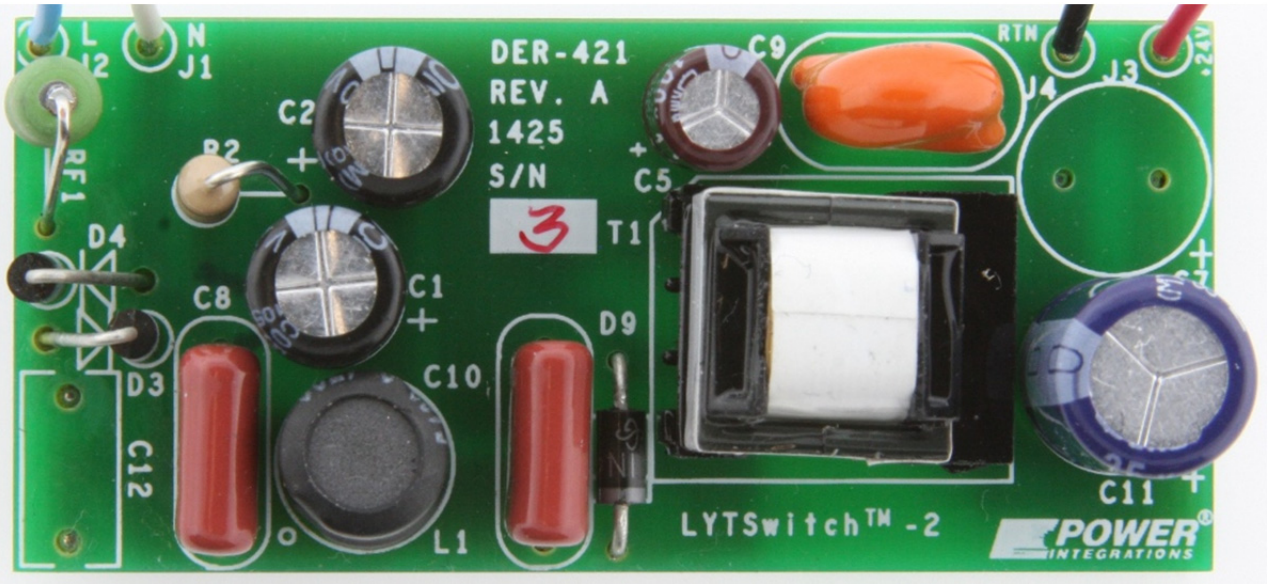

Figure 5 – PCB Assembly Top.

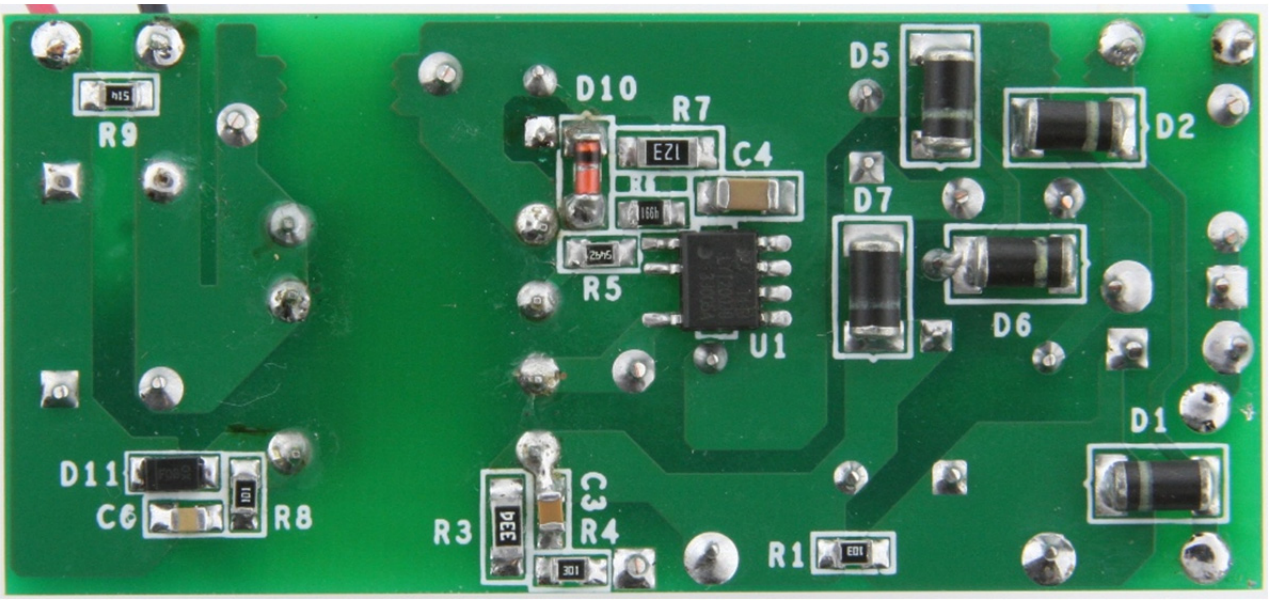

Figure 6 – PCB Assembly Bottom, Showing the LYTSwitch-IC.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C2	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	SHD400WV 4.7uF	Sam Young
2	1	C3	1 nF, 1000 V, Ceramic, X7R, 0805	C0805C102KDRACTU	Kemet
3	1	C4	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
4	1	C5	10 μF, 100 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG101ELL100MF11D	Nippon Chemi-Con
5	1	C6	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
6	1	C11 C7 (Opt)	470 μF, 35 V, Electrolytic, Low ESR, 52 mΩ, (10 x 20)	ELXZ350ELL471MJ20S	Nippon Chemi-Con
7	2	C8 C10	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
8	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
9	0	C12 (Opt)	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
10	5	D1 D2 D5 D6 D7	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
11	2	D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
12	1	D9	1000 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4007GP	Vishay
13	1	D10	250 V, 0.2 A, Fast Switching, 50 ns, SOD-123	BAV21W-7-F	Diodes, Inc.
14	1	D11	200 V, 1 A, DIODE SCHOTTKY 1 A 200 V PWRDI 123	DFLS1200-7	Diodes, Inc.
15	1	L1	10 mH, 0.076 A, 20%	RL-5480-3-10000	Renco
16	1	R1	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
17	1	R2	1 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-1R0	Yageo
18	1	R3	330 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ334V	Panasonic
19	1	R4	300 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
20	1	R5	54.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5492V	Panasonic
21	1	R6	4.99 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4991V	Panasonic
22	1	R7	12 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ123V	Panasonic
23	1	R8	100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
24	1	R9	510 k Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ514V	Panasonic
25	1	RF1	10 Ω, 2 W, Wire Wound Fusible	FW20A10R0JA	Bourns
26	1	T1	Bobbin, EE13, Horizontal, 8 pins Transformer	Custom SNX-R1748	Custom Santronics
27	1	U1	LYTSwitch-2, CV/CC, SO-8D	LYT2003D	Power Integrations
Mechanical BOM					
1	1	J3	Wire, UL1007, #22 AWG, Red, PVC, 4 inches	1007-22/7-02	Anixter
2	1	J4	Wire, UL1007, #22 AWG, Blk, PVC, 4 inches	1007-22/7-00	Anixter
3	1	J1	Wire, UL1007, #22 AWG, Wht, PVC, 4 inches	1007-22/7-09	Anixter
4	1	J2	Wire, UL1007, #22 AWG, Blu, PVC, 4 inches	1007-22/7-06	Anixter

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7 Transformer Specification

7.1 Electrical Diagram

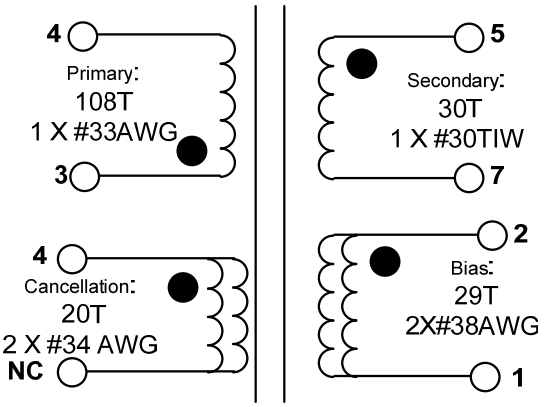

Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 8-9.	3000 VAC
Primary Inductance	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1100 μH ±10%
Resonant Frequency	Pins 3-4 all other windings open.	700 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, and pins 5-7 shorted, measured at 100 kHz, 0.4 V_{RMS}.	50 μH (Max.)

7.3 Materials

Item	Description
[1]	Core: EE13, PC34, AL = 94nH/A^2 ±10%.
[2]	Bobbin: EE13;4/4 pin; Extended horizontal; Hical magnetics-548 or equivalent (PI part number 25-00002-00)
[3]	Triple Insulated Magnet Wire: #30 AWG.
[4]	Magnet Wire: #33 AWG.
[5]	Magnet Wire: #34 AWG.
[6]	Magnet Wire: #38 AWG.
[7]	Transformer Polyester film tape; 7.9 mm wide.
[8]	Varnish.

7.4 Transformer Build Diagram

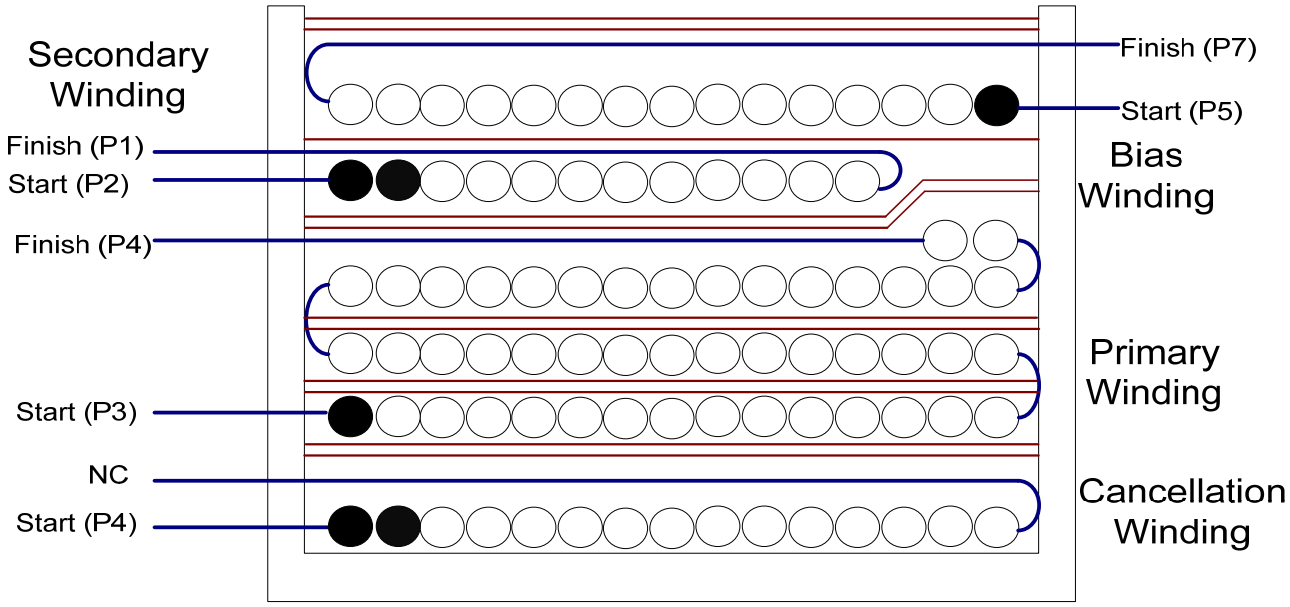

Figure 8 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise. Follow the pin number assignment in the specification. Construction description starts with the wire closest to the bobbin. Construction description starts with the wire closest to the bobbin. Cut pin number 6.
WDG1; Cancellation Winding	Wound 20 turns (x 2 filar) of Item [5] and solder the start of this winding at pin 4. Spread the winding evenly across the entire bobbin. Finish this winding by temporarily (do not solder) winding it on pin 8. Leave this end of primary shield winding not connected. Bend the end 90 degrees with respect to the wound wire and cut this wire in the middle of the bobbin.
Insulation	Add 2 layer of tape, item [7], for insulation.
WDG2; Primary Winding	Wound 108 turns (x 1 filar) of Item [4], terminating this start at pin 3 (soldered). Spread the winding evenly across the entire bobbin in four layers, placing two layers of tape, Item [7], in between layers. Finish this winding on pin 4 (soldered).
Insulation	Add 2 layers of tape, item [7], for insulation.
WDG3; Bias Winding	Wound 29 turns (x 2 filar) of Item [6], soldering this start on pin 2. Spread the winding evenly across the entire bobbin. Terminate the end of this winding on pin 1 (soldered).
Insulation	Add 2 layers of tape, item [7], for insulation.
WDG4; Secondary Winding	Wound 30 turns (x 1 filar) of Item [3], terminating this start on pin 5 (soldered). Evenly spread the winding across the bobbin. Terminate this end on pin 7 (soldered).
Insulation	Add 2 layers of tape, item [7], for insulation.
Core Preparation	Grind one of the cores to get the desired inductance. Wrap with 2 layers of tape to secure the cores together.
Varnish	Dip the transformer to the varnish Item [8], then, dry.

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8 Transformer Design Spreadsheet

ACDC_LYTSwitch-2_102413; Rev.1.0; Copyright Power Integrations 2013	INPUT	INFO	OUTPUT	UNIT	ACDC_LYTSwitch-2_102413_Rev1-0; Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	120		120.00	V	Minimum AC Input Voltage
VACMAX	265		265.00	V	Maximum AC Input Voltage
fL	50		50.00	Hz	AC Mains Frequency
Application Type	**Ballast**		Ballast		Choose application type
VO	24.00		24.00	V	Output Voltage (at continuous power)
IO	0.17		0.17	A	Power Supply Output Current (corresponding to peak power)
Power			4.08	W	Continuous Output Power
n	0.80		0.80		Efficiency Estimate at output terminals
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	9.40		9.40	uF	Input Capacitance
ENTER LYTSwitch-2 VARIABLES					
Chosen Device	**LYT2003D**		LYT2003D		Chosen LYTSwitch-2 device
ILIMITMIN			0.36	A	Minimum Current Limit
ILIMITTYP			0.39	A	Typical Current Limit
ILIMITMAX			0.42	A	Maximum Current Limit
FS	60.00		60.00	kHz	Typical Device Switching Frequency at maximum power
VOR			73.66	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LYTSwitch-2 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP_WORST_CASE			2.41		KP assuming minimum LP, VMIN, and Maximum Switching Frequency. Ensure that this value is above 1.00
FEEDBACK WINDING PARAMETERS					
NFB	29.00		29.00		Feedback winding turns
VFLY			19.74	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			39.10	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
VB			N/A	V	Feedback Winding Voltage (VFLY) is greater than 10 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.
NB			N/A		Bias Winding number of turns
REXT			29.00	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON			4.60	us	Output diode conduction time
TON			2.33	us	LYTSwitch-2 On-time (calculated at minimum inductance)
RUPPER		Info	46.41	k-ohm	Upper resistor in Feedback resistor divider. Once the initial prototype is running, it is necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current
RLOWER			5.06	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					

Core Type					
Core	**EE13**		EE13		Enter Transformer Core.
Bobbin			BE-13		Bobbin part number
AE			17.10	mm^2	Core Effective Cross Sectional Area
LE			30.20	mm	Core Effective Path Length
AL			1130.00	nH/turn^2	Ungapped Core Effective Inductance
BW			7.40	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3.00		Number of Primary Layers
NS			36.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			145.62	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.17		Maximum duty cycle measured at VMIN
IAVG			0.04	A	Input Average current
IP			0.36	A	Peak primary current
IR			0.36	A	Primary ripple current
IRMS			0.10	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			933.39	uH	Minimum Primary Inductance
LPTYP			1037.10	uH	Typical Primary inductance
LP_TOLERANCE			10.00	%	Tolerance in primary inductance
NP			108.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			88.91	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2190.06		2190.06	Gauss	Target Flux Density
BM			2190.06	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended
BP			2575.85	Gauss	Peak Operating Flux Density (calculated at maximum inducatnce and max current limit), BP < 3000 is recommended
BAC			1095.03	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			158.81		Relative Permeability of Ungapped Core
LG			0.25	mm	Gap Length (LG > 0.1 mm)
BWE			22.20	mm	Effective Bobbin Width
OD			0.21	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.16	mm	Bare conductor diameter
AWG			34	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			40.32	Cmils	Bare conductor effective area in circular mils
CMA			401.84	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			1.09	A	Peak Secondary Current
ISRMS			0.42	A	Secondary RMS Current
IRIPPLE			0.39	A	Output Capacitor RMS Ripple Current
CMS			84.64	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			30.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			549.45	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)

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PIVS			148.92	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL	52.30		52.30	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL	4.99		4.99	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)	22.87		22.87	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)	0.17		0.17	Amps	Measured Output current from first prototype
RUPPER_FINE			54.89	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 54.9 k-ohms
RLOWER_FINE			4.97	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 4.99 k-ohms

Note: VACMIN = 120 V to guarantee start-up at 190 V for a valley-fill circuit.

9 Performance Data

All measurements performed at room temperature unless specified.

9.1 Efficiency

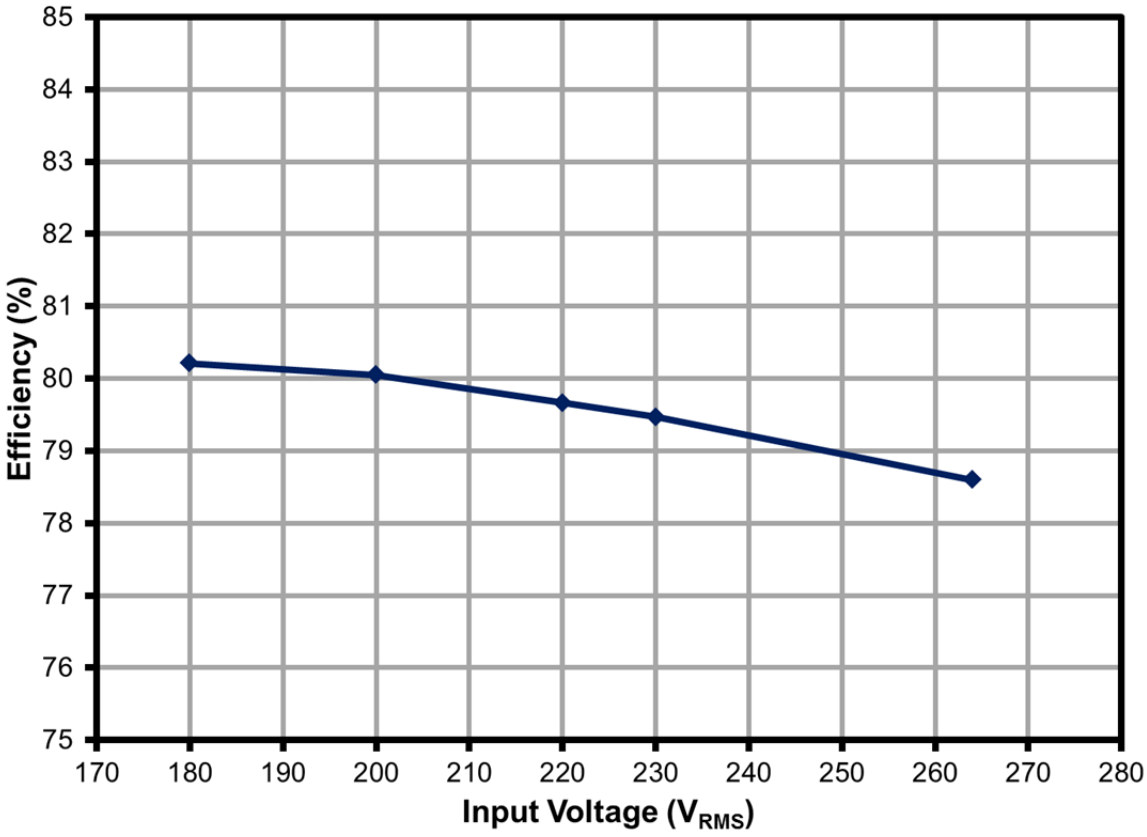

Figure 9 – Efficiency vs. Input Voltage, Room Temperature, 50 Hz.

Input Measurement				Load Measurement			
V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
179.93	0.03	4.93	0.783	23.98	0.17	3.96	80.21
199.91	0.03	4.94	0.767	23.98	0.17	3.96	80.05
219.97	0.03	4.96	0.748	23.98	0.17	3.96	79.67
229.91	0.03	4.98	0.738	23.97	0.17	3.95	79.47
263.99	0.03	5.03	0.672	23.96	0.17	3.95	78.60

Table 1 – Data for Figure 9.

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9.2 Active Mode Efficiency

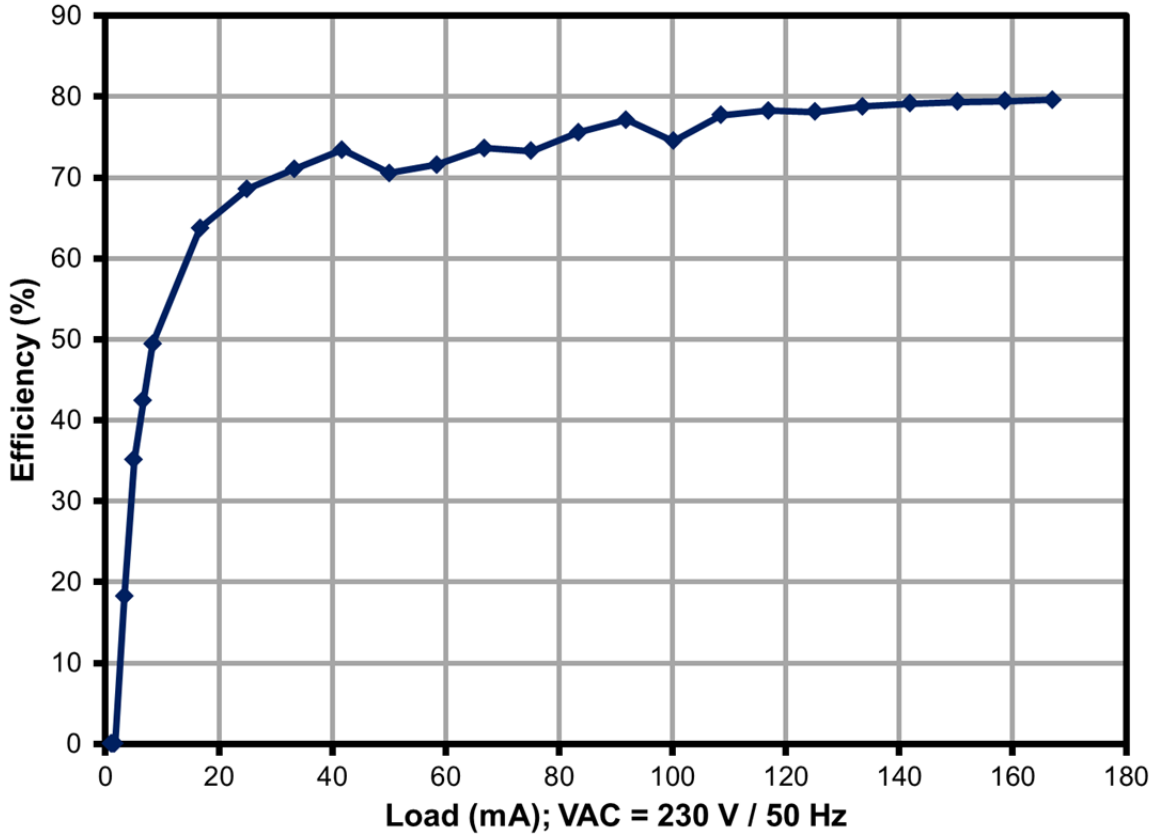

Figure 10 – Efficiency vs Load, 230 V_{RMS} / 50 Hz line, Room Temperature.

Load Setting		Input Measurement				Load Measurement			
% Load	Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	PF	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency (%)
100%	0.1670	229.91	0.03	4.97	0.74	23.98	167.00	3.96	79.58
95%	0.1587	229.91	0.03	4.72	0.73	23.98	158.65	3.75	79.43
90%	0.1503	229.91	0.03	4.48	0.72	24.00	150.30	3.56	79.35
85%	0.1420	229.91	0.03	4.23	0.72	23.93	141.95	3.34	79.13
80%	0.1336	229.91	0.02	3.98	0.76	23.85	133.60	3.14	78.79
75%	0.1253	229.91	0.02	3.76	0.74	23.84	125.25	2.94	78.13
70%	0.1169	229.91	0.02	3.49	0.69	23.80	116.90	2.73	78.28
65%	0.1086	229.91	0.02	3.26	0.67	23.80	108.55	2.53	77.69
60%	0.1002	229.91	0.02	3.11	0.67	23.65	100.20	2.32	74.50
55%	0.0919	229.91	0.02	2.77	0.65	23.80	91.85	2.13	77.13
50%	0.0835	229.91	0.02	2.56	0.63	23.75	83.50	1.93	75.58
45%	0.0752	229.91	0.02	2.35	0.64	23.61	75.15	1.72	73.25
40%	0.0668	229.91	0.01	2.08	0.62	23.66	66.80	1.53	73.62
35%	0.0585	229.91	0.01	1.85	0.61	23.58	58.45	1.33	71.59
30%	0.0501	229.91	0.01	1.60	0.60	23.58	50.10	1.13	70.55
25%	0.0418	229.91	0.01	1.27	0.51	23.57	41.75	0.93	73.45
20%	0.0334	229.91	0.01	1.03	0.59	23.47	33.40	0.73	71.05
15%	0.0251	229.91	0.01	0.78	0.39	23.48	25.05	0.54	68.57
10%	0.0167	-0.01	0.00	0.53	0.30	23.49	16.70	0.34	63.74
5%	0.0084	229.91	0.01	0.29	0.24	23.68	8.35	0.14	49.45
4%	0.0067	229.91	0.00	0.24	0.29	23.33	6.68	0.10	42.41
3%	0.0050	229.92	0.00	0.18	0.25	23.73	5.01	0.06	35.08
2%	0.0033	229.92	0.00	0.17	0.32	23.32	3.34	0.03	18.21
1%	0.0017	229.92	0.00	0.12	0.29	23.40	1.67	0.00	0.00
0.80%	0.0013	229.91	0.00	0.12	0.28	23.43	1.34	0.00	0.00
0.60%	0.0010	229.91	0.00	0.11	0.27	23.46	1.00	0.00	0.00
							% Average Efficiency		76.68

Table 2 – Data for Figure 10.

For adapter applications that require compliance to ENERGY STAR, the external power supply requirements indicated in 8.2.1 and 8.2.2 describes active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined by the nameplate output power and the output voltage as shown in the tables in 8.2.1 and 8.2.2. The efficiency is the average efficiency measure at 25, 50, 75 and 100% load.

The measurements are done at a single rated input voltage for power supplies that are specified at either low line (115 VAC) or high line (230 VAC) only. For this design, 230 VAC was selected.

The approved test method can be found here:
http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

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For the latest up to date information, please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0

This specification took effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq$ 550 mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

9.3 No-Load Input Power

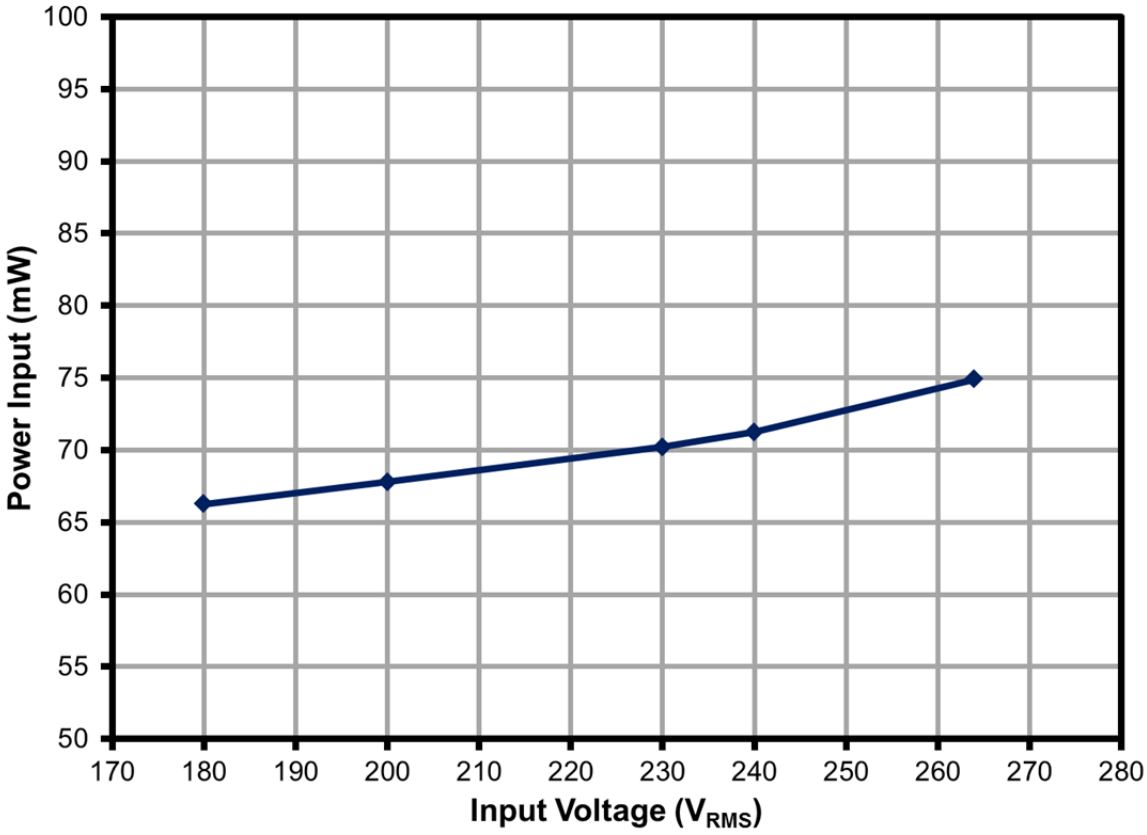

Figure 11 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

Input		Input Measurement			Output Voltage (V)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (mW)	
180	50	179.94	1.55	67.70	66.27
200	50	199.92	1.45	68.30	67.80
230	50	229.91	1.30	68.90	70.22
240	50	239.94	1.32	71.10	71.24
264	50	263.97	1.23	75.60	74.92

Table 3 – Data for Figure 11.

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9.4 Regulation

9.4.1 Output Voltage vs. Load

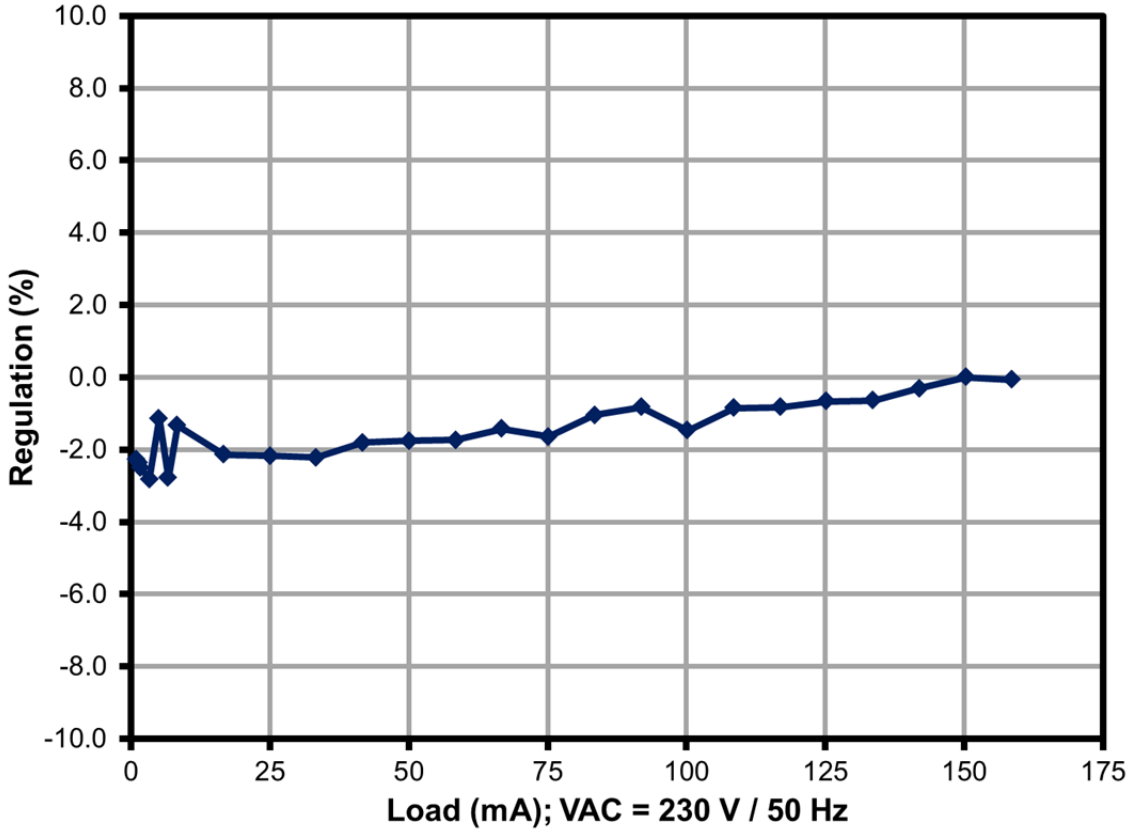

Figure 12 – V_{OUT} Regulation vs. Load, Room Temperature.

9.4.2 Output Voltage vs. Line

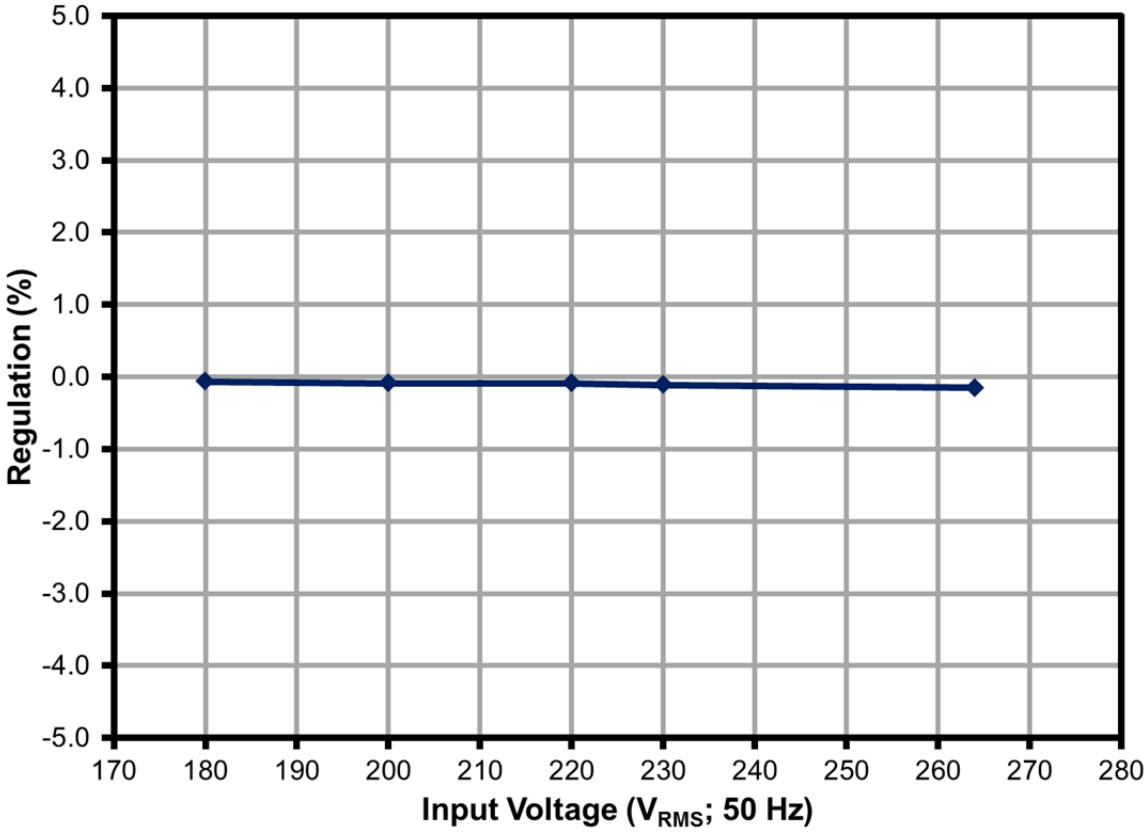

Figure 13 – V_{OUT} Regulation vs. AC Input Voltage, Room Temperature, Full Load and 50 Hz.

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9.5 Power Factor (PF)

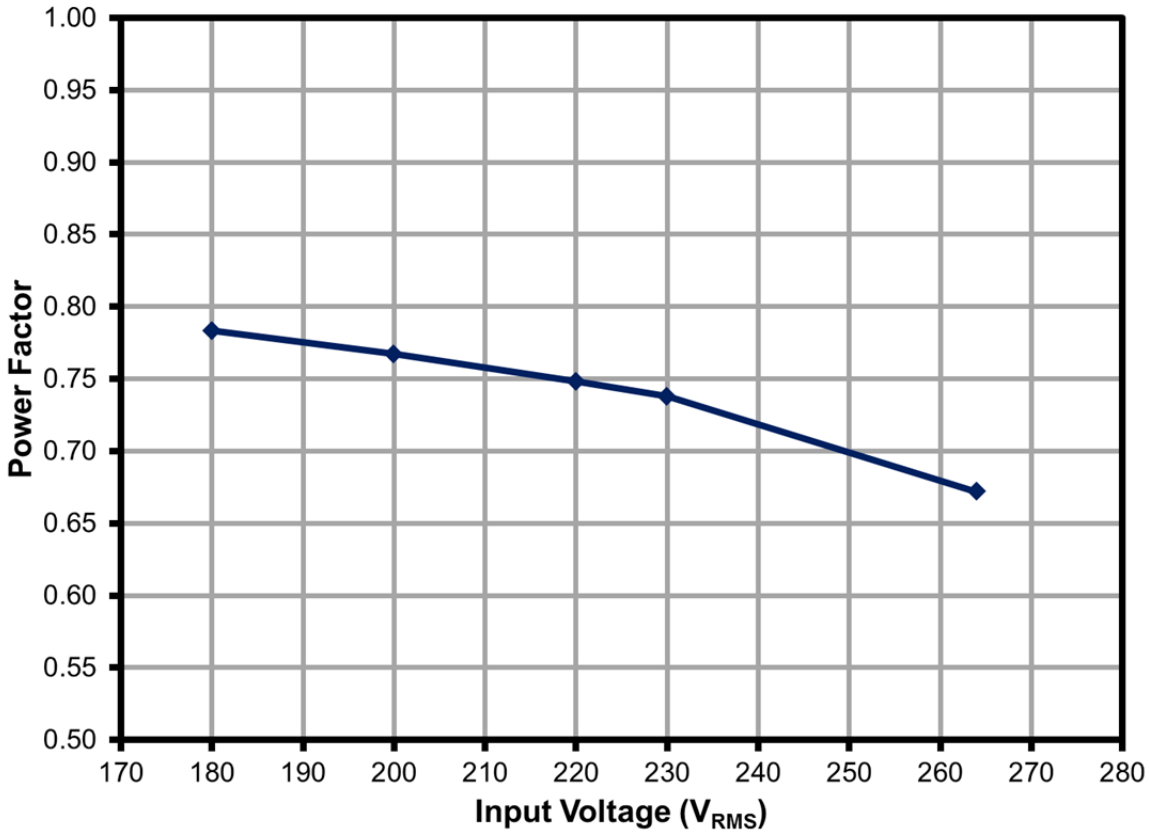

Figure 14 – Power Factor vs. AC Input, Full Load.

9.6 CV/CC Curve

Load resistance is reduced from 1,500 Ω down to the point the unit will enter auto-restart.

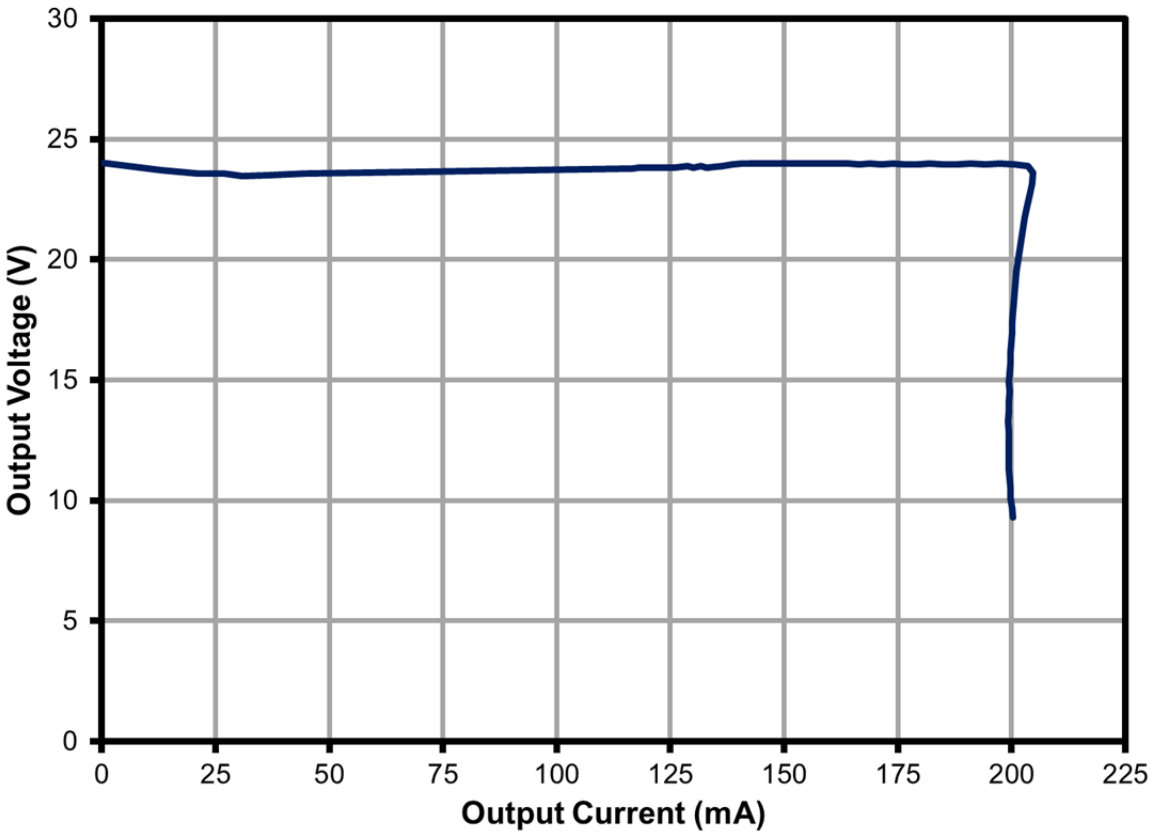

Figure 15 – CV/CC Curve Using CR Mode of Electronic Load.

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9.7 Power Curve

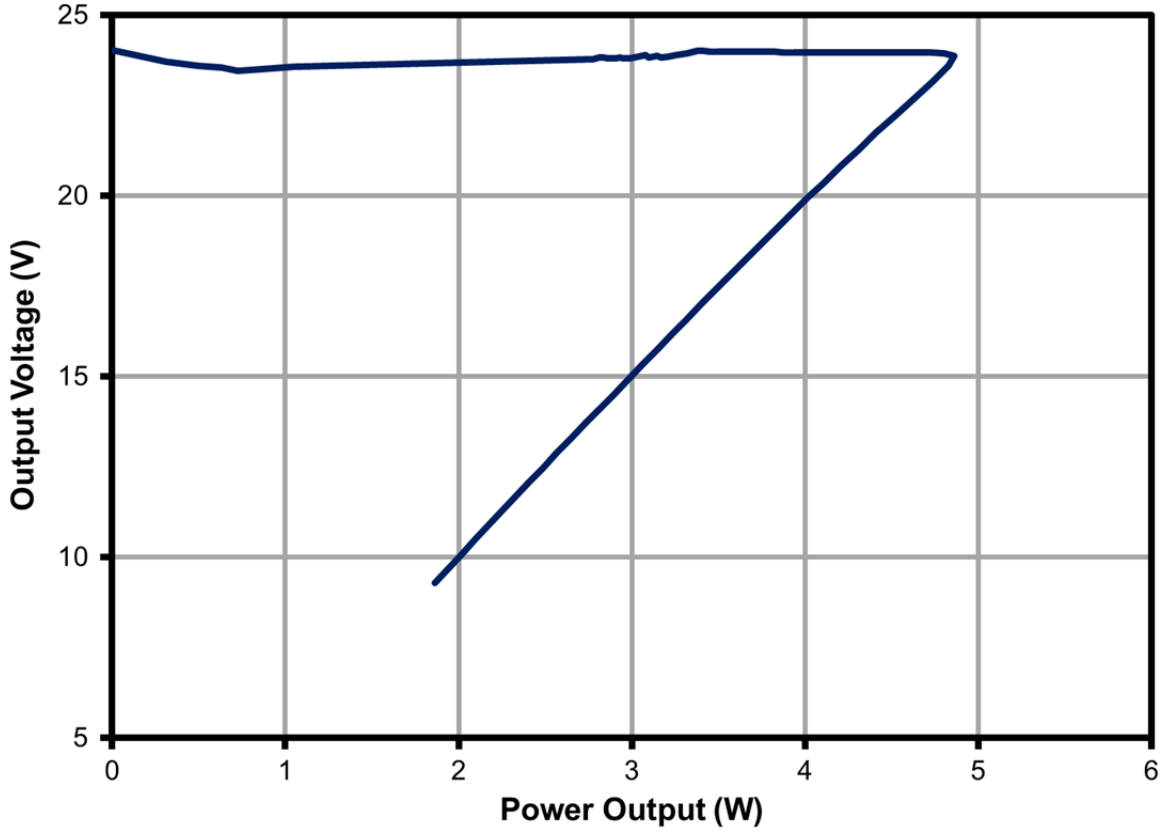

Figure 16 – Power Curve in CR Mode from Electronic Load.

9.8 Thermal Performance

9.8.1 Thermal Images

Thermals measurements were taken without enclosure (open frame). Temperatures were allowed to stabilize for >60 minutes prior to taking the thermal images.

9.8.2 Test Conditions (190 VAC, 50 Hz, 25 °C Ambient)

9.8.2.1 Component Side

Figure 17 – Top side component guide for thermal scan.

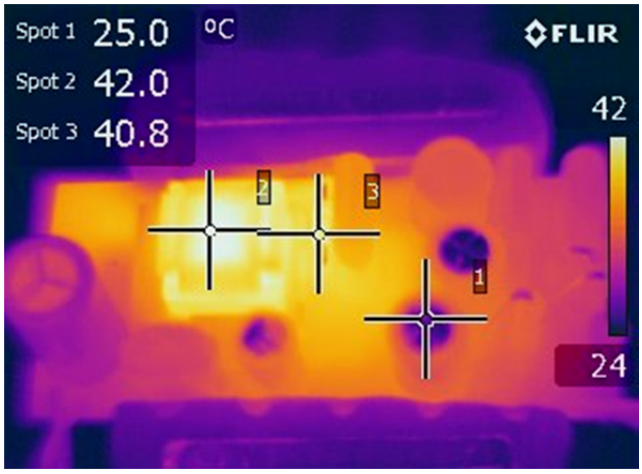

Figure 18 – SP1 – Valley Fill PFC Capacitor (C2).
SP2 – Transformer (T1).
SP3 – Primary Snubber Diode (D9).

Figure 19 – SP1 – Bias Capacitor (C5).
SP2 – Output Capacitor (C11).
SP3 – Valley Fill PFC Capacitor (C1).

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9.8.2.2 Solder Side

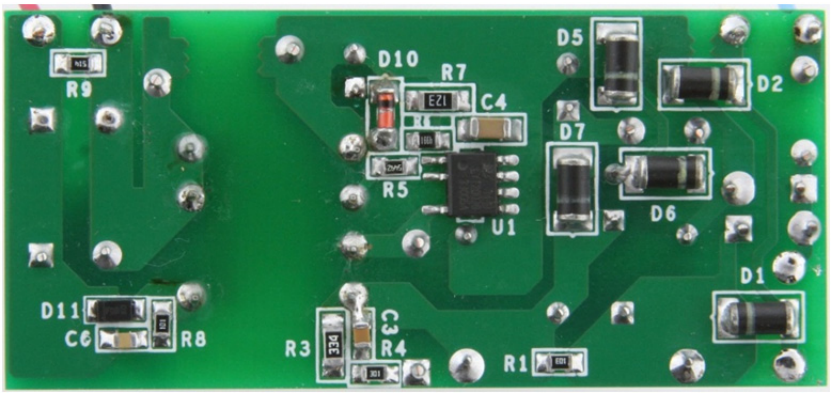

Figure 20 – Bottom side component guide for thermal scan.

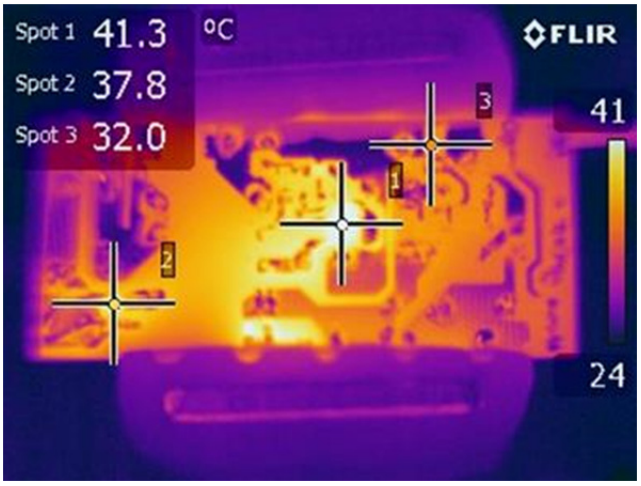

Figure 21 – SP1 – LYT2003D (U1).
SP2 – Output Diode (D11).
SP3 – Bridge Diode (D2).

9.8.3 Test Conditions (265 VAC, 50 Hz, 25 °C Ambient)

9.8.3.1 Component Side

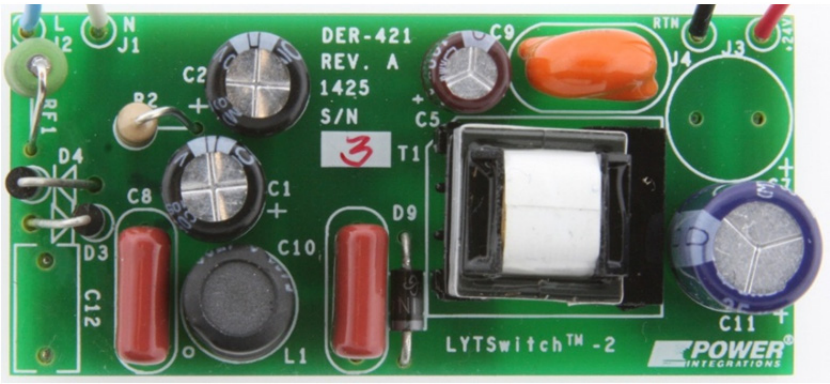

Figure 22 – Top side component guide for thermal scan.

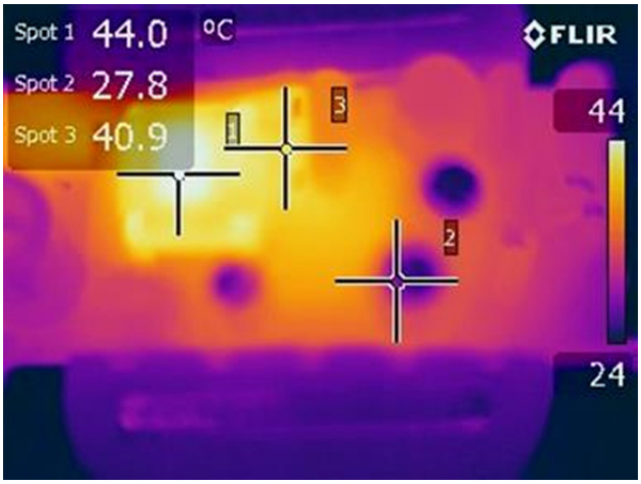

Figure 23 – SP1 – Transformer (T1).
SP2 – Valley Fill PFC Capacitor (C2).
SP3 – Primary Snubber Diode (D9).

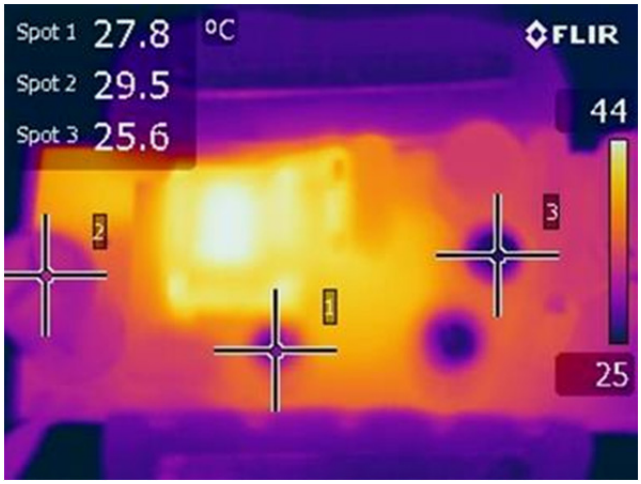

Figure 24 – SP1 – Bias Capacitor (C5).
SP2 – Output Capacitor (C11).
SP3 – Valley Fill PFC Capacitor (C1).

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9.8.3.2 Solder Side

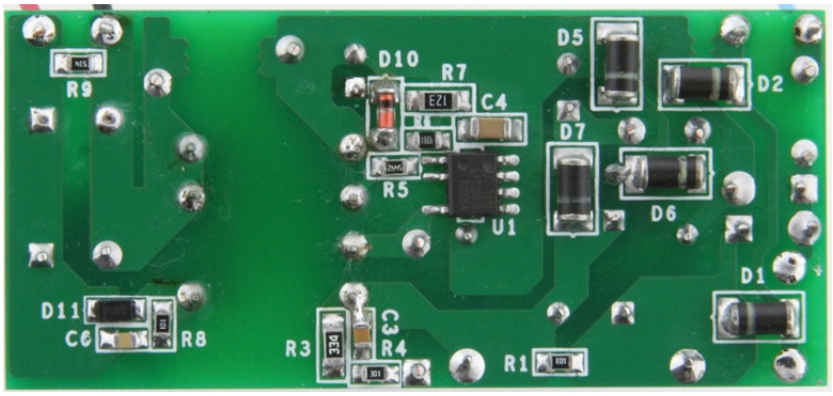

Figure 25 – Bottom side component guide for thermal scan.

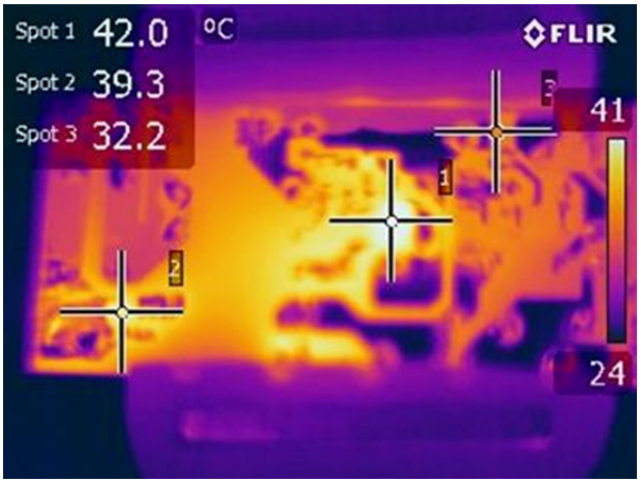

Figure 26 – SP1 – LYT2003D (U1).
SP2 – Output Diode (D11).
SP3 – Bridge Diode (D2).

10 Waveforms

10.1 Input Voltage and Current, Normal Operation

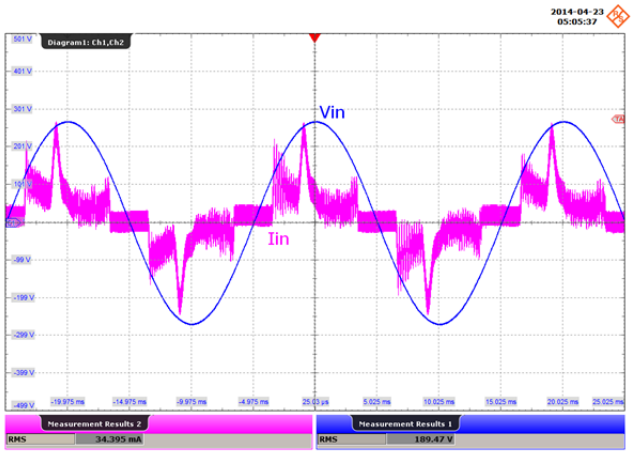

Figure 27 – 190 VAC, Full Load.
Pink: I_{IN}, 50 mA / div.
Blue (Sinusoidal Wave): V_{IN}, 100 V,
5 ms / div.

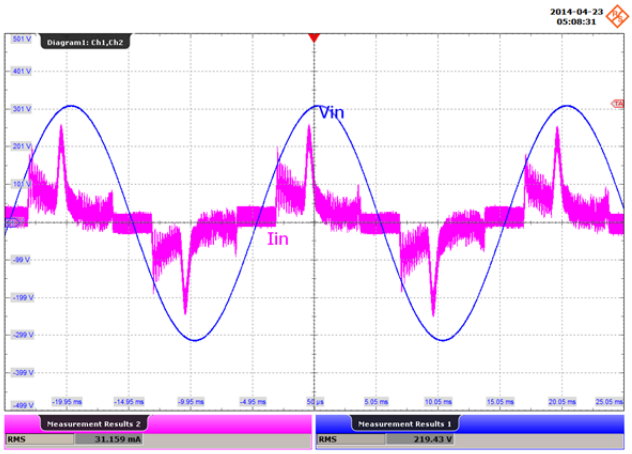

Figure 28 – 220 VAC, Full Load.
Pink: I_{IN}, 50 mA / div.
Blue (Sinusoidal Wave): V_{IN}, 100 V,
5 ms / div.

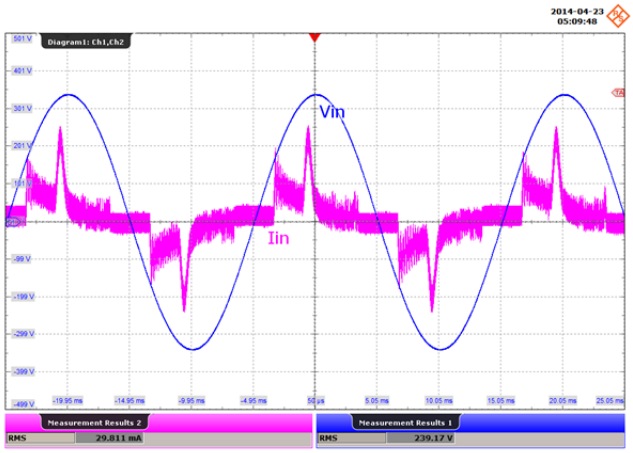

Figure 29 – 240 VAC, Full Load.
Pink: I_{IN}, 50 mA / div.
Blue (Sinusoidal Wave): V_{IN}, 100 V,
5 ms / div.

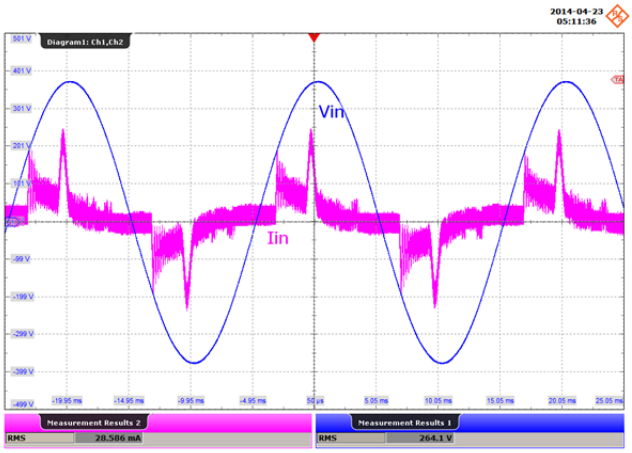

Figure 30 – 265 VAC, Full Load.
Pink: I_{IN}, 50 mA / div.
Blue (Sinusoidal Wave): V_{IN}, 100 V,
5 ms / div.

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10.2 Drain Voltage and Current, Normal Operation

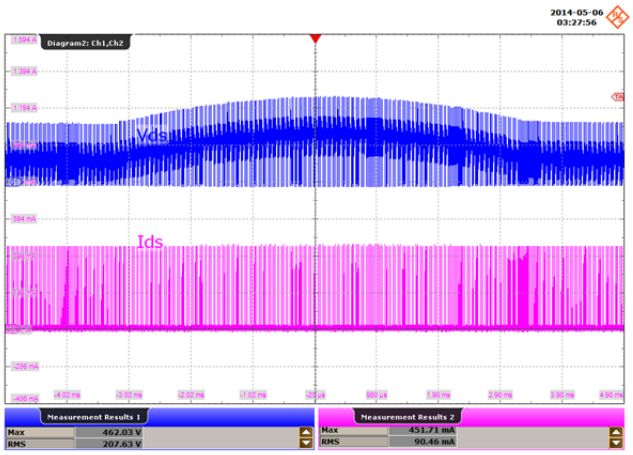

Figure 31 – 190 VAC, Full Load.
Upper: V_{DRAIN}, 200 V
Lower: I_{DRAIN}, 0.2 A / div., 1 ms / div.

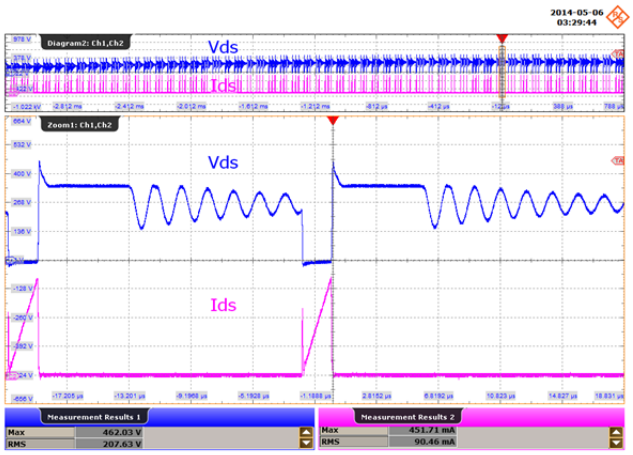

Figure 32 – 190 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div., 400 µs / div.
Zoom Time Scale: 4 µs / div.

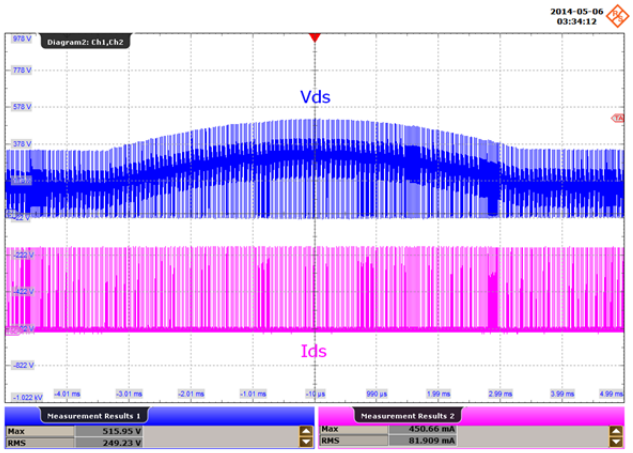

Figure 33 – 230 VAC, Full Load.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 0.2 A / div., 1 ms / div.

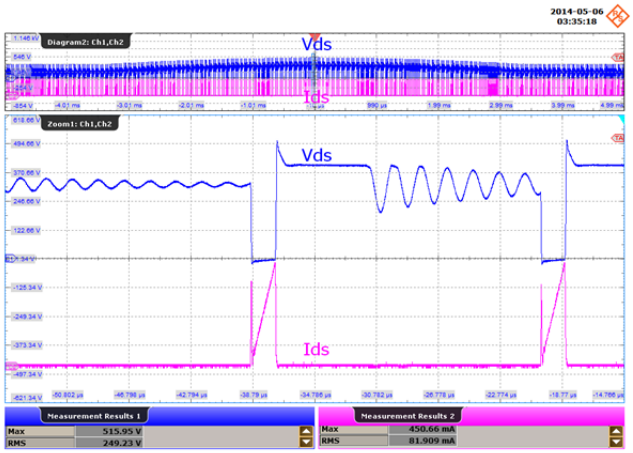

Figure 34 – 230 VAC, Full Load.
Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 2 µs / div.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 0.2 A / div., 1 ms / div.

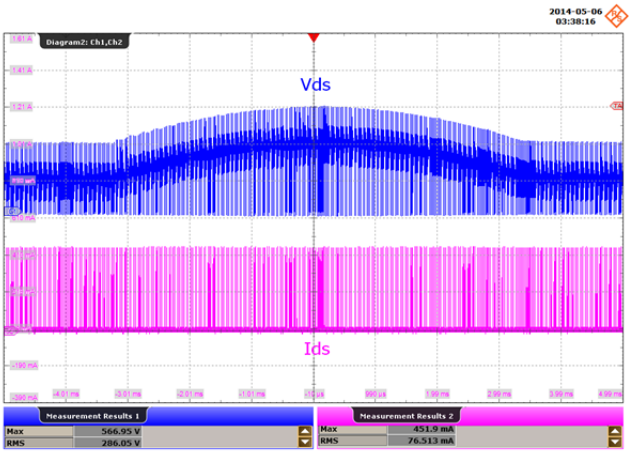

Figure 35 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 0.2 A / div., 1 ms / div.

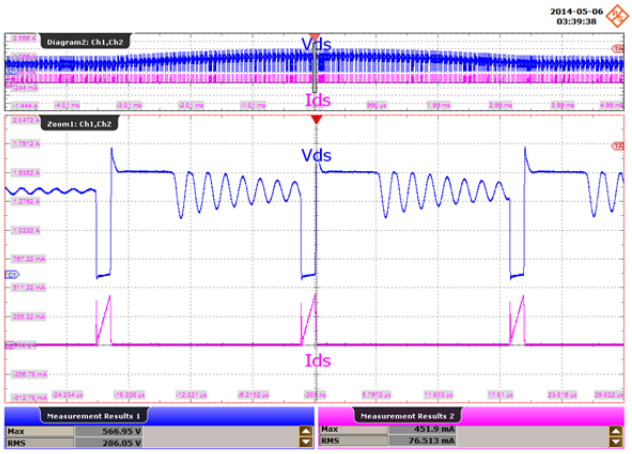

Figure 36 – 265 VAC, Full Load.
Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 5 µs / div.
Upper: V_{DRAIN}, 200 V.
Lower: I_{DRAIN}, 0.2 A / div.

10.3 Drain Voltage and Current Start-up Profile

No saturation or any possible cause of failure.

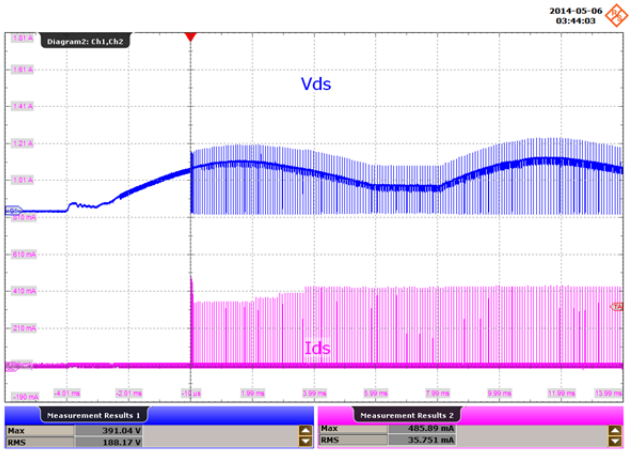

Figure 37 – 190 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.
Time Scale: 2 ms / div.

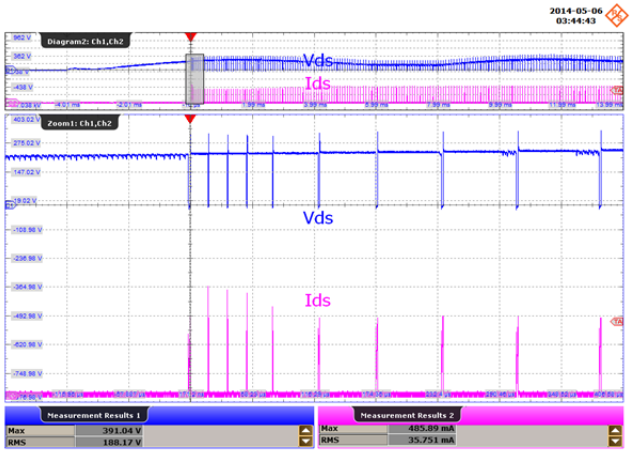

Figure 38 – 190 VAC Input and Full Load.
Upper Frame: Normal Sample; 2 ms / div.
Lower Frame: Zoom Center; 5 µs / div.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.

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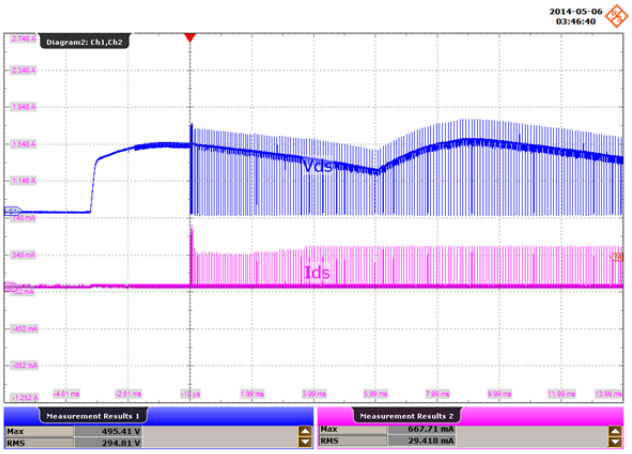

Figure 39 – 265 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.4 A / div.
Time Scale: 2 ms / div.

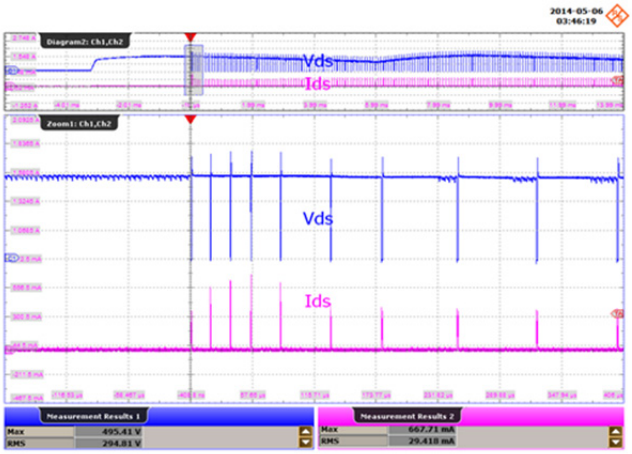

Figure 40 – 265 VAC Input and Full Load.
Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 2 μs / div.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.4 A / div.

10.4 Drain Voltage and Current Start-up Short Waveform

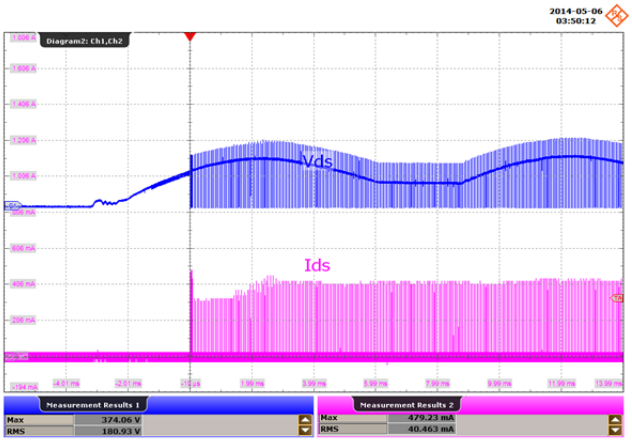

Figure 41 – 190 VAC Input and Shorted Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.
Time Scale: 2 ms / div.

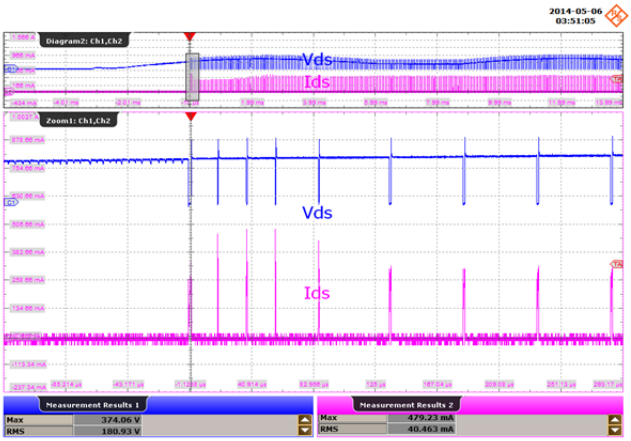

Figure 42 – 190 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 2 ms / div.
Lower Frame: Zoom Center; 40 µs / div.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.

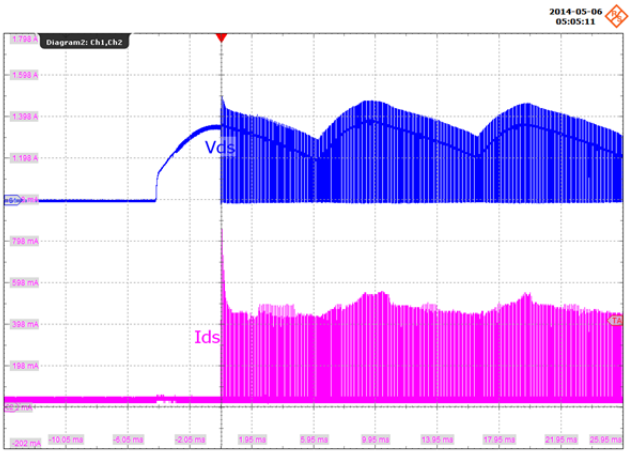

Figure 43 – 265 VAC Input and Shorted Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.
Time Scale: 4 ms / div.

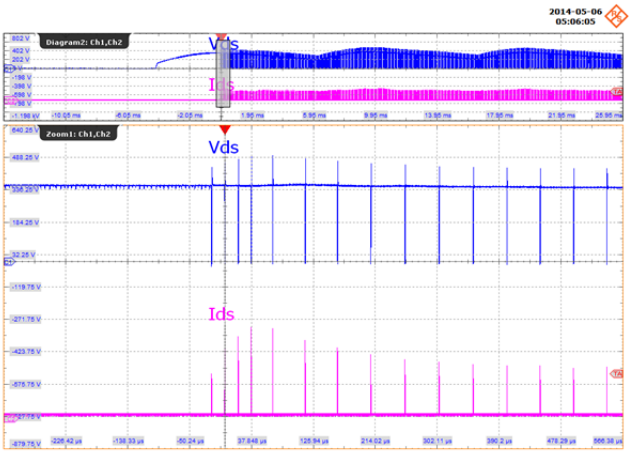

Figure 44 – 265 VAC Input and Shorted Load.
Upper Frame: Normal sample; 4 ms / div.
Lower Frame: Zoom Center; 88 µs / div.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.4 A / div.

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10.5 Drain Voltage and Current Normal Running Short Waveform

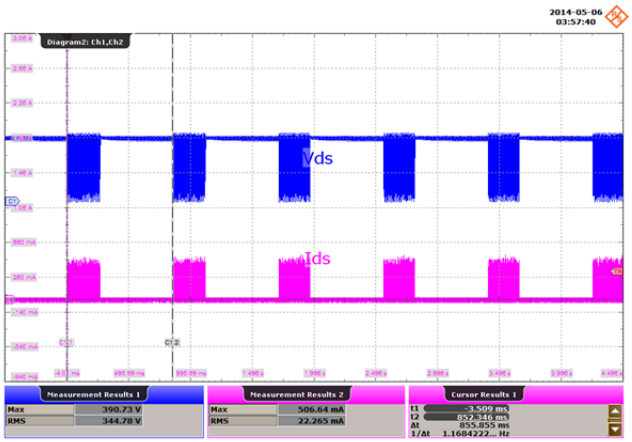

Figure 45 – 265 VAC Input, Full Load then Short. 266 ms Continuous Switching.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.4 A / div.
Time Scale: 500 ms / div.

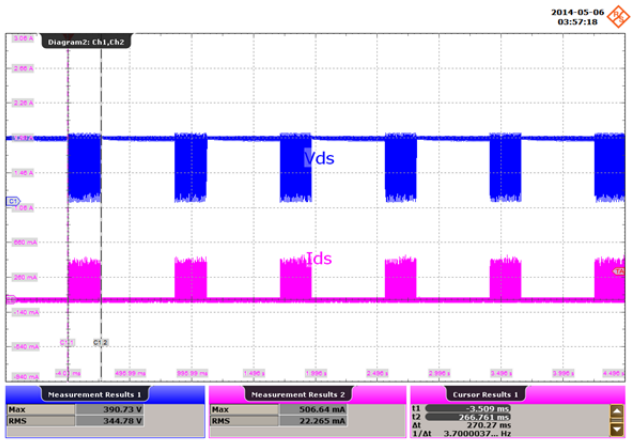

Figure 46 – 265 VAC Input, Full Load then Short.
850 ms Off Time between Auto-Restarts.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.4 A / div.
Time Scale: 500 ms / div.

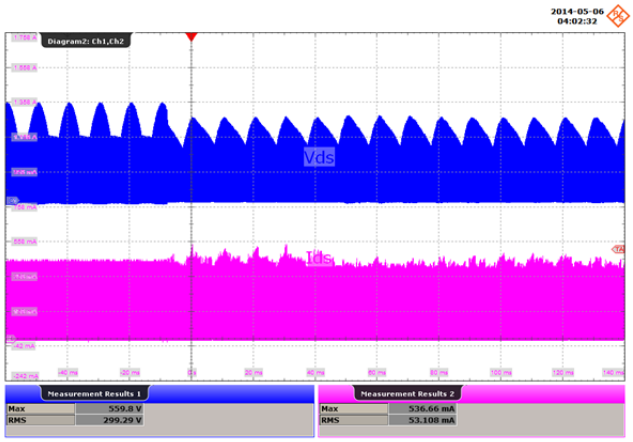

Figure 47 – 265 VAC Input, Full Load then Short.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.
Time Scale: 20 ms / div.

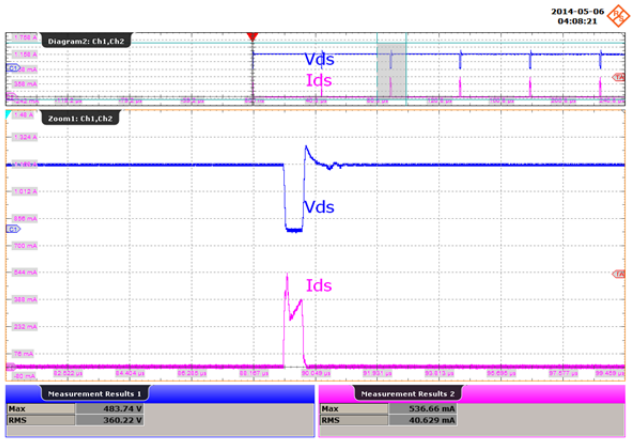

Figure 48 – 265 VAC Input, Full Load then Short.
Upper Frame: Normal Sample; 40 µs / div.
Lower Frame: Zoom Center; 12 µs / div.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div.

10.6 Output Diode Waveforms at Normal Operation

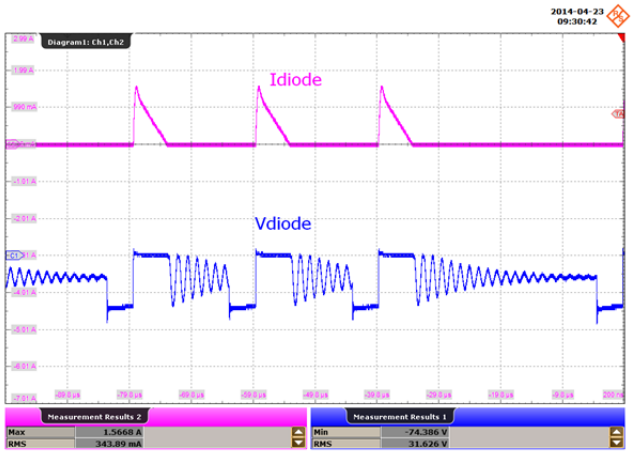

Figure 49 – 190 VAC Input, Normal Operation.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DIODE}, 40 V / div.
Time Scale: 10 μs / div.

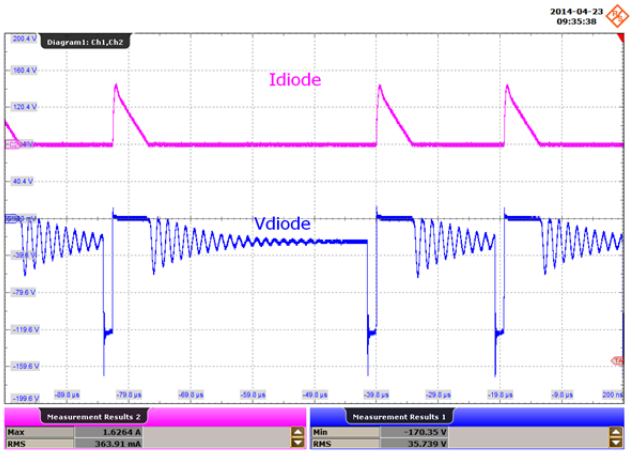

Figure 50 – 265 VAC Input, Normal Operation.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DIODE}, 40 V / div.
Time Scale: 10 μs / div.

10.7 Output Diode Waveforms at Start-up

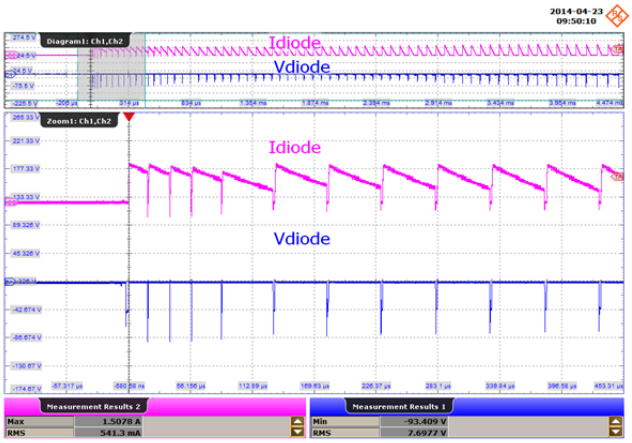

Figure 51 – 190 VAC Input, Start-up.
Upper Frame: Normal Sample; 520 μs / div.
Lower Frame:Zoom; 56 μs / div.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DIODE}, 50 V / div.

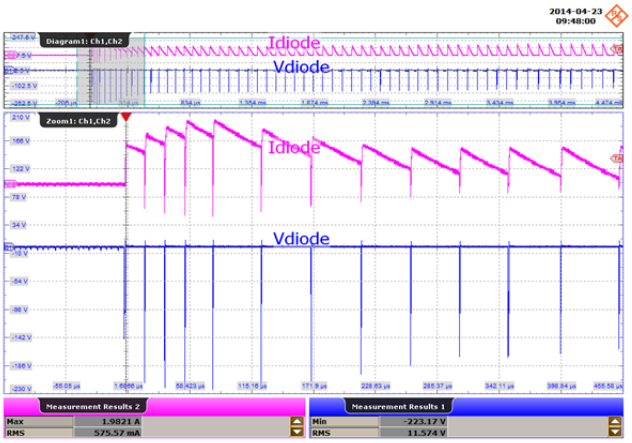

Figure 52 – 265 VAC Input, Normal Operation.
Upper Frame: Normal Sample; 520 μs / div.
Lower Frame: Zoom; 56 μs / div.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DIODE}, 50 V / div.

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10.8 Diode Start-up Short Waveforms

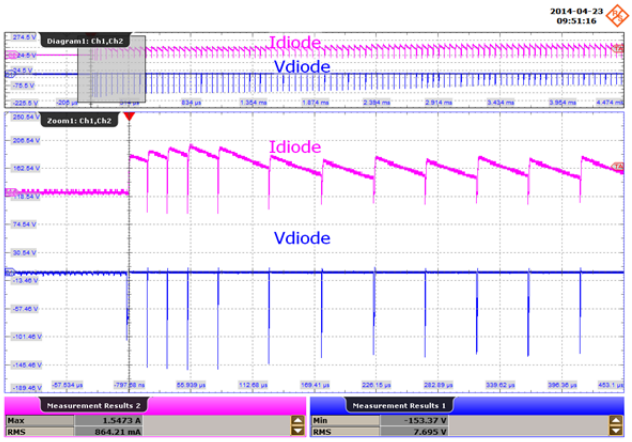

Figure 53 – 190 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 520 µs / div.
Lower Frame: Zoom; 56 µs / div.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DIODE}, 50 V / div.

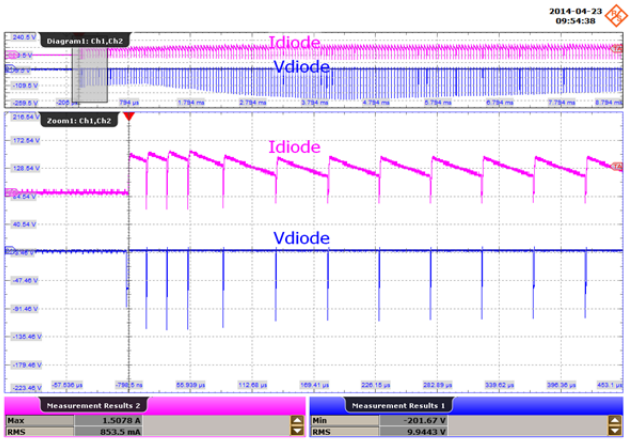

Figure 54 – 265 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 520 µs / div.
Lower Frame: Zoom; 56 µs / div.
Upper: I_{DIODE}, 1 A / div.
Lower: V_{DRAIN}, 50 V / div.

10.1 Output Diode Normal Running Short Waveforms

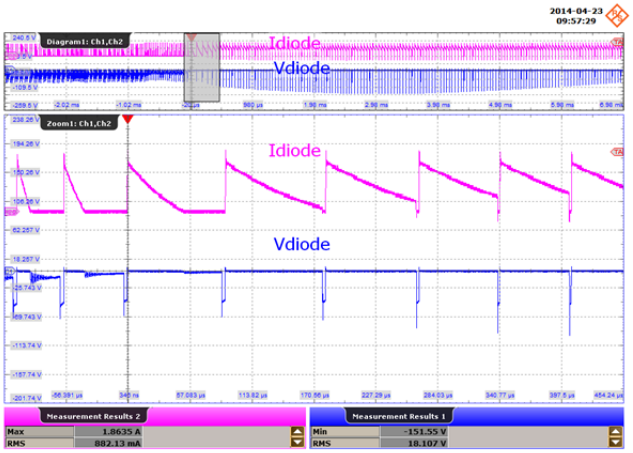

Figure 55 – 190 VAC Input and Shorted Load. Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 56 µs / div.
Upper: I_{DIODE}, 1 A / div.
Lower: $V_{AK-DIODE}$, 50 V / div.

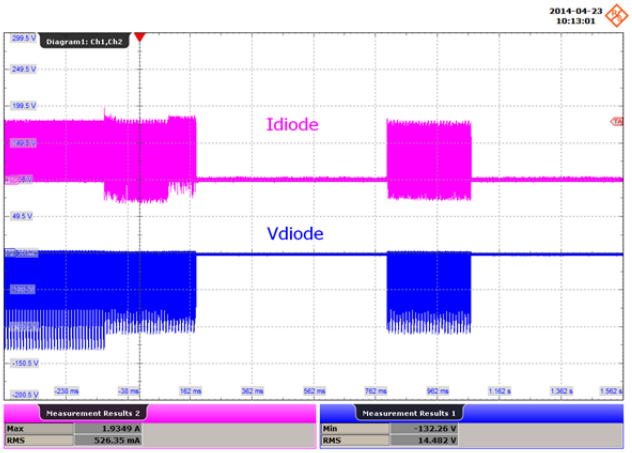

Figure 56 – 265 VAC Input and Shorted Load.
Upper: I_{DIODE}, 1 A / div.
Lower: $V_{AK-DIODE}$, 50 V / div.
Time Scale: 200 ms / div.

10.2 Output Voltage Start-up Profile

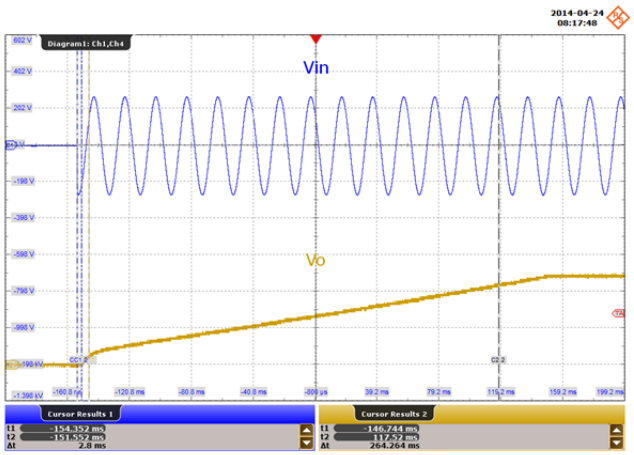

Figure 57 – Start-up Profile, 190 VAC.
Upper: V_{IN}, 200 V / div.
Lower: V_{OUT}, 10 V / div.
Time Scale: 40 ms / div.

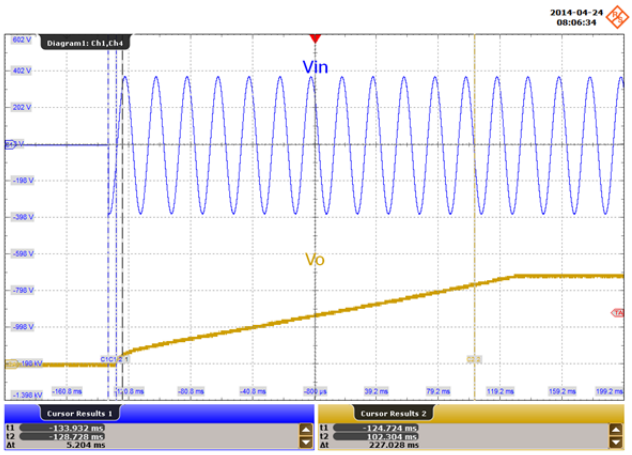

Figure 58 – Start-up Profile, 265 VAC.
Upper: V_{IN}, 200 V / div.
Lower: V_{OUT}, 10 V / div.
Time Scale: 40 ms / div.

10.1 Output Voltage and Output Current at Normal Operation

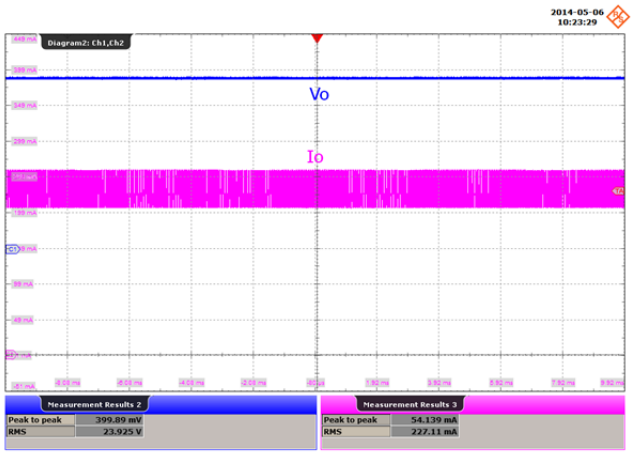

Figure 59 – V_{OUT} and I_{OUT}, 190 VAC.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 50 mA / div.
Time Scale: 2 ms / div.

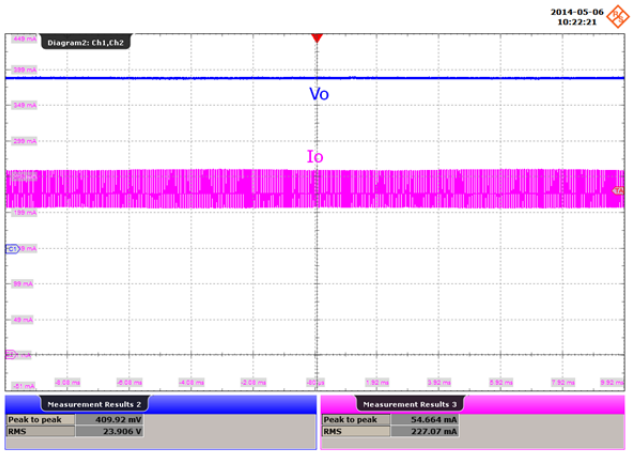

Figure 60 – V_{OUT} and I_{OUT}, 230 VAC.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 50 mA / div.
Time Scale: 2 ms / div.

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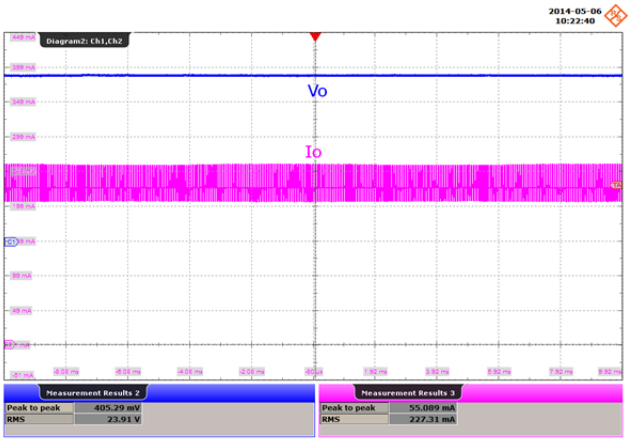

Figure 61 – V_{OUT} and I_{OUT}, 265 VAC.
Upper: V_{OUT}, 5 V / div.
Lower: I_{OUT}, 50 mA / div.
Time Scale: 2 ms / div.

10.2 Load Transient Response (0% to 100% and from 50% to 100% Load Step)

In the figures shown below, both AC coupling and DC coupling for the V_{OUT} waveforms are shown.

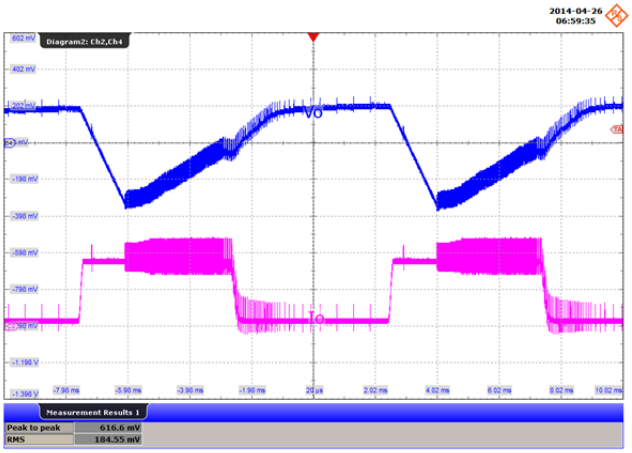

Figure 62 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 100 Hz.
Upper: V_{OUT}, 200 mV / div. AC Coupling.
Lower: I_{OUT}, 100 mA / div.
Time Scale: 2 ms / div.

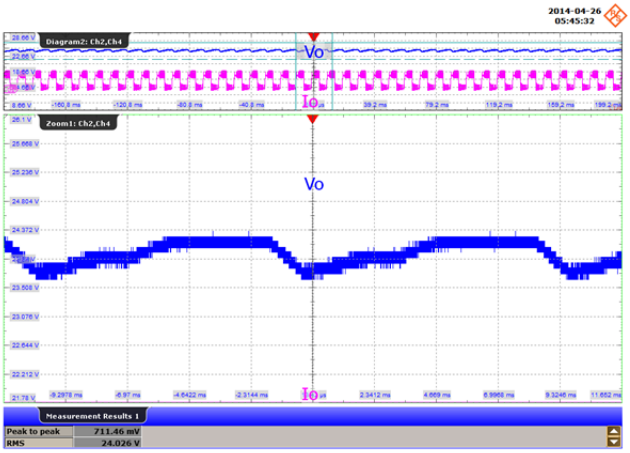

Figure 63 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 100 Hz.

Upper Frame: Normal Sample; 40 ms / div.
Upper: V_{OUT}, 2 V / div. DC Coupling.
Lower: I_{OUT}, 100 mA / div.

Lower Frame: Zoom Center; 2 ms / div.
Center: V_{OUT}, 2 V / div. DC Coupling.

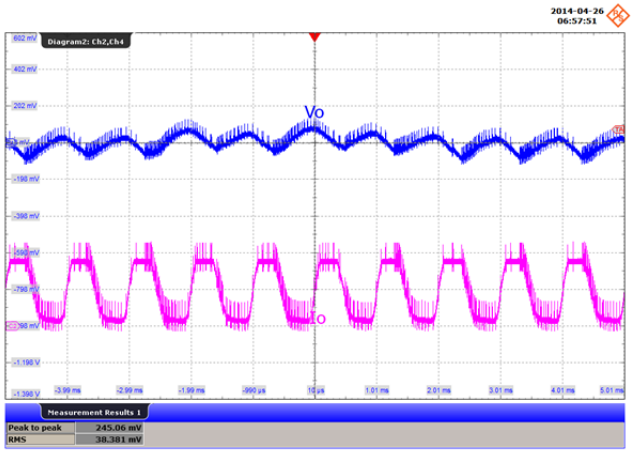

Figure 64 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.
Upper: V_{OUT}, 200 mV / div. AC Coupling.
Lower: I_{OUT}, 100 mA / div.
Time Scale: 1 ms / div.

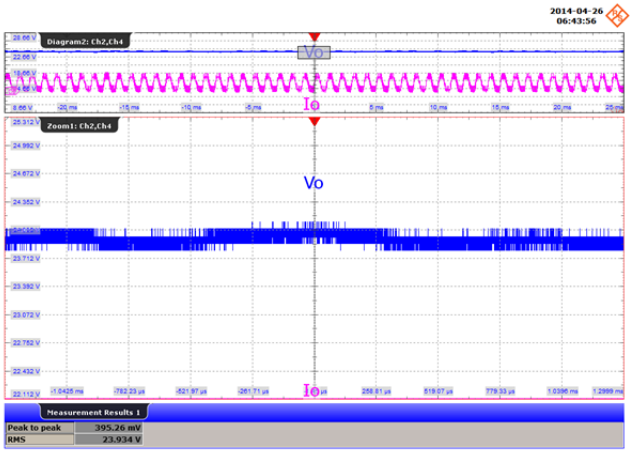

Figure 65 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.

Upper Frame: Normal Sample; 5 ms / div.
Upper: V_{OUT}, 2 V / div. DC Coupling.
Lower: I_{OUT}, 100 mA / div.

Lower Frame: Zoom Center; 2 ms / div.
Center: V_{OUT}, 2 V / div. DC Coupling.

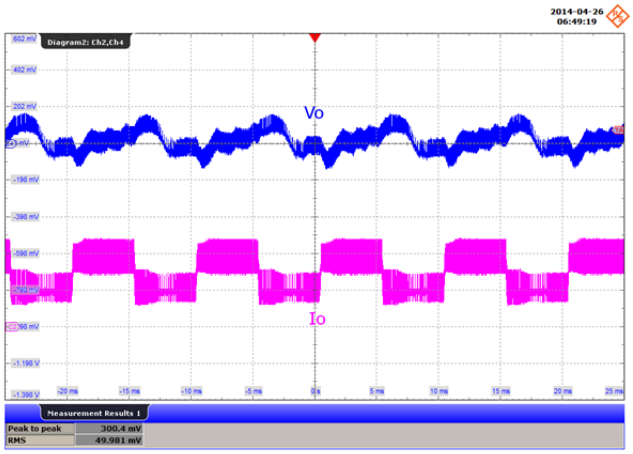

Figure 66 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 100 Hz.
Upper: V_{OUT}, 200 mV / div. AC Coupling.
Lower: I_{OUT}, 100 mA / div.
Time Scale: 5 ms / div.

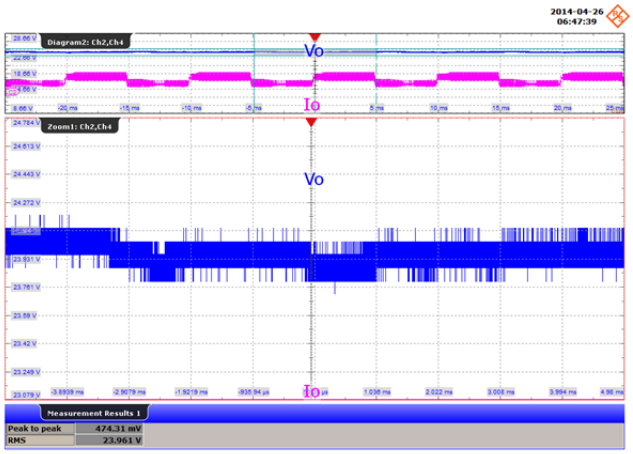

Figure 67 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 100 Hz.

Upper Frame: Normal Sample; 5 ms / div.
Upper: V_{OUT}, 2 V / div. DC Coupling.
Lower: I_{OUT}, 100 mA / div.

Lower Frame: Zoom Center; 2 ms / div.
Center: V_{OUT}, 2 V / div. DC Coupling.

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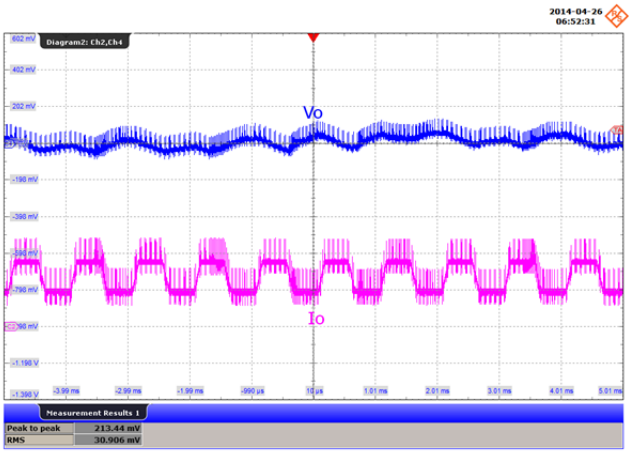

Figure 68 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 1 kHz.
Upper: V_{OUT}, 200 mV / div. AC Coupling.
Lower: I_{OUT}, 100 mA / div.
Time Scale: 1 ms / div.

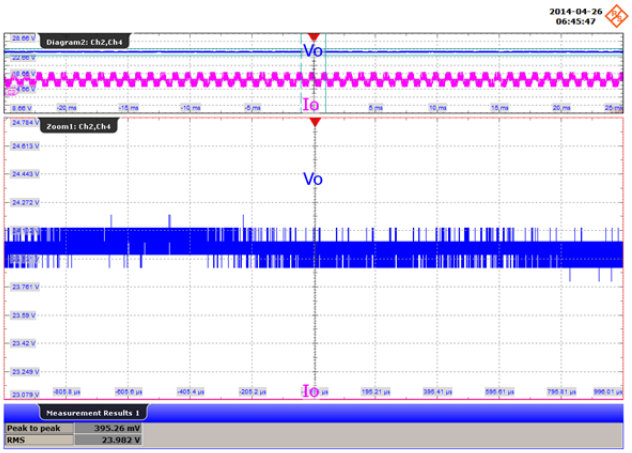

Figure 69 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 1 kHz.

Upper Frame: Normal Sample; 5 ms / div.
Upper: V_{OUT}, 2 V / div. DC Coupling.
Lower: I_{OUT}, 100 mA / div.

Lower Frame: Zoom Center; 2 ms / div.
Center: V_{OUT}, 2 V / div. DC Coupling.

10.3 Brown-out Test

No component failure was observed.

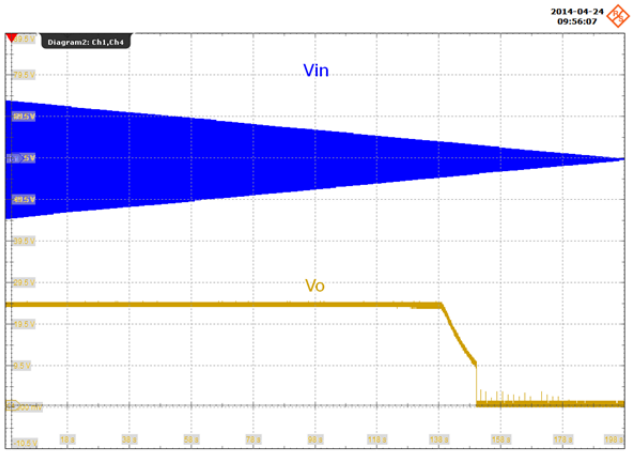

Figure 70 – Brown-out. V_{IN} Decrements at 1 V / s.
Upper: V_{IN}, 200 V / div.
Lower: V_{OUT}, 10 V / div.
Time Scale: 20 s / div.

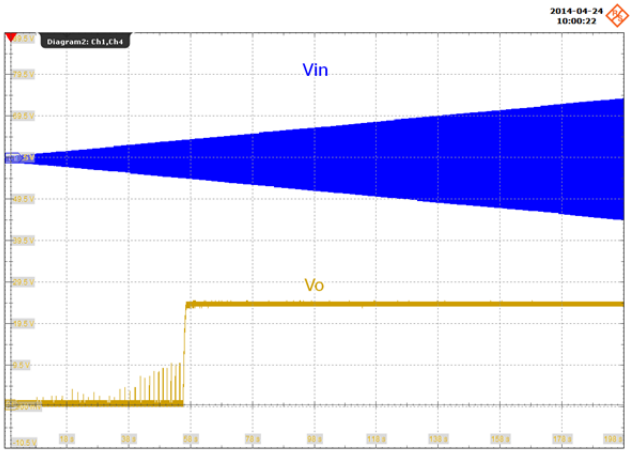

Figure 71 – Brown-in. V_{IN} Increments by 1 V / s.
Upper: V_{IN}, 200 V / div.
Lower: V_{OUT}, 10 V / div.
Time Scale: 20 s / div.

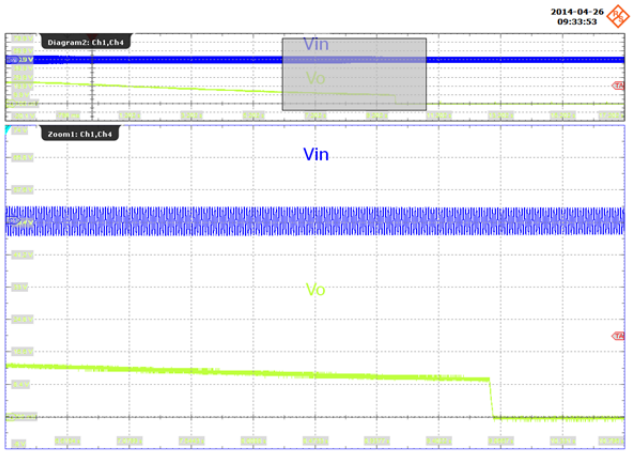

Figure 72 – Brown-out at 1 V / s.
Blue: V_{IN}, 200 V / div.
Yellow: V_{OUT}, 10 V / div.
Time Scale: 2 s / div.
Zoom Time Scale: 1.5 s / div.

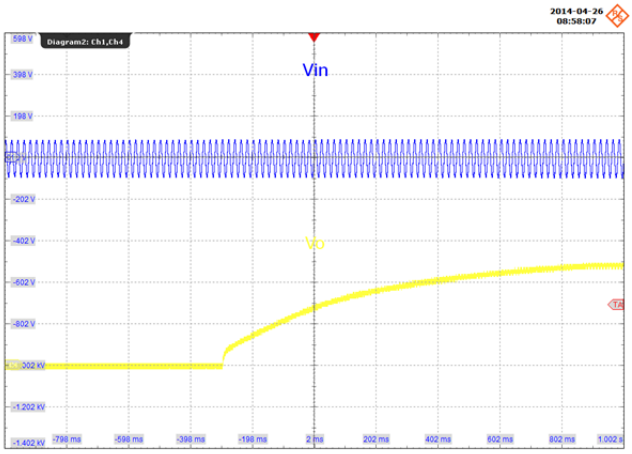

Figure 73 – Brown-in at 1 V / s.
Upper: V_{IN}, 200 V / div.
Lower: V_{OUT}, 10 V / div.
Time Scale: 200 ms / div.

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10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to noise pickup. Details of the probe modification are provided in the figures below.

To minimize the loop area between the probe (+) and its ground, a short probe is used as shown in the figures below. This is done by wrapping the grounding of the probe with wire and using it, instead, of the usual probe ground wire.

Two capacitors in parallel are utilized to ensure that ripple measurements will not vary from one setup to another. This reduces noise pick from the sets of equipment during testing. One (1) 0.1 μF/50 V ceramic type, preferably, a thru hole type(not shown) and one (1) 1.0 μF/50 V aluminum electrolytic are used as shown. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). The oscilloscope is set to 20 Mhz bandwidth during measurements.

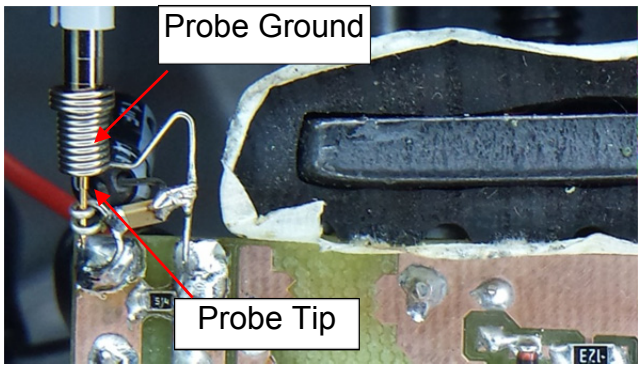

Figure 74 – Oscilloscope Probe Prepared for Ripple Measurement. (Probe Cap and Ground Lead Removed)

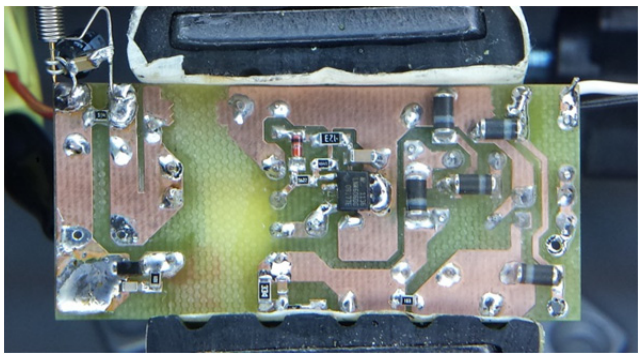

Figure 75 – Ripple Measurement Set-up.

10.4.2 Ripple and Noise Measurement Results

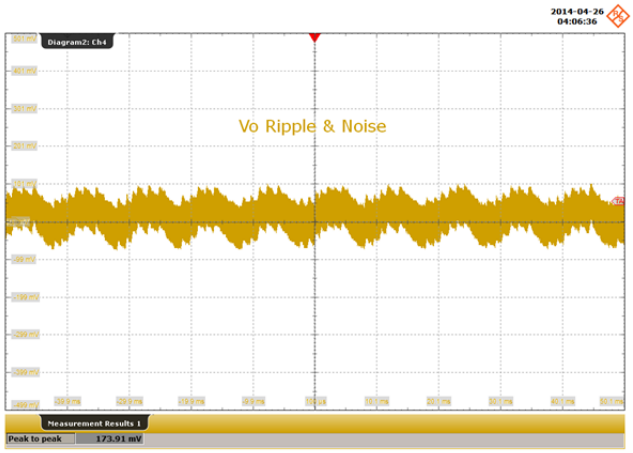

Figure 76 – Ripple, 190 VAC, Full Load.
10 ms / div., 100 mV / div.

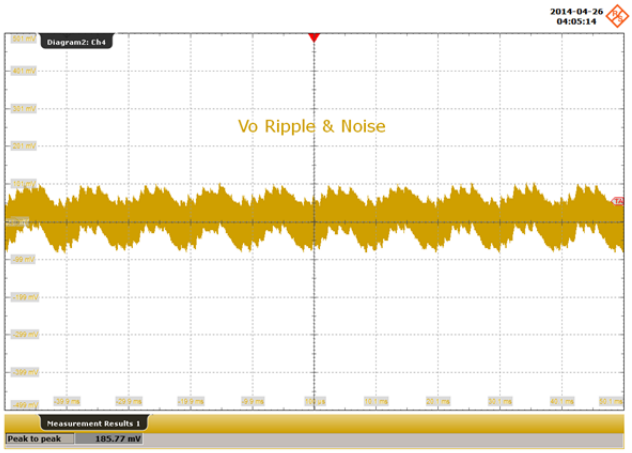

Figure 77 – Ripple, 265 VAC, Full Load.
10 ms, 100 mV / div.

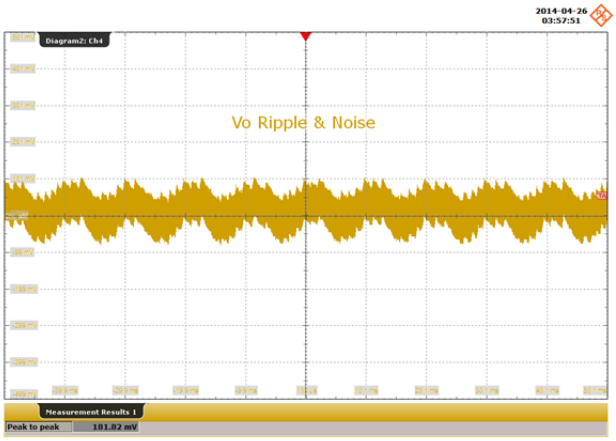

Figure 78 – Ripple, 230 VAC, Full Load.
10 ms, 100 mV / div.

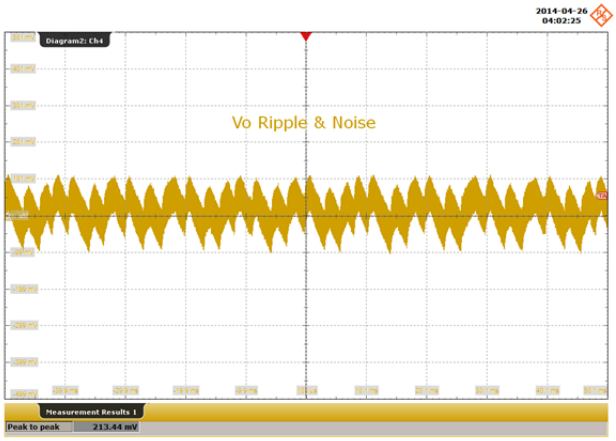

Figure 79 – Ripple, 230 VAC, 75% of Full Load.
5 ms, 100 mV / div.

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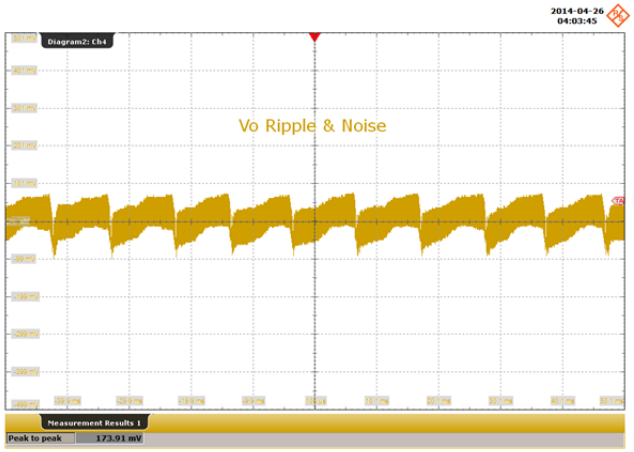

Figure 80 – Ripple, 230 VAC, 50% of Full Load.
10 ms, 100 mV / div.

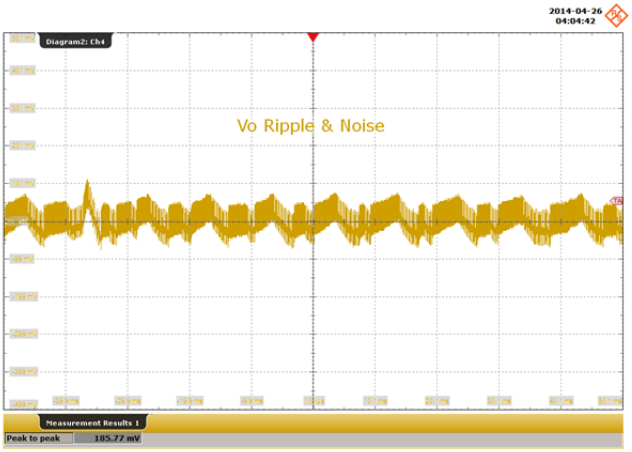

Figure 81 – Ripple, 230 VAC, 25% of Full Load.
10 ms, 100 mV / div.

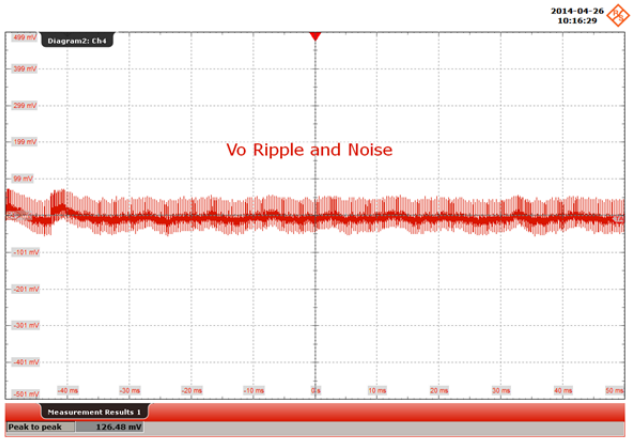

Figure 82 – Ripple, 230 VAC, 12.5% of Full Load.
10 ms, 100 mV / div.

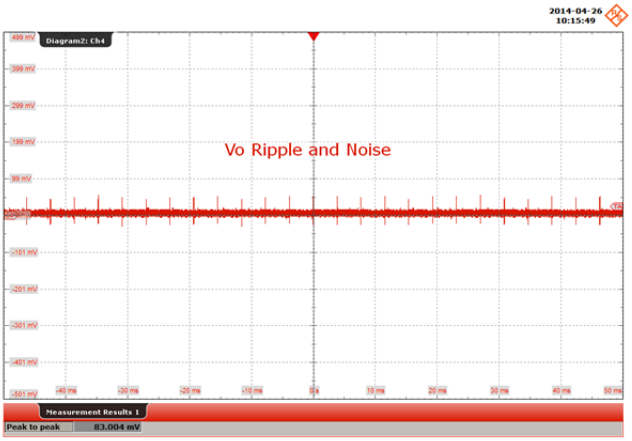

Figure 83 – Ripple, 230 VAC, No-Load.
10 ms, 100 mV / div.

12 Line Surge

Differential Ring input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	90	Pass
-25000	230	L to N	90	Pass
+2500	230	L to N	0	Pass
-25000	230	L to N	0	Pass

Unit passes under all test conditions.

Differential input line 1.2/50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+250	230	L to N	90	Pass
-250	230	L to N	90	Pass
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass
+750	230	L to N	90	Pass
-750	230	L to N	90	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

Unit passes under all test conditions.

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12.1 Surge Waveforms

12.1.1 Ring Wave Surge

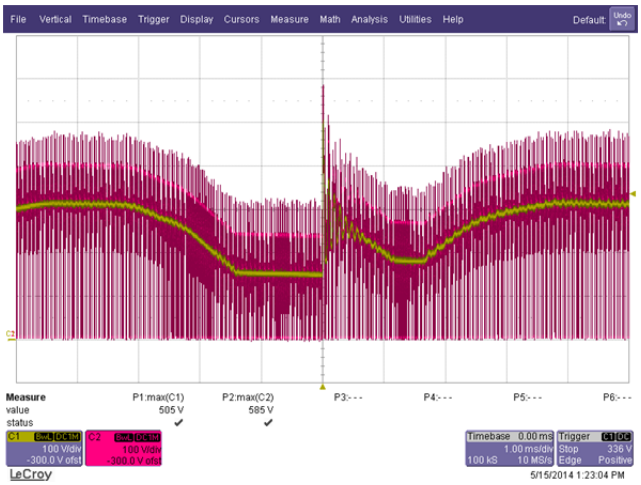

Figure 84 – Ring Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

Figure 85 – Ring Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 50 μs / div.

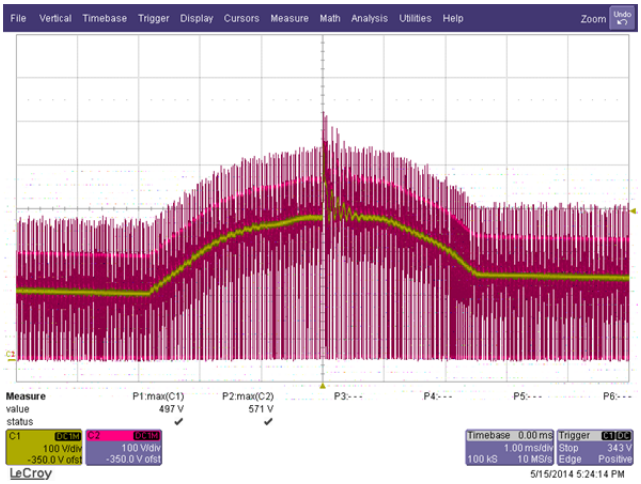

Figure 86 – Ring Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

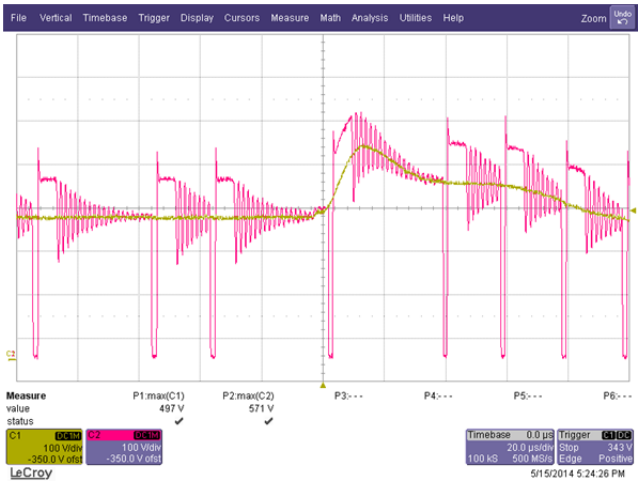

Figure 87 – Ring Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 50 μs / div.

12.1.2 Differential Surge

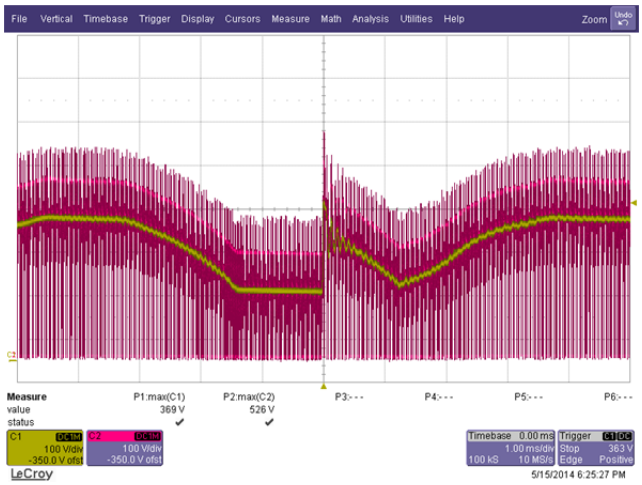

Figure 88 – Differential Surge of 2.5 kV,
230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

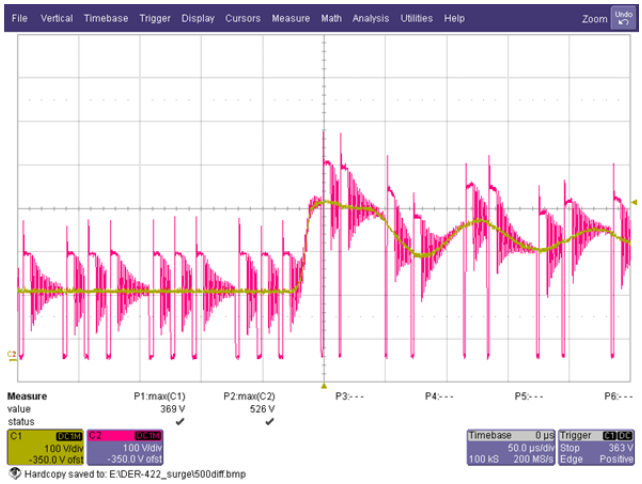

Figure 89 – Differential Surge of 2.5 kV,
230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

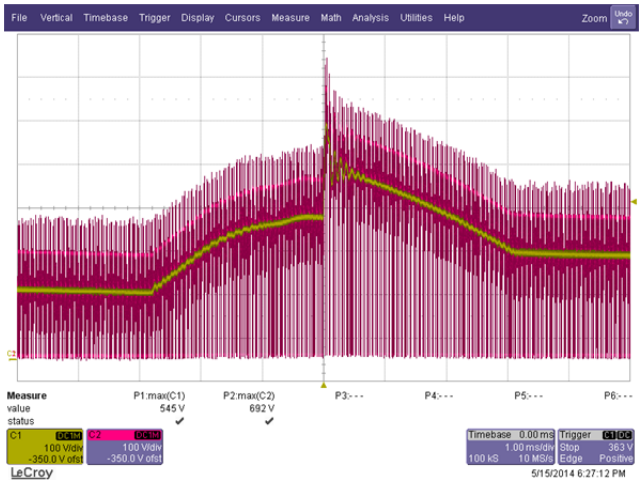

Figure 90 – Differential Surge of 2.5 kV,
230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

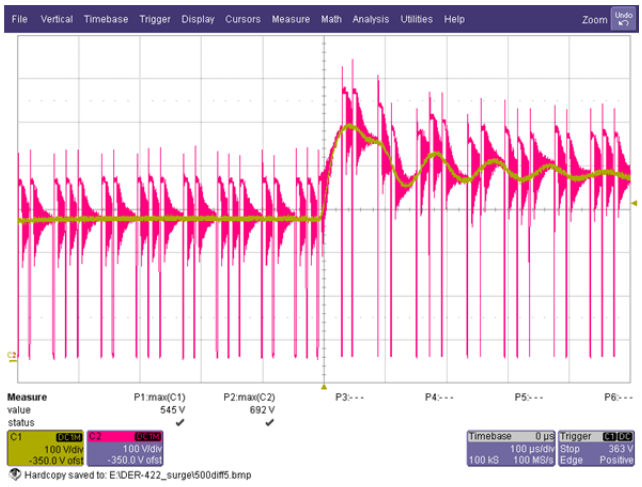

Figure 91 – Differential Surge of 2.5 kV,
230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

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13 Conducted EMI

Figure 92 – Conducted EMI Set-up.

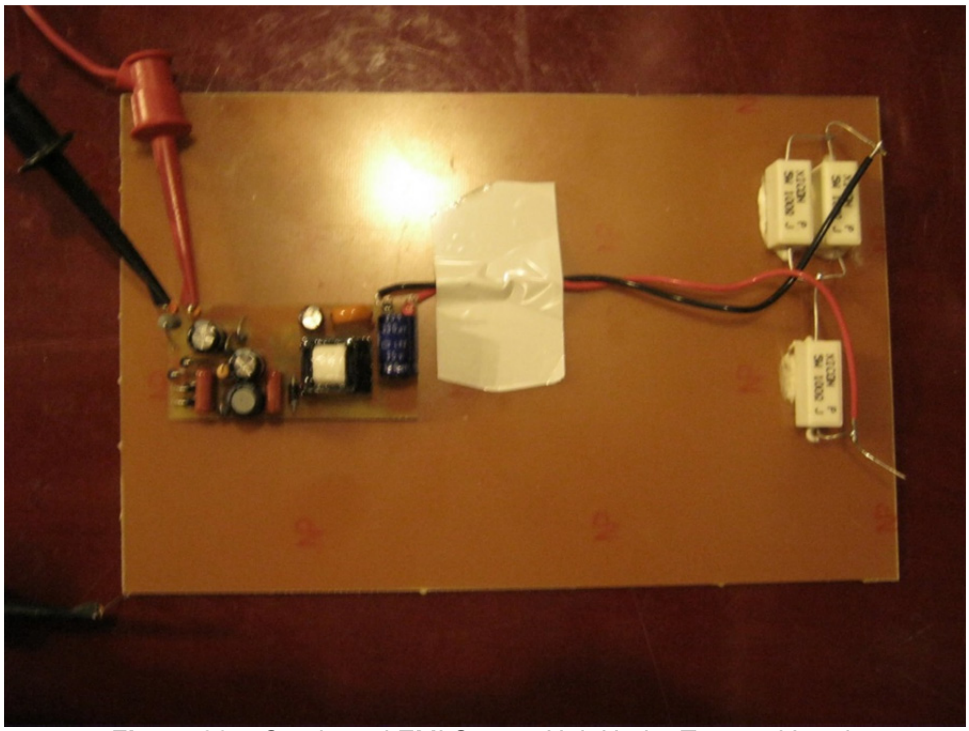

Figure 93 – Conducted EMI Set-up. Unit Under Test and Load.

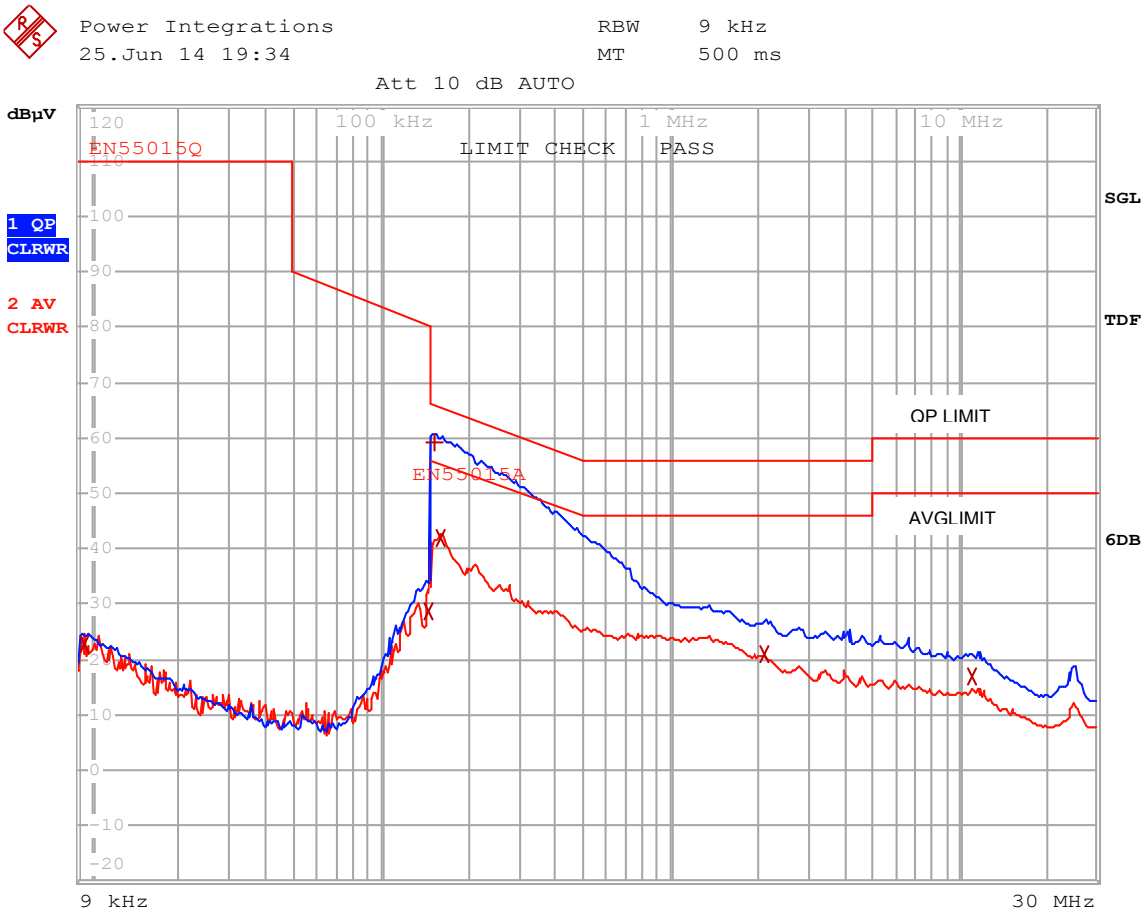

Figure 94 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). UUT is Floating (Ungrounded and Not on the Metal Plane).

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.36543609 kHz	22.67	L1 gnd	
2	Average	144.512626646 kHz	28.69	L1 gnd	
1	Quasi Peak	153.015 kHz	59.30	L1 gnd	-6.53
2	Average	160.820302816 kHz	41.89	L1 gnd	-13.52
2	Average	2.11629733595 MHz	21.06	N gnd	-24.93
2	Average	11.0388729048 MHz	17.04	N gnd	-32.95

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Table 4 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. UUT is Floating (Ungrounded and Not on the Metal Plane).

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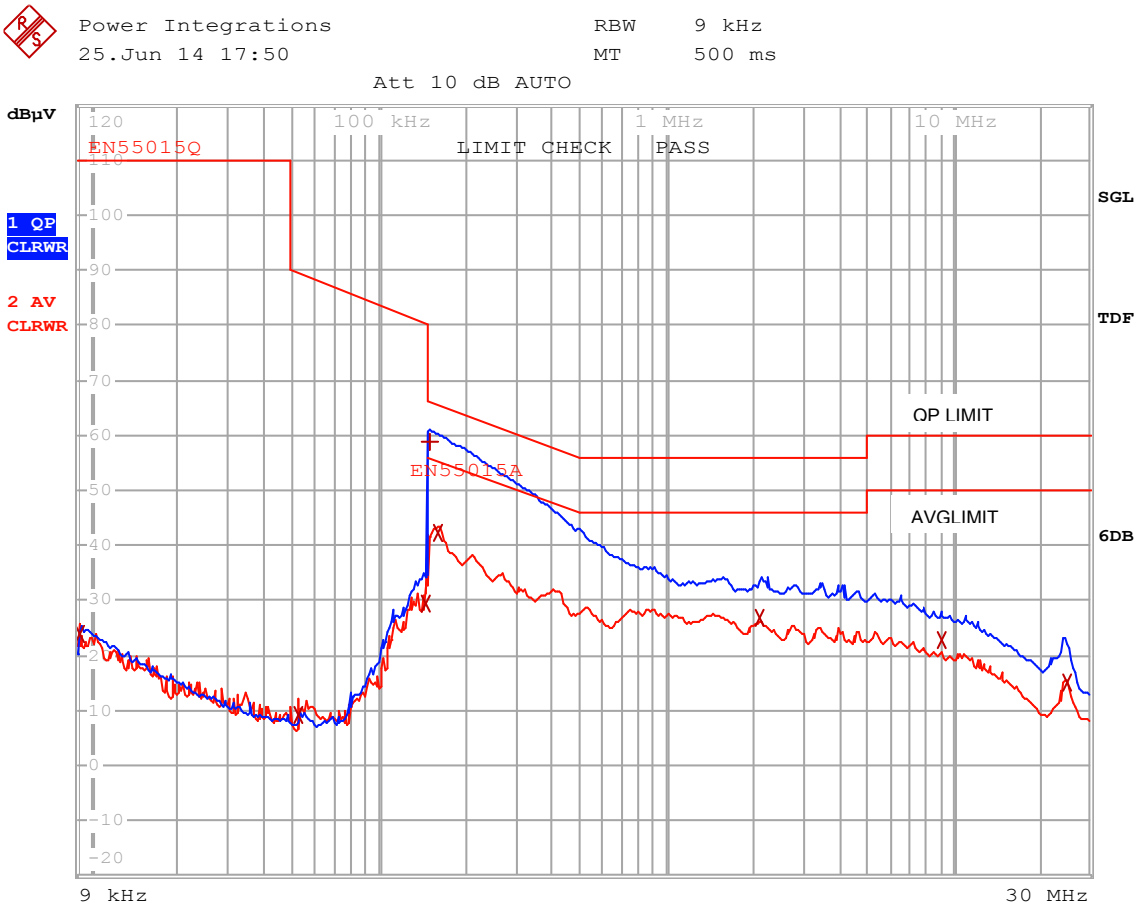

Figure 95 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). Unit is on Top of Ungrounded Copper Plane.

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.09 kHz	23.94	L1 gnd	
2	Average	52.3751969359 kHz	9.25	L1 gnd	
2	Average	144.512626646 kHz	29.38	N gnd	
1	Quasi Peak	151.5 kHz	58.93	N gnd	-6.98
2	Average	160.820302816 kHz	42.45	L1 gnd	-12.96
2	Average	2.11629733595 MHz	26.93	N gnd	-19.06
2	Average	9.13731572038 MHz	22.71	N gnd	-27.28
2	Average	24.9618853035 MHz	15.11	L1 gnd	-34.89

Table 5 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit is on Top of Ungrounded Copper Plane.

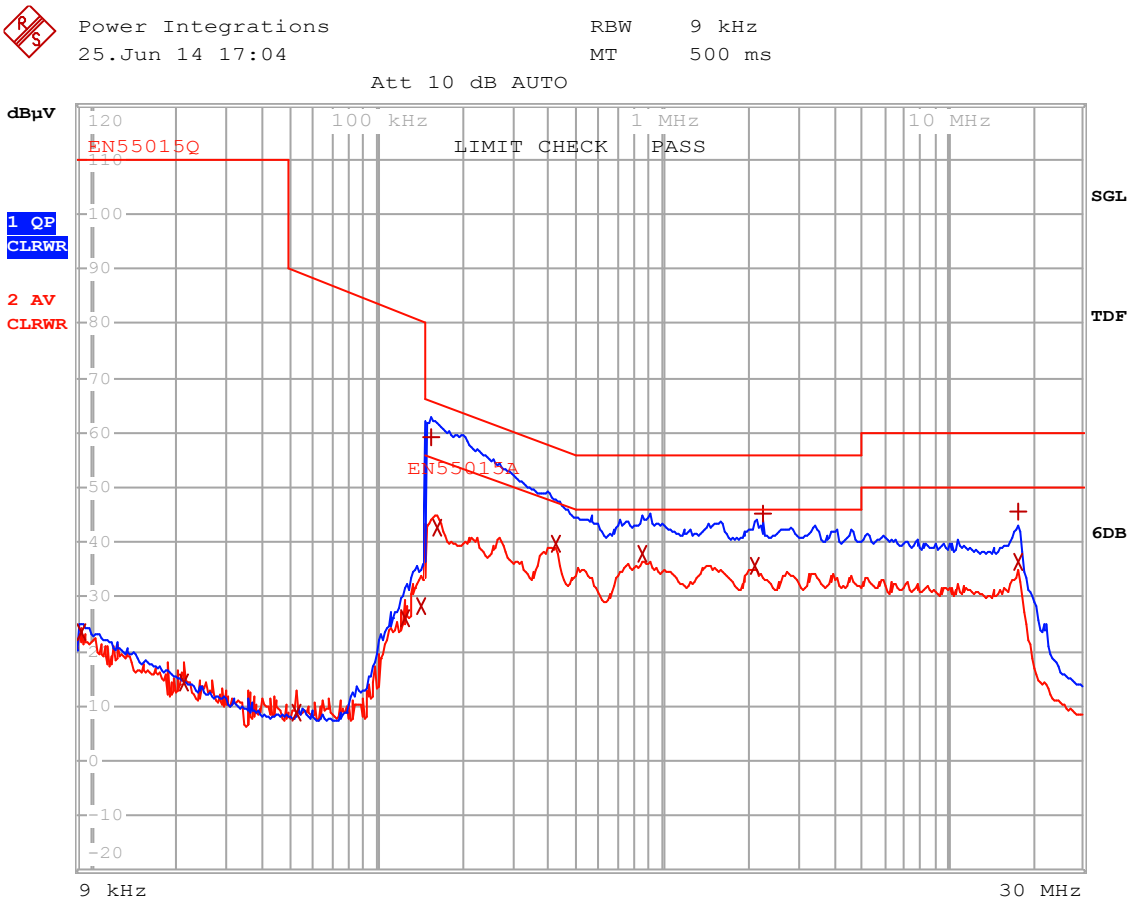

Figure 96 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). Unit is on Top of Grounded Copper Plane.

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.1809 kHz	23.66	L1 gnd	
2	Average	20.9681097433 kHz	14.26	L1 gnd	
2	Average	51.8566306296 kHz	8.96	L1 gnd	
2	Average	125.720633819 kHz	26.06	N gnd	
2	Average	143.081808561 kHz	28.28	L1 gnd	
1	Quasi Peak	156.0906015 kHz	59.06	L1 gnd	-6.60
2	Average	162.428505844 kHz	42.60	L1 gnd	-12.73
2	Average	422.19601758 kHz	39.53	N gnd	-7.87
2	Average	855.719977385 kHz	37.85	N gnd	-8.14
2	Average	2.11629733595 MHz	35.80	N gnd	-10.19
1	Quasi Peak	2.24649226677 MHz	45.06	N gnd	-10.93
1	Quasi Peak	17.6209492727 MHz	45.57	N gnd	-14.42
2	Average	17.6209492727 MHz	36.52	N gnd	-13.47

Table 6 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit is on Top of Grounded Copper Plane.

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
20-Aug-14	JdC	1.2	Initial Release	Apps & Mktg

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