Design Example Report

Title	***4.95 W Non-Dimmable, Non-Isolated Power Factor Corrected Tapped-Buck LED Driver Using LinkSwitch™-PL LNK457DG***
Specification	90 VAC – 132 VAC Input; 9 V, 550 mA Output
Application	GU10 LED Driver
Author	Applications Engineering Department
Document Number	DER-398
Date	December 5, 2013
Revision	1.0

Summary and Features

- Single-stage power factor corrected (0.9 at 115 VAC) with accurate constant current (CC) output
- Low cost, low component count and small PCB footprint
- Highly energy efficient, 81% at 120 VAC input
- Integrated protection and reliability features
  - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
  - No damage during brown-out conditions
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI

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Important Note:
This board is a non-isolated design. The engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document describes a power supply utilizing the LinkSwitch™-PL family (LNK457DG) in a highly compact tapped-buck topology.

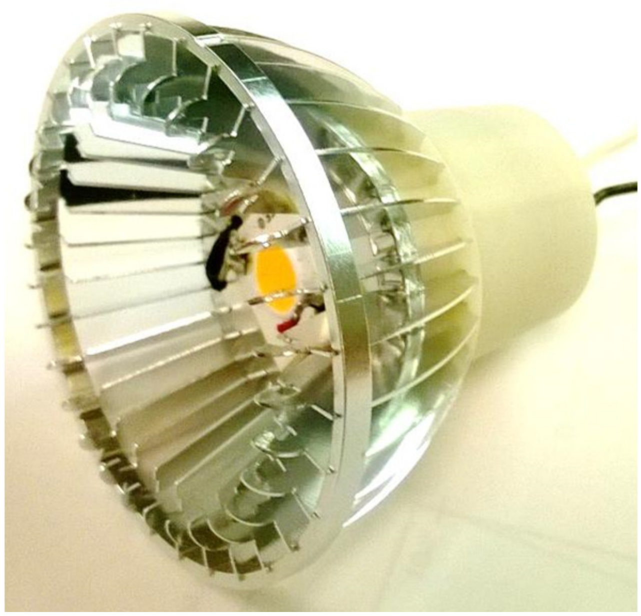

Figure 1 – GU10 Bulb from CREE.

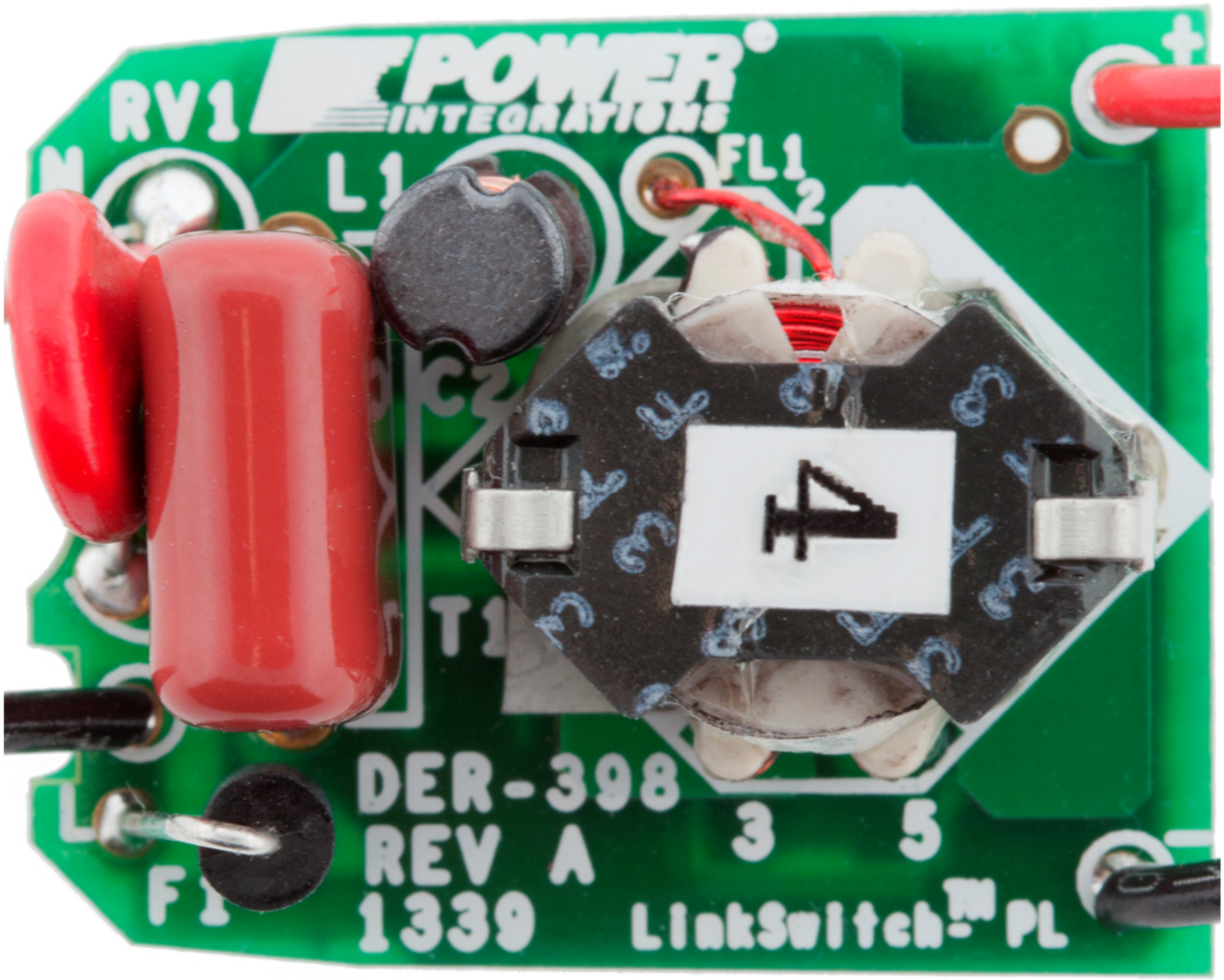

Figure 2 – Populated Circuit Board Photograph, Top.

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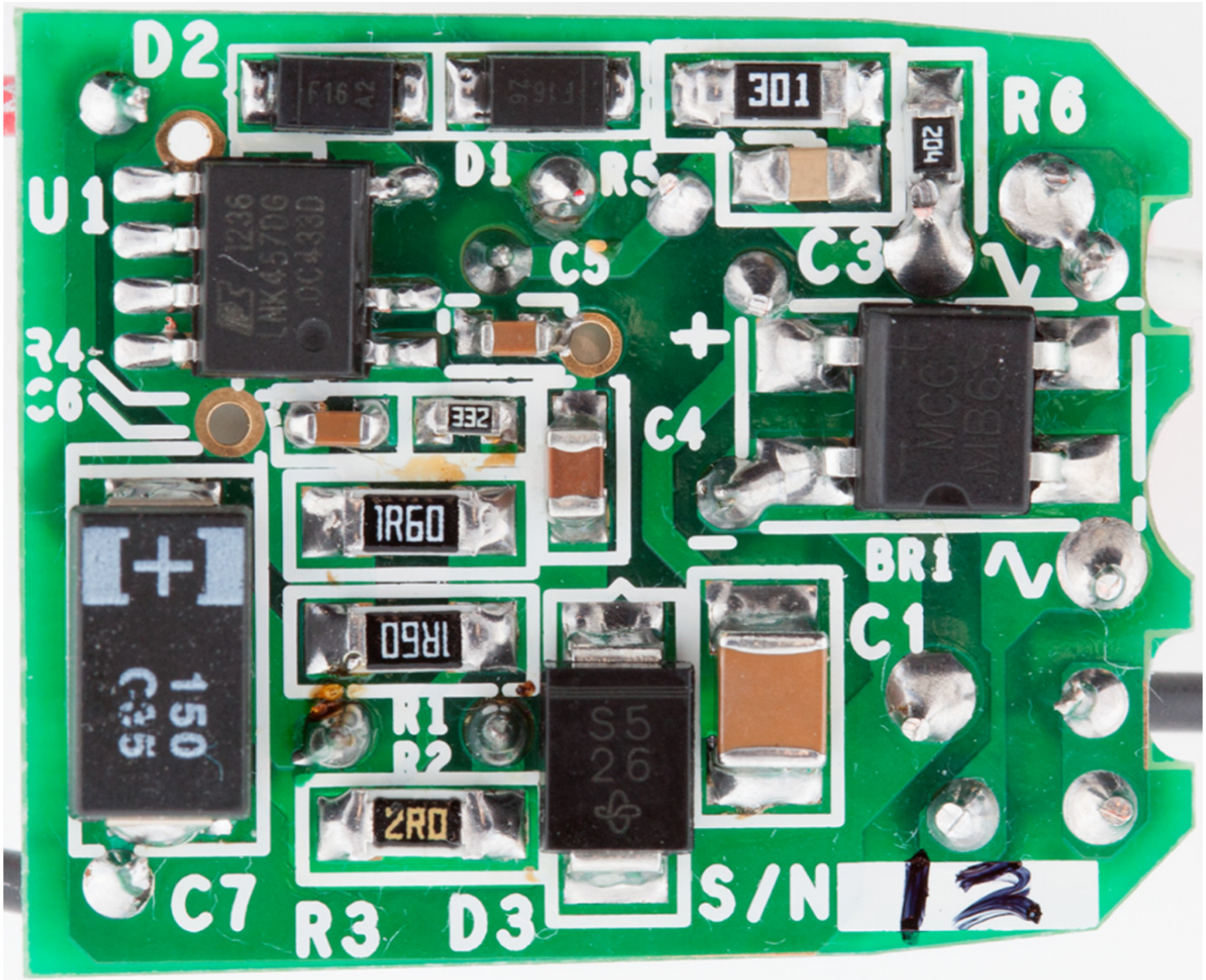

Figure 3 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage Operation	V_{IN}	90	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	60		Hz	
Output						
Output Voltage	V_{OUT}		9		V	
Output Current	I_{OUT}		550		mA	±5% at 90 VAC - 132 VAC
Total Output Power						
Continuous Output Power	P_{OUT}		4.95		W	
Efficiency						
115 VAC; 9 V LED	η		81		%	Measured at P_{OUT} 25 °C
Power Factor						
115 VAC; 9 V LED	PF		0.9			Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55015B				
Line Surge Differential Mode (L1-L2)			0.5		kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	500 A short circuit Series Impedance: Differential Mode: 2 Ω
Ambient Temperature	T_{AMB}			50	°C	See thermal results section

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3 Schematic

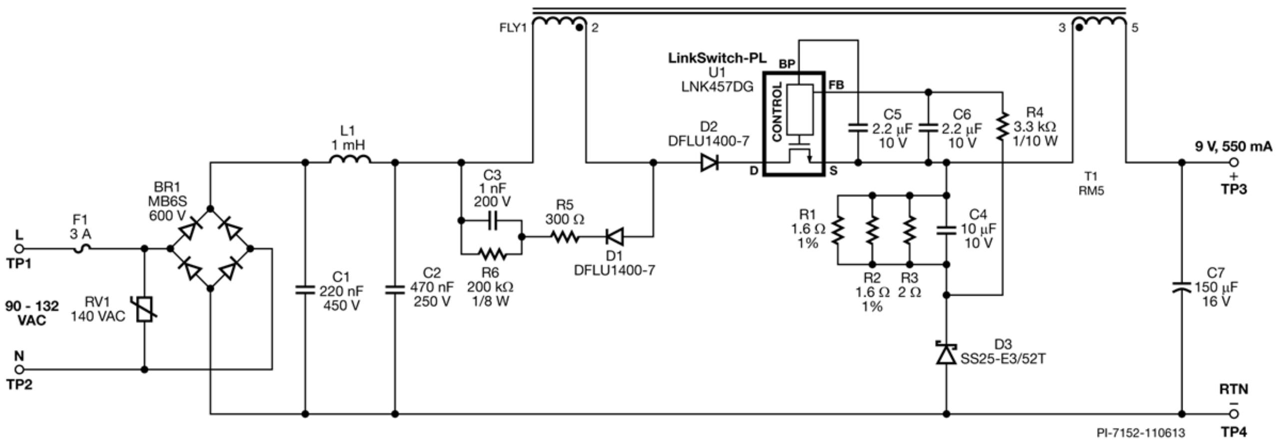

Figure 4 – Schematic.

4 Circuit Description

The power supply shown in Figure 4 uses the LNK457DG (U1) in a tapped-buck configuration to deliver a constant 550 mA current at an output voltage of 9 VDC.

4.1 Input EMI Filtering

Fuse F1 provides circuit protection for abnormal conditions. Bridge BR1 provides full wave rectification. Capacitor C1, C2 and differential choke L1 form a π filter in order meet conducted EMI standards. Capacitor C1 and C2 are also used for energy storage reducing line noise and protecting against line surge.

4.2 Power Circuit

The topology chosen in this design is a tapped-buck configured to provide low THD, high power factor, and constant current output for the input voltage range of 90 VAC to 132 VAC.

The tapped-buck converter was chosen to overcome the switch duty-cycle and peak current limitation inherent in low voltage designs. It also offers the advantage of reduced current stress on the main switch U1, and reduced voltage stress on the output diode D3. The reduced current stress on the main switch enables the use of a smaller switching device for more cost effective design. The lower voltage stress on the output diode enables the use of low V_F (schottky) device for improved efficiency.

Component T1 is the main inductor of the buck converter. It consists of two windings - primary and secondary. The ratio is chosen to be 4.44:1 (primary to secondary) to enable the use of a 50 V output diode while keeping the maximum voltage on U1 LNK457DG well below its maximum value. The inductance is chosen to keep the operation in discontinuous mode (DCM). DCM operation enables the driver to have high power factor and low THD.

Output Diode D3 conducts every time U1 is off and transfers energy to the load. Diode D2 is necessary to prevent reverse current from flowing through U1 while the voltage across C2 (rectified input AC) falls below the output voltage. A voltage clamp circuit was also added to damp the ringing caused by the leakage inductance of T1. The voltage clamp network is formed by diode D1, capacitor C3, and resistor R6. Resistor R5 is also added to limit the reverse current on through diode D1.

Capacitor C5 provides local decoupling for the BP pin of U1 which is the supply pin for the internal controller. During start-up, C5 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN pin. Once charged U1 starts switching.

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4.3 Output Feedback

Resistors R1, R2, and R3 are used to sense the buck converter diode current. Its value is adjusted to center the output current at 550 mA at nominal input voltage. Capacitor C4 is used to filter out the high frequency component of the diode current which helps improve overall efficiency. Resistor R4 and capacitor C6 provide additional filtering to lower the ripple voltage feed to the FEEDBACK (FB) pin of U1 for improved regulation.

4.4 No Open-Load Protection

The unit has no open load protection.

5 PCB Layout

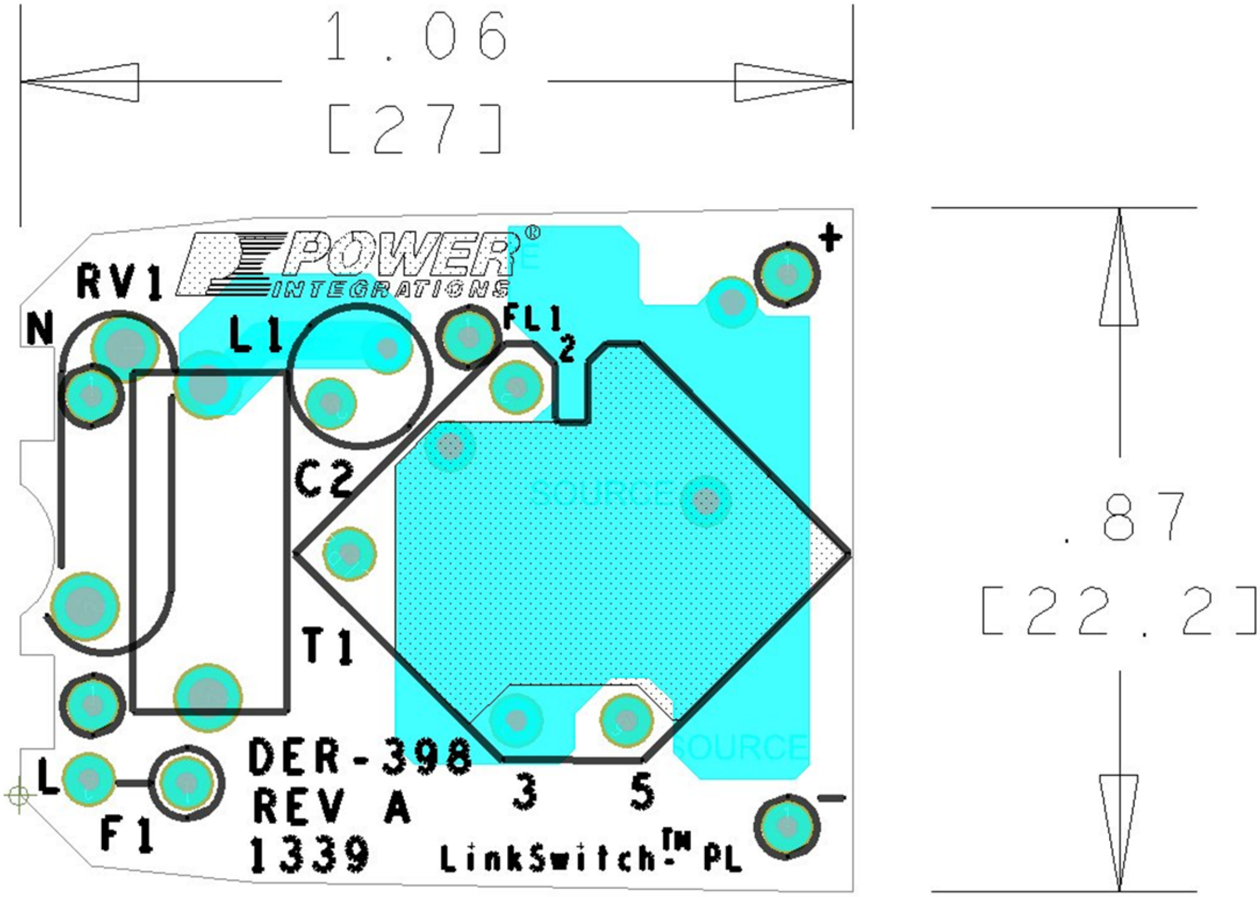

Figure 5 – Printed Circuit Layout, Top View.

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Figure 6 – Printed Circuit Layout, Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	220 nF, 450 V, Ceramic, X7T, 1210	3225X7T2W224K200AA	TDK
3	1	C2	470 nF, 250 V, Film	ECQ-E2474KB	Panasonic
4	1	C3	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
5	1	C4	10 μF, 10 V, Ceramic, X7R, 0805	C2012X7R1A106M	TDK
6	1	C5	2.2 μF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
7	1	C6	2.2 μF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
8	1	C7	150 μF, 16 V, Tant Electrolytic,SMD	16TQC150MYF	Panasonic
9	1	D1	400 V, 1 A, DIODE SUP FAST 1 A PWRDI 123	DFLU1400-7	Diodes, Inc.
10	1	D2	400 V, 1 A, DIODE SUP FAST 1 A PWRDI 123	DFLU1400-7	Diodes, Inc.
11	1	D3	50 V, 2 A, Schottky, SMD, DO-214AA	SS25-E3/52T	Vishay
12	1	F1	3 A, 125 V, Fast, Microfuse, Axial	MQ3	Bel Fuse
13	1	L1	1 mH, 0.15 A, Ferrite Core	SBCP-47HY102B	Tokin
14	1	R1	1.6 Ω, 1%, 1/4 W, Thick Film, 1206	RC1206FR-071R6L	Yago
15	1	R2	1.6 Ω, 1%, 1/4 W, Thick Film, 1206	RC1206FR-071R6L	Yago
16	1	R3	2 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ2R0V	Panasonic
17	1	R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
18	1	R5	300 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ301V	Panasonic
19	1	R6	200 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ204V	Panasonic
20	1	RV1	140 V, 12 J, 7 mm, RADIAL	V140LA2P	Littlefuse
21	1	T1	Bobbin, RM5, Vertical, 4 pins	B65806P1004D001	EPCOS
22	1	U1	LinkSwitch-PL, SO-8C	LNK457DG	Power Integrations

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7 Design Spreadsheet

ACDC_LinkSwitch-PL-TapBuck_121611; Rev.1.0; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL_TB LinkSwitch-PL Tapped Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90		90.00	V	Minimum AC Input Voltage
VACTYP	120		120.00	V	Typical AC Input Voltage
VACMAX	132		132.00	V	Maximum AC Input Voltage
FL			50.00	Hz	AC Mains Frequency
VOMIN			8.10		Minimum Output Voltage of LED string
VO	9.00		9.00	V	Output Voltage of LED string
VOMAX			9.90		Maximum Output Voltage of LED string
IO	0.55		0.55	A	Output Current riving LED strings
Power			4.95	W	Continuous Output Power
n	0.81		0.81		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Dimming Application	**No**		No		Enter Yes if design uses TRIAC dimming, otherwise select No
ENTER LinkSwitch-PL VARIABLES					
Chosen Device	**LNK457**		LNK457		Chosen LinkSwitch-II device
ILIMITMIN			0.80	A	Minimum Current Limit
ILIMITTYP			0.91	A	Typical Current Limit
ILIMITMAX			1.02	A	Maximum Current Limit
VOR			42.22	V	Reflected output voltage
Turns Ratio			4.44		Primary to secondary turns ratio
TON			2.34	us	Expected on-time of MOSFET at low line and PO
FSW			122.81	kHz	Expected switching frequency at low line and PO
Duty Cycle			28.69	%	Expected operating duty cycle at low line and PO
IRMS			0.15	A	Worst case primary RMS current at VO
IPK			0.78	A	Worst case peak primary current at VO
KDP			1.33		Worst case ratio between off-time of switch and reset time of core
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
Core Type					
Core Type	**RM5/I**		RM5/I		Enter Transformer Core
Core Part Number					If custom core is used - Enter part number here
Bobbin part number					Bobbin Part number (if available)
AE			24.80	mm^2	Core Effective Cross Sectional Area
LE			23.20	mm^2	Core Effective Path Length
AL			1700.00	nH/turn^2	Ungapped Core Effective Inductance
BW			4.70	mm	Bobbin Physical Winding Width
INDUCTOR DESIGN PARAMETERS					
LPMIN			372.00	uH	Minimum Inductance (Includes inductance of input and output winding)
LPTYP	400.00		400.00	uH	Typical inductance (Includes inductance of input and output winding)
LP_TOLERANCE	7.00		7.00	%	Tolerance of the inductance
TURNS_TOTAL			49.00	Turns	Total number of turns (Includes input and output winding turns).
ALG			166.60	nH/turn^2	Gapped Core Effective Inductance
BM			2738.19	Gauss	Calculated Worst Case Maximum Flux Density (BM < 3000 G)
BP			3592.50	Gauss	Calculated Worst Case Peak Flux Density (BP < 3600 G)

BAC			1369.09	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			126.55		Relative Permeability of Ungapped Core
LG			0.17	mm	Gap Length (Lg > 0.1 mm)
Input Section					Section of winding that conducts only during ON time of the LINKSwitch-II
NL_INPUT			40.00		Number of turns in Input section.
AWG	28.00		28.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
L			3.11		Number of Layers (Input section)
CMA			1089.29	Cmils	Design will work, but it is possible to reduce wire thickness
Output Section					Section of winding that conducts both when the Linkswitch-II is ON and OFF.
TURNS_OUTPUT			9.00		Number of Turns in Output winding. To adjust number of turns change INDUCTOR_RATIO
AWG_OUTPUT	25		25.00		Output Winding Wire Gauge (Rounded to next smaller standard AWG value)
L_OUTPUT			0.97		Number of Layers (Output winding)
CMA_OUTPUT			321.07	Cmils	Current Density capacity 200 < CMA < 500
Bias Section					
Use Bias?	Auto		No		Is a Bias winding used?
TURNS_BIAS			0.00	Turns	Number of turns of Bias Winding
VBIAS			0.00	V	Bias Voltage. Always check performance at minimum VO and maximum VAC.
PIVBS			0.00	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at maximum VAC and max VO)
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			28.69	%	Duty cycle measured at minimum input voltage
IAVG			0.06	A	Input average current measured at the minimum input voltage
IP			0.78	A	Peak Primary current at maximum input voltage
ID_PK			3.46	A	Peak output winding current at the maximum input voltage
ISW_RMS			0.15	A	Switch RMS current measured at the minimum input voltage
ID_RMS			1.00	A	RMS current of freewheeling diode at maximum input voltage
IL_RMS			0.15	A	RMS current of the primary section of the inductor measured at the minimum input voltage
IL_TAP_RMS			1.00	A	RMS current of the output winding section of the inductor at the maximum input voltage
FEEDBACK WINDING PARAMETERS					
RFEEDBACK			0.59	ohm	This is a first approximation for the sense resistor and will likely require fine tuning in the bench
CBP			1.00	uF	Minimum required Bypass pin capacitor for correct operation
VOLTAGE STRESS PARAMETERS					
VDRAIN			280.68	V	Estimated worst case drain voltage at maximum input voltage
VOR			42.22	V	Reflected output voltage
PIVS			44.19	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at maximum VAC and maximum VO)

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8 Transformer Specifications

8.1 Electrical Diagram

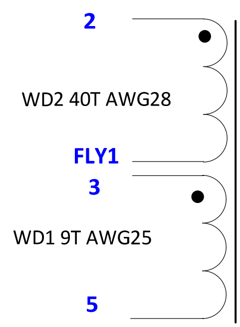

Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Primary Inductance	Temporarily connect FLY1 to pin 3, measure pins 2-5.	400 µH ±7%
Resonant Frequency	Pins 2-FLY1, all other windings open.	1 MHz (Min.)

8.3 Materials

Item	Description
[1]	Core: B-RM5-V-4 Pins (2/2) PI PN: 25-01012-00.
[2]	Bobbin: RM5/I – 3F3.
[3]	Clip: RM5: Allstar Magnetic, PN: CLI/P-RM4/5/I.
[4]	Magnet Wire, #28 AWG, solderable double coated.
[5]	Magnet Wire, #25 AWG, solderable double coated.
[6]	Tape: 3M 1298, Polyester Film, 2.0 mil thick, 4.5 mm wide.
[7]	Tape: 3M 1298, Polyester Film, 2.0 mil thick, 9.0 mm wide.
[8]	Varnish: Dolph BC-359; or equivalent.

8.4 Build Diagram

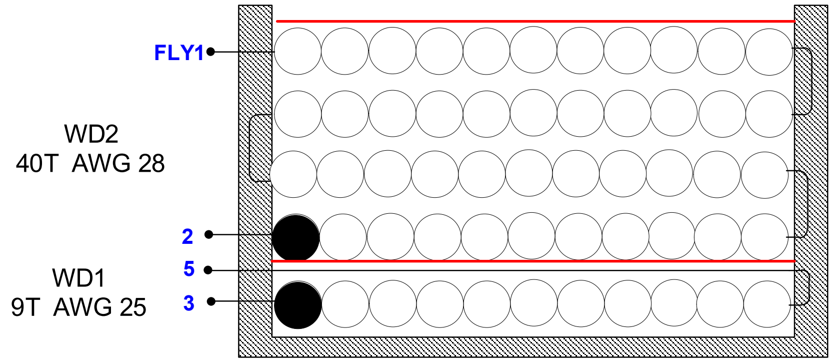

Figure 8 – Transformer Build Diagram.

8.5 Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 3 side is on the right.
WD1	Start at pin 3. Wind 9 turns of item [5] as shown in Figure 8. Terminate at pin 5.
WD2	Start at pin 2. Wind 40 turns of item [4] and terminate the other end at FLY1.
Finish	Grind the core to get the specified inductance. Assemble cores with clips item [3]. Cut pin 6 and ground pin of clip where closes to pins 2, 6. Wrap 1 piece of tape item [7] with 15.0 mm length over bottom core (see picture below). Varnish with item [8].

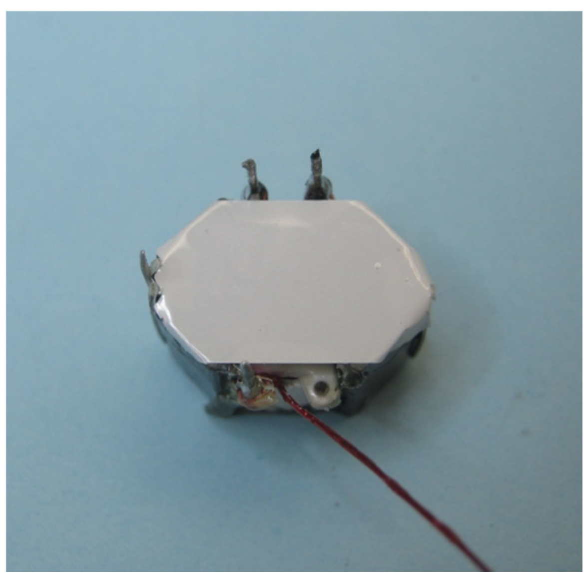

Figure 9 – Completed Transformer.
(Pin 6 cut, one clip pin cut, and tape applied at the bottom of the inductor.)

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9 Performance Data

All measurements performed at room temperature (~25 ºC) otherwise specified.

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
90.05	82.18	7.02	0.949	11.60	9.33	570.20	5.69	5.32	81.03	1.33
100.02	74.14	6.91	0.931	14.11	9.30	564.40	5.61	5.25	81.26	1.29
115.07	65.55	6.79	0.900	17.58	9.29	560.10	5.53	5.20	81.49	1.26
120.05	62.57	6.66	0.886	19.79	9.27	552.40	5.43	5.12	81.61	1.22
132.08	57.69	6.53	0.857	24.85	9.25	545.20	5.33	5.04	81.59	1.20

Table 1 – Test Data for ~9 V LED Load.

9.1 Efficiency

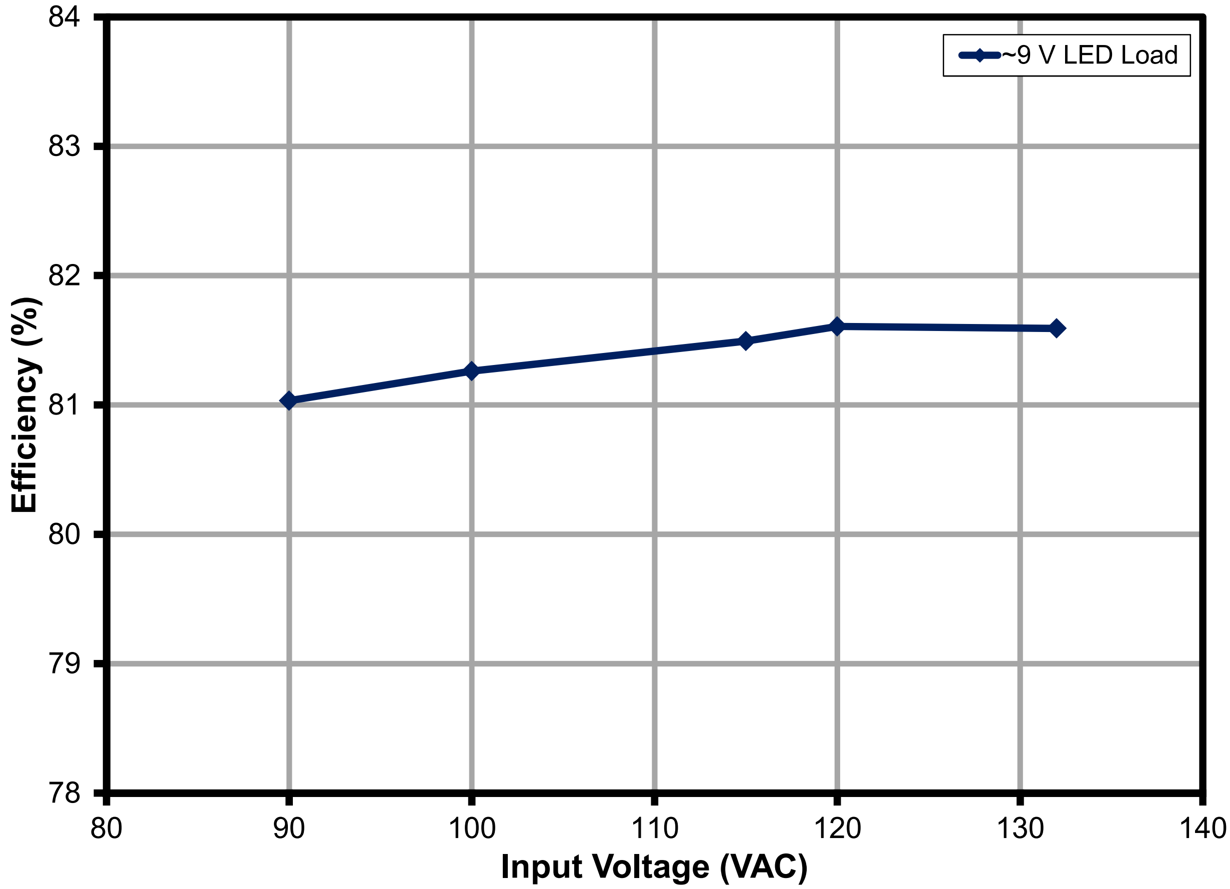

Figure 10 – Efficiency with Respect to AC Input Voltage. 90-132 VAC (60 Hz) Input.

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9.2 *Output Current Regulation*

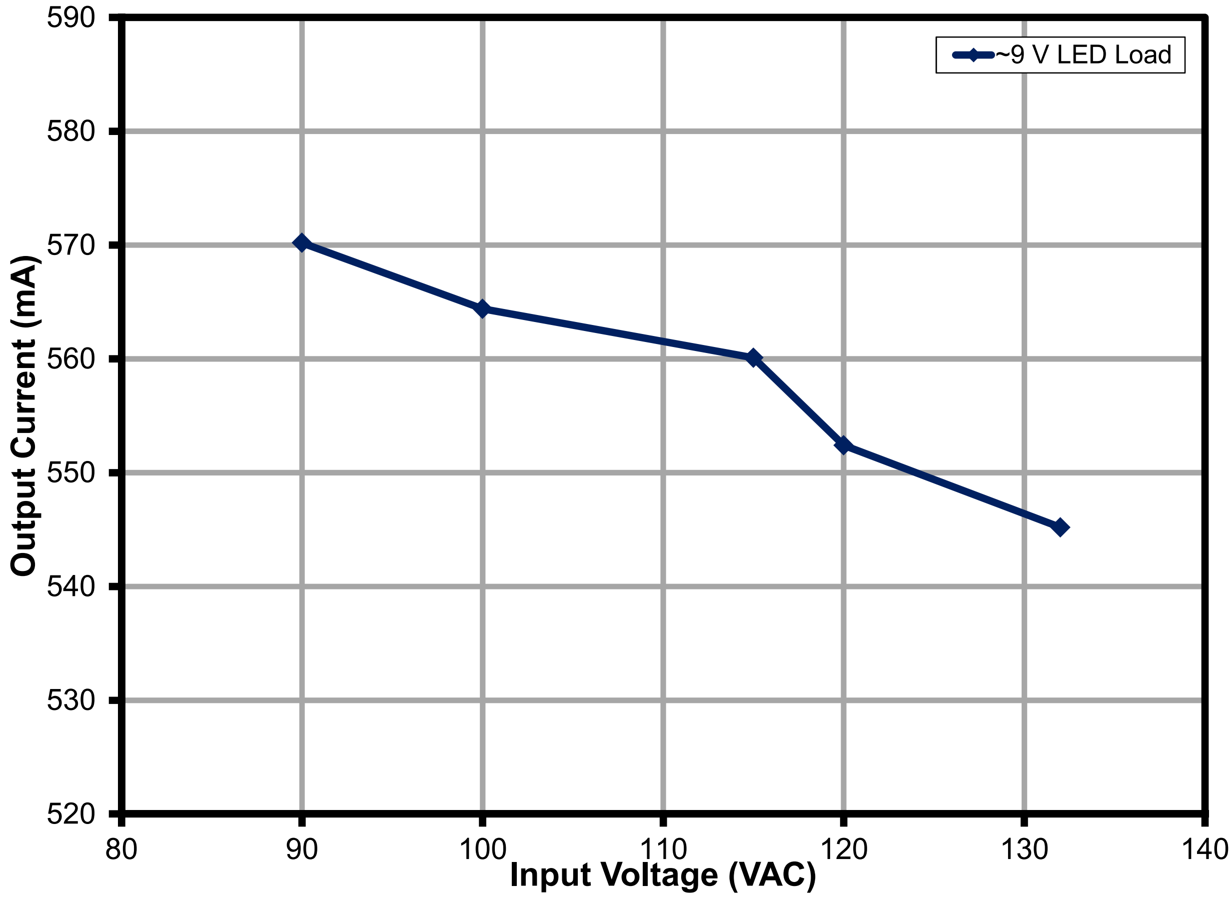

Figure 11 – Line Regulation.

9.3 Power Factor

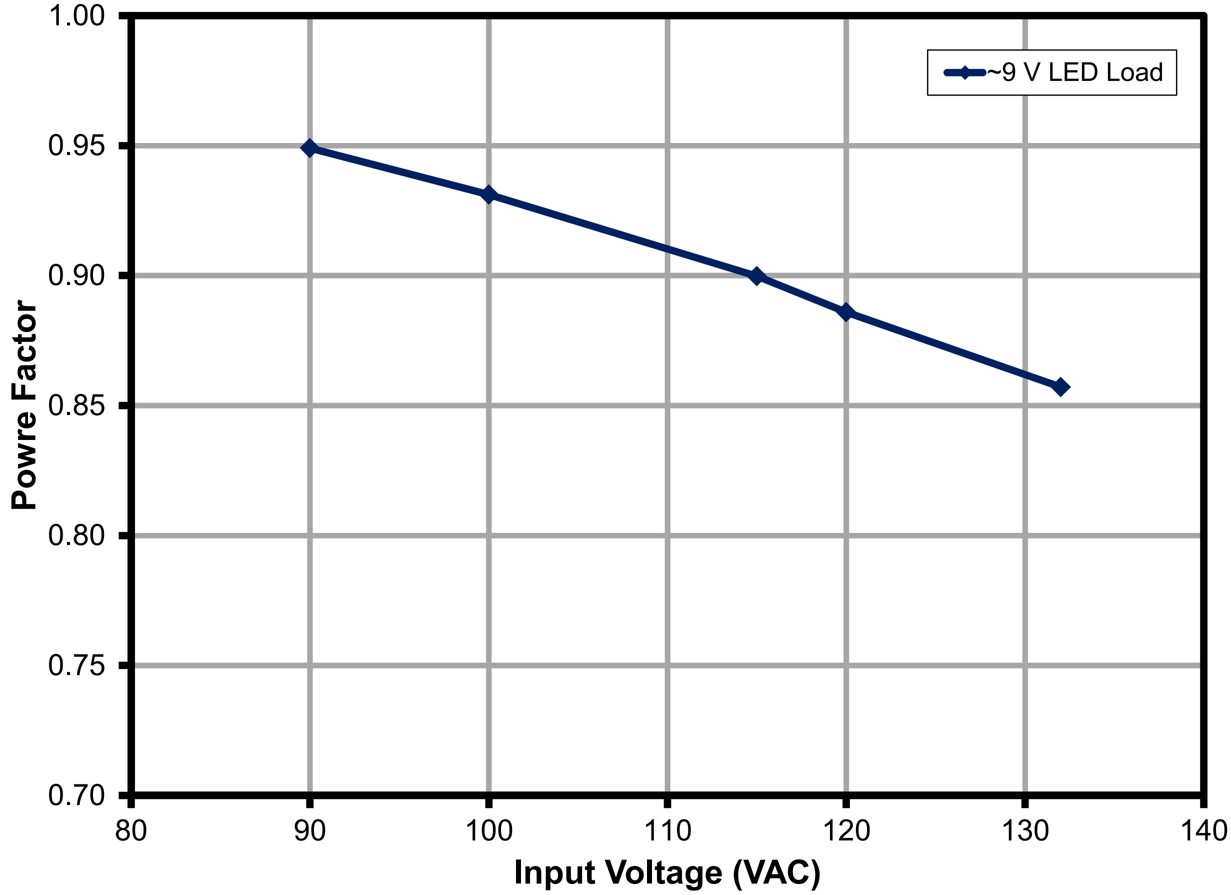

Figure 12 – Line Regulation.

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9.4 A-THD %

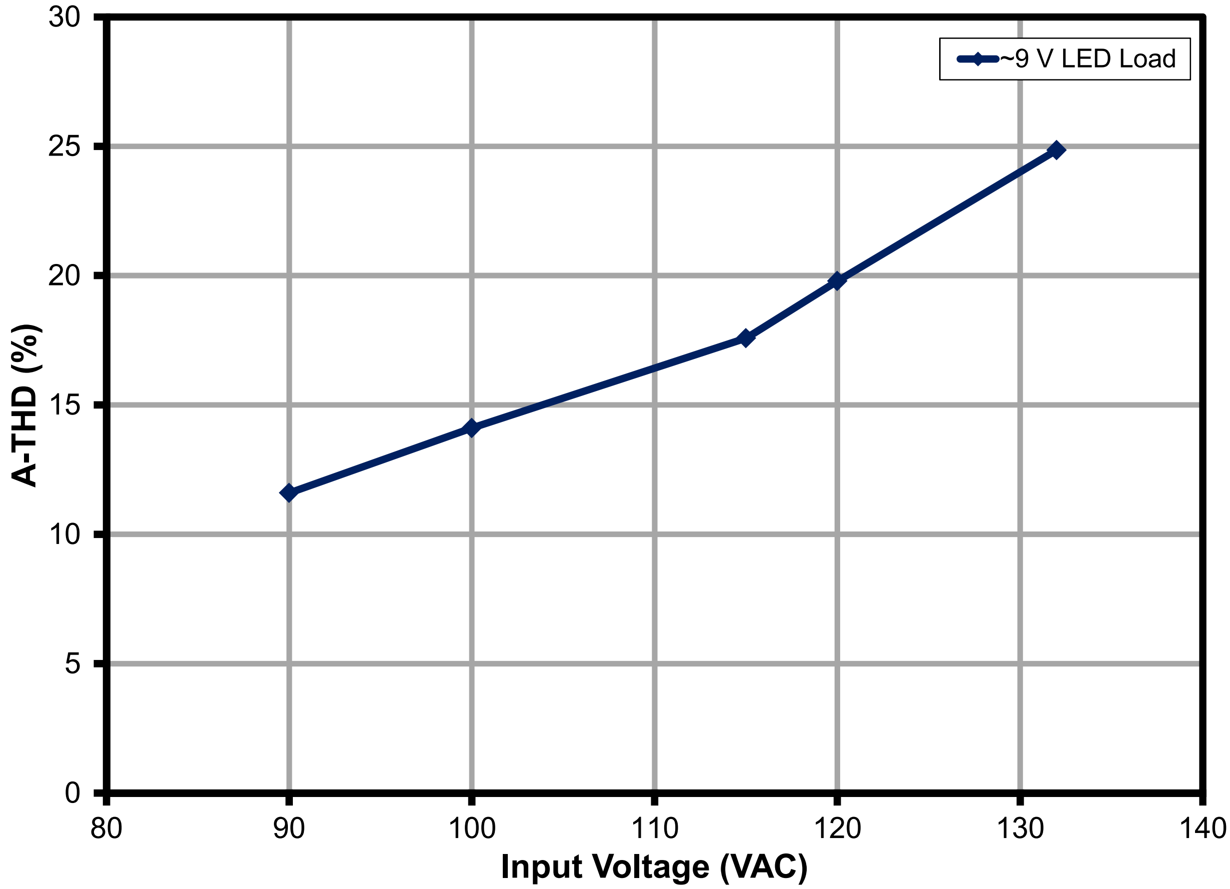

Figure 13 – Line Regulation.

10 Thermal Performance

10.1 Thermal Set-up

The LED Driver was placed inside a GU10 assembly provided by CREE and thermal test was run with the unit placed inside the chamber. Note: The GU10 assembly shown in Figure 1 has no light diffuser which may have a slight beneficial affect on thermal performance.

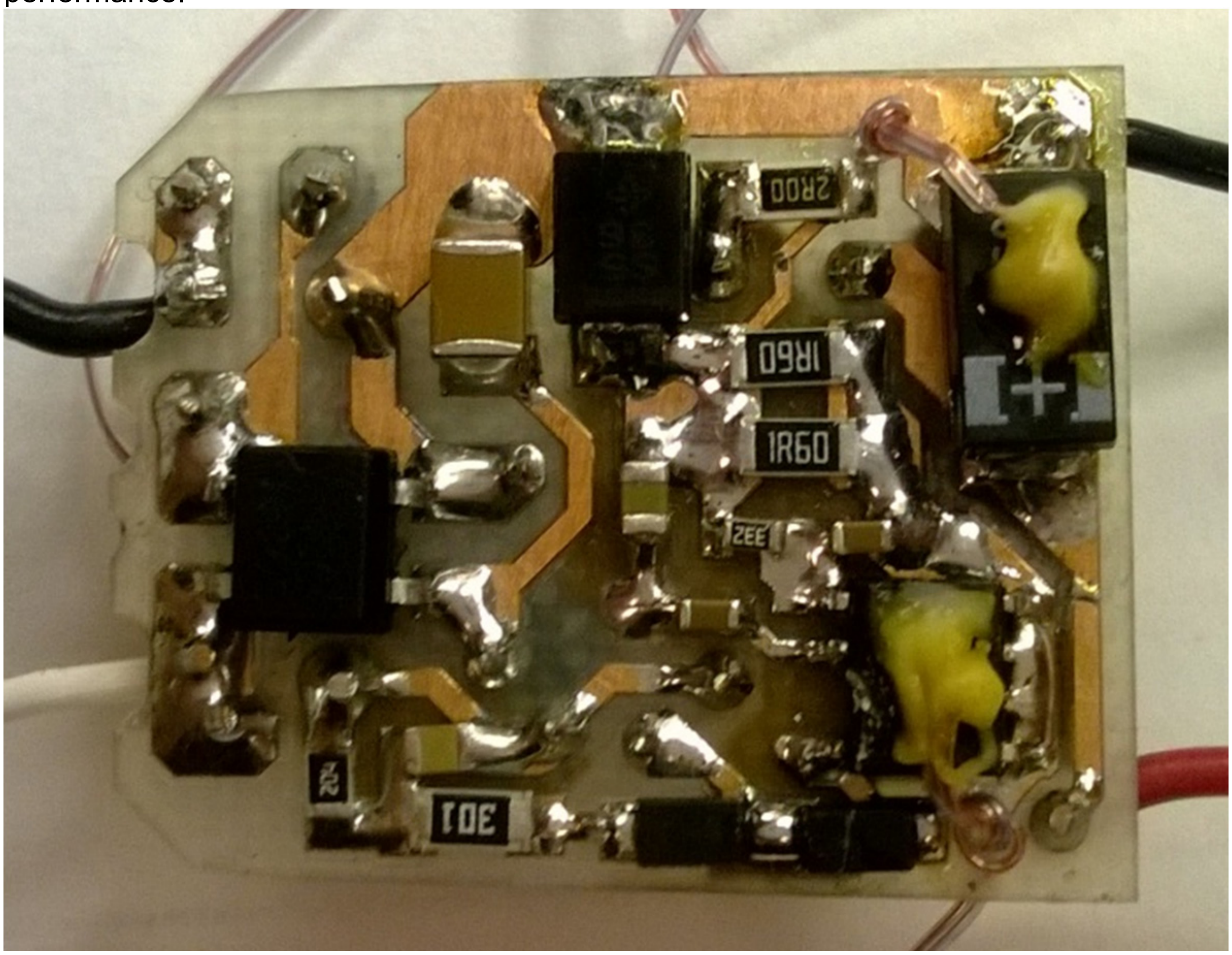

Figure 14 – Bottom Side Thermocouple Location.

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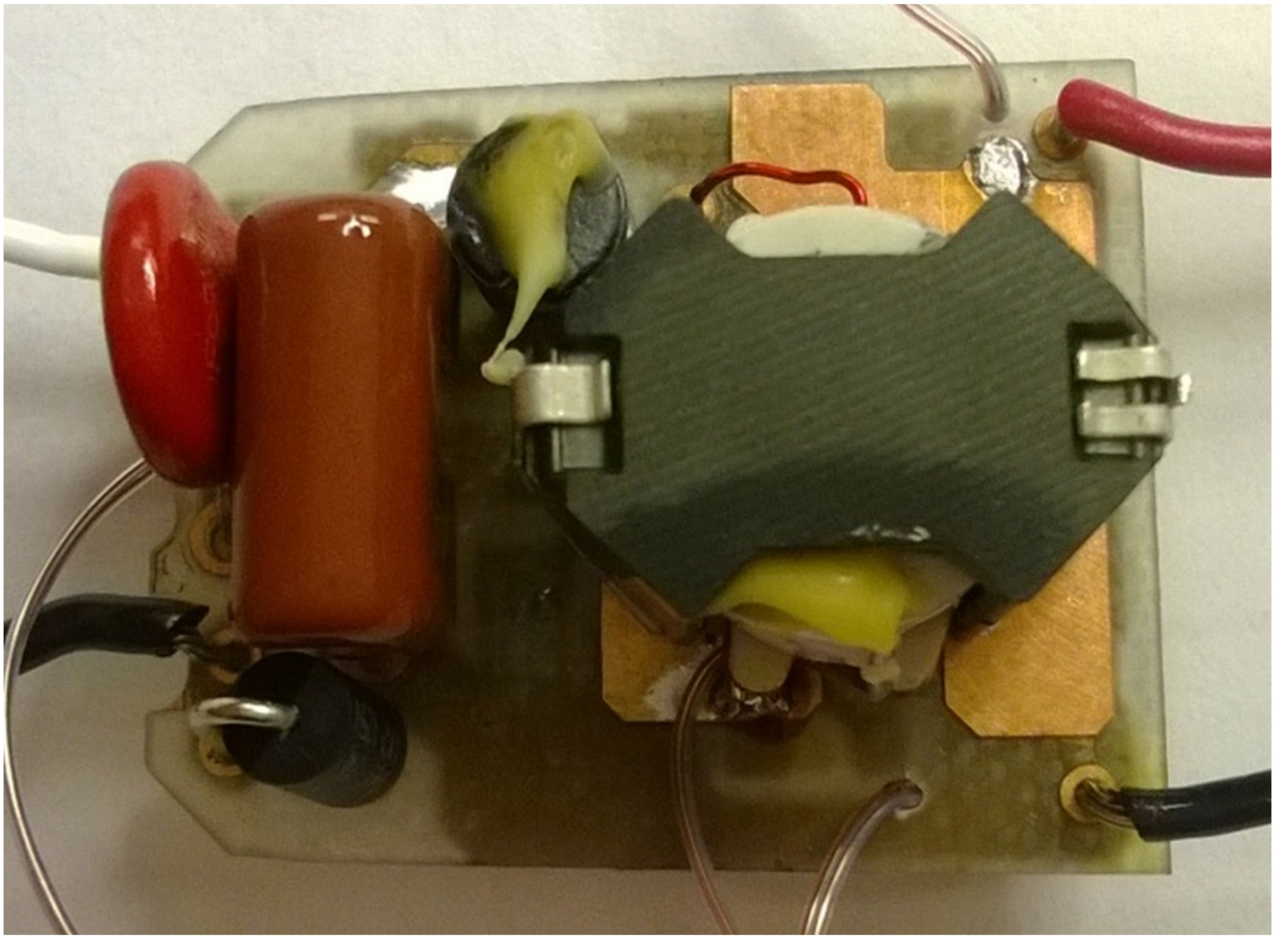

Figure 15 – Top Side Thermocouple Locations.

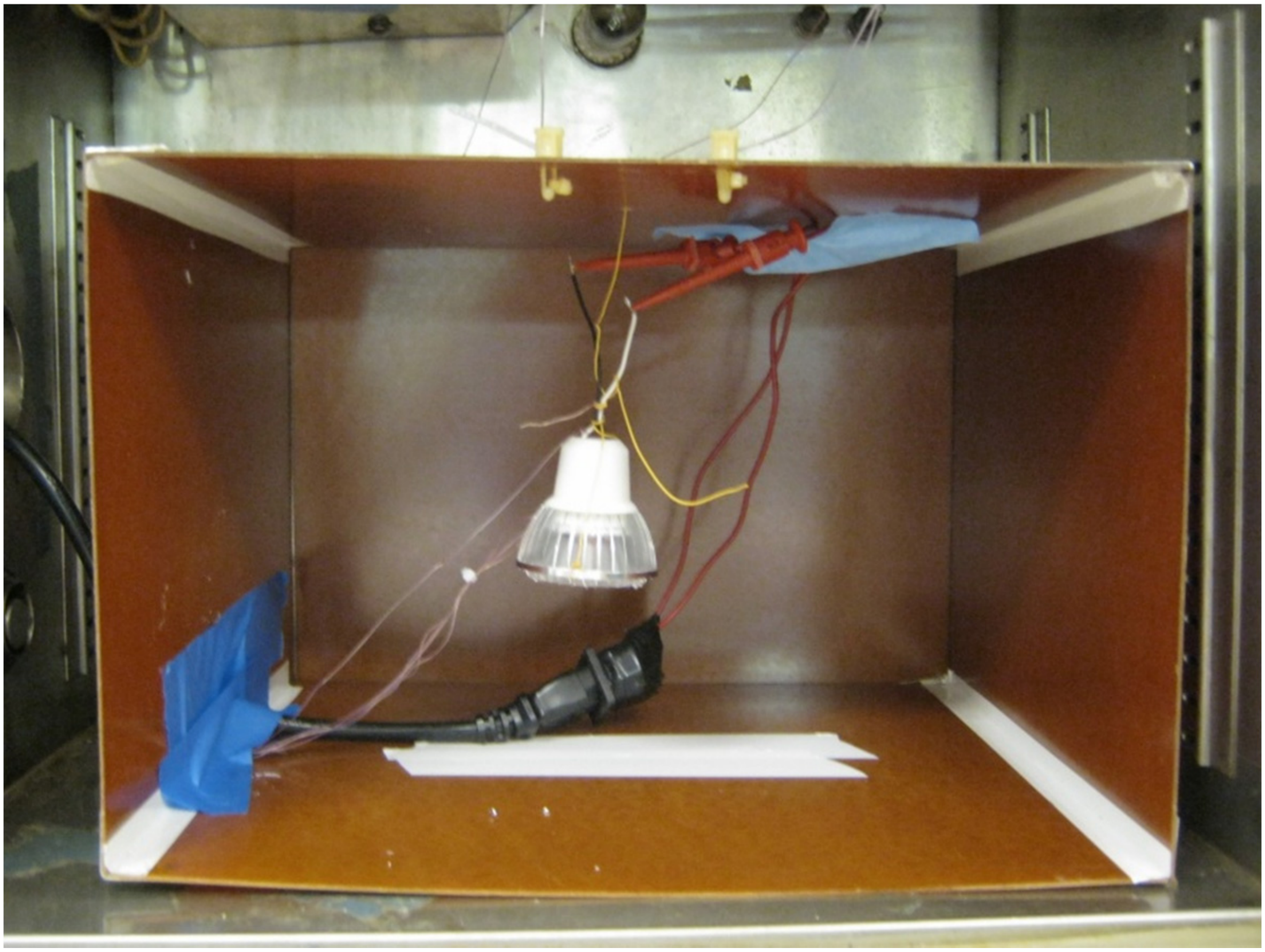

Figure 16 – GU10 Bulb Placed Inside the Box to Block Thermal Chamber Fan.

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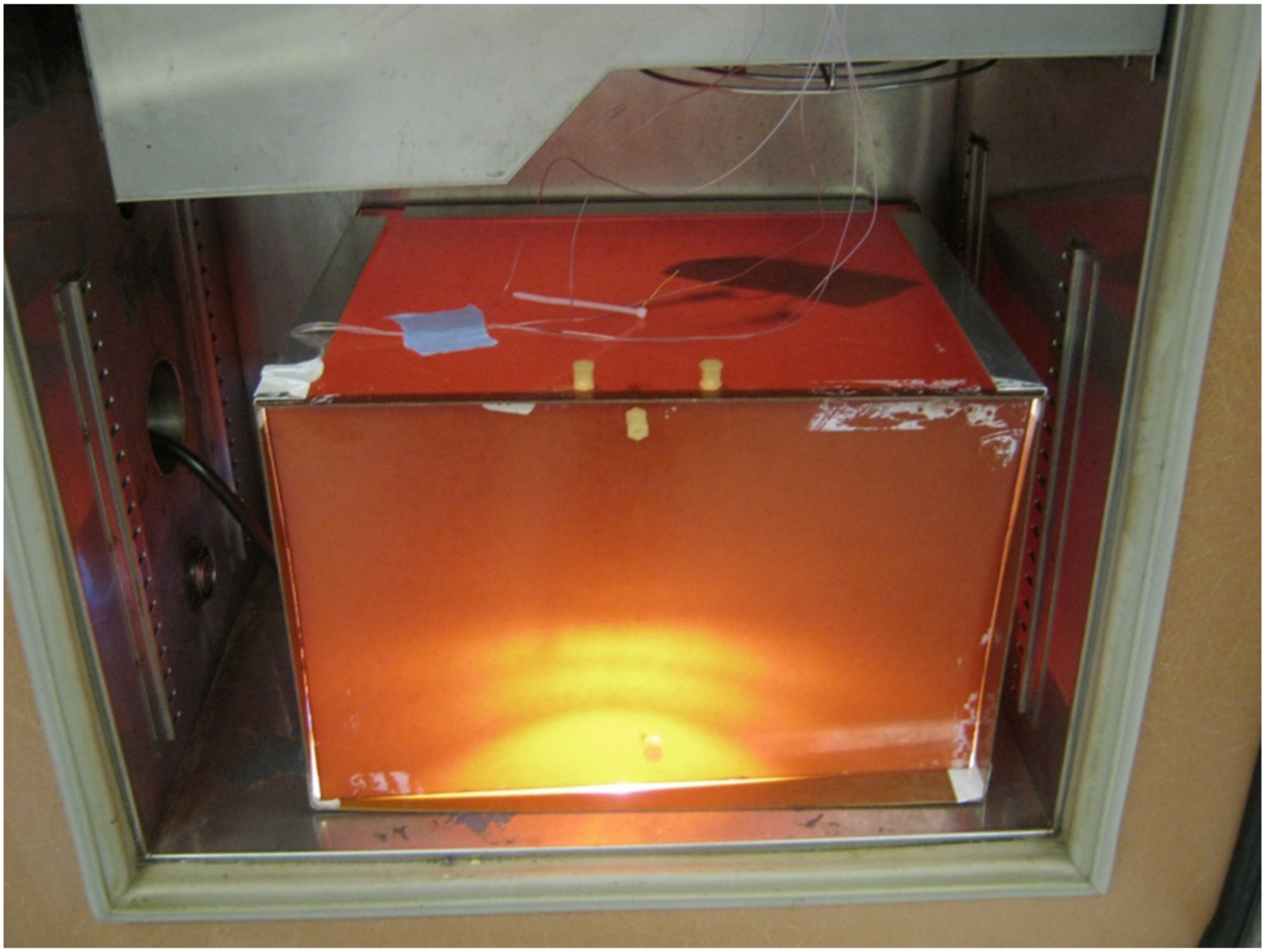

Figure 17 – Box Was Covered Before the Chamber Door Was Closed**.**

10.2 Thermal Results

10.2.1 Input: 90 VAC / 60 Hz
Load: ~9 V LED Load

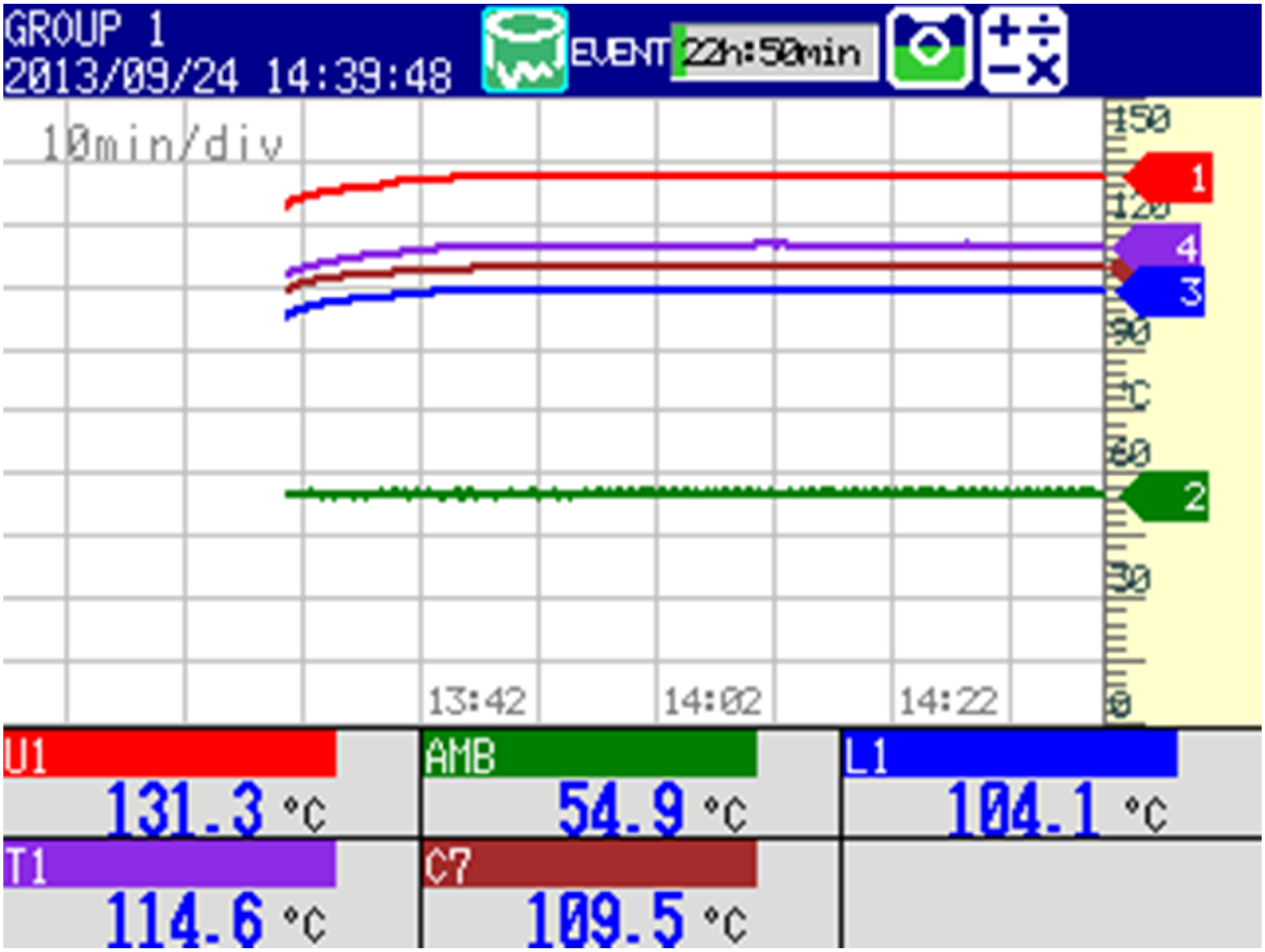

Figure 18 – Thermal Measurement at 90 VAC Input, ~50 ºC Ambient.

Location	Description	Temperature (ºC)
AMB	External Ambient	54.9
U1	LNK457DG	131.3
L1	Differential Choke	104.1
T1	Transformer	114.6
C7	Output Capacitor	109.5

Table 2 – 90 VAC Input Critical Components Thermal Measurement.

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10.2.2 Input: 120 VAC / 60 Hz
Load: ~9 V LED Load

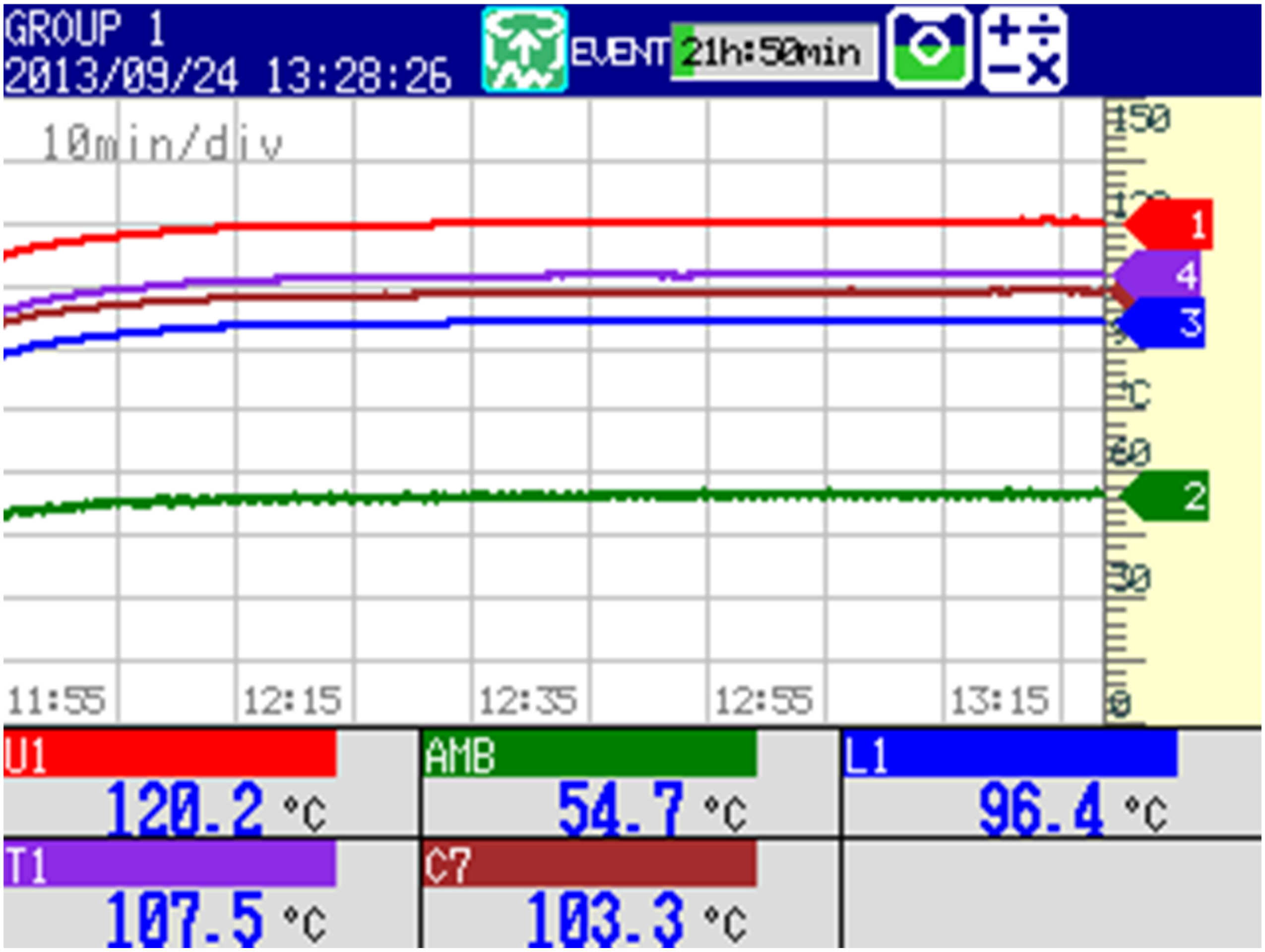

Figure 19 – Thermal Measurement at 120 VAC Input, ~50 ºC Ambient.

Location	Description	Temperature (ºC)
AMB	External Ambient	54.7
U1	LNK457DG	120.2
L1	Differential Choke	96.4
T1	Transformer	107.5
C7	Output Capacitor	103.3

Table 3 – 120 VAC Input Critical Components Thermal Measurement.

10.2.3 Input: 132 VAC / 60 Hz
Load: ~9 V LED Load

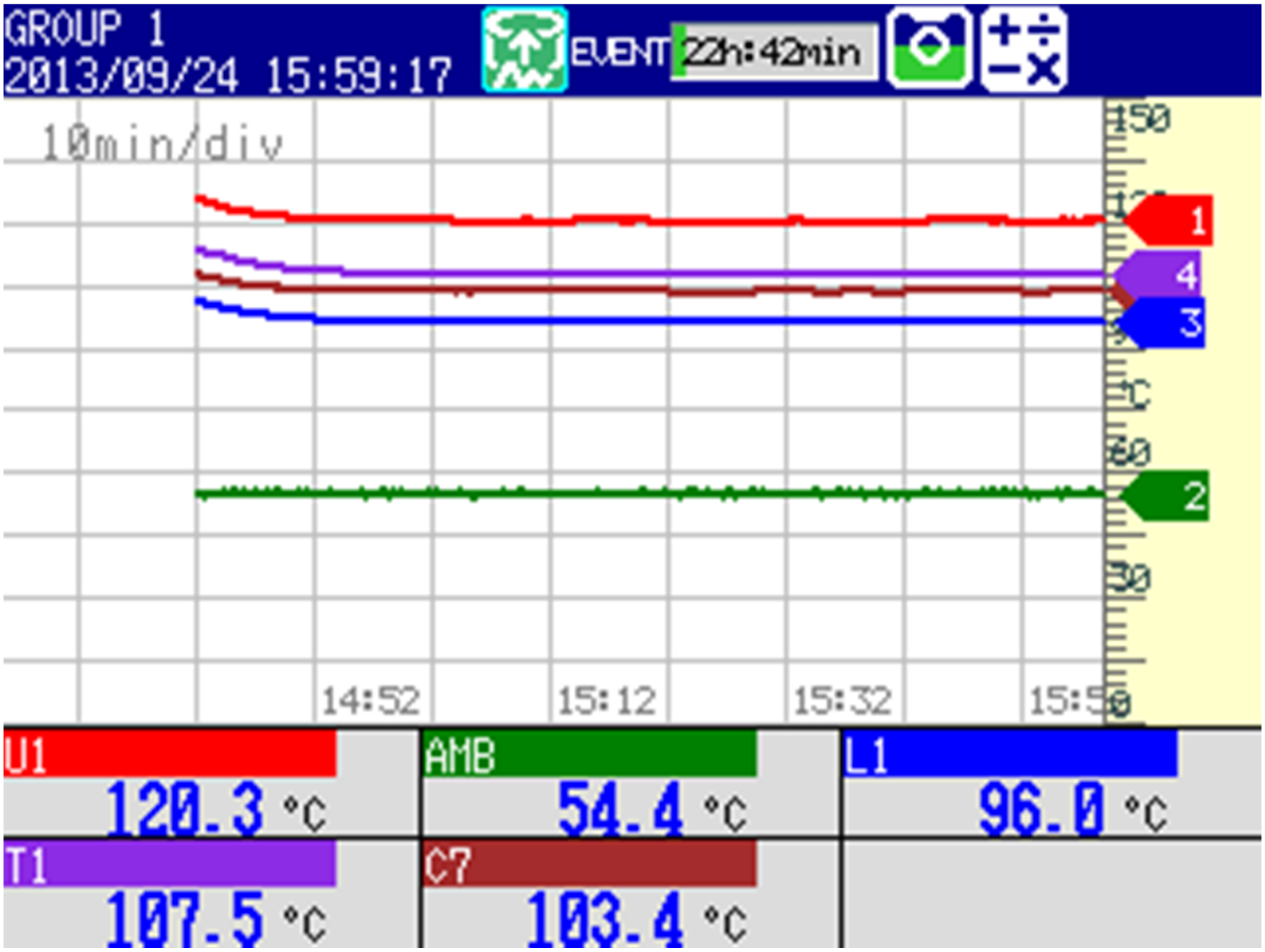

Figure 20 – Thermal Measurement at 132 VAC Input, ~50 ºC Ambient.

Location	Description	Temperature (ºC)
AMB	External Ambient	54.4
U1	LNK457DG	120.3
L1	Differential Choke	96
T1	Transformer	107.5
C7	Output Capacitor	103.4

Table 4 – 132 VAC Input Critical Components Thermal Measurement.

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11 Waveforms

11.1 Drain Voltage Normal Operation

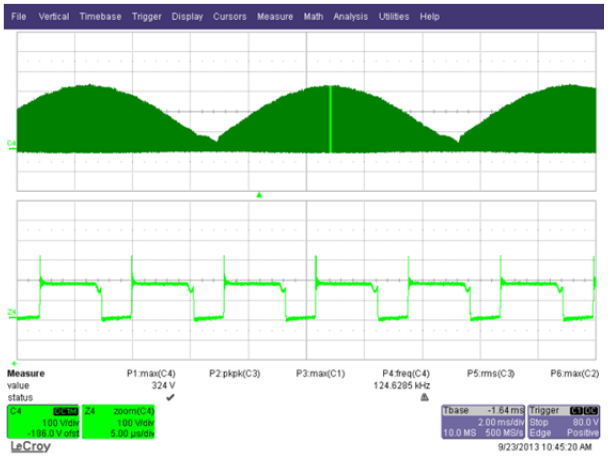

Figure 21 – 90 VAC, 60 Hz, Full Load.
Ch4: V_{D-S}, 100 V / div., 2 ms / div.
Z4: V_{D-S}, 100 V, 5 μs / div.

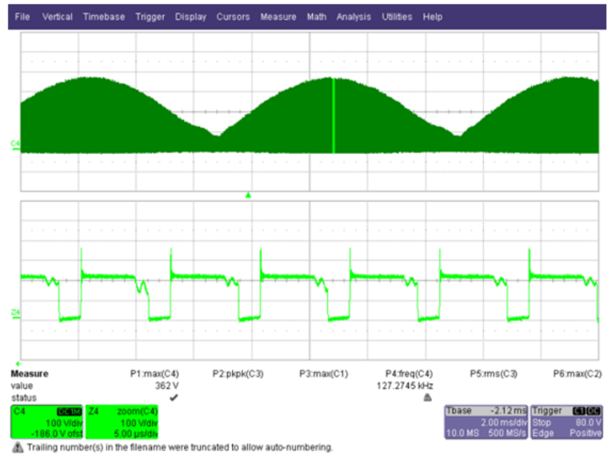

Figure 22 – 115 VAC, Full Load.
Ch4: V_{D-S}, 100 V / div., 2 ms / div.
Z4: V_{D-S}, 100 V, 5 μs / div.

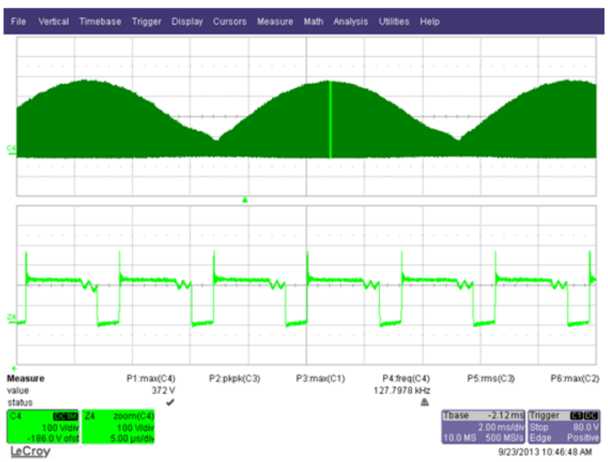

Figure 23 – 120 VAC, 60 Hz, Full Load.
Ch4: V_{D-S}, 100 V / div., 2 ms / div.
Z4: V_{D-S}, 100 V, 5 μs / div.

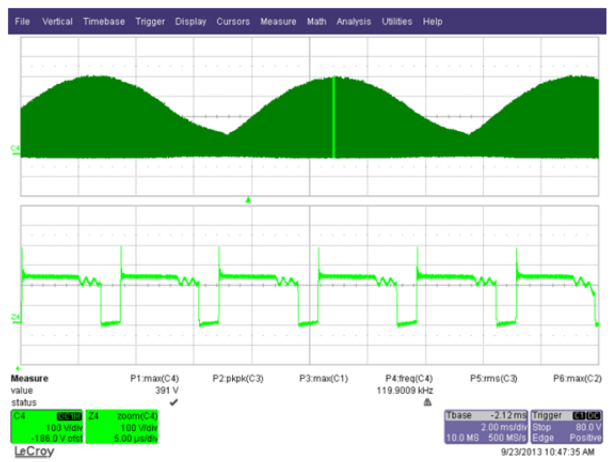

Figure 24 – 132 VAC, Full Load.
Ch4: V_{D-S}, 100 V / div., 2 ms / div
Z4: V_{D-S}, 100 V, 5 μs / div.

11.2 Drain Current at Normal Operation

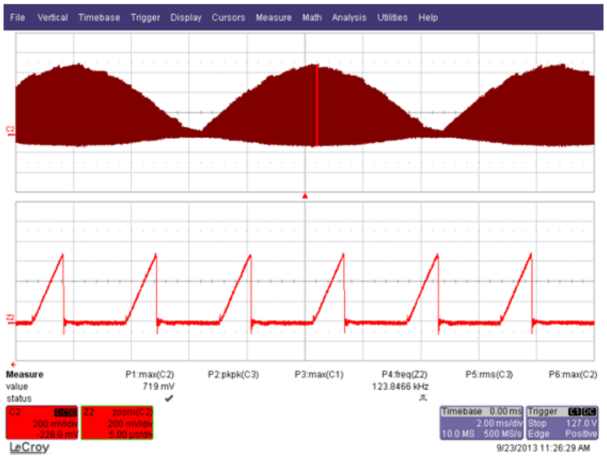

Figure 25 – 90 VAC, 60 Hz, 9 V_{LED}.
Ch2: $I_{D\text{-}S}$, 200 mA / div., 2 ms / div.
Z2: $I_{D\text{-}S}$, 200 mA, 5 μs / div.

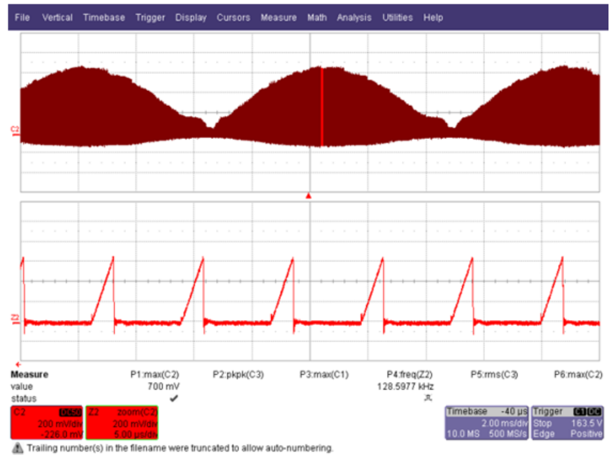

Figure 26 – 115 VAC, 60 Hz, 9 V_{LED}.
Ch2: $I_{D\text{-}S}$, 200 mA / div., 2 ms / div.
Z2: $I_{D\text{-}S}$, 200 mA, 5 μs / div.

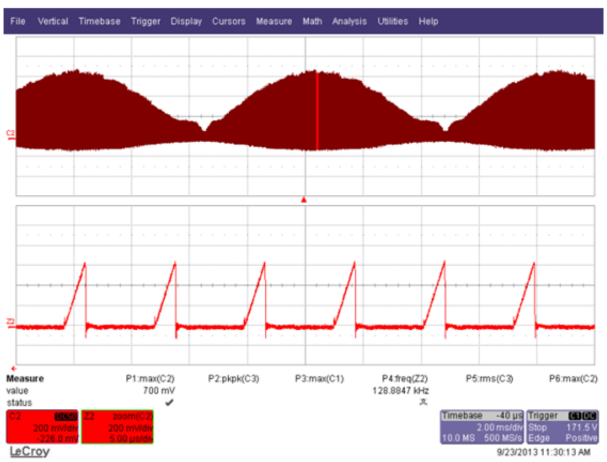

Figure 27 – 120 VAC, 60 Hz, 9 V_{LED}.
Ch2: $I_{D\text{-}S}$, 200 mA / div., 2 ms / div.
Z2: $I_{D\text{-}S}$, 200 mA, 5 μs / div.

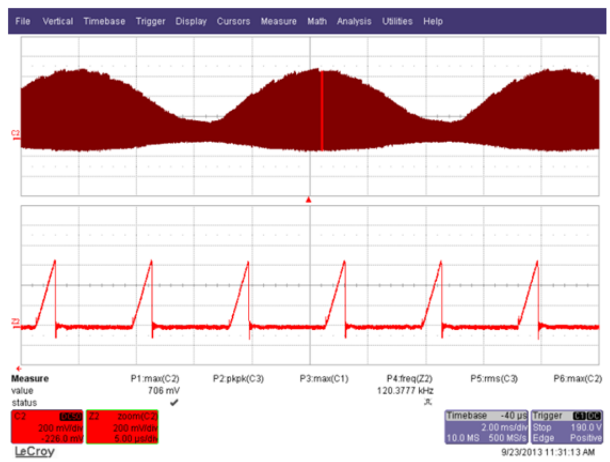

Figure 28 – 132 VAC, 60 Hz, 9 V_{LED}.
Ch2: $I_{D\text{-}S}$, 200 mA / div., 2 ms / div.
Z2: $I_{D\text{-}S}$, 200 mA, 5 μs / div.

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11.3 Drain Voltage and Current When Output Short

Device is operating within the range and no inductor saturation was observed.

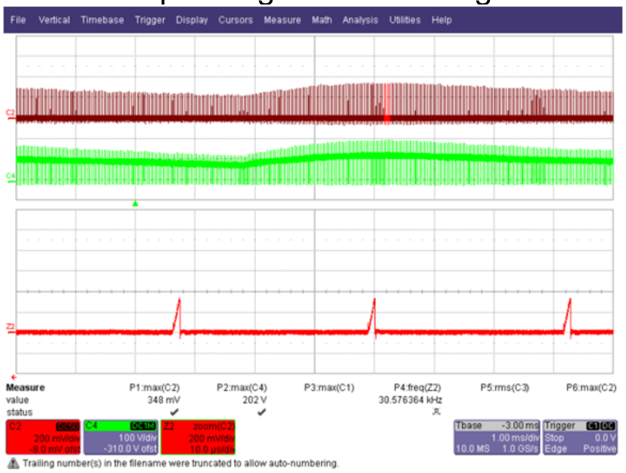

Figure 29 – 90 VAC Input, Output Short.
Ch4: V_{D-S}, 100 V / div., 1 ms / div.
Ch2: I_{D-S}, 200 mA / div., 1 ms / div.
Z2: I_{D-S}, 200 mA / div., 10 µs / div.

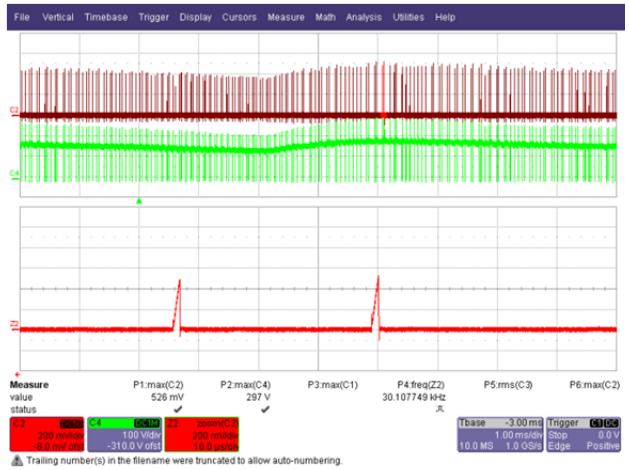

Figure 30 – 132 VAC Input, Output Short.
Ch4: V_{D-S}, 100 V / div., 1 ms / div.
Ch2: I_{D-S}, 200 mA / div., 1 ms / div.
Z2: I_{D-S}, 200 mA / div., 10 µs / div.

11.4 Drain Voltage and Current Start-up Profile

Device is operating within the range and no inductor saturation was observed.

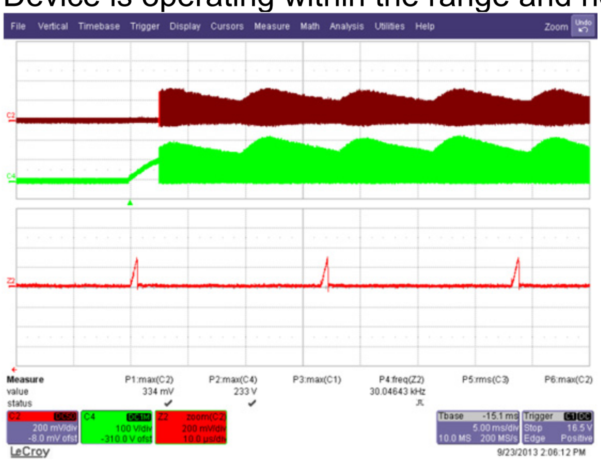

Figure 31 – 90 VAC / 60 Hz Start-up.
Ch4: V_{D-S}, 100 V / div., 5 ms / div.
Ch2: I_{D-S}, 200 mA / div., 5 ms / div.
Z2: I_{D-S}, 200 mA / div., 10 µs / div.

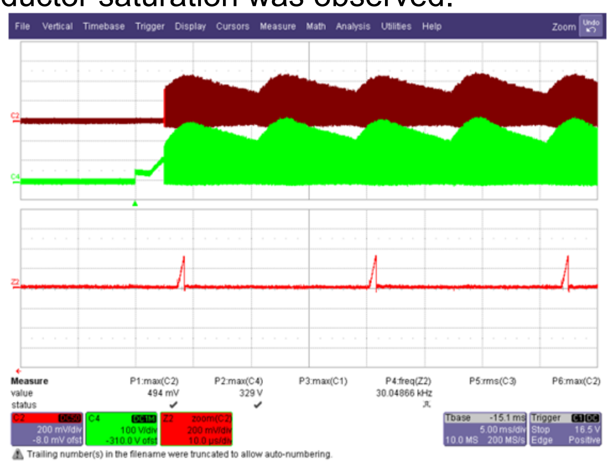

Figure 32 – 132 VAC / 60 Hz Start-up.
Ch4: V_{D-S}, 100 V / div., 5 ms / div.
Ch2: I_{D-S}, 200 mA / div., 5 ms / div.
Z2: $I_{D-S,}$ 200 mA / div., 10 µs / div.

11.5 Output Current Start-up and Power-Down Profile

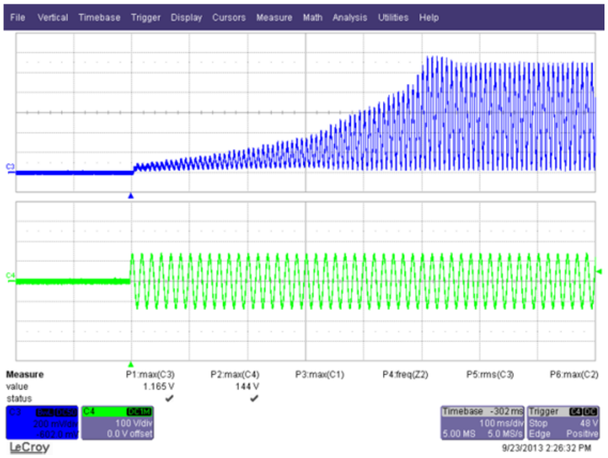

Figure 33 – 90 VAC, 60 Hz, Full Load Start-up.
Ch3: I_{OUT}, 200 mA / div., 100 ms / div.
Ch4: V_{IN}, 100 V / div., 100 ms / div.

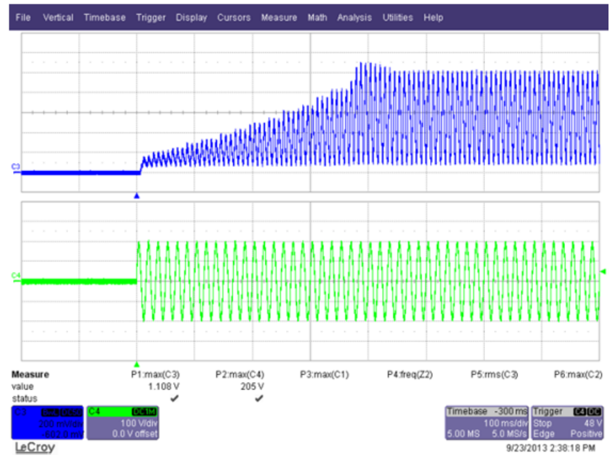

Figure 34 – 132 VAC, 60 Hz, Full Load Start-up.
Ch3: I_{OUT}, 200 mA / div., 100 ms / div.
Ch4: V_{IN}, 100 V / div., 100 ms / div.

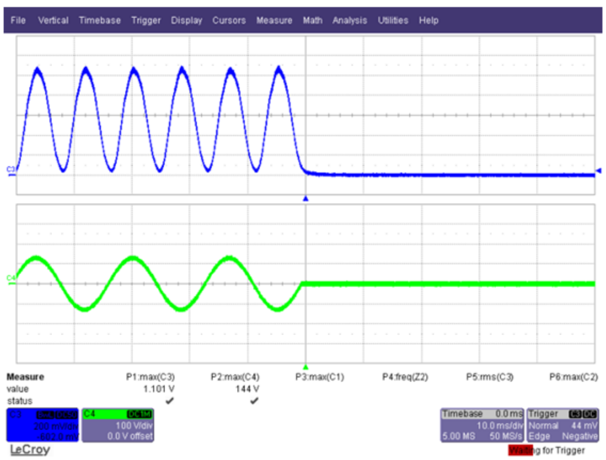

Figure 35 – 90 VAC, 60 Hz, Full Load, Power Down.
Ch3: I_{OUT}, 200 mA / div., 10 ms / div.
Ch4: V_{IN}, 100 V / div., 10 ms / div.

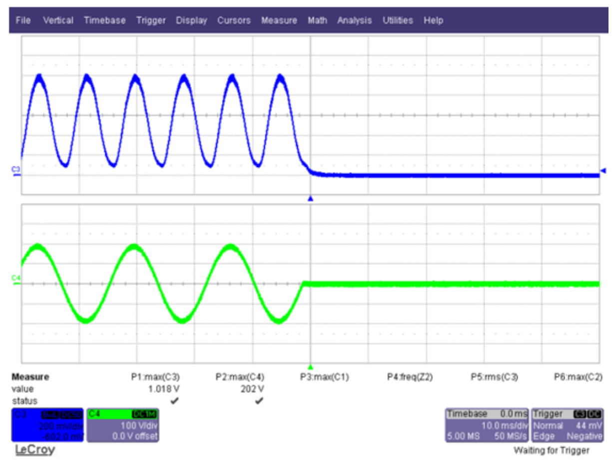

Figure 36 – 132 VAC, 60 Hz, Full Load, Power Down.
Ch3: I_{OUT}, 200 mA / div., 10 ms / div.
Ch4: V_{IN}, 100 V / div., 10 ms / div.

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11.6 Input-Output Profile

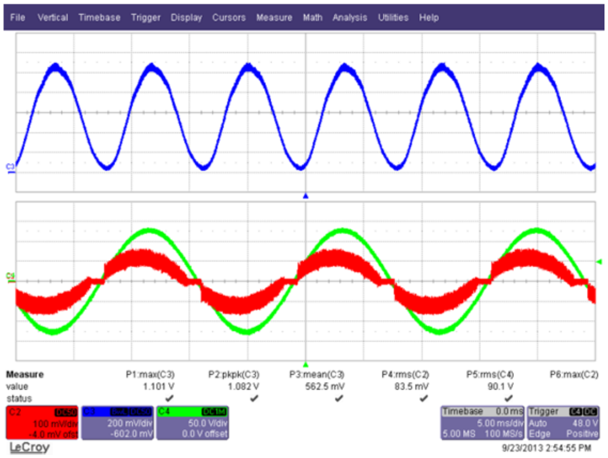

Figure 37 – 90 VAC, 60 Hz, Full Load.
Ch3: I_{OUT}, 200 mA / div, 5 ms / div
Ch2: I_{IN}, 100 mA / div, 5 ms / div
Ch4: V_{IN}, 50 V / div, 5 ms / div

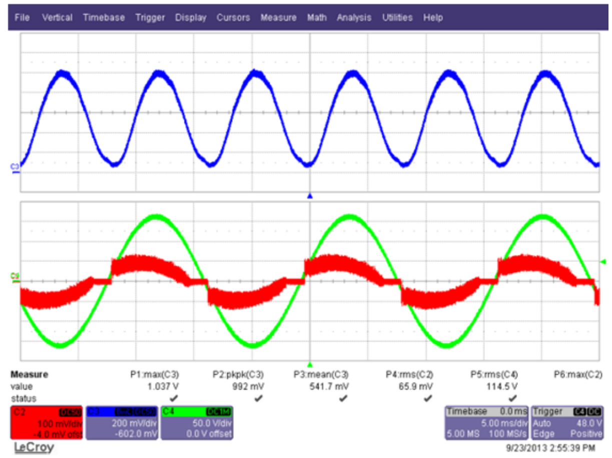

Figure 38 – 115 VAC, Full Load.
Ch3: I_{OUT}, 200 mA / div, 5 ms / div.
Ch2: I_{IN}, 100 mA / div, 5 ms / div
Ch4: V_{IN}, 50 V / div, 5 ms / div

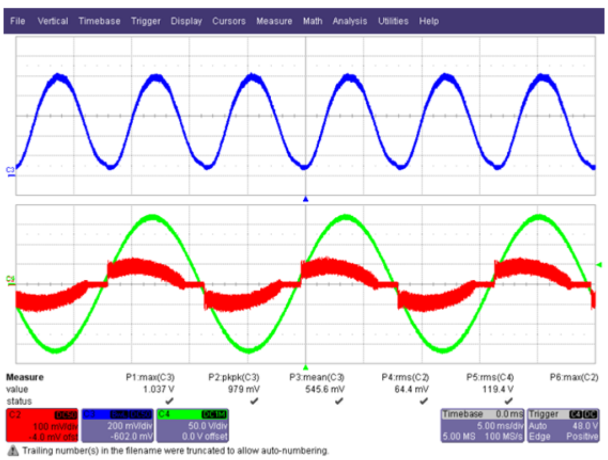

Figure 39 – 120 VAC, 60 Hz, Full Load.
Ch3: I_{OUT}, 200 mA / div., 5 ms / div.
Ch2: I_{IN}, 100 mA / div., 5 ms / div.
Ch4: V_{IN}, 50 V / div., 5 ms / div.

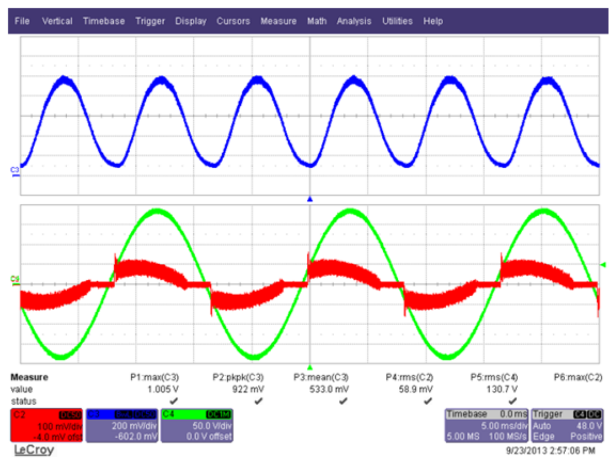

Figure 40 – 132 VAC, Full Load.
Ch3: I_{OUT}, 200 mA / div., 5 ms / div.
Ch2: I_{IN}, 100 mA / div., 5 ms / div.
Ch4: V_{IN}, 50 V / div., 5 ms / div.

11.7 Brown-out/ Brown-in

No failure of any component during brownout test of 0.5 V / sec AC cut-in and cut-off.

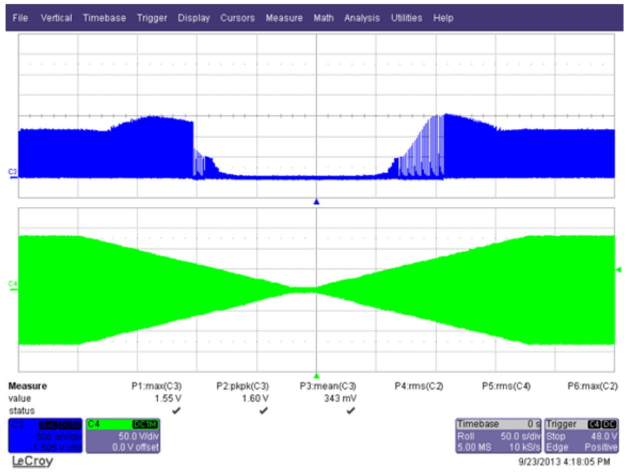

Figure 41 – Brown-out Test at 0.5 V / s. Maximum LED Peak Current Measured is 1.55 A.
Ch4: V_{IN}, 50 V / div.
Ch3: $I_{OUT,}$ 500 mA / div.
Time Scale: 50 s / div.

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12 Line Surge

The unit was subjected to ±2500 V 100 kHz ring wave and ±500 V differential surge at 120 VAC, 60 Hz using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	120	L to N	90	Pass
-500	120	L to N	90	Pass
+500	120	L to N	0	Pass
-500	120	L to N	0	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	120	L to N	90	Pass
-2500	120	L to N	90	Pass
+2500	120	L to N	0	Pass
-2500	120	L to N	0	Pass

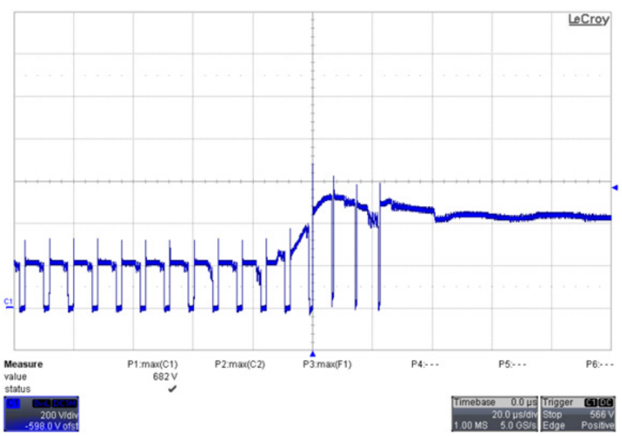

Figure 42 – Differential Line Surge at 500 V / 90°. Peak Drain Voltage Recorded is 682 V. Unit Enters Auto-Restart but No Damage.
Ch1: V_{DRAIN}, 200 V / div.
Time Scale: 20 µs / div.

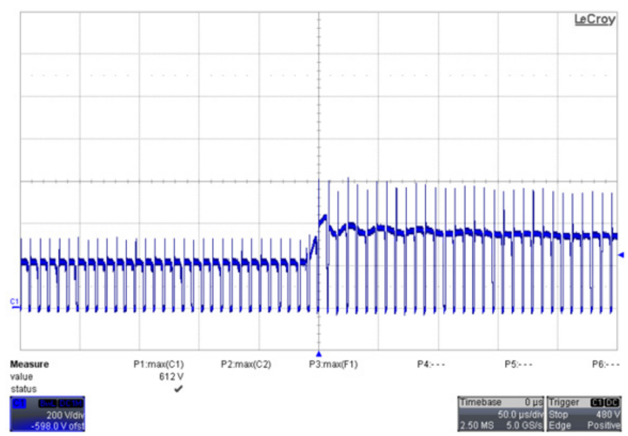

Figure 43 – Differential Ring Surge at 2500 V / 90°. Peak Drain Voltage Recorded is 612 V.
Ch1: V_{DRAIN}, 200 V / div.
Time Scale: 50 µs / div.

13 Conducted EMI

13.1 Test Set-up

The LED driver was first placed inside a GU10 assembly with ~9 V LED Load and then placed inside a cone.

Figure 44 – Conducted EMI Test Set-up.

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13.2 Test Result

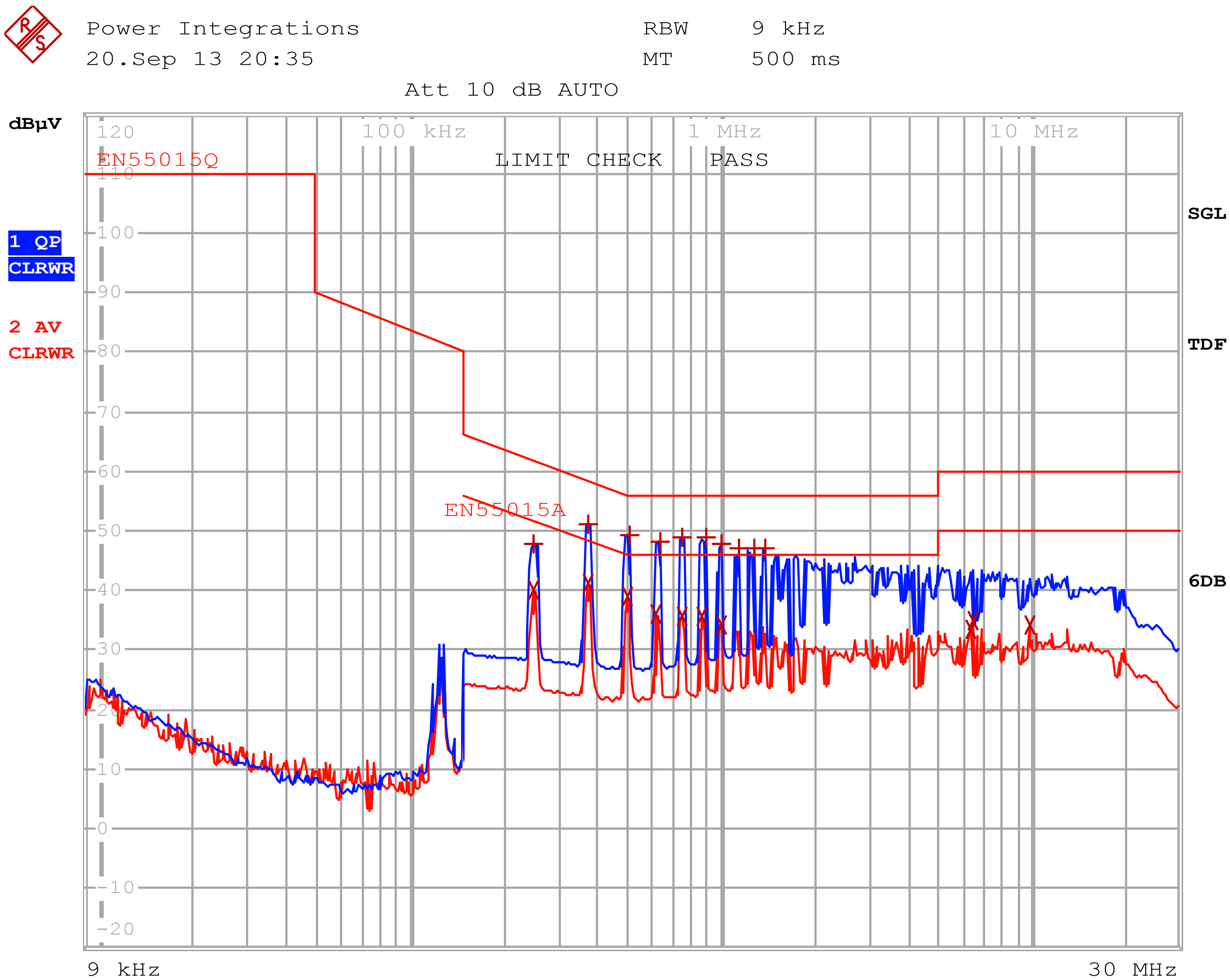

Figure 45 – Conducted EMI, Maximum Steady-State Load, 115 VAC, 60 Hz, and EN55015 B Limits.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	246.694773277 kHz	47.80	L1 gnd	-14.06
2	Average	249.161721009 kHz	40.20	N gnd	-11.57
1	Quasi Peak	370.967850209 kHz	51.09	L1 gnd	-7.38
2	Average	374.677528711 kHz	41.25	N gnd	-7.14
2	Average	495.058034186 kHz	39.09	L1 gnd	-6.98
1	Quasi Peak	505.008700673 kHz	49.22	L1 gnd	-6.77
2	Average	616.206586648 kHz	36.07	N gnd	-9.92
1	Quasi Peak	634.878262431 kHz	48.31	L1 gnd	-7.68
2	Average	744.444692652 kHz	35.82	N gnd	-10.17
1	Quasi Peak	751.889139579 kHz	48.80	L1 gnd	-7.19
2	Average	864.277177159 kHz	35.48	N gnd	-10.51
1	Quasi Peak	890.465639904 kHz	48.96	L1 gnd	-7.03
2	Average	993.464328234 kHz	34.14	L1 gnd	-11.85
1	Quasi Peak	1.00339897152 MHz	47.70	L1 gnd	-8.29
1	Quasi Peak	1.13065507631 MHz	46.91	L1 gnd	-9.08
1	Quasi Peak	1.27405044044 MHz	47.12	L1 gnd	-8.87
1	Quasi Peak	1.37961406273 MHz	47.11	L1 gnd	-8.88
2	Average	6.3862979296 MHz	33.29	N gnd	-16.70
2	Average	6.51466251798 MHz	35.11	N gnd	-14.88
2	Average	9.89440359926 MHz	34.35	N gnd	-15.64

Figure 46 – Conducted EMI Final Measurements, Maximum Steady-State Load, 115 VAC, 60 Hz, and EN55015 B Limits.

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
05-Dec-13	CA	1.0	Initial Release	Apps & Mktg

For the latest updates, visit our website: www.powerint.com

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