



Design Example Report

Title	12.8 W Constant Current, High Power Factor (>0.9) Tapped Buck LED Driver Using LinkSwitch™-PH LNK414EG
Specification	140 VAC – 280 VAC Input; 16 V, 800 mA Output
Application	Down Light LED Driver
Author	Applications Engineering Department
Document Number	DER-344
Date	October 19, 2012
Revision	1.0

Summary and Features

- Highly energy efficient
 - ≥85% at 230 VAC
- High power factor, >0.95 typical
- Low THD <15% at 230 VAC, easily meets IEC 61000-3-2 Class C and D
- Low cost, low component count and small single-sided printed circuit board
 - Frequency jitter for smaller, lower cost EMI filter
 - Uses low cost EE16 core
- Integrated protection and reliability features
 - Output short-circuit protected with auto-recovery
 - Line input overvoltage shutdown extends voltage withstand during line faults
 - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
- IEC 61000-4-5, and EN55015 B conducted EMI compliant

PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a non-isolated high power factor (PF) LED driver designed to drive a nominal LED string voltage of 16 V at 800 mA from an input voltage range of 140 VAC to 280 VAC. The LED driver utilizes the LNK414EG from the LinkSwitch-PH family of ICs.

The topology used is a single-stage non-isolated continuous mode tapped buck (combined PFC and CC in a single switching stage).

High power factor and low THD is achieved by employing the LinkSwitch-PH IC which also provides a sophisticated range of protection features including auto-restart for open control loop and output short-circuit conditions. Integrated line overvoltage protection provides extended line fault and surge withstand.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.



Figure 1 – Populated Circuit Board Photograph.



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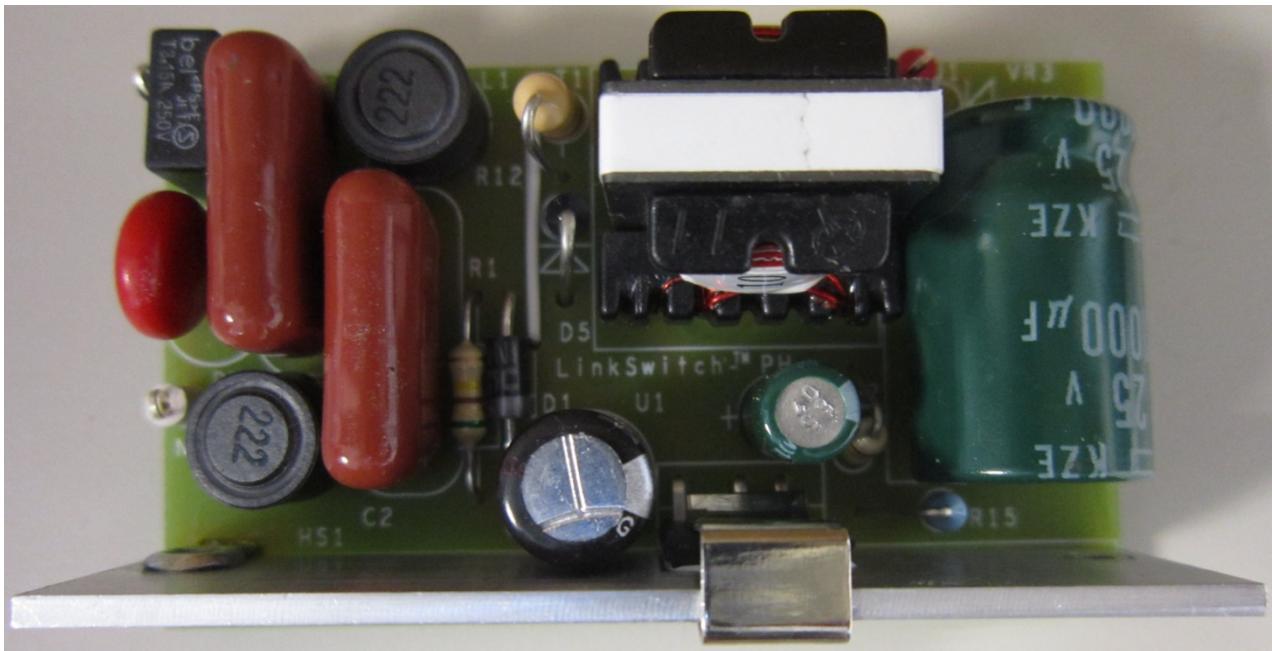


Figure 2 – Populated Circuit Board Photograph (Top View).

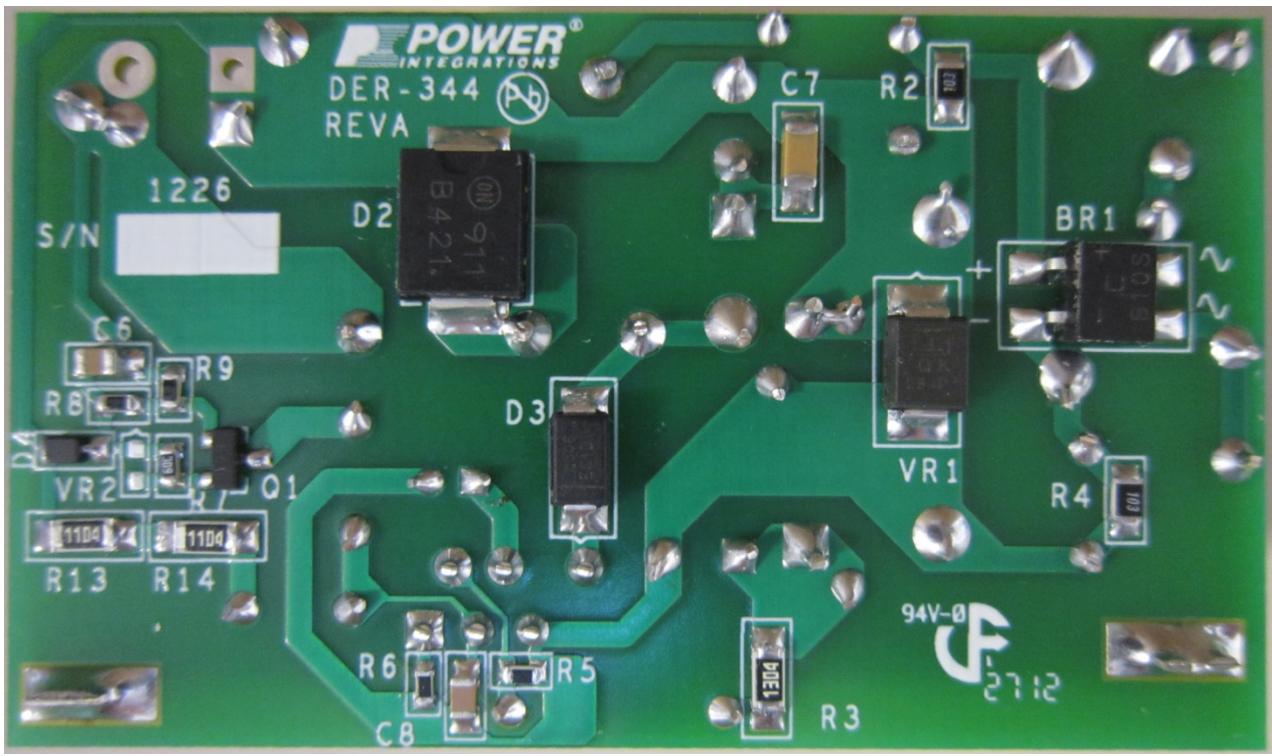


Figure 3 – Populated Circuit Board Photograph (Bottom View).



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input Voltage Frequency	V_{IN} f_{LINE}	140	230 50/60	280	VAC Hz	2 Wire – no P.E.
Output Output Voltage Output Current	V_{OUT} I_{OUT}	15	16 800	17	V mA	$V_{OUT} = 16$ V, $V_{IN} = 230$ VAC, 25°C
Total Output Power Continuous Output Power	P_{OUT}		12.8		W	
Efficiency Full Load	η	84	85		%	$V_{OUT} = 16$ V, $V_{IN} = 230$ VAC, 25°C
Environmental Conducted EMI Safety Ring Wave (100 kHz) Differential Mode (L1-L2) Common Mode (L1/L2-PE)			CISPR 15B / EN55015B Non-Isolated 2.5		kV	
Differential Surge			2		kV	
Power Factor			0.95			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents			EN 61000-3-2 Class C			Class C specifies Class D Limits when $P_{IN} < 25$ W
Ambient Temperature	T_{AMB}		60		°C	Free convection



3 Schematic

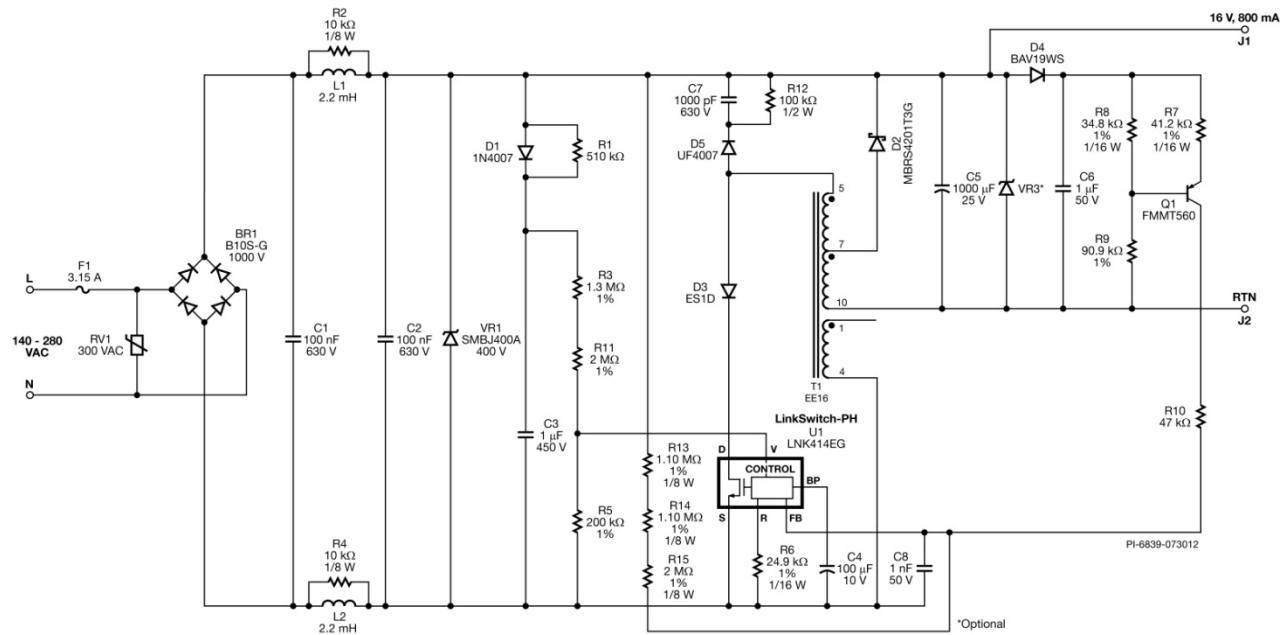


Figure 4 – Schematic.

Note: VR3 is an optional component for open load protection.



4 Circuit Description

The LinkSwitch-PH device is a controller with an integrated 725 V power MOSFET for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage continuous conduction mode tapped buck topology and provides a regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 provides protection from component failure and RV1 provides a clamp to limit the maximum voltage during differential line surge events. A 300 VAC rated part was selected, being slightly above the maximum specified operating voltage of 280 VAC. TVS VR1 was also added since the maximum clamping voltage of RV1 (~775 V) was above the maximum drain to source voltage rating of U1. VR1 was selected to have a clamping voltage (~650 V) below the maximum drain to source voltage rating of U1.

Diode bridge BR1 rectifies the AC line voltage with capacitor C2 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C1 and C2) is necessary to maintain a power factor of greater than 0.9.

EMI filtering is provided by inductors L1 and L2, and capacitors C1 and C2. Resistor R2 and R4 across L1 and L2 damp any LC resonances due to the filter components and the AC line impedance which would ordinarily show up on the conducted EMI measurements.

4.2 Power Circuit and LinkSwitch-PH External Components

The topology chosen in this design is a low-side tapped buck configured to provide low THD, unity power factor, and constant current output for the input voltage range of 140 VAC to 280 VAC

The tapped buck converter offers the advantage of reduced magnetic component size, reduced current stress on the main switch U1, and reduced voltage stress on the output diode D2. The reduced current stress on the main switch enables the use of a smaller LinkSwitch-PH device for more cost effectiveness of the design. The lower voltage stress on the output diode enables the use of low V_F (Schottky) device for improved efficiency.

Transformer T1 is the main inductor of the buck converter. It consists of two windings, primary and secondary windings. The ratio is chosen to be 2:1 (primary to secondary ratio) to enable the use of a 200 V output diode while keeping the maximum voltage of U1 LNK414EG still well below its maximum value. The inductance is chosen to keep the operation in CCM in order to reduced RMS currents and at the same time meet Class C harmonic limits.

Output Diode D2 conducts every time U1 is off and transfers energy to the load. Diode D3 is necessary to prevent reverse current from flowing through U1 while the voltage



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across C2 (rectified input AC) falls below the output voltage. A voltage clamp circuit was also added to limit voltage spike created by the leakage inductance of T1. The clamp network is formed by diode D5, capacitor C7, and resistor R12.

To provide peak line voltage information to U1, the incoming rectified AC peak charges C3 via D1. This is then fed into the VOLTAGE MONITOR (V) pin of U1 as a current via R3, and R11. The combination of R3, R11, and R5 centers the operating input voltage range from 90 VAC (brown-in) to 298 VAC (OVP) typical.

The line overvoltage shutdown function, sensed via the V pin current, extends the rectified line voltage withstand (during surges and line swells) to the 725 BV_{DSS} rating of the internal power MOSFET.

Capacitor C4 provides local decoupling for the BYPASS pin of U1 which is the supply pin for the internal controller. During start-up, C8 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN pin of U1. Capacitor C4 is also chosen to be 100 μ F to enable the device to operate on the full power mode.

The REFERENCE pin of U1 is tied to ground (SOURCE) via resistor R6. A 24.9 k Ω value is used for non-dimming application.

4.3 I_{FB} Feedback and Line Compensation

The total feedback current fed into the FEEDBACK pin of U1 is the sum of the output voltage feedback current and line compensation current.

The FEEDBACK pin current used by U1 for output voltage feedback is provided by the voltage to current converter network formed by R7-R10, Q1, C6, and D4. Output voltage is converted to feedback current by the following relation:

$IFB \approx k * Vout$ where

$$k = \frac{1}{R7} * \frac{R8}{R8 + R9}$$

THD line compensation was also added to increase margin on odd harmonics from the Class C limit. A current proportional to the rectified line input voltage was fed to the FB pin thru resistors R13, R14, and R15.

The feedback current coming from Q1 at typical output voltage of 16 V is ~91 μ A. The line compensation network formed by resistors R13, R14, and R15 add a dc offset of ~28 μ A to ~57 μ A from input voltage of 140 VAC to 280 VAC. This makes the operating I_{FB} to be in the range of ~119 μ A to ~148 μ A. It should also be noted that peak instantaneous I_{FB} current which occurs at the highest input and output voltage should not reach the $I_{FB(SKIP)}$ specifications of the device. In this design, at 280 VAC input and 17 V output,

peak I_{FB} current is $\sim 187 \mu\text{A}$. This is well below the minimum $I_{FB(\text{SKIP})}$ of $220 \mu\text{A}$ of the device.

4.4 Open Load and Short Circuit Protection

The unit is not designed to operate under no load condition. In case of accidental open load condition during evaluation, a Zener diode VR3 can be placed to clamp the output voltage. This diode should fail short in case of open load condition and the unit will enter the short circuit condition.

The presence of the line compensation prevents the current to fall below $I_{FB(\text{AR})}$ especially at high input voltage conditions during short circuit condition and does not enter the auto-restart operation. The unit is protected by the SOA protection mode of the device. SOA protection mode disables FET switching for 40 cycles in the event the peak switch current reaches the I_{LIMIT} threshold and the switch on-time is less than $t_{\text{ON(SOA)}}$. The figure below shows the drain voltage and current of U1 (LNK414EG) during output short condition at 280 VAC input.

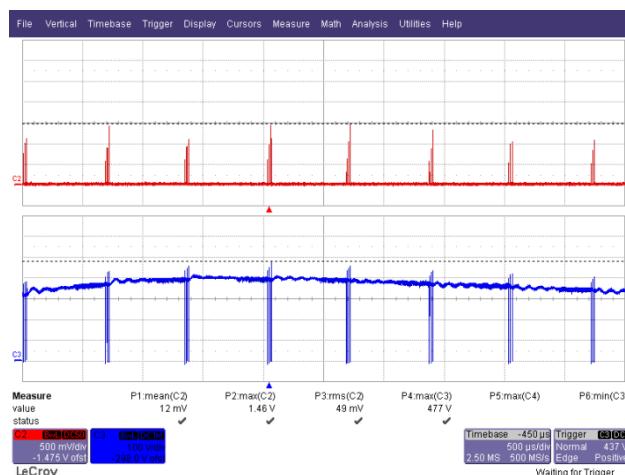


Figure 5 – 280 VAC Output Short Condition Showing SOA Protection Mode Operation.

C2: Drain Current, 500 mA / div., 500 μs / div.;

C3: Drain Voltage, 100 V / div., 500 μs / div.

The unit is also placed inside the chamber with output shorted, 280 VAC, 60 Hz input, and 60°C ambient temperature. Maximum temperature of 91.4°C was measured on the output diode D2. Refer to Section 10.5, Figure 24 for the other components thermal measurements during this condition. The device stress and external components stayed within rated specifications during short circuit condition.



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5 PCB Layout

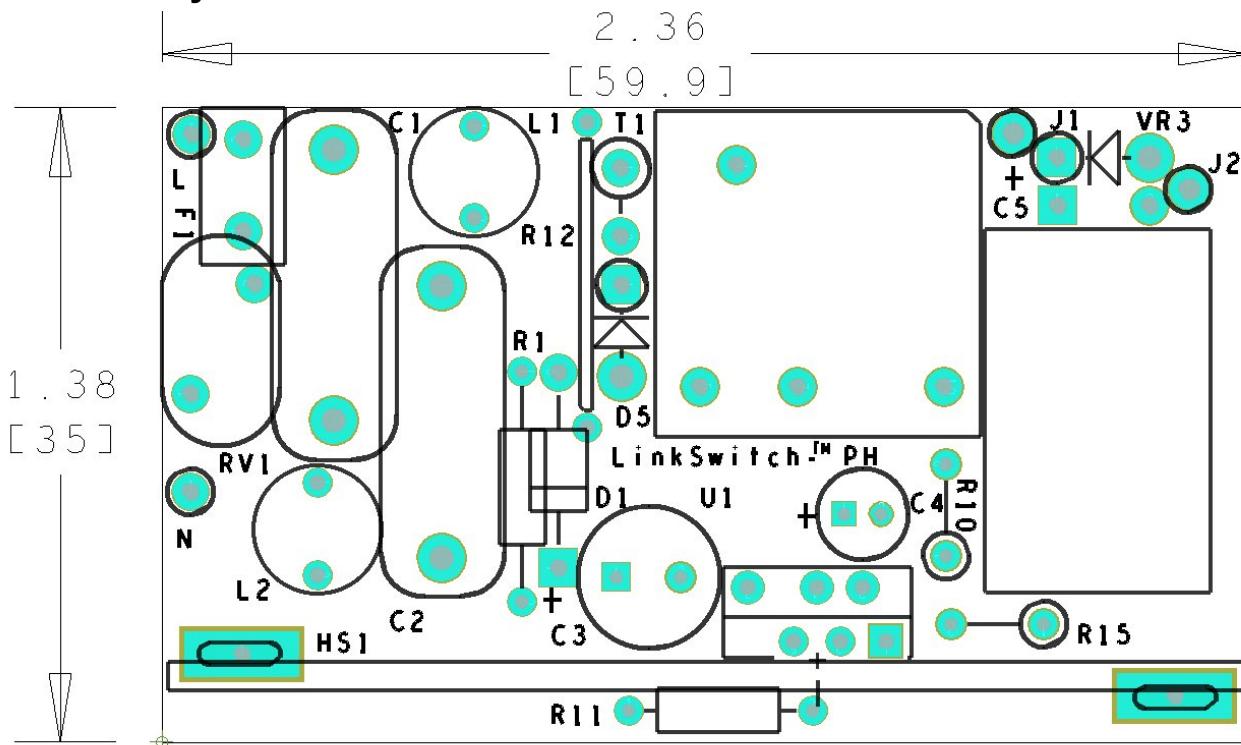
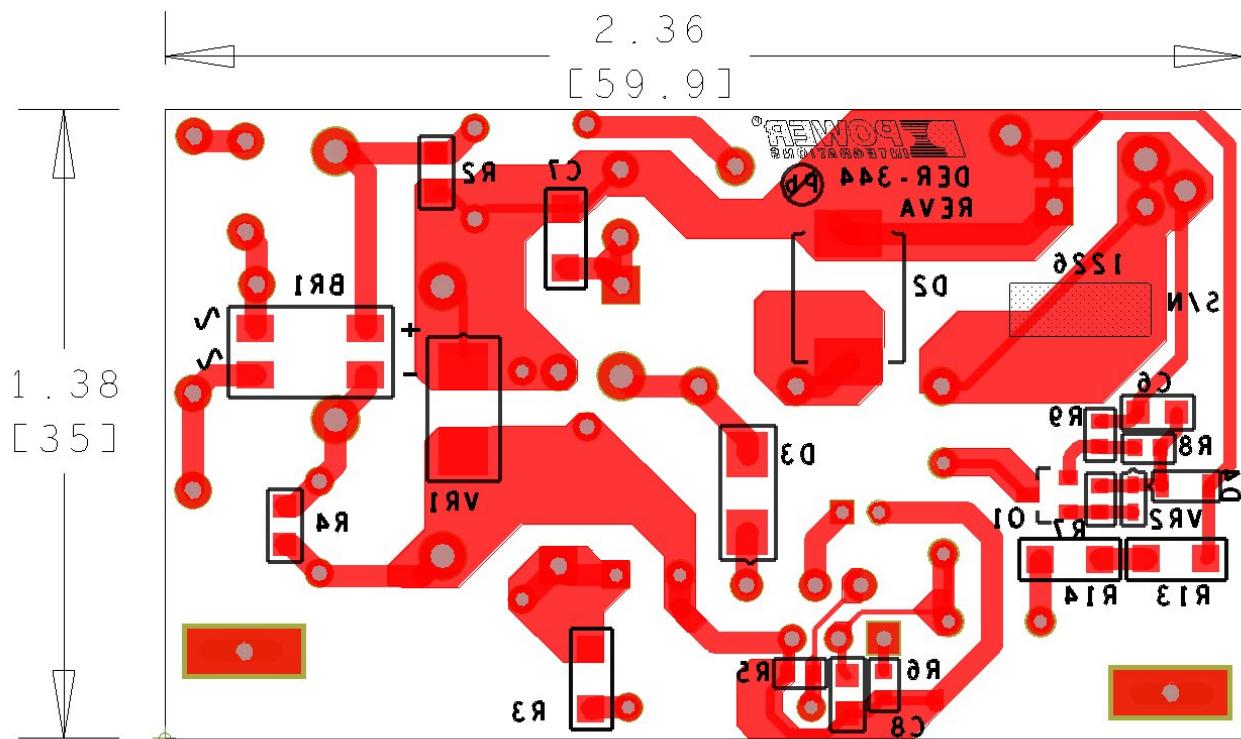


Figure 6 – PCB Layout and Outline, Top Side (in / [mm]).



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	2	C1 C2	100 nF, 630 V, Film	ECQ-E6104KF	Panasonic
3	1	C3	1.0 µF, 450 V, Electrolytic, NHG, (8 x 11.5)	ECA-2WHG010	Panasonic
4	1	C4	100 µF, 10 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE100ELL101ME11D	Nippon Chemi-Con
5	1	C5	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	EKZE250ELL102MK20S	Nippon Chemi-Con
6	1	C6	1 µF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
7	1	C7	1000 pF, 630 V, Ceramic, X7R, 1206	ECJ-3FB2J102K	Panasonic
8	1	C8	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
9	1	D1	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
10	1	D2	200 V, 4 A, Schottky, SMC, DO-214AB	MBRS4201T3G	ON Semi
11	1	D3	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D	Vishay
12	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
13	1	D5	1000 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4007-E3	Vishay
14	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
15	2	L1 L2	2.2 mH, 0.16 A, Ferrite Core	CTSCH875DF-222K	CT Parts
16	1	Q1	PNP, Small Signal BJT, 500 V, 0.15 A, SOT23	FMMT560TA	Zetex
17	1	R1	510 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-510K	Yageo
18	2	R2 R4	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
19	1	R3	1.30 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1304V	Panasonic
20	1	R5	200 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2003V	Panasonic
21	1	R6	24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
22	1	R7	41.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4122V	Panasonic
23	1	R8	34.8 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3482V	Panasonic
24	1	R9	90.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9092V	Panasonic
25	1	R10	47 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-47K	Yageo
26	2	R11 R15	2.00 MΩ, 1%, 1/4 W, Metal Film	RNF14FTD2M00	Stackpole
27	1	R12	100 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-100K	Yageo
28	2	R13 R14	1.10 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1104V	Panasonic
29	1	RV1	300 V, 25 J, 7 mm, RADIAL	V300LA4P	Littlefuse
30	1	T1	Bobbin, EE16, Vertical, 10 pins (4 x 6)	EL-16 (YW-193-02B)	Yih-Hwa Enterprises
31	1	U1	LinkSwitch-PH, eSIP	LNK414EG	Power Integrations
32	1	VR1	400 V, 600 W, 5%, DO214AC (SMB)	SMBJ400A	Littlefuse
33	1	HS1	Heat Sink, Custom, Al, 3003, 0.062" Thk		Custom



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7 Transformer Specification

7.1 Electrical Diagram

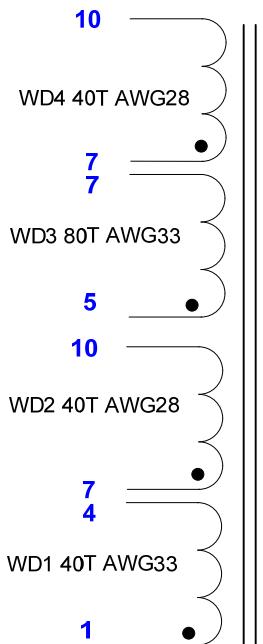


Figure 8 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 5-10 all other windings open, measured at 66 kHz, 0.4 V _{RMS}	900 μ H $\pm 7\%$
Resonant Frequency	Pins 5-10, all other windings open	0.7 MHz (Min.)

7.3 Materials

Item	Description
[1]	Core: PC44 EE16 Z
[2]	Bobbin: B-EE16-V-10 ins (4/6)
[3]	Magnet Wire, #28 AWG, solderable double coated.
[4]	Magnet Wire, #33 AWG, solderable double coated.



7.4 Inductor Build Diagram

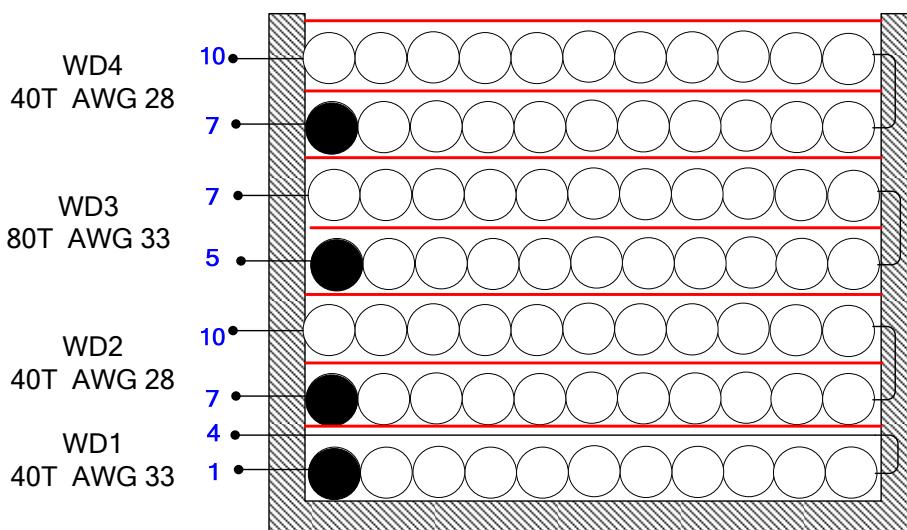


Figure 9 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left.
WD1	Start at pin 1. Wind 40 turns of item [4] as shown in Figure 2. Terminate at pin 4.
WD2	Start at pin 7. Wind 40 turns of item [3] and terminate the other end at pin 10.
WD3	Start at pin 5. Wind 80 turns of item [4] as shown in Figure 2. Terminate at pin 7.
WD4	Start at pin 7. Wind 40 turns of item [3] and terminate the other end at pin 10.
Finish	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 1, 2, 3, 6, and 9.



8 LNK414EG (U1) Heat Sink Assembly

8.1 Heat Sink Fabrication Drawing

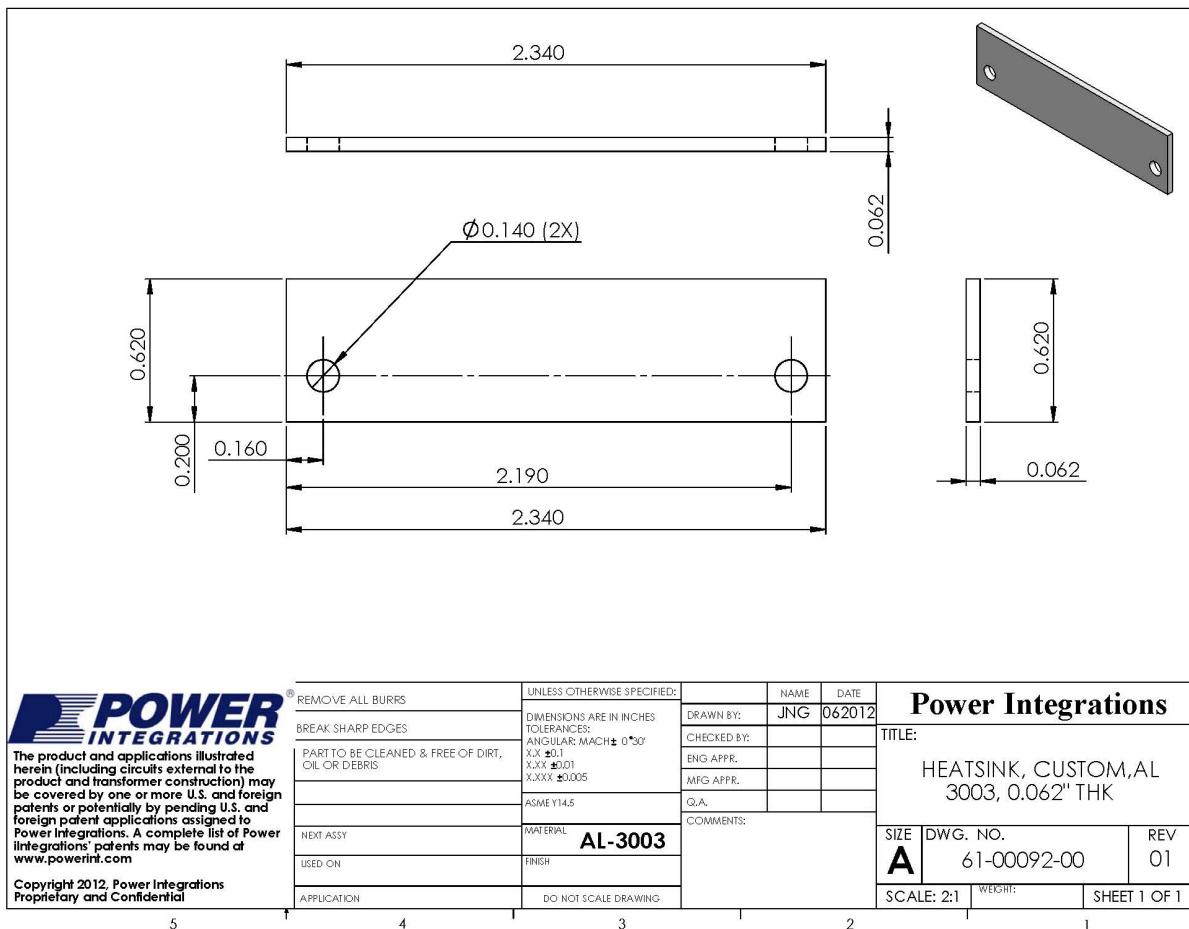


Figure 10 – Heat Sink Dimensions.



8.2 Heat Sink Assembly Drawing

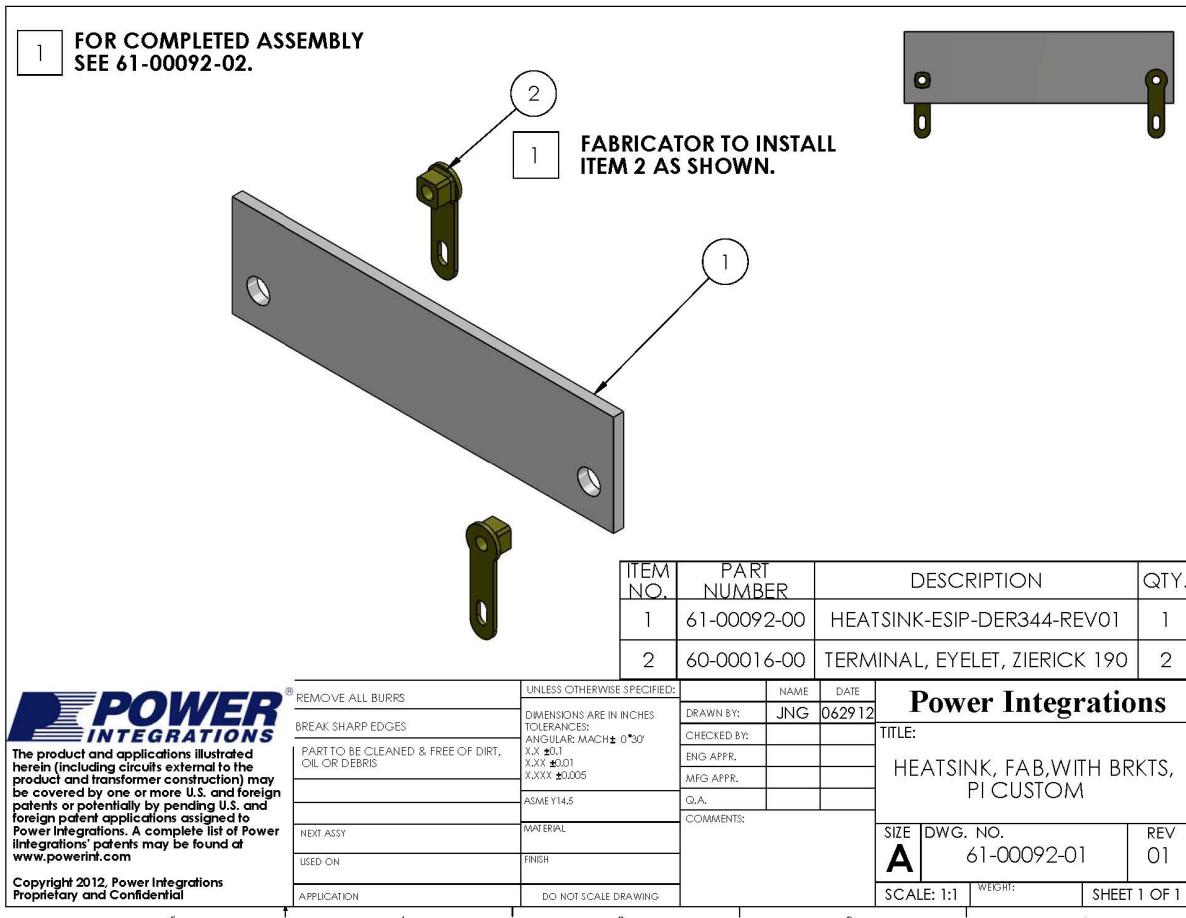


Figure 11 – Heat Sink Assembly Drawing.



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8.3 LNK414EG (U1) and Heat Sink Assembly Drawing.

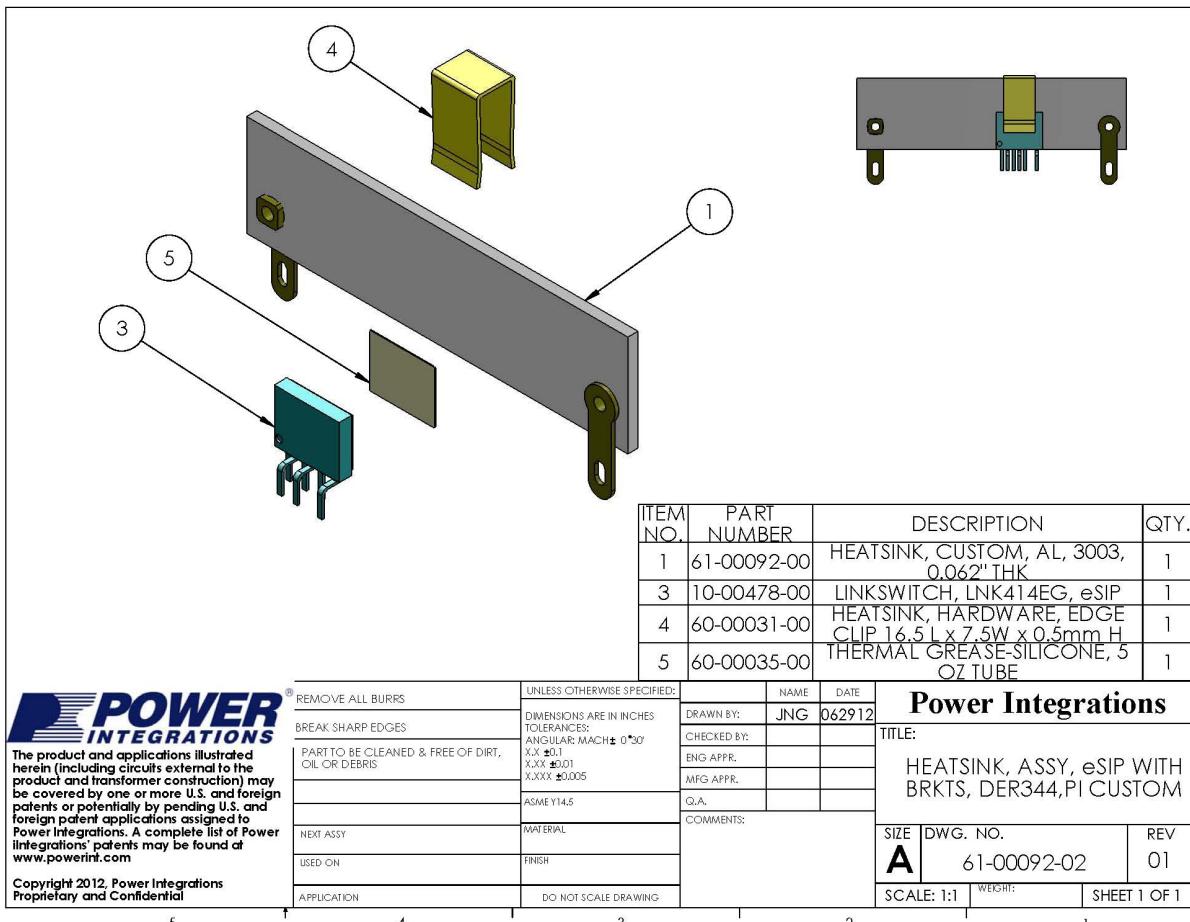


Figure 12 – LNK414EG (U1) and Heat Sink Assembly Drawing.



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9 Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent a voltage of 15 V ~ 17 V. The table in Section 9.6 shows complete test data values.

9.1 Efficiency

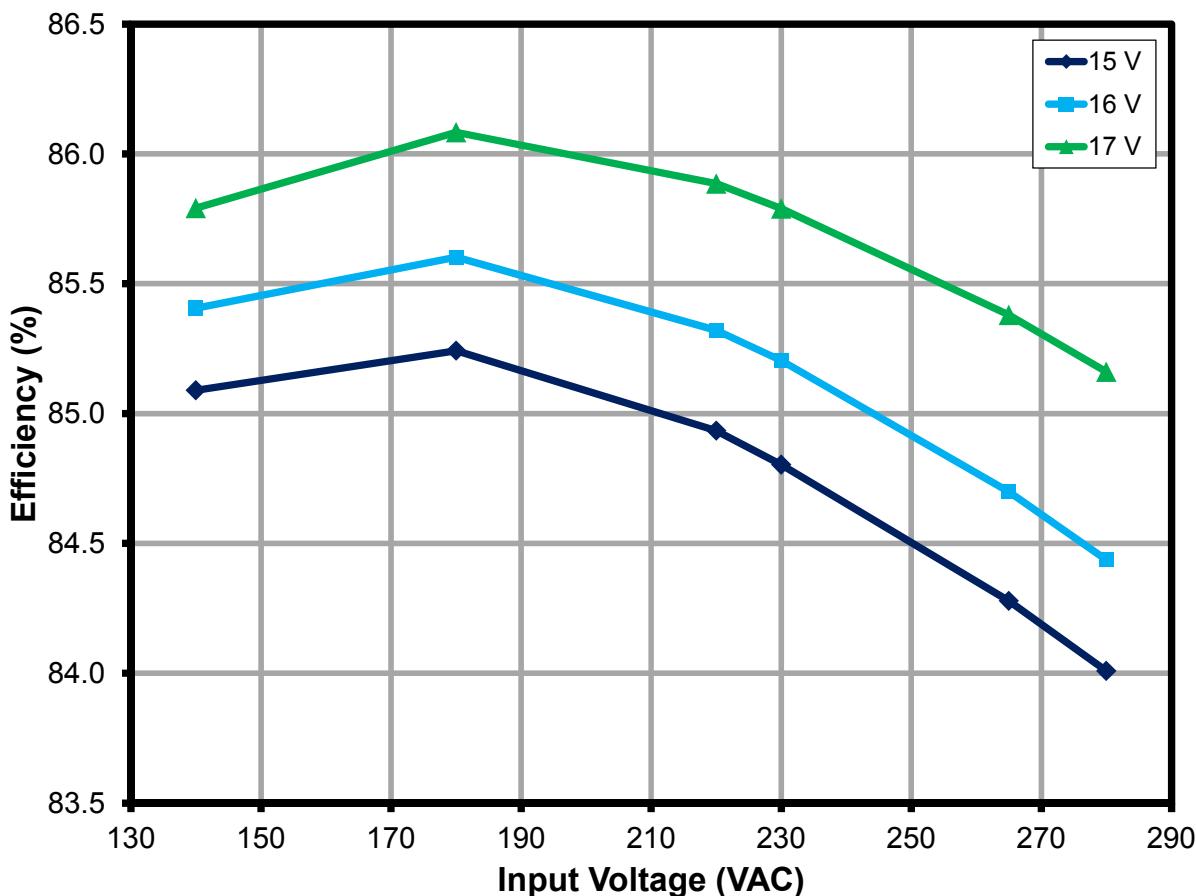


Figure 13 – Efficiency vs. Line and Load.



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9.2 Line and Load Regulation

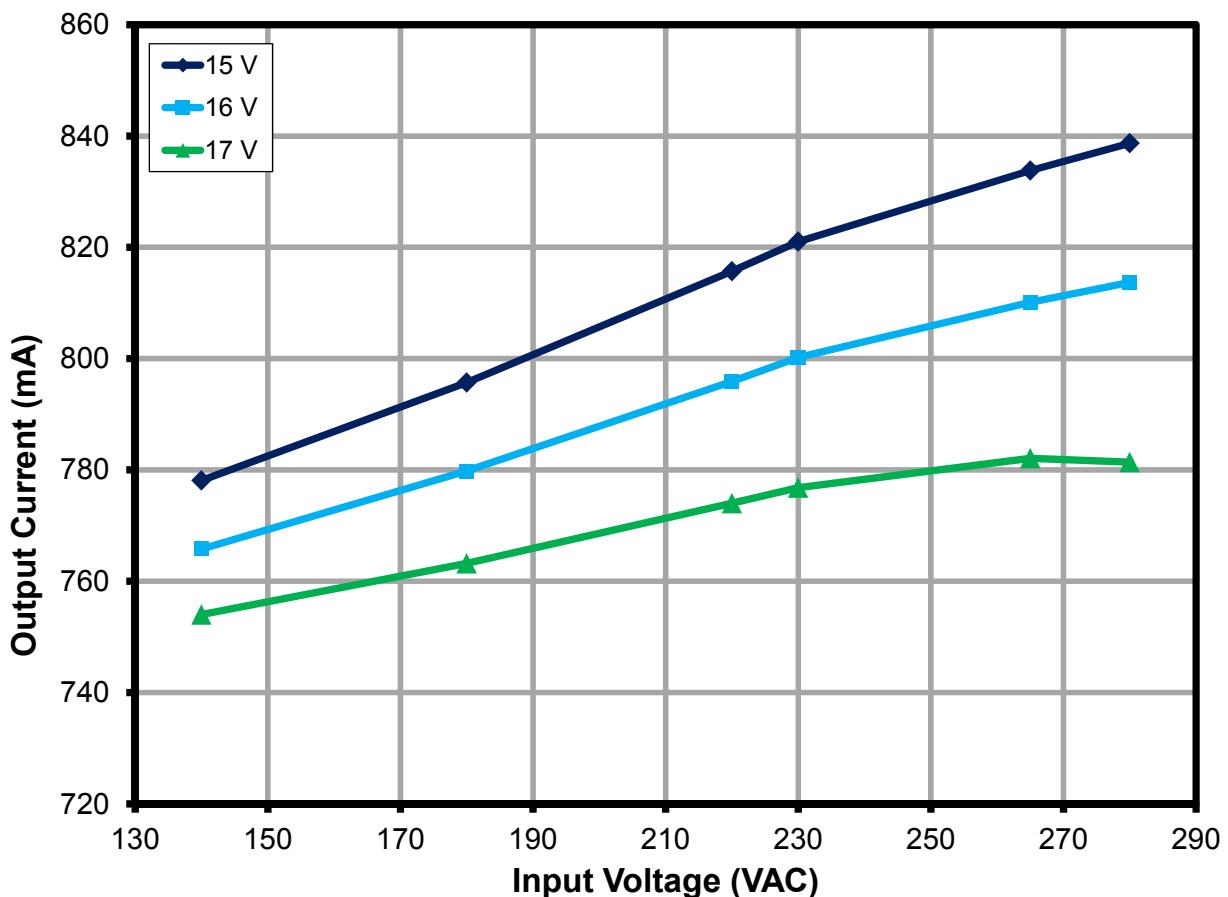


Figure 14 – Regulation vs. Line and Load.

9.3 Power Factor

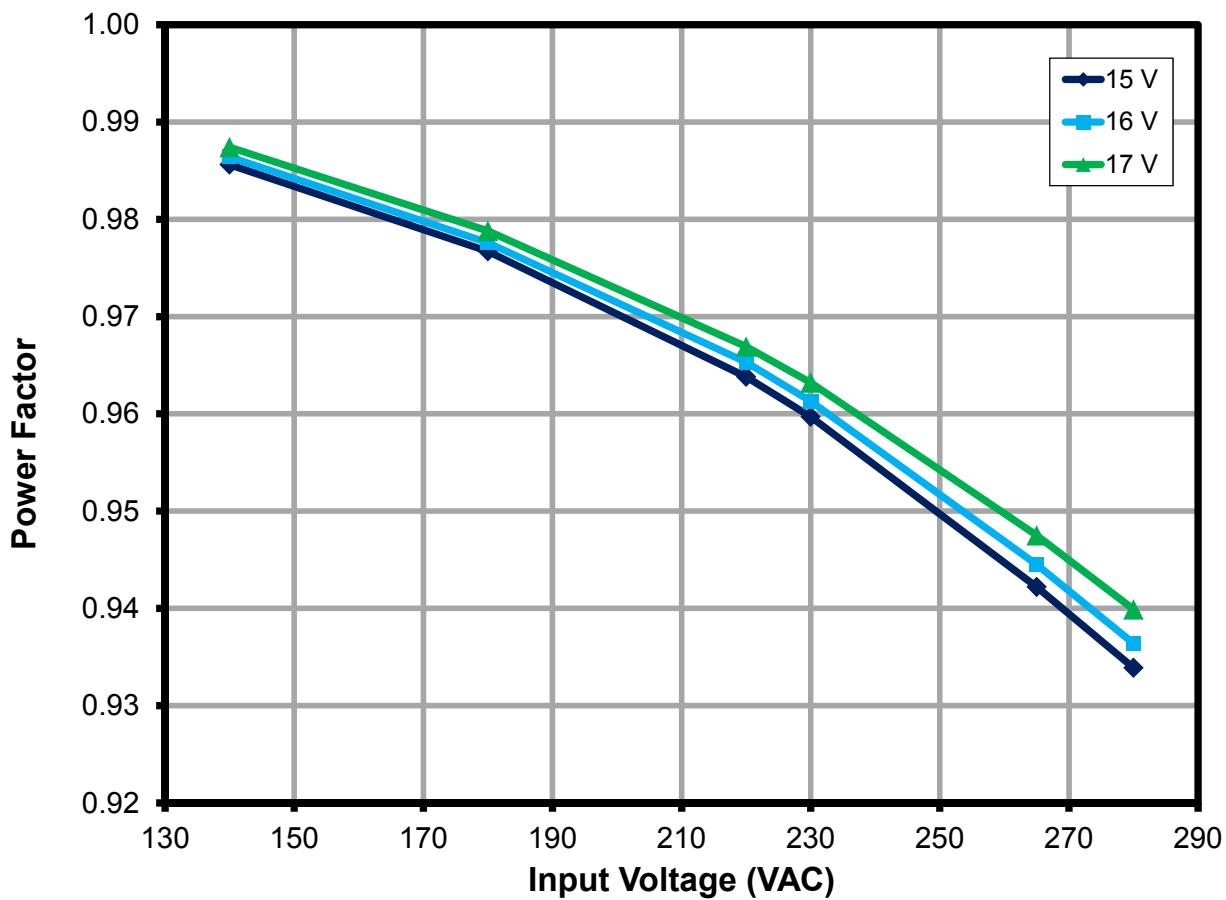


Figure 15 – Power Factor vs. Line and Load.



9.4 A-THD

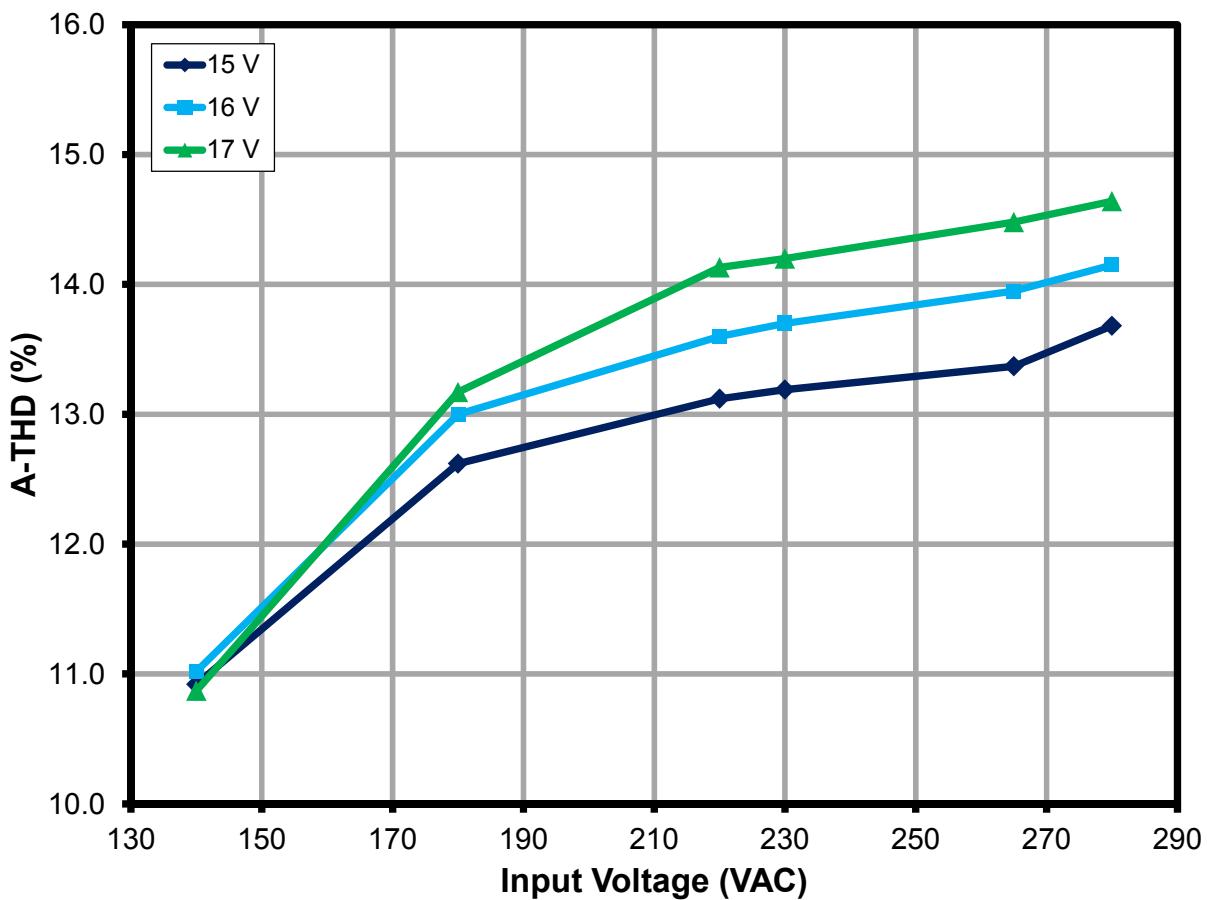


Figure 16 – A-THD vs. Line and Load.



9.5 Harmonic Currents

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment¹. Therefore the limits shown in the charts below are Class D limits which must not be exceeded to meet Class C compliance.

9.5.1 15 V LED Load

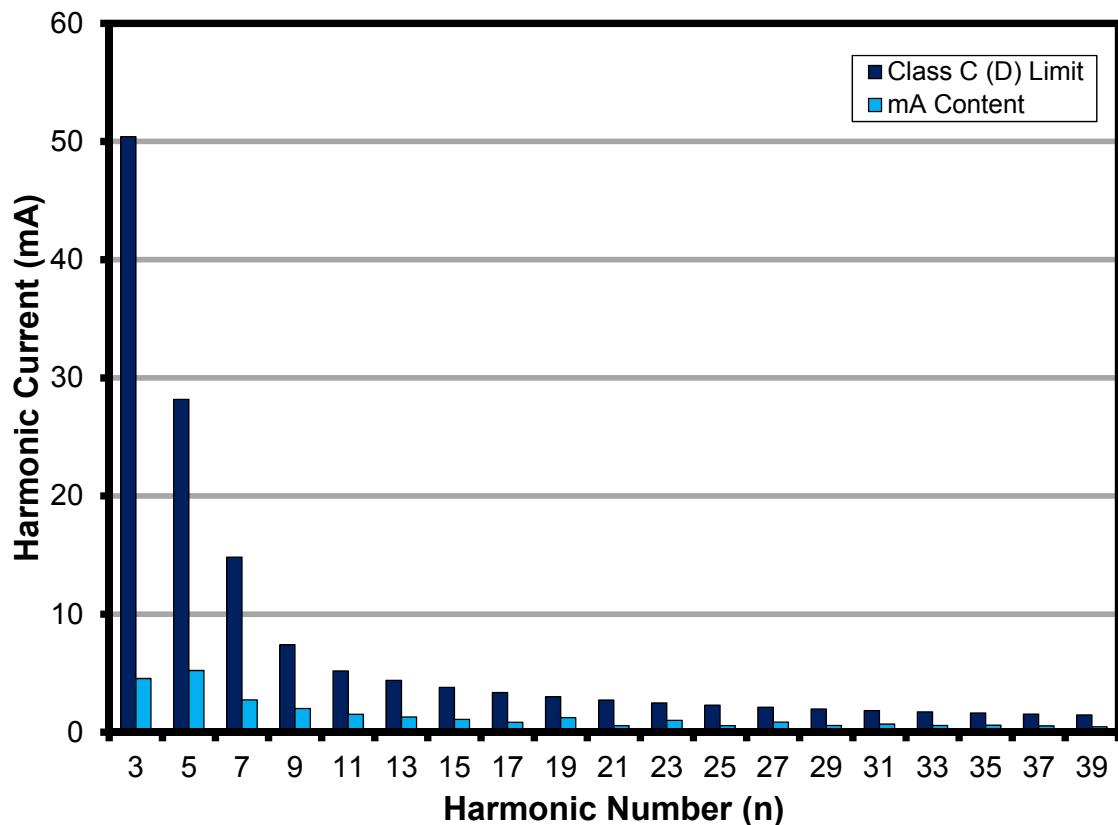


Figure 17 – 15 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

¹ IEC6000-3-2 Section 7.3, table 2, column 2.



9.5.3 16 V LED Load

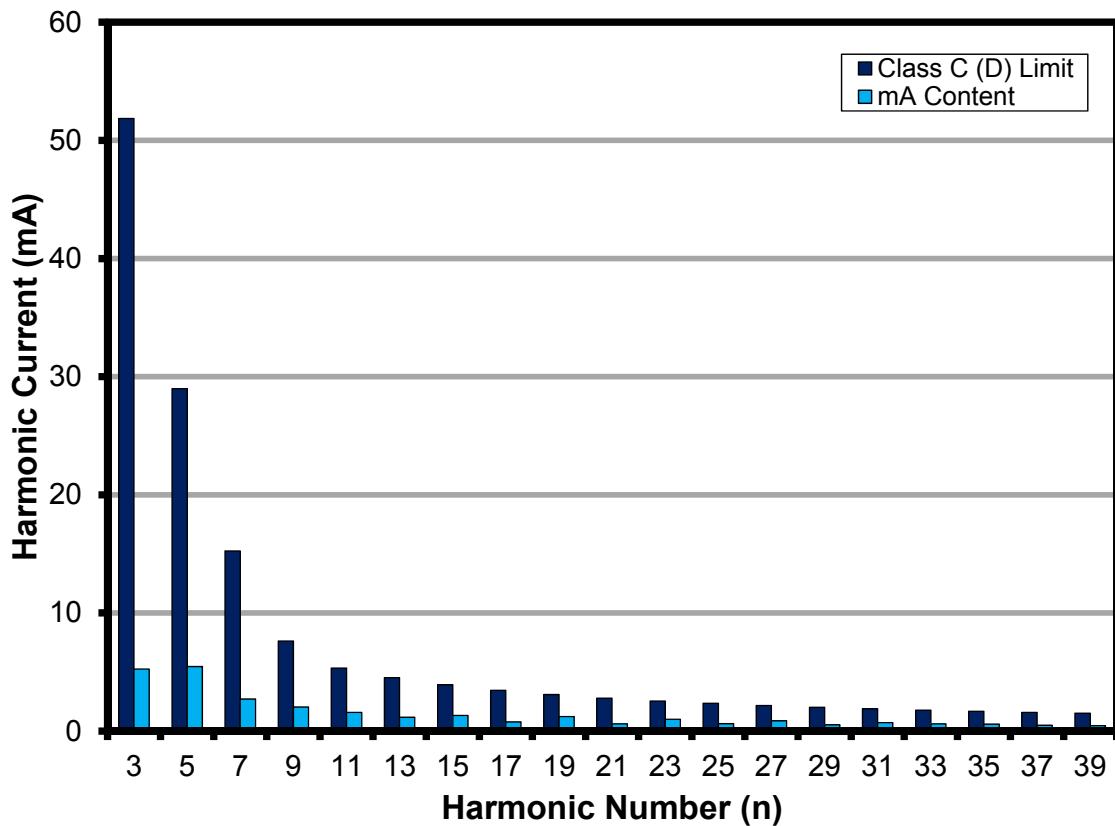


Figure 18 – 16 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

9.5.4 17 V LED Load

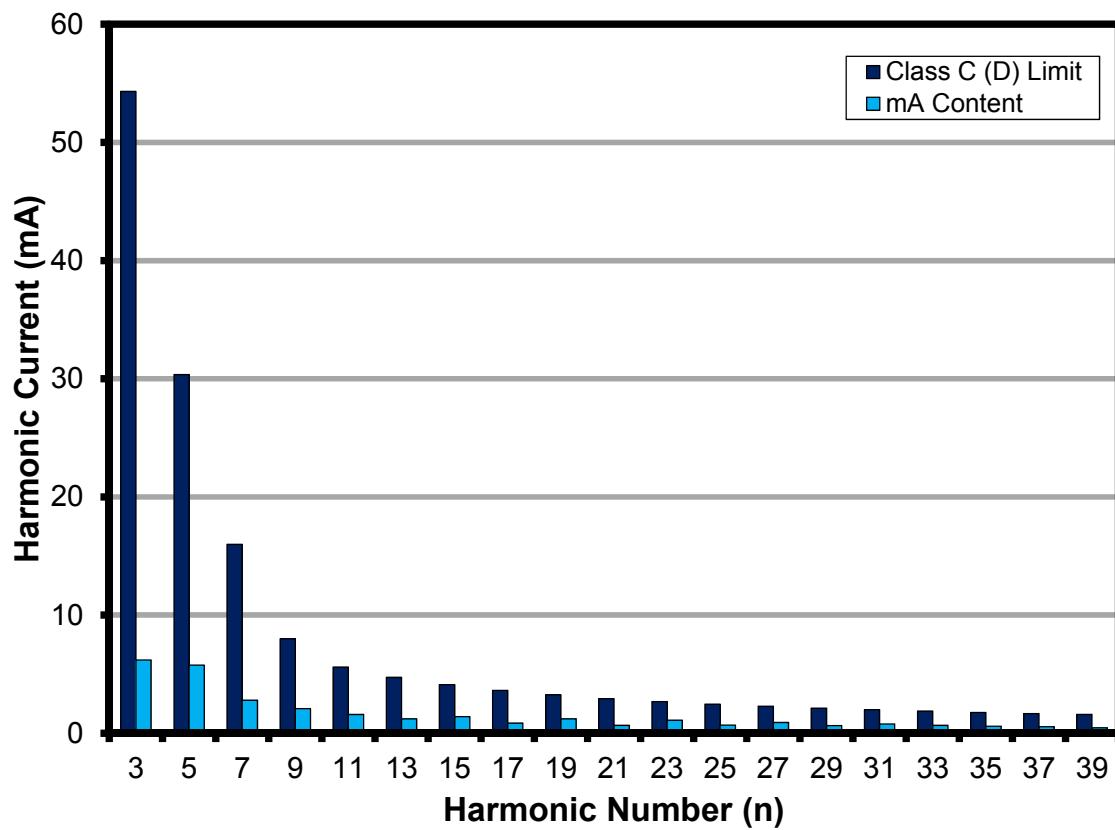


Figure 19 – 17 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.



9.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient.

9.6.1 Test Data, 15 V LED Load

Input Measurement					Load Measurement			Calculation		
V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
140.06	101.00	13.943	0.986	10.92	15.02	778.10	11.86	11.69	85.09	2.08
180.08	81.06	14.257	0.977	12.62	15.05	795.70	12.15	11.97	85.24	2.10
220.12	69.30	14.702	0.964	13.12	15.07	815.70	12.49	12.29	84.93	2.22
230.18	67.11	14.825	0.960	13.19	15.08	821.00	12.57	12.38	84.80	2.25
265.16	60.72	15.170	0.942	13.37	15.09	833.80	12.79	12.58	84.28	2.39
280.20	58.53	15.315	0.934	13.68	15.09	838.70	12.87	12.66	84.01	2.45

9.6.2 Test Data, 16 V LED Load

Input Measurement					Load Measurement			Calculation		
V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
140.06	105.09	14.519	0.986	11.02	15.98	765.80	12.40	12.24	85.41	2.12
180.09	83.87	14.766	0.978	13	16.00	779.80	12.64	12.48	85.60	2.13
220.13	71.27	15.144	0.965	13.6	16.02	795.90	12.92	12.75	85.32	2.22
230.18	68.91	15.248	0.961	13.7	16.02	800.20	12.99	12.82	85.20	2.26
265.16	62.05	15.541	0.945	13.95	16.02	810.10	13.16	12.98	84.70	2.38
280.20	59.68	15.659	0.936	14.15	16.02	813.70	13.22	13.04	84.44	2.44

9.6.3 Test Data, 17 V LED Load

Input Measurement					Load Measurement			Calculation		
V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
140.06	111.81	15.462	0.987	10.87	17.39	754.00	13.27	13.11	85.79	2.20
180.08	88.55	15.607	0.979	13.17	17.41	763.20	13.44	13.29	86.08	2.17
220.12	74.63	15.884	0.967	14.13	17.43	774.00	13.64	13.49	85.89	2.24
230.18	72.05	15.974	0.963	14.2	17.45	776.80	13.70	13.55	85.79	2.27
265.16	64.74	16.265	0.948	14.48	17.56	782.10	13.89	13.73	85.38	2.38
280.20	62.23	16.389	0.940	14.64	17.66	781.40	13.96	13.80	85.16	2.43



9.6.4 230 VAC 50 Hz, 15 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	67.11	14.8250	0.9597	13.19
nth Order	mA Content	% Content	Limit <25 W	Limit >25 W	Remarks
1	65.75				
2	0.07	0.11%		2.00%	
3	4.55	6.92%	50.4050	28.79%	Pass
5	5.23	7.95%	28.1675	10.00%	Pass
7	2.75	4.18%	14.8250	7.00%	Pass
9	2.00	3.04%	7.4125	5.00%	Pass
11	1.52	2.31%	5.1888	3.00%	Pass
13	1.30	1.98%	4.3905	3.00%	Pass
15	1.08	1.64%	3.8051	3.00%	Pass
17	0.85	1.29%	3.3574	3.00%	Pass
19	1.24	1.89%	3.0040	3.00%	Pass
21	0.56	0.85%	2.7179	3.00%	Pass
23	1.02	1.55%	2.4816	3.00%	Pass
25	0.56	0.85%	2.2831	3.00%	Pass
27	0.87	1.32%	2.1139	3.00%	Pass
29	0.58	0.88%	1.9681	3.00%	Pass
31	0.70	1.06%	1.8412	3.00%	Pass
33	0.57	0.87%	1.7296	3.00%	Pass
35	0.59	0.90%	1.6308	3.00%	Pass
37	0.55	0.84%	1.5426	3.00%	Pass
39	0.46	0.70%	1.4635	3.00%	Pass
41	0.45	0.68%			
43	0.44	0.67%			
45	0.42	0.64%			
47	0.46	0.70%			
49	0.45	0.68%			



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9.6.5 230 VAC 50 Hz, 16 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	68.91	15.2480	0.9613	13.7
nth Order	mA Content	% Content	Limit <25 W	Limit >25 W	Remarks
1	67.55				
2	0.12	0.18%		2.00%	
3	5.26	7.79%	51.8432	28.84%	Pass
5	5.46	8.08%	28.9712	10.00%	Pass
7	2.71	4.01%	15.2480	7.00%	Pass
9	2.04	3.02%	7.6240	5.00%	Pass
11	1.58	2.34%	5.3368	3.00%	Pass
13	1.18	1.75%	4.5158	3.00%	Pass
15	1.32	1.95%	3.9137	3.00%	Pass
17	0.78	1.15%	3.4532	3.00%	Pass
19	1.22	1.81%	3.0897	3.00%	Pass
21	0.61	0.90%	2.7955	3.00%	Pass
23	1.01	1.50%	2.5524	3.00%	Pass
25	0.62	0.92%	2.3482	3.00%	Pass
27	0.88	1.30%	2.1743	3.00%	Pass
29	0.54	0.80%	2.0243	3.00%	Pass
31	0.73	1.08%	1.8937	3.00%	Pass
33	0.60	0.89%	1.7789	3.00%	Pass
35	0.58	0.86%	1.6773	3.00%	Pass
37	0.49	0.73%	1.5866	3.00%	Pass
39	0.46	0.68%	1.5053	3.00%	Pass
41	0.51	0.75%			
43	0.37	0.55%			
45	0.47	0.70%			
47	0.66	0.98%			
49	0.63	0.93%			



9.6.6 230 VAC 50 Hz, 17 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	72.05	15.9740	0.9632	14.2
nth Order	mA Content	% Content	Limit <25 W	Limit >25 W	Remarks
1	70.57				
2	0.07	0.10%		2.00%	
3	6.19	8.77%	54.3116	28.90%	Pass
5	5.76	8.16%	30.3506	10.00%	Pass
7	2.79	3.95%	15.9740	7.00%	Pass
9	2.07	2.93%	7.9870	5.00%	Pass
11	1.59	2.25%	5.5909	3.00%	Pass
13	1.21	1.71%	4.7308	3.00%	Pass
15	1.39	1.97%	4.1000	3.00%	Pass
17	0.86	1.22%	3.6176	3.00%	Pass
19	1.21	1.71%	3.2368	3.00%	Pass
21	0.67	0.95%	2.9286	3.00%	Pass
23	1.10	1.56%	2.6739	3.00%	Pass
25	0.68	0.96%	2.4600	3.00%	Pass
27	0.91	1.29%	2.2778	3.00%	Pass
29	0.64	0.91%	2.1207	3.00%	Pass
31	0.78	1.11%	1.9839	3.00%	Pass
33	0.66	0.94%	1.8636	3.00%	Pass
35	0.58	0.82%	1.7571	3.00%	Pass
37	0.55	0.78%	1.6622	3.00%	Pass
39	0.46	0.65%	1.5769	3.00%	Pass
41	0.50	0.71%			
43	0.40	0.57%			
45	0.44	0.62%			
47	0.39	0.55%			
49	0.41	0.58%			



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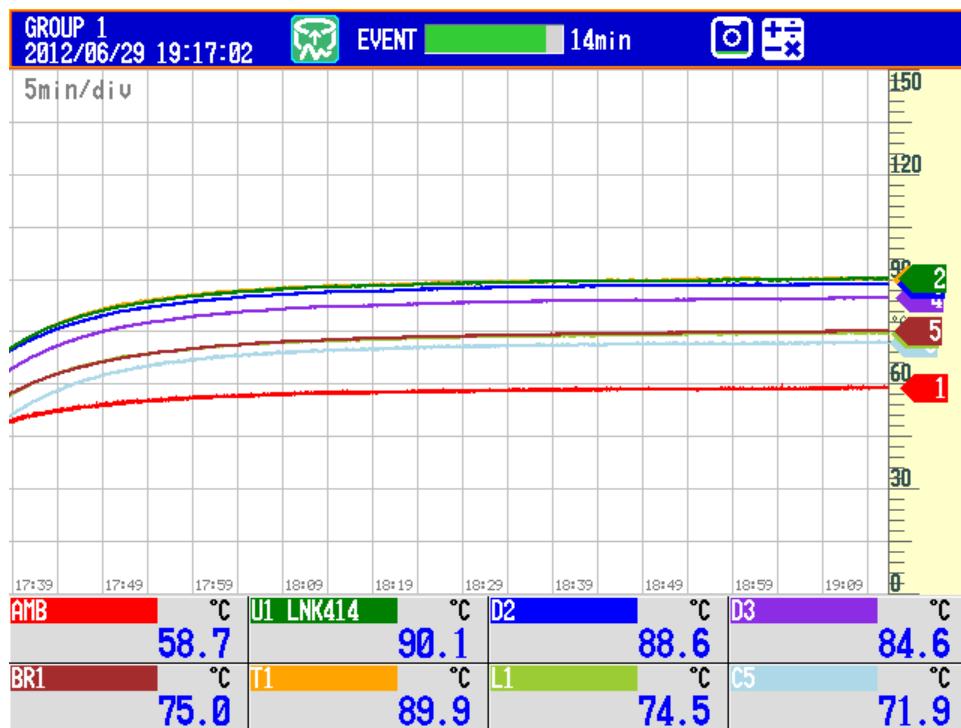
10 Thermal Performance

10.1 Test Set-up

The unit was placed inside a box and in to the chamber for an ambient of ~60°C (ambient inside the box). The box is closed before closing the chamber door to block the thermal chamber fan on blowing air to the unit. Thermal measurements were taken after approximately 1 hour for each line condition.

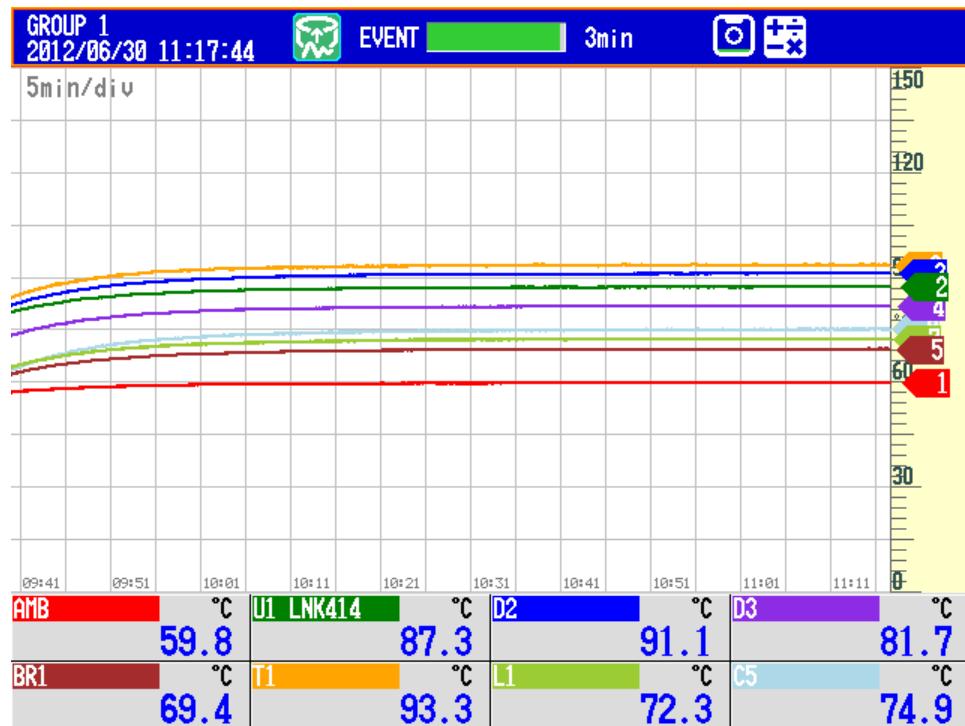


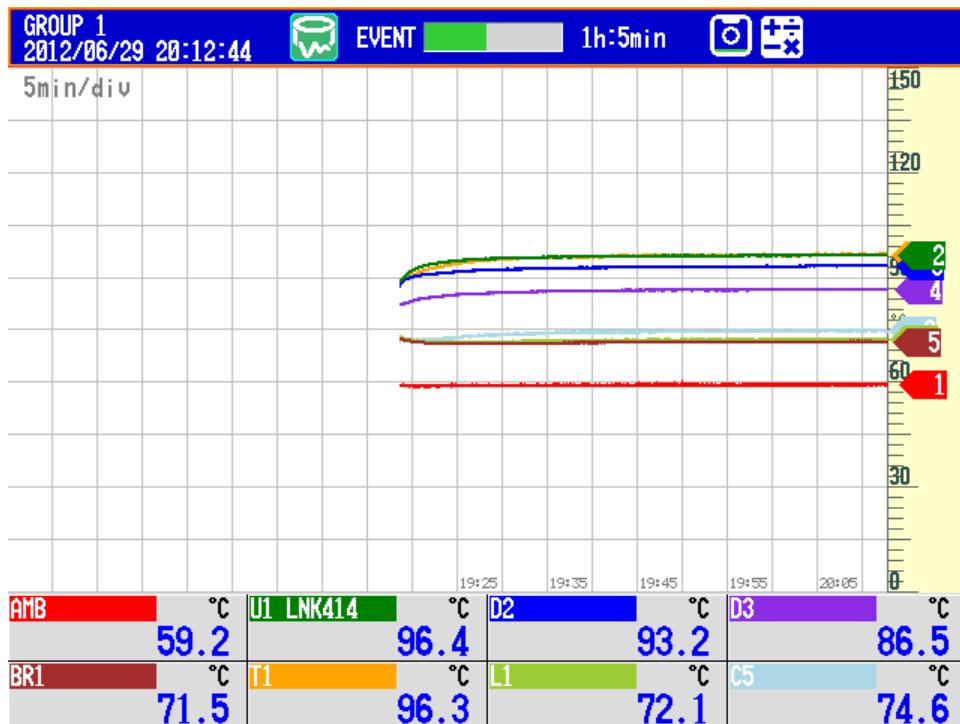
Figure 20 – Thermal Test Set-up.

10.2 140 VAC, 50 Hz, 16 V LED Load

Part Ref	Description	Temp, °C	ΔT, °C
U1	LinkSwitch-PH	90.1	31.4
D2	Output Diode	88.6	29.9
D3	Blocking Diode	84.6	25.9
BR1	Bridge Rectifier	75	16.3
T1	Transformer	89.9	31.2
L1	Differential Choke	74.5	15.8
C5	Output Capacitor	71.9	13.2
AMB	Ambient Inside the Box	58.7	

Figure 21 – Thermal Reading at 140 VAC, 50 Hz, Full Load

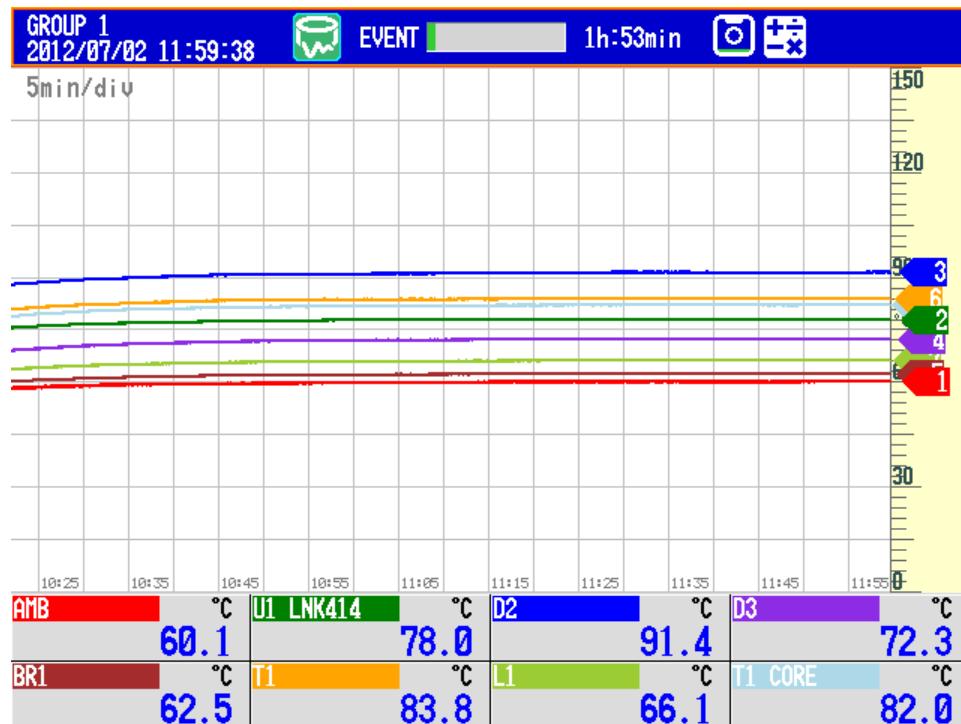
10.3 230 VAC, 50 Hz, 16 V LED Load**Figure 22 – Thermal Reading at 230 VAC, 50 Hz, Full Load.**

10.4 280 VAC, 50 Hz, 16 V LED Load

Part Ref	Description	Temp, °C	ΔT, °C
U1	LinkSwitch-PH	96.4	37.2
D2	Output Diode	93.2	34
D3	Blocking Diode	86.5	27.3
BR1	Bridge Rectifier	71.5	12.3
T1	Transformer	96.3	37.1
L1	Differential Choke	72.1	12.9
C5	Output Capacitor	74.6	15.4
AMB	Ambient Inside the Box	59.2	

Figure 23 – Thermal Reading at 280 VAC, 50 Hz, Full Load.

10.5 280 VAC, 60 Hz, Output Short Condition



Part Ref	Description	Temp, °C	ΔT, °C
U1	LinkSwitch-PH	78	17.9
D2	Output Diode	91.4	31.3
D3	Blocking Diode	72.3	12.2
BR1	Bridge Rectifier	62.5	2.4
T1-W	Transformer Wire	83.8	23.7
L1	Differential Choke	66.1	6
T1-C	Transformer Core	82	21.9
AMB	Ambient Inside the Box	60.1	

Figure 24 – Thermal Reading at 280 VAC, 60 Hz Output Short Condition.



11 Waveforms

11.1 Input Line Voltage and Current

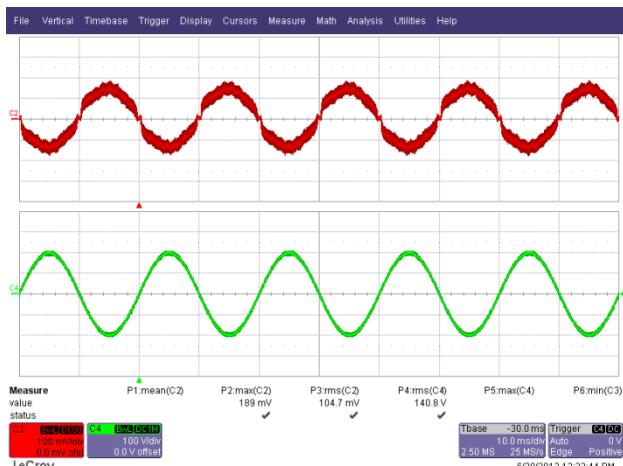


Figure 25 – 140 VAC, Full Load.

Upper: I_{IN} , 100 mA / div.

Lower: V_{IN} , 100 V, 10 ms / div.

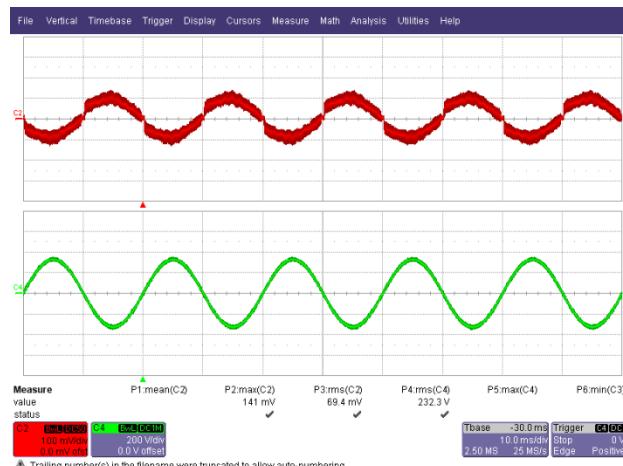


Figure 26 – 230 VAC, Full Load.

Upper: I_{IN} , 100 mA / div.

Lower: V_{IN} , 200 V, 10 ms / div.

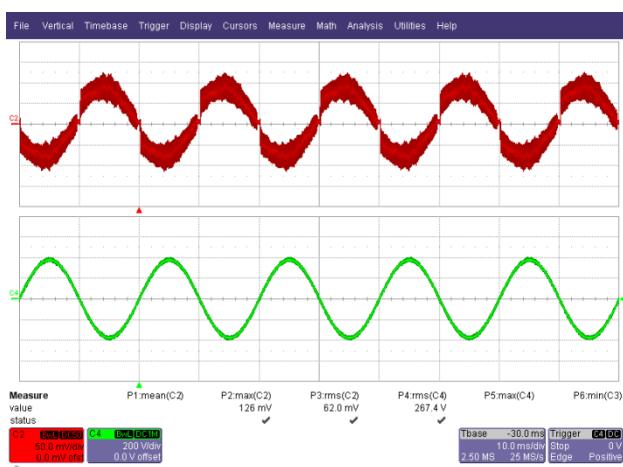


Figure 27 – 265 VAC, Full Load.

Upper: I_{IN} , 50 mA / div.

Lower: V_{IN} , 200 V, 10 ms / div.

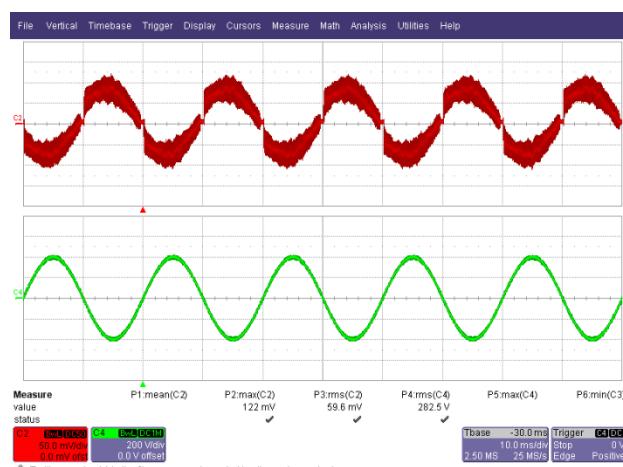


Figure 28 – 280 VAC, Full Load.

Upper: I_{IN} , 50 mA / div.

Lower: V_{IN} , 200 V, 10 ms / div.



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11.2 Output Voltage and Current at Normal Operation

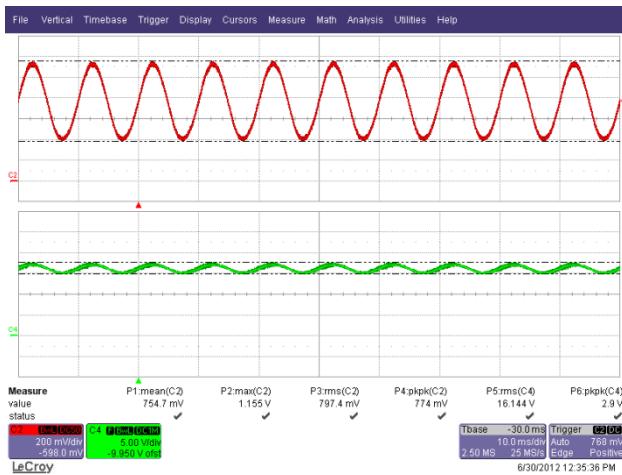


Figure 29 – 140 VAC, Full Load.

Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 5 V, 10 ms / div.

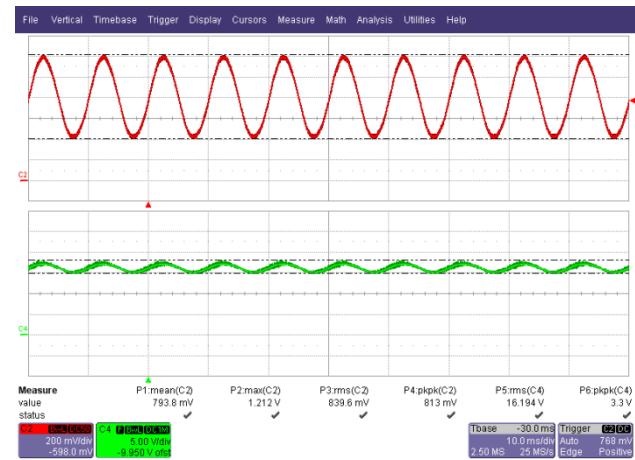


Figure 30 – 230 VAC, Full Load.

Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 5 V, 10 ms / div.

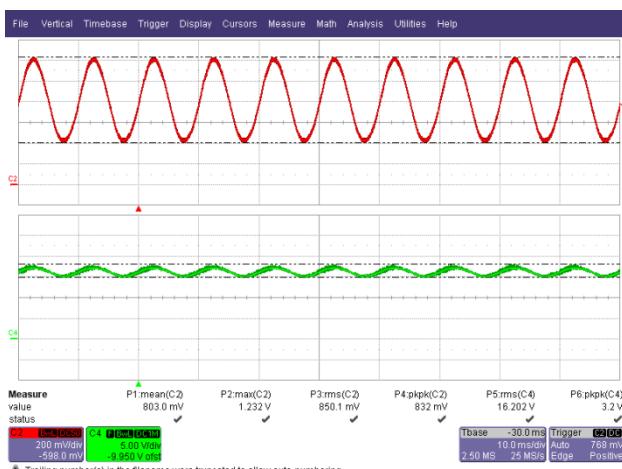


Figure 31 – 265 VAC, Full Load.

Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 5 V, 10 ms / div.

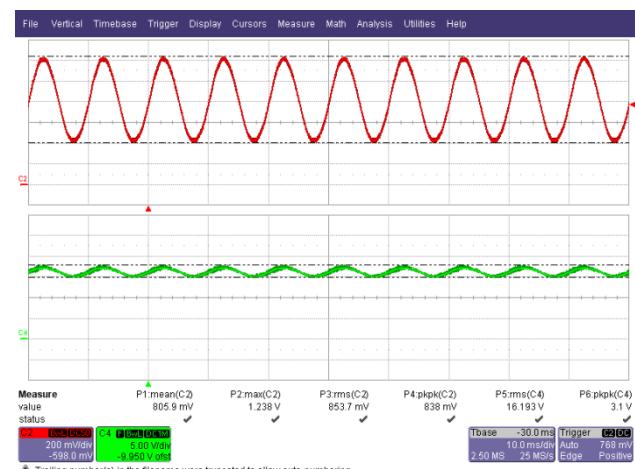
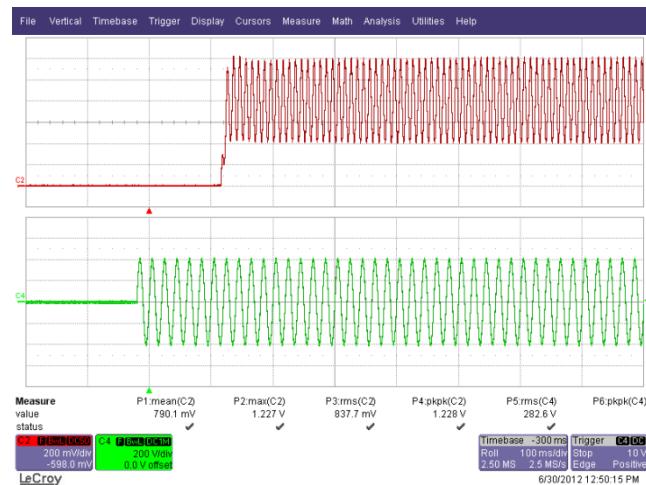
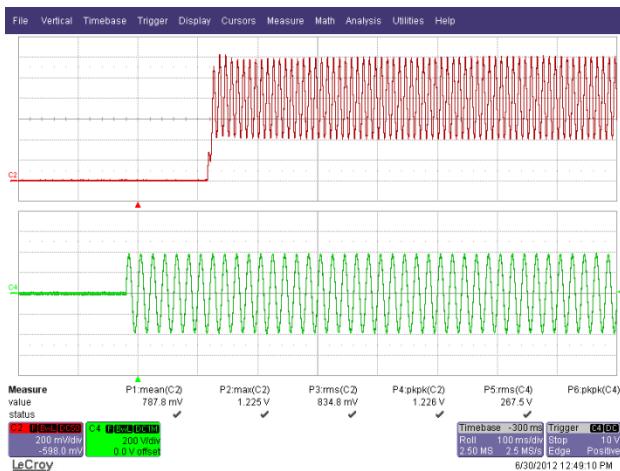


Figure 32 – 280 VAC, Full Load.

Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 5 V, 10 ms / div.



11.3 Start-up Time



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11.4 Drain Voltage and Current at Normal Operation

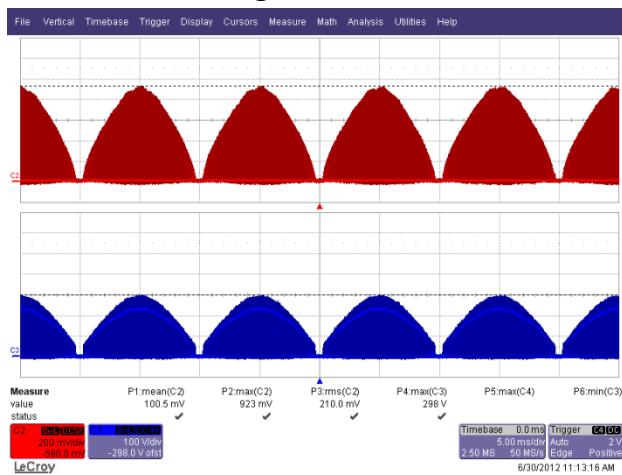


Figure 37 – 140 VAC, 50 Hz, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 100 V / div., 5 ms / div.

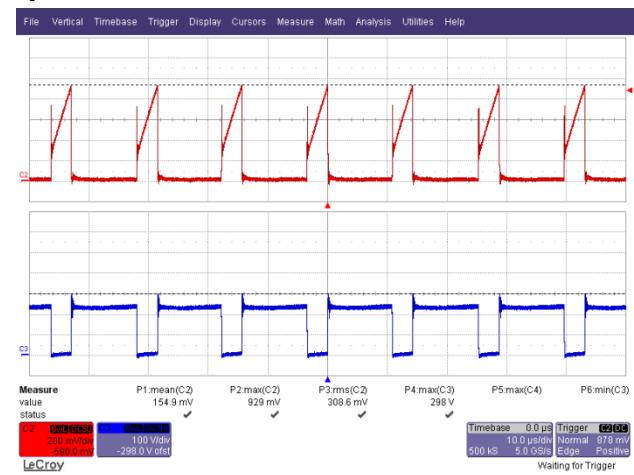


Figure 38 – 140 VAC, 50 Hz, Full Load.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 100 V / div., 10 μs / div.

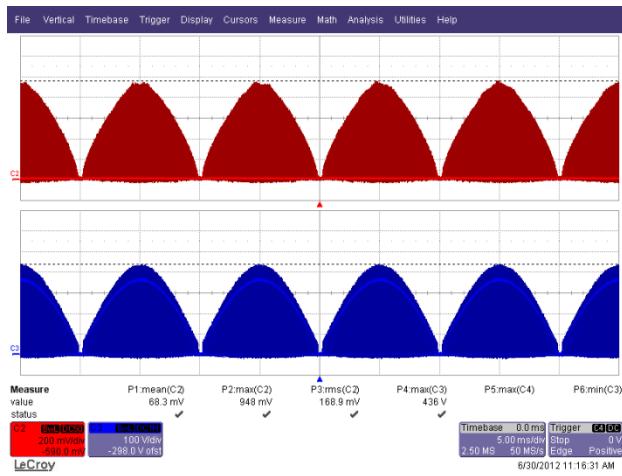


Figure 39 – 230 VAC, 50 Hz.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 100 V / div., 5 ms / div.

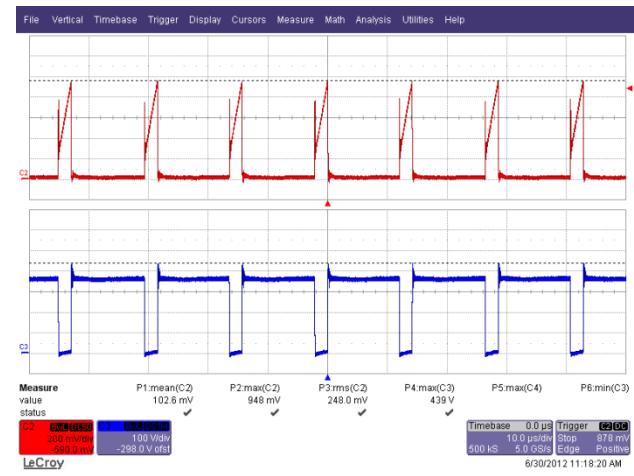
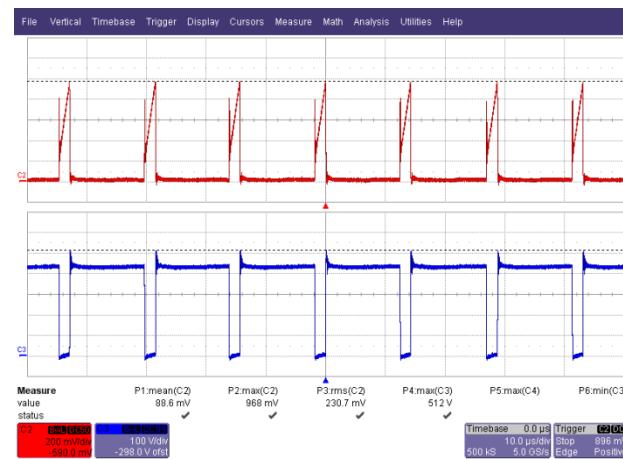
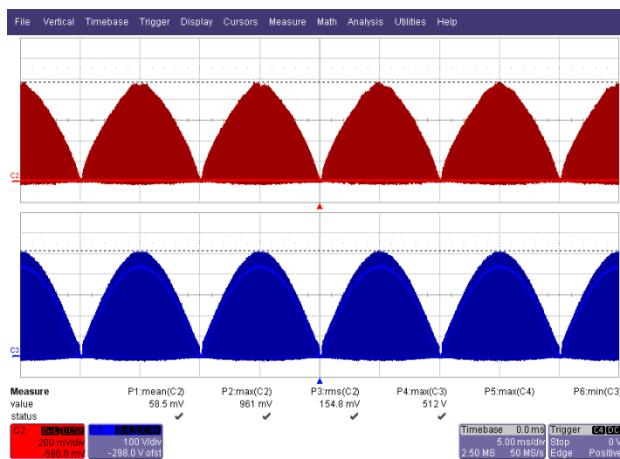


Figure 40 – 230 VAC, 50 Hz.
Upper: I_{DRAIN} , 0.2 A / div.
Lower: V_{DRAIN} , 100 V / div., 10 μs / div.





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11.5 Output Diode (D2) Voltage and Current at Normal Operation

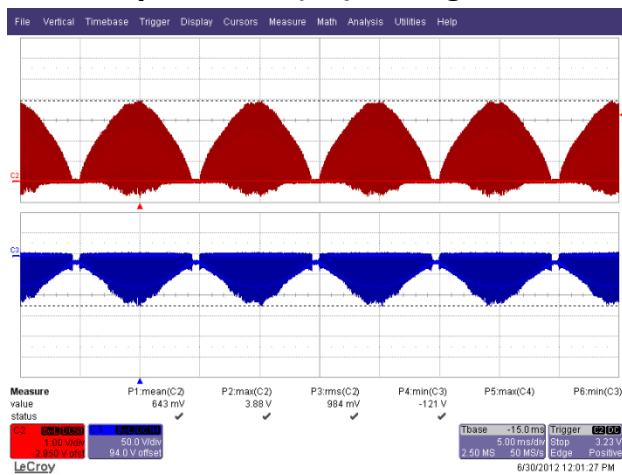


Figure 43 – 140 VAC, 50 Hz, Full Load.
Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 5 ms / div.

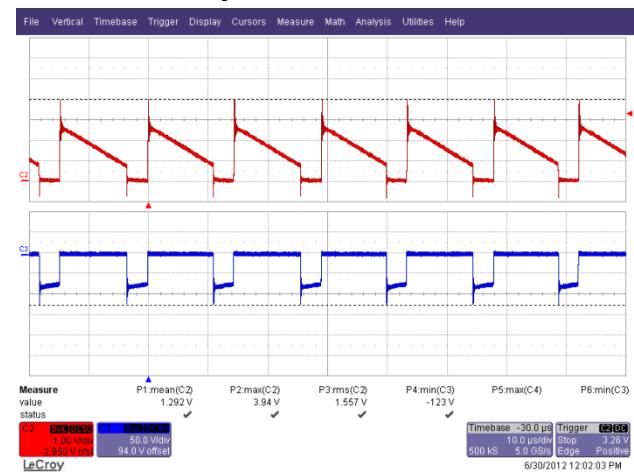


Figure 44 – 140 VAC, 50 Hz, Full Load.
Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 10 µs / div.

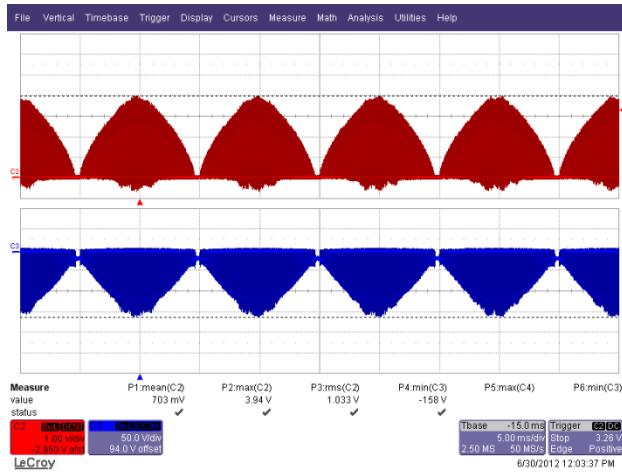


Figure 45 – 230 VAC, 50 Hz.
Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 5 ms / div.

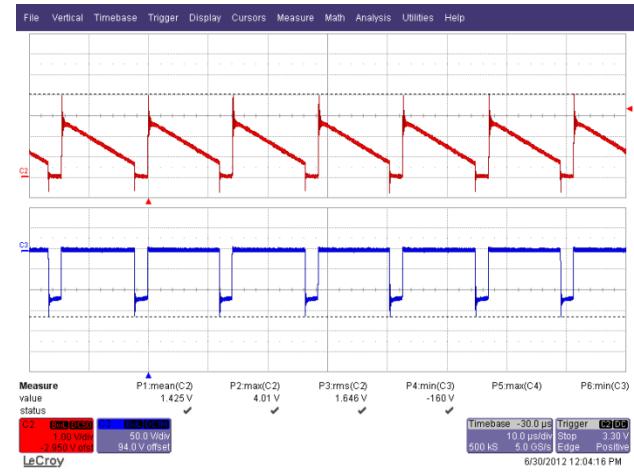
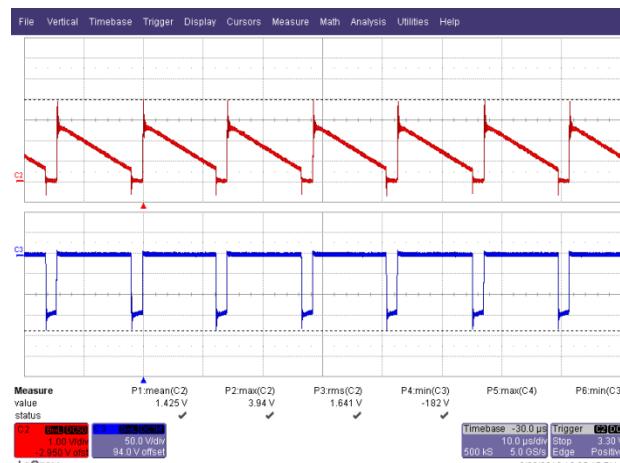
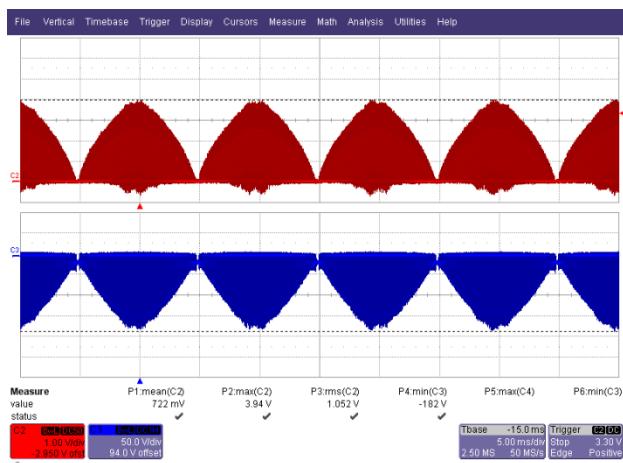


Figure 46 – 230 VAC, 50 Hz.
Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 10 µs / div.





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11.6 LNK414EG Start-Up Drain Voltage and Current

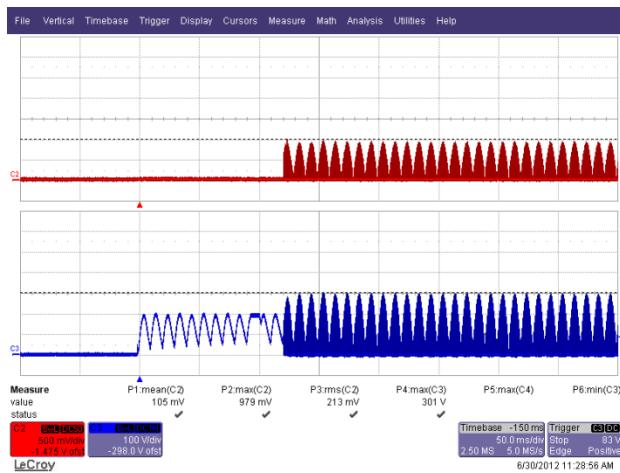


Figure 49 – 140 VAC Start-up.

Upper: I_{DRAIN} , 500 mA / div.
Lower: V_{DRAIN} , 100 V, 50 ms / div.

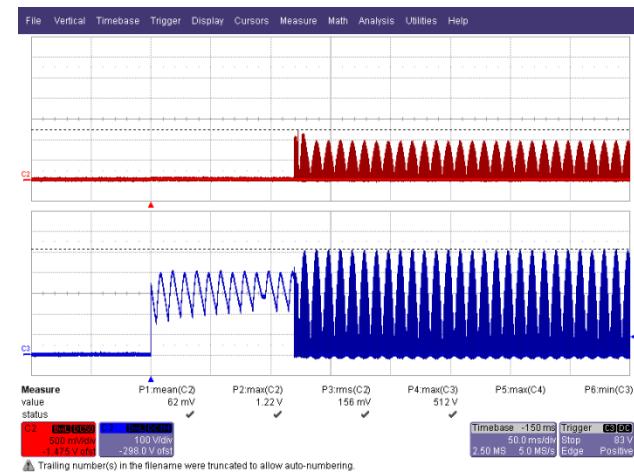


Figure 50 – 280 VAC Start-up.

Upper: I_{DRAIN} , 500 mA / div.
Lower: V_{DRAIN} , 100 V, 50 ms / div.

11.7 Output Diode (D2) Start-Up Voltage and Current

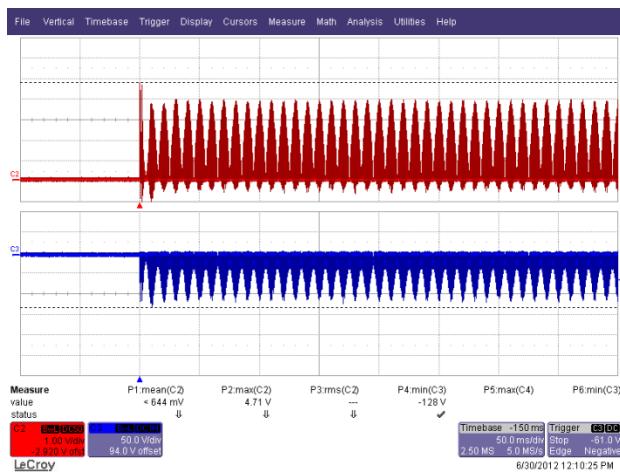


Figure 51 – 140 VAC Start-up.

Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V, 50 ms / div.

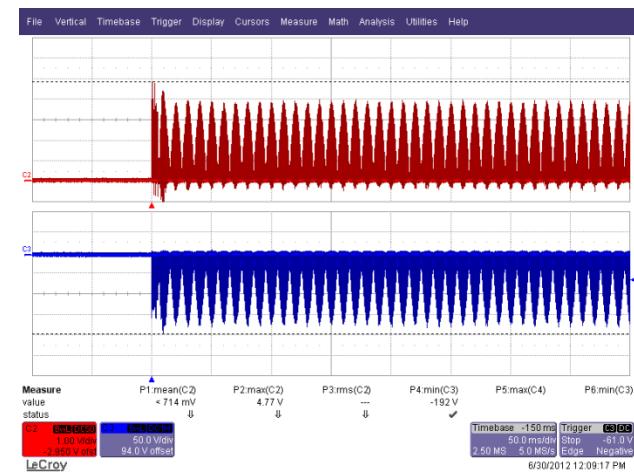


Figure 52 – 280 VAC Start-up.

Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V, 50 ms / div.



11.8 Drain Current and Drain Voltage During Output Short Condition

During output short condition, the maximum drain-source voltage of LNK414EG was measured at 280 VAC input. Maximum peak voltage measured was 477 V.

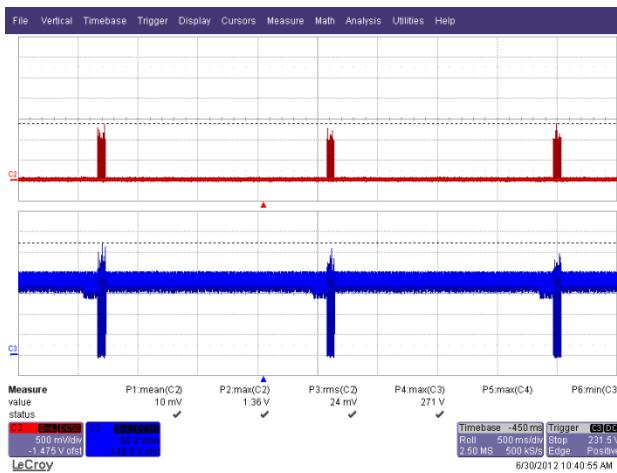


Figure 53 – 140 VAC Output Short.
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 50 V / div., 500 ms / div.

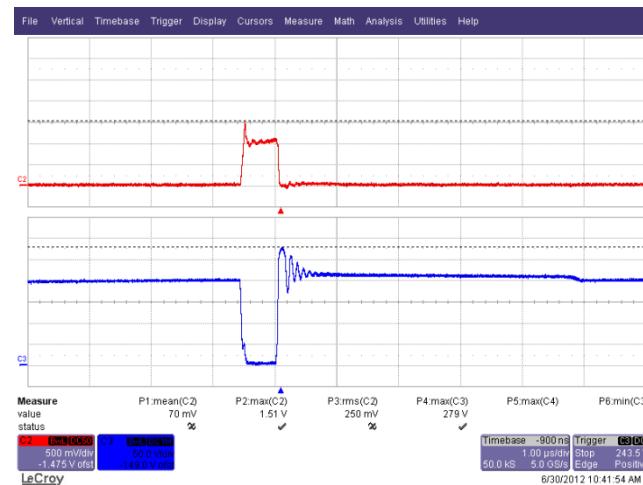


Figure 54 – 140 VAC Output Short.
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 50 V / div., 1 μ s / div.

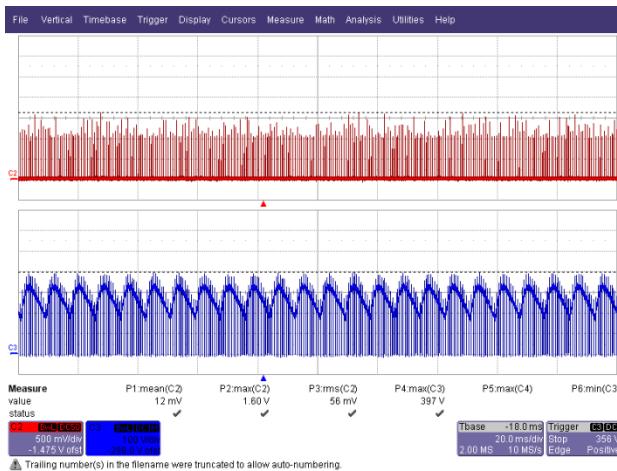


Figure 55 – 230 VAC Output Short.
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 100 V / div., 20 ms / div.

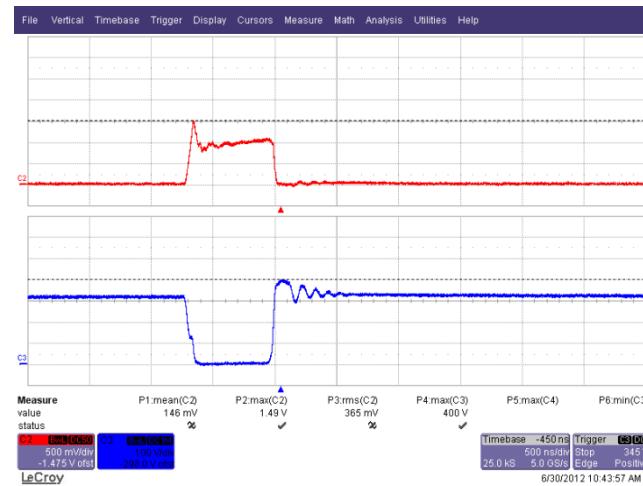
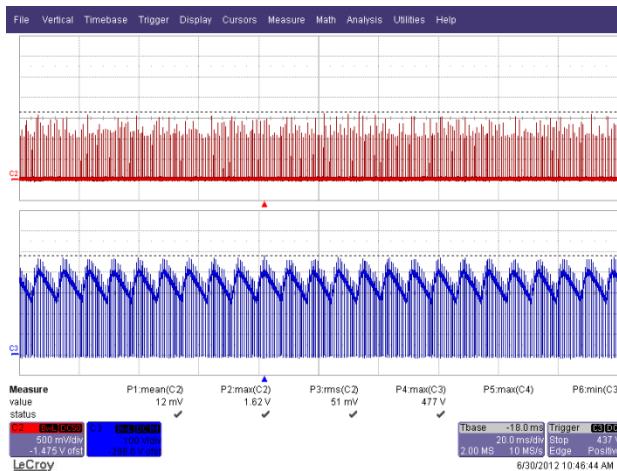


Figure 56 – 230 VAC Output Short.
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 100 V / div., 0.5 μ s / div.

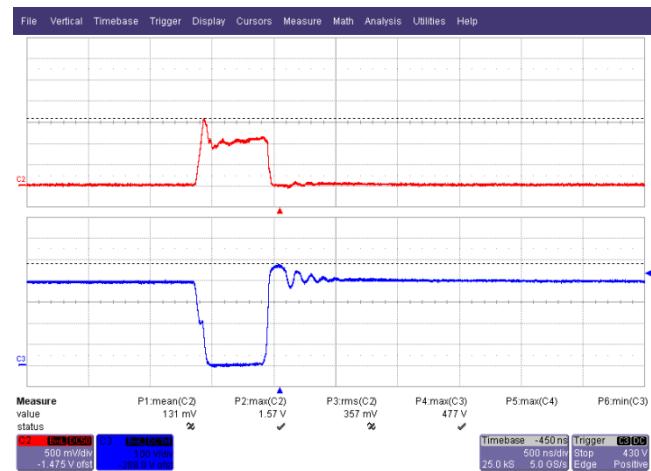


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**Figure 57 – 280 VAC Output Short.**

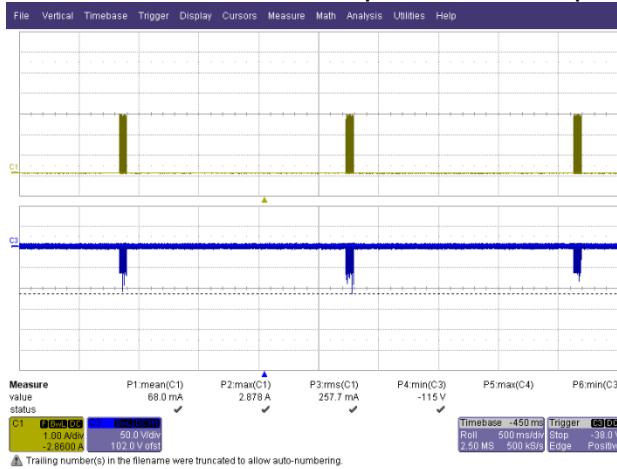
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 100 V / div., 1 s / div.

**Figure 58 – 280 VAC Output Short.**

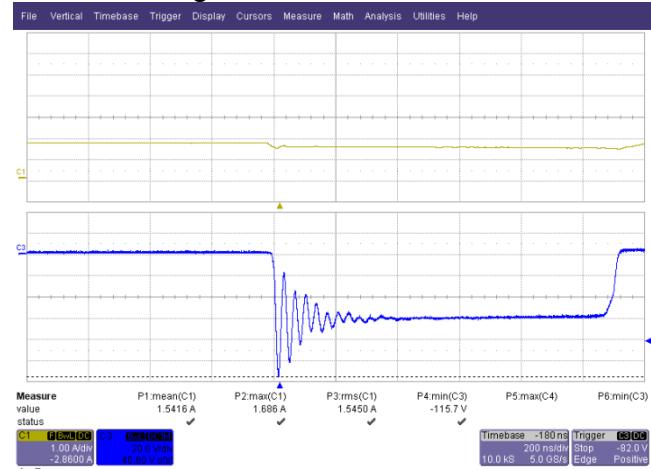
Upper: I_{DRAIN} , 0.5 A / div.
Lower: V_{DRAIN} 100 V / div., 0.5 μ s / div.

11.9 Output Diode (D2) Current and Voltage During Output Short Condition

During output short condition, the maximum reverse voltage of output diode D2 was measured at 280 VAC input. Maximum peak inverse voltage measured is 190 V.

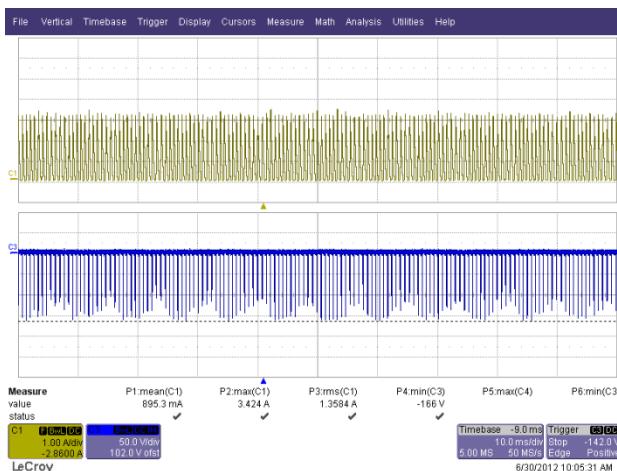
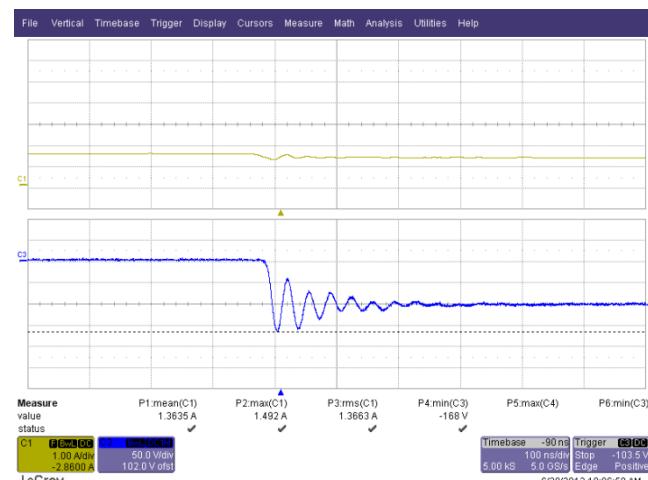
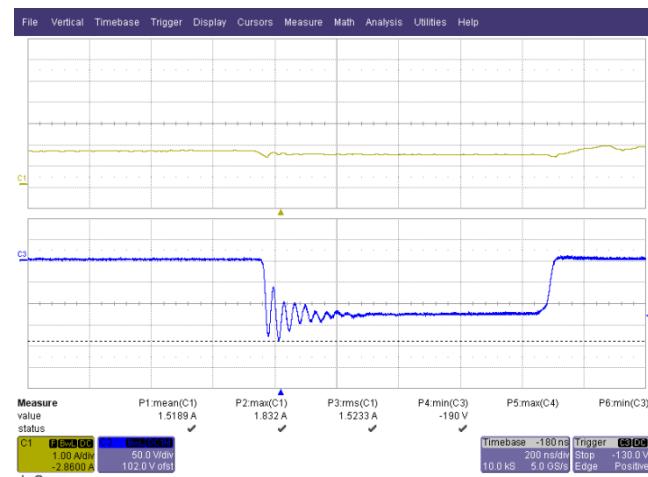
**Figure 59 – 140 VAC Output Short.**

Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 1 s / div.

**Figure 60 – 140 VAC Output Short.**

Upper: I_{D2} , 1 A / div.
Lower: V_{D2} , 50 V / div., 200 ns / div.



**Figure 61 – 230 VAC Output Short.**Upper: I_{D2} , 1 A / div.Lower: V_{D2} , 50 V / div., 10 ms / div.**Figure 62 – 230 VAC Output Short.**Upper: I_{D2} , 1 A / div.Lower: V_{D2} , 50 V / div., 100 ns / div.**Figure 63 – 280 VAC Output Short.**Upper: I_{D2} , 1 A / div.Lower: V_{D2} , 50 V / div., 5 ms / div.**Figure 64 – 280 VAC Output Short.**Upper: I_{D2} , 1 A / div.Lower: V_{D2} , 50 V / div., 200 ns / div.**Power Integrations, Inc.**Tel: +1 408 414 9200 Fax: +1 408 414 9201
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12 Conducted EMI

Conducted EMI were measured at 230 VAC, 60 Hz line input, 16 V LED load, and at room temperature.

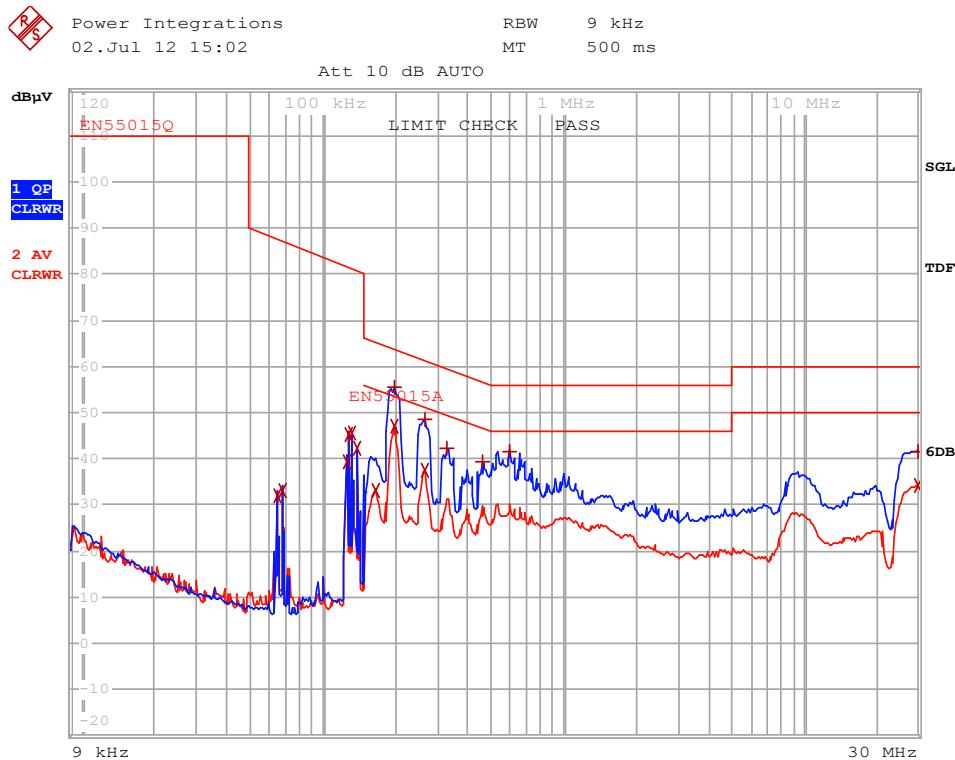
12.1 Test Set-up



Figure 65 – EMI Set-up: LED Driver and Load were Placed Inside the Cone.



12.2 Test Result



EDIT PEAK LIST (Final Measurement Results)					
Trace1:	EN55015Q				
Trace2:	EN55015A				
Trace3:	---				
TRACE	FREQUENCY	LEVEL dB μ V	L1	N	DELTA LIMIT dB
2 Average	64.5467705779 kHz	32.09	gnd		
2 Average	67.8393045788 kHz	33.05	gnd		
2 Average	125.720633819 kHz	39.42	N gnd		
2 Average	128.247618558 kHz	45.36	L1 gnd		
2 Average	130.825395691 kHz	45.63	L1 gnd		
2 Average	138.873793737 kHz	42.22	N gnd		
2 Average	165.693318812 kHz	33.24	L1 gnd	-21.93	
1 Quasi Peak	198.193645035 kHz	55.57	L1 gnd	-8.10	
2 Average	198.193645035 kHz	46.92	L1 gnd	-6.75	
1 Quasi Peak	264.49018761 kHz	48.59	L1 gnd	-12.69	
2 Average	264.49018761 kHz	37.64	L1 gnd	-13.64	
1 Quasi Peak	329.215131266 kHz	42.10	L1 gnd	-17.36	
1 Quasi Peak	461.749566613 kHz	39.42	L1 gnd	-17.23	
1 Quasi Peak	598.084042089 kHz	41.72	L1 gnd	-14.27	
1 Quasi Peak	29.5624713804 MHz	41.60	N gnd	-18.39	
2 Average	29.8580960942 MHz	34.32	L1 gnd	-15.67	

Figure 66 – Conducted EMI, 16 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.



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13 Line Surge

The unit was subjected to ± 2500 V 100 kHz ring wave and ± 2 kV differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2 kV	230	L1, L2	0	Surge (2Ω)	Pass
-2 kV	230	L1, L2	0	Surge (2Ω)	Pass
+2 kV	230	L1, L2	90	Surge (2Ω)	Pass
-2 kV	230	L1, L2	90	Surge (2Ω)	Pass

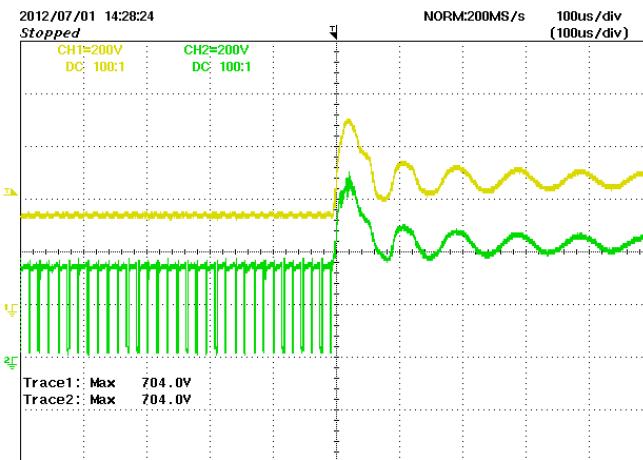


Figure 67 – Peak Rectified Input Voltage (Trace 1) and U1 Drain-Source Voltage (Trace 2) after 90° 2 kV Differential Surge at the Input. Maximum Drain to Source Voltage Measured was 704 V.



14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
19-Oct-12	CA	1.0	Initial Release	Apps & Mktg



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