Design Example Report

Title	***40.5 W, High Power Factor (>0.95), <5% I_{OUT} Tolerance, Non-Isolated Buck LED Driver Using LinkSwitch™-PH LNK419EG***
Specification	90 VAC – 300 VAC Input; 54 V, 750 mA Output
Application	Street Lamp
Author	Applications Engineering Department
Document Number	DER-340
Date	August 22, 2012
Revision	1.0

Summary and Features

- Highly energy efficient
  - >88% at 230 VAC
  - >87% at 120 VAC
  - <2% line and load regulation
  - <5% I_{OUT} tolerance
- Low cost, low component count and small, single-sided printed circuit board
- Frequency jitter allows smaller, lower cost EMI filter
- Integrated protection and reliability features
  - Output open circuit / output short-circuit protected with auto-recovery
  - Line input overvoltage shutdown extends voltage withstand during line faults
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
- IEC 61000-4-5, IEC 61000-3-2 Class C, and EN55015 B conducted EMI compliant

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Important Note: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

The document describes a non-isolated high power factor (PF) LED driver designed to drive a nominal LED string voltage of 54 V at 750 mA from an input voltage range of 90 VAC to 300 VAC. The LED driver utilizes the LNK419EG from the LinkSwitch-PH family of ICs.

The topology is a single-stage non-isolated buck converter that meets the high efficiency requirements for this design. Good line and load output current regulation is achieved by directly sensing the output current and using shunt regulator for closed-loop feedback control.

High power factor and low THD is achieved by employing the LinkSwitch-PH IC which also provides a sophisticated range of protection features including auto-restart to prevent damage in the event of open control loop or during output short-circuit. Line overvoltage protection provides extended line fault and surge withstand. Output overvoltage protects the supply should the load be disconnected. Accurate hysteretic thermal shutdown ensures safe PCB temperatures under all conditions.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.

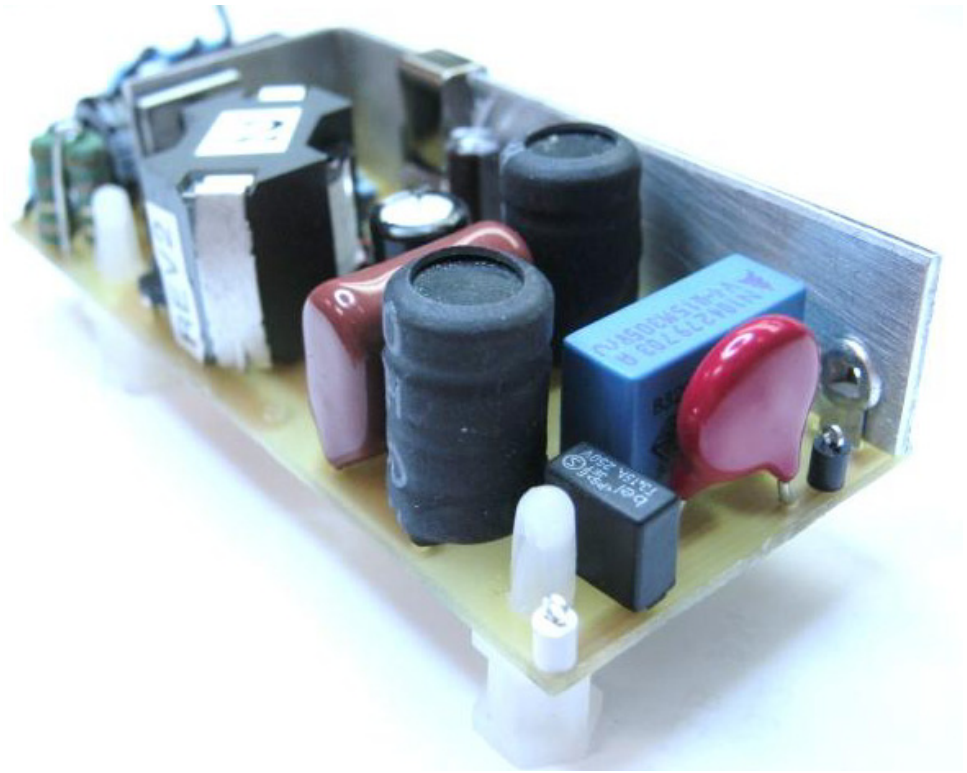

Figure 1 – Populated Circuit Board.

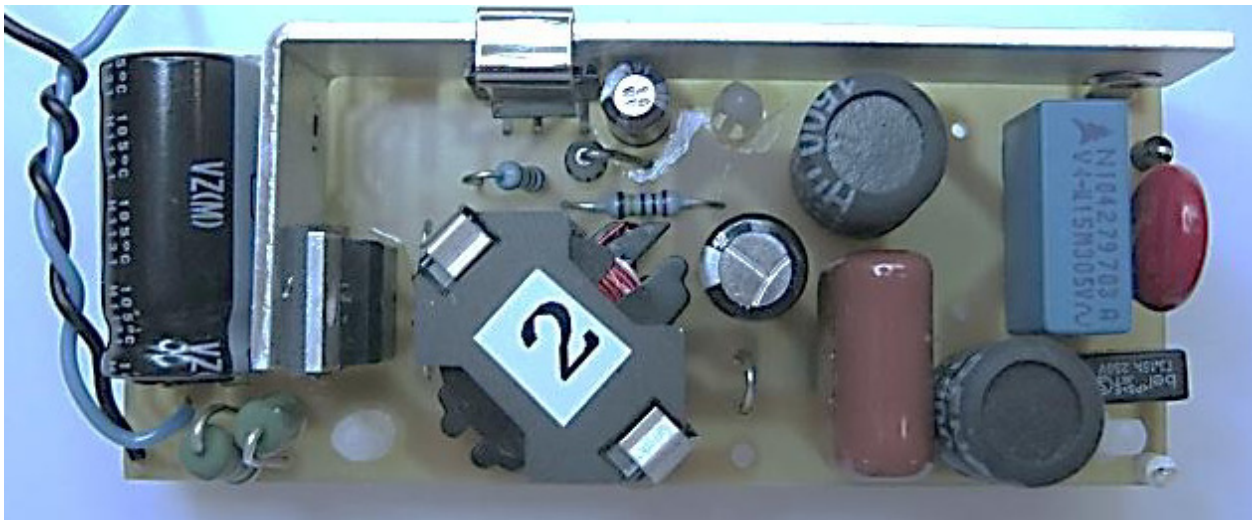

Figure 2 – Populated Circuit Board (Top View), 86 mm x 36 mm.

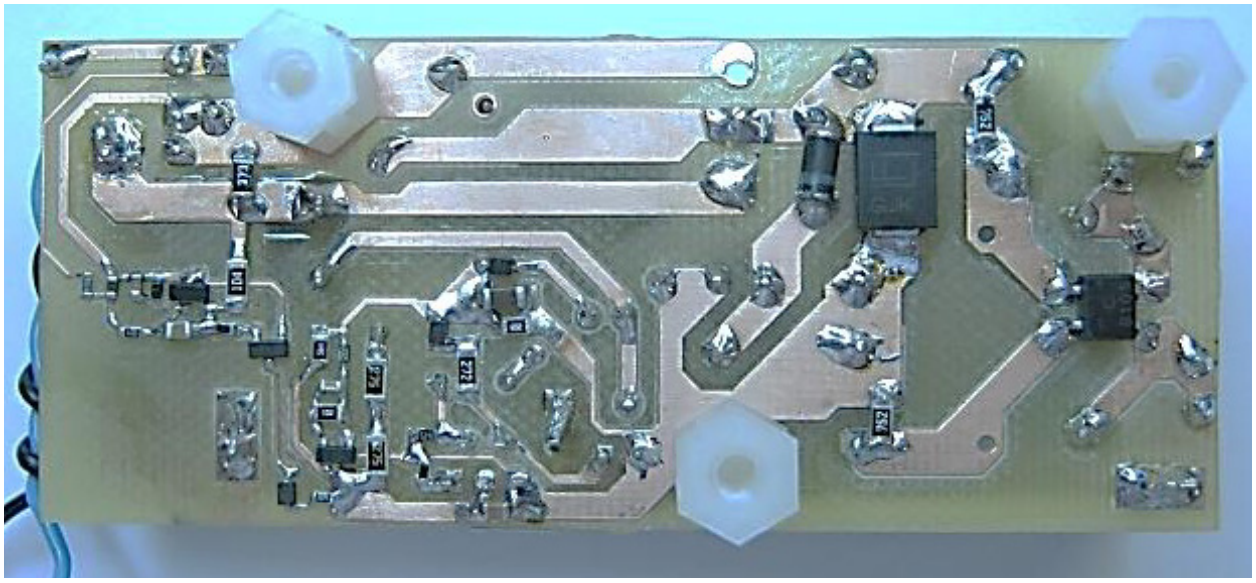

Figure 3 – Populated Circuit Board (Bottom View).

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	300	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		60/50		Hz	
Output						
Output Voltage	V_{OUT}		54		V	
Output Current	I_{OUT}	712	750	787	mA	V_{OUT} = 54 V, V_{IN} = 230 VAC, 25°C
Total Output Power						
Continuous Output Power	P_{OUT}		40.5		W	
Efficiency						
Full Load	η	85	88		%	V_{OUT} = 54 V, V_{IN} = 230 VAC, 25°C
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Non-Isolated				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	
Common mode (L1/L2-PE)						
Differential Surge			1		kV	
Power Factor			0.9			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class C				
Ambient Temperature	T_{AMB}		50		°C	Free convection, sea level

3 Schematic

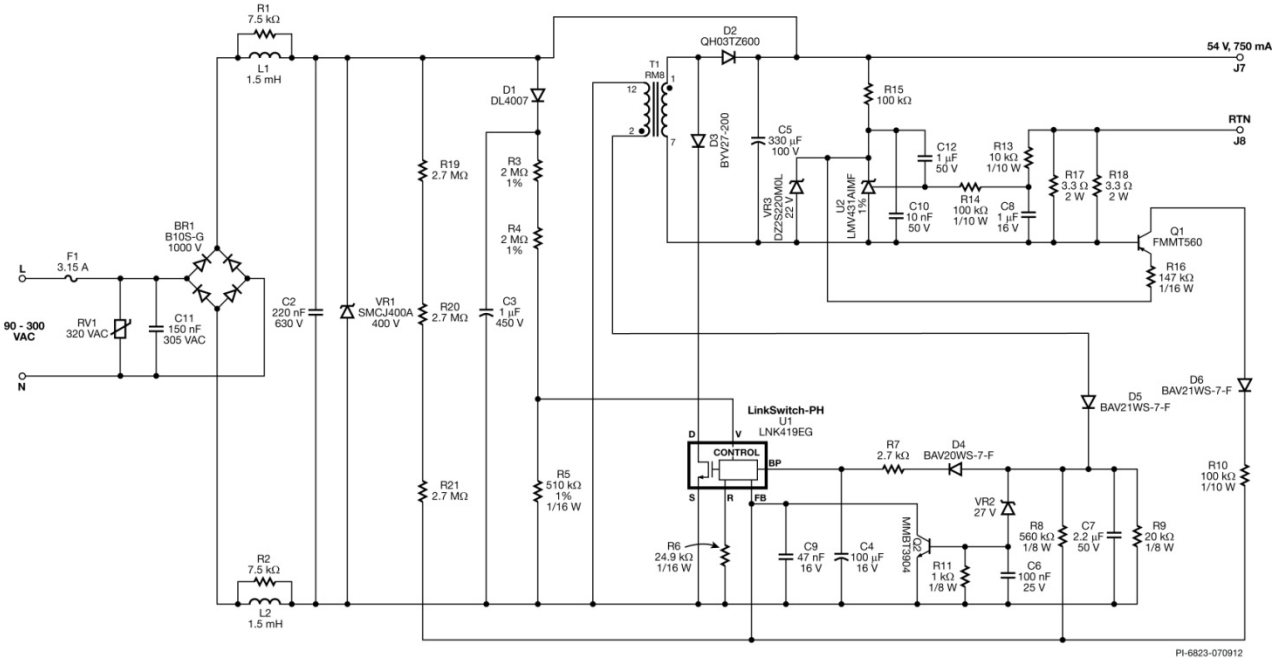

Figure 4 – Schematic.

Note: J1 is used as an option to make the board configurable for buck or buck-boost topology. For buck configuration, pin 1 of J1 is shorted to pin 2 of J1. For buck-boost configuration, pin 2 of J1 is shorted to pin 3 of J1.

Capacitor C11 is not mounted on the board for this buck design. It is a differential filter option for a buck-boost configuration where differential currents are typically higher.

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4 Circuit Description

The LinkSwitch-PH device is a controller with an integrated 725 V power MOSFET for use in LED driver applications. This LinkSwitch-PH circuit used here is configured as a single-stage continuous conduction mode (CCM) buck topology and provides a regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 provides protection from component failure and RV1 provides a clamp to limit the maximum voltage during differential line surge events. A 320 VAC rated part was selected, being slightly above the maximum specified operating voltage of 300 VAC. Diode bridge BR1 rectifies the AC line voltage with capacitor C2 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C11 and C2) is necessary to maintain a power factor of greater than 0.9.

EMI filtering is provided by inductors L1 and L2, and capacitors C2 and C11. Resistor R1 and R2 across L1 and L2 damp any LC resonances due to an interaction between filter components and the AC line impedance which might occur, increasing conducted EMI levels.

4.2 Power Circuit and LinkSwitch-PH External Components

The topology chosen in this design is a low-side buck configured to provide unity power factor and constant current output for a wide input voltage range of 90 VAC to 300 VAC. The buck converter offers the advantage of reduced magnetic component size and reduced voltage and current stress on the semiconductors (compared to buck-boost or flyback). It also offers an advantage for meeting surge requirements since the voltage stress of the main switch (U1) and freewheeling diode (D2) is clamped to the peak of the input voltage. The low-side configuration greatly simplifying EMI filtering.

Transformer T1 is the main inductor of the buck converter. The inductance is chosen to keep the operation in CCM in order to reduced RMS currents and at the same time meet Class C harmonic limits. A bias winding coupled to the main winding is used to provide supply to U1 thru the BYPASS (BP) pin for improved efficiency. The bias winding flyback voltage is rectified by D5 and fed to capacitor C7. A bleed resistor R22 is necessary to discharge C7 during an output short condition. This bias voltage is then fed to BP pin thru diode D4 and resistor R7. Resistor R7 limits the current into the BP pin of U1 and diode D4 prevents internal supply current from charging C7 during start-up.

Diode D2 conducts every time U1 is off and transfers the energy stored in T1 to the load. Diode D2 is an ultra-fast recovery diode that eliminates/minimizes reverse recovery current for improved efficiency and EMI performance. The reverse recovery current from slow diodes increases dissipation on the main switch U1 and causes EMI related problems especially at high input voltage and CCM operation. Care should be taken selecting this diode.

Diode D3 is necessary to prevent reverse current from flowing through U1 while the voltage across C2 (rectified input AC) falls below the output voltage.

To provide peak line voltage information to U1, the incoming rectified AC peak charges C3 via D1. The rectified peak voltage is then fed into the VOLTAGE MONITOR (V) pin of U1 as a current via R3 and R4. Resistor R5 is used to adjust line undervoltage and overvoltage protection set points. The combination of R3, R4, and R5 centers the operating input voltage range from 71 VAC to 324 VAC typical.

The line overvoltage shutdown function, sensed via the V pin current, increases the rectified line voltage withstand (during surges and line swells) to the 725 BV_{DSS} rating of the internal power MOSFET.

Capacitor C4 provides local decoupling for the BP pin of U1 which is the supply pin for the internal controller. During start-up, C4 is charged to ~6 V from an internal high-voltage current source connected to the D pin of U1. Once charged, U1 starts switching at which point the operating supply current is provided from the bias supply via R7. Diode D4 isolates the BP pin from the bias capacitance C7 to prevent the start-up time increasing due to charging of both C7 and C4. Capacitor C4 also selects the power mode of U1, 100 μF selecting full power mode.

The REFERENCE (R) pin of U1 is tied to ground (SOURCE) via resistor R6. A 24.9 kΩ value is used for non-dimming, universal input designs.

4.3 Closed Loop Feedback

A current sense resistor (R17 parallel with R18) and a shunt regulator U2 is employed to enable tight output current regulation for this design. Output current sensed by R17 and R18 is filtered by R13 and C8, with values chosen to filter the line ripple present on the output current. This voltage is then compared with the internal reference of U2 to provide a regulated output current of 750 mA. Capacitor C12 and resistor R14 provide feedback compensation for the shunt regulator U2.

If the average output current is less than the desired value, U2 cathode voltage increases with reference to its anode, which in turn increases the voltage across resistor R16. The increased current flowing into R16 minus the base current of Q1 is fed to the FB pin of U1 to increase the power delivery (duty cycle) of the system until the average current seen by the sense resistors is equal to the desired value. A larger output current on the other hand results to a smaller feedback current fed to the FB pin of U1 which reduces the duty cycle of the converter. The larger time constants of C12 and R14 were necessary to keep the converter from responding to line frequency and maintain high power factor at the input.

Zener diode VR3 clamps the maximum cathode voltage of U2 to 22 V. This prevents the U2 from exceeding its maximum rated voltage and at the same time clamps the

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maximum feedback current fed to the FB pin thru Q1 and D6. Resistor R15 limits the dissipation in VR3 and also provides the path for U2 supply current and feedback current thru R16. Resistor R16 is chosen to provide sufficient current to keep the output regulated.

Resistor R10 and capacitor C9 was added for additional filtering of the feedback current from transistor Q1. Resistor R8 is used to boost the feedback current (~30 μA at full load) to speed-up start-up at low line conditions. This is required because of the slow feedback current path from transistor Q1. Without resistor R8, the unit does not have enough duty cycle during start-up to charge the output capacitor and will reach the end of the soft-start period and enter auto restart condition.

THD line compensation was also added to increase margin on odd harmonics from the Class C limit. A current proportional to the rectified line input voltage was fed to the FB pin thru resistors R19, R20, and R21. This network also adds a dc value to the feedback current but is compensated by the closed feedback system.

4.4 Open Load and Short-Circuit Protection

The controller annunciates both short-circuit and open-loop conditions once the FB pin current falls below the $I_{FB(AR)}$ threshold after the soft-start period. To minimize the power dissipation under this fault condition the shutdown/auto-restart circuit turns the power supply on (same as the soft-start period) and off at an auto-restart duty cycle of typically DC_{AR} for as long as the fault condition persists.

During open load condition, the rise of the output voltage is sensed thru the bias winding. If the reflected output voltage seen on capacitor C7 exceeds the threshold voltage of Zener diode VR2, transistor Q2 pulls down the FB pin to ground forcing U1 to enter auto-restart condition.

During short circuit condition, voltage on capacitor C7 drops to almost zero forcing the feedback current to the FB pin to reach the auto-restart condition ($I_{FB(AR)} \leq 25$ μA).

5 PCB Layout

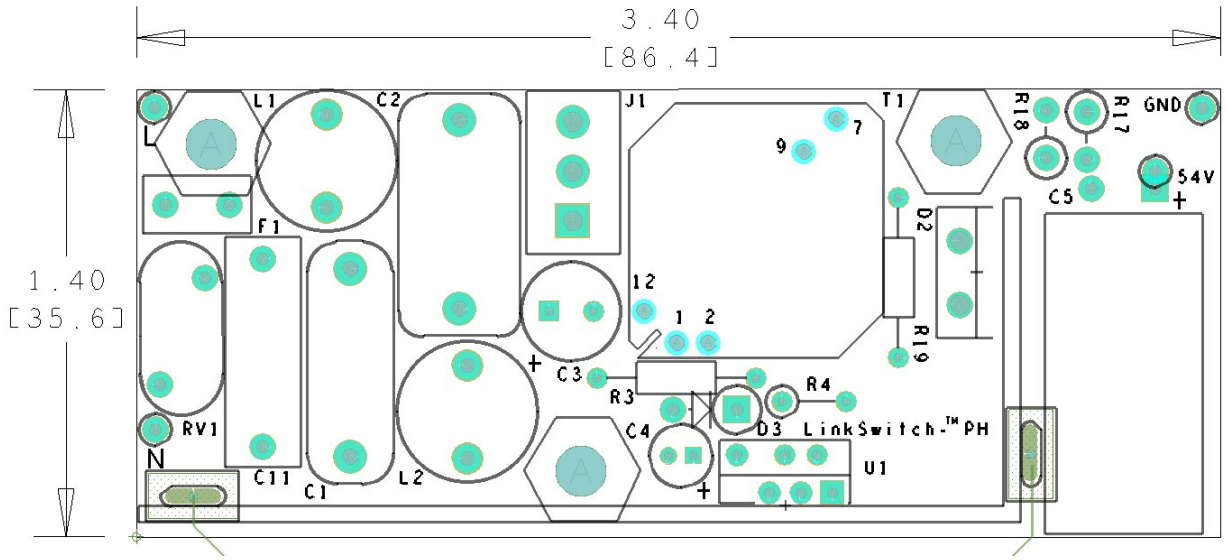

Figure 5 – PCB Layout and Outline, Top Side (in/ [mm]).

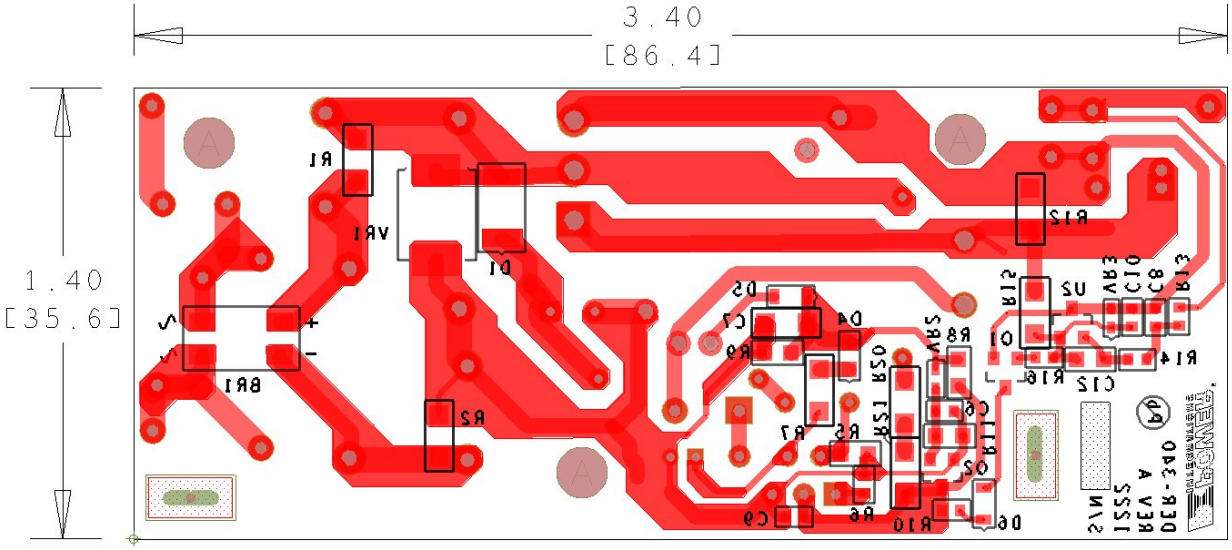

Figure 6 – Bottom Side (in/ [mm]).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Technology
2	1	C1	Not Populated		
3	1	C2	220 nF, 630 V, Film	ECQ-E6224KF	Panasonic
4	1	C3	1.0 µF, 450 V, Electrolytic, NHG, (8 x 11.5)	ECA-2WHG010	Panasonic
5	1	C4	100 µF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG160ELL101ME11D	Nippon Chemi-Con
6	1	C5	3300 µF, 100 V, Electrolytic, (12.5 x 25)	UVZ2A331MHD	Nichicon
7	1	C6	100 nF 25 V, Ceramic, X7R, 0603	ECJ-1VB1E104K	Panasonic
8	1	C7	2.2 µF, 50 V, Ceramic, Y5V, 1206	GRM31MF51H225ZA01L	Murata
9	1	C8	1 µF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
10	1	C9	47 nF 16 V, Ceramic, X7R, 0603	ECJ-1VB1C473K	Panasonic
11	1	C10	10 nF 50 V, Ceramic, X7R, 0603	ECJ-1VB1H103K	Panasonic
12	1	C11	150 nF, 305 VAC, X2	B32922A2154M	Epcos
13	1	C12	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX
14	1	D1	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
15	1	D2	600 V, 3 A, TO-220AC	QH03TZ600	Power Integrations
16	1	D3	200 V, 2 A, Ultrafast Recovery, 25 ns, SOD57	BYV27-200-TR	Vishay
17	1	D4	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	On Semi
18	2	D5 D6	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
19	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
20	2	L1 L2	1.5 mH, 0.8 A, 20%	RL-5480-4-1500	Renco
21	1	Q1	PNP, Small Signal BJT, 500 V, 0.15 A, SOT23	FMMT560TA	Zetex
22	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semi
23	2	R1 R2	7.5 k, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ752V	Panasonic
24	2	R3 R4	2.00 MΩ, 1%, 1/4 W, Metal Film	RNF14FTD2M00	Stackpole
25	1	R5	510 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5103V	Panasonic
26	1	R6	24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
27	1	R7	2.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ272V	Panasonic
28	1	R8	560 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ564V	Panasonic
29	1	R9	20 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
30	2	R10 R14	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
31	1	R11	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
32	1	R12	27 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ273V	Panasonic
33	1	R13	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
34	1	R15	100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
35	1	R16	147 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1473V	Panasonic
36	2	R17 R18	3.3 Ω, 5%, 2 W, Metal Oxide	RSMF2JT3R30	Stackpole
37	1	R19	2.7 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2M7	Yageo
38	2	R20 R21	2.7 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ275V	Panasonic
39	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	LittleFuse
40	1	T1	Bobbin, RM8, Vertical, 12 pins	RM8/12/1	Schwartzpunkt
41	1	U1	LinkSwitch-PH, eSIP	LNK419EG	Power Integrations
42	1	U2	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF	National Semi
43	1	VR1	400 V, 1500 W, SMC	SMCJ400A	LittleFuse
44	1	VR2	27 V, 5%, 150 mW, SSMINI-2	MAZS2700ML	Panasonic
45	1	VR3	22 V, 5%, 150 mW, SSMINI-2	DZ2S220M0L	Panasonic

7 Inductor Specification

7.1 Electrical Diagram

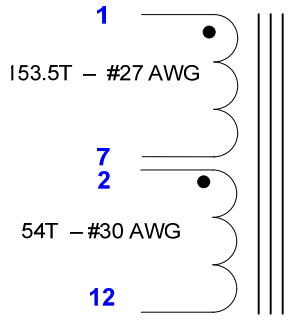

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-7, all other windings open, measured at 66 kHz, 0.4 V_{RMS}	1000 µH ±7%
Resonant Frequency	Pins 1-7, all other windings open	0.9 MHz (Min.)

7.3 Materials

Item	Description
[1]	Core: RM8I-3F3 or equivalent
[2]	Bobbin: BRM08-9112ASQ
[3]	Magnet Wire, #27 AWG, solderable double coated.
[4]	Magnet Wire, #30 AWG, solderable double coated.

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7.4 Inductor Build Diagram

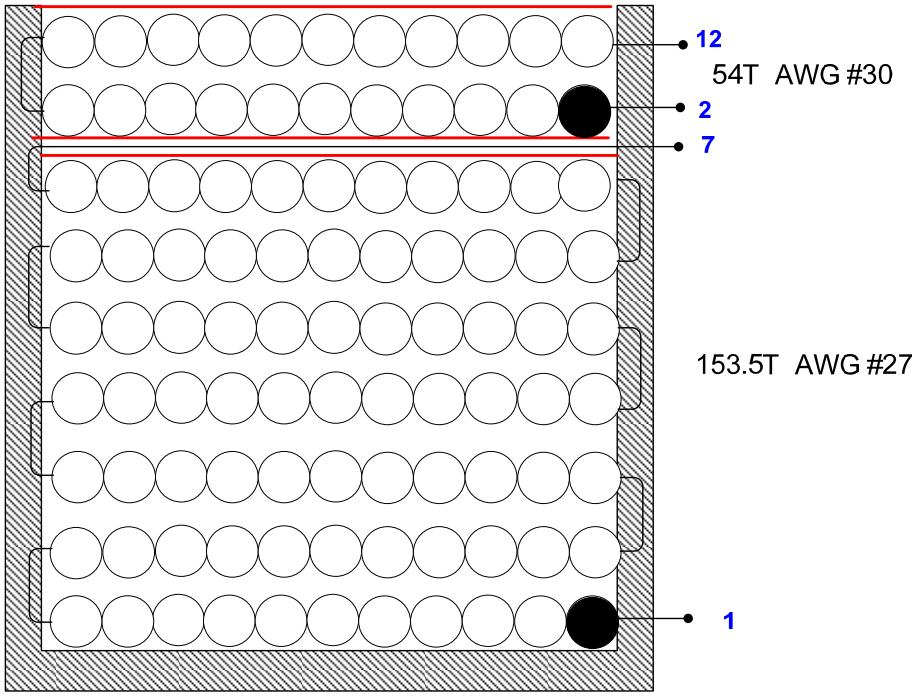

Figure 8 – Inductor Build Diagram.

7.5 Inductor Construction

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the right.
WD1	Start at pin 1. Wind 153.5 turns of item [3] as shown in Figure 2. Terminate at pin 7
WD2	Start at pin 2. Wind 54 turns of item [4] and terminate the other end at pin 12.
Finish	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 3, 4, 5, 6, 10, 11.

8 Inductor Design Spreadsheet

ACDC_LNK-PH_Buck_040711; Rev.1.0; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	LNK-PH_040711: LinkSwitch-PH Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**NO**		**NO**		Select "YES" option if dimming is required. Otherwise select "NO".
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	305		305	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	54.00		54.00	V	Typical output voltage of LED string at full load
VO_MAX			67.50	V	Maximum LED string Voltage. Ensure that the maximum LED string voltage is below VO_MAX
VO_MIN			40.50	V	Minimum LED string Voltage. Ensure that the minimum LED string voltage is above VO_MIN
V_OVP			73.86	V	Over-voltage setpoint
IO	0.75		0.75		Typical full load LED current
PO			40.5	Watts	Output Power
n	0.85		0.85		Estimated efficiency of operation
ENTER LinkSwitch-PH VARIABLES					
LNK-PH	**LNK419**		**LNK419**		Selected Linkswitch-PH device. If Dimming is required, select device from LNK40X family, Otherwise select device from LNK41X family
Current Limit Mode	**FULL**		**FULL**		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			3.160	A	Minimum current limit
ILIMITMAX			3.860	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			38.70	uA	V pin current
Rv			3.909	M-ohms	Upper V pin resistor
RV2			1.402	M-ohms	Lower V pin resistor
IFB			160.85	uA	FB pin current (75 uA < IFB < 250 uA)
R7			94.00	k-ohms	IFB setting resistor (See RDR254 schematic)
R8			35.35	k-ohms	Upper resistor in base divider (See RDR254 schematic)
R9			90.90	k-ohms	Lower resistor in base divider (See RDR254 schematic)
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD			0.60	V	Output Winding Diode Forward Voltage Drop
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	0.50		0.50		Ripple to Peak Current Ratio (0.4 < KRP < 1.3)
LP			984	uH	Primary Inductance
KP Expected			0.24		Ripple to Peak Current Ratio (0.4 < KRP < 1.3)
Expected IO (average)			0.76	A	Expected Average Output Current
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM8**		**RM8**		Selected Core for inductor
Core		RM8		P/N:	*
Bobbin		RM8_BOBBIN		P/N:	CSV-RM8-1S-8P-G
AE			0.52	cm^2	Core Effective Cross Sectional Area

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LE		3.55	cm	Core Effective Path Length
AL		1550	nH/T^2	Ungapped Core Effective Inductance
BW		9.1	mm	Bobbin Physical Winding Width
M		0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	8.00	8		Number of Primary Layers
dDC INPUT VOLTAGE PARAMETERS				
VMIN		127	V	Peak input voltage at VACMIN
VMAX		431	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.42		Minimum duty cycle at peak of VACMIN
IAVG		0.76	A	Average Primary Current
IP		1.96	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS		0.76	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP		984	uH	Primary Inductance
NP		155		Primary Winding Number of Turns
ALG		41	nH/T^2	Gapped Core Effective Inductance
BM		2397	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3279	Gauss	Peak Flux Density (BP<4200)
BAC		599	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		842		Relative Permeability of Ungapped Core
LG		1.55	mm	Gap Length (Lg > 0.1 mm)
BWE		72.8	mm	Effective Bobbin Width
OD		0.47	mm	Maximum Primary Wire Diameter including insulation
INS		0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.41	mm	Bare conductor diameter
AWG		27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		203	Cmils	Bare conductor effective area in circular mils
CMA		269	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

9 Heat Sink Assembly

9.1 Heat Sink Fabrication Drawing

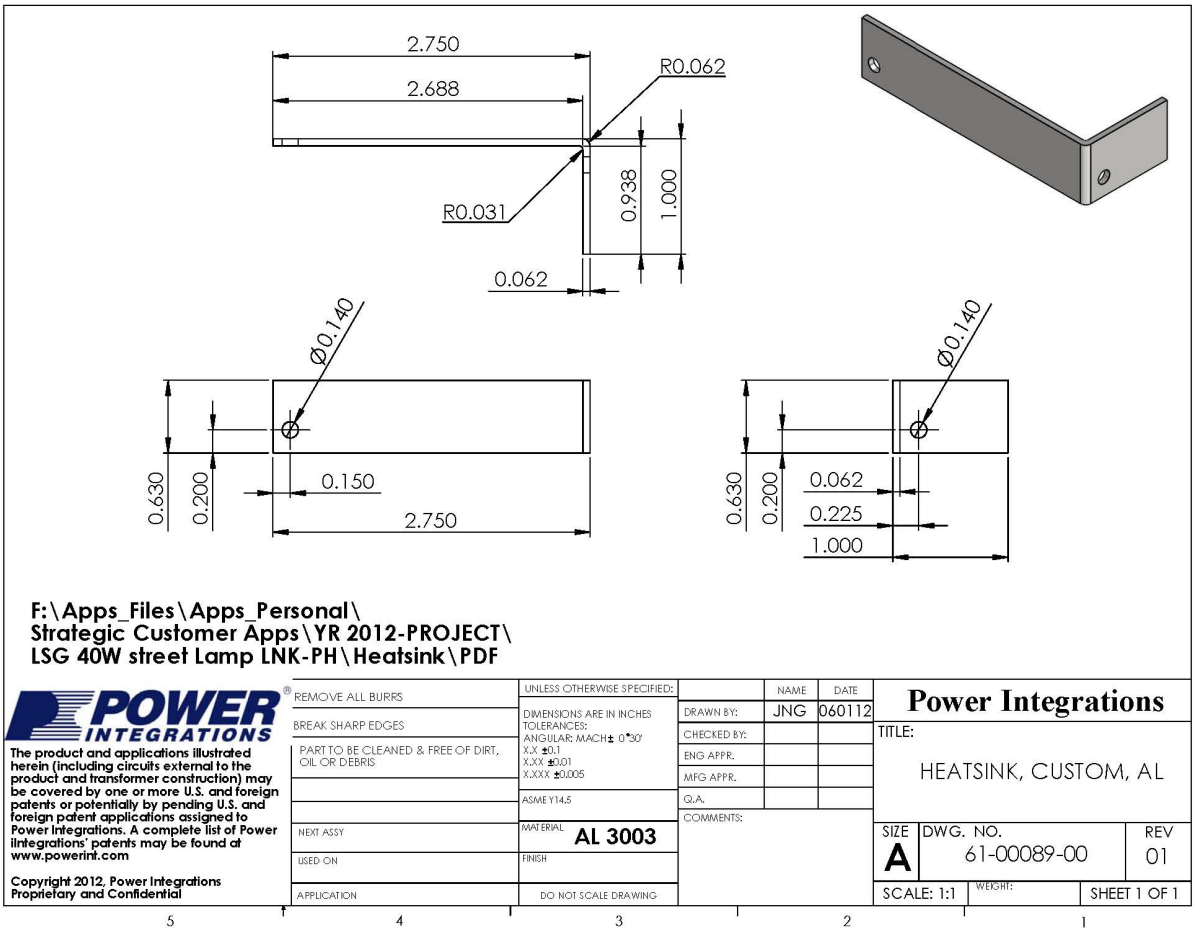

Figure 9 – Heat Sink Fabrication Drawing (Inches).

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9.2 Heat Sink Assembly Drawing

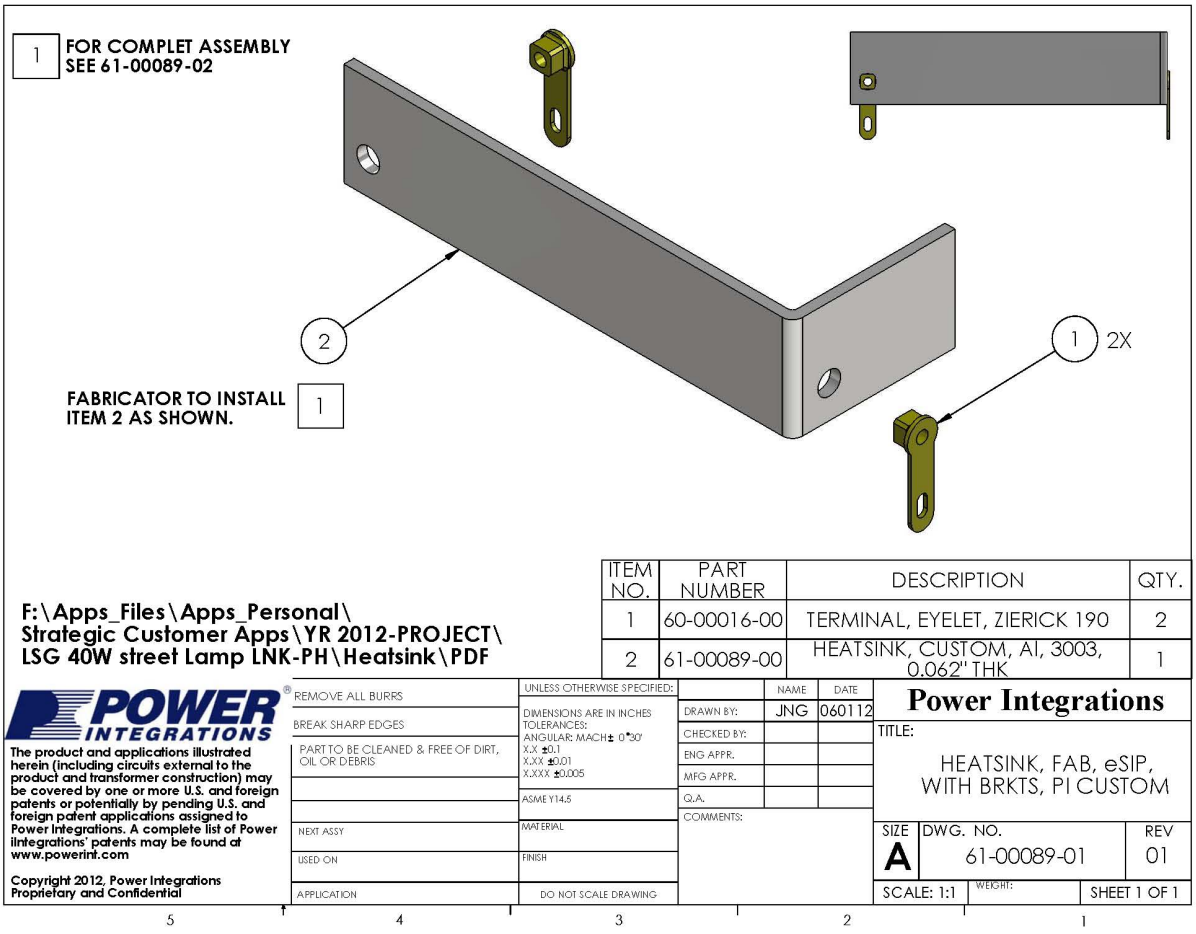

Figure 10 – Heat Sink Assembly Drawing.

9.3 Heat Sink, LNK419EG and Diode Assembly Drawing

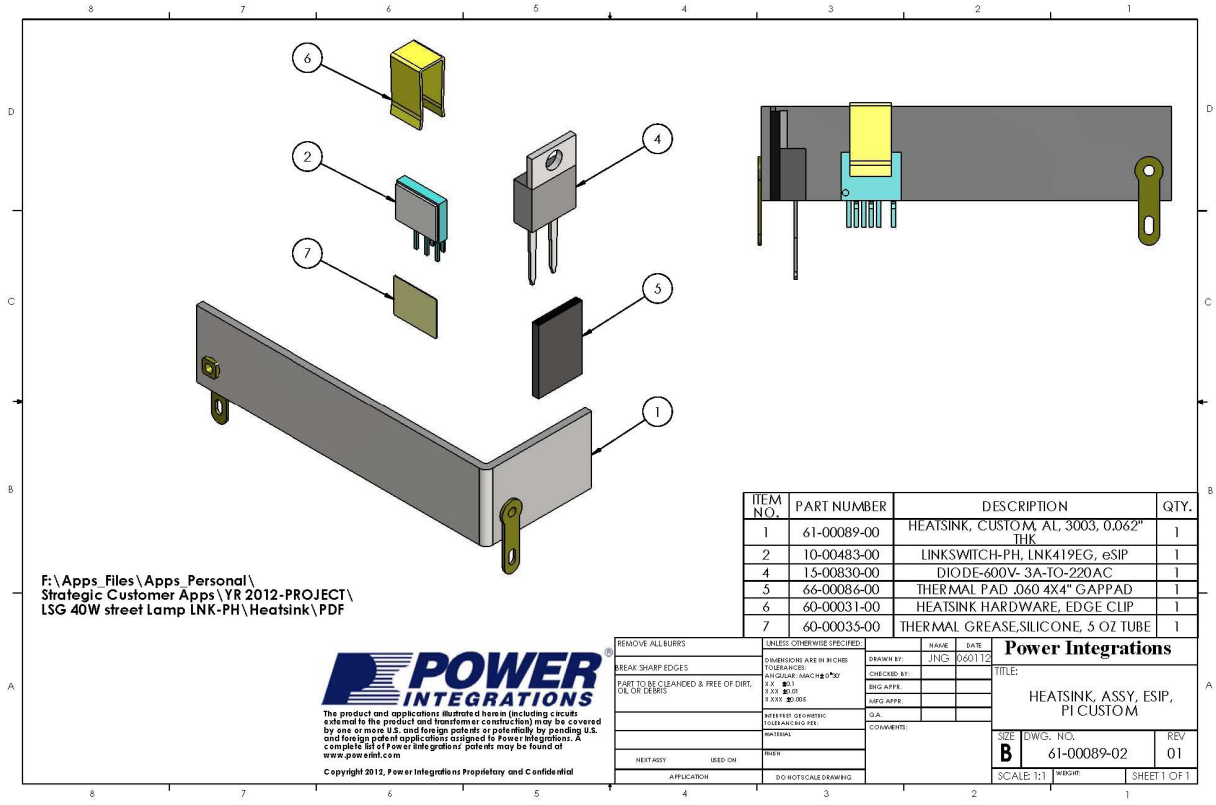

Figure 11 – Heat Sink, LNK419EG and Diode Assembly Drawing.

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10 Performance Data

All measurements were performed at room temperature using an LED load. The following data was measured using 3 sets of loads representing voltages of 51 V to 57 V. The table in Section 10.6 shows values.

10.1 Efficiency

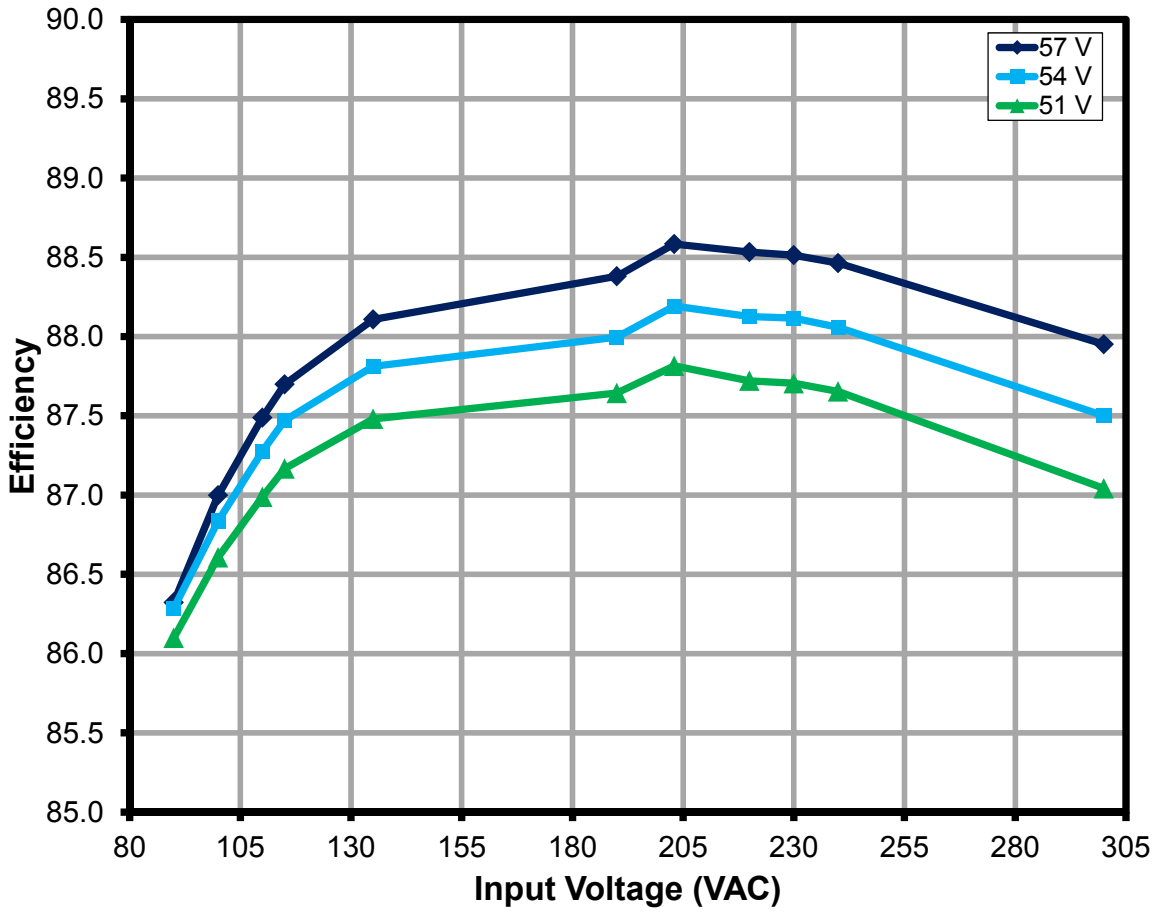

Figure 12 – Efficiency vs. Line and Load.

10.2 Line and Load Regulation

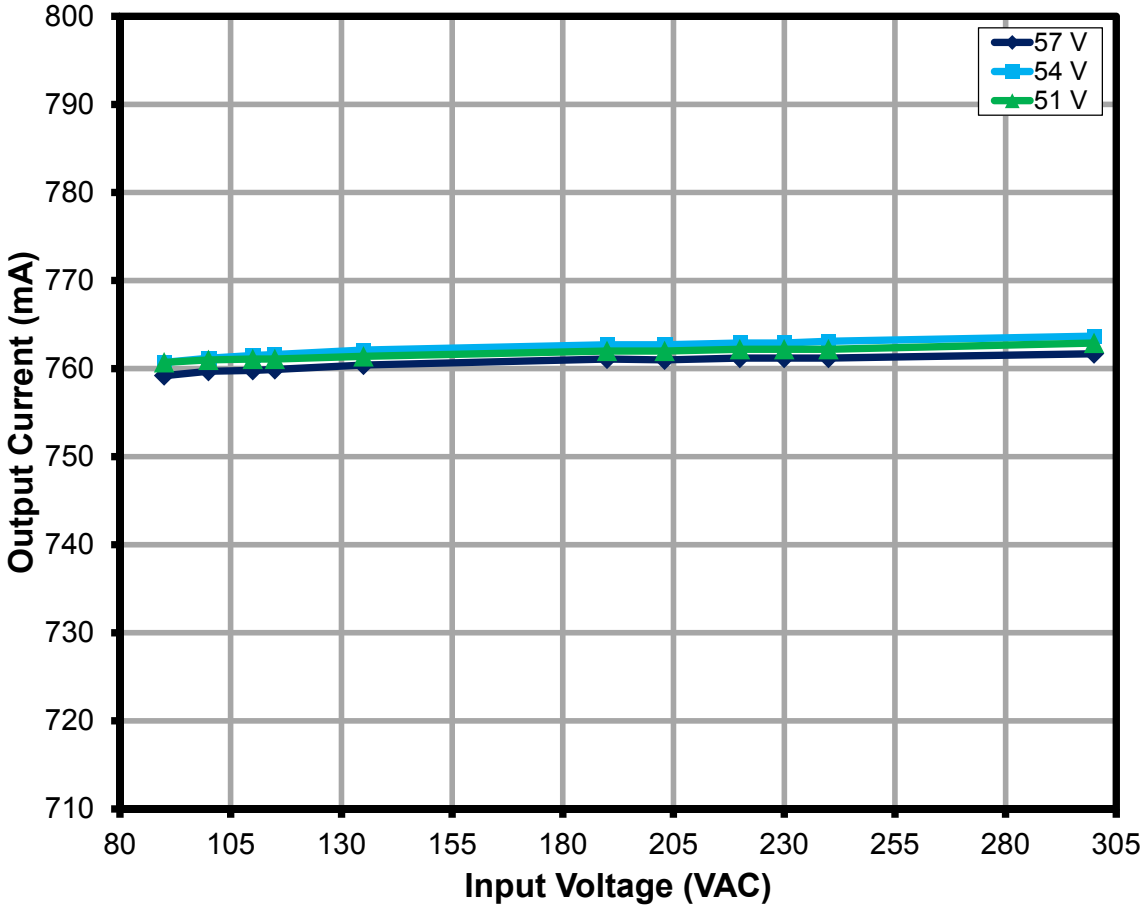

Figure 13 – Regulation vs. Line and Load.

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10.3 Power Factor

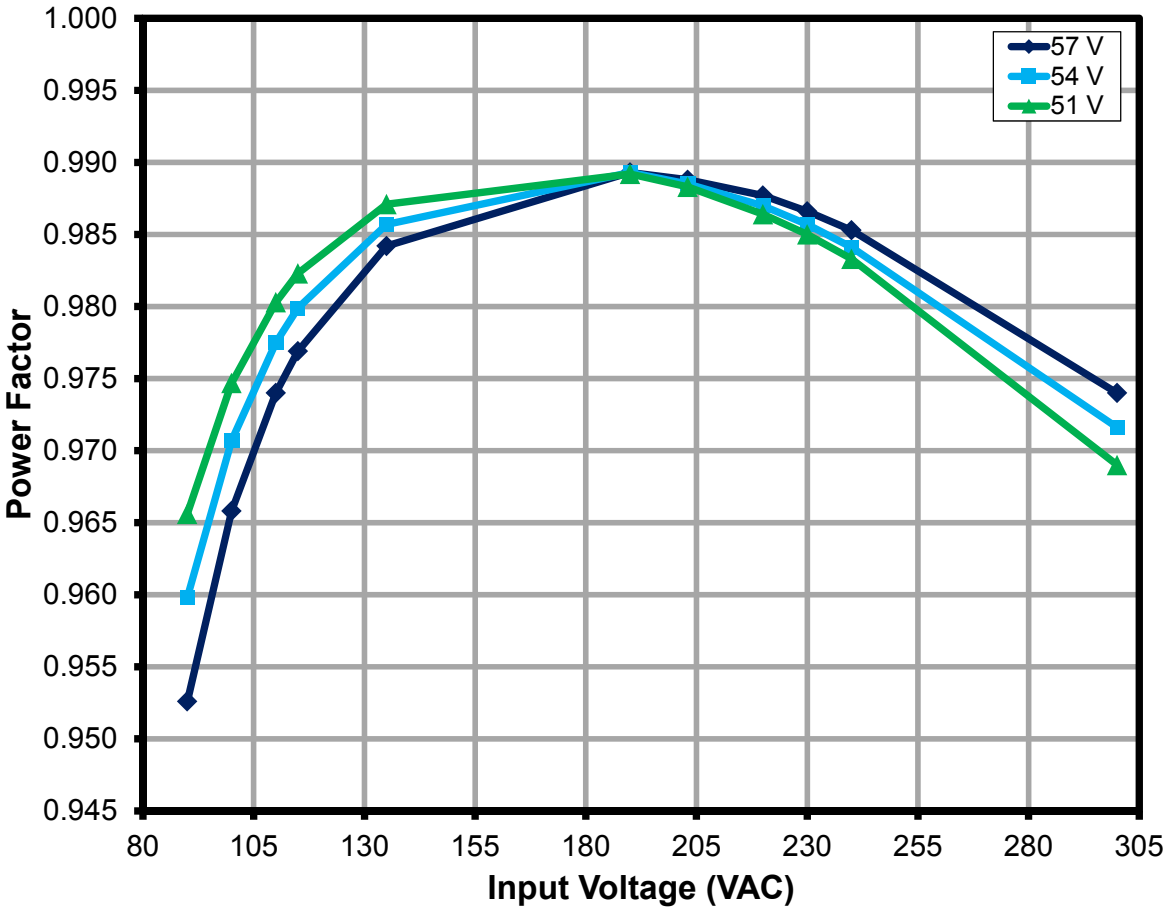

Figure 14 – Power Factor vs. Line and Load.

10.4 A-THD

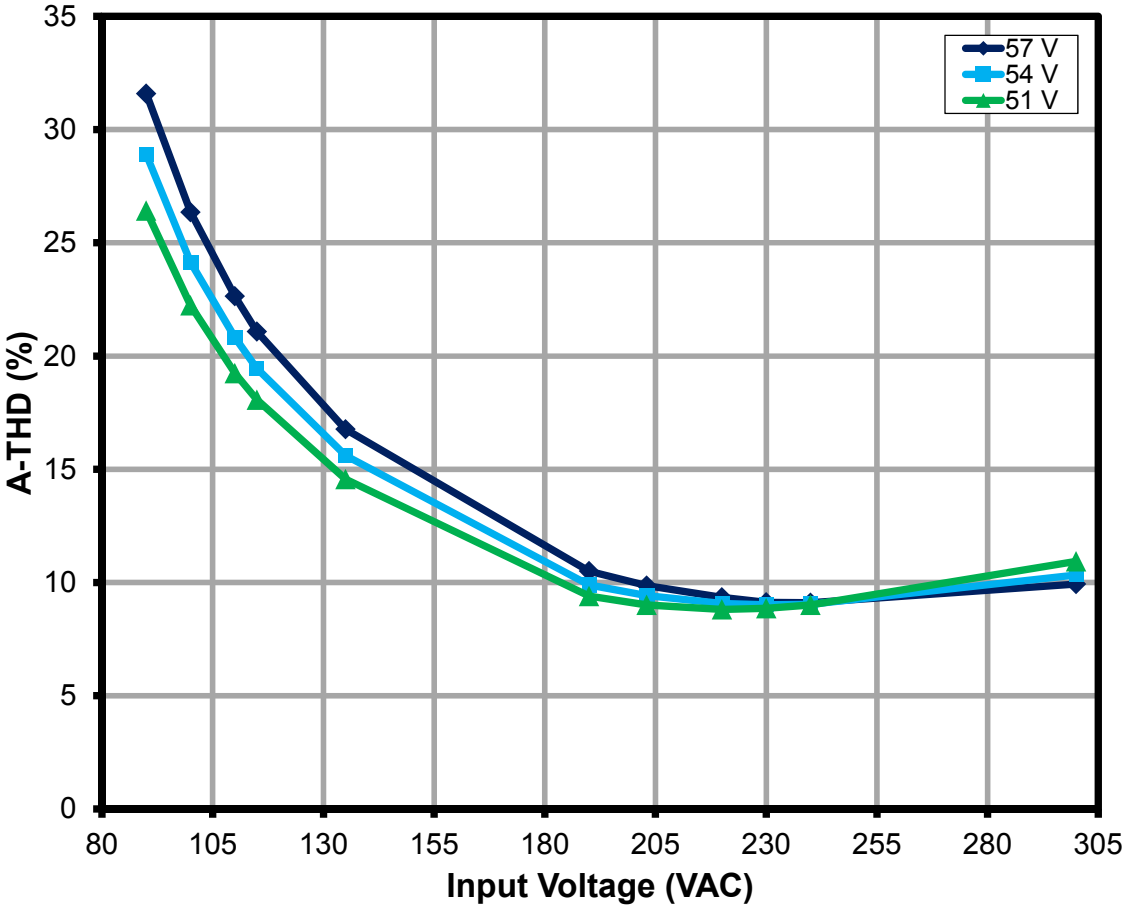

Figure 15 – A-THD vs. Line and Load.

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10.5 Harmonic Currents

The design met the limits for Class C equipment for an active input power of >25 W.

10.5.1 57 V LED Load

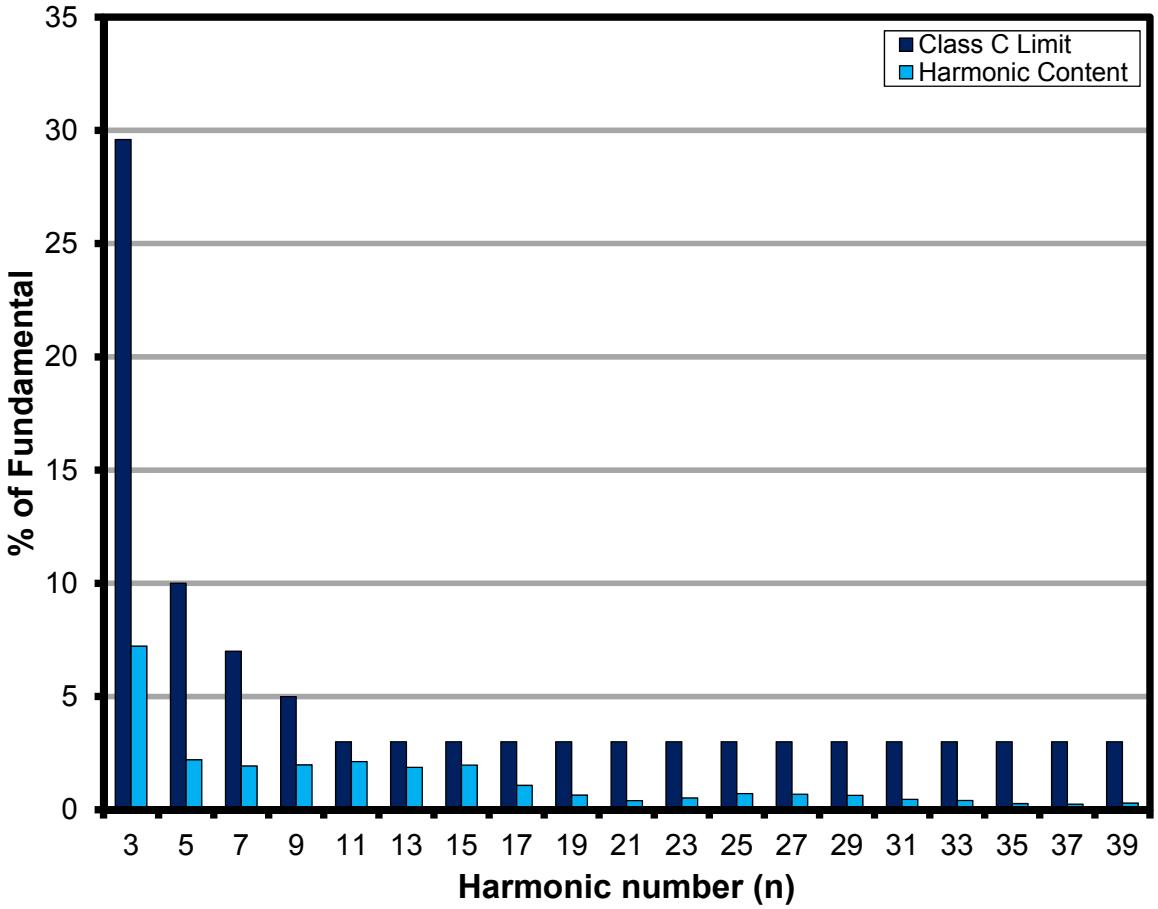

Figure 16 – 57 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

10.5.3 54 V LED Load

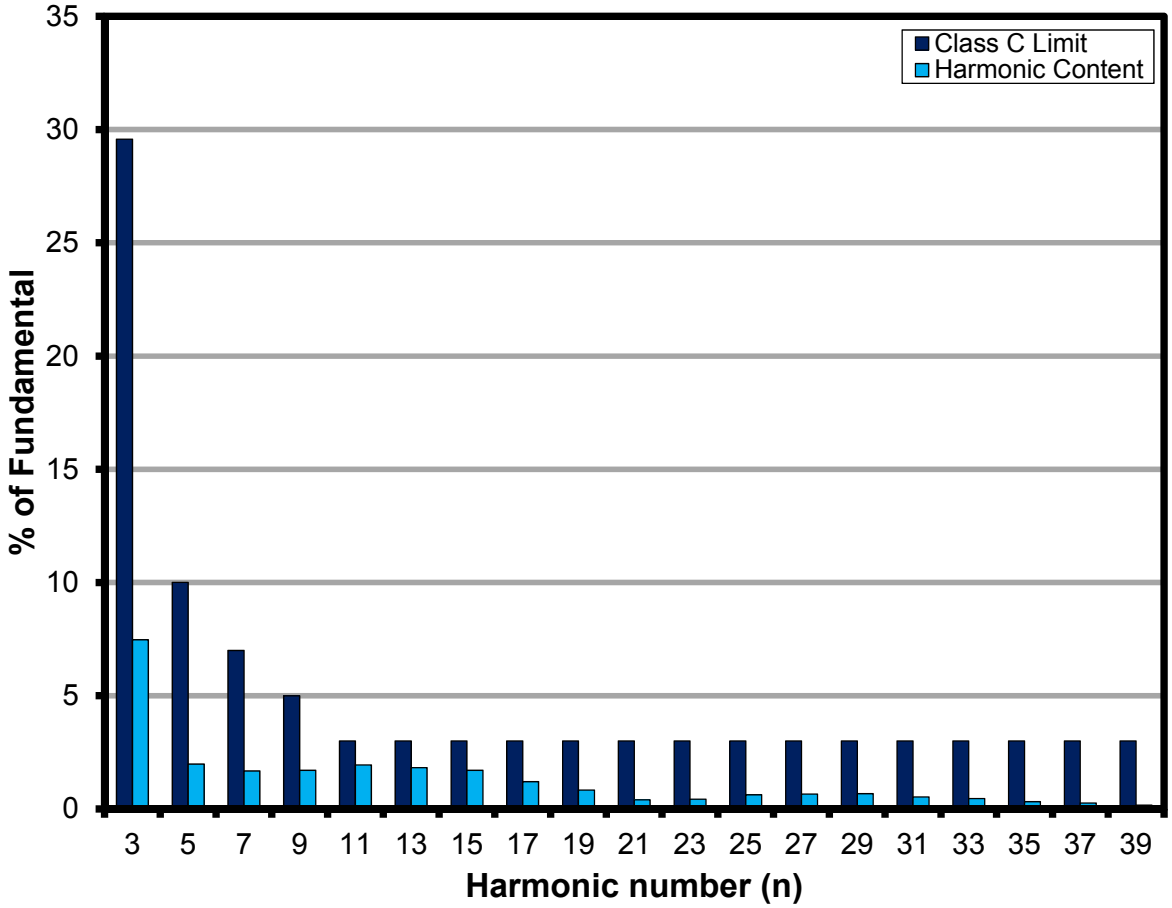

Figure 17 – 54 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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10.5.4 51 V LED Load

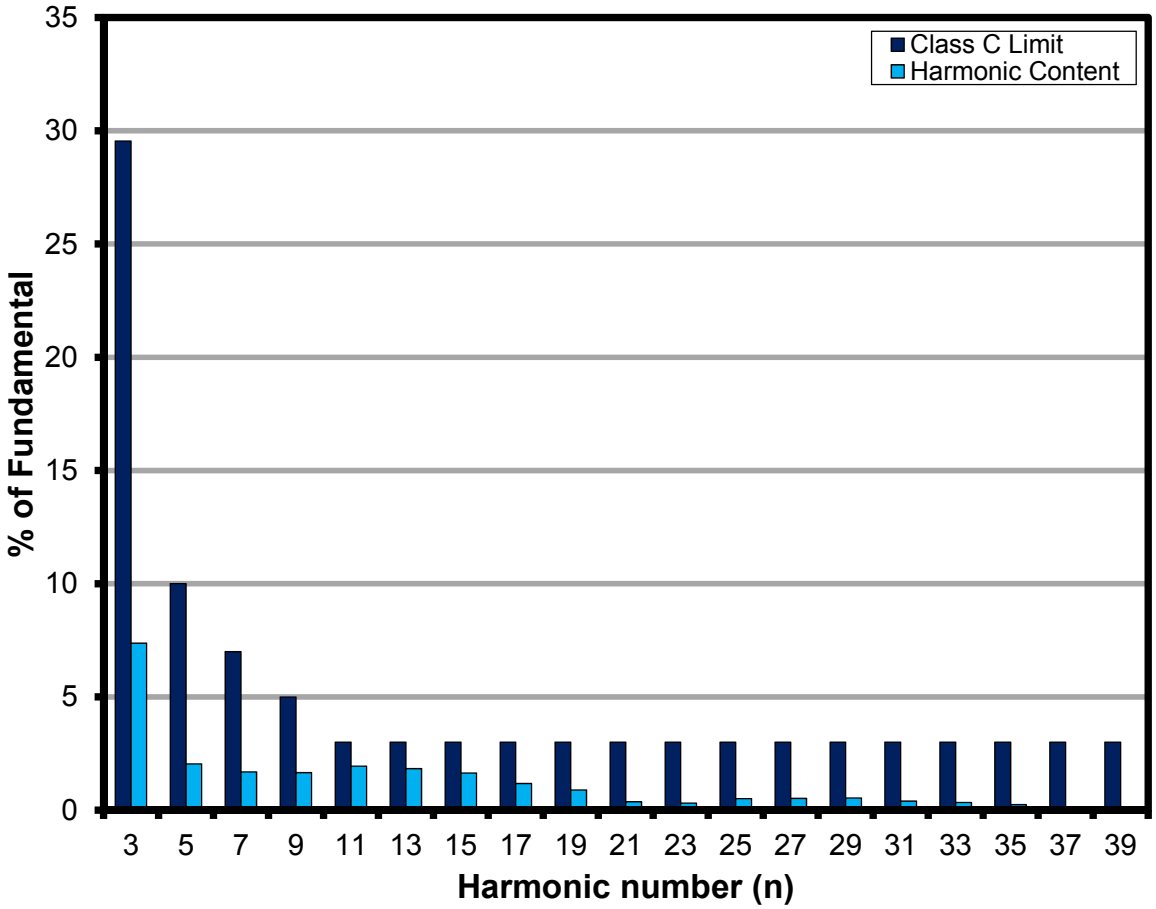

Figure 18 – 51 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

10.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient.

10.6.1 Test Data, 57 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
89.92	597.64	51.19	0.95	31.58	57.65	759.20	44.19	43.77	86.32	7.00
99.90	526.40	50.79	0.97	26.35	57.66	759.70	44.18	43.80	87.00	6.60
109.97	471.27	50.48	0.97	22.64	57.66	759.80	44.16	43.81	87.49	6.32
114.96	448.31	50.35	0.98	21.08	57.66	759.90	44.16	43.81	87.70	6.19
135.00	377.27	50.13	0.98	16.76	57.67	760.40	44.16	43.85	88.11	5.96
190.07	266.56	50.12	0.99	10.50	57.67	761.10	44.30	43.89	88.38	5.82
203.06	249.00	50.00	0.99	9.86	57.67	761.00	44.29	43.89	88.58	5.71
220.08	230.22	50.04	0.99	9.34	57.67	761.20	44.30	43.90	88.53	5.74
230.14	220.42	50.05	0.99	9.12	57.67	761.20	44.30	43.90	88.51	5.75
240.11	211.66	50.08	0.99	9.11	57.68	761.20	44.30	43.90	88.46	5.78
300.19	172.44	50.42	0.97	9.93	57.69	761.70	44.35	43.94	87.95	6.08

10.6.2 Test Data, 54 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
89.92	561.55	48.47	0.96	28.90	54.43	760.70	41.82	41.41	86.29	6.65
99.91	496.42	48.14	0.97	24.14	54.43	761.20	41.81	41.43	86.84	6.34
109.98	445.45	47.89	0.98	20.82	54.42	761.50	41.80	41.44	87.28	6.09
114.97	423.91	47.76	0.98	19.45	54.40	761.60	41.78	41.43	87.47	5.98
135.01	357.52	47.58	0.99	15.61	54.41	762.10	41.78	41.46	87.81	5.80
190.08	253.27	47.62	0.99	9.89	54.40	762.70	41.91	41.49	88.00	5.72
203.07	236.67	47.51	0.99	9.42	54.39	762.70	41.90	41.48	88.19	5.61
220.09	218.91	47.55	0.99	9.08	54.38	762.90	41.90	41.49	88.13	5.65
230.15	209.68	47.56	0.99	9.02	54.38	762.90	41.91	41.49	88.12	5.65
240.11	201.44	47.60	0.98	9.04	54.38	763.10	41.92	41.50	88.06	5.68
300.19	164.46	47.96	0.97	10.33	54.39	763.70	41.97	41.53	87.50	6.00

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10.6.3 Test Data, 51 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
89.94	529.65	46.00	0.97	26.42	51.54	760.70	39.60	39.21	86.10	6.39
99.92	469.42	45.72	0.97	22.23	51.54	761.00	39.60	39.22	86.61	6.12
109.99	421.97	45.50	0.98	19.24	51.54	761.10	39.58	39.23	86.99	5.92
114.98	401.94	45.40	0.98	18.07	51.54	761.10	39.57	39.23	87.17	5.83
135.01	339.42	45.23	0.99	14.57	51.55	761.40	39.57	39.25	87.48	5.66
190.08	240.90	45.30	0.99	9.40	51.55	762.00	39.70	39.28	87.64	5.60
203.07	225.27	45.21	0.99	9.01	51.55	762.00	39.70	39.28	87.81	5.51
220.09	208.51	45.27	0.99	8.81	51.55	762.20	39.71	39.29	87.72	5.56
230.15	199.75	45.28	0.99	8.86	51.55	762.20	39.71	39.29	87.71	5.57
240.11	191.92	45.31	0.98	9.01	51.56	762.20	39.72	39.30	87.65	5.59
300.19	157.10	45.70	0.97	10.93	51.56	762.90	39.78	39.34	87.04	5.92

10.6.4 230 VAC 50 Hz, 57 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	220.42	50.0500	0.9866	9.12
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
1	218.64				
2	0.16	0.07%		2.00%	
3	15.80	7.23%	170.1700	29.60%	Pass
5	4.82	2.20%	95.0950	10.00%	Pass
7	4.22	1.93%	50.0500	7.00%	Pass
9	4.32	1.98%	25.0250	5.00%	Pass
11	4.66	2.13%	17.5175	3.00%	Pass
13	4.09	1.87%	14.8225	3.00%	Pass
15	4.30	1.97%	12.8462	3.00%	Pass
17	2.35	1.07%	11.3349	3.00%	Pass
19	1.42	0.65%	10.1417	3.00%	Pass
21	0.88	0.40%	9.1758	3.00%	Pass
23	1.13	0.52%	8.3779	3.00%	Pass
25	1.57	0.72%	7.7077	3.00%	Pass
27	1.49	0.68%	7.1368	3.00%	Pass
29	1.39	0.64%	6.6446	3.00%	Pass
31	1.01	0.46%	6.2159	3.00%	Pass
33	0.90	0.41%	5.8392	3.00%	Pass
35	0.60	0.27%	5.5055	3.00%	Pass
37	0.52	0.24%	5.2079	3.00%	Pass
39	0.64	0.29%	4.9408	3.00%	Pass
41	0.75	0.34%			
43	0.84	0.38%			
45	0.62	0.28%			
47	0.45	0.21%			
49	0.49	0.22%			

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10.6.5 230 VAC 50 Hz, 54 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	209.68	47.5600	0.9857	9.02
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
1	207.84				
2	0.16	0.08%		2.00%	
3	15.53	7.47%	161.7040	29.57%	Pass
5	4.12	1.98%	90.3640	10.00%	Pass
7	3.48	1.67%	47.5600	7.00%	Pass
9	3.54	1.70%	23.7800	5.00%	Pass
11	4.04	1.94%	16.6460	3.00%	Pass
13	3.78	1.82%	14.0851	3.00%	Pass
15	3.54	1.70%	12.2071	3.00%	Pass
17	2.51	1.21%	10.7709	3.00%	Pass
19	1.72	0.83%	9.6372	3.00%	Pass
21	0.83	0.40%	8.7193	3.00%	Pass
23	0.89	0.43%	7.9611	3.00%	Pass
25	1.31	0.63%	7.3242	3.00%	Pass
27	1.36	0.65%	6.7817	3.00%	Pass
29	1.41	0.68%	6.3140	3.00%	Pass
31	1.10	0.53%	5.9066	3.00%	Pass
33	0.95	0.46%	5.5487	3.00%	Pass
35	0.67	0.32%	5.2316	3.00%	Pass
37	0.55	0.26%	4.9488	3.00%	Pass
39	0.35	0.17%	4.6950	3.00%	Pass
41	0.55	0.26%			
43	0.66	0.32%			
45	0.82	0.39%			
47	0.86	0.41%			
49	0.78	0.38%			

10.6.6 230 VAC 50 Hz, 51 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	199.75	45.2800	0.9850	8.86
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
1	197.97				
2	0.09	0.05%		2.00%	
3	14.59	7.37%	153.9520	29.55%	Pass
5	4.04	2.04%	86.0320	10.00%	Pass
7	3.34	1.69%	45.2800	7.00%	Pass
9	3.27	1.65%	22.6400	5.00%	Pass
11	3.84	1.94%	15.8480	3.00%	Pass
13	3.63	1.83%	13.4098	3.00%	Pass
15	3.24	1.64%	11.6219	3.00%	Pass
17	2.33	1.18%	10.2546	3.00%	Pass
19	1.76	0.89%	9.1752	3.00%	Pass
21	0.74	0.37%	8.3013	3.00%	Pass
23	0.62	0.31%	7.5795	3.00%	Pass
25	1.00	0.51%	6.9731	3.00%	Pass
27	1.02	0.52%	6.4566	3.00%	Pass
29	1.06	0.54%	6.0113	3.00%	Pass
31	0.80	0.40%	5.6235	3.00%	Pass
33	0.68	0.34%	5.2827	3.00%	Pass
35	0.48	0.24%	4.9808	3.00%	Pass
37	0.31	0.16%	4.7116	3.00%	Pass
39	0.23	0.12%	4.4699	3.00%	Pass
41	0.26	0.13%			
43	0.27	0.14%			
45	0.45	0.23%			
47	0.40	0.20%			
49	0.63	0.32%			

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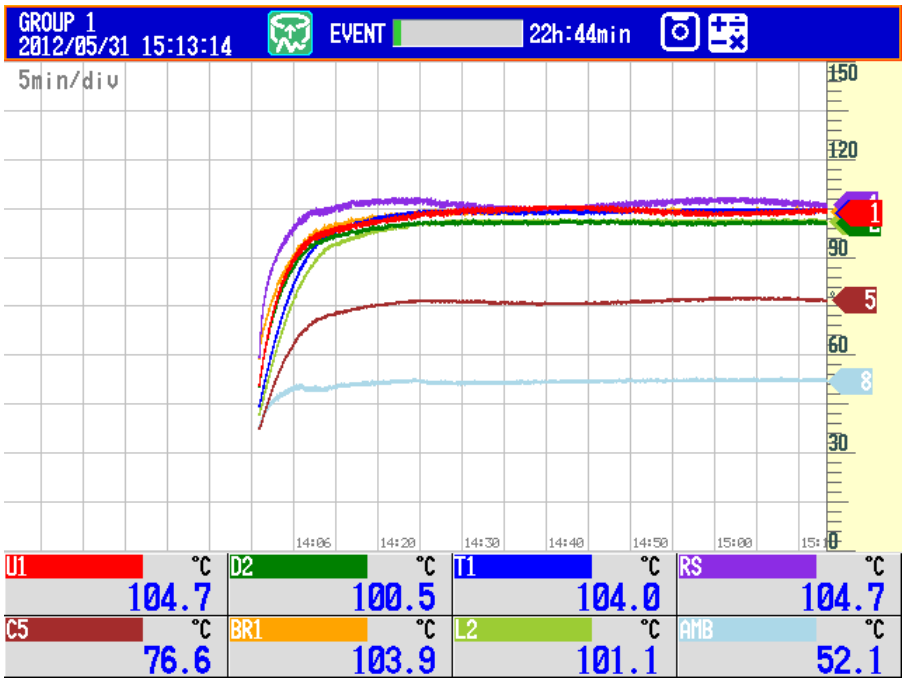
11 Thermal Performance

11.1 Test Set-up

The unit was placed inside a box in the chamber that was set to deliver an ambient of ~50˚C (ambient inside the box). Thermal measurements were taken after 1 hour for each line condition.

Figure 19 – Thermal Test Set-up.

11.2 90 VAC, 60 Hz, 54 V LED Load



Part Ref	Description	Temp, ˚C	ΔT, ˚C
U1	LinkSwitch-PH	104.7	52.6
D2	Output Diode	100.5	48.4
T1	Inductor	104.0	51.9
R17	Current Sense Resistor	104.7	52.6
C5	Output Capacitor	76.6	24.5
BR1	Bridge Diode	103.9	51.8
L2	Differential Choke	101.1	49.0
AMB	Ambient Inside the Box	52.1	

Figure 20 – Thermal Reading at 90 VAC, 60 Hz.

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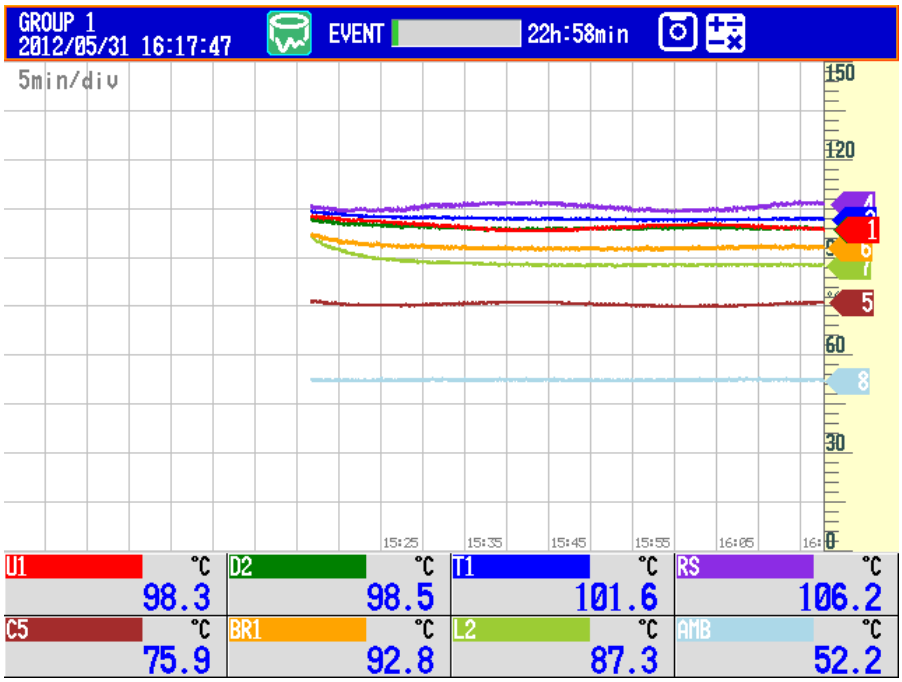
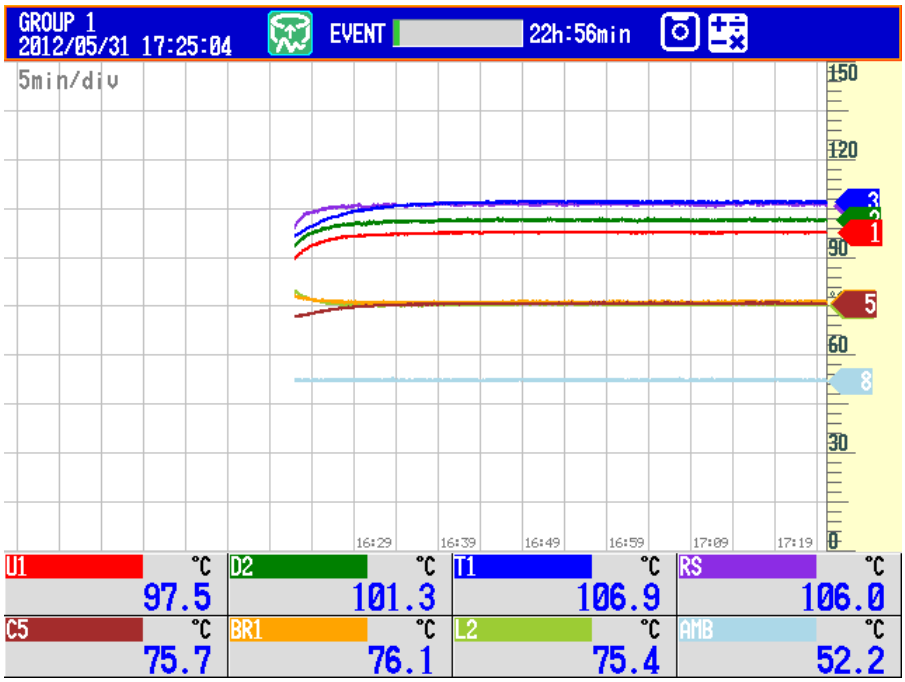
11.3 115 VAC, 60 Hz, 54 V LED Load



Part Ref	Description	Temp, ˚C	ΔT, ˚C
U1	LinkSwitch-PH	98.3	46.1
D2	Output Diode	98.5	46.3
T1	Inductor	101.6	49.4
R17	Current Sense Resistor	106.2	54.0
C5	Output Capacitor	75.9	23.7
BR1	Bridge Diode	92.8	40.6
L2	Differential Choke	87.3	35.1
AMB	Ambient Inside the Box	52.2	

Figure 21 – Thermal Reading at 115 VAC, 60 Hz.

11.4 230 VAC, 50 Hz, 54 V LED Load



Part Ref	Description	Temp, ˚C	ΔT, ˚C
U1	LinkSwitch-PH	97.5	45.3
D2	Output Diode	101.3	49.1
T1	Inductor	106.9	54.7
R17	Current Sense Resistor	106.0	53.8
C5	Output Capacitor	75.7	23.5
BR1	Bridge Diode	76.1	23.9
L2	Differential Choke	75.4	23.2
AMB	Ambient Inside the Box	52.2	

Figure 22 – Thermal Reading at 230 VAC, 50 Hz.

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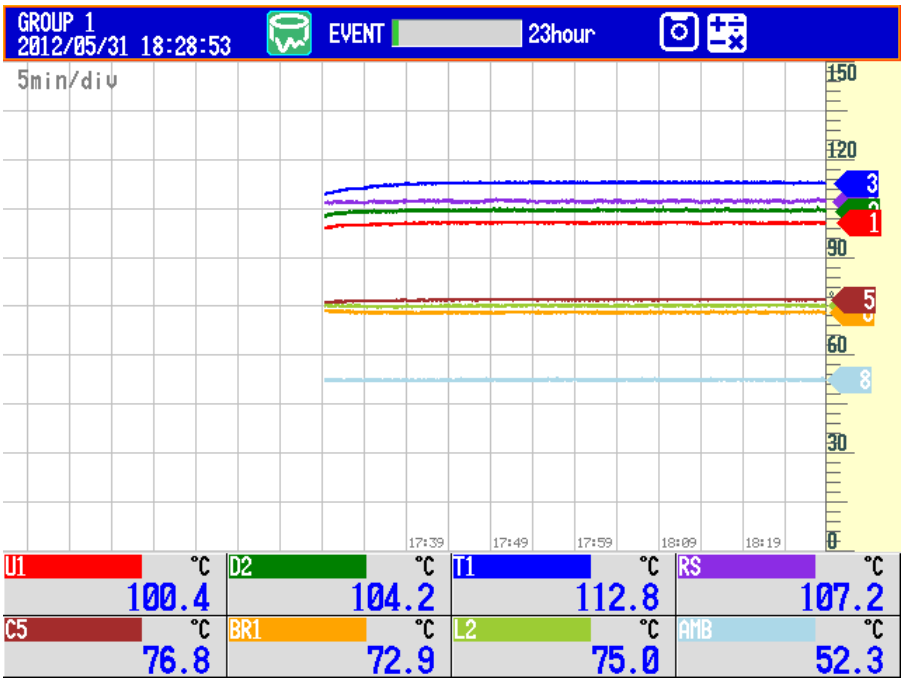
11.5 300 VAC, 50 Hz, 54 V LED Load



Part Ref	Description	Temp, ˚C	ΔT, ˚C
U1	LinkSwitch-PH	100.4	48.1
D2	Output Diode	104.2	51.9
T1	Inductor	112.8	60.5
R17	Current Sense Resistor	107.2	54.9
C5	Output Capacitor	76.8	24.5
BR1	Bridge Diode	72.9	20.6
L2	Differential Choke	75.0	22.7
AMB	Ambient Inside the Box	52.3	

Figure 23 – Thermal Reading at 300 VAC, 50 Hz.

12 Waveforms

12.1 Input Line Voltage and Current

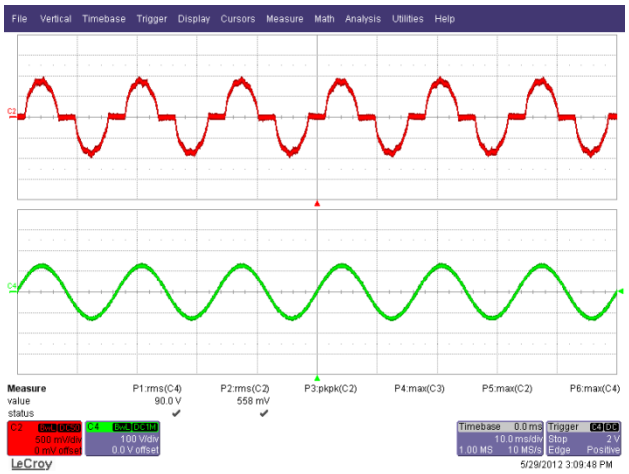


Figure 24 – 90 VAC, Full Load.
Upper: I_{IN}, 500 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

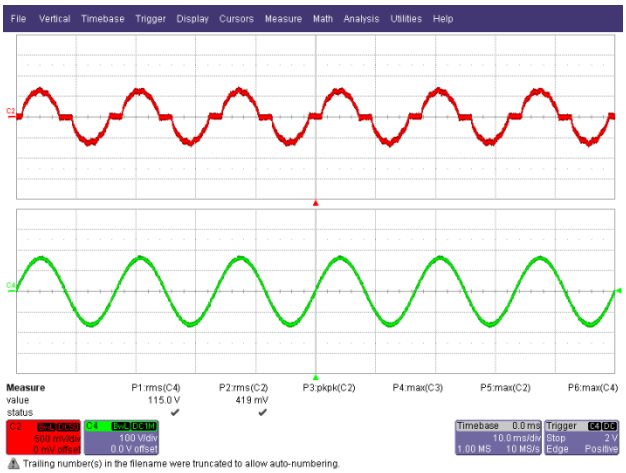


Figure 25 – 115 VAC, Full Load.
Upper: I_{IN}, 500 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

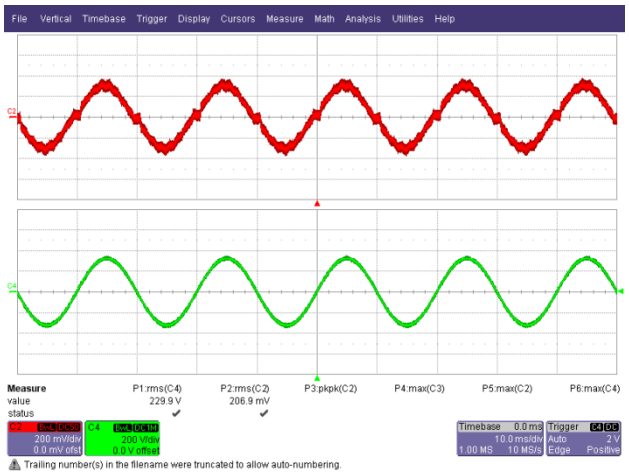


Figure 26 – 230 VAC, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

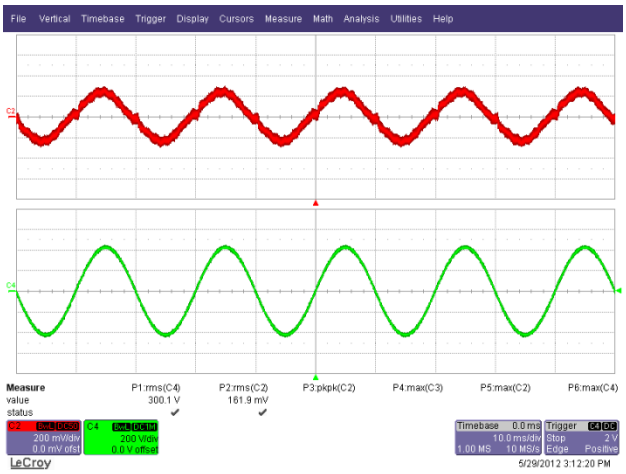


Figure 27 – 300 VAC, Full Load.
Upper: I_{IN}, 200 mA / div.
Lower: V_{IN}, 200 V, 10 ms / div.

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12.2 Output Voltage and Current at Normal Operation

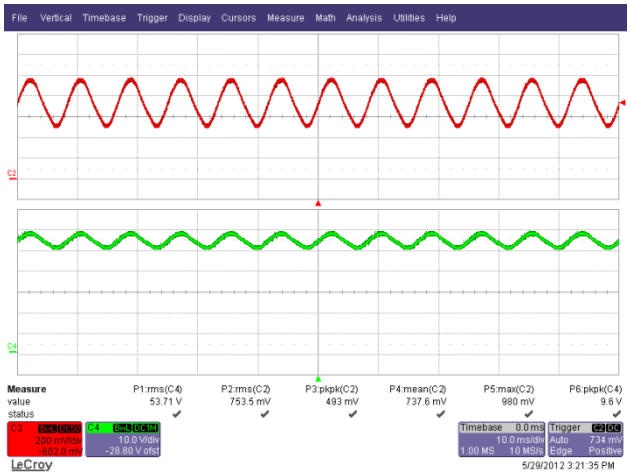

Figure 28 – 90 VAC, Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{OUT}, 10 V, 10 ms / div.

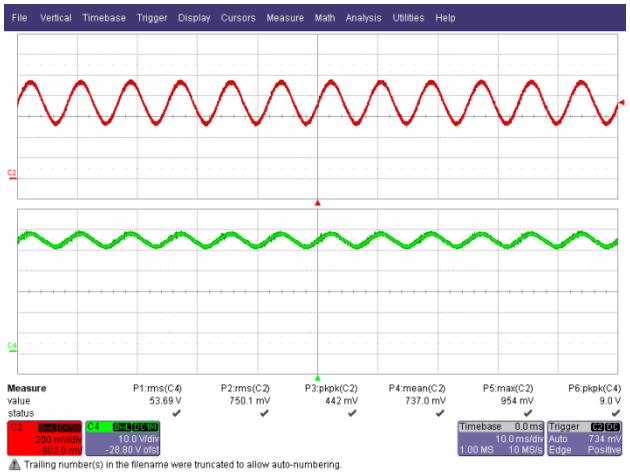

Figure 29 – 115 VAC, Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{OUT}, 10 V, 10 ms / div.

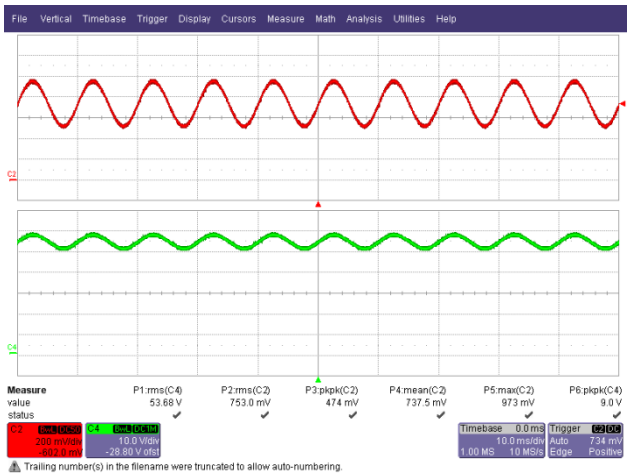

Figure 30 – 230 VAC, Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{OUT}, 10 V, 10 ms / div.

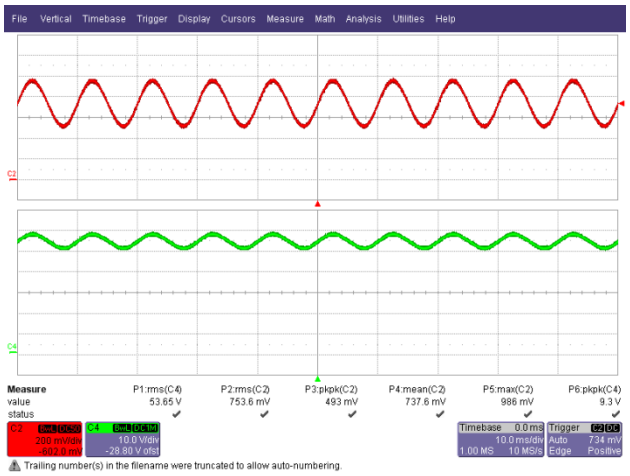

Figure 31 – 300 VAC, Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{OUT}, 10 V, 10 ms / div.

12.3 Drain Voltage and Current at Normal Operation

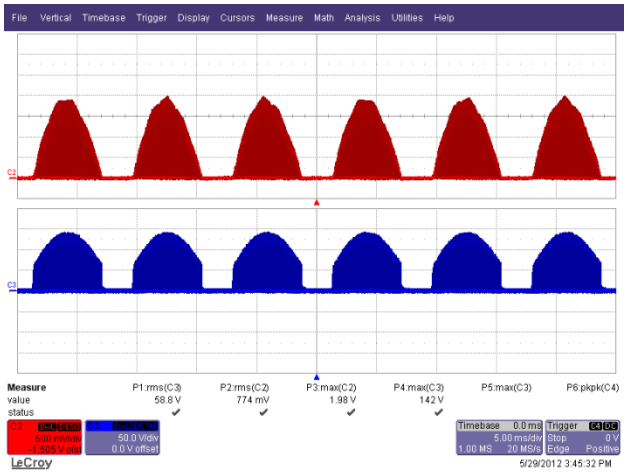

Figure 32 – 90 VAC, 60 Hz.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 5 ms / div.

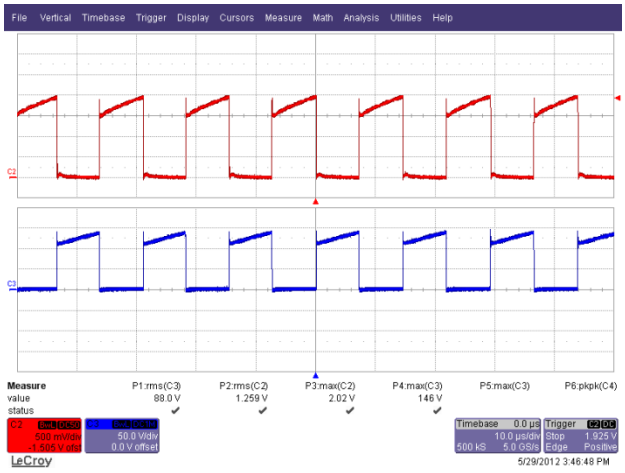

Figure 33 – 90 VAC, 60 Hz.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V / div., 10 µs / div.

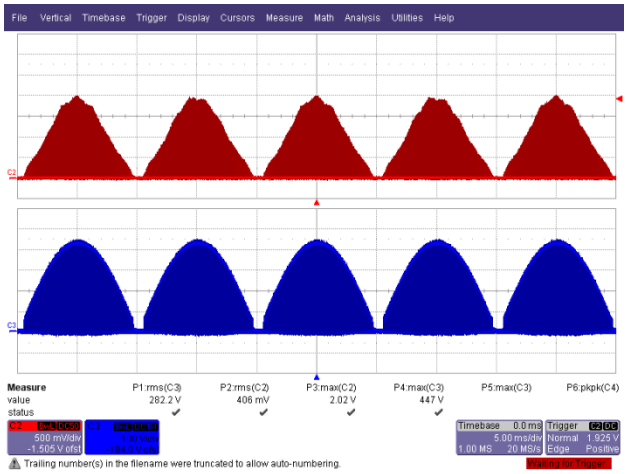

Figure 34 – 300 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

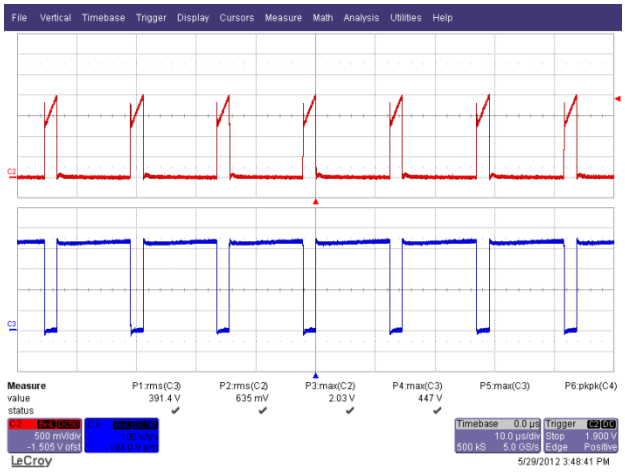

Figure 35 – 300 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 µs / div.

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12.4 Start-Up Drain Voltage and Current

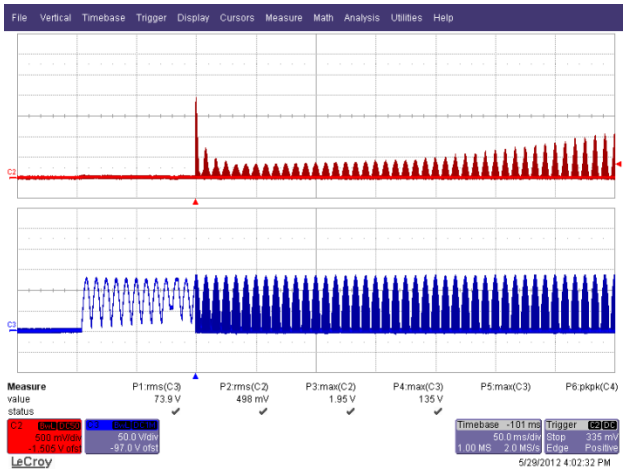

Figure 36 – 90 VAC Start-up.
Upper: I_{DRAIN}, 500 mA / div.
Lower: $V_{DRAIN,}$ 50 V, 50 ms / div.

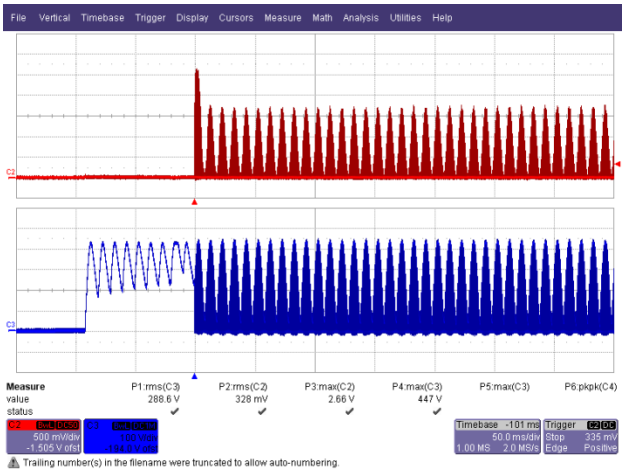

Figure 37 – 300 VAC Start-up.
Upper: I_{DRAIN}, 500 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 50 ms / div.

12.5 Start-up time

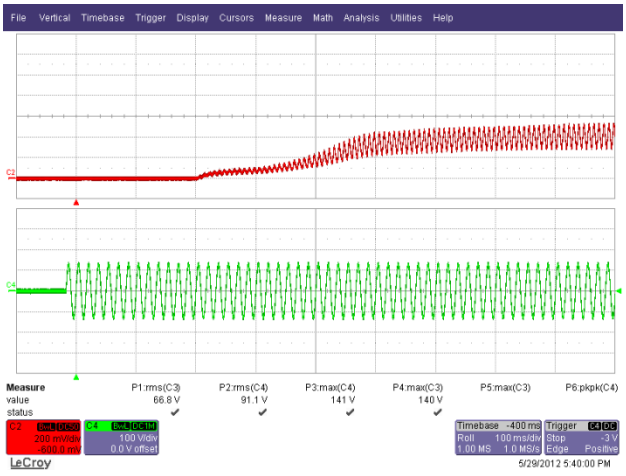

Figure 38 – 90 VAC Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

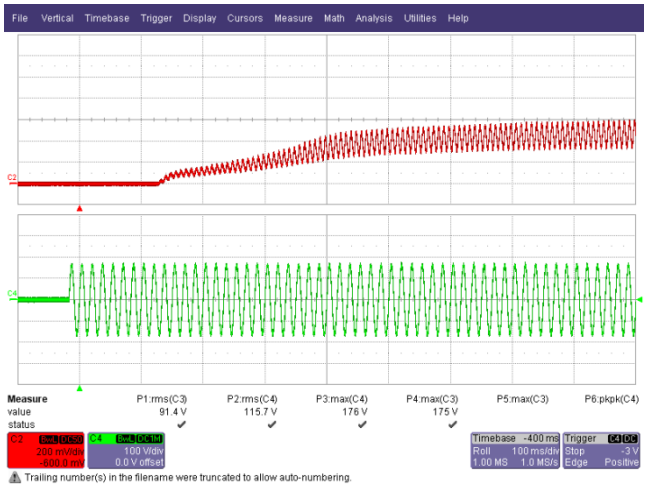

Figure 39 – 115 VAC Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 100 V / div., 100 ms / div.

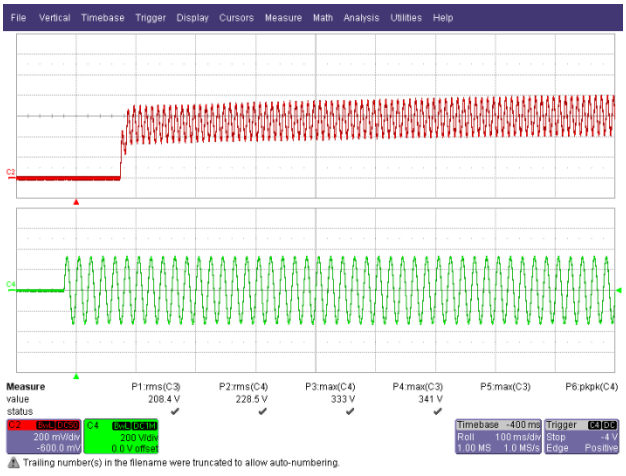

Figure 40 – 230 VAC Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 200 V / div., 100 ms / div.

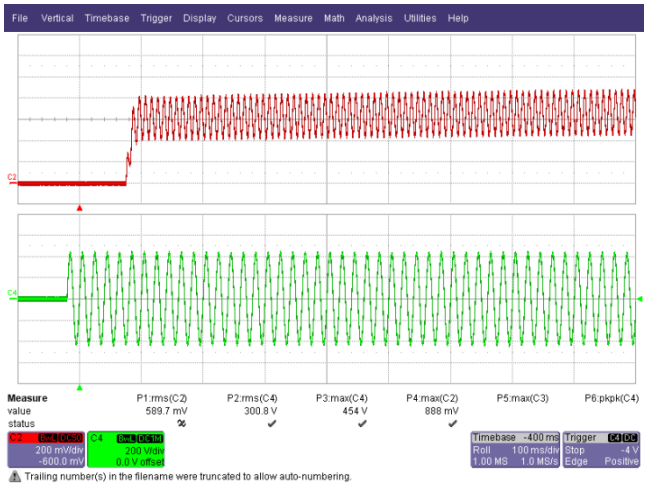

Figure 41 – 300 VAC Full Load.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 200 V / div., 100 ms / div.

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12.6 Output Current / Voltage Rise and Fall

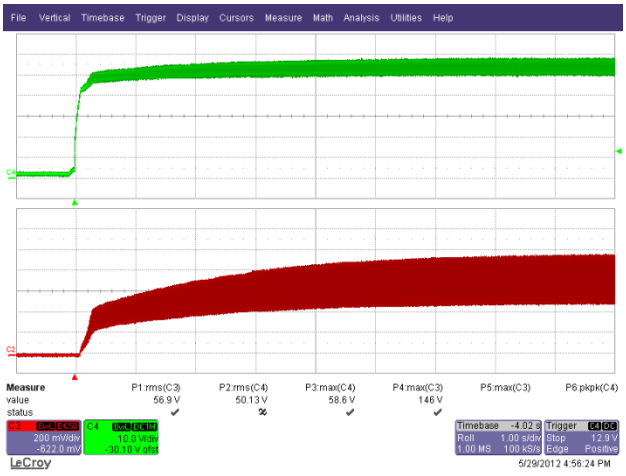

Figure 42 – 90 VAC Output Rise.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA / div., 1 s / div.

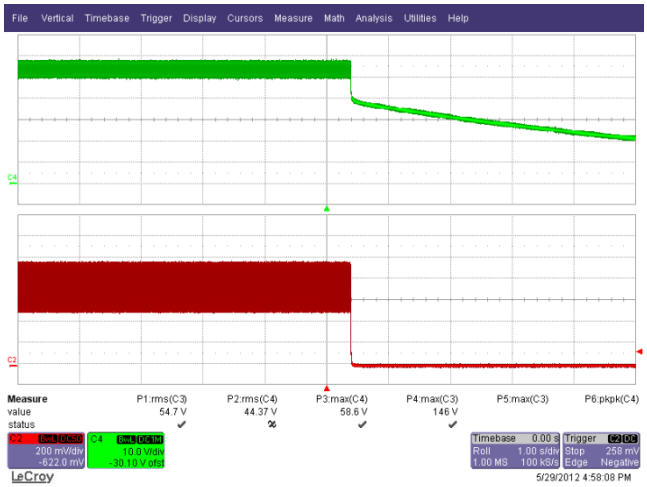

Figure 43 – 90 VAC Output Fall.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA / div., 1 s / div.

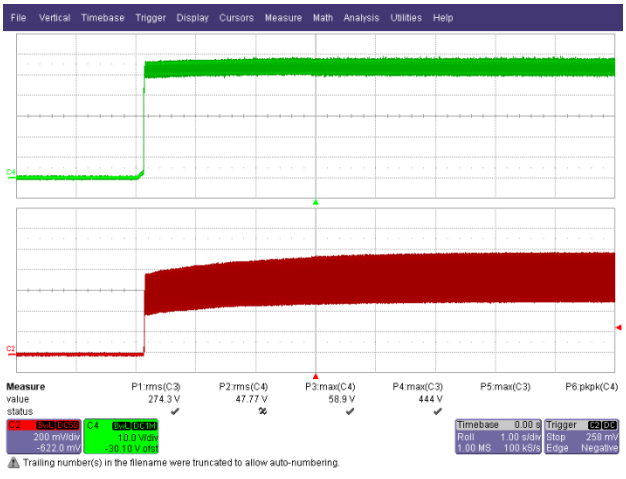

Figure 44 – 300 VAC Output Rise.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA / div., 1 s / div.

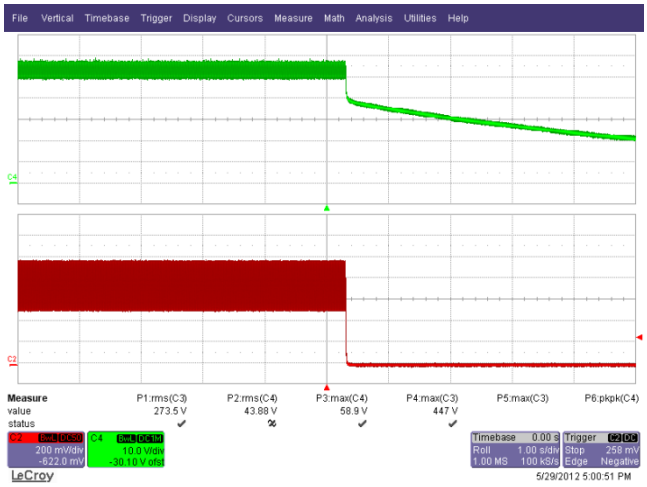

Figure 45 – 300 VAC Output Fall.
Upper: V_{OUT}, 10 V / div.
Lower: I_{OUT}, 200 mA / div., 1 s / div.

12.7 Output Current During Line Transient

During a sudden change in input voltage, output current overshoots/undershoots due to the inherently slow loop response of the system. Maximum (peak) output current for this design is shown below.

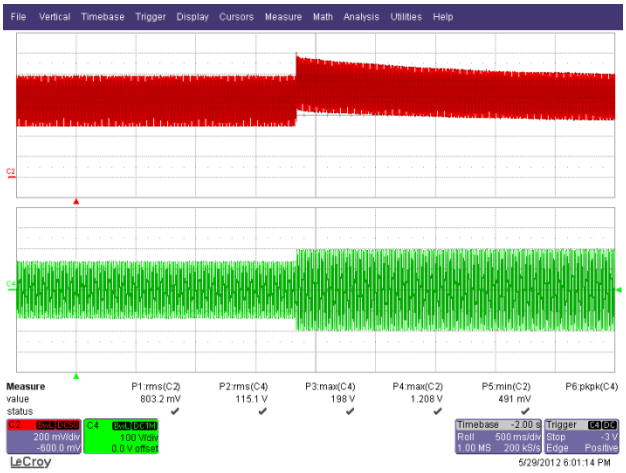

Figure 46 – 90 VAC – 132 VAC, 60 Hz.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 100 V / div., 500 ms / div.
I_{OUT} Peak: 1.21 A.

Figure 47 – 132 VAC – 90 VAC, 60 Hz.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 100 V / div., 500 ms / div.
I_{OUT} Minimum: 261 mA.

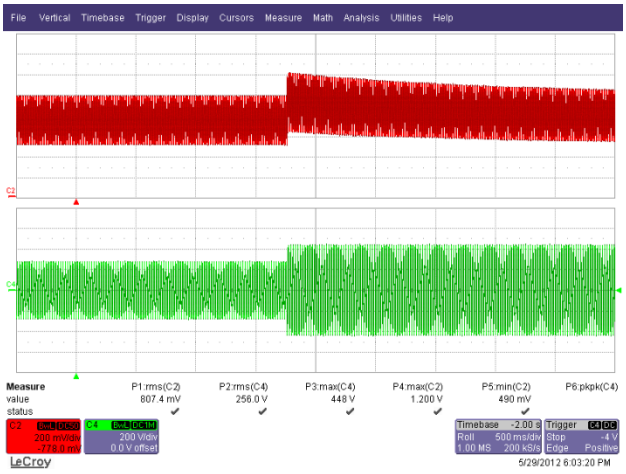

Figure 48 – 185 VAC – 300 VAC, 50 Hz.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 200 V / div., 500 ms / div.
I_{OUT} Peak: 1.21 A.

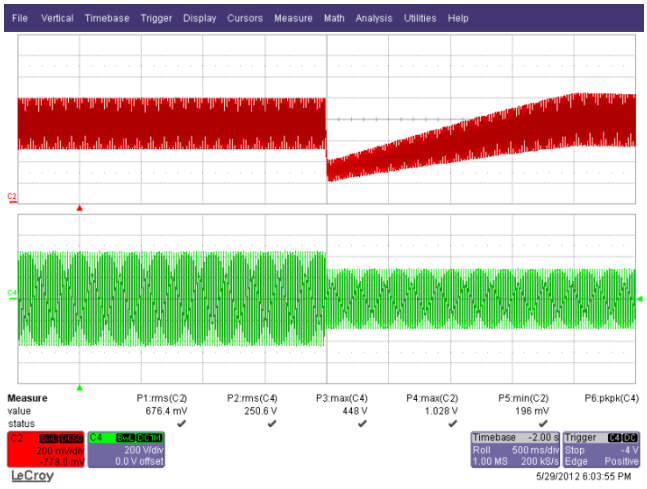

Figure 49 – 300 VAC – 185 VAC, 50 Hz.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 200 V / div., 500 ms / div.
I_{OUT} Minimum: 196 mA.

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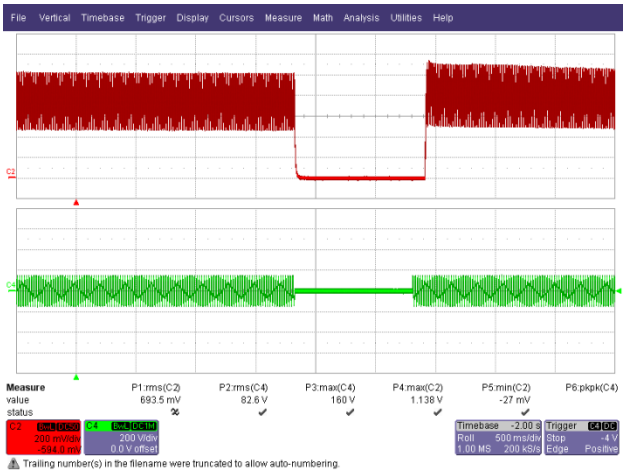

Figure 50 – 90 VAC – 0 VAC – 90 VAC, 60 Hz.
Upper: I_{OUT}, 200 mA / div.
Lower: V_{IN}, 200 V / div., 500 ms / div.
I_{OUT} Peak: 1.14 A.

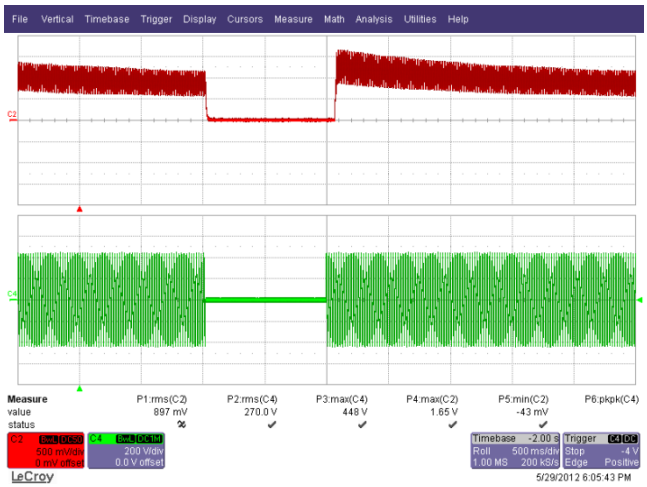

Figure 51 – 300 VAC – 0 VAC – 300 VAC, 50 Hz.
Upper: I_{OUT}, 500 mA / div.
Lower: V_{IN}, 200 V / div., 500 ms / div.
I_{OUT} Peak: 1.65 A.

12.8 Drain Current and Drain Voltage During Output Short Condition

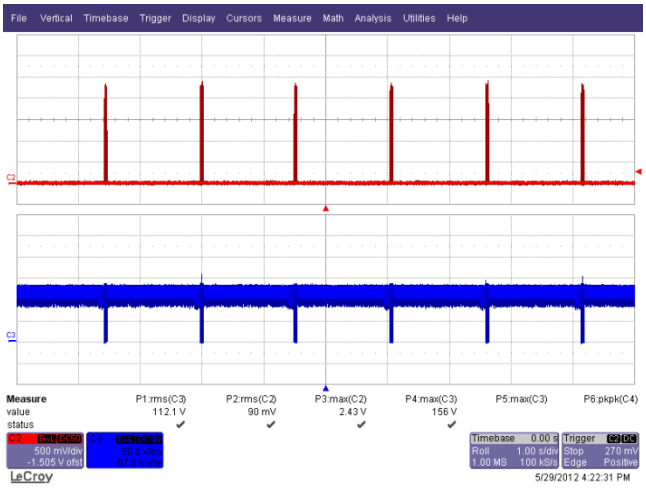

Figure 52 – 90 VAC Output Short Condition.
Upper: I_{DRAIN}, 500 mA / div.
Lower: $V_{DRAIN,}$ 50 V, 1 s / div.

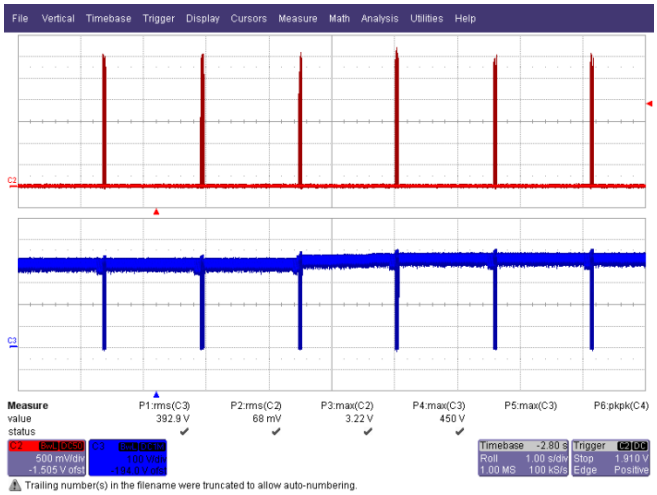

Figure 53 – 300 VAC Output Short Condition.
Upper: I_{DRAIN}, 500 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 1 s / div.

12.9 Open Load Output Voltage

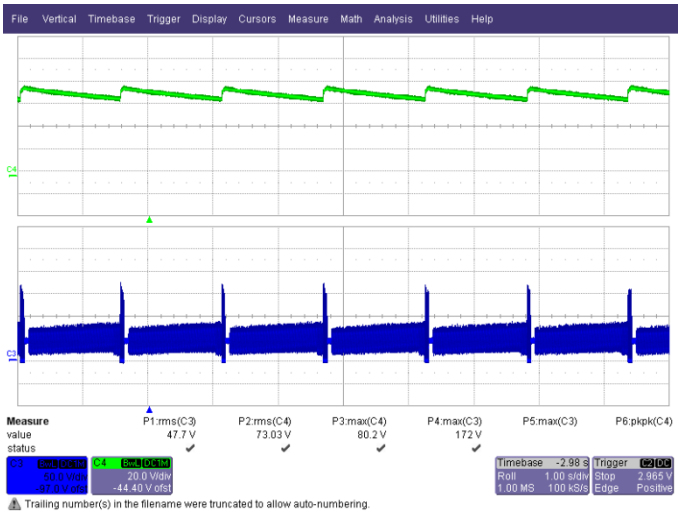

Figure 54 – 90 VAC Open Load Characteristic.
Upper: V_{OUT}, 20 V / div., 1 s / div.
Lower: V_{DRAIN}, 50 V / div., 1 s / div.

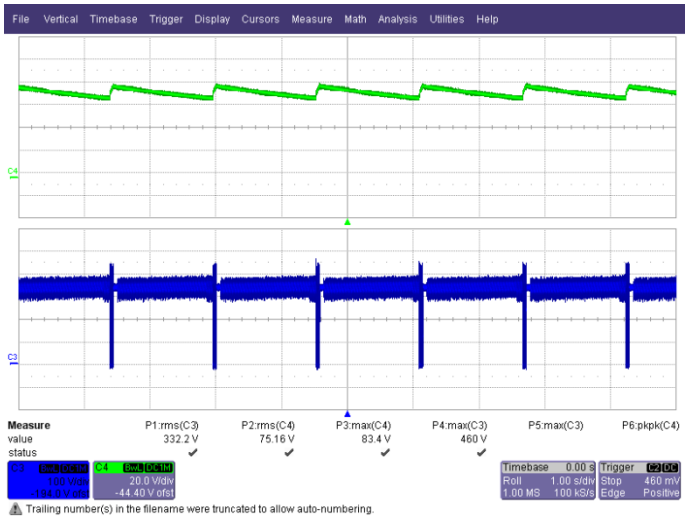

Figure 55 – 300 VAC Open Load Characteristic.
Upper: V_{OUT}, 20 V / div., 1 s / div.
Lower: V_{DRAIN}, 100 V / div., 1 s / div.

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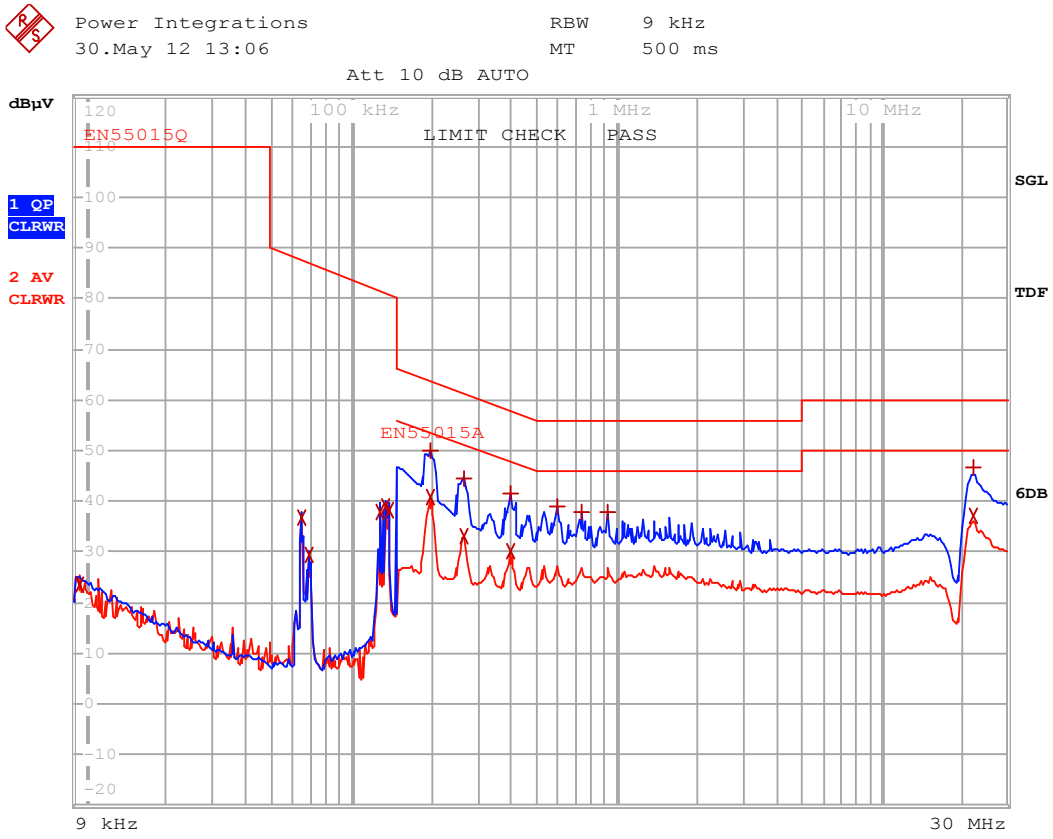
13 Conducted EMI

Conducted EMI was measured at 115 VAC and 230 VAC, 60 Hz line input and at room temperature.

13.1 Test Set-up

Figure 56 – EMI Set-up: LED Driver and Load were Placed Inside the Cone.

13.2 Test Result



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.36543609 kHz	23.55	N gnd	
2	Average	64.5467705779 kHz	36.92	L1 gnd	
2	Average	68.5176976246 kHz	29.44	L1 gnd	
2	Average	128.247618558 kHz	37.77	L1 gnd	
2	Average	133.454986145 kHz	38.80	N gnd	
2	Average	137.49880568 kHz	38.20	N gnd	
1	Quasi Peak	198.193645035 kHz	50.13	L1 gnd	-13.55
2	Average	198.193645035 kHz	40.66	L1 gnd	-13.02
1	Quasi Peak	264.49018761 kHz	44.66	L1 gnd	-16.62
2	Average	264.49018761 kHz	33.07	L1 gnd	-18.21
1	Quasi Peak	397.727746704 kHz	41.50	L1 gnd	-16.39
2	Average	397.727746704 kHz	30.07	L1 gnd	-17.82
1	Quasi Peak	598.084042089 kHz	38.84	L1 gnd	-17.15
1	Quasi Peak	729.776191209 kHz	38.01	L1 gnd	-17.98
1	Quasi Peak	926.622115652 kHz	37.87	L1 gnd	-18.13
1	Quasi Peak	22.1524057738 MHz	46.83	N gnd	-13.16
2	Average	22.1524057738 MHz	37.25	N gnd	-12.74

Figure 57 – Conducted EMI, 54 V LED Load, 115 VAC, 60 Hz, and EN55015 B Limits.

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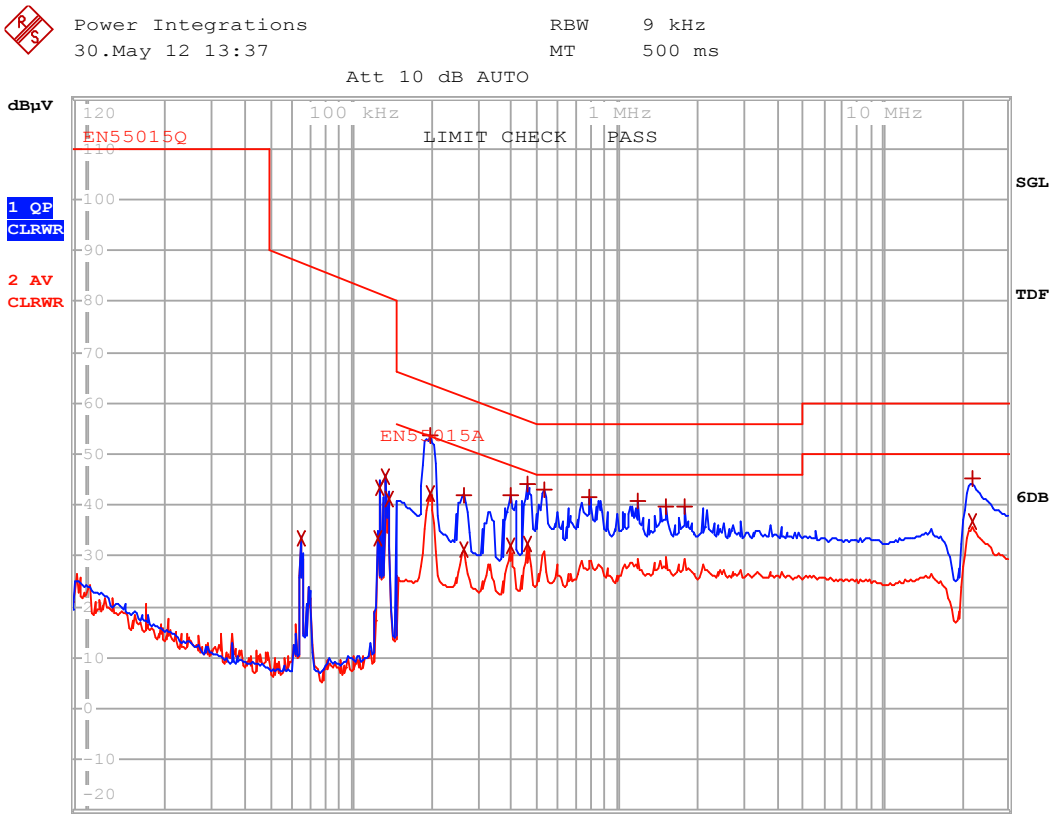

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV			DELTA LIMIT dB
2	Average	64.5467705779 kHz	33.31	L1	gnd	
2	Average	124.475875068 kHz	33.64	L1	gnd	
2	Average	128.247618558 kHz	43.24	N	gnd	
2	Average	133.454986145 kHz	45.61	L1	gnd	
2	Average	137.49880568 kHz	41.03	N	gnd	
1	Quasi Peak	198.193645035 kHz	53.74	L1	gnd	-9.94
2	Average	198.193645035 kHz	42.38	L1	gnd	-11.29
1	Quasi Peak	264.49018761 kHz	42.09	L1	gnd	-19.19
2	Average	264.49018761 kHz	31.17	L1	gnd	-20.11
1	Quasi Peak	397.727746704 kHz	42.04	L1	gnd	-15.85
2	Average	397.727746704 kHz	31.94	L1	gnd	-15.95
1	Quasi Peak	461.749566613 kHz	44.06	L1	gnd	-12.60
2	Average	461.749566613 kHz	32.28	L1	gnd	-14.37
1	Quasi Peak	530.769219795 kHz	43.11	L1	gnd	-12.88
1	Quasi Peak	790.243042258 kHz	41.61	L1	gnd	-14.38
1	Quasi Peak	1.1883298484 MHz	40.73	L1	gnd	-15.26
1	Quasi Peak	1.52395221823 MHz	39.85	L1	gnd	-16.14
1	Quasi Peak	1.78695382697 MHz	39.77	L1	gnd	-16.22
1	Quasi Peak	21.9330750235 MHz	45.39	N	gnd	-14.60
2	Average	21.9330750235 MHz	36.59	N	gnd	-13.40

Figure 58 – Conducted EMI, 66 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.

14 Line Surge

The unit was subjected to ±2500 V 100 kHz ring wave and ±1 kV differential surge at 230 VAC using 10 strikes in each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
-2500	230	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
+2500	230	L1, L2	90	100 kHz Ring Wave (200 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (200 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+1kV	230	L1, L2	0	Surge (2Ω)	Pass
-1kV	230	L1, L2	0	Surge (2Ω)	Pass
+1kV	230	L1, L2	90	Surge (2Ω)	Pass
-1kV	230	L1, L2	90	Surge (2Ω)	Pass

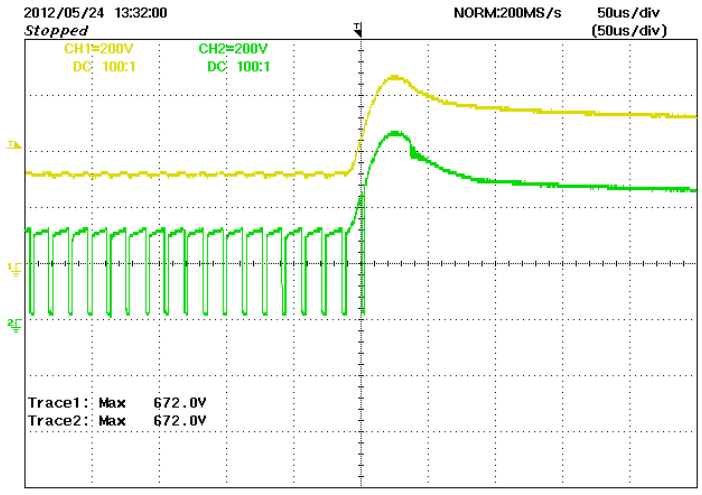

Figure 59 – Peak Rectified Input Voltage (Trace 1) and U1 Drain Voltage During (Trace 2) 90˚ 1 kV Differential Surge at the Input.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
22-Aug-12	CA	1.0	Initial Release	Apps & Mktg

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