Design Example Report

Title	***7.5 W Power Factor Corrected TRIAC Dimmable Non-Isolated Tapped-Buck PAR16 Lamp Replacement LED Driver Using LinkSwitch™-PL LNK458KG***
Specification	190 VAC – 265 VAC Input; 9 V (Typical), 800 mA Output
Application	LED Driver for PAR16 Lamp Replacement
Author	Applications Engineering Department
Document Number	DER-327
Date	June 29, 2012
Revision	1.0

Summary and Features

- NEMA SSL 6-2010 compliant TRIAC dimming
- Single-stage, power factor corrected and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Highly energy efficient, >76% at 230 VAC input
- Fast start-up time (<50 ms) – no perceptible delay
- Integrated protection and reliability features
    - No-load protection / hard short-circuit protected
    - Auto-recovering thermal shutdown
    - No damage during line brown-out or brown-in conditions
- PF >0.9 at 230 VAC
- ATHD <25% at 230 VAC
- Meets IEC 2.5 kV ring wave, 500 V differential line surge and EN55015 conducted EMI

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Important Note:
Although this board is designed to satisfy safety requirements for non-isolated LED drivers, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK458KG from the LinkSwitch-PL family of devices.

The DER-327 provides a single 7.5 W dimmable constant current output.

The key design goals were high efficiency and small size. This allowed the driver to fit into PAR16 sized lamps and be as close to a production design as possible.

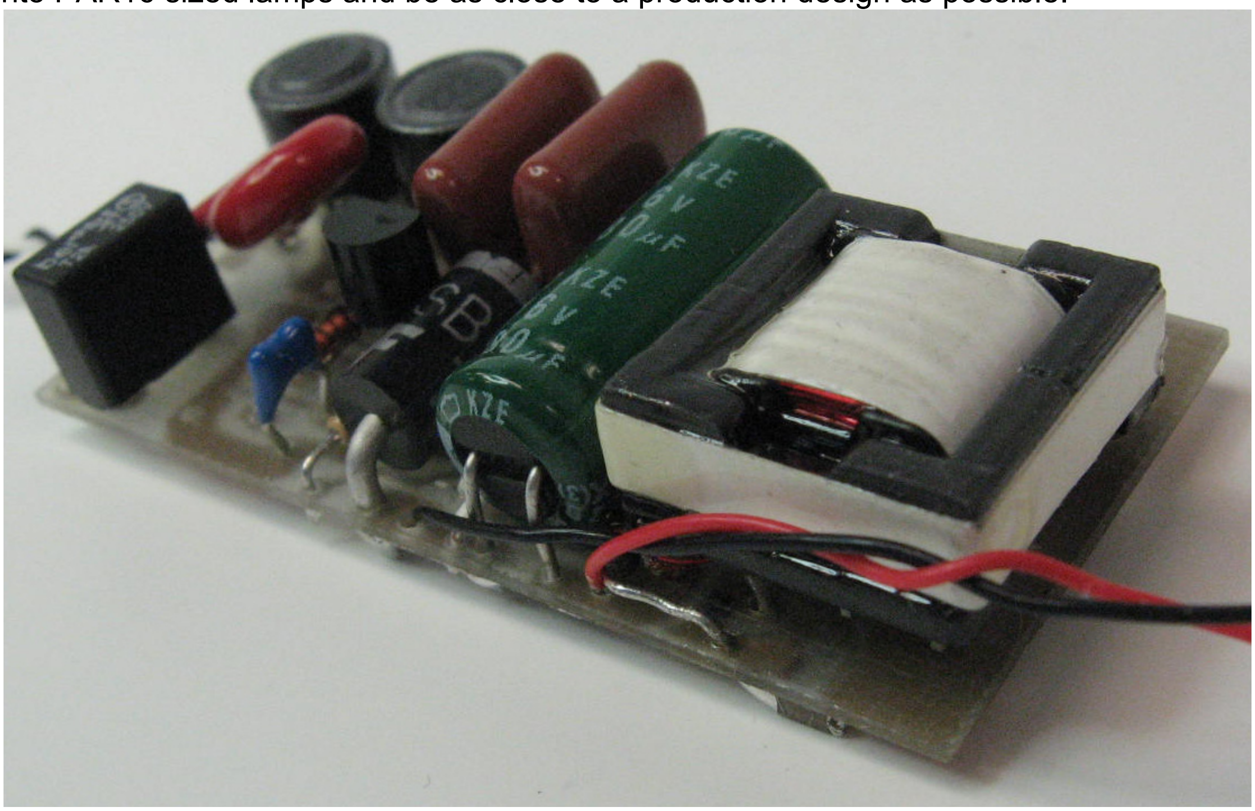

Figure 1 – PCB Assembly.

The board was optimized to operate over the high-line AC input voltage range (190 VAC to 265 VAC, 47 Hz to 63 Hz). LinkSwitch-PL IC based designs provide a high power factor (>0.9) meeting current international requirements.

The form factor of the board was chosen to meet the requirements for standard PAR16 LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, PIXI spreadsheet and performance data.

2 Power Supply Specifications

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output Voltage	V_{OUT}	8.4	9	9.6	V	
Output Current	I_{OUT}	760	800	840	mA	At 230 VAC
Total Output Power						
Continuous Output Power	P_{OUT}		7.5		W	
Efficiency						
Nominal	η		76		%	Measured at P_{OUT} 25 °C at 230 VAC
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				
Line Surge Differential Mode (L1-L2)			500		V	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)			2.5		kV	2 Ω Short-Circuit Series Impedance
Power Factor		0.9				At 230 VAC
ATHD				25	%	At 230 VAC

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3 Schematic

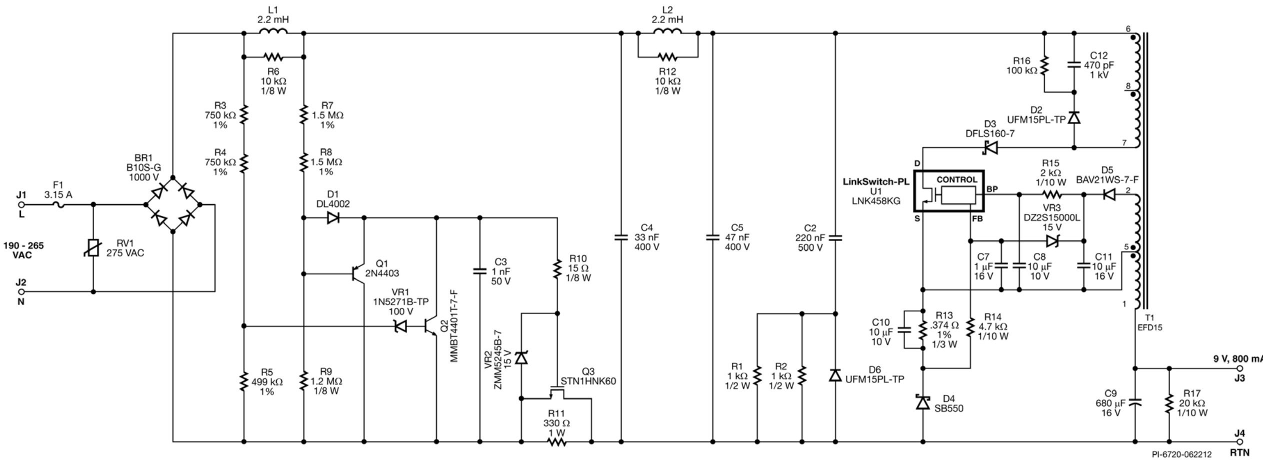

Figure 2 – Schematic for 9 V / 800 mA PAR16 Replacement Lamp

4 Circuit Description

The LinkSwitch-PL (U1) family is highly integrated power ICs intended for use in LED driver applications. The LinkSwitch-PL provides high power factor in a single-stage conversion topology while regulating the output current across the range of input (190 VAC to 265 VAC) and output voltage conditions typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus a high-voltage power MOSFET is incorporated into the IC.

4.1 Input Stage

Fuse F1 provides protection against component failure. A relatively high, fast 3.15 A rating was needed to prevent false opening during line surges. Fuse F1 may be replaced with a fusible resistor (2 W, 3.3 Ω) for lower cost but lowers efficiency.

The maximum input voltage is clamped by RV1 during differential line surges.

The AC input is full wave rectified by BR1.

Capacitor C4, C5 and differential choke L1 and L2 form the EMI filter. Total input filter capacitance is limited to low value to maintain high power factor. This input multiple L-filter networks plus the frequency jittering feature of LinkSwitch-PL ensures compliance with Class B emission limits. Resistors R6 and R12 damp the resonance of the EMI filter, preventing peaks in the EMI spectrum when measured in a system (driver plus enclosure). Remove R6 and R12 if radiated EMI spectrum has significant margin in system level application.

- Inductor L1 and L2 are positioned after the bridge to avoid an imbalance in the EMI scan between line and neutral. This also allows the use of small high-voltage ceramic capacitors in the input filter.

4.2 Tapped-buck Topology Using LinkSwitch-PL Devices

The tapped-buck power train is composed of U1 (power switch + control), D4 (freewheeling diode), C9 (output capacitor), and T1 (inductor). Diode D3 was used to prevent negative voltage appearing across the drain-source of U1 especially near the zero-crossing of the input voltage. The bypass capacitor C8 provides the internal supply for U1, it is charged via the drain during MOSFET off-time during start-up. For better efficiency and during dimming it is supplied via the extra winding of the inductor through the rectification of D5 and filtering of C11.

4.3 Output Feedback

The output current is sensed by the voltage drop across R13 and then filtered by a low pass filter (R14 and C7). This biases the LinkSwitch-PL operating point such that the average FEEDBACK (FB) pin voltage is maintained at 290 mV in steady-state operation (800 mA output current). Bypass capacitor C10 is used to reduce dissipation across R13 thus increasing efficiency.

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4.4 Disconnected Load Protection

The reference is design is protected against accidental LED load disconnection (such as during production). The controller will operate in burst mode in order to prevent drastic failure in the board by limiting the output voltage via the reflected voltage from the auxiliary winding of the inductor through VR3 and the FB pin. The controller will in pulse-skip mode every time the FB pin voltage reaches 520 mV threshold.

4.5 Overload and Short-Circuit Protection

The load is protected against overload and short-circuits via a primary current limit. During short, primary current will build-up until it reaches current limit. Refer to short-circuit waveforms for more information.

4.6 Active Damper

The active damper network is used to limit the inrush current, associated voltage spikes and ringing when the TRIAC within a dimmer turns on. This connects a resistance (R11) in series with the input rectifier for a short period during each AC half-cycle, to minimize the dissipation across damper resistor R11. It is then bypassed for the remainder of the AC cycle via a parallel MOSFET (Q3). Resistor R7, R8, R9 and C3 determine the delay before the turn-on of Q3. Transistor Q1 ensures the reset of Q3 every AC half-cycle.

4.7 RCD Bleeder

Resistors R1, R2 and C2 form a bleeder network which ensures that the initial input current is high enough to meet the TRIAC latching and holding current requirement, especially during small TRIAC conduction angle. Diode D6 reduces the power loss (through R1 and R2) during the decay of energy in C2.

4.8 Line Surge Protection

The active damper is used to reduce the voltage stress across the power MOSFET in U1. If the instantaneous input voltage exceeds 400 V, Q3 will turn-off making a potential voltage divider between the impedance of the tapped-buck converter and R11.

5 PCB Layout and Outline

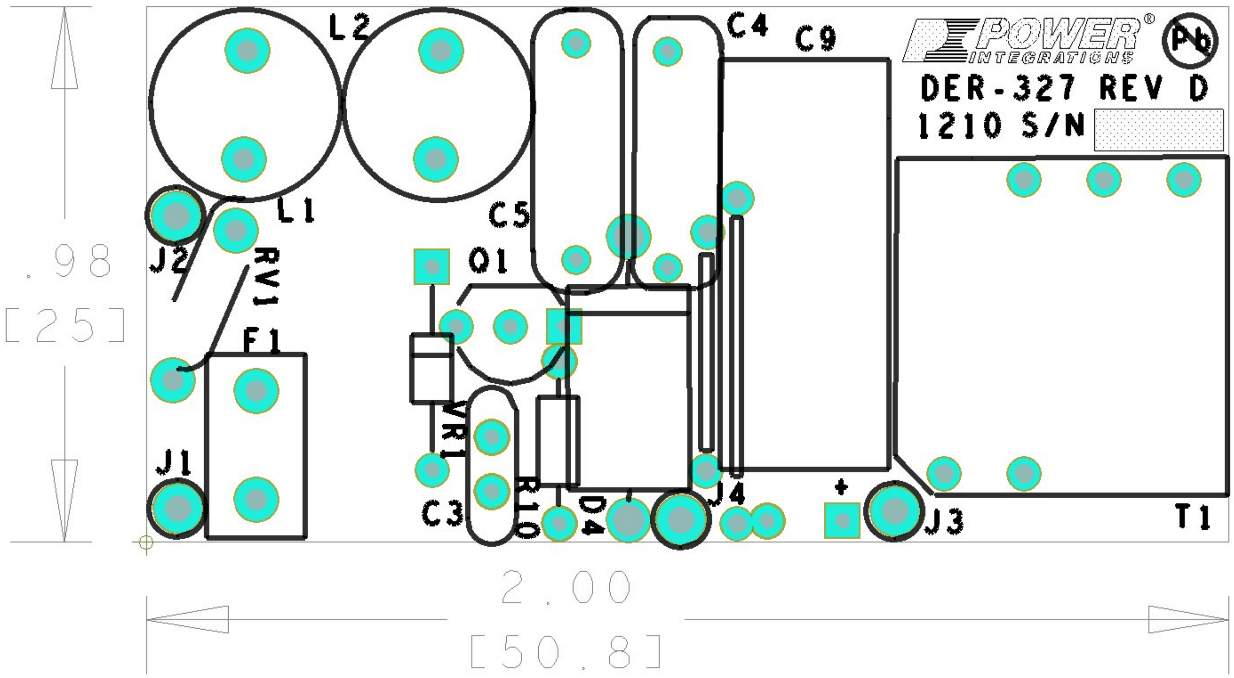

Figure 3 – Top Printed Circuit Layout.

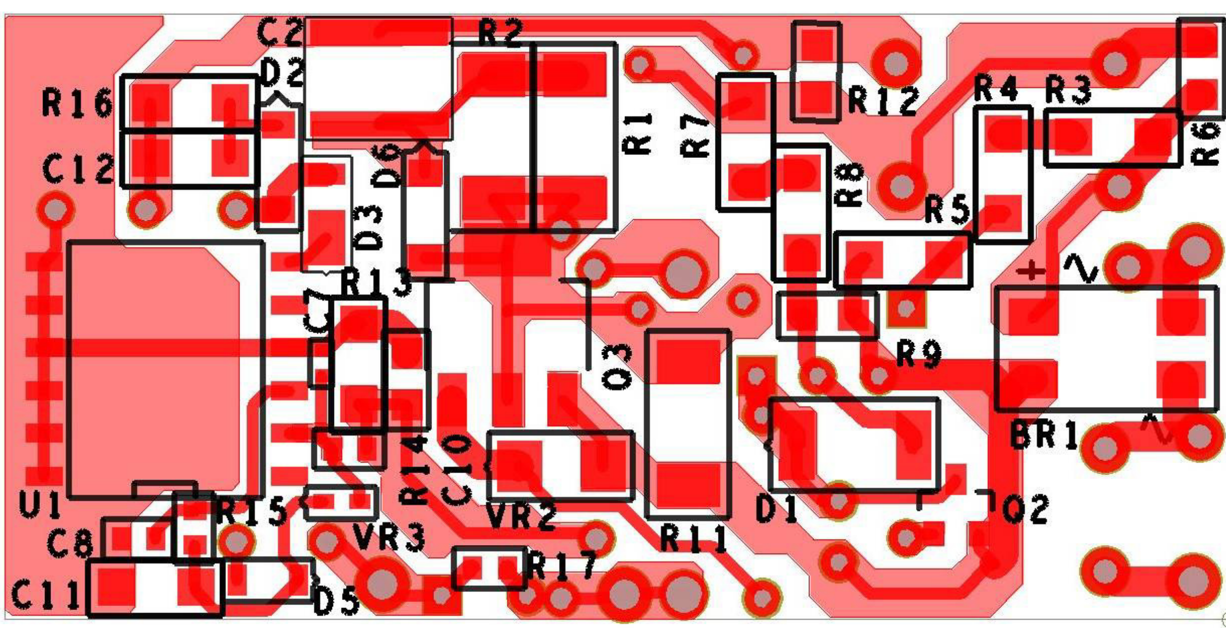

Figure 4 – Bottom Printed Circuit Layout.

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6 Populated PCB

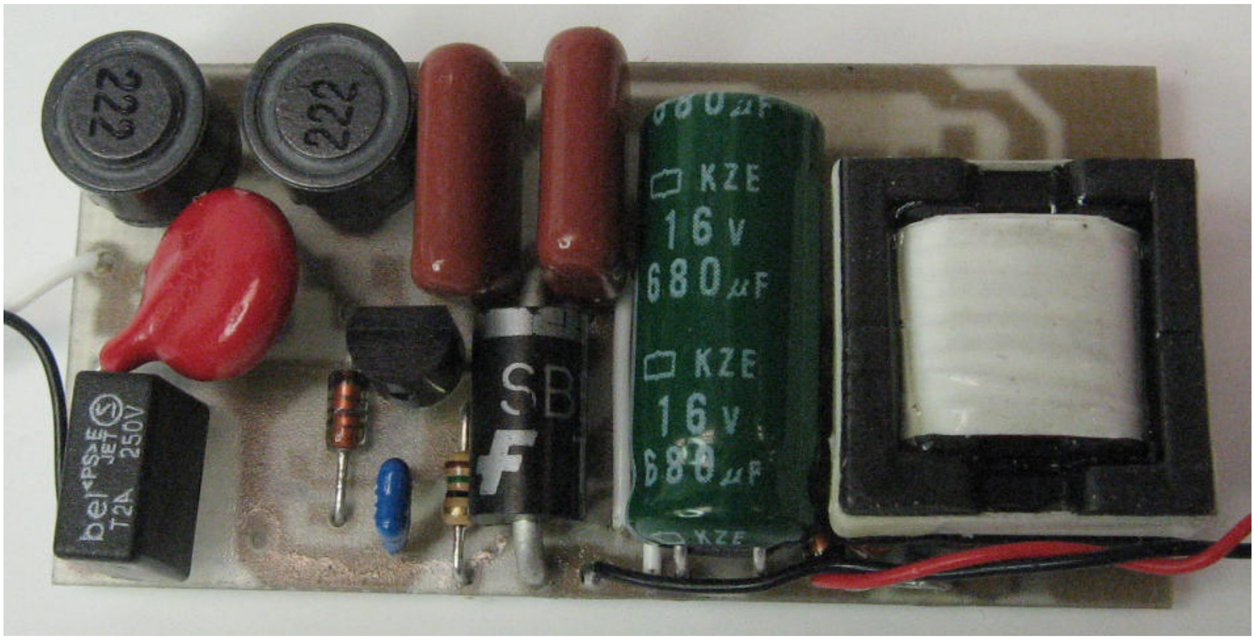

Figure 5 – Populated Circuit Board (top side).

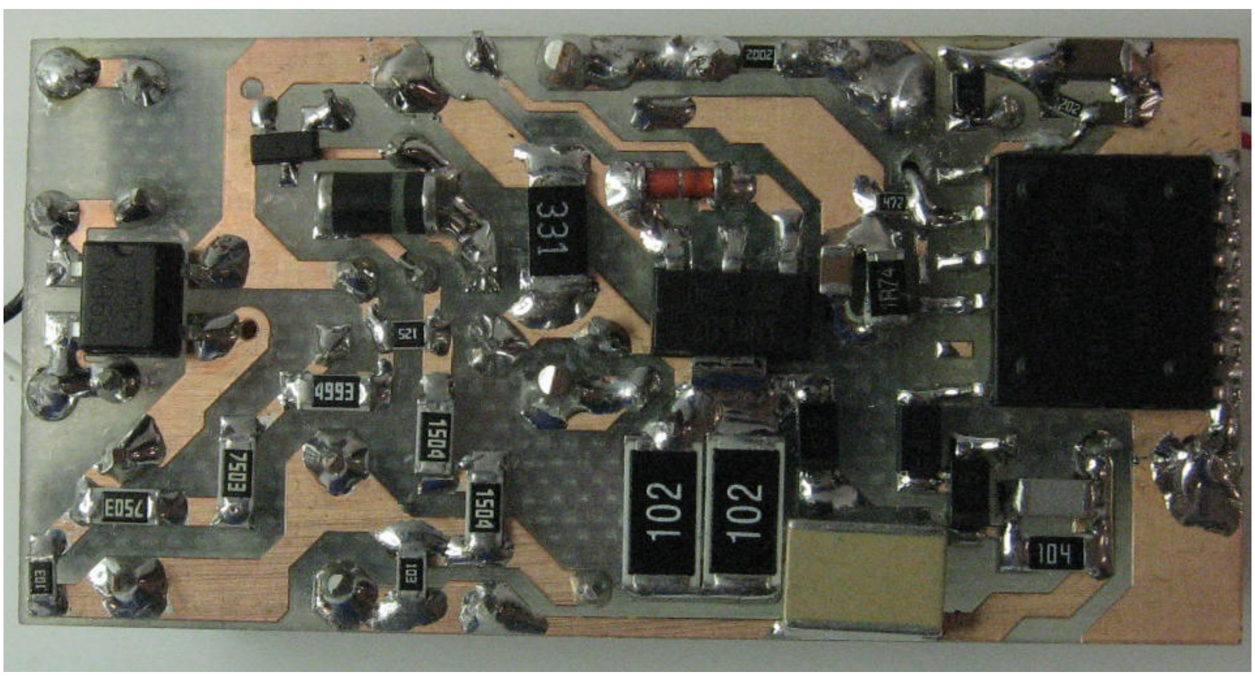

Figure 6 – Populated Circuit Board (bottom side).

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C2	220 nF, 500 V, Ceramic, X7R, 1825	VJ1825Y224KBEAT4X	Vishay
3	1	C3	1 nF, 50 V, Ceramic, COG	B37979G5102J000	Epcos
4	1	C4	33 nF, 400 V, Film	ECQ-E4333KF	Panasonic
5	1	C5	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
6	1	C7	1 μF 16 V, Ceramic, X5R, 0402	C1005X5R1C105M	TDK
7	1	C8	10 μF, 10 V, Ceramic, X5R, 0603	C1608X5R1A106M	TDK
8	1	C9	680 μF, 16 V, Electrolytic, Very Low ESR, 38 mΩ, (8 x 20)	EKZE160ELL681MH20D	Nippon Chemi-Con
9	1	C10	10 μF, 10 V, Ceramic, X7R, 0805	C2012X7R1A106M	TDK
10	1	C11	10 μF, 16 V, Ceramic, X7R, 1206	C3216X7R1C106M	TDK
11	1	C12	470 pF, 1000 V, Ceramic, COG, 1206	VJ1206A471JXGAT5Z	Vishay
12	1	D1	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002-13-F	Diodes, Inc.
13	2	D2 D6	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
14	1	D3	60 V, 1 A, Diode Schottky PWRDI 123	DFLS160-7	Diodes, Inc.
15	1	D4	50 V, 5 A, Schottky, DO-201AD	SB550	Vishay
16	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
18	2	L1 L2	2.2 mH, 0.27 A	CTSCH875DF-222K	Coilcraft
19	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, TO-92	2N4403RLRAG	On Semi
20	1	Q2	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401T-7-F	Diodes, Inc.
21	1	Q3	600 V, 400 mA, 8.5 Ω, N-Channel, SOT 223	STN1HNK60	ST
22	2	R1 R2	1 kΩ , 5%, 1/2 W, Thick Film, 2010	ERJ-14YJ102U	Panasonic
23	2	R3 R4	750 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7503V	Panasonic
24	1	R5	499 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4993V	Panasonic
25	2	R6 R12	10 kΩ 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
26	2	R7 R8	1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
27	1	R9	1.2 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ125V	Panasonic
28	1	R10	15 Ω, 5%, 1/8 W, Carbon Film	CFR-12JB-15R	Yageo
29	1	R11	300 Ω, 5%, 1 W, Pulse Proof, Thick Film, 2010	CRCW2010330RJNEFHP	Vishay/Dale
30	1	R13	0.374 Ω, 1%, 1/3 W, Thick Film, 1206	SR732BLTER374F	KOA Speer
31	1	R14	4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
32	1	R15	2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ202V	Panasonic
33	1	R16	100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
34	1	R17	20 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
35	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
36	1	T1	Custom Made, EFD15, Horizontal, 8 pins	Custom Made	Custom Made
37	1	U1	LinkSwitch-PL, eSOP-12B	LNK458KG	Power Integrations
38	1	VR1	100 V, 5%, 500 mW, DO-35	1N5271B-TP	Micro Commercial
39	1	VR2	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes, Inc.
40	1	VR3	15 V, 5%, 150 mW, SSMINI-2	DZ2S15000L	Panasonic

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8 Inductor Specification

8.1 Electrical Diagram

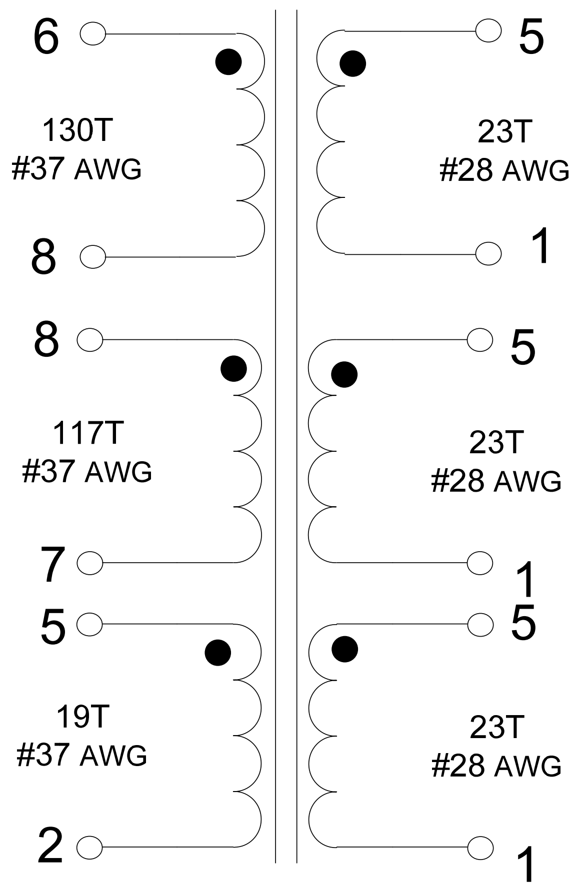

Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Primary Inductance	Pins 6-7, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	1.25 mH ±7%

8.3 Materials

Item	Description
[1]	Core: EFD-15; TDK-PC44 or equivalent.
[2]	Bobbin: EFD-15; 4/4 pin Horizontal
[3]	Magnet Wire: #28 AWG.
[4]	Magnet Wire: #37 AWG.
[5]	Tape, Polyester film, 3M 1350F-1 or equivalent, 9 mm wide.
[6]	Loctite Super Glue Control Gel.

8.4 Inductor Build Diagram

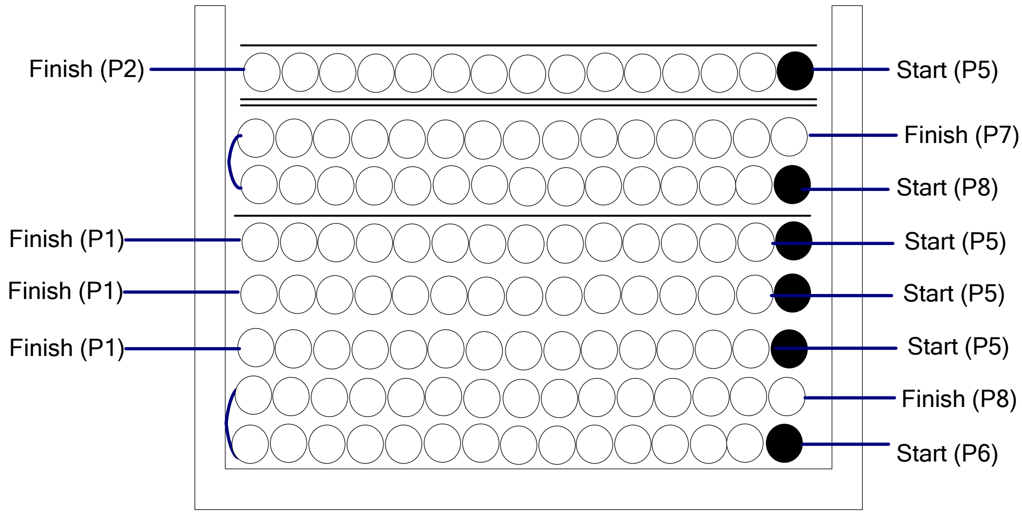

Figure 8 – Transformer Build Diagram.

8.5 Inductor Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise.
WDG 1	Start at pin 6. Wind 130 turns of item [4] and terminate at pin 8.
WDG 2	Start at pin 5. Wind 23 turns of item [3] and terminate at pin 1.
WDG 3	Start at pin 5. Wind 23 turns of item [3] and terminate at pin 1.
WDG 4	Start at pin 5. Wind 23 turns of item [3] and terminate at pin 1.
Insulation	Add 1 layer of tape of item [5].
WDG 5	Start at pin 8. Wind 177 turns of item [4] and terminate at pin 7.
Insulation	Add 2 layer of tape of item [5].
WDG 6	Start at pin 5. Wind 19 turns of item [4] and terminate at pin 2.
Taping	Add 1 layer of tape to secure the winding.
Final Assembly	Grind the core to get the specified inductance. Apply tape to secure both cores. Cut pins 3, 4 and 8. Apply adhesive item [6] to core and bobbin to prevent core movement.

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9 Transformer Design Spreadsheet

ACDC_LinkSwitch-PL-TapBuck_121611; Rev.1.0; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL_TB LinkSwitch-PL Tapped Buck Design Spreadsheet
ENTER APPLICATION VARIABLES					**Design Title**
VACMIN	190		190.00	V	Minimum AC Input Voltage
VACTYP	230		230.00	V	Typical AC Input Voltage
VACMAX	265		265.00	V	Maximum AC Input Voltage
FL			50.00	Hz	AC Mains Frequency
VOMIN	8.40		8.40		Minimum Output Voltage of LED string
VO	9.00		9.00	V	Output Voltage of LED string
VOMAX	9.60		9.60		Maximum Output Voltage of LED string
IO	0.80		0.80	A	Output Current riving LED strings
Power			7.20	W	Continuous Output Power
n	0.76		0.76		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Dimming Application	**Yes**		Yes		Enter Yes if design uses TRIAC dimming, otherwise select No
ENTER LinkSwitch-PL VARIABLES					
Chosen Device	**LNK458**		LNK458		Chosen LinkSwitch-II device
ILIMITMIN			1.01	A	Minimum Current Limit
ILIMITTYP			1.15	A	Typical Current Limit
ILIMITMAX			1.29	A	Maximum Current Limit
VOR			102.02	V	Reflected output voltage
Turns Ratio			10.74		Primary to secondary turns ratio
TON			2.55	us	Expected on-time of MOSFET at low line and PO
FSW			122.81	kHz	Expected switching frequency at low line and PO
Duty Cycle			31.35	%	Expected operating duty cycle at low line and PO
IRMS			0.10	A	Worst case primary RMS current at VO
IPK			0.48	A	Worst case peak primary current at VO
KDP		Warning	1.03		LinkSwitch-PL must operate in discontinuous mode (KP > 1) for good power factor. Consider reducing the primary inductance, changing the number of turns or increasing the device size
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
Core Type					
Core Type	**Custom**		EFD15		Enter Transformer Core
Core Part Number			**EFD15**		If custom core is used - Enter part number here
Bobbin part number			-		Bobbin Part number (if available)
AE	15.00		15.00	mm^2	Core Effective Cross Sectional Area
LE	34.00		34.00	mm^2	Core Effective Path Length
AL	780.00		780.00	nH/turn^2	Ungapped Core Effective Inductance
BW	8.85		8.85	mm	Bobbin Physical Winding Width
INDUCTOR DESIGN PARAMETERS					
LPMIN			1348.50	uH	Minimum Inductance (Includes inductance of input and output winding)
LPTYP	1450.00		1450.00	uH	Typical inductance (Includes inductance of input and output winding)
LP_TOLERANCE	7.00		7.00	%	Tolerance of the inductance
TURNS_TOTAL	270		270.00	Turns	Total number of turns (Includes input and output winding turns).
ALG			19.89	nH/turn^	Gapped Core Effective Inductance

				2	
BM			1839.89	Gauss	Calculated Worst Case Maximum Flux Density (BM < 3000 G)
BP		Warning	4934.15	Gauss	Peak Flux Density above maximum recommended value (BP < 3600 G). Reduce BP by increasing the number of turns, increasing the core size, or reducing the IC size; Verify at short-circuit condition
BAC			919.95	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			140.69		Relative Permeability of Ungapped Core
LG			0.92	mm	Gap Length (Lg > 0.1 mm)
Input Section					Section of winding that conducts only during ON time of the LINKSwitch-II
NL_INPUT			247.00		Number of turns in Input section.
AWG			36.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
L			4.25		Number of Layers (Input section)
CMA			245.24	Cmils	Current Density capacity 200 < CMA < 500
Output Section					Section of winding that conducts both when the Linkswitch-II is ON and OFF.
TURNS_OUTPUT			23.00		Number of Turns in Output winding. To adjust number of turns change INDUCTOR_RATIO
AWG_OUTPUT			24.00		Output Winidng Wire Gauge (Rounded to next smaller standard AWG value)
L_OUTPUT			1.47		Number of Layers (Output winding)
CMA_OUTPUT			251.24	Cmils	Current Density capacity 200 < CMA < 500
Bias Section					
Use Bias?	Auto		Yes		Is a Bias winding used?
TURNS_BIAS			21.00	Turns	Number of turns of Bias Winding
VBIAS	8	Warning	8.00	V	Bias Voltage may be too low to supply the IC with Energy. Verify performance on the bench
PIVBS			37.68	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at maximum VAC and max VO)
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			31.35	%	Duty cycle measured at minimum input voltage
IAVG			0.04	A	Input average current measured at the minimum input voltage
IP			0.48	A	Peak Primary current at maximum input voltage
ID_PK			5.16	A	Peak output winding current at the maximum input voltage
ISW_RMS			0.10	A	Switch RMS current measured at the minimum input voltage
ID_RMS			1.61	A	RMS current of freewheeling diode at maximum input voltage
IL_RMS			0.10	A	RMS current of the primary section of the inductor measured at the minimum input voltage
IL_TAP_RMS			1.62	A	RMS current of the output winding section of the inductor at the maximum input voltage
FEEDBACK WINDING PARAMETERS					
RFEEDBACK			0.38	ohm	This is a first approximation for the sense resistor and will likely require fine tuning in the bench
CBP			10.00	uF	Minimum required Bypass pin capacitor for correct operation
VOLTAGE STRESS PARAMETERS					
VDRAIN			527.86	V	Estimated worst case drain voltage at maximum input voltage

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VOR	102.02	V	Reflected output voltage
PIVS	41.52	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at maximum VAC and maximum VO)

Note: Peak Flux Density (BP) is above the recommended 3600 G, in this particular design actual measurement at worst case condition with line, load and temperature no core saturation occurred.

10 Performance Data

All measurements performed at 25 ºC room temperature, with an input frequency of 60 Hz unless otherwise specified.

10.1 Active Mode Efficiency

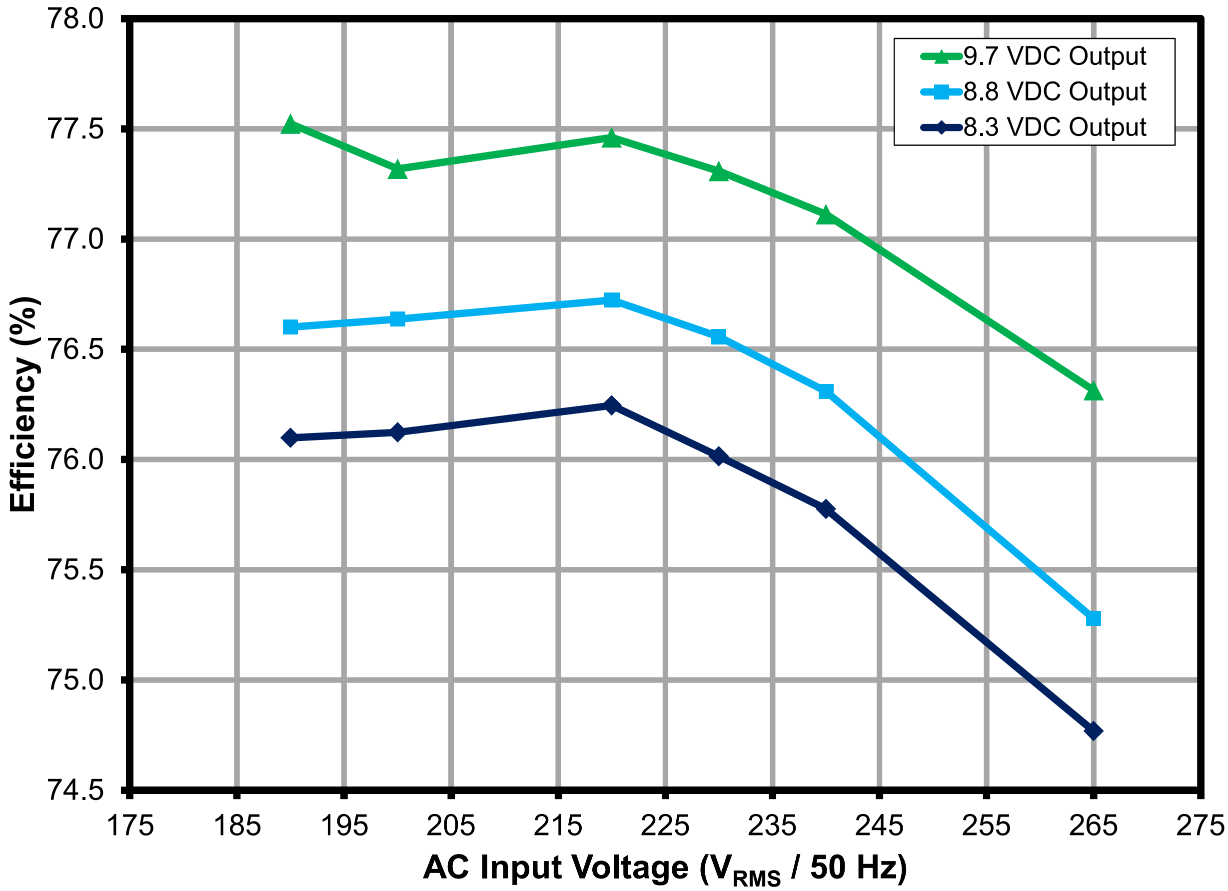

Figure 9 – Efficiency with Respect to AC Input Voltage at 30 mA.

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10.2 Line Regulation

The LinkSwitch-PL device regulates the output by controlling the power MOSFET on-time and switching frequency to maintain the average FEEDBACK pin at its 0.29 V threshold. Slight changes in output current may be observed when input or output conditions are changed or after AC cycling due to the device selecting a slightly different operating state (selection of on-time and frequency).

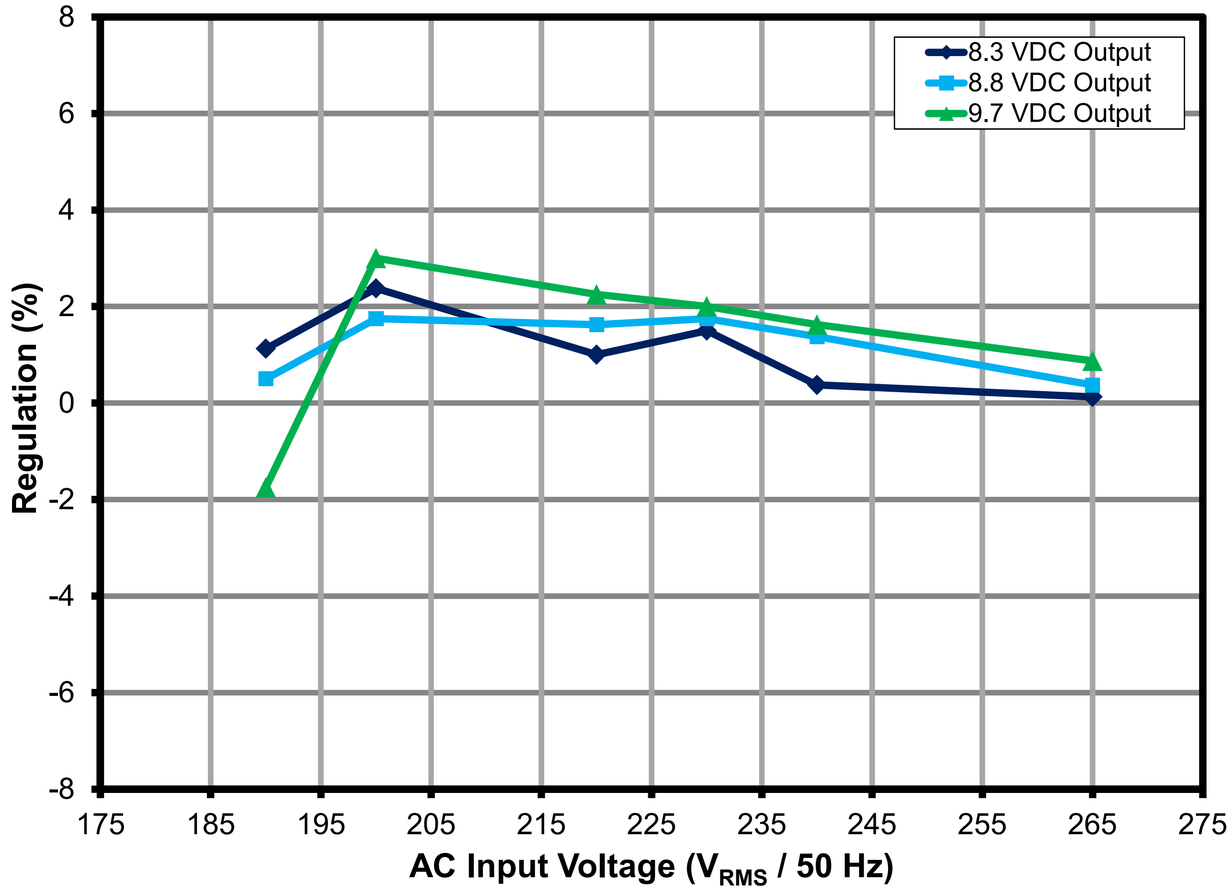

Figure 10 – Line Regulation, Room Temperature.

10.3 Power Factor

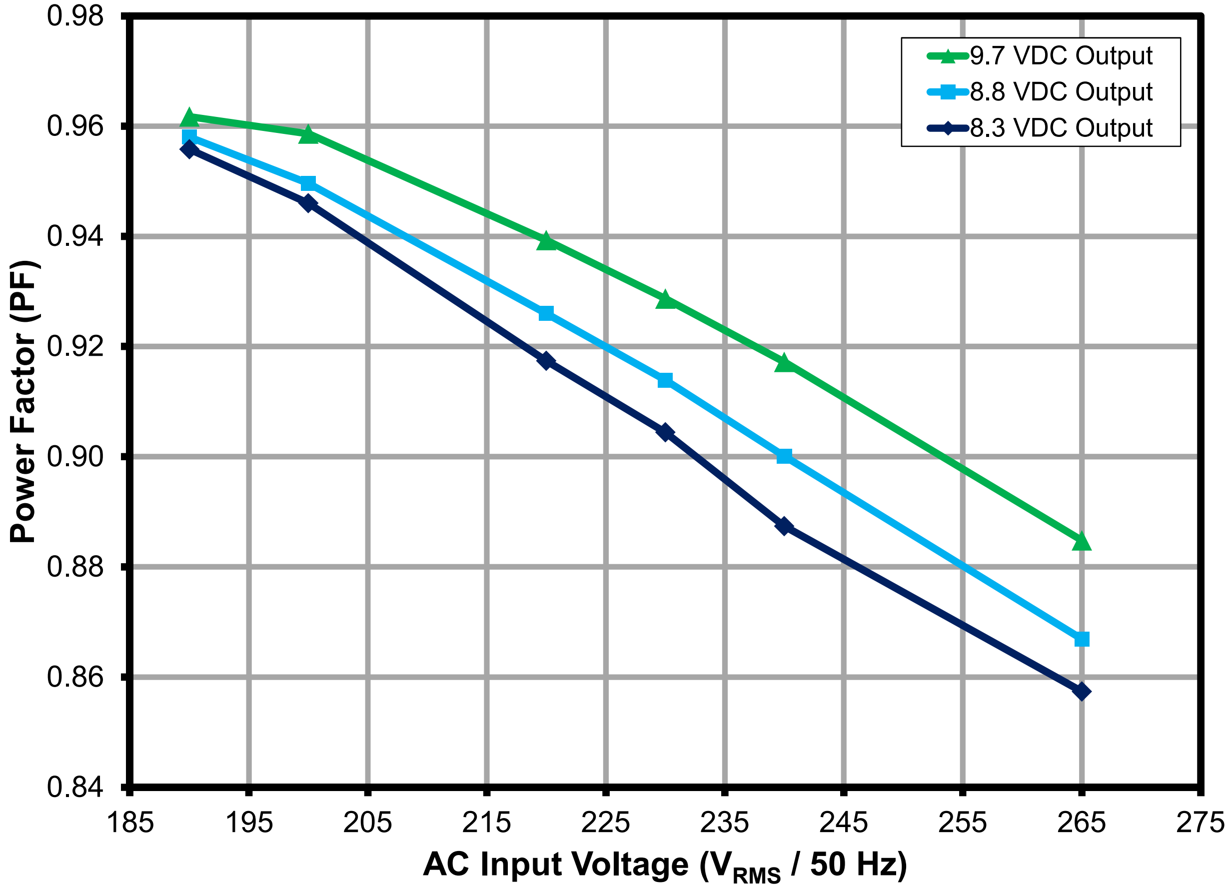

Figure 11 – High Power Factor within the Operating Range for 230 V LED.

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10.4 %ATHD

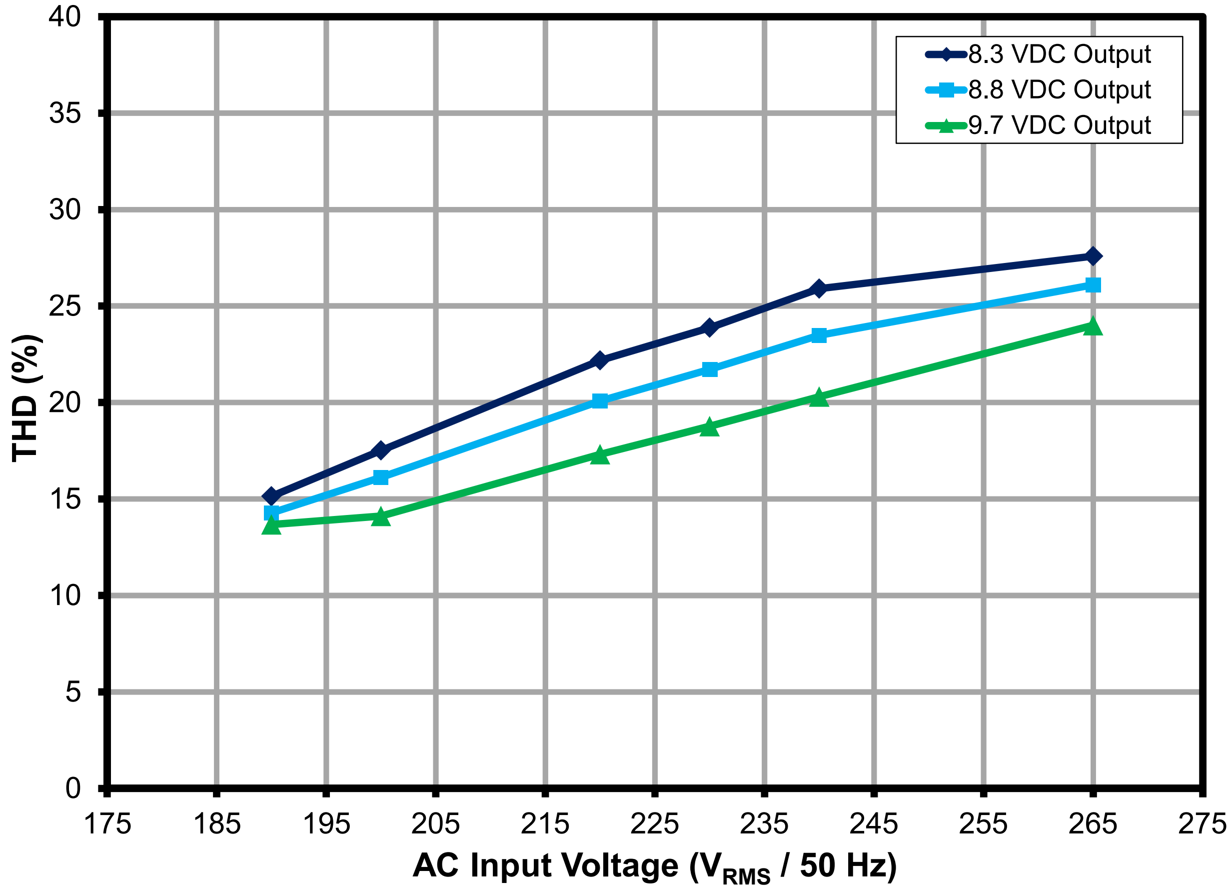

Figure 12 – Very Low %ATHD at 115 VAC.

10.5 Harmonic Content

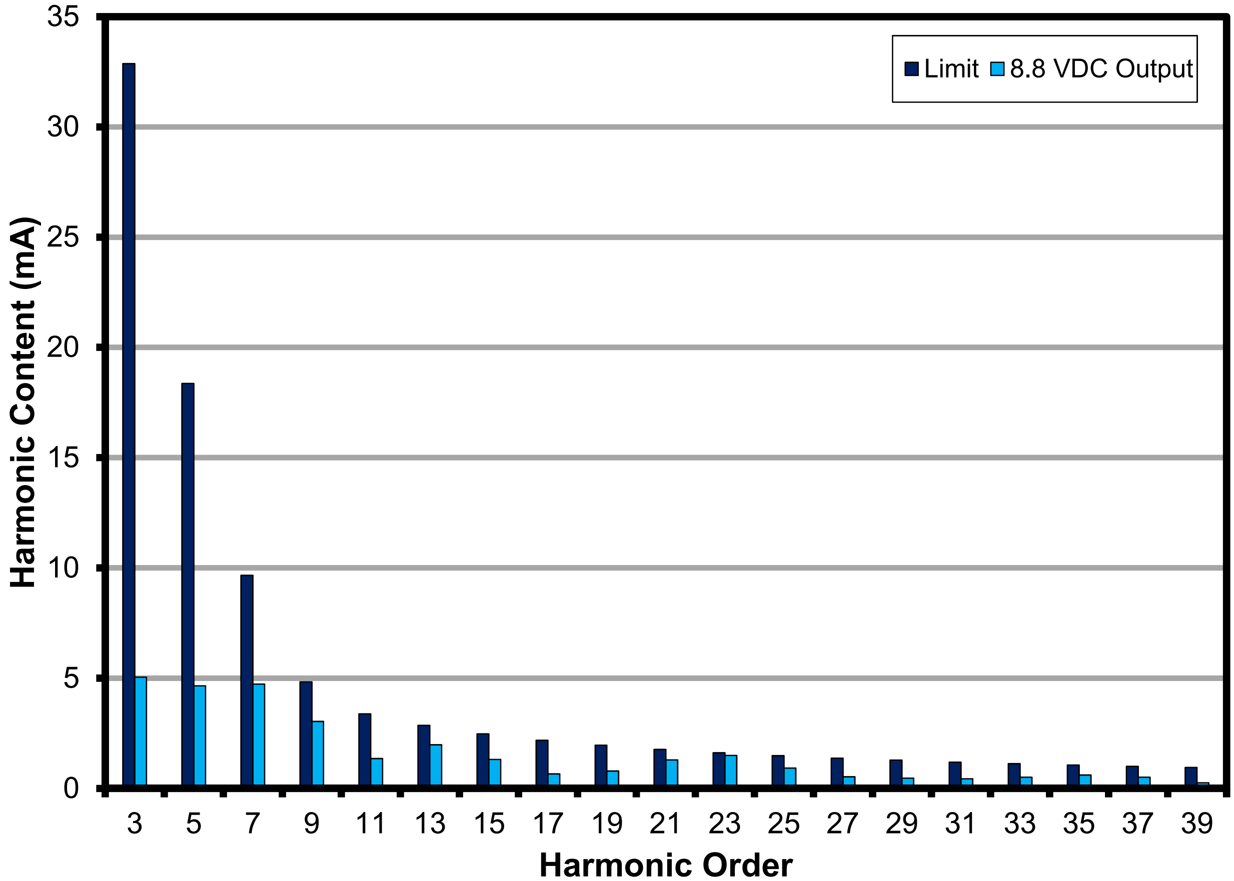

Figure 13 – Meets EN61000-3-2 Harmonics Contents Standards for <25 W Rating for 230 V LED Output.

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10.6 Harmonic Measurements

VAC (V_{RMS})	Freq (Hz)	I (mA)	P	PF
230	50.00	45.91	9.6660	0.9139
nth Order	**mA Content**	**% Content**	**Limit (mA) <25 W**	**Remarks**
1	44.83			
2	0.03	0.06%		
3	5.04	11.25%	32.8644	Pass
5	4.66	10.39%	18.3654	Pass
7	4.73	10.56%	9.6660	Pass
9	3.05	6.79%	4.8330	Pass
11	1.36	3.02%	3.3831	Pass
13	1.98	4.42%	2.8626	Pass
15	1.32	2.94%	2.4809	Pass
17	0.66	1.47%	2.1891	Pass
19	0.79	1.77%	1.9586	Pass
21	1.30	2.90%	1.7721	Pass
23	1.50	3.34%	1.6180	Pass
25	0.92	2.05%	1.4886	Pass
27	0.53	1.17%	1.3783	Pass
29	0.47	1.05%	1.2832	Pass
31	0.44	0.99%	1.2005	Pass
33	0.51	1.14%	1.1277	Pass
35	0.62	1.37%	1.0633	Pass
37	0.51	1.14%	1.0058	Pass
39	0.26	0.59%	0.9542	Pass
41	0.33	0.74%		
43	0.44	0.98%		
45	0.38	0.85%		
47	0.31	0.69%		
49	0.24	0.54%		

Table 1 – 230 VAC Input Current Harmonic Measurement for 9 V LED.

10.7 *Dimming Characteristic*

Dimming characteristic from a controlled AC supply to emulate the TRIAC conduction pattern. The reference design meets the dimming requirement as set by National Electrical Manufacturers Association (NEMA) Standards Publication SSL 1-2010 (Electronic Drivers for LED Devices, Arrays or Systems) and SSL 6-2010 (Solid State Lighting for Incandescent Replacement-Dimming).

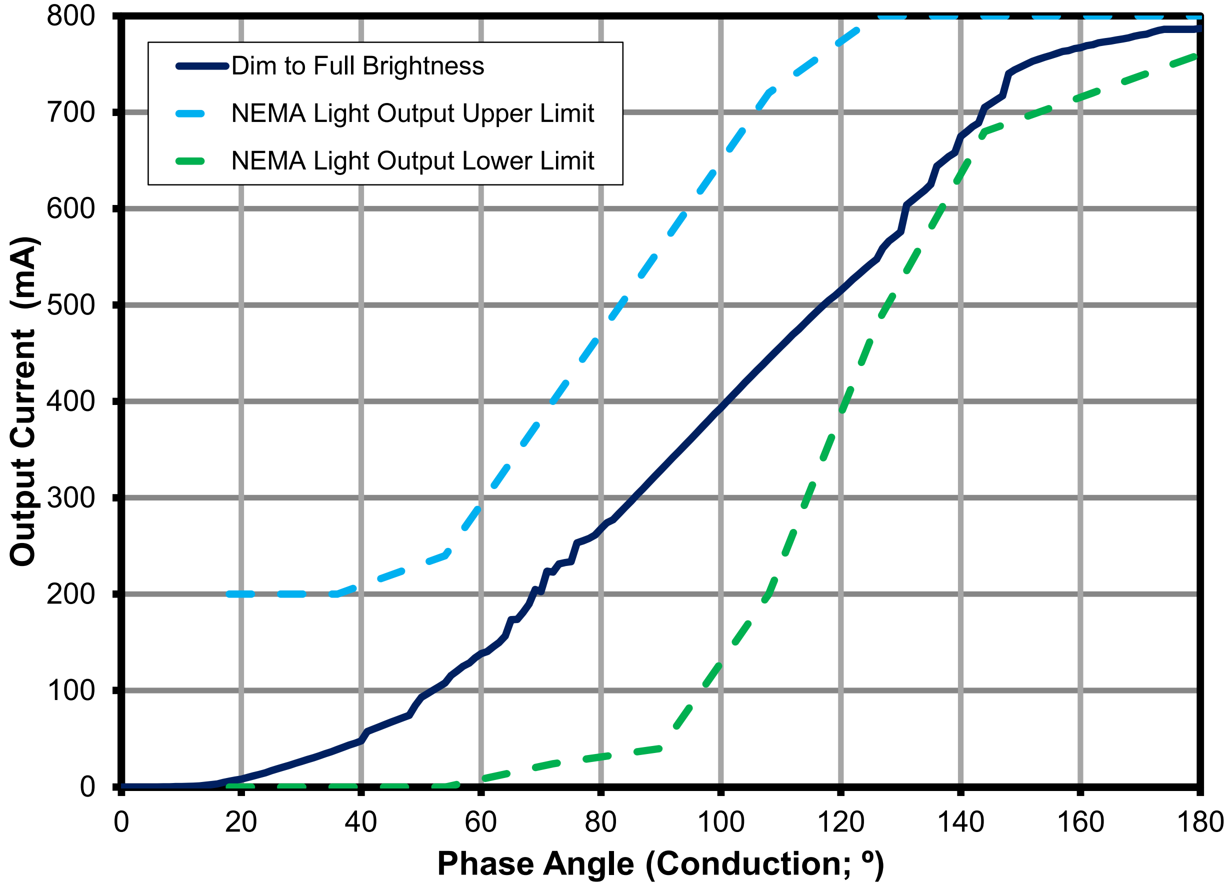

Figure 14 – Dimming Curve Characteristic from Full Dim to Full Brightness. Meets NEMA SSL 6-2010.

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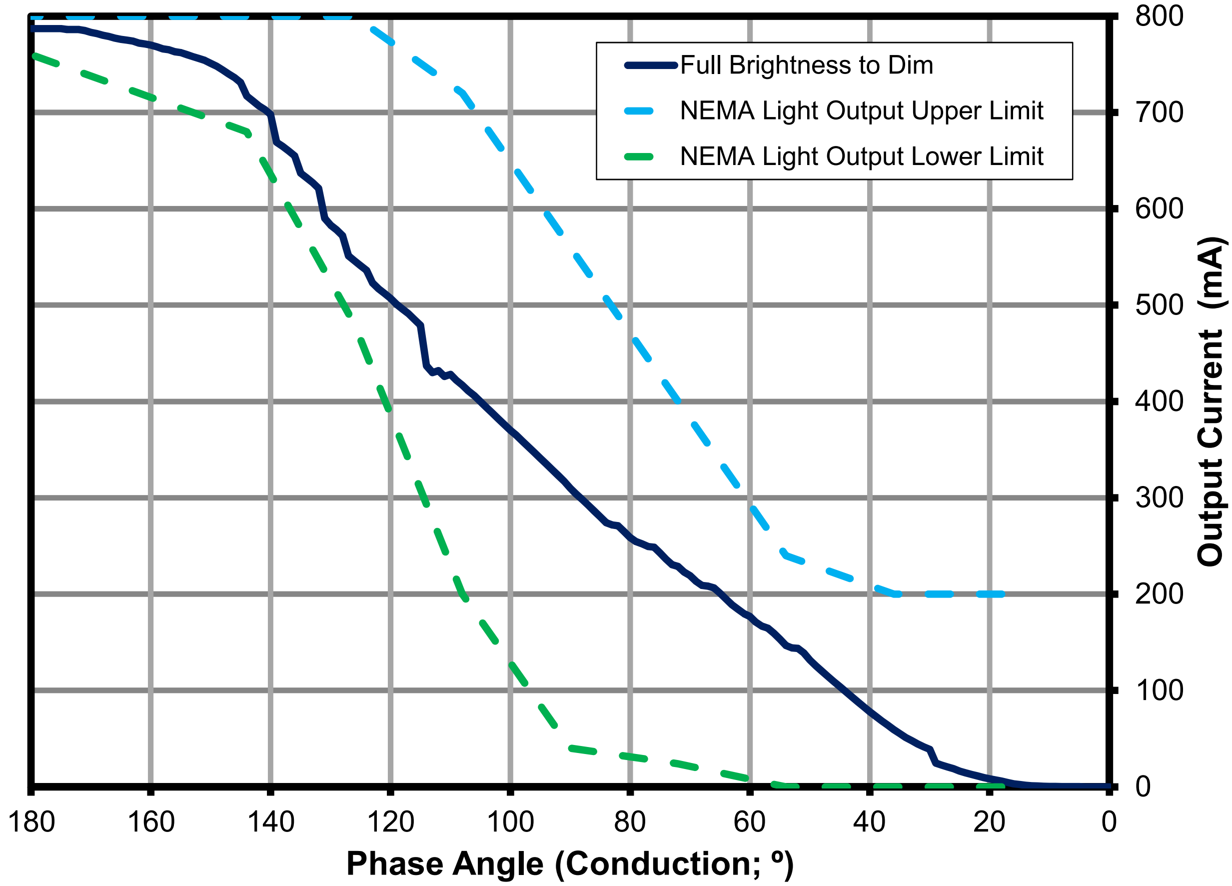

Figure 15 – Dimming Characteristic from Full Brightness to Full Dimming. Meets NEMA SSL 6-2010.

10.8 Unit to Dimmer Compatibility

These are the list of dimmers verified for this reference design. Users are not limited on the following list. Make sure to test the dimmers according to its recommended operating line input frequency to avoid flicker.

Input	Origin	Dimmer	Maximum		Minimum		Dimming Ratio	
		Brand	Conduction Angle (º)	I_{OUT} (mA)	Conduction Angle (º)	I_{OUT} (mA)		
230 V / 50 Hz	China	TCL 630 W	174	793.2	37.11	67.5	11.8	:1
230 V / 50 Hz	China	SEN BO LANG 300 W	167	790.5	56.88	134.3	5.9	:1
230 V / 50 Hz	China	EBA HUANG	165	774.2	41.76	63.6	12.2	:1
230 V / 50 Hz	China	SB ELECTRC 600 W	166	778.5	49	94.8	8.2	:1
230 V / 50 Hz	China	MYONGBO	169	814	62.71	130.7	6.2	:1
230 V / 50 Hz	China	KBE 650 W	171	804.2	34.74	55	14.6	:1
230 V / 50 Hz	China	CLIPMEI	172	808	54	112	7.2	:1
230 V / 50 Hz	China	MANK 200 W	166	803	68.5	66.186	12.1	:1
230 V / 50 Hz	German	BUSCH2250 600 W	152	776.5	43.74	74.9	10.4	:1
230 V / 50 Hz	German	REV 300 W	151	745.2	38.06	44.9	16.6	:1
230 V / 50 Hz	German	MERTEN 572499	159	805	40.35	65.8	12.2	:1
230 V / 50 Hz	German	BERKER	150	747	54.18	105	7.1	:1
230 V / 50 Hz	Italy	RM34DMA 160 W	160.27	780	48.42	96.5	8.1	:1
230 V / 50 Hz	Italy	Relco RT34DSL	163	797	50.22	119	6.7	:1

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11 Thermal Performance

11.1 Equipment Used

Chamber:	Tenney Environmental Chamber Model No: TJR-17 942
AC Source:	Chroma Programmable AC Source Model No: 6415
Wattmeter:	Yokogawa Power Meter Model No: WT2000
Data Logger:	Yokogawa MV2000

Figure 16 – Thermal Chamber Set-up Showing Box Used to Prevent Airflow Over UUT.

11.2 Thermal Test Results

11.2.1 Normal Operation

Load: 8 V / 800 mA LED load.

The unit was verified inside an enclosure box to avoid the effect of the circulating air in the chamber (LED load was outside the chamber).

Component	Device Temperature (ºC)			
	190 VAC / 50 Hz		265 VAC / 50 Hz	
PCB Board Ambient	25	50	25	50
Bridge (BR1)	40.7	63.7	38.2	63.0
LNK458KG (U1)	77.4	99.2	78.4	99.6
FET Damper (Q3)	64.7	93.1	59.6	84.7
Output Diode (D4)	69.8	92.8	68.7	91.1
Transformer (T1)	69.8	92.6	60.4	81.6
EMI Choke (L1)	43.9	67.7	38.0	62.4

Table 2 – Thermal Data, No Potting.

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11.3 Thermal Scans

The scan is conducted at ambient temperature of 25 ºC open frame, 190 VAC / 50 Hz input.

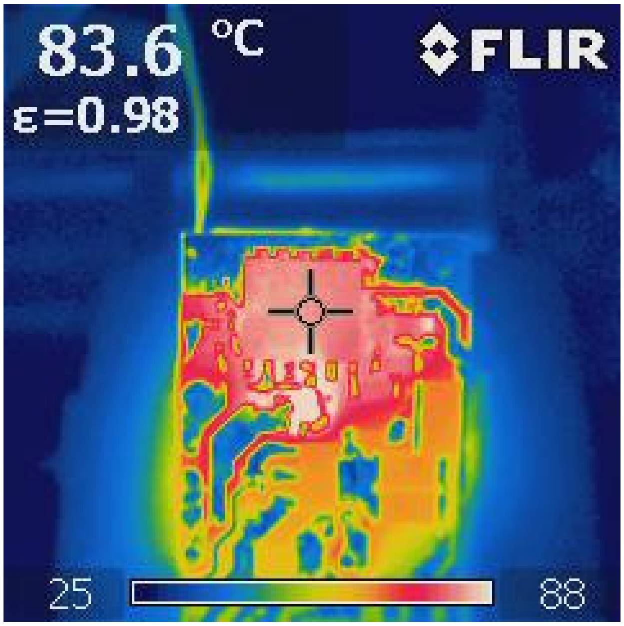

Figure 17 – LNK458KG U1 Case Temperature.

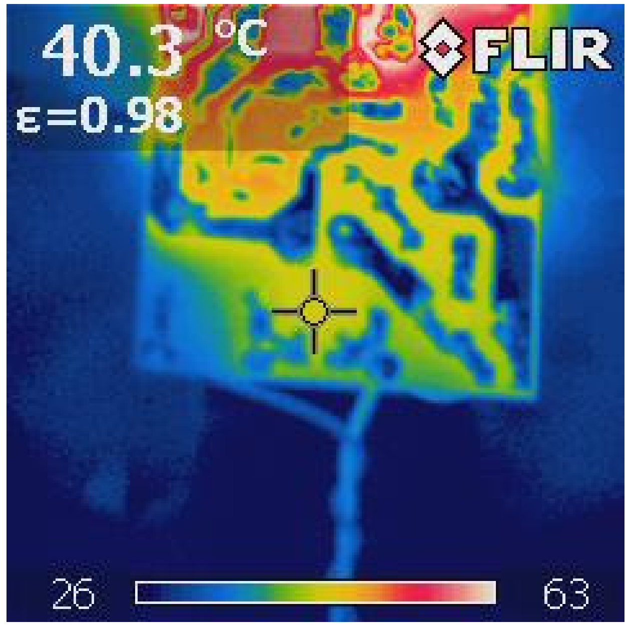

Figure 18 – BR1 Bridge Rectifier.

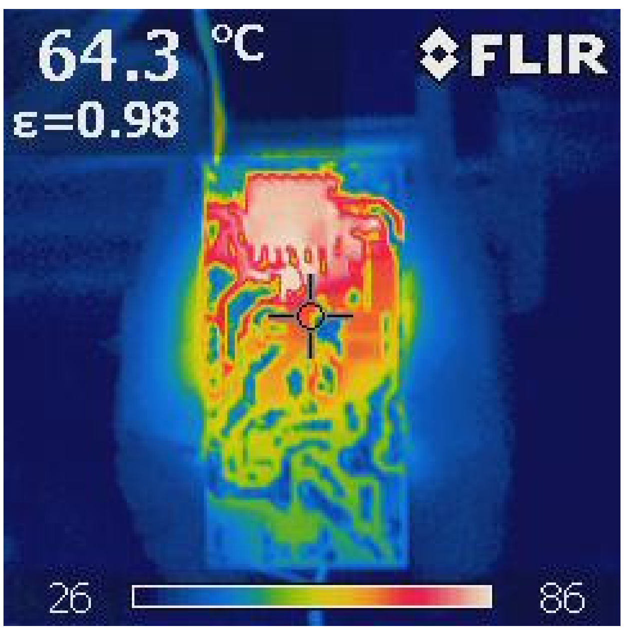

Figure 19 – Damper FET Q3 Case Temperature.

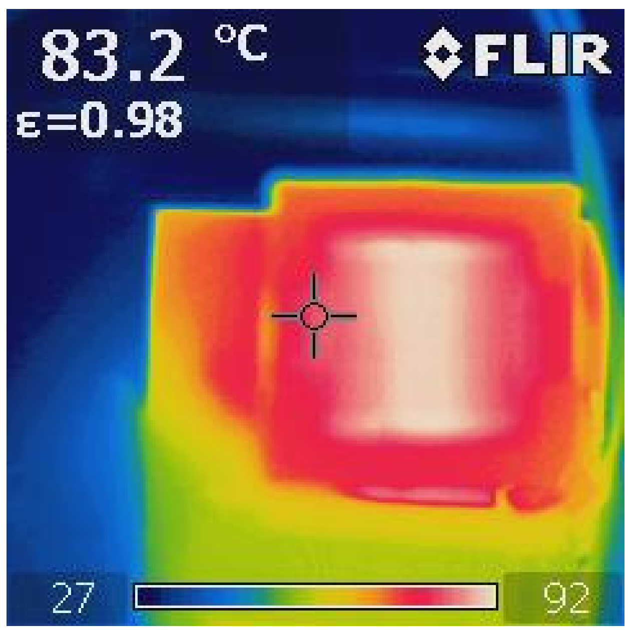

Figure 20 – Transformer T1.

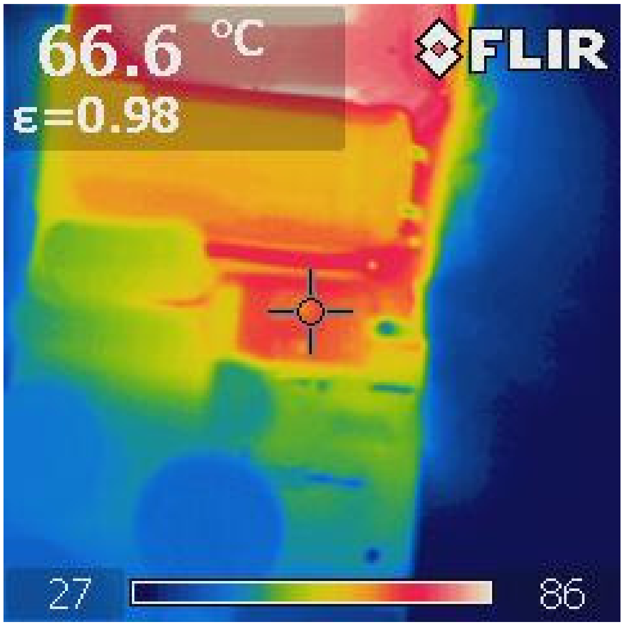

Figure 21 – D4 Output Diode.

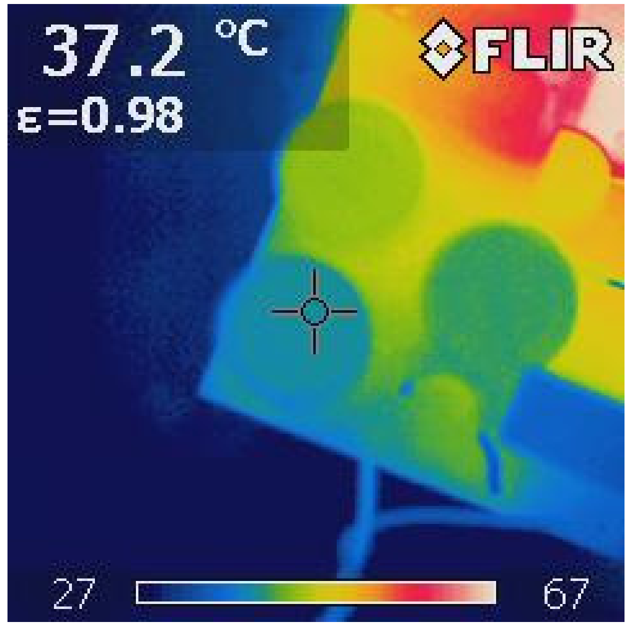

Figure 22 – L1 EMI Choke.

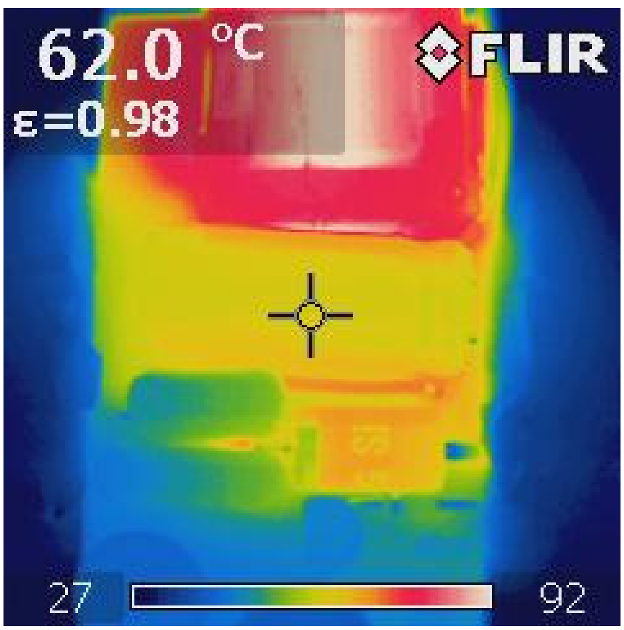

Figure 23 – C9 Output Capacitor.

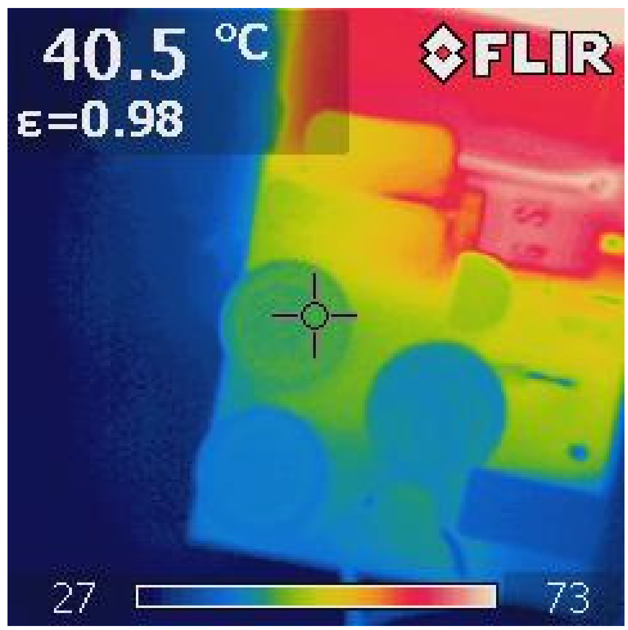

Figure 24 – L2 EMI Choke.

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12 Waveforms

12.1 Drain Voltage and Current, Normal Operation

No saturation in the inductor and design guaranteed to work in discontinuous mode within the operating input voltage.

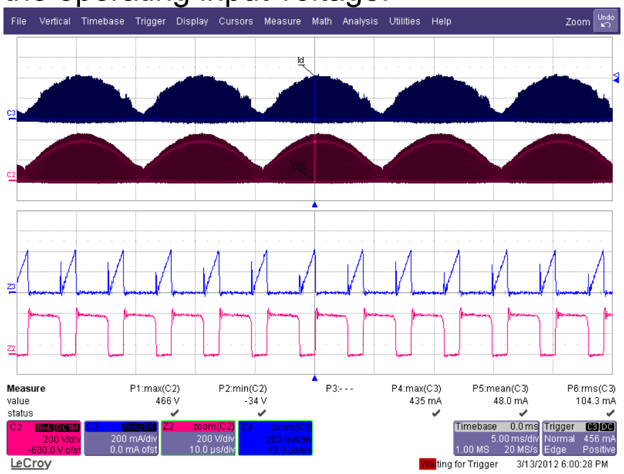

Figure 25 – 190 VAC / 50 Hz, 9 V LED String.
Ch2: V_{DRAIN}, 200 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

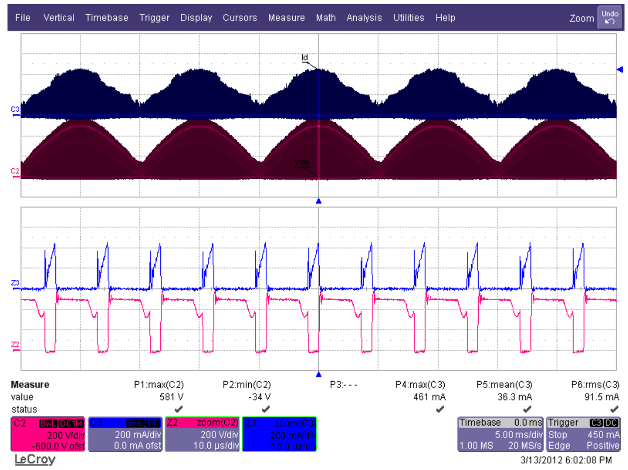

Figure 26 – 265 VAC / 50 Hz, 9 V LED String.
Ch2: V_{DRAIN}, 200 V / div.
Ch3: I_{DRAIN}, 0.2 A / div.
Time Scale: 5 ms / div.
Zoom Time Scale: 10 μs / div.

12.2 Drain Voltage and Current Start-up Profile

Device has a built in soft-start thereby reducing the stress in the device, transformer and output diode.

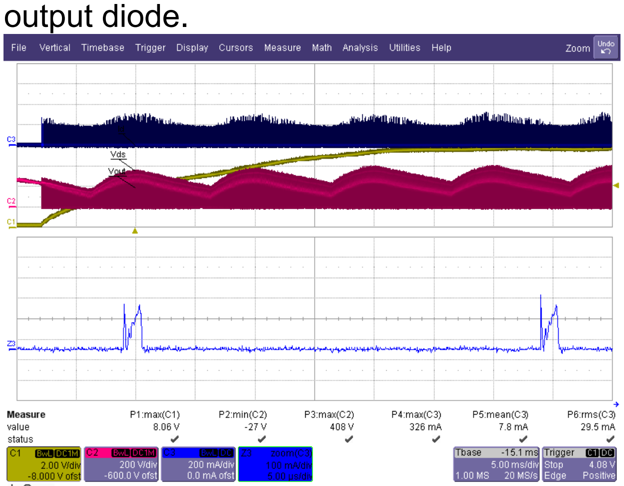

Figure 27 – 190 VAC / 50 Hz, 9 V LED String.
Ch1: V_{OUT}, 2 V / div.
Ch2: V_{DS}, 200 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale: 5 ms / div.
Zoom Time Scale: 5 μs / div.

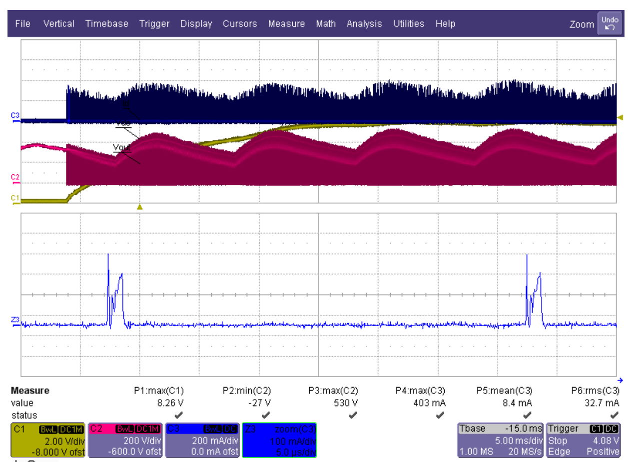

Figure 28 – 265 VAC / 50 Hz, 9 V LED String.
Ch1: V_{OUT}, 2 V / div.
Ch2: V_{DS}, 200 V / div.
Ch3: I_{DRAIN}, 200 mA / div.,
Time Scale: 5 ms / div.
Zoom Time Scale: 5 μs / div.

12.3 Output Voltage Start-up Profile

Start-up time <50 ms; the reference design will emit light within 50 ms at non-dimming operation.

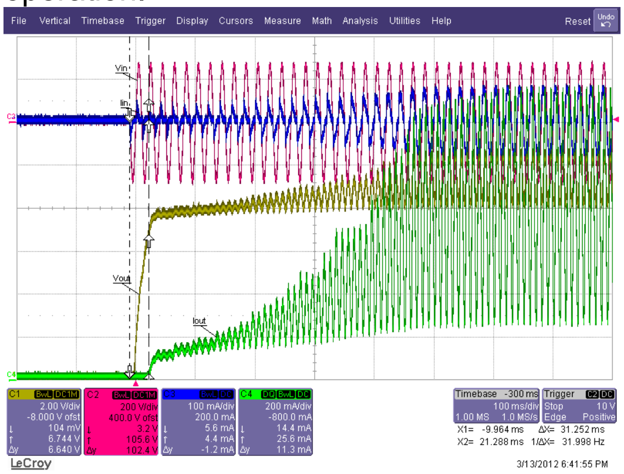

Figure 29 – 190 VAC / 60 Hz, 9 V LED.
Ch1: V_{OUT}, 2 V / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div., 100 ms / div.

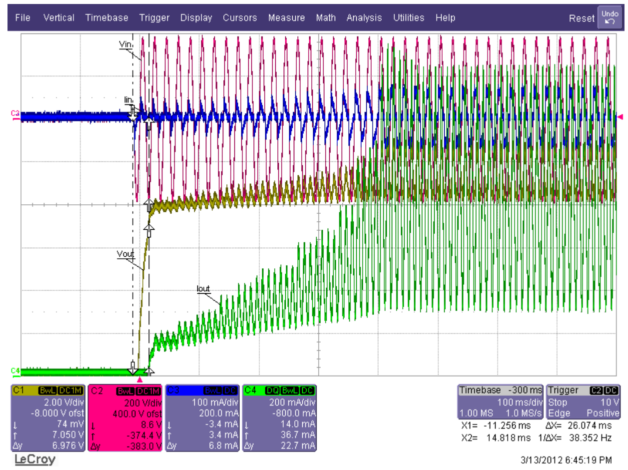

Figure 30 – 265 VAC / 60 Hz, 9 V LED.
Ch1: V_{OUT}, 2 V / div.
Ch2: V_{IN}, 200 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div., 100 ms / div.

12.4 Input and Output Voltage and Current Profiles

Output current ripple is inversely proportional to the impedance of the LED. Verify the current ripple on the actual LED to be used in the system. Increase output capacitance for less output current ripple.

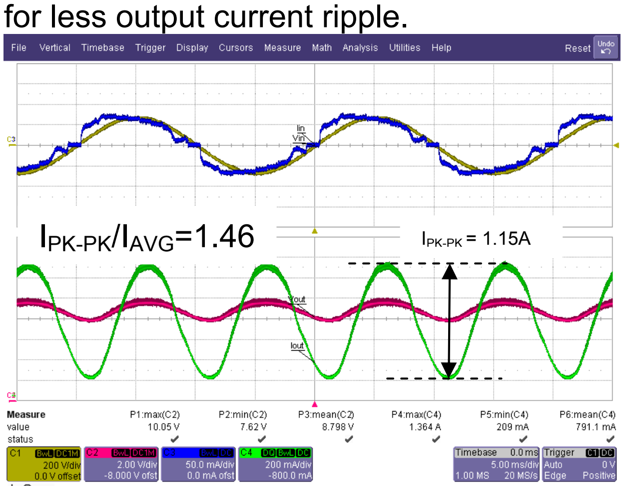

Figure 31 – 190 VAC / 50 Hz, 9 V LED String.
C_{OUT} = 680 μF
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 200 mA / div., 5 ms / div.

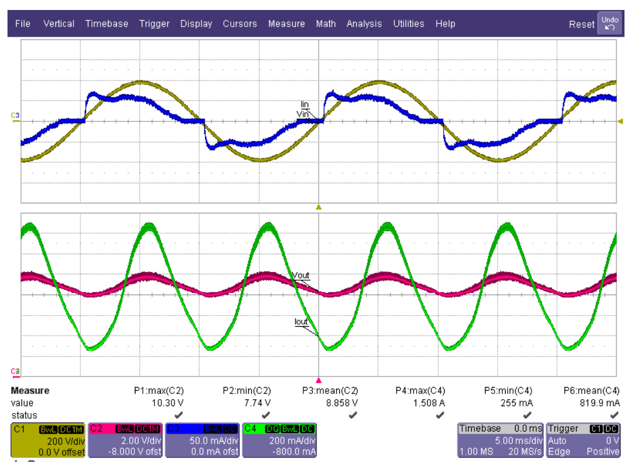

Figure 32 – 265 VAC / 50 Hz, 9 V LED String.
C_{OUT} = 680 μF
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 200 mA / div., 5 ms / div.

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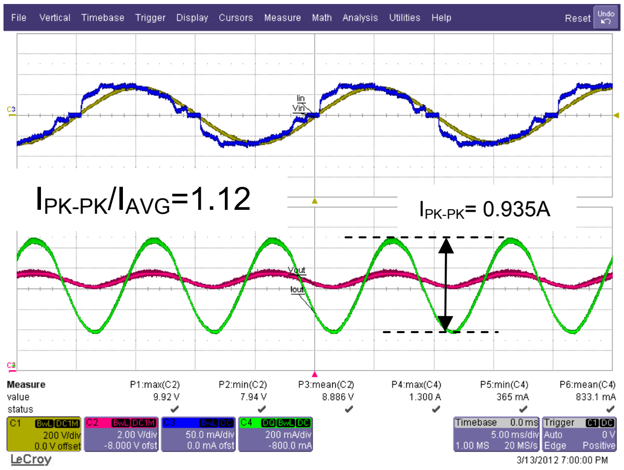

Figure 33 – 190 VAC / 50 Hz, 9 V LED String.
C_{OUT} = 2 X 680 μF
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 200 mA / div., 5 ms / div.

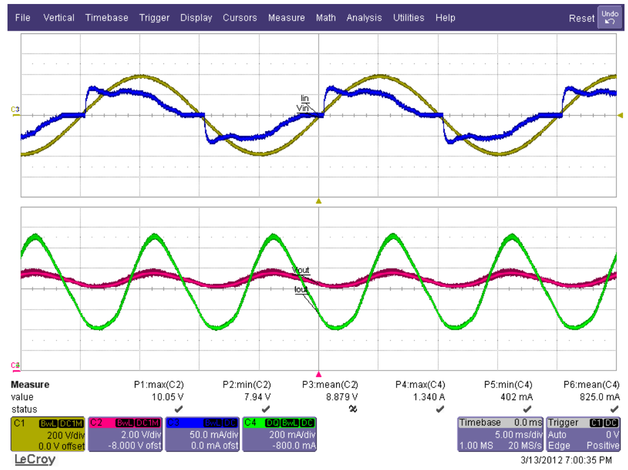

Figure 34 – 265 VAC / 50 Hz, 9 V LED String.
C_{OUT} = 2 X 680 μF
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 50 mA / div.
Ch4: I_{OUT}, 200 mA / div., 5 ms / div.

12.5 Drain Voltage and Current Profile: Normal Operation to Output Short

No saturation in the inductor during short-circuit, inductor current is limited by the I_{LIM}.

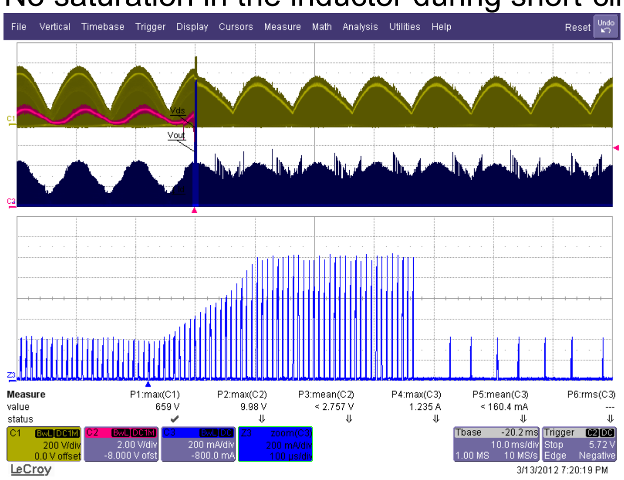

Figure 35 – 265 VAC / 50 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div., 10 ms / div.
Z3: I_{DRAIN}, 0.2A / div., 100 μs / div.

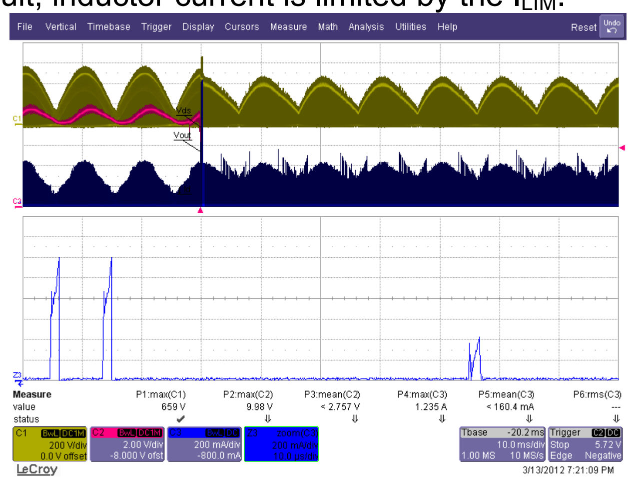

Figure 36 – 265 VAC / 50 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div., 10 ms / div.
Z3: I_{DRAIN}, 0.2A / div., 100 μs / div.

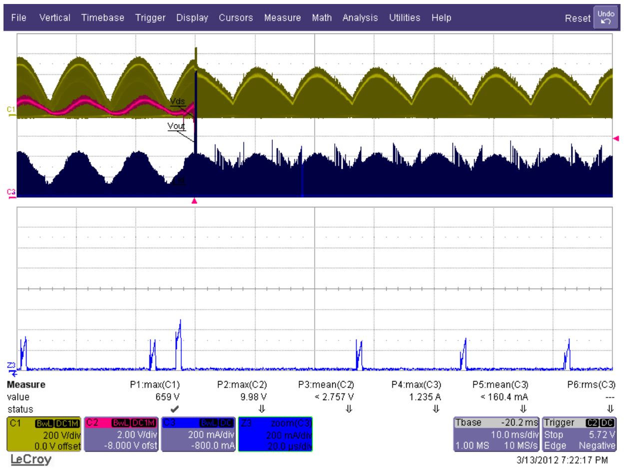

Figure 37 – 265 VAC / 50 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div., 10 ms / div.
Z3: I_{DRAIN}, 0.2 A / div., 200 µs / div.

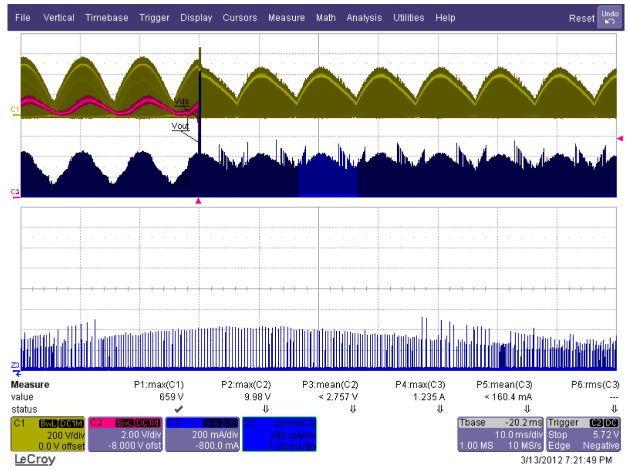

Figure 38 – 265 VAC / 50 Hz, Normal Operation then Output Short.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div., 10 ms / div.
Z3: I_{DRAIN}, 0.2 A / div., 1 ms / div.

12.6 Drain Voltage and Current Profile: Start-up with Output Shorted

No saturation in the inductor during start-up short-circuit due to the built-in soft-start.

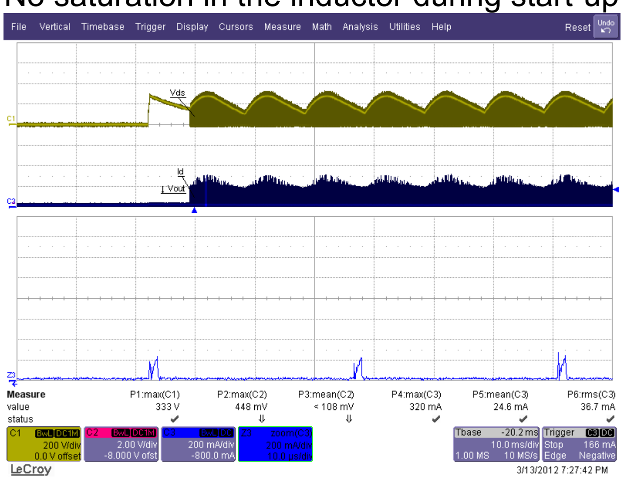

Figure 39 – 190 VAC / 50 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div, 10 ms / div.
Z3: I_{DRAIN}, 0.2 A / div., 10 µs / div.

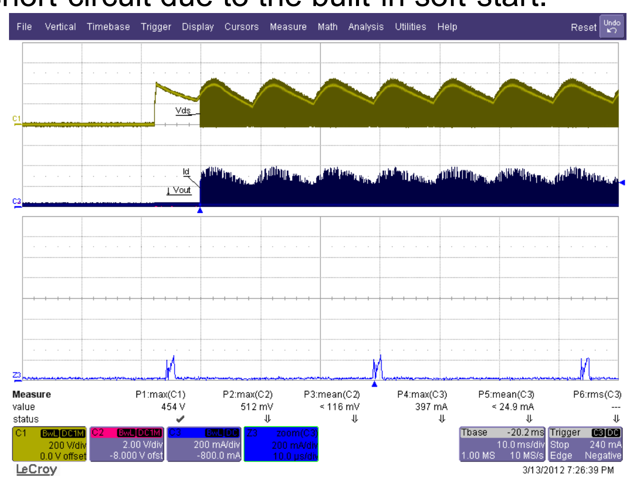

Figure 40 – 265 VAC / 50 Hz, Output Shorted.
Ch1: V_{DRAIN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{DRAIN}, 0.2 A / div, 10 ms / div.
Z3: I_{DRAIN}, 0.2 A / div., 10 µs / div.

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12.7 No-Load Operation

The driver is protected during no-load operation, U1 operating is cycle skipping mode.

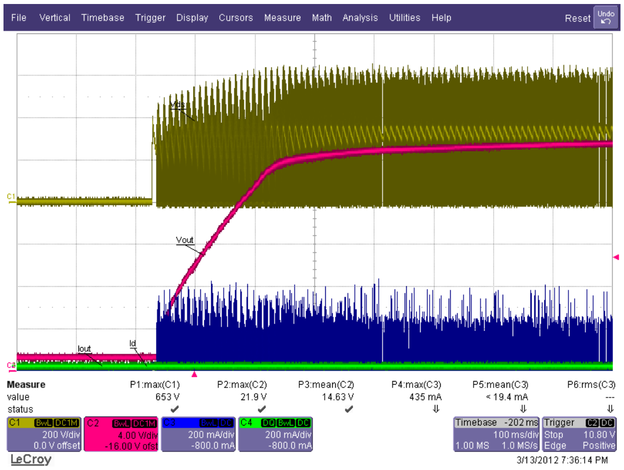

Figure 41 – 265 VAC / 50 Hz, Start-up No-load.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{OUT}, 4 V / div.
Ch2: I_{DRAIN}, 0.2 A / div.
Ch4: I_{OUT}, 0.2 A / div.
Time Scale: 100 ms / div.

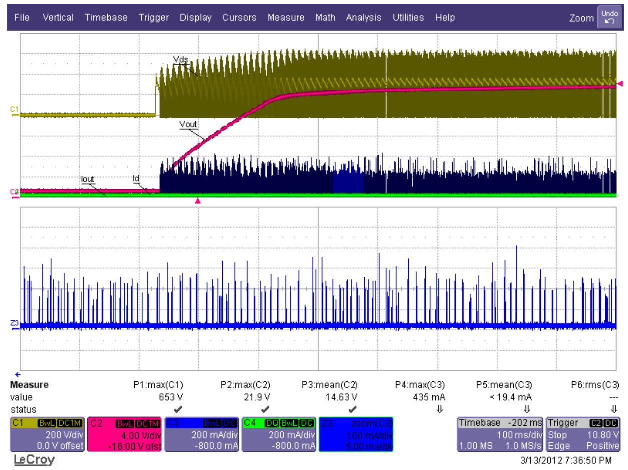

Figure 42 – 265 VAC / 50 Hz, Start-up No-load.
Ch1: V_{OUT}, 200 V / div.
Ch2: V_{OUT}, 4 V / div.
Ch2: I_{DRAIN}, 0.2 A / div.
Ch4: I_{OUT}, 0.2 A / div.,100 ms / div.
Z3: I_{DRAIN}, 0.1A / div., 5 s / div.

12.8 AC Cycling

The reference design has no perceptible delay.

Figure 43 – 230 VAC / 50 Hz,
1 s On – 1 s Off.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch4: I_{OUT}, 500 mA / div.
Time Scale: 2 s / div.

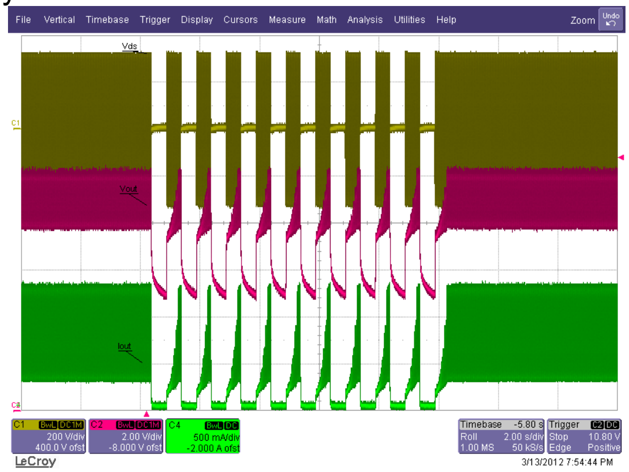

Figure 44 – 230 VAC / 50 Hz,
500 ms On – 500 ms Off.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch4: I_{OUT}, 500 mA / div.
Time Scale: 2 s / div.

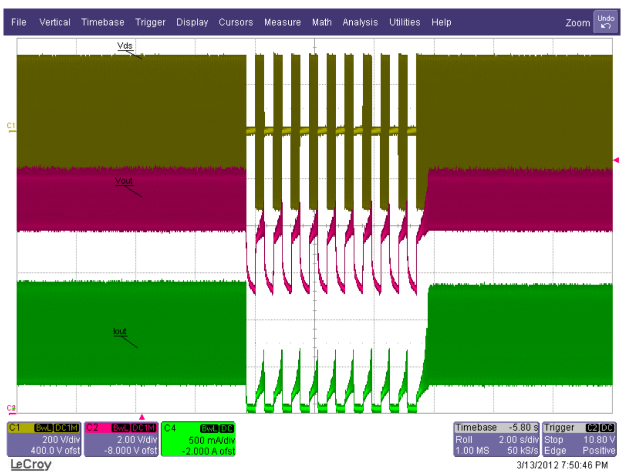

Figure 45 – 230 VAC / 50 Hz,
300 ms On – 300 ms Off.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch4: I_{OUT}, 500 mA / div.
Time Scale: 2 s / div.

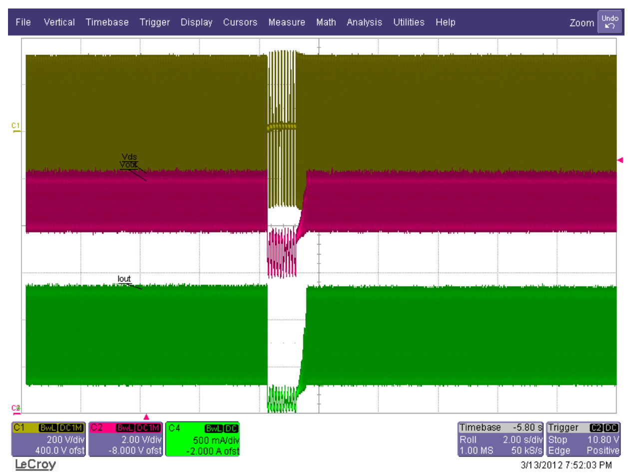

Figure 46 – 230 VAC / 50 Hz,
1 s On – 1 s Off.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch4: I_{OUT}, 500 mA / div.
Time Scale: 2 s / div.

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12.9 Dimming Sample Waveforms

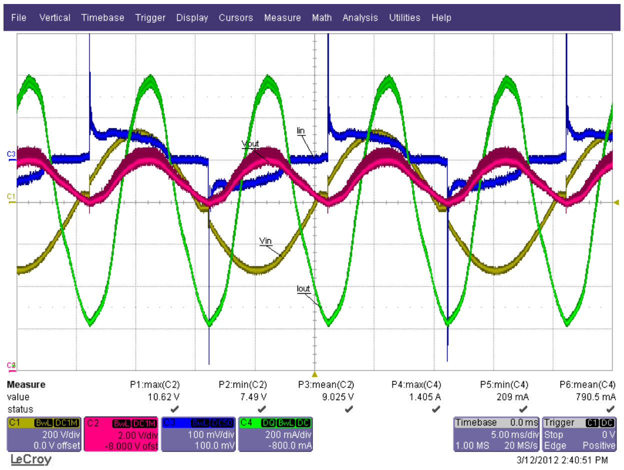

Figure 47 – 230 VAC / 50 Hz, Sen Bo Lang Chinese Dimmer at Full TRIAC Conduction.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div.
Time Scale: 5 ms / div.

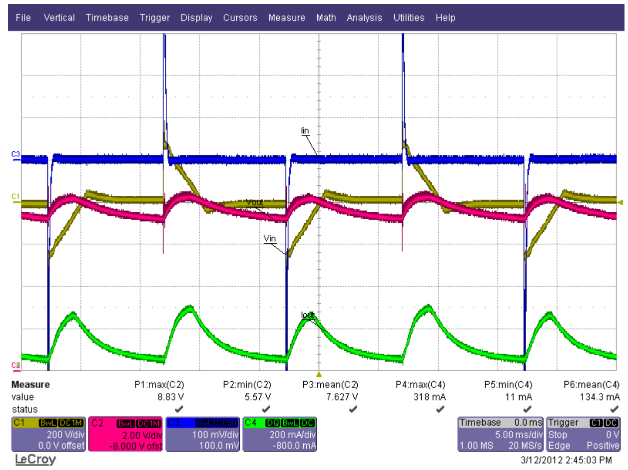

Figure 48 – 230 VAC / 50 Hz, Sen Bo Lang Chinese Dimmer at Minimum TRIAC Conduction.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div.
Time Scale: 5 ms / div.

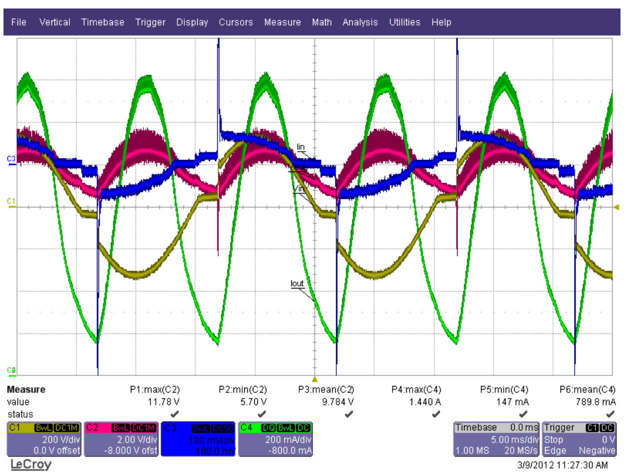

Figure 49 – 230 VAC / 50 Hz, BUSCH2250 600 W German Dimmer at Full TRIAC Conduction.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div.
Time Scale: 5 ms / div.

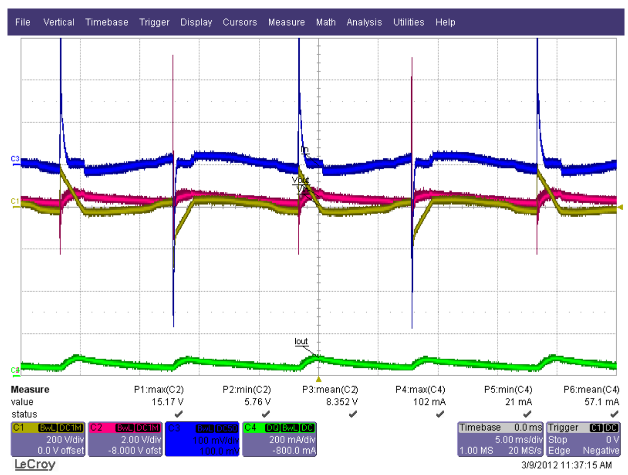

Figure 50 – 230 VAC / 50 Hz, BUSCH2250 600 W German Dimmer at Minimum TRIAC Conduction.
Load: 9 V LED String.
Ch1: V_{IN}, 200 V / div.
Ch2: V_{OUT}, 2 V / div.
Ch3: I_{IN}, 100 mA / div.
Ch4: I_{OUT}, 200 mA / div.
Time Scale: 5 ms / div.

12.10 Line Surge Waveform

12.10.1 Ring Wave Surge

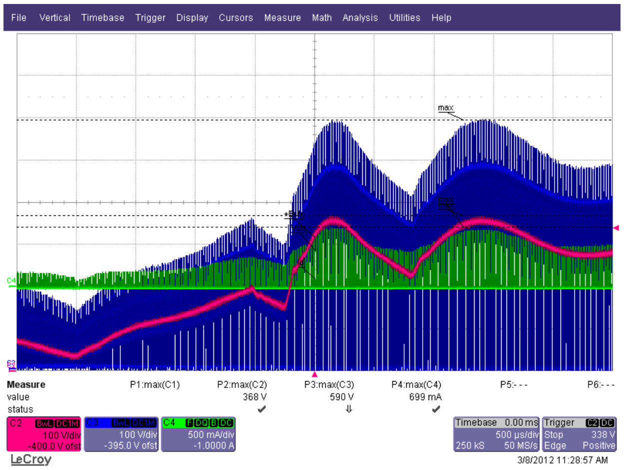

Figure 51 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 590 V_{PK}
(+) 2.5 kV Differential Ring Surge at 0º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 500 µs / div.

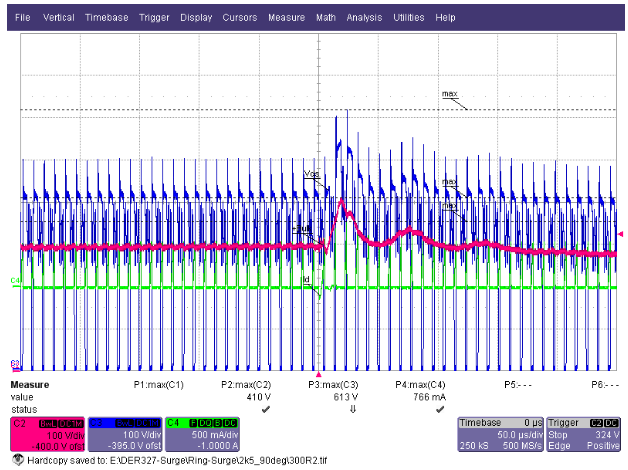

Figure 52 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 613 V_{PK}
(+) 2.5 kV Differential Ring Surge at 90º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 50 µs / div.

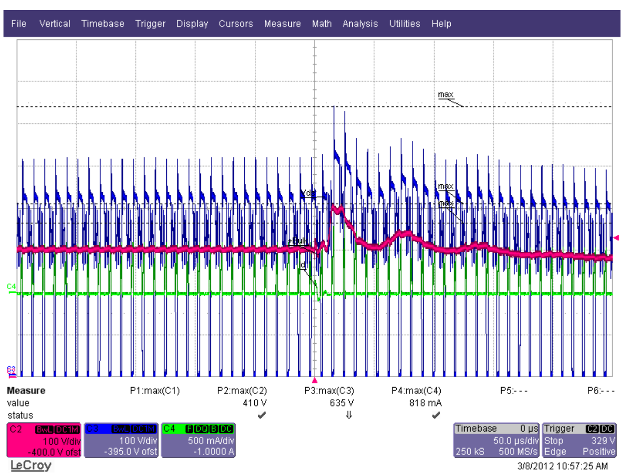

Figure 53 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 635 V_{PK}
(-) 2.5 kV Differential Ring Surge at 270º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 50 µs / div.

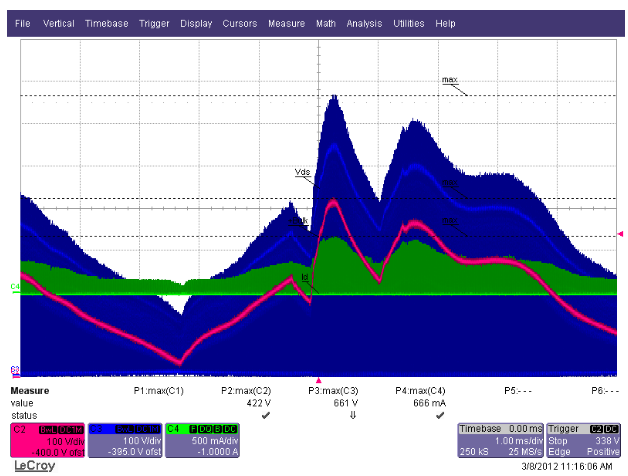

Figure 54 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 661 V_{PK}
(-) 2.5 kV Differential Ring Surge at 0º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 1 ms / div.

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12.10.2 Differential Line Surge

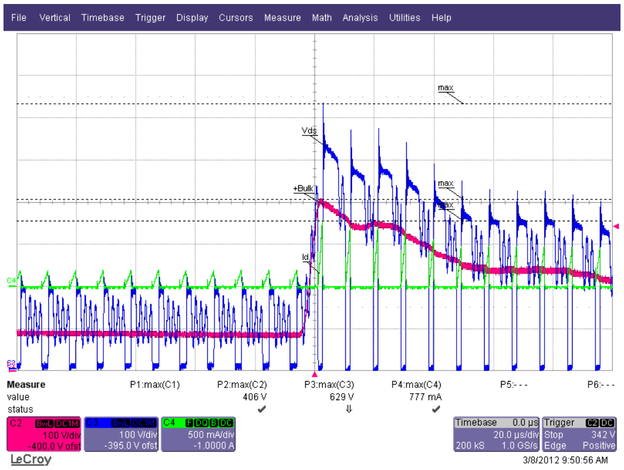

Figure 55 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 629 V_{PK}
(+) 500 V Differential Line Surge at 0º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 20 µs / div.

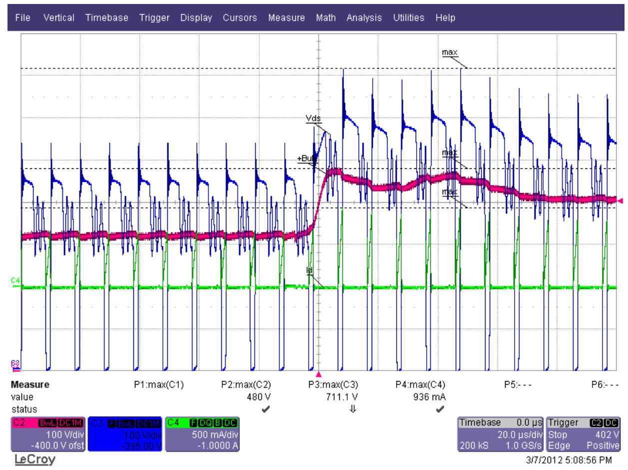

Figure 56 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 711 V_{PK}
(+) 500 V Differential Line Surge at 90º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 20 µs / div.

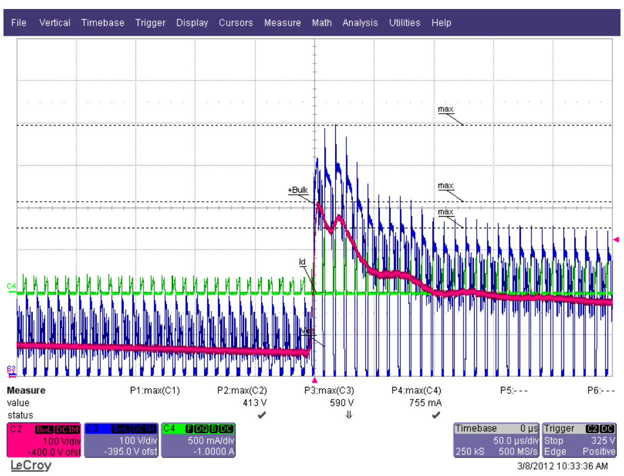

Figure 57 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 590 V_{PK}
(-) 500 V Differential Line Surge at 0º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 50 µs / div.

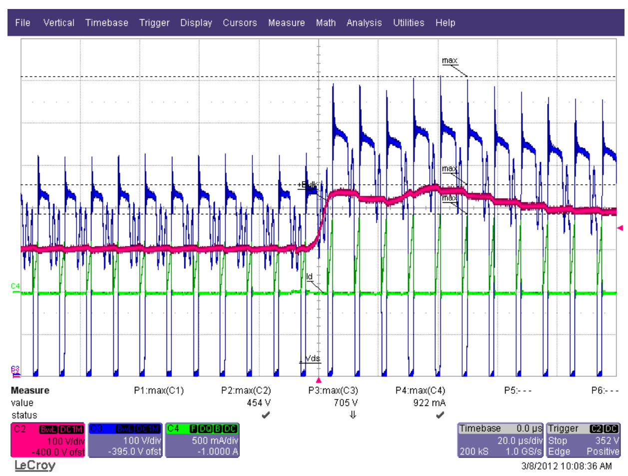

Figure 58 – 230 VAC / 60 Hz, 9 V Load,
V_{DS} = 705 V_{PK}
(-) 500 V Differential Line Surge at 270º.
Ch2: V_{BULK}, 100 V / div.
Ch3: V_{DS}, 100 V / div.
Ch4: I_{DRAIN}, 0.5 A / div.
Time Scale: 20 µs / div.

13 Line Surge

Input voltage was set at 230 VAC / 60 Hz. Output was loaded with 9 V LED string and operation was verified following each surge event. Two units were tested to confirm the results.

Differential input line 1.2 / 50 μs surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	230	L to N	0	Pass
-500	230	L to N	270	Pass
+500	230	L to N	90	Pass
-500	230	L to N	180	Pass

Differential input line ring surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	270	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	180	Pass

Unit operated normally under all test conditions.

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14 Conducted EMI

14.1 Equipment

Receiver:

Rohde & Schwartz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Schwartz
Two-Line-V-Network
Model No: ENV216

14.2 EMI Test Set-up

Usually the LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2) but since the lamp housing was not available the UUT was tested as shown in the Figure 59.

Figure 59 – Conducted Emissions Measurement Set-up.

14.3 EMI Test Result

Figure 60 – Conducted EMI, 9 V Output / 800 mA Steady-State Load, 230 VAC, 60 Hz, and EN55015 Limits.

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EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	9.64921816896 kHz	23.65	L1 gnd	
2	Average	11.6573068347 kHz	21.09	N gnd	
2	Average	129.530094744 kHz	28.73	N gnd	
1	Quasi Peak	165.693318812 kHz	47.31	L1 gnd	-17.85
2	Average	259.278686021 kHz	37.44	L1 gnd	-14.00
1	Quasi Peak	790.243042258 kHz	38.46	L1 gnd	-17.53
1	Quasi Peak	1.29965885429 MHz	38.62	L1 gnd	-17.37
1	Quasi Peak	1.71722750422 MHz	38.58	L1 gnd	-17.41
1	Quasi Peak	1.84110031489 MHz	38.03	L1 gnd	-17.96
2	Average	2.0745979178 MHz	22.90	L1 gnd	-23.09
1	Quasi Peak	2.24649226677 MHz	38.92	L1 gnd	-17.07
1	Quasi Peak	2.55671775336 MHz	38.50	L1 gnd	-17.49
2	Average	3.41194975314 MHz	23.43	L1 gnd	-22.56
1	Quasi Peak	3.80660433999 MHz	39.69	L1 gnd	-16.30
2	Average	3.80660433999 MHz	25.04	L1 gnd	-20.96
1	Quasi Peak	4.04078721227 MHz	38.63	L1 gnd	-17.36
2	Average	4.04078721227 MHz	23.89	L1 gnd	-22.10
1	Quasi Peak	4.20485937664 MHz	39.40	L1 gnd	-16.59
2	Average	20.4573750697 MHz	17.29	N gnd	-32.70
2	Average	29.8580960942 MHz	25.43	L1 gnd	-24.56

Figure 61 – Conducted EMI, 9 V / 800 mA Steady-State Load Steady-State Load, 230 VAC, 60 Hz, and EN55015 Limits. Line and Neutral Scan Design Margin Measurement.

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
29-Jun-12	JDC	1.0	Initial Release	Apps & Mktg

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