Design Example Report

Title	***88% Efficiency, High Power Factor Corrected (>0.99), 18 W_{max} Output Non-Isolated Buck-Boost LED Driver Using LinkSwitch™-PL LNK460VG***
Specification	90 VAC – 135 VAC Input; 85 V_{TYP}, 200 mA Output
Application	A19 LED Driver
Author	Applications Engineering Department
Document Number	DER-323
Date	June 21, 2012
Revision	1.0

Summary and Features

- Single-stage combined power factor correction and constant current (CC) output
- Low cost, low component count, small size and single-sided PCB
- Highly energy efficient, >88% at 115 VAC input for 85 V LED load
- Fast start-up time (<300 ms) – no perceptible delay
- Integrated protection and reliability features
  - Output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with hysteresis
  - No damage during brown-out conditions
- PF >0.99 at 115 VAC
- ATHD <20% at 115 VAC
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. In addition, this design does not provide galvanic isolation of the output from the AC input. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

The document describes a non-isolated, high efficiency, high power factor (PF) LED driver designed to drive a nominal LED string voltage of 85 V at 200 mA from an input voltage range of 90 VAC to 135 VAC (47 Hz – 63 Hz). The LED driver utilizes the LNK460VG from the LinkSwitch-PL family of ICs.

The topology used is a single-stage non-isolated buck-boost that meets the stringent space and efficiency requirements for this design. LinkSwitch-PL based designs provide a high power factor (>0.99) meeting international requirements.

This document contains the LED driver specification, schematic, PCB details, bill of materials, transformer documentation and typical performance characteristics.

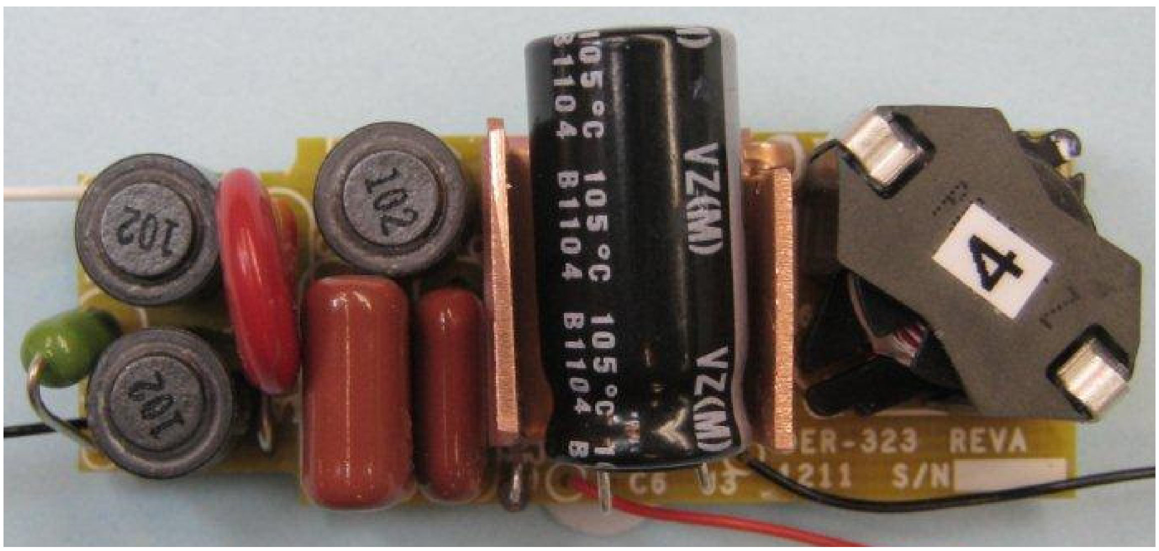

Figure 1 – Populated Circuit Board, Top View.

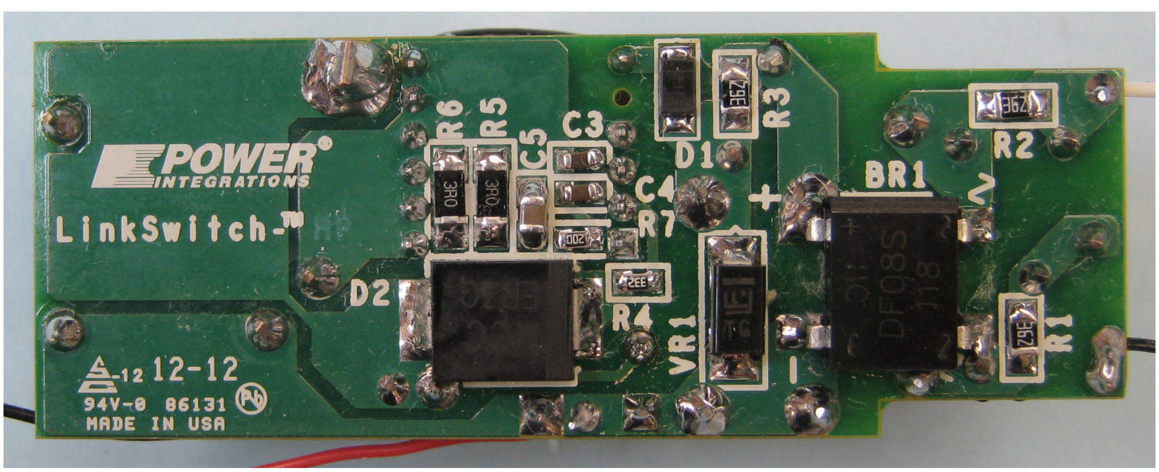

Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90	100/115	135	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		60		Hz	
Output						
Output Voltage	V_{OUT}	80	85	90	V	
Output Current	I_{OUT}		200		mA	
Total Output Power						
Continuous Output Power	P_{OUT}			18	W	
Efficiency						
Full Load	η	86	88		%	Measured at P_{OUT} 25 ^{o}C
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Non-Isolated				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	
Differential Surge (1.2 / 50 μs)			1000		V	
Power Factor		0.99				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 115 VAC, 60 Hz
Harmonic Currents		EN 61000-3-2 Class D (C)				Class C specifies Class D Limits when P_{IN} <25 W
ATHD				20	%	At 115 VAC
Ambient Temperature	T_{AMB}		40		^{o}C	Free convection, sea level

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3 Schematic

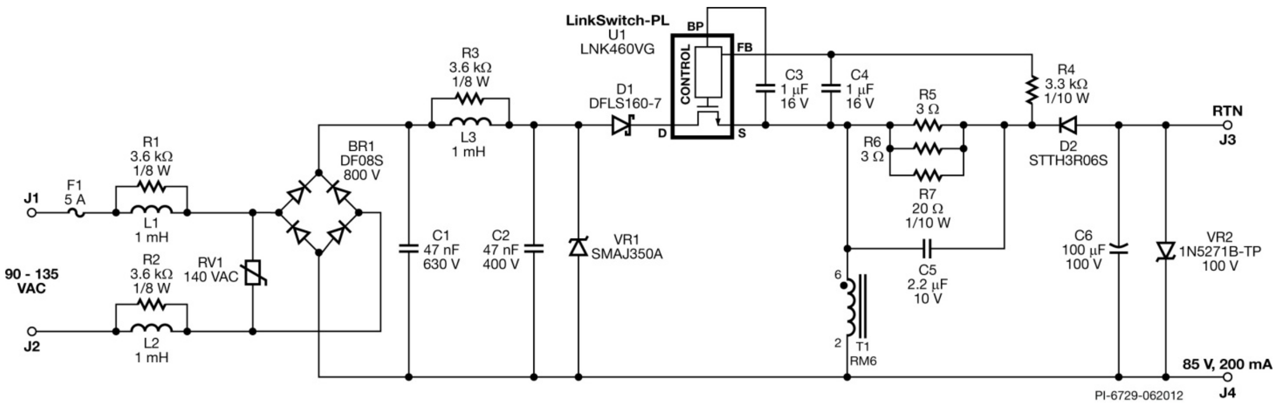

Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary-side controller intended for use in LED driver applications. The LinkSwitch-PL provides high power factor while regulating the output current across a range of input (90 VAC to 135 VAC) in a single conversion stage. The design also supports the output voltage variation typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus the high-voltage power MOSFET is incorporated into the IC.

4.1 Input EMI Filtering

Inductors L1-L3 and C1-C2 filters the input switching current presented by the buck-boost converter to the input line. Resistor R1, R2 and R3 across L1, L2 and L3 damp any resonances between the input inductors, capacitors and the AC line impedance which would ordinarily show up as increased conducted EMI.

MOV RV1 and VR1 provide a clamp to limit the maximum voltage during differential line surge events. The 140 V rating has a clamping voltage of <400 V providing a large margin with respect to the 725 V rating of U1. Bridge rectifier BR1 rectifies the AC line voltage with capacitor C1 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C1 and C2) is necessary to maintain a power factor of greater than 0.9.

4.2 Power and Feedback Circuits

The circuit is configured as a buck-boost converter with the SOURCE (S) pin of U1 connected to the cathode of the freewheeling diode D2 through current sense resistors. The current sense resistors R5, R6, and R7 are used to sense the diode current in the buck-boost converter. The resistor value is adjusted to center the output current at 200 mA at nominal input voltage. Capacitor C4 and R4 are used to filter the high frequency component of the diode current, which helps improve overall efficiency

The DRAIN (D) pin is connected to the positive side of the DC rectified input thru D1. Diode D1 is used to prevent reverse current from flowing through U1. An RM6 core size was selected to optimize the inductor for highest system efficiency.

Capacitor C3 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C3 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN pin.

4.3 Disconnected Load Protection

The system is protected by VR2 if the load is not connected. This prevents catastrophic failure of C6 (output capacitor). Zener diode VR2 will short the output it the load is not connected; this protection is not auto-recovering. Note that at the system level the LED load is always connected.

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Another option shown in Figure 3A is an auto restart overvoltage protection. Zener VR2 is connected to V_{OUT+} and in series with blocking diode D4. If a no-load condition occurs on the output of the supply, the output overvoltage Zener diode (VR2 in Figure 3A) will conduct once its threshold is reached. A voltage in excess of $V_{FB(AR)}$ = 2 V will appear across the FEEDBACK (FB) pin, and the IC will enter auto-restart. Note: Diode D4 is not included in the PCB layout.

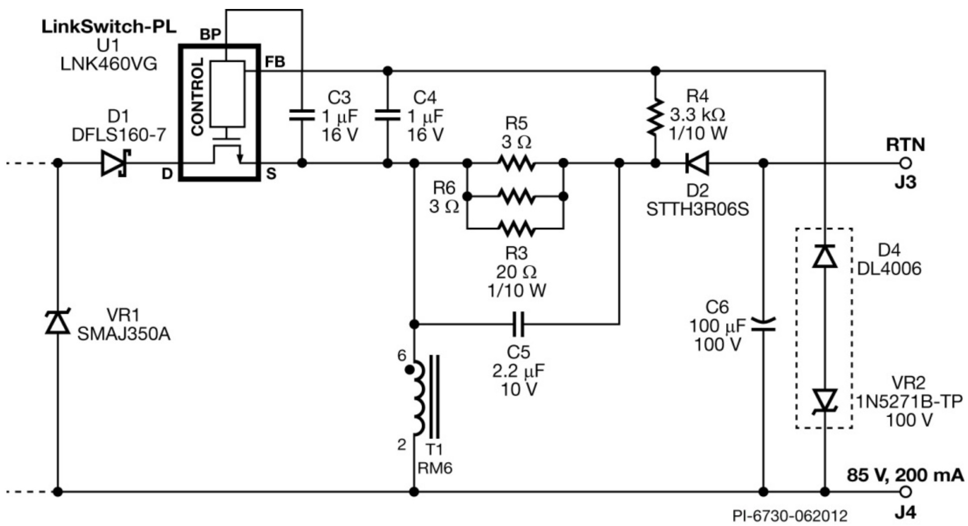

Figure 3A – Auto-Restart Overvoltage Protection with Buck-Boost Configuration.

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5 PCB Layout

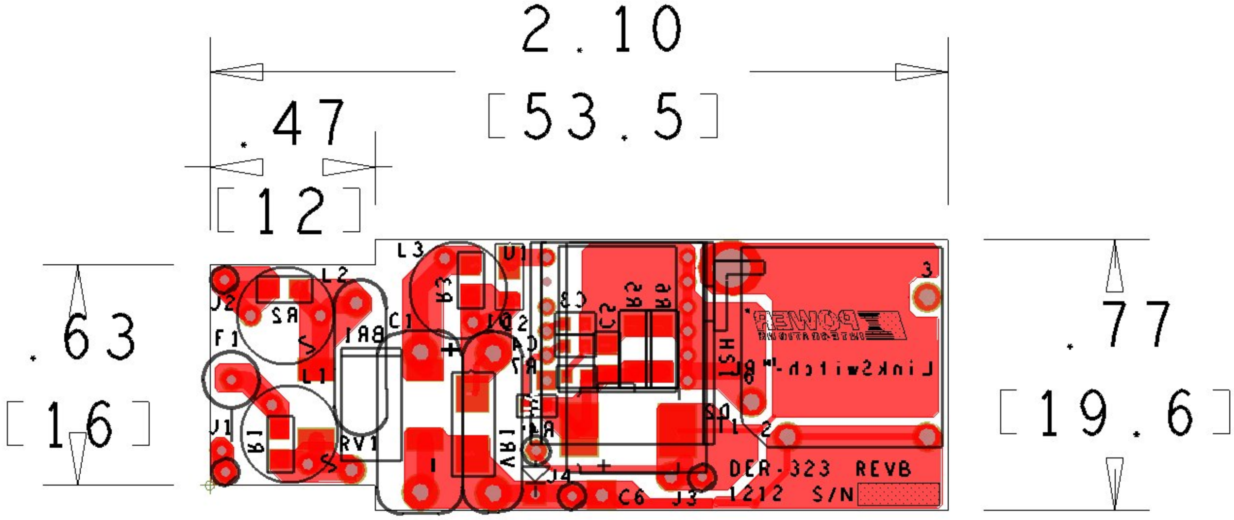

Figure 4 – PCB Layout and Outline (in/[mm]).

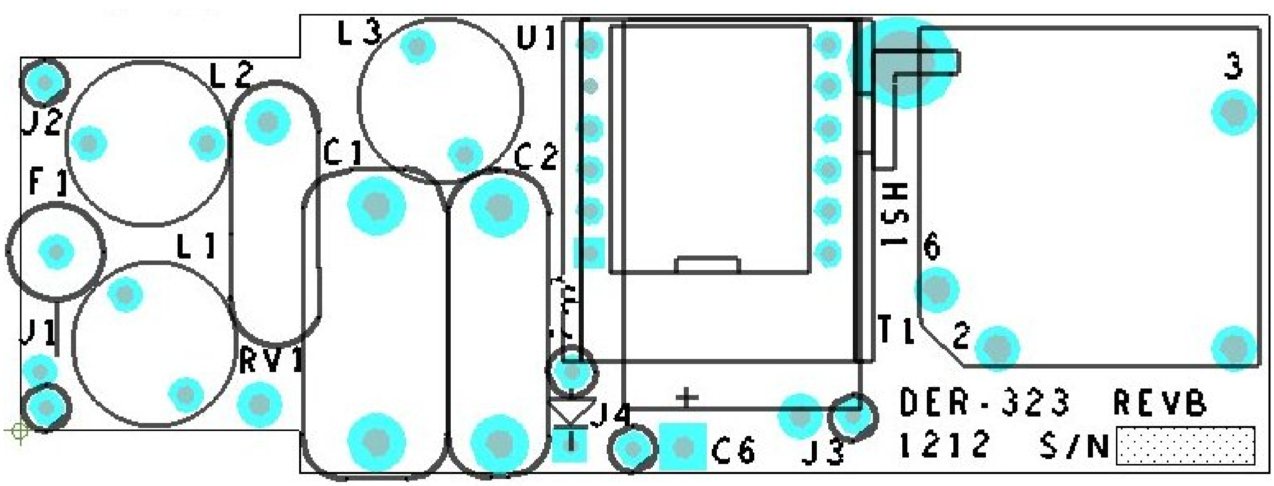

Figure 5 – Top Side.

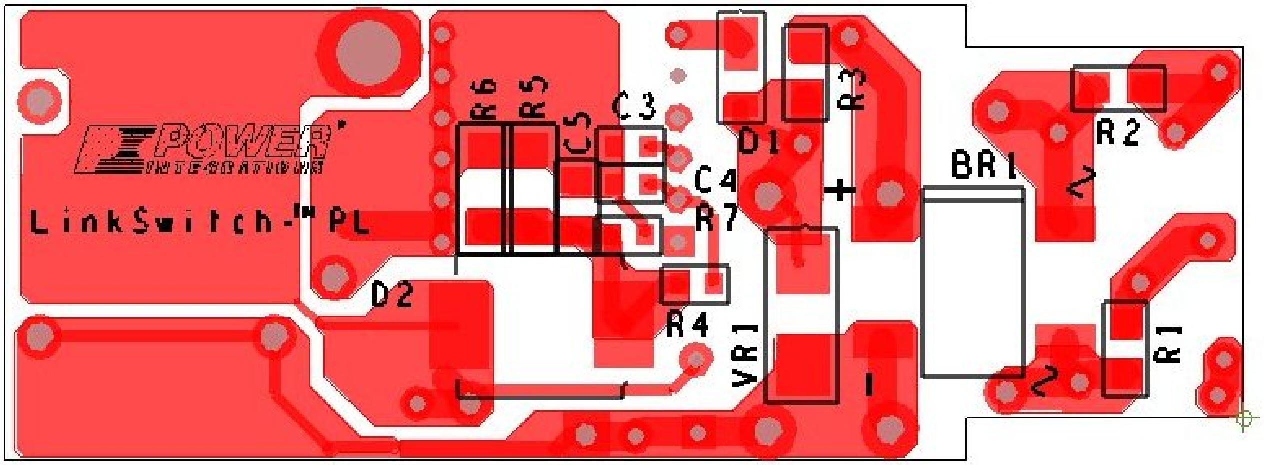

Figure 6 – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 1 A, Bridge Rectifier, SMD, DFS	DF08S	Diodes, Inc.
2	1	C1	47 nF, 630 V, Film	ECQ-E6473KF	Panasonic
3	1	C2	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
4	2	C3 C4	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
5	1	C5	2.2 μF, 10 V, Ceramic, X7R, 0805	GRM21BR71A225MA01L	Murata
6	1	C6	100 μF, 100 V, Electrolytic, Gen. Purpose, (10 x 20)	UVZ2A101MPD	Nichicon
7	1	D1	60 V, 1 A, Diode Schottky, PWRDI 123	DFLS160-7	Diodes, Inc.
8	1	D2	600 V, 3 A, SMC, DO-214AB	STTH3R06S	ST Micro
9	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	Littlefuse
10	3	L1 L2 L3	1 mH, 0.23 A, Ferrite Core	CTSCH875DF-102K	CT Parts
11	3	R1 R2 R3	3.6 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ362V	Panasonic
12	1	R4	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
13	2	R5 R6	3 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ3R0V	Panasonic
14	1	R7	20 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ200V	Panasonic
15	1	RV1	140 V, 22 J, 10 mm, RADIAL	V140LA5P	Littlefuse
16	1	T1	Bobbin, RM6, Vertical, 6 pins	B65808-N1006-D1	Epcos
17	1	U1	LinkSwitch-PL, eDIP-12P	LNK460VG	Power Integrations
18	1	VR1	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	Littlefuse
19	1	VR2	100 V, 5%, 500 mW, DO-35	1N5271B-TP	Micro Commercial
20	1	HS1	Heat Sink, Fab, eSIP with Brackets, DER-323, PI Custom		

7 Inductor Specification

7.1 Electrical Diagram

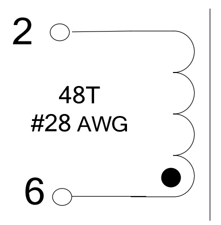

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 2-6, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	330 µH ±10%
Resonant Frequency	Pins 2-6, all other windings open	2 MHz (Min.)

7.3 Materials

Item	Description
[1]	Core: TDKPC95RM6S/I.
[2]	Bobbin: B-RM6-V-6pins-(3/3) with mounting clip, CLIP-RM6.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 6.4 mm wide.
[4]	Wire: Magnet, #28 AWG, solderable double coated.

7.4 Inductor Build Diagram

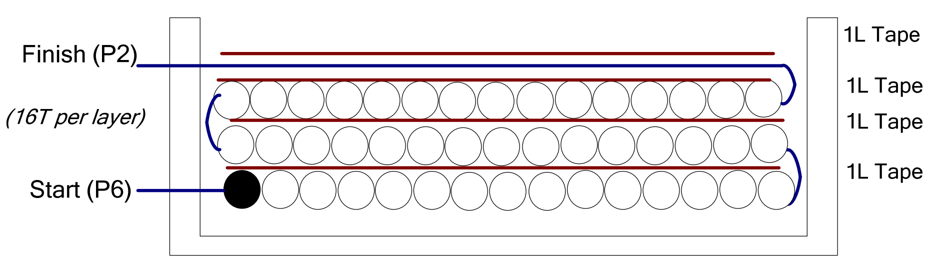

Figure 8 – Inductor Build Diagram.

7.5 Inductor Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WDG 1	Starting at pin 6, wind 48 turns of wire item [4] in three layers. Apply one layer of tape item [3] per layer. Finish at pin 2.
Final Assembly	Grind core to 330 µH inductance. Assemble and secure halves with mounting clips.

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8 Inductor Design Spreadsheet

ACDC_LinkSwitch-PL-Buck-Boost_121211; Rev.1.0; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL-Buck-Boost_121211; LinkSwitch-PL Buck-Boost Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	90		90	V	Minimum AC input voltage
VACNOM			115	V	Nominal AC input voltage
VACMAX	135		135	V	Maximum AC input voltage
FL			50	Hz	Minimum line frequency
VO_MIN			80.8	V	Minimum output voltage tolerance
VO_NOM	85.00		85.00	V	Nominal Output Voltage
VO_MAX			89.25	V	Maximum output voltage tolerance
IO	0.200		0.200	A	Average output current specification
n	0.88		0.880	%/100	Total power supply efficiency
Z			0.5		Loss allocation factor
Enclosure	Retrofit Lamp		Retrofit Lamp		Enclosure selections determine thermal conditions and maximum power. Enter "Retrofit Lamp" or "Open frame"
PO			17.00	W	Total output power
VD			0.4	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES					
Device	LNK460		LNK460		Chosen LinkSwitch-PL Device
TON			2.72	us	Expected on-time of MOSFET at low line and PO
FSW			122.8	kHz	Expected switching frequency at low line and PO
Duty Cycle			33.4	%	Expected operating duty cycle at low line and PO
VDRAIN			301	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS			0.317	A	Nominal RMS current through the switch
IPK			1.444	A	Worst Case Peak current
ILIM_MIN			1.637	A	Minimum device current limit
KDP			1.05		LinkSwitch-PL must operate in discontinuous mode (KDP > 1), change the device
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			1.450	Ohms	Output current sense resistor
Standard RSENSE			1.47	Ohms	Closest 1% value for RSENSE
PSENSE			58.0	mW	Power dissipated by RSENSE
ENTER INDUCTOR CORE/CONSTRUCTION VARIABLES					
Core Type	RM6S/I		RM6S/I		Core Type
AE			37.00	mm^2	Core Effective Cross Sectional Area
LE			29.20	mm	Core Effective Path Length
AL			2150	nH/T^2	Ungapped Core Effective Inductance
BW			6.3	mm	Bobbin Physical Winding Width
L	3		3		Number of winding layers
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			330.0	uH	Primary Inductance
LP Tolerance			10	%	Tolerance of Primary Inductance
N	48.00		48	Turns	Number of Turns
ALG			143	nH/T^2	Gapped Core Effective Inductance
BM			2684	Gauss	Operating Flux Density
BAC			1342	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)

BP		Warning	4257	Gauss	!!! Reduce peak flux density (BP < 3600 G) by increasing NP, selecting a bigger core or decreasing KDP
LG			0.325	mm	Gap Length (Lg > 0.1 mm)
BWE			18.9	mm	Effective Bobbin Width
L_IRMS			0.542	A	RMS Current through the inductor
OD			0.39	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.33	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			297	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Current Density (J)			6.69	A/mm^2	Inductor Winding Current density (3.8 < J < 9.75 A/mm^2)
Output Parameters					
IO			0.200	A	Expected Output Current
PIVD			401.7	V	Peak Inverse Voltage at VO_MAX on output diode

Note: The peak flux density warning (BP) can be ignored for this design. The spreadsheet BP calculation assumes that the LNK460VG will operate at $I_{LIM(MAX)}$ during start-up. In practice, due to the internal soft-start function this current level is not reached and therefore no core saturation occurs. This was confirmed in both Figures 38 and 39 for normal start-up and Figures 41 and 43 for start-up with a shorted output (fault condition). In all cases, the peak drain current is below the absolute maximum data sheet specification

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9 Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent the load range of 80 V to 90 V. Refer to the table in Section 8.6 for the complete set of test data values.

9.1 Efficiency

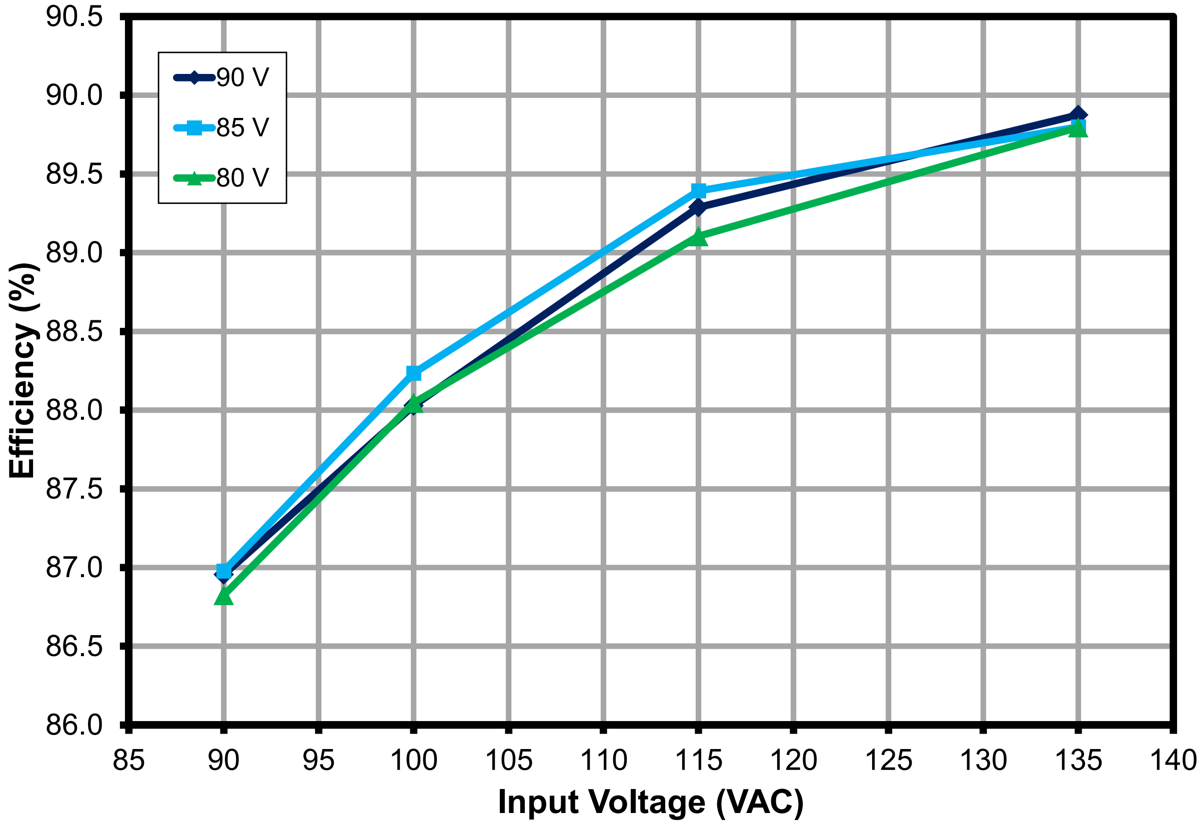

Figure 9 – Efficiency vs. Line and Load.

9.2 Line and Load Regulation

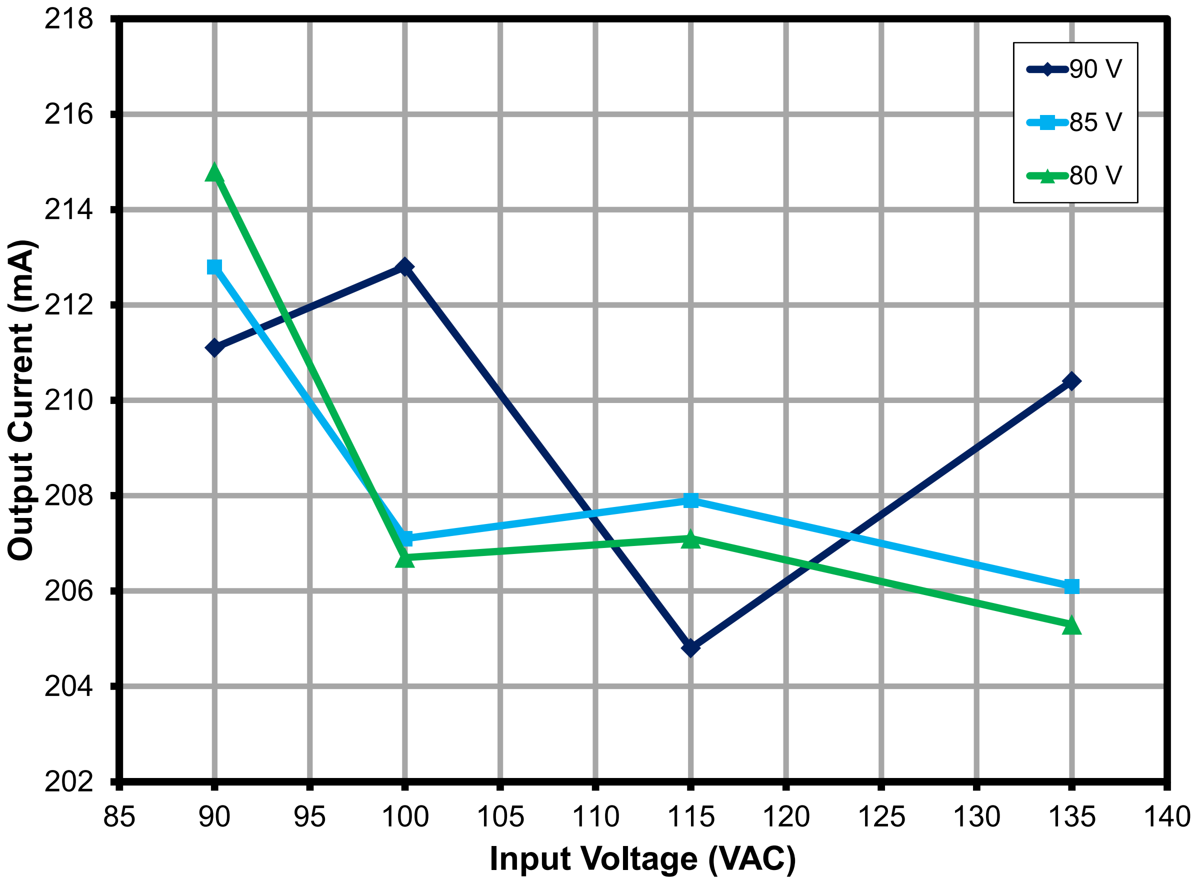

Figure 10 – Regulation vs. Line and Load.

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9.3 Power Factor

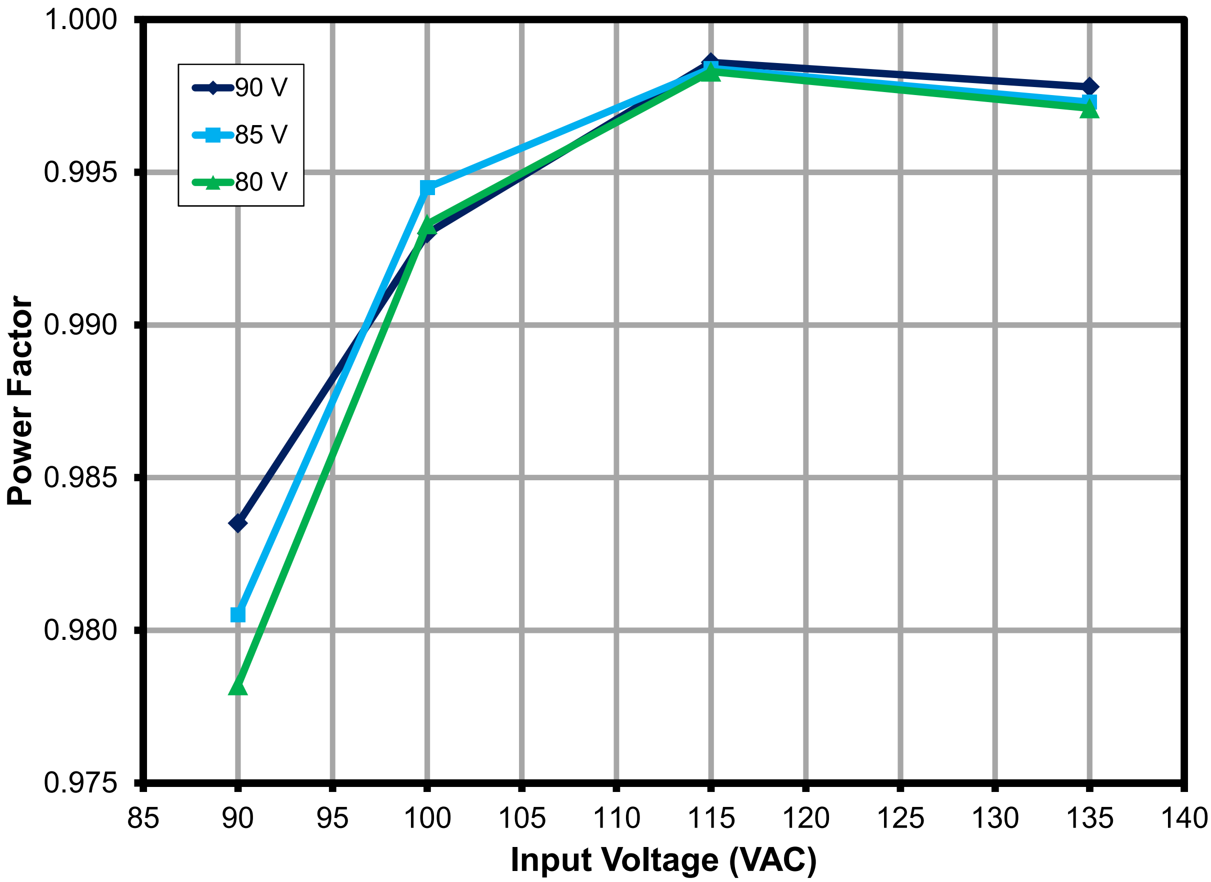

Figure 11 – Power Factor vs. Line and Load.

9.4 A-THD

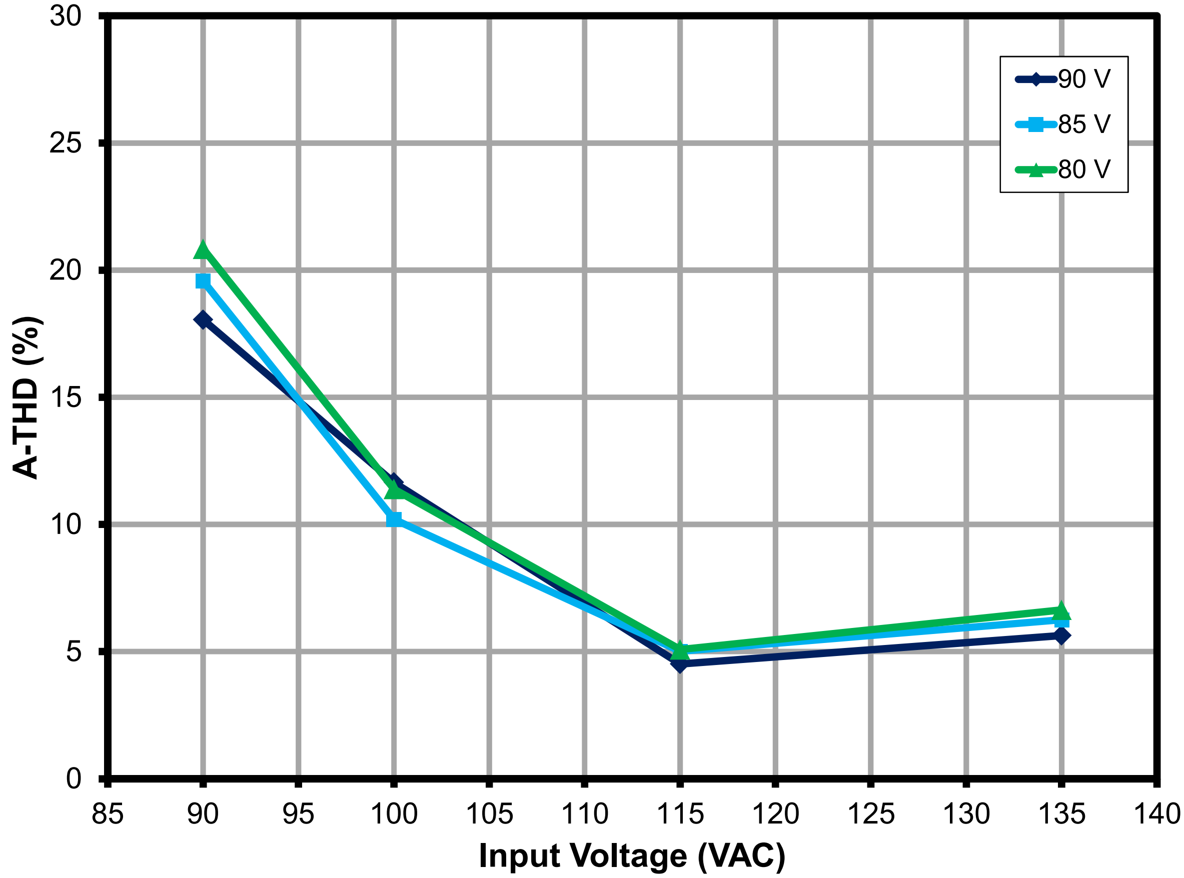

Figure 12 – A-THD vs. Line and Load.

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9.5 Harmonics

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment[1]. The limits shown in the charts below are Class D limits.

9.5.1 80 V LED Load

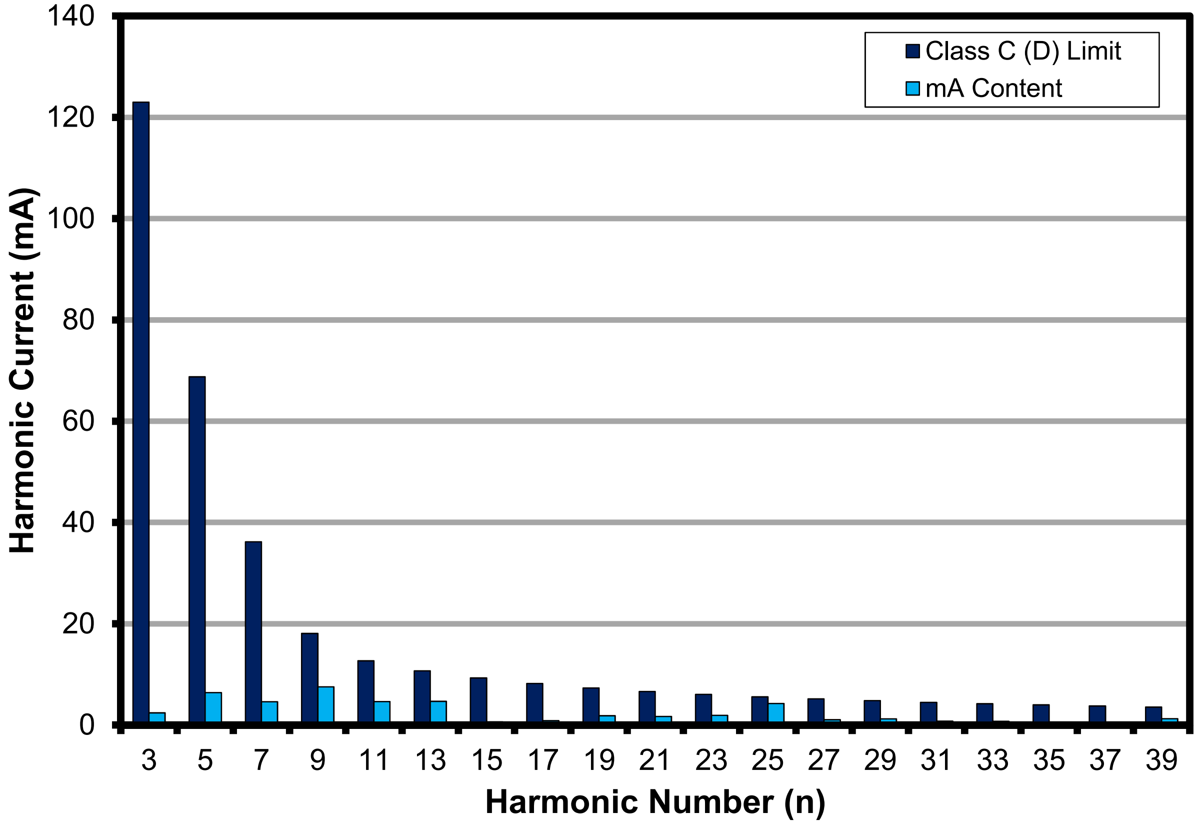

Figure 13 – 80 V LED Load Input Current Harmonics at 115 VAC, 60 Hz.

[1] IEC6000-3-2 Section 7.3, table 2, column 2.

9.5.2 85 V LED Load

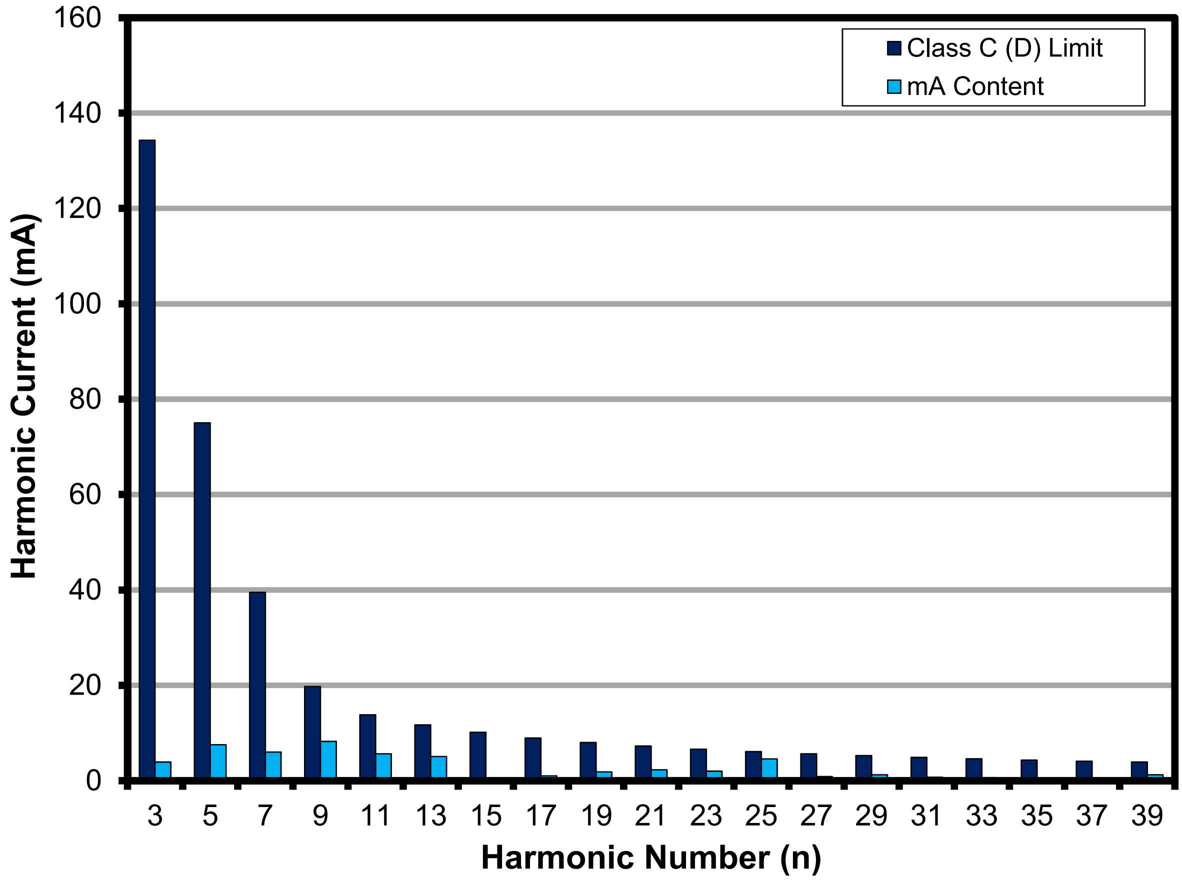

Figure 14 – 85 V LED Load Input Current Harmonics at 115 VAC, 60 Hz.

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9.5.3 90 V LED Load

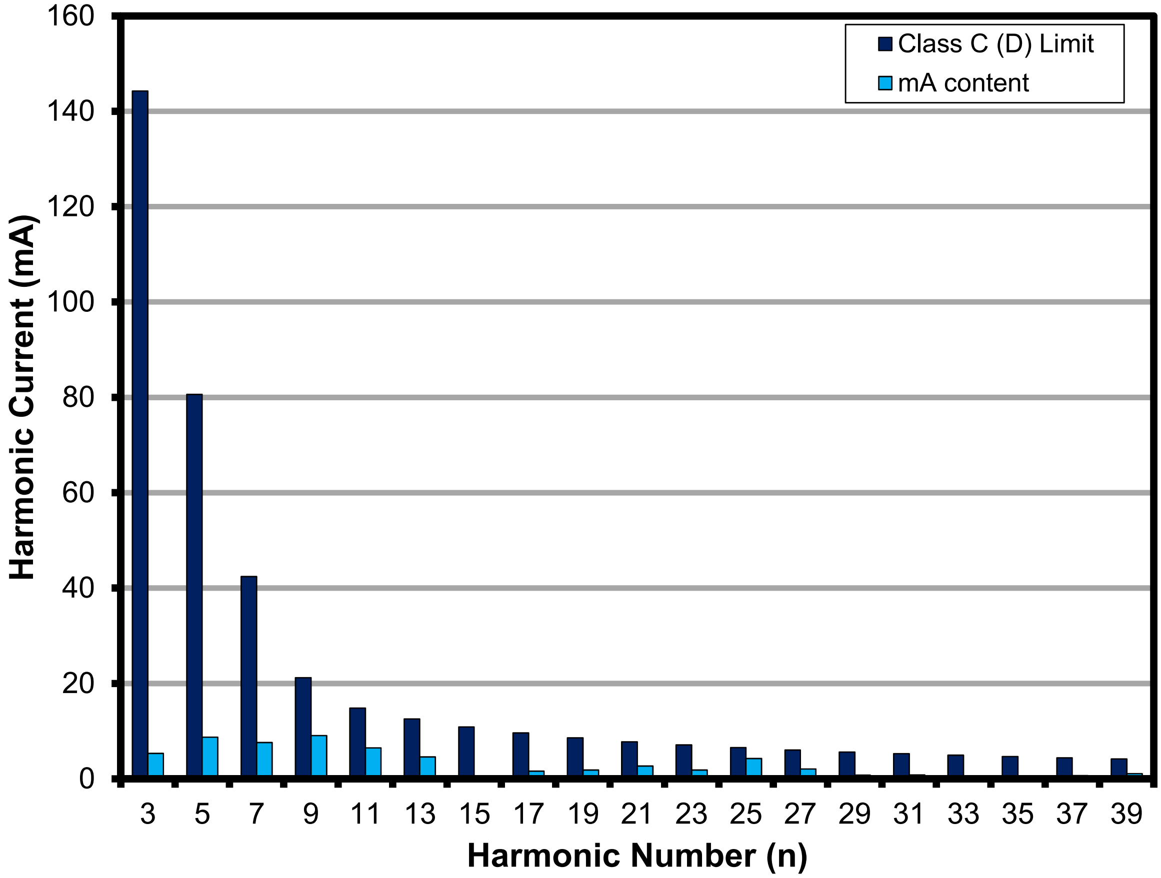

Figure 15 – 90 V LED Load Input Current Harmonics at 115 VAC, 60 Hz.

9.6 Test Data

All measurements were taken with the board in an open frame configuration, 25 ºC ambient, and 60 Hz line frequency.

9.6.1 Test Data, 80 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
90	60	89.88	226.36	19.902	0.978	20.84	79.6000	214.800	17.280	17.10	86.83	2.62
100	60	99.93	189.36	18.797	0.993	11.39	79.4000	206.700	16.550	16.41	88.05	2.25
115	60	114.96	161.94	18.585	0.998	5.08	79.4000	207.100	16.560	16.44	89.10	2.03
135	60	134.96	135.97	18.297	0.997	6.64	79.4000	205.300	16.430	16.30	89.80	1.87

9.6.2 Test Data, 85 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
90	60	89.89	237.42	20.925	0.981	19.57	84.7000	212.800	18.200	18.02	86.98	2.73
100	60	99.94	201.39	20.015	0.995	10.2	84.6000	207.100	17.660	17.52	88.23	2.36
115	60	114.96	172.82	19.834	0.998	5.01	84.6000	207.900	17.730	17.59	89.39	2.10
135	60	134.96	145.28	19.555	0.997	6.25	84.6000	206.100	17.560	17.44	89.80	2.00

9.6.3 Test Data, 90 V LED Load

Input		Input Measurement					Load Measurement			Calculation		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
90	60	89.87	248.13	21.931	0.984	18.05	89.6000	211.100	19.070	18.91	86.95	2.86
100	60	99.93	219.81	21.811	0.993	11.65	89.5000	212.800	19.200	19.05	88.03	2.61
115	60	114.95	179.72	20.630	0.999	4.51	89.4000	204.800	18.420	18.31	89.29	2.21
135	60	134.95	156.68	21.096	0.998	5.63	89.5000	210.400	18.960	18.83	89.87	2.14

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9.6.4 115 VAC 60 Hz, 80 V LED Load Harmonics Data

V	Freq	I (mA)	P	%THD
115	60.00	161.94	18.5850	5.08
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	161.63			
2	0.09	0.06%		
3	4.10	2.54%	126.3780	Pass
5	1.09	0.67%	70.6230	Pass
7	2.37	1.47%	37.1700	Pass
9	1.32	0.82%	18.5850	Pass
11	0.63	0.39%	13.0095	Pass
13	3.10	1.92%	11.0080	Pass
15	0.56	0.35%	9.5403	Pass
17	0.69	0.43%	8.4179	Pass
19	2.09	1.29%	7.5318	Pass
21	0.88	0.54%	6.8145	Pass
23	1.47	0.91%	6.2219	Pass
25	1.77	1.10%	5.7242	Pass
27	0.63	0.39%	5.3002	Pass
29	3.28	2.03%	4.9346	Pass
31	1.53	0.95%	4.6163	Pass
33	0.70	0.43%	4.3365	Pass
35	0.81	0.50%	4.0887	Pass
37	0.76	0.47%	3.8677	Pass
39	0.66	0.41%	3.6693	Pass

9.6.5 115 VAC 60 Hz, 85 V LED Load Harmonics Data

V	Freq	I (mA)	P	%THD
115	60.00	172.82	19.8340	5.01
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Remarks**
1	172.50			
2	0.23	0.13%		
3	4.45	2.58%	134.8712	Pass
5	1.68	0.97%	75.3692	Pass
7	3.00	1.74%	39.6680	Pass
9	0.20	0.12%	19.8340	Pass
11	1.34	0.78%	13.8838	Pass
13	2.30	1.33%	11.7478	Pass
15	0.54	0.31%	10.1815	Pass
17	0.63	0.37%	8.9836	Pass
19	2.18	1.26%	8.0380	Pass
21	1.46	0.85%	7.2725	Pass
23	1.08	0.63%	6.6401	Pass
25	2.32	1.34%	6.1089	Pass
27	0.98	0.57%	5.6564	Pass
29	3.33	1.93%	5.2663	Pass
31	0.91	0.53%	4.9265	Pass
33	0.55	0.32%	4.6279	Pass
35	0.77	0.45%	4.3635	Pass
37	0.68	0.39%	4.1276	Pass
39	1.01	0.59%	3.9159	Pass

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9.6.6 115 VAC 60 Hz, 90 V LED Load Harmonics Data

V	Freq	I (mA)	P	%THD
115	60.00	179.72	20.6300	4.51
nth Order	**mA Content**	**% Content**	**Limit <25W**	**Remarks**
1	179.46			
2	0.19	0.11%		
3	2.76	1.54%	140.2840	Pass
5	0.92	0.51%	78.3940	Pass
7	2.74	1.53%	41.2600	Pass
9	0.62	0.35%	20.6300	Pass
11	2.23	1.24%	14.4410	Pass
13	1.38	0.77%	12.2193	Pass
15	0.66	0.37%	10.5901	Pass
17	1.27	0.71%	9.3442	Pass
19	2.06	1.15%	8.3606	Pass
21	1.92	1.07%	7.5643	Pass
23	2.25	1.25%	6.9066	Pass
25	1.65	0.92%	6.3540	Pass
27	3.03	1.69%	5.8834	Pass
29	2.03	1.13%	5.4776	Pass
31	0.21	0.12%	5.1242	Pass
33	0.52	0.29%	4.8137	Pass
35	0.88	0.49%	4.5386	Pass
37	0.70	0.39%	4.2933	Pass
39	1.49	0.83%	4.0731	Pass

10 Thermal Performance

Images captured after running for more than 30 minutes at room temperature (25 °C), open frame for the conditions specified.

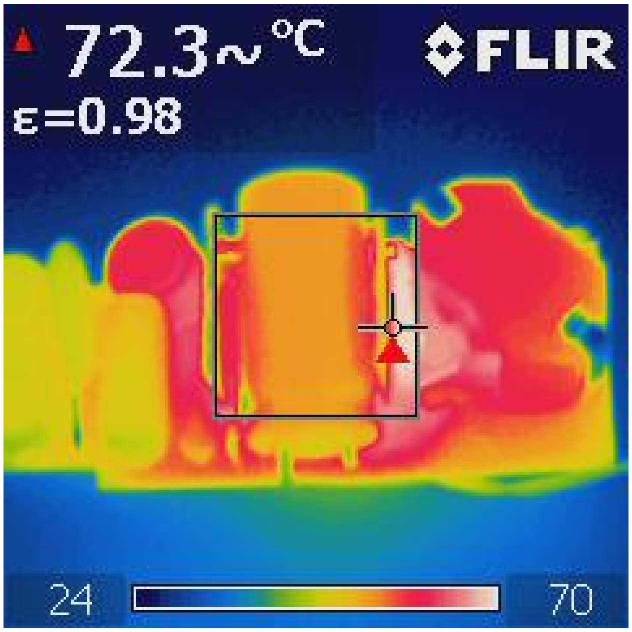

Figure 16 – Top Side.
U1- LNK460VG: 72.3 ºC.

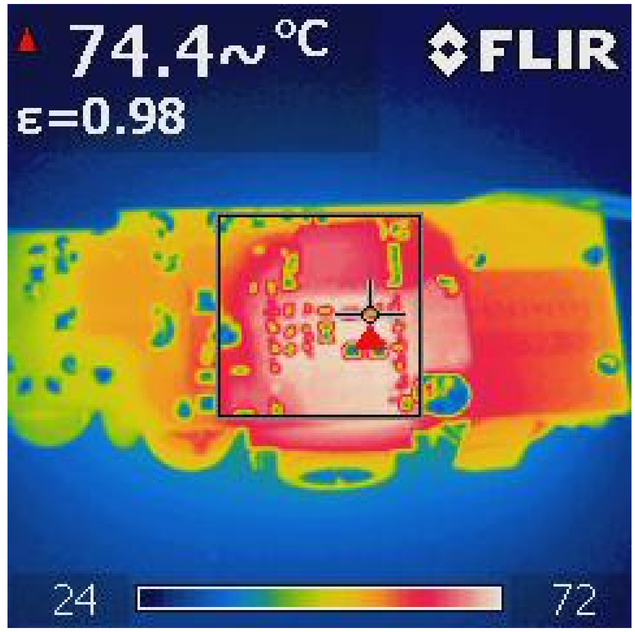

Figure 17 – Bottom Side.
R5- Current Sense Resistor: 74.4 ºC.

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11 Waveforms

11.1 Input Voltage and Input Current Waveforms

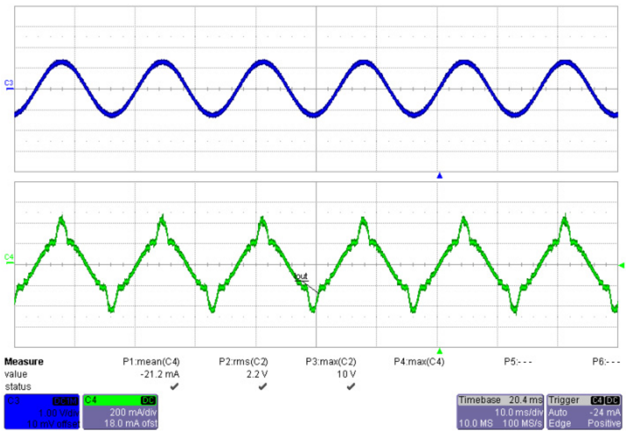

Figure 18 – 90 VAC, Full Load.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 200 mA, 10 ms / div.

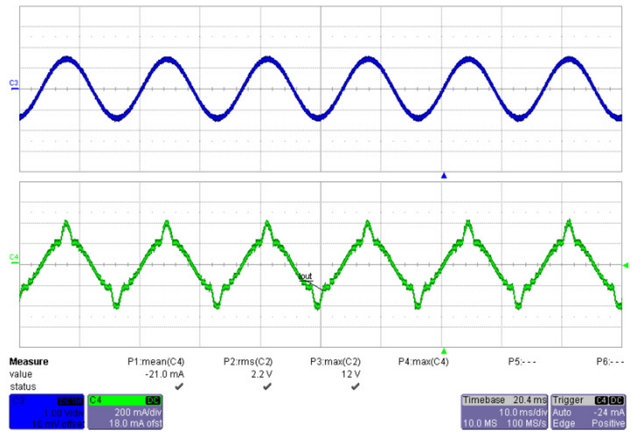

Figure 19 – 100 VAC, Full Load.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 200 mA, 10 ms / div.

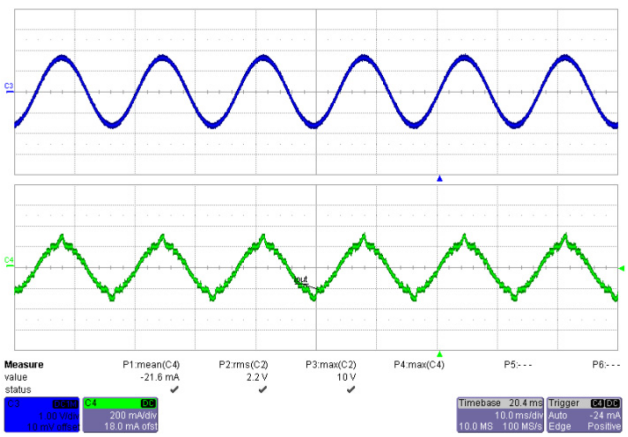

Figure 20 – 115 VAC, Full Load.
Upper: I_{IN}, 100 V / div.
Lower: V_{IN}, 200 mA, 10 ms / div.

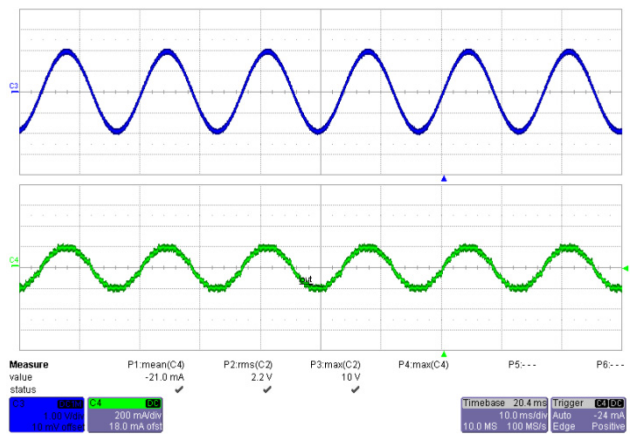

Figure 21 – 135 VAC, Full Load.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 200 mA, 10 ms / div.

11.2 Output Current and Output Voltage at Normal Operation

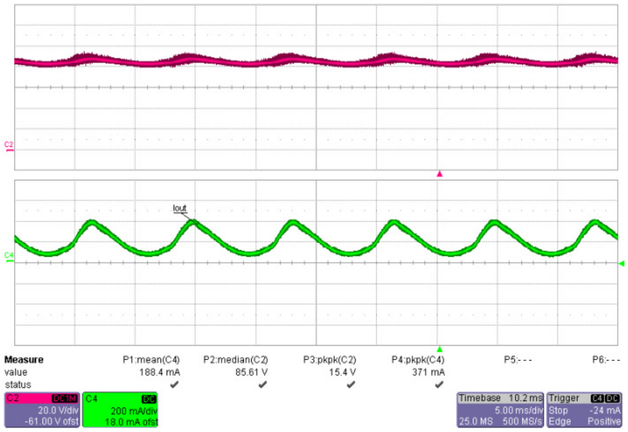

Figure 22 – 90 VAC, 60 Hz Full Load.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 5 ms / div.

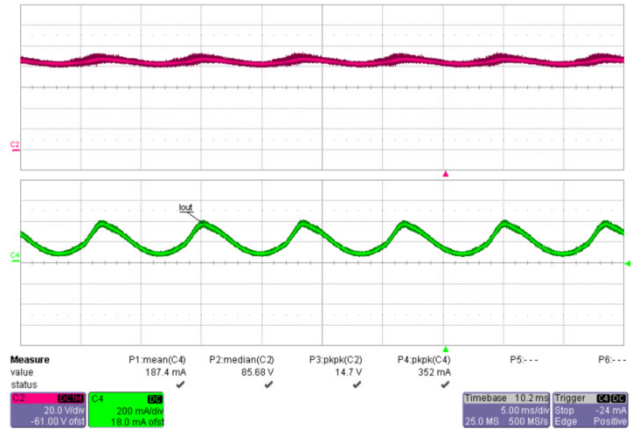

Figure 23 – 100 VAC, 60 Hz Full Load.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 5 ms / div.

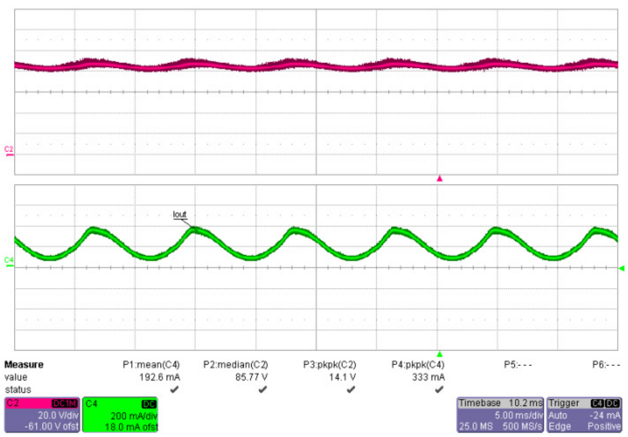

Figure 24 – 115 VAC, 60 Hz Full Load.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 5 ms / div.

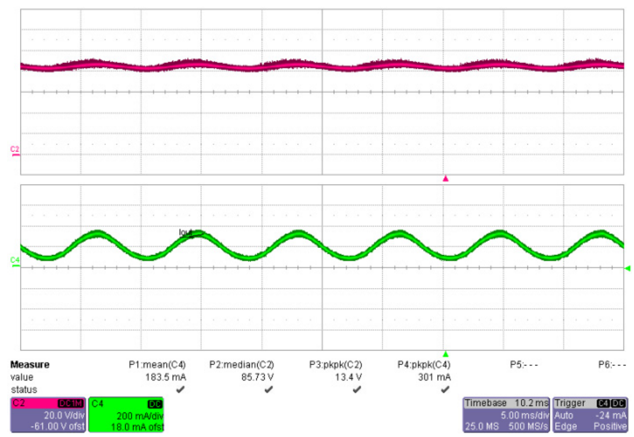

Figure 25 – 135 VAC, 60 Hz Full Load.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 5 ms / div.

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11.3 Output Current/Voltage Rise and Fall

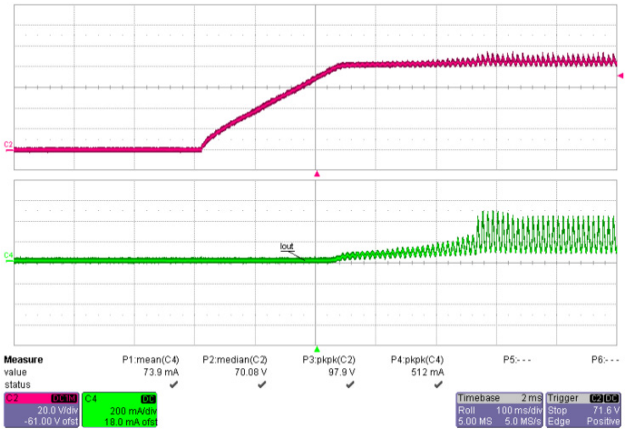

Figure 26 – 90 VAC Output Rise.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

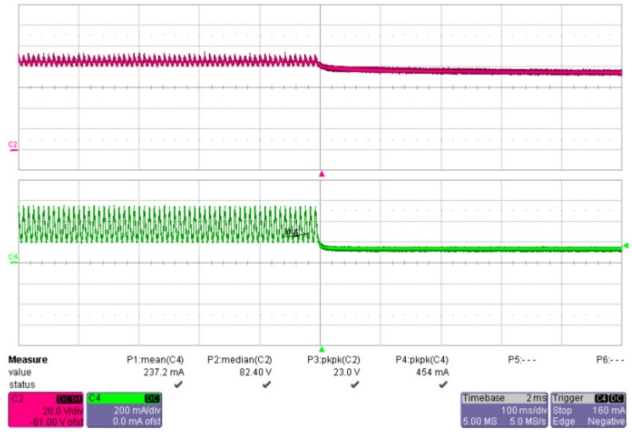

Figure 27 – 90 VAC Output Fall.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

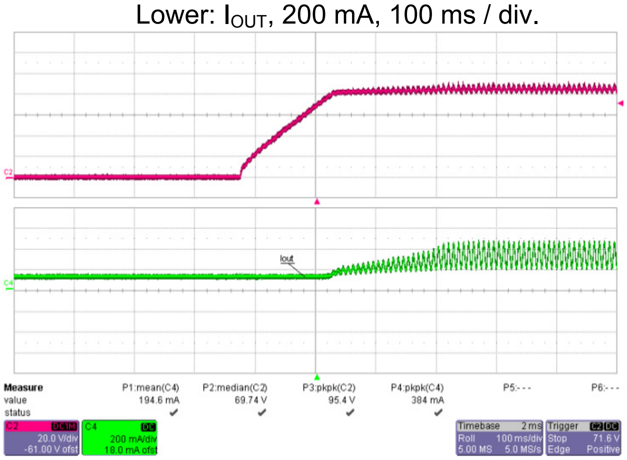

Figure 28 – 135 VAC Output Rise.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

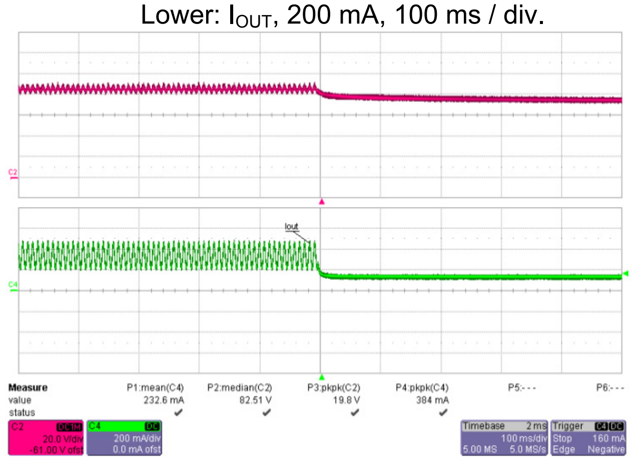

Figure 29 – 135 VAC Output Fall.
Upper: V_{OUT}, 20 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

11.4 Input Voltage and Output Current Waveform at Start-up

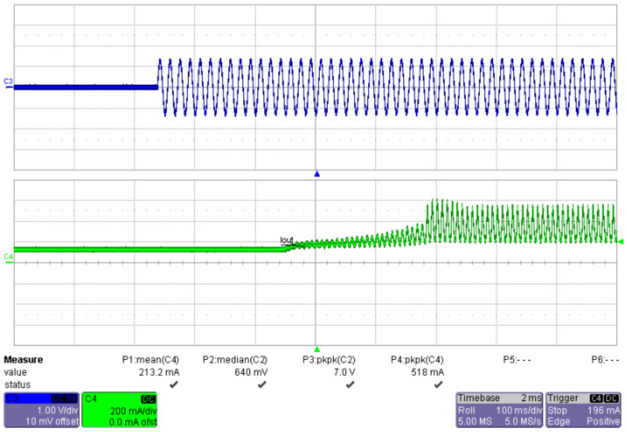

Figure 30 – 90 VAC, 60 Hz.
Upper: I_{OUT}, 0.1 A / div.
Lower: V_{IN}, 50 V, 100 ms / div.

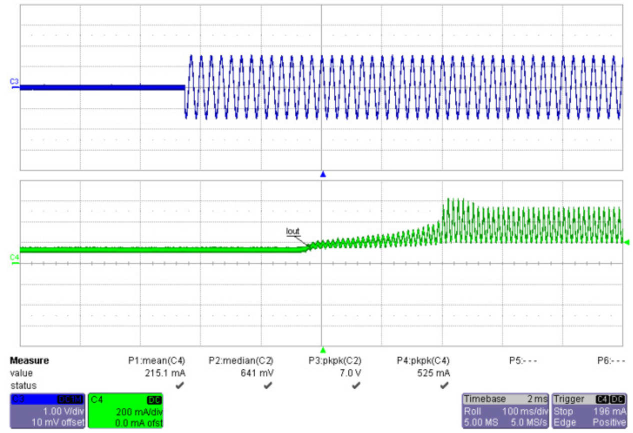

Figure 31 – 100 VAC, 60 Hz.
Upper: V_{IN}, 100 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

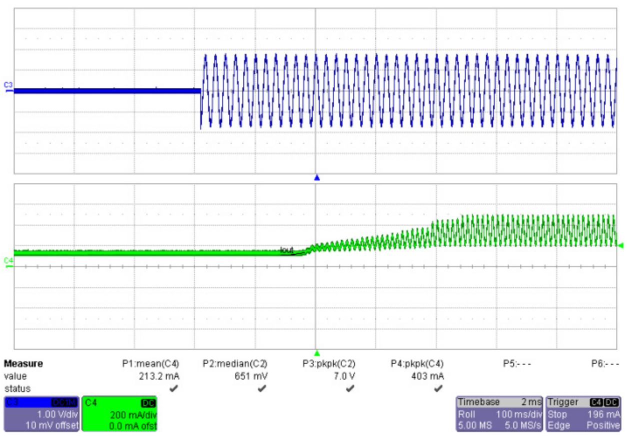

Figure 32 – 115 VAC, 60 Hz.
Upper: V_{IN}, 100 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

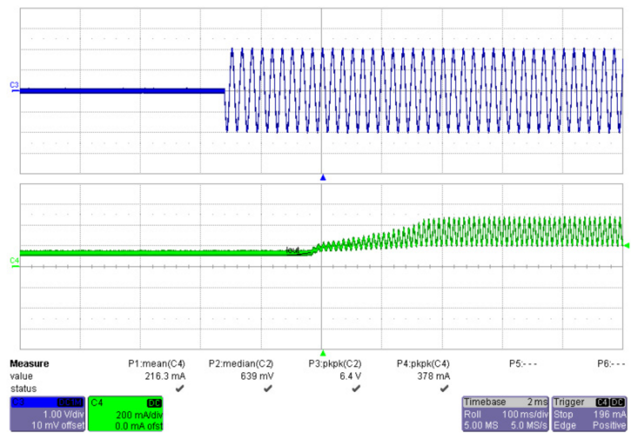

Figure 33 – 135 VAC, 60 Hz.
Upper: V_{IN}, 100 V / div.
Lower: I_{OUT}, 200 mA, 100 ms / div.

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11.5 Drain Voltage and Current at Normal Operation

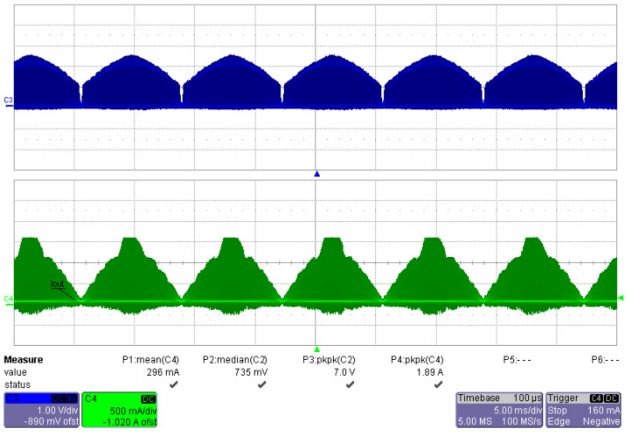

Figure 34 – 90 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 5 ms / div.

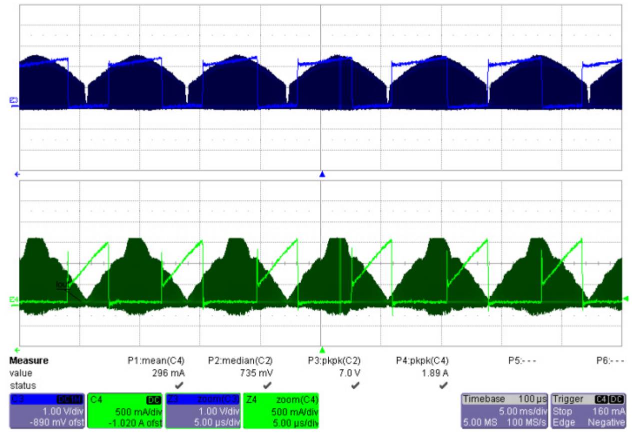

Figure 35 – 90 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 5 μs / div.

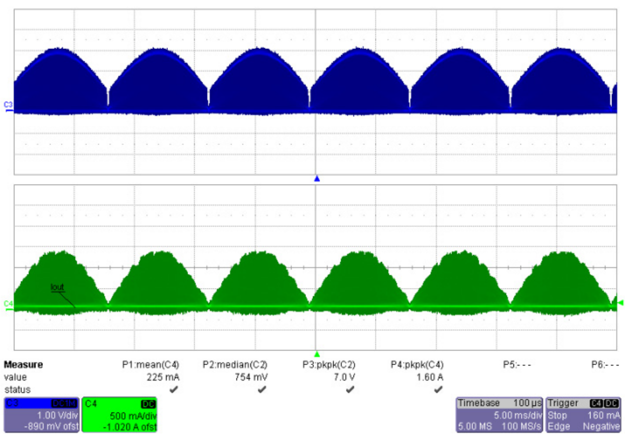

Figure 36 – 135 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 5 ms / div.

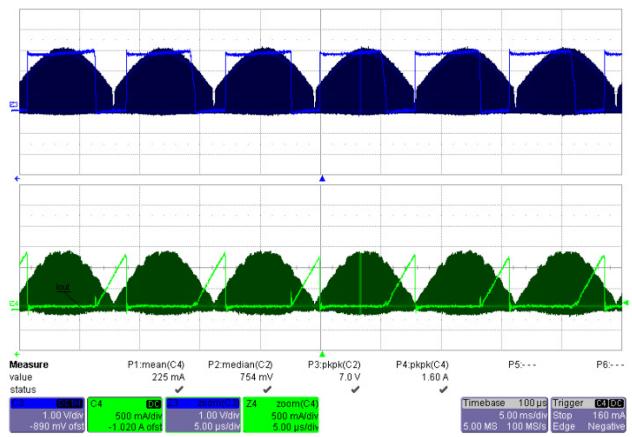

Figure 37 – 135 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: V_{DRAIN}, 500 mA, 5 μs / div.

11.6 Start-up Drain Voltage and Current

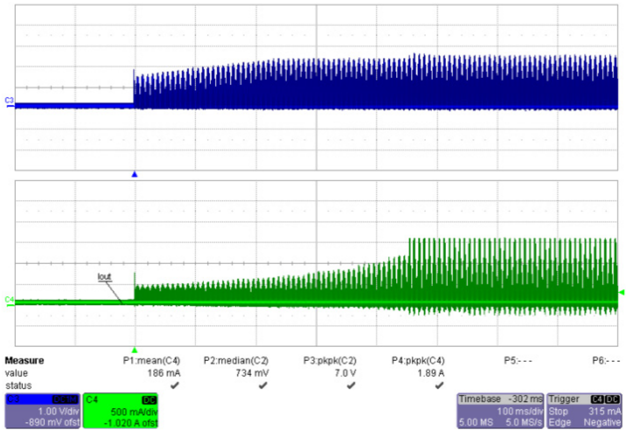

Figure 38 – 90 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 100 ms / div.

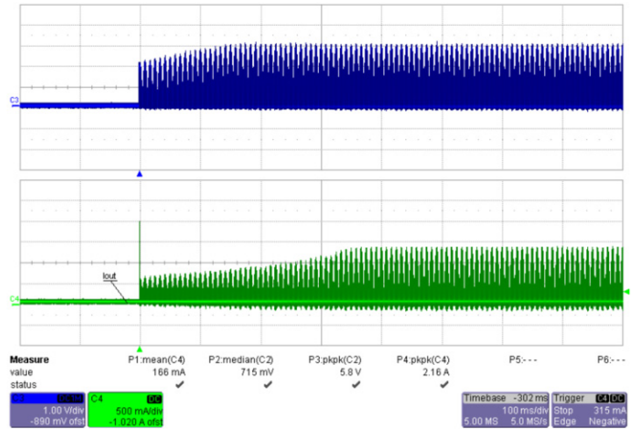

Figure 39 – 135 VAC, 60 Hz.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 100 ms / div.

11.7 Drain Current and Drain Voltage During Output Short Condition

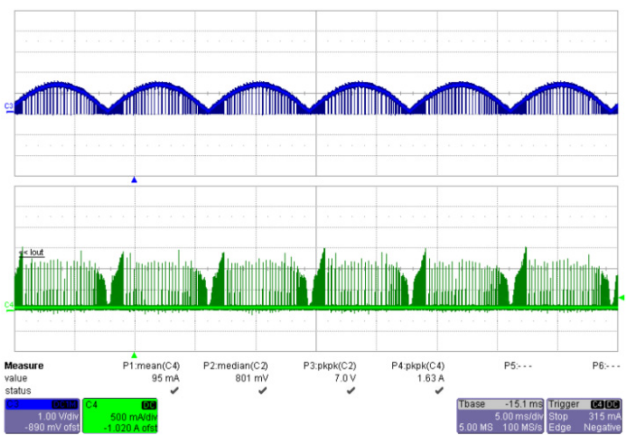

Figure 40 – 90 VAC, 60 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 5 ms / div.

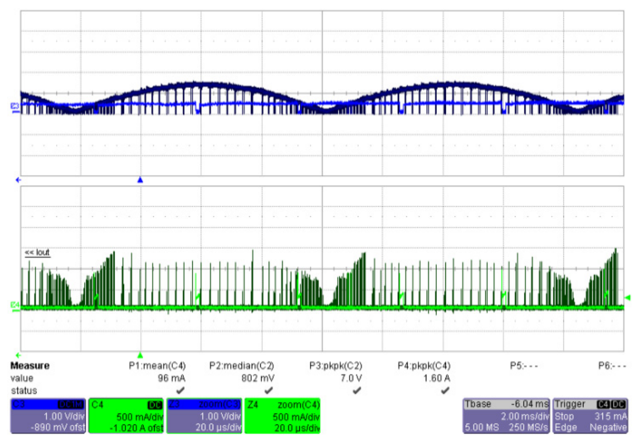

Figure 41 – 90 VAC, 60 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 20 μs / div.

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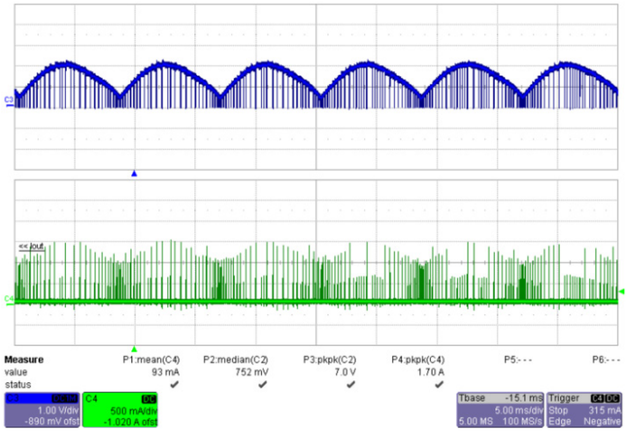

Figure 42 – 135 VAC, 60 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 5 ms / div.

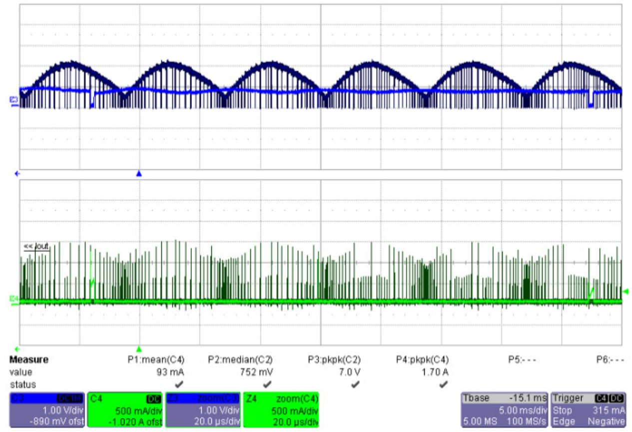

Figure 43 – 135 VAC, 60 Hz Output Short Condition.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 500 mA, 20 µs / div.

11.8 Open Load Output Voltage

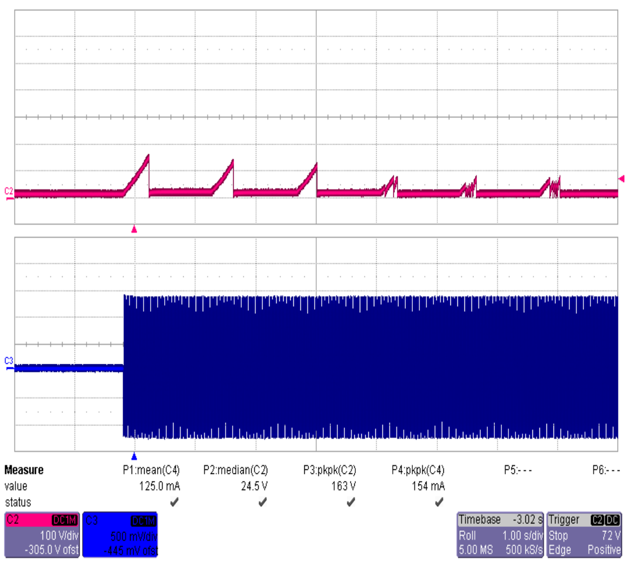

Figure 44 – 90 VAC, 60 Hz Open Load.
Upper: V_{OUT}, 100 V / div.
Lower: V_{IN}, 100 V / div., 1 s / div.

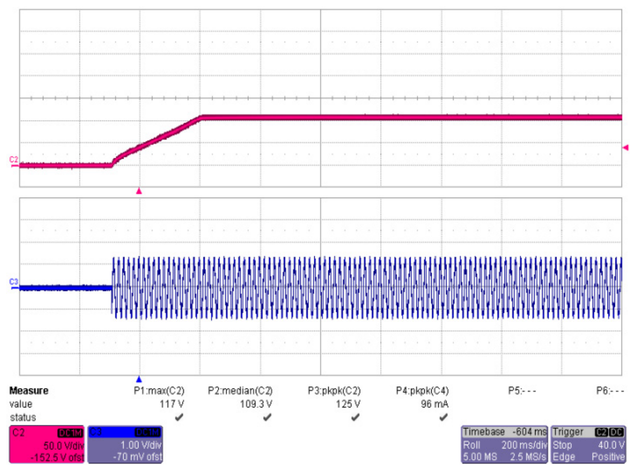

Figure 45 – Auto-Restart Overvoltage Protection Circuit in Figure 3A. 90 VAC, 60 Hz.
Upper: V_{OUT}, 50 V / div.
Lower: V_{IN}, 100 V / div., 200 ms / div.

11.9 Brown-in and Brown-out Condition

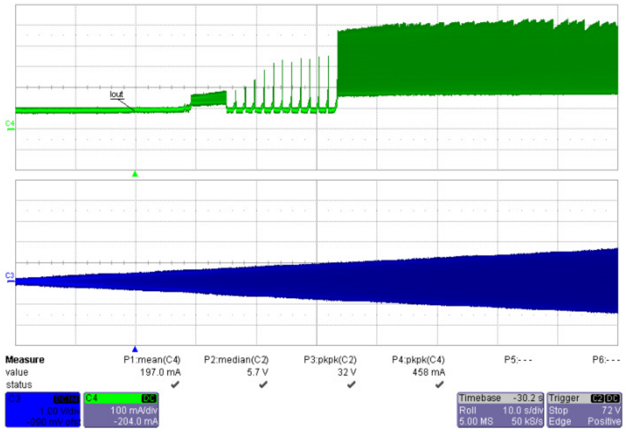

Figure 45 – 0 VAC – 115 VAC, 3 V / µs Slew Rate.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{INAC}, 50 V, 5 s / div.

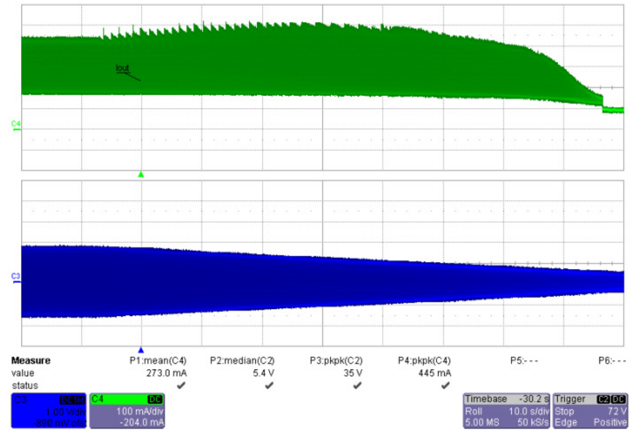

Figure 46 – 115 VAC – 0 VAC, 3 V / µs Slew Rate.
Upper: I_{OUT}, 100 mA / div.
Lower: V_{INAC}, 50 V, 5 s / div.

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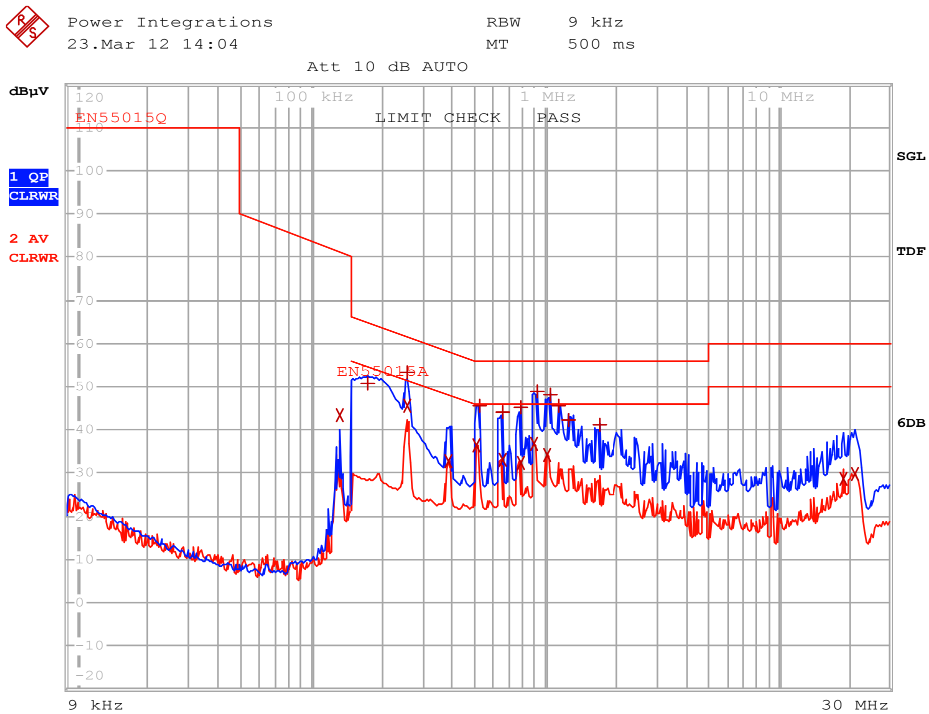
12 Conducted EMI



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	130.825395691 kHz	43.26	N gnd	
1	Quasi Peak	172.421131986 kHz	50.76	L1 gnd	-14.08
1	Quasi Peak	254.169871602 kHz	53.38	N gnd	-8.23
2	Average	256.711570318 kHz	45.48	N gnd	-6.05
2	Average	386.030632509 kHz	32.71	L1 gnd	-15.43
2	Average	510.05878768 kHz	36.38	L1 gnd	-9.61
1	Quasi Peak	525.514079005 kHz	45.54	L1 gnd	-10.45
1	Quasi Peak	654.11570866 kHz	44.26	L1 gnd	-11.73
2	Average	654.11570866 kHz	33.17	L1 gnd	-12.82
1	Quasi Peak	782.418853721 kHz	45.33	L1 gnd	-10.66
2	Average	782.418853721 kHz	32.22	L1 gnd	-13.77
2	Average	890.465639904 kHz	36.82	L1 gnd	-9.17
1	Quasi Peak	917.447639259 kHz	48.74	L1 gnd	-7.25
2	Average	1.01343296123 MHz	34.06	L1 gnd	-11.93
1	Quasi Peak	1.04414099339 MHz	48.16	L1 gnd	-7.83
1	Quasi Peak	1.13065507631 MHz	45.75	L1 gnd	-10.24
1	Quasi Peak	1.26143607964 MHz	42.39	L1 gnd	-13.61
1	Quasi Peak	1.7002252517 MHz	41.18	L1 gnd	-14.81
2	Average	18.8920426529 MHz	28.81	L1 gnd	-21.18
2	Average	21.2880265316 MHz	29.75	L1 gnd	-20.25

Figure 47 – Conducted EMI, 85 V LED Load, 115 VAC, 60 Hz, and EN55015 B Limits.

13 Line Surge

The unit was subjected to ±2500 V 100 kHz ring wave and ±1 kV differential surge at 115 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	115	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
-2500	115	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
+2500	115	L1, L2	90	100 kHz Ring Wave (200 A)	Pass
-2500	115	L1, L2	90	100 kHz Ring Wave (200 A)	Pass

Level (kV)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+1 kV	115	L1, L2	0	Surge (2 Ω)	Pass
-1 kV	115	L1, L2	0	Surge (2 Ω)	Pass
+1 kV	115	L1, L2	90	Surge (2 Ω)	Pass
-1 kV	115	L1, L2	90	Surge (2 Ω)	Pass

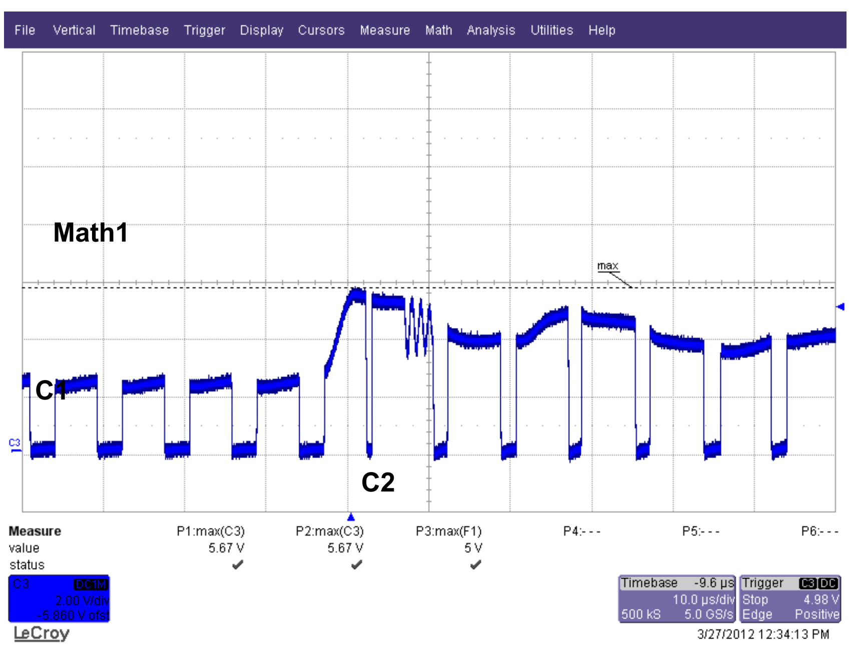


Figure 48 – 1 kV (90º Injection Phase) Differential Surge V_{DS} Waveforms. U1 V_{DS} Maximum Voltage, 567 V.

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14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
21-Jun-12	DK	1.0	Initial Release	Apps & Mktg

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@powerint.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 114, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 1601/1610, Tower 1
Kerry Everbright City
No. 218 Tianmu Road West
Shanghai, P.R.C. 200070
Phone: +86-021-6354-6323
Fax: +86-021-6354-6325
e-mail: chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

EUROPE HQ
1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
3rd Floor, Block A, Zhongtou
International Business Center, No. 1061, Xiang Mei Road, FuTian District,
ShenZhen, China, 518040
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760