



Design Example Report

Title	<i>High Efficiency (>93%), High Power Factor (>0.9), 18 W Output Non-Isolated Buck LED Driver Using LinkSwitch™-PL LNK460VG</i>
Specification	195 VAC – 265 VAC Input; 78 V _{TYP} , 230 mA Output
Application	A19 LED Lamp
Author	Application Engineering Department
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Revision	1.0

Summary and Features

- Single-stage power factor correction combined with constant current (CC) output
- Low cost, low component count, small size and single-sided PCB
- Highly energy efficient, >93% at 230 VAC input for 78 V LED Load
- Integrated protection and reliability features
 - Single shot no-load protection / output short-circuit protected with auto-recovery
 - Auto-recovering thermal shutdown with large hysteresis protects both components and PCB
 - No damage during brown-out conditions
- PF >0.9 at 230 VAC
- % ATHD <20% at 230 VAC; 78 V LED
- Meets IEC ring wave, differential line surge and EN55015 conducted EMI

PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

The document describes a non-isolated, high efficiency, high power factor (PF) LED driver designed to drive a nominal LED string voltage of 78 V at 230 mA from an input voltage range of 195 VAC to 265 VAC (47 Hz – 63 Hz). The LED driver utilizes the LNK460VG from the LinkSwitch-PL family of ICs.

The topology used is a single-stage non-isolated buck that meets the stringent space and efficiency requirements for this design. LinkSwitch-PL based designs provide high power factor (>0.9) meeting international requirements.

This document contains the LED driver specification, schematic, PCB details, bill of materials, transformer documentation and typical performance characteristics.

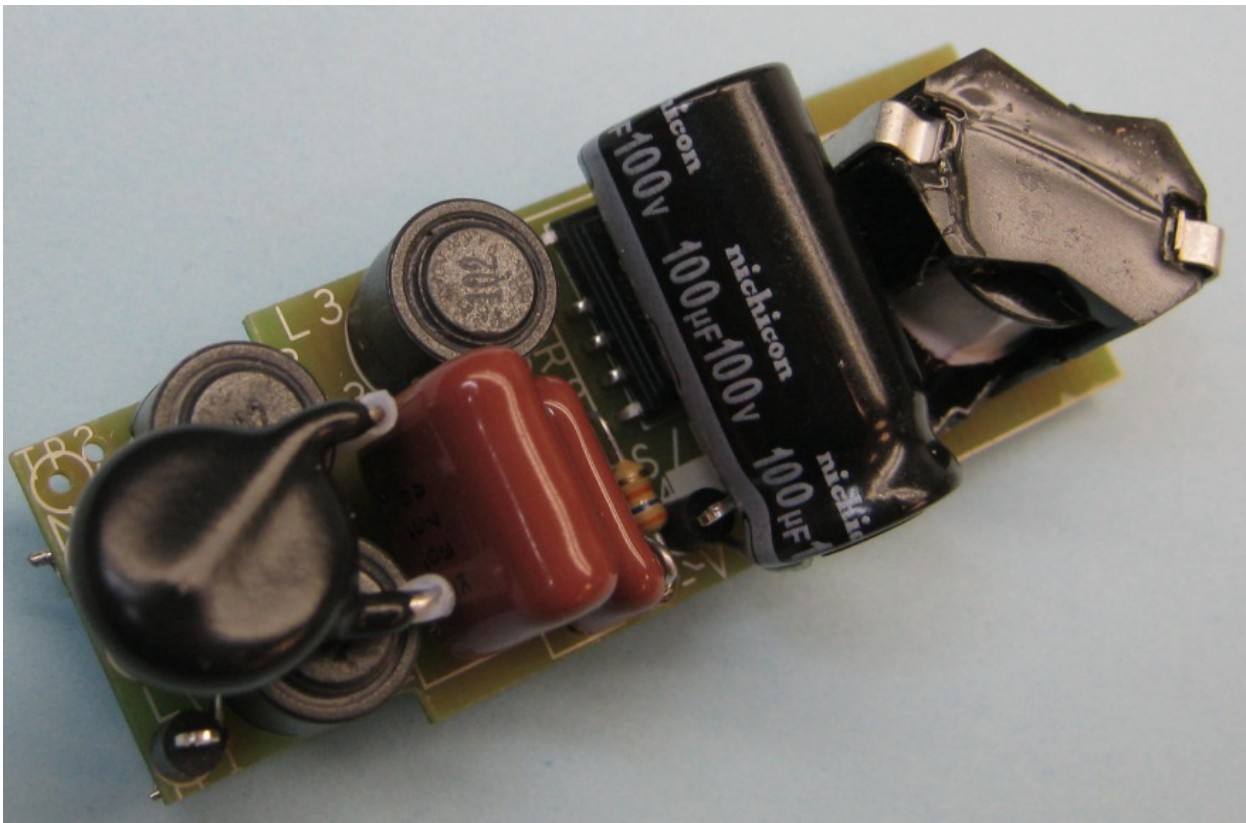


Figure 1 – Populated Circuit Board.



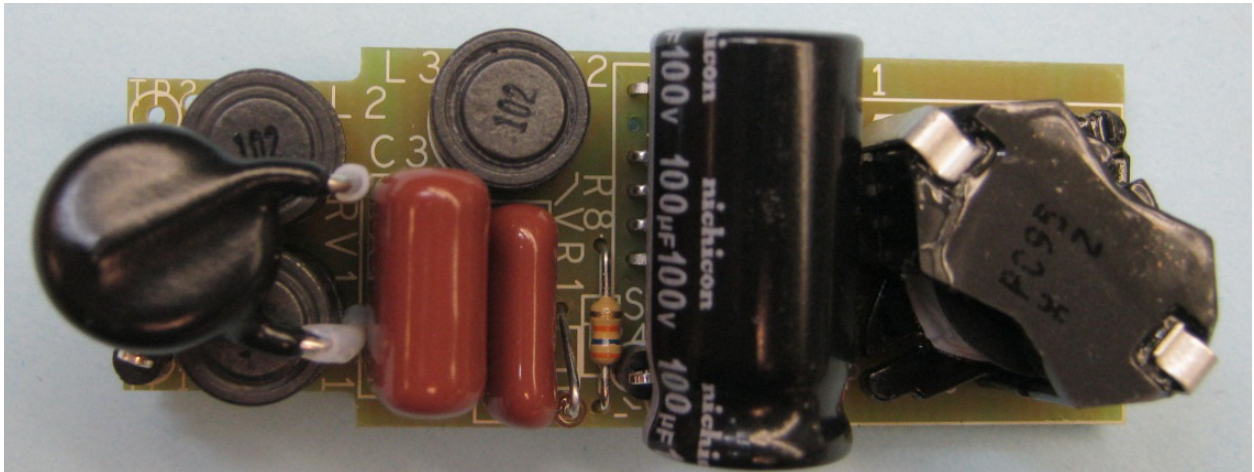


Figure 2 – Populated Circuit Board, Top View.

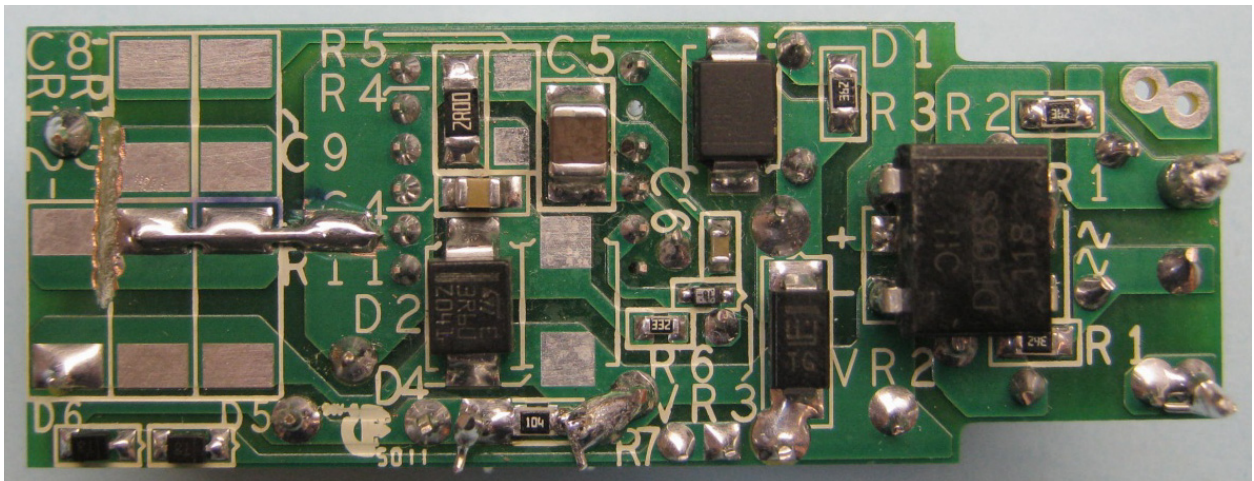


Figure 3 – Populated Circuit Board, Bottom View.

Note: This design utilizes the DER-305 PCB and is modified to maximize LNK460VG heat sink area.



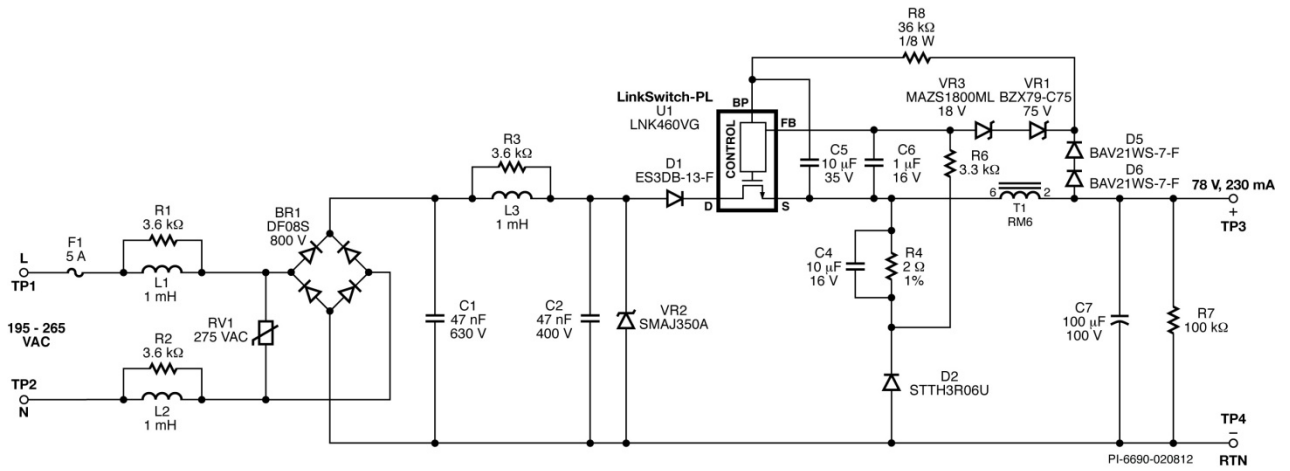
Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input Voltage Frequency	V_{IN} f_{LINE}	195	230 50	265	VAC Hz	2 Wire – no P.E.
Output Output Voltage Output Current Total Output Power Continuous Output Power	V_{OUT} I_{OUT} P_{OUT}	75	78 230 18	81	V mA W	$V_{OUT} = 78\text{ V}$, $V_{IN} = 230\text{ VAC}$, 25 °C
Efficiency Full Load	η	93			%	Measured at P_{OUT} 25 °C
Environmental Conducted EMI Safety Ring Wave (100 kHz) Differential Mode (L1-L2) Differential Surge						CISPR 15B / EN55015B Non-Isolated 2.5 kV 500 V
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class D (C)				Class C specifies Class D Limits when $P_{IN} < 25\text{ W}$
Ambient Temperature	T_{AMB}		50		°C	Free convection, sea level



2 Schematic



3 Circuit Description

The LinkSwitch-PL (U1) is a highly integrated primary-side controller intended for use in LED driver applications. The LinkSwitch-PL provides high power factor while regulating the output current across a range of input (195 VAC to 265 VAC) in a single conversion stage. The design also supports the output voltage variations typically encountered in LED driver applications. All of the control circuitry responsible for these functions plus the high-voltage power MOSFET is incorporated into the IC.

3.1 Input EMI Filtering

Inductors L1-L3 and C1-C2 filter the switching current presented by the buck converter to the line. Resistor R1, R2 and R3 across L1, L2 and L3 damp any resonances between the input inductors, capacitors and the AC line impedance which create peaks in the conducted EMI spectrum.

MOV RV1 provides a clamp to limit the maximum voltage during differential line surge events. Zener diode VR2 is added to increase immunity to differential line surge, clamping at a lower voltage than the MOV. Bridge rectifier BR1 rectifies the AC line voltage with capacitor C2 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C1 and C2) is necessary to maintain a power factor greater than 0.9.

3.2 Power Circuit

The circuit is configured as a buck converter with the SOURCE (S) pin of U1 connected to the cathode side of the freewheeling diode D2 and DRAIN (D) pin connected to the positive side of the DC rectified input through D1. Diode D1 is used to prevent reverse current to flow through U1. An RM6 core size was selected to optimize the inductor T1 for highest system efficiency. Capacitor C7 filters the switching frequency.

Capacitor C5 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C5 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN pin. Once charged U1 starts switching at which point the operating supply current is provided from the T1 inductor via R8, D5 and D6

Rectifier diodes D5 and D6 were selected to be low capacitance diodes to minimize the effect of the OVP circuit (D5, D6, VR1 and VR3) on the output regulation. A single ultrafast diode (e.g. UF4005) may be substituted for lower cost resulting in a ~10 mA increase in load regulation.

3.3 Output Feedback

Resistor R4 is used to sense the diode current of the buck converter. The value was adjusted to center the output current at 230 mA at nominal input voltage. Capacitor C4 is used to filter the high frequency component of the diode current which helps improve overall efficiency by reducing the RMS current through R4. Resistor R6 and C6 provide



additional filtering to lower the ripple of the voltage feed to the FEEDBACK (FB) pin of U1 for improved regulation.

3.4 Open Load Protection

The LED driver is protected in the event of accidental open load operation by monitoring the voltage across the output inductor during energy decay (MOSFET off time). Zener diodes VR1 and VR3 set the OVP threshold which forces U1 to enter cycle-skipping mode.

During a disconnected load condition, the output capacitor can be charged to a voltage that exceeds the threshold of VR1 and VR3 because of the leakage current that flows to the output capacitor even when U1 is off. Resistor R7 is used to limit the maximum output voltage by partially discharging the output when the load is disconnected. This reduces efficiency during normal operation but also ensures the LEDs extinguishing completely when the AC is removed. Zener diodes VR1 and VR3 may be replaced with a single part where a suitable standard value exists.

For designs which require more precise OVP protection for the output capacitor, a Zener diode with Zener voltage greater than or equal to VR1 and VR3 can be added across the output.



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4 PCB Layout

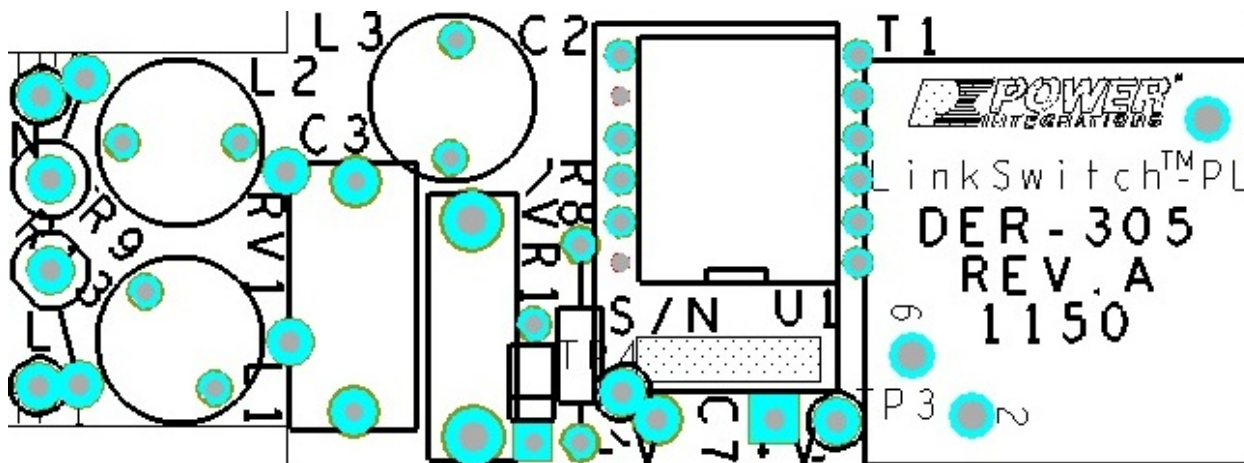


Figure 5 – Top Side. Dimension 53.5 mm x 19.6 mm.

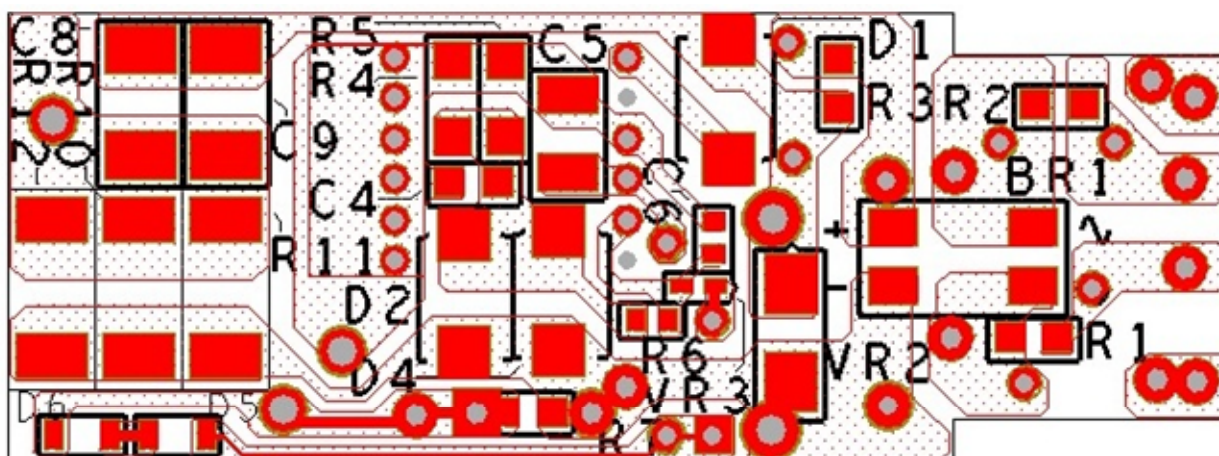


Figure 6 – Bottom Side. Dimension 53.5 mm x 19.6 mm.

Note: This design uses the same basic layout as the DER-305. Please refer to DER-305 Rev. A for the PCB CAD file.



5 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 1 A, Bridge Rectifier, SMD, DFS	DF08S	Diodes, Inc.
2	1	C1	47 nF, 630 V, Film	ECQ-E6473KF	Panasonic
3	1	C2	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
4	1	C4	10 μ F, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
5	1	C5	10 μ F, 35 V, Ceramic, Y5V, 1210	GMK325F106ZH-T	Taiyo Yuden
6	1	C6	1 μ F 16 V, Ceramic, X7R, 0603	C1608X7R1C105M	TDK
7	1	C7	100 μ F, 100 V, Electrolytic, Gen. Purpose, (10 x 20)	UVZ2A101MPD	Nichicon
8	1	D1	200 V, 3 A, DIODE SUPER FAST SMD, SMB	ES3DB-13-F	Diodes, Inc.
9	1	D2	600 V, 3 A, Fast Recovery, 35 ns, SMB Case	STTH3R06U	ST Micro
10	2	D5 D6	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
11	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	LittleFuse
12	3	L1 L2 L3	1 mH, 0.23 A, Ferrite Core	CTSCH875DF-102K	CTParts
13	3	R1 R2 R3	3.6 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ362V	Panasonic
14	1	R4	2.00 Ω , 1%, 1/4 W, Thick Film, 1206	MCR18EZHFL2R00	Rohm Semi
15	1	R6	3.3 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
16	1	R7	100 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
17	1	R8	36 k Ω , 5%, 1/8 W, Carbon Film	CFR-12JB-36K	Yageo
18	1	RV1	275 V, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
19	1	T1	Bobbin, RM6, Vertical, 6 pins	B65808-N1006-D1	Epcos
20	1	U1	LinkSwitch-PL, eDIP-12P	LNK460VG	Power Integrations
21	1	VR1	75 V, 500 mW, 5%, DO-35	BZX79-C75	Taiwan Semi
22	1	VR2	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	LittleFuse
23	1	VR3	18 V, 5%, 150 mW, SSMINI-2	MAZS1800ML	Panasonic



6 Inductor (T1) Specification

6.1 Electrical Diagram

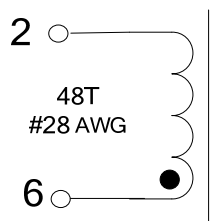


Figure 7 – Inductor Electrical Diagram.

6.2 Electrical Specifications

Primary Inductance	Pins 2-6, all other windings open, measured at 100 kHz, 0.4 V _{RMS}	360 μH ±7%
Resonant Frequency	Pins 2-6, all other windings open	2 MHz (Min.)

6.3 Materials

Item	Description
[1]	Core: TDKPC95RM06-Z.
[2]	Bobbin: B-RM6-V-6pins-(3/3) with mounting clip, CLIP-RM6.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 6.4 mm wide.
[4]	Wire: Magnet, #28 AWG, solderable double coated.

6.4 Inductor Build Diagram

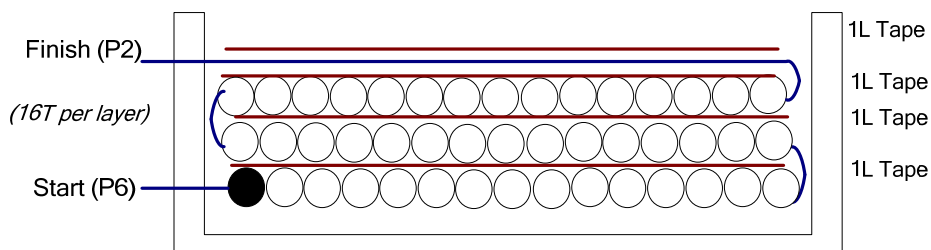


Figure 8 – Inductor Build Diagram.

6.5 Inductor Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WDG 1	Starting at pin 6, wind 48 turns of wire item [4] in three layers. Apply one layer of tape item [3] per layer. Finish at pin 2.
Final Assembly	Grind core to get 0.36 mH inductance.



7 Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent the load range of 75 V ~ 81 V output voltage. Refer to the table on Section 7.6 for the complete set of test data values.

7.1 Efficiency

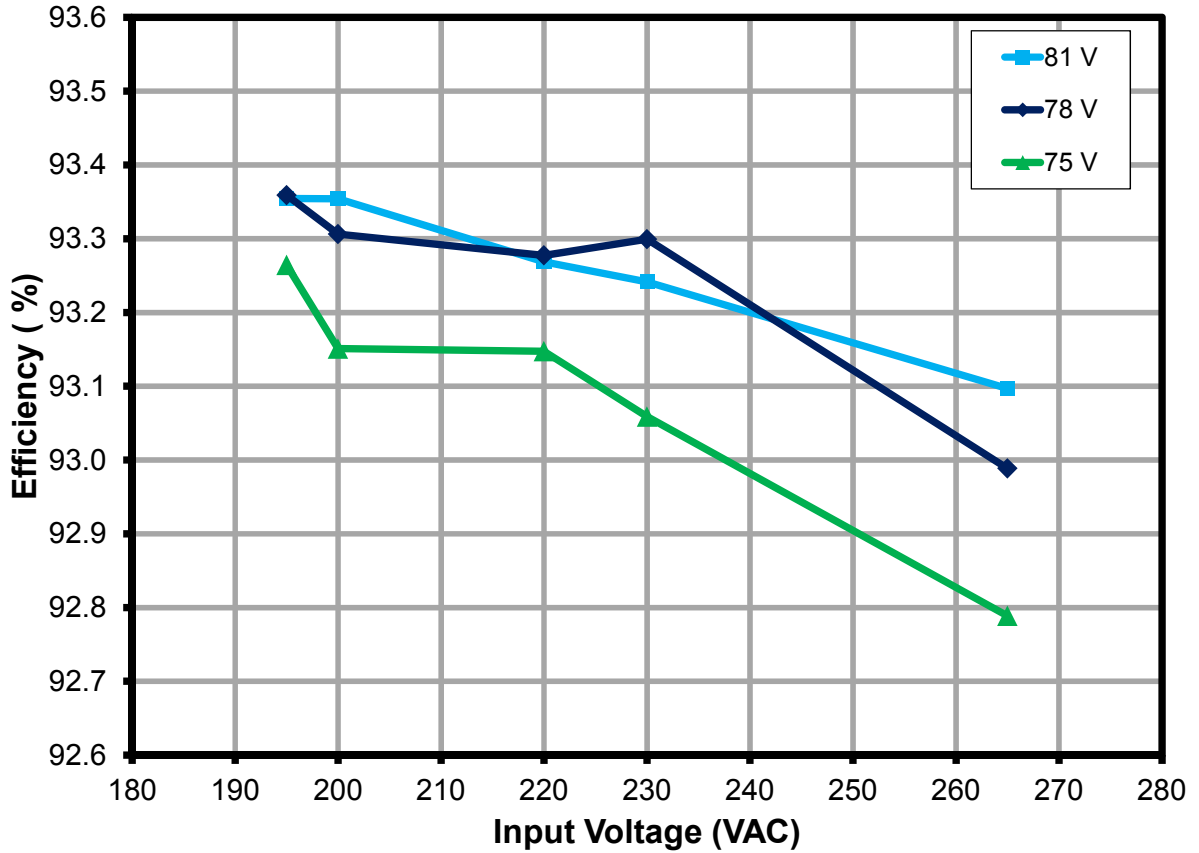


Figure 9 – Efficiency vs. Line and Load.



7.2 Line and Load Regulation

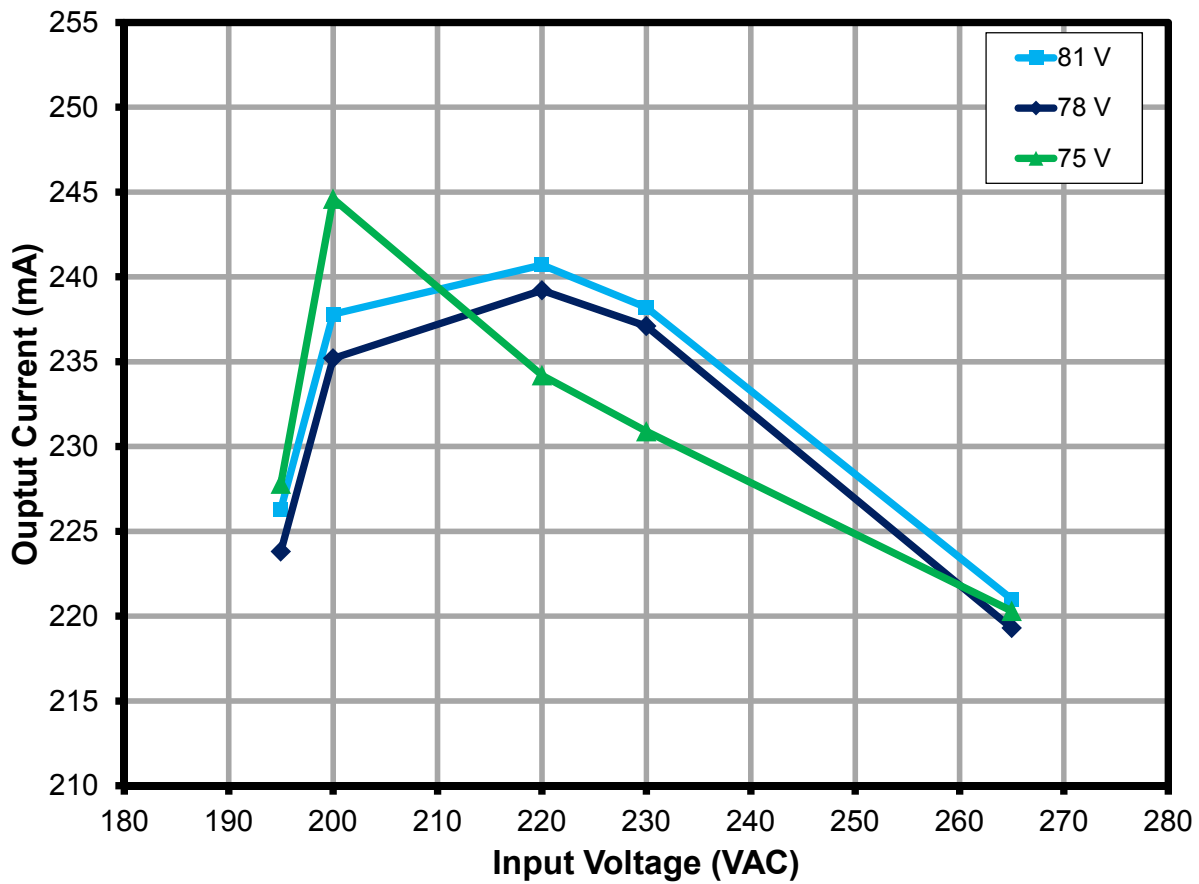


Figure 10 – Regulation vs. Line and Load.



7.3 Power Factor

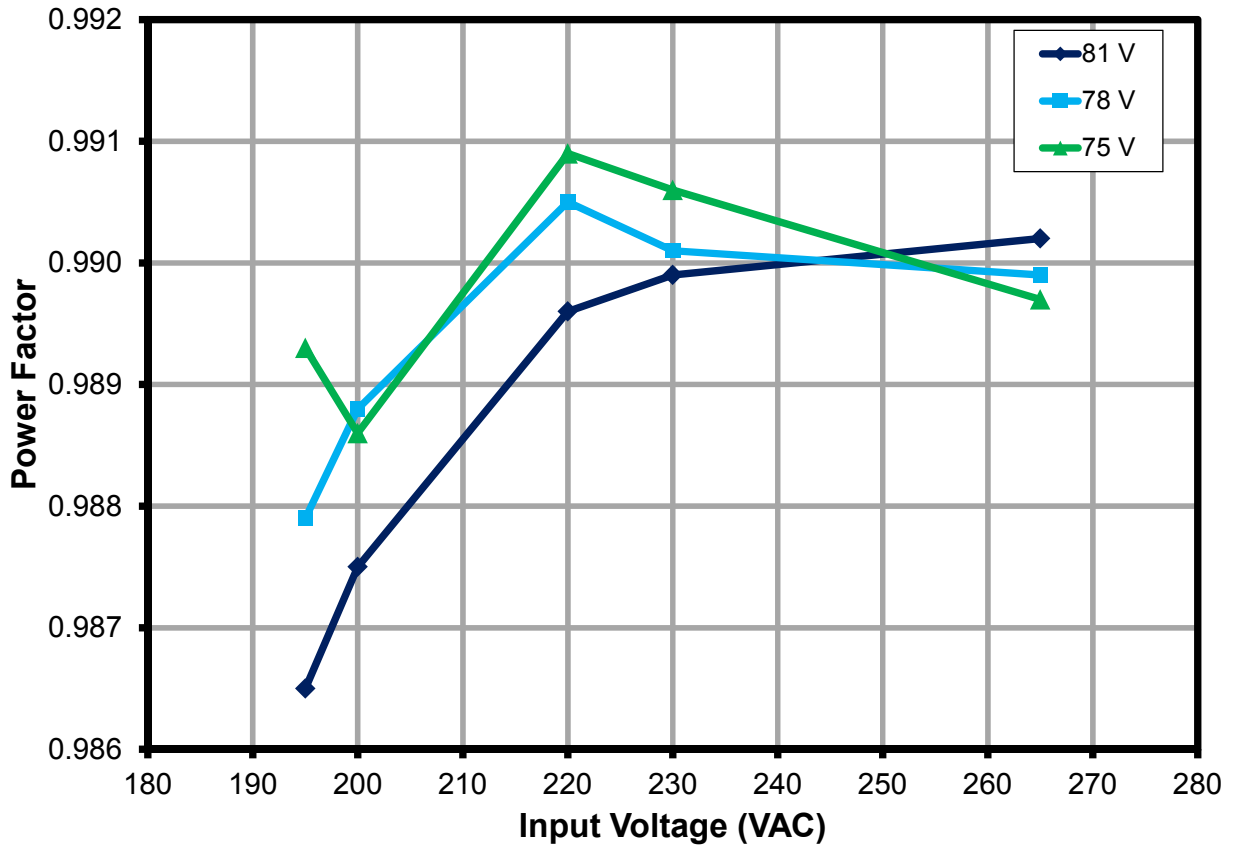


Figure 11 – Power Factor vs. Line and Load.



7.4 A-THD

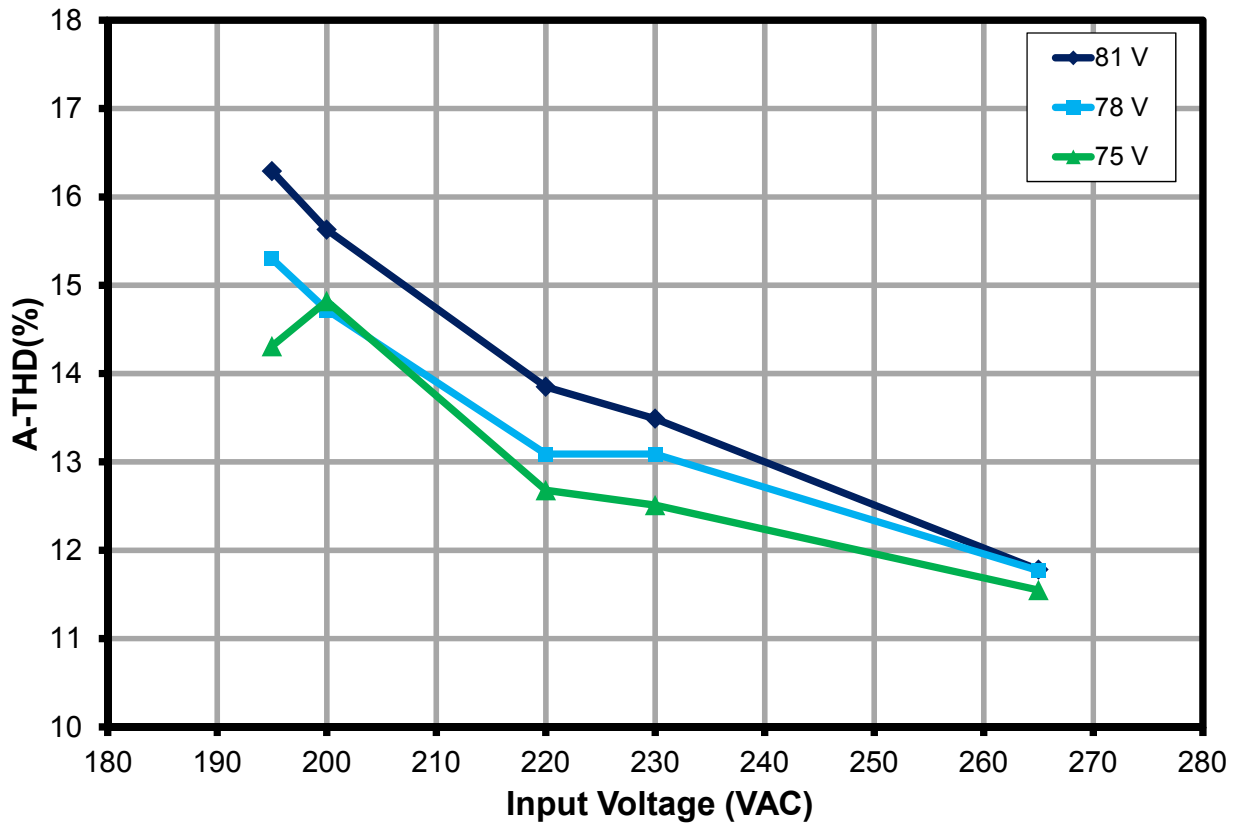


Figure 12 – A-THD vs. Line and Load.



7.5 Harmonics Content

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment¹. Therefore the limits shown in the charts below are Class D limits which must not be exceeded to meet Class C compliance.

7.5.1 75 V Output

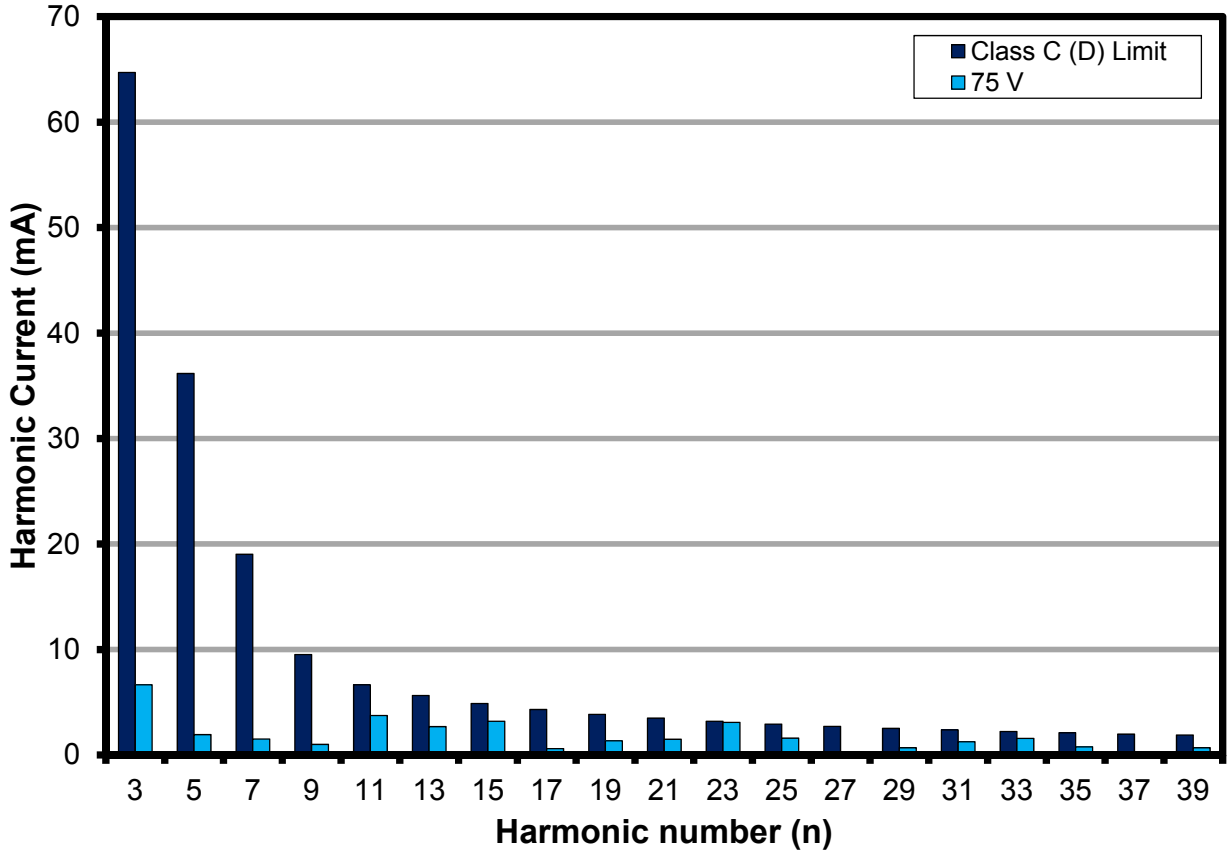


Figure 13 – 75 V Output. Input Current Harmonics at 230 VAC, 50 Hz.

¹ IEC6000-3-2 Section 7.3, table 2, column 2.

7.5.2 78 V Output

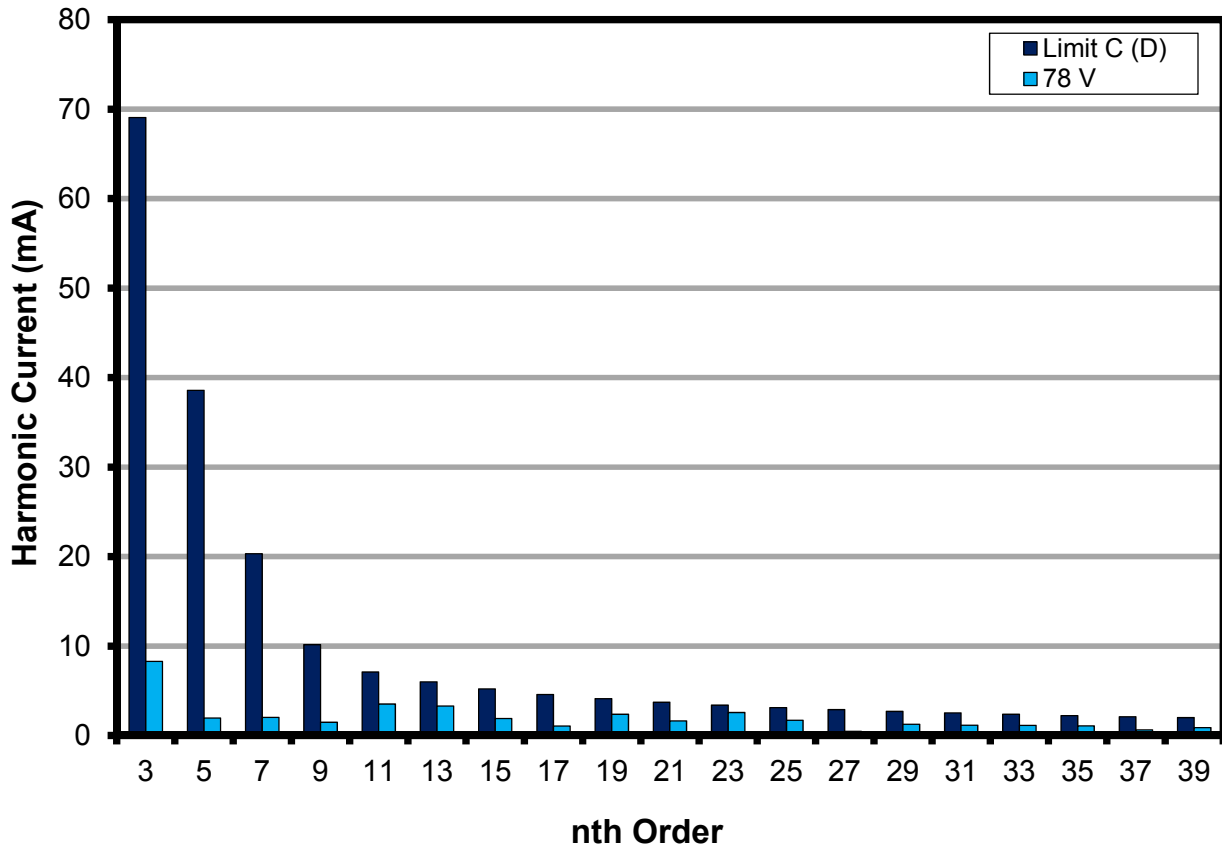


Figure 14 – 78 V Output. Input Current Harmonics at 230 VAC, 50 Hz.



7.5.3 81 V Output

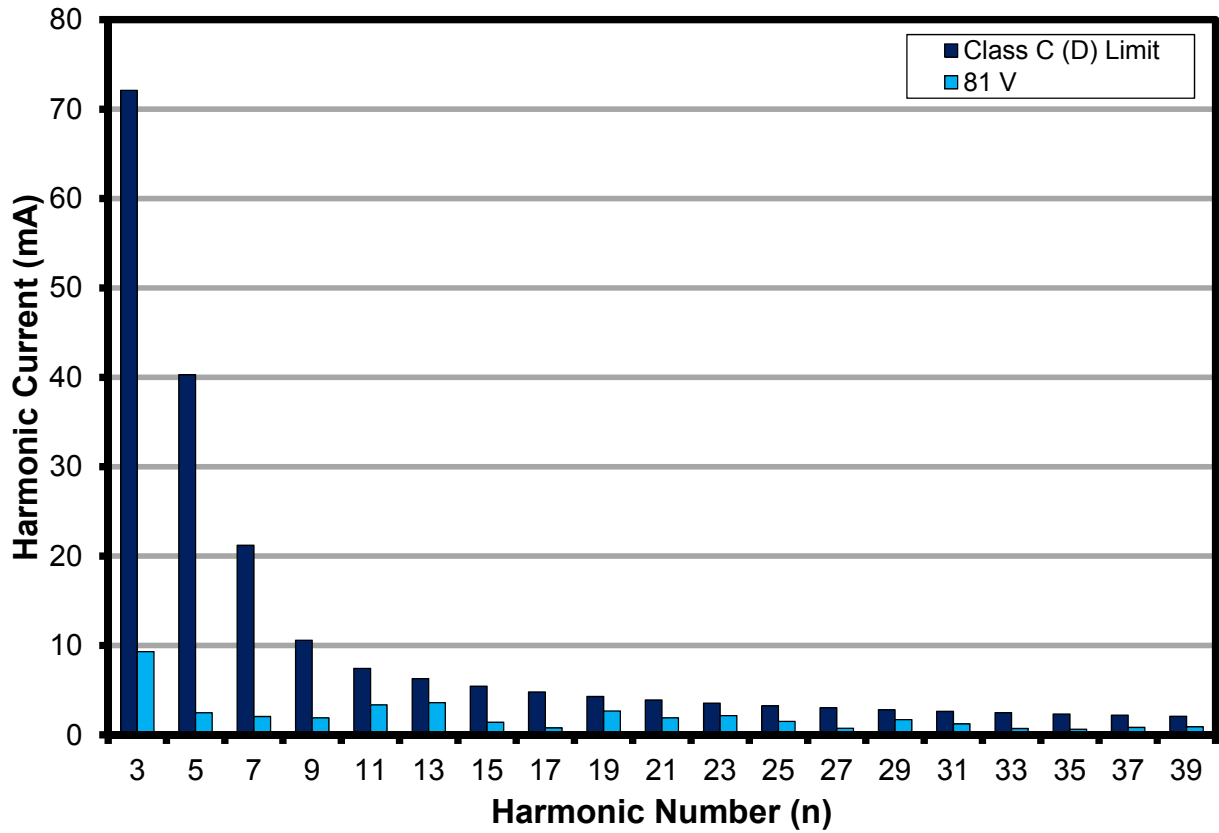


Figure 15 – 81 V Output. Input Current Harmonics at 230 VAC, 50 Hz.



7.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient, and 50 Hz line frequency.

7.6.1 Test Data, 75 V Output

Input		Input Measurement					Load Measurement			Calculation		
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
195	50	195.02	97.08	18.721	0.989	14.31	75.7000	227.800	17.460	17.24	93.26	1.26
200	50	200.00	102.19	20.193	0.988	14.82	75.8000	244.600	18.810	18.54	93.15	1.38
220	50	220.00	88.54	19.292	0.990	12.68	75.7000	234.200	17.970	17.73	93.15	1.32
230	50	230.03	83.56	19.031	0.990	12.51	75.7000	230.900	17.710	17.48	93.06	1.32
265	50	265.05	69.17	18.138	0.989	11.55	75.5000	220.300	16.830	16.63	92.79	1.31

7.6.2 Test Data, 78 V Output

Input		Input Measurement					Load Measurement			Calculation		
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
195	50	195.02	99.24	19.109	0.987	15.3	78.7000	223.800	17.840	17.61	93.36	1.27
200	50	200.00	101.89	20.138	0.988	14.72	78.8000	235.200	18.790	18.53	93.31	1.35
220	50	220.00	94.12	20.498	0.990	13.09	78.9000	239.200	19.120	18.87	93.28	1.38
230	50	230.03	89.22	20.311	0.990	13.09	78.9000	237.100	18.950	18.71	93.30	1.36
265	50	265.05	71.52	18.755	0.989	11.77	78.6000	219.300	17.440	17.24	92.99	1.32

7.6.3 Test Data, 81 V Output

Input		Input Measurement					Load Measurement			Calculation		
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	P _{CAL} (W)	Efficiency (%)	Loss (W)
195	50	195.02	104.40	20.074	0.986	16.29	81.7000	226.300	18.740	18.49	93.35	1.33
200	50	200.00	107.17	21.156	0.987	15.63	82.0000	237.800	19.750	19.50	93.35	1.41
220	50	220.00	98.44	21.422	0.989	13.85	81.9000	240.700	19.980	19.71	93.27	1.44
230	50	230.03	93.16	21.203	0.989	13.49	82.0000	238.200	19.770	19.53	93.24	1.43
265	50	265.05	74.77	19.614	0.990	11.78	81.7000	221.000	18.260	18.06	93.10	1.35



7.6.4 230 VAC 50 Hz, 75 V Output, Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	83.56	19.0310	0.9901	12.51
nth Order	mA Content	% Content	Limit <25 W	Remarks	
1	82.85				
2	0.13	0.16%			
3	6.66	8.04%	64.7054	Pass	
5	1.94	2.34%	36.1589	Pass	
7	1.50	1.81%	19.0310	Pass	
9	1.00	1.21%	9.5155	Pass	
11	3.75	4.53%	6.6609	Pass	
13	2.69	3.25%	5.6361	Pass	
15	3.20	3.86%	4.8846	Pass	
17	0.61	0.74%	4.3100	Pass	
19	1.35	1.63%	3.8563	Pass	
21	1.49	1.80%	3.4890	Pass	
23	3.08	3.72%	3.1856	Pass	
25	1.60	1.93%	2.9308	Pass	
27	0.14	0.17%	2.7137	Pass	
29	0.69	0.83%	2.5265	Pass	
31	1.26	1.52%	2.3635	Pass	
33	1.57	1.89%	2.2203	Pass	
35	0.77	0.93%	2.0934	Pass	
37	0.24	0.29%	1.9803	Pass	
39	0.68	0.82%	1.8787	Pass	



7.6.5 230 VAC 50 Hz, 78 V Output, Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	89.22	20.3110	0.9896	13.09
nth Order	mA Content	% Content	Limit <25 W	Remarks	
1	88.45				
2	0.09	0.10%			
3	8.30	9.38%	69.0574	Pass	
5	1.96	2.22%	38.5909	Pass	
7	2.02	2.28%	20.3110	Pass	
9	1.48	1.67%	10.1555	Pass	
11	3.51	3.97%	7.1089	Pass	
13	3.30	3.73%	6.0152	Pass	
15	1.91	2.16%	5.2132	Pass	
17	1.05	1.19%	4.5998	Pass	
19	2.37	2.68%	4.1157	Pass	
21	1.63	1.84%	3.7237	Pass	
23	2.57	2.91%	3.3999	Pass	
25	1.71	1.93%	3.1279	Pass	
27	0.47	0.53%	2.8962	Pass	
29	1.26	1.42%	2.6965	Pass	
31	1.17	1.32%	2.5225	Pass	
33	1.14	1.29%	2.3696	Pass	
35	1.08	1.22%	2.2342	Pass	
37	0.64	0.72%	2.1134	Pass	
39	0.89	1.01%	2.0051	Pass	



7.6.6 230 VAC 50 Hz, 81 V Output, Harmonics Data

V	Freq	I (mA)	P	PF	%THD
230	50.00	93.16	21.2030	0.9894	13.49
nth Order	mA Content	% Content	Limit <25 W	Remarks	
1	92.29				
2	0.10	0.11%			
3	9.32	10.10%	72.0902	Pass	
5	2.48	2.69%	40.2857	Pass	
7	2.06	2.23%	21.2030	Pass	
9	1.92	2.08%	10.6015	Pass	
11	3.34	3.62%	7.4211	Pass	
13	3.60	3.90%	6.2794	Pass	
15	1.41	1.53%	5.4421	Pass	
17	0.78	0.85%	4.8019	Pass	
19	2.68	2.90%	4.2964	Pass	
21	1.91	2.07%	3.8872	Pass	
23	2.17	2.35%	3.5492	Pass	
25	1.50	1.63%	3.2653	Pass	
27	0.74	0.80%	3.0234	Pass	
29	1.72	1.86%	2.8149	Pass	
31	1.23	1.33%	2.6333	Pass	
33	0.72	0.78%	2.4737	Pass	
35	0.64	0.69%	2.3323	Pass	
37	0.84	0.91%	2.2063	Pass	
39	0.92	1.00%	2.0931	Pass	



8 Thermal Performance

Images captured after running for >30 minutes at room temperature (25 °C), open frame for the conditions specified.

8.1 $V_{IN} = 195 \text{ VAC}$, 50 Hz, 78 V LED Load

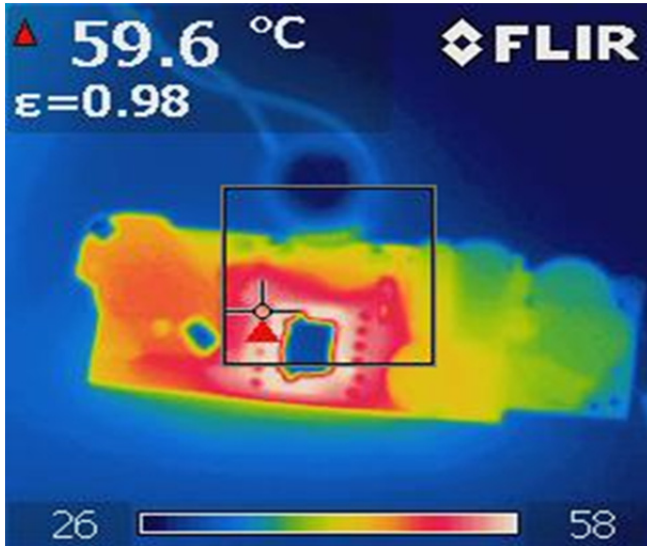


Figure 16 – Top Side.

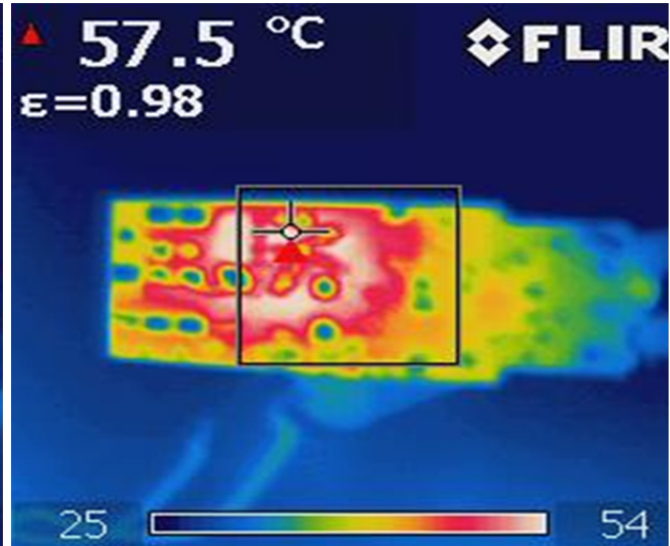


Figure 17 – Bottom Side.

8.2 $V_{IN} = 230 \text{ VAC}$, 50 Hz, 78 V LED Load

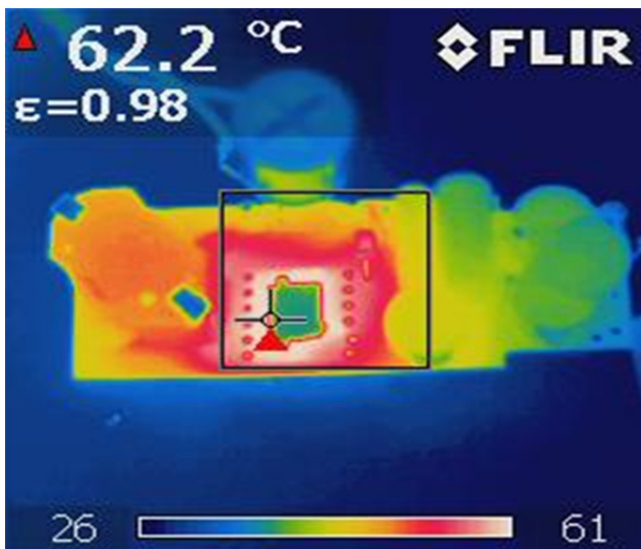


Figure 18 – Top Side.

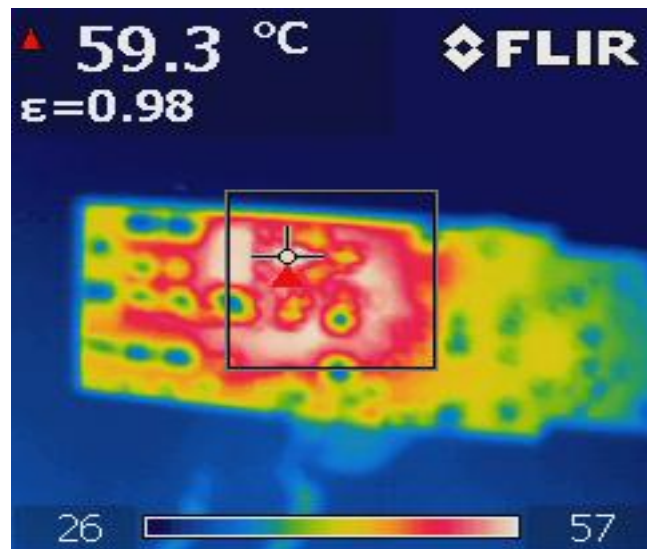


Figure 19 – Bottom Side.

9 Waveforms

9.1 Input Voltage and Input Current at Normal Operation

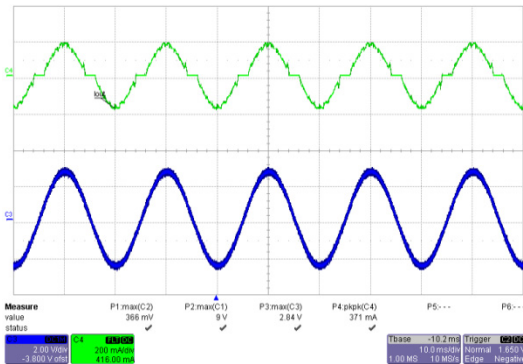


Figure 20 – 195 VAC, Full Load.
Upper: I_{IN} , 200 mA / div.
Lower: V_{IN} , 200 V, 10 ms / div.

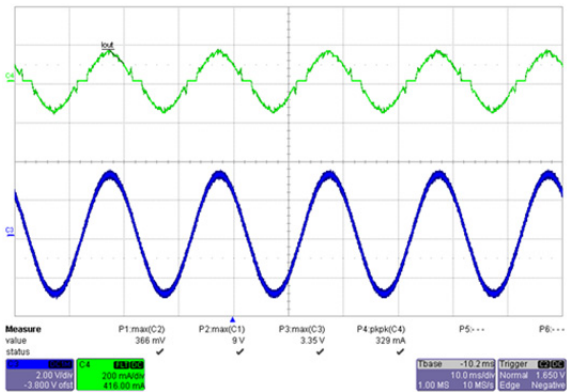


Figure 21 – 220 VAC, Full Load.
Upper: I_{IN} , 200 mA / div.
Lower: V_{IN} , 200 V, 10 ms / div.

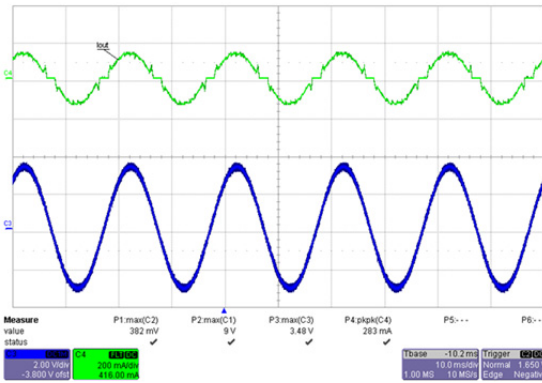


Figure 22 – 230 VAC, Full Load.
Upper: I_{IN} , 200 mA / div.
Lower: V_{IN} , 200 V, 10 ms / div.

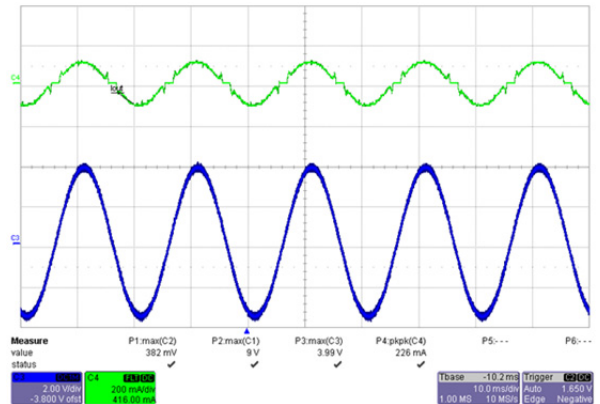


Figure 23 – 265 VAC, Full Load.
Upper: I_{IN} , 200 mA / div.
Lower: V_{IN} , 200 V, 10 ms / div.

9.2 Output Current and Output Voltage at Normal Operation

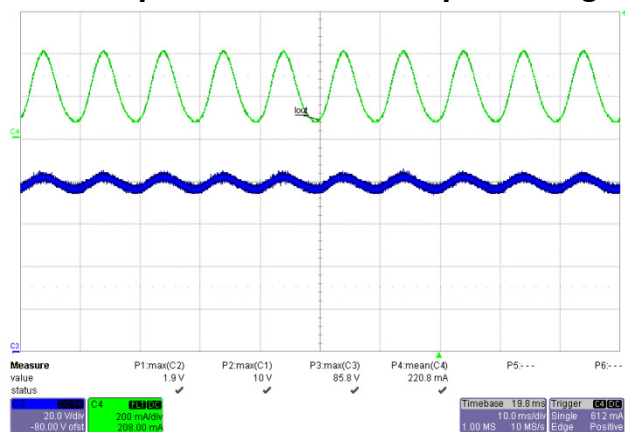


Figure 24 – 195 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{OUT} , 20 V, 10 ms / div.

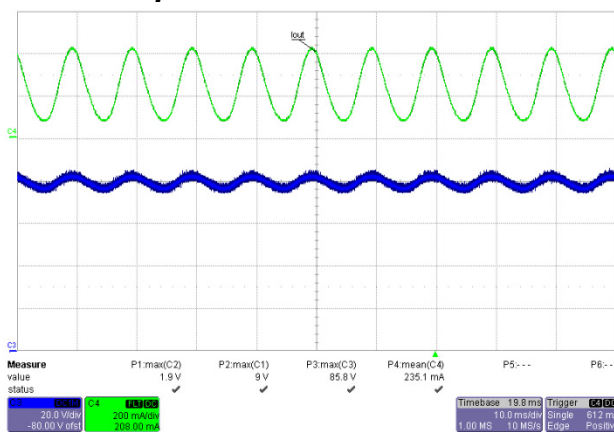


Figure 25 – 220 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{OUT} , 20 V, 10 ms / div.

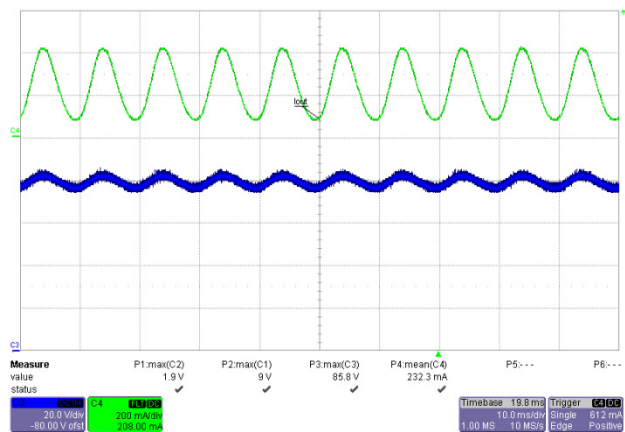


Figure 26 – 230 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{OUT} , 20 V, 10 ms / div.

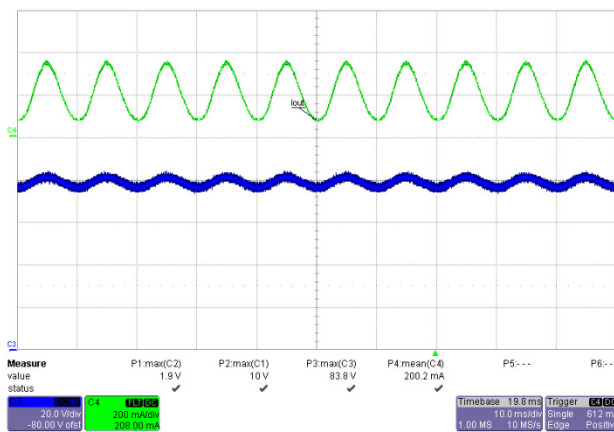


Figure 27 – 265 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{OUT} , 20 V, 10 ms / div.



9.3 Output Current/Voltage Rise and Fall

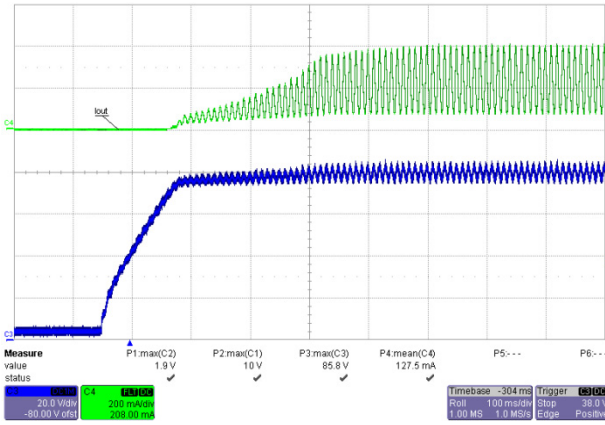


Figure 28 – 195 VAC Output Rise.
Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 20 V, 100 ms / div.

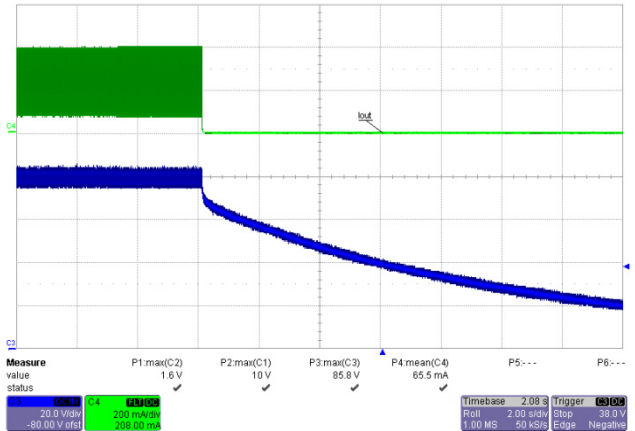


Figure 29 – 195 VAC Output Fall.
Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 20 V, 2 s / div.

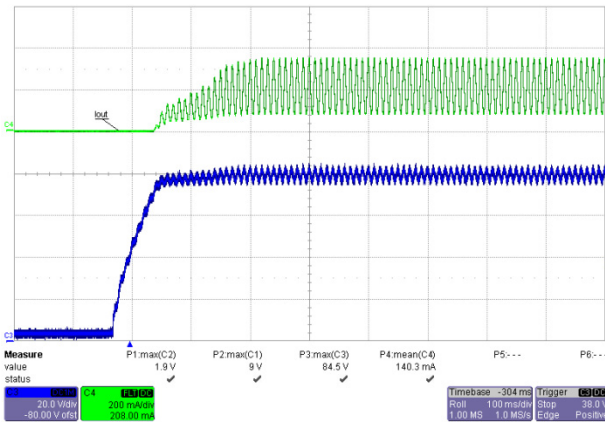


Figure 30 – 265 VAC Output Rise.
Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 20 V, 100 ms / div.

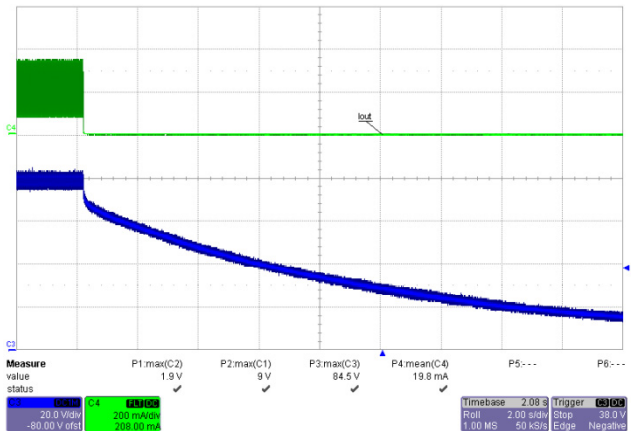


Figure 31 – 265 VAC Output Fall.
Upper: I_{OUT} , 200 mA / div.
Lower: V_{OUT} , 20 V, 2 s / div.



9.4 Input Voltage and Output Current Waveform at Start-up

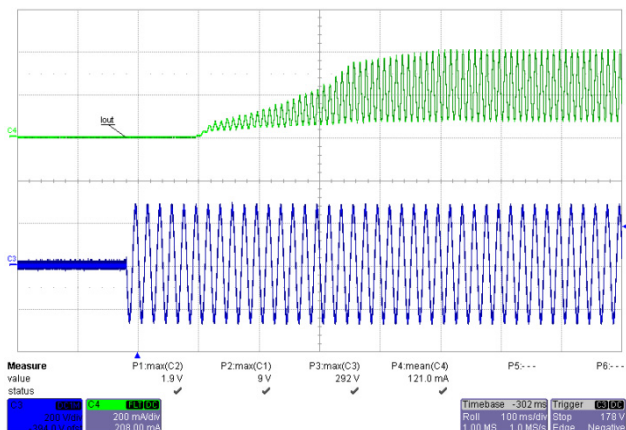


Figure 32 – 195 VAC, 50 Hz.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{IN} , 200 V, 100 ms / div.

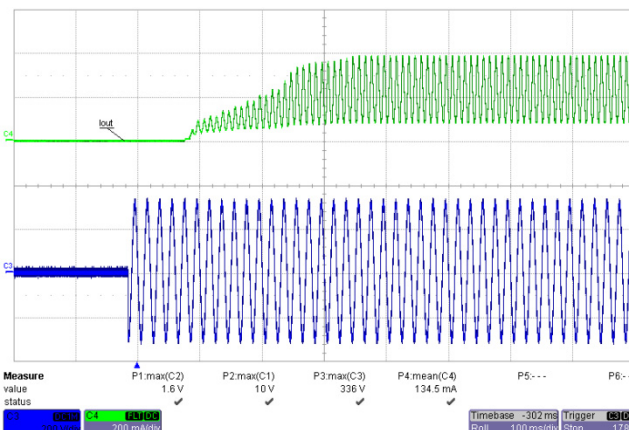


Figure 33 – 220 VAC, 50 Hz.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{IN} , 200 V, 100 ms / div.

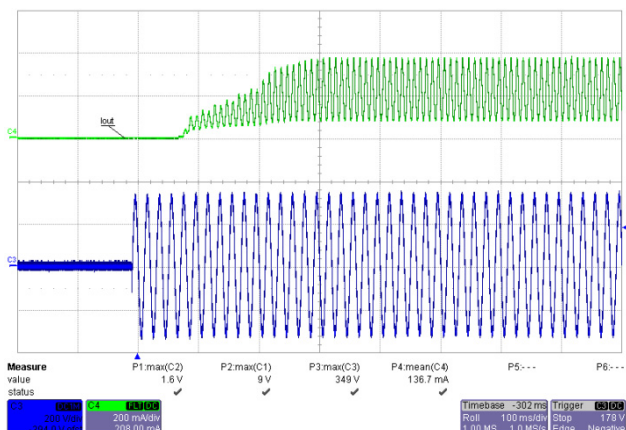


Figure 34 – 230 VAC, 50 Hz.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{IN} , 200 V, 100 ms / div.

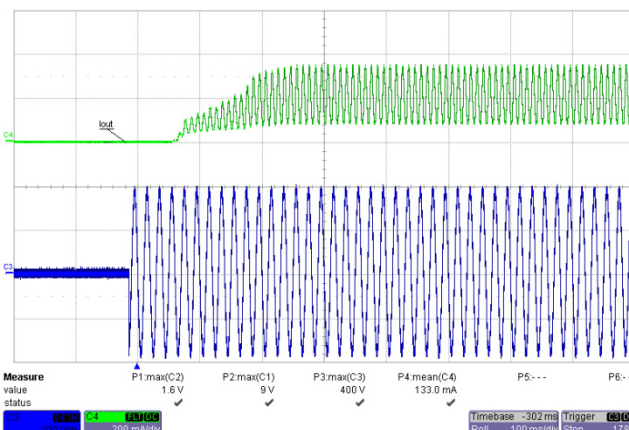


Figure 35 – 265 VAC, 50 Hz.
 Upper: I_{OUT} , 200 mA / div.
 Lower: V_{IN} , 200 V, 100 ms / div.



9.5 Drain Waveforms at Normal Operation

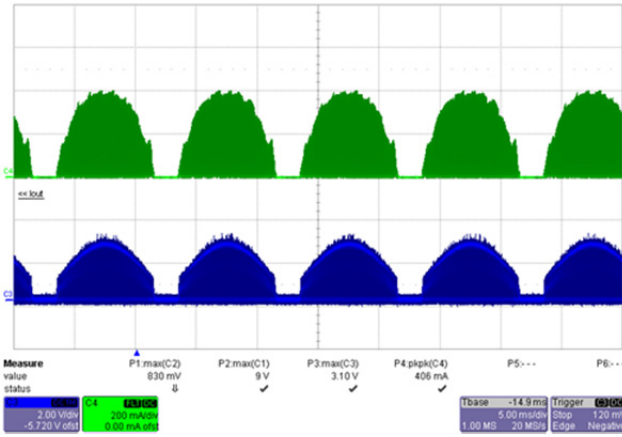


Figure 36 – 195 VAC, 50 Hz.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 ms / div.

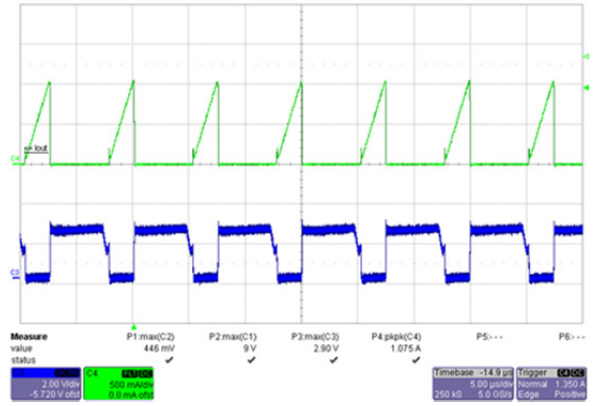


Figure 37 – 195 VAC, 50 Hz.
 Upper: I_{DRAIN} , 500 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 μs / div.

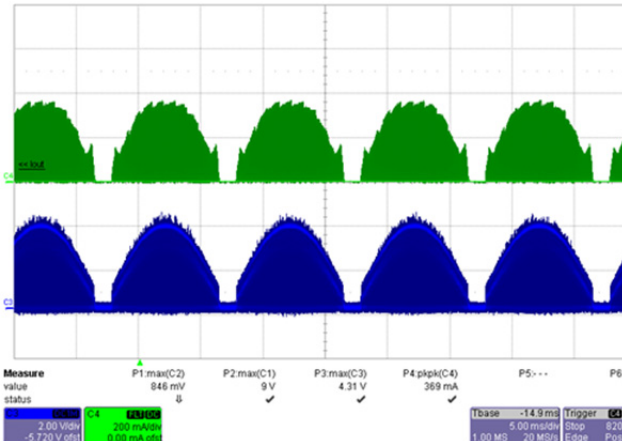


Figure 38 – 265 VAC, 50 Hz.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 ms / div.

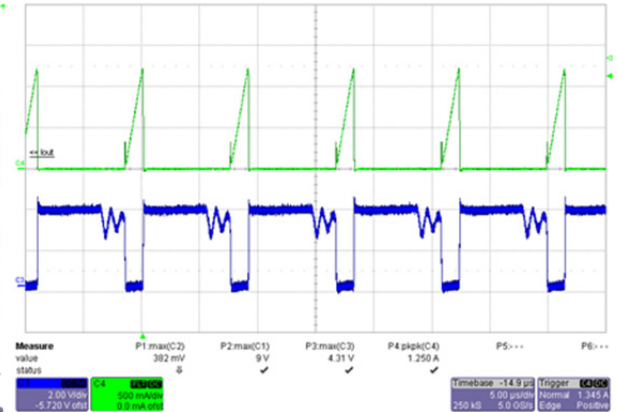


Figure 39 – 265 VAC, 50 Hz.
 Upper: I_{DRAIN} , 500 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 μs / div.



9.6 Start-up Drain Voltage and Current

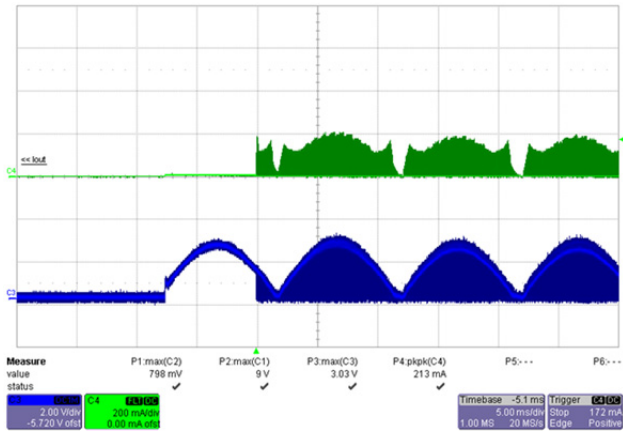


Figure 40 – 195 VAC, 50 Hz.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 ms / div.

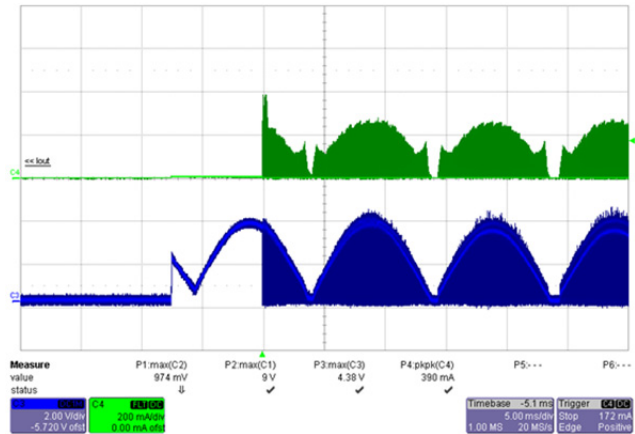


Figure 41 – 265 VAC, 50 Hz.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 200 V, 5 ms / div.



9.7 Drain Current and Drain Voltage During Output Short-Circuit

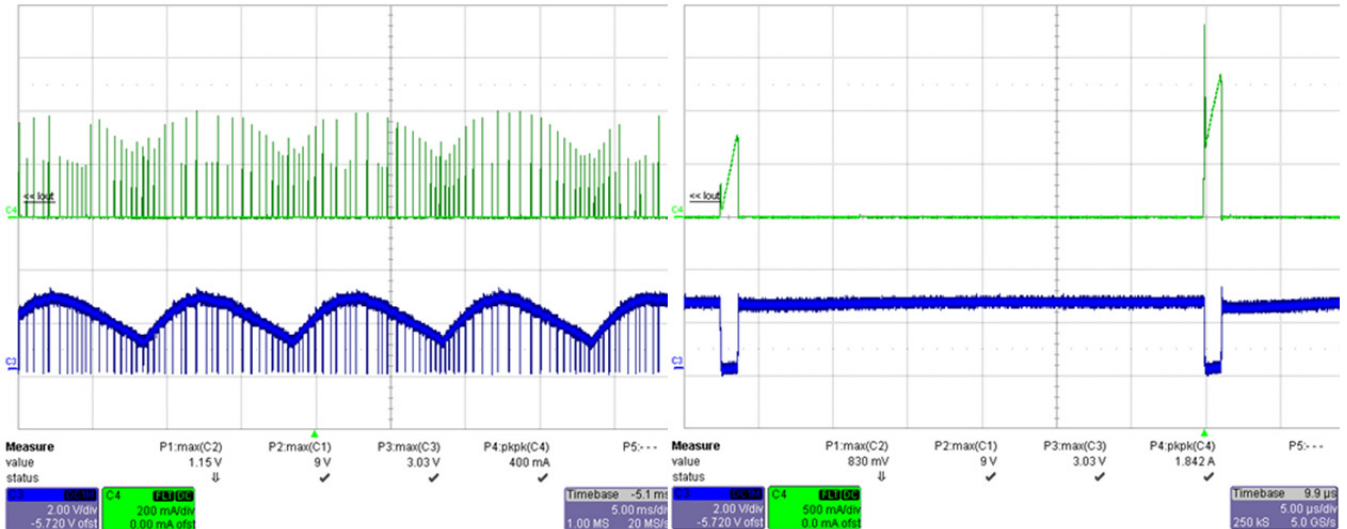


Figure 42 – 195 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN} , 200 mA / div.
Lower: V_{DRAIN} , 200 V, 5 ms / div.

Figure 43 – 195 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN} , 500 mA / div.
Lower: V_{DRAIN} , 200 V, 5 μ s / div.

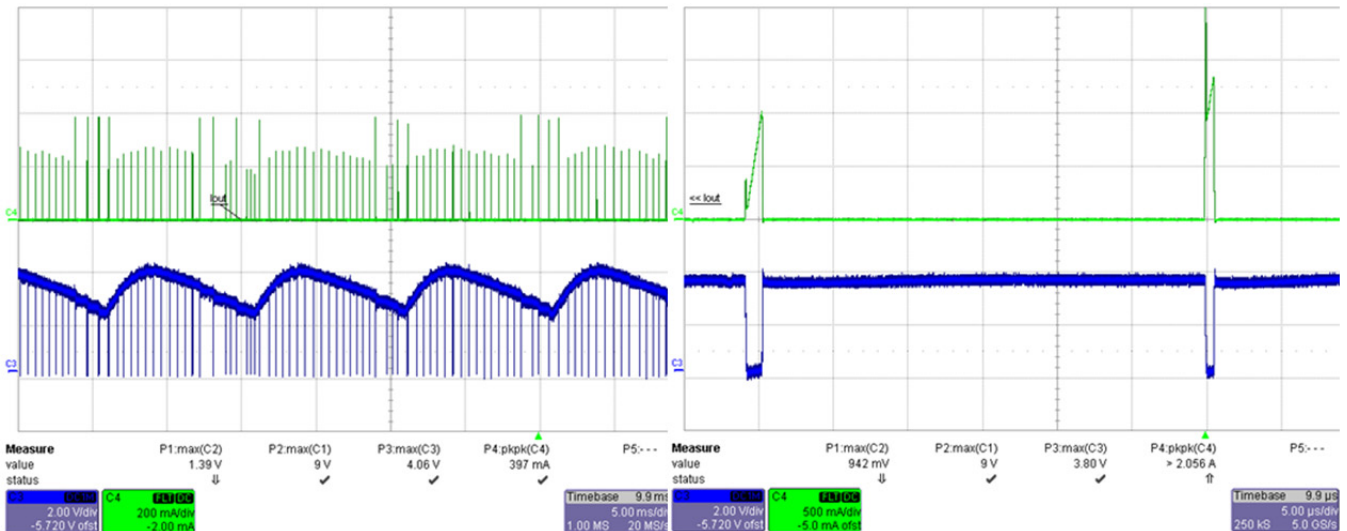


Figure 44 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN} , 200 mA / div.
Lower: V_{DRAIN} , 200 V, 5 ms / div.

Figure 45 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN} , 500 mA / div.
Lower: V_{DRAIN} , 200 V, 5 μ s / div.



9.8 No-Load Output Voltage

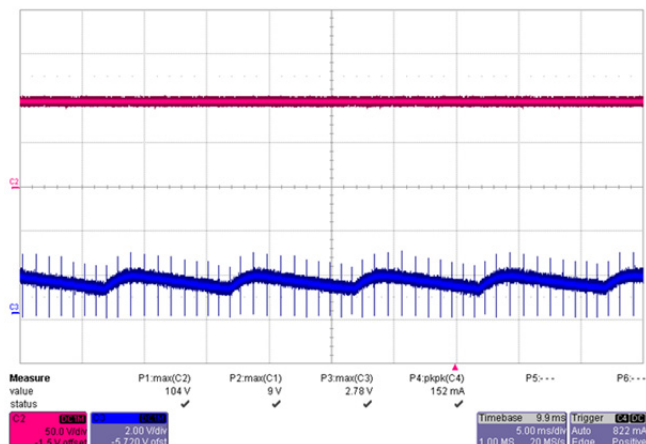


Figure 46 – 195 VAC, 50 Hz No-Load Characteristic.
 Upper: V_{OUT} , 50 V / div.
 Lower: V_{DRAIN} , 200 V / div., 5 ms / div.

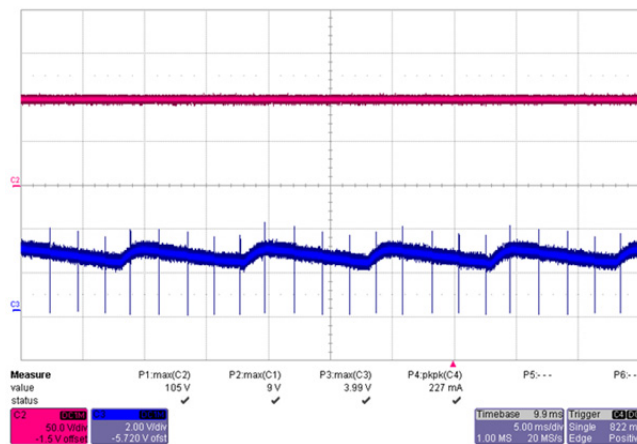


Figure 47 – 265 VAC, 50 Hz No-Load Characteristic.
 Upper: V_{OUT} , 50 V / div.
 Lower: V_{DRAIN} , 200 V / div., 5 ms / div.



10 Conducted EMI

The unit was tested using LED load (~78 V V_{OUT}) with input voltage of 230 VAC, 60 Hz at room temperature.

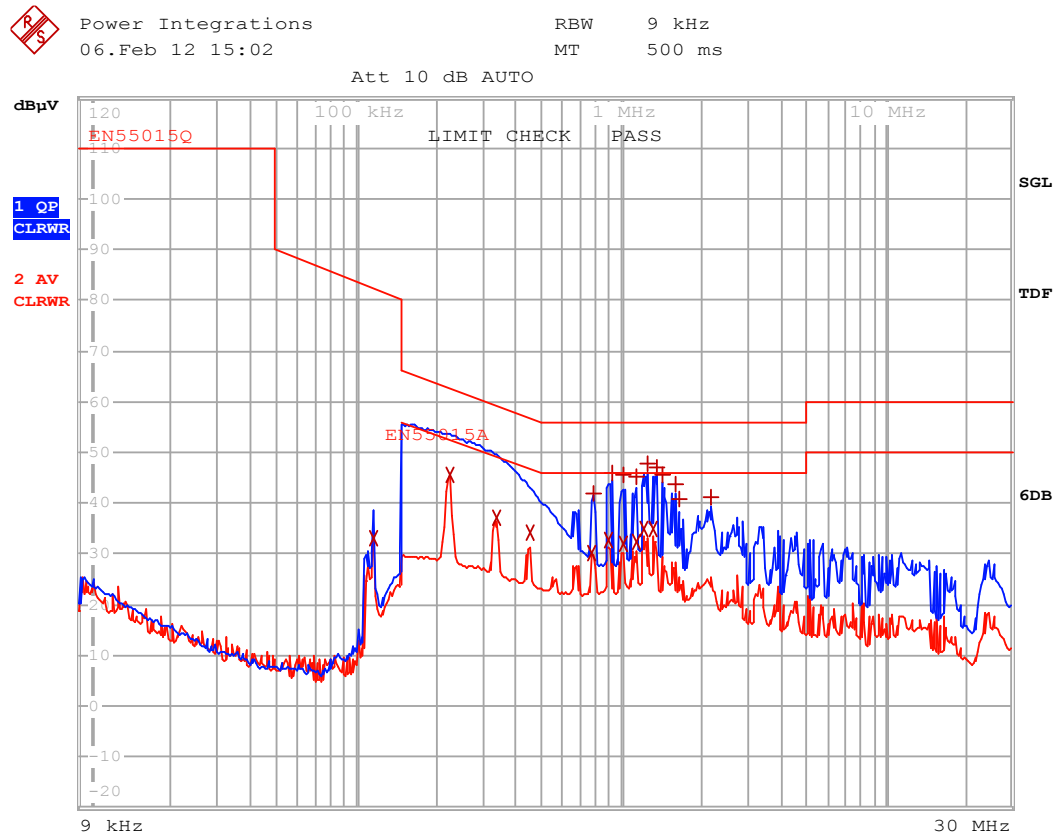


Figure 48 – Conducted EMI, L1 Phase. 78 V / 230 mA Load, 230 VAC, 60 Hz, and EN55015 Limits.



EDIT PEAK LIST (Final Measurement Results)				
Trace1:	EN55015Q			
Trace2:	EN55015A			
Trace3:	---			
TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2 Average	116.100896051 kHz	32.98	L1 gnd	
2 Average	223.329560038 kHz	45.55	L1 gnd	-7.14
2 Average	335.832355405 kHz	36.98	N gnd	-12.32
2 Average	452.651275966 kHz	34.07	N gnd	-12.75
2 Average	774.672132397 kHz	30.25	N gnd	-15.74
1 Quasi Peak	790.243042258 kHz	41.76	N gnd	-14.23
2 Average	890.465639904 kHz	32.77	N gnd	-13.22
1 Quasi Peak	917.447639259 kHz	46.05	N gnd	-9.94
1 Quasi Peak	1.02356729084 MHz	45.69	N gnd	-10.30
2 Average	1.02356729084 MHz	32.17	N gnd	-13.82
1 Quasi Peak	1.13065507631 MHz	45.39	N gnd	-10.60
2 Average	1.13065507631 MHz	32.25	N gnd	-13.74
2 Average	1.22433743114 MHz	34.94	N gnd	-11.05
1 Quasi Peak	1.26143607964 MHz	47.72	N gnd	-8.27
2 Average	1.32578199726 MHz	34.86	N gnd	-11.13
1 Quasi Peak	1.3524302154 MHz	47.00	N gnd	-8.99
1 Quasi Peak	1.43563192593 MHz	45.67	N gnd	-10.32
1 Quasi Peak	1.60168909723 MHz	43.57	N gnd	-12.42
1 Quasi Peak	1.66672409735 MHz	40.89	N gnd	-15.10
1 Quasi Peak	2.18042326152 MHz	41.00	N gnd	-14.99

Figure 49 – Conducted EMI, Final. 78 V / 230 mA Load, 230 VAC, 60 Hz, and EN55015 Limits.



11 Line Surge

Input voltage was set at 230 VAC / 60 Hz. Output was loaded with 78 V LED string and operation was verified following each surge event.

Differential input line 1.2 / 50 μ s surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V) 10strikes/condition	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+500	230	L to N	0	Pass
-500	230	L to N	0	Pass
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass

Differential input line ring surge testing was completed on one test unit to IEC61000-4-5.

Surge Level (V) 10strikes/condition	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass

Unit passes under all test conditions.



12 Revision History

Date	Author	Revision	Description and Changes	Reviewed
19-Mar-12	DK	1.0	Initial Release	Apps & Mktg



For the latest updates, visit our website: www.powerint.com

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