Design Example Report

Title	***Highly Accurate (<±5%) Constant Current TRIAC Dimmable, High Power Factor (0.9) 7.4 W Output LED Driver Using LinkSwitch™-PH LNK403EG***
Specification	176 VAC – 265 VAC Input; 66 V, 112 mA Output
Application	A19 LED Driver
Author	Applications Engineering Department
Document Number	DER-296
Date	November 3, 2011
Revision	1.0

Summary and Features

- TRIAC dimmer compatible
  - >1000:1 dimming range (TRIAC dependent)
  - Clean monotonic start-up – no output blinking
  - Fast start-up (<300 ms) – no perceptible delay
- Highly energy efficient
  - ≥82% at 230 VAC
- Low cost, low component count and small printed circuit board footprint solution
  - Excellent line and load regulation, <2% typical
  - Frequency jitter for smaller, lower cost EMI filter
- Integrated protection and reliability features
  - Output open circuit / output short-circuit protected with auto-recovery
  - Line input overvoltage shutdown extends voltage withstand during line faults
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
- IEC 61000-4-5 ring wave, IEC 61000-3-2 Class C and EN55015 B conducted EMI compliant

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PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a non-isolated high power factor (PF) TRIAC dimmable LED driver designed to drive a nominal LED string voltage of 66 V at 110 mA from an input voltage range of 176 VAC to 265 VAC. The LED driver utilizes the LNK403EG from the LinkSwitch-PH family of ICs.

The topology used is a single-stage non-isolated flyback that meets the stringent space requirements for this design. Enhanced line and load output current regulation requirement is achieved by using a sensing resistance and shunt regulator.

High power factor and low THD is achieved by employing the LinkSwitch-PH IC which also provides a sophisticated range of protection features including auto-restart for open control loop and output short-circuit conditions. Line overvoltage provides extended line fault and surge withstand, output overvoltage protects the supply should the load be disconnected and accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.

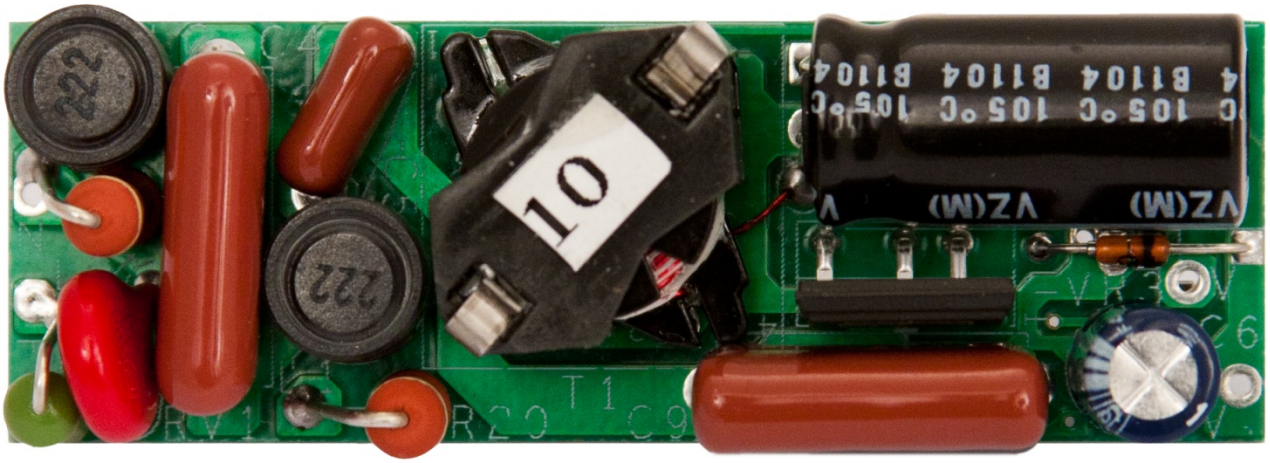

Figure 1 – Populated Circuit Board Photograph (Top View).

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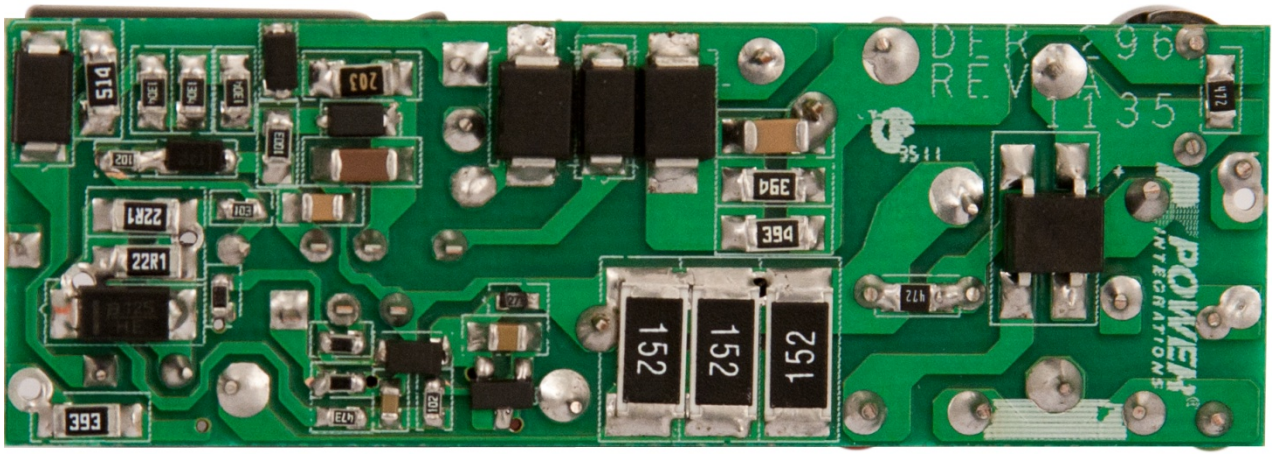

Figure 2 – Populated Circuit Board Photograph (Bottom View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	176	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50		Hz	
Output						
Output Voltage	V_{OUT}		66		V	
Output Current	I_{OUT}	108	112	116	mA	V_{OUT} = 66, V_{IN} = 230 VAC, 25°C
Total Output Power						
Continuous Output Power	P_{OUT}		7.4		W	
Efficiency						
Full Load	η	81	82		%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		CISPR 15B / EN55015B				
Safety		Non-Isolated				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	
Common mode (L1/L2-PE)						
Differential Surge			500		V	
Power Factor			0.9			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents		EN 61000-3-2 Class D (C)				Class C specifies Class D Limits when P_{IN} <25 W
Ambient Temperature	T_{AMB}		50		°C	Free convection, sea level

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3 Schematic

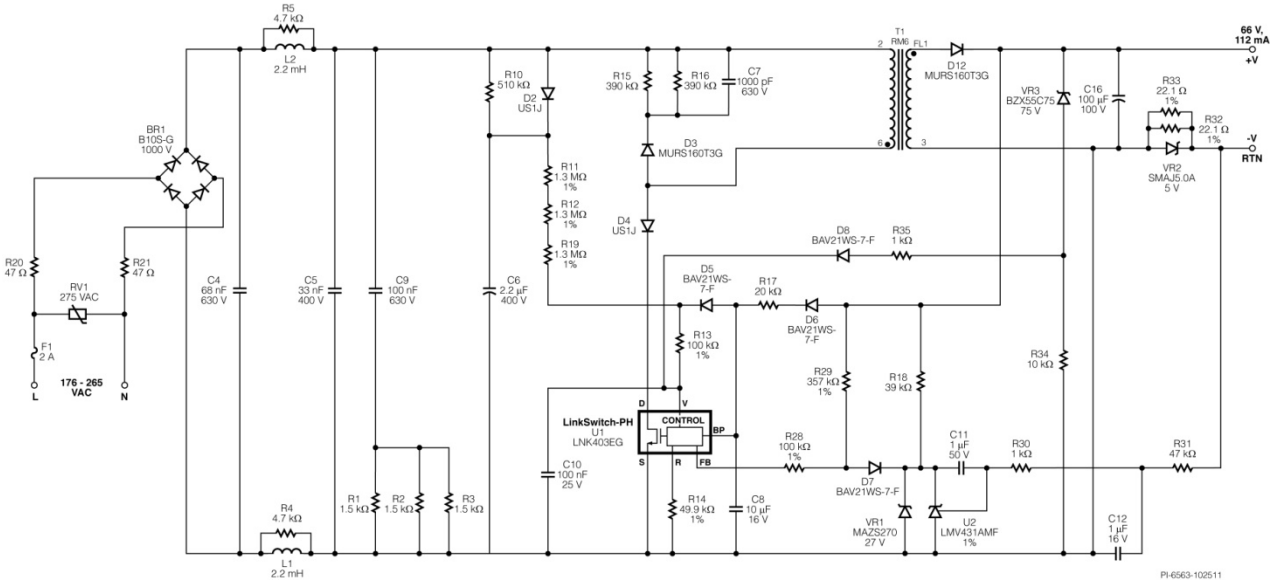

Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-PH device is a controller with an integrated 725 V power MOSFET for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage continuous conduction mode flyback topology and provides a primary side regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 provides protection from component failure and RV1 provides a clamp to limit the maximum voltage during differential line surge events. A 275 VAC rated part was selected, being slightly above the maximum specified operating voltage of 265 VAC. Diode bridge BR1 rectifies the AC line voltage with capacitor C5 providing a low impedance path (decoupling) for the primary switching current. A low value of capacitance (sum of C4 and C5) is necessary to maintain a power factor of greater than 0.9.

EMI filtering is provided by inductors L1 and L2, and capacitors C4 and C5. Resistor R4 and R5 across L1 and L2 damp any LC resonances due to the filter components and the AC line impedance which would ordinarily show up on the conducted EMI measurements.

4.2 LinkSwitch-PH Primary

One side of the transformer (T1) is connected to the DC bus and the other to the DRAIN pin of the LinkSwitch-PH. During the on-time of the MOSFET current ramps through the primary, storing energy which is then delivered to the output during the MOSFET off-time. An RM6 core size was selected to meet both the power handling and size requirements of the design.

To provide peak line voltage information to U1, the incoming rectified AC peak charges C6 via D2. This is then fed into the VOLTAGE MONITOR (V) pin of U1 as a current via R11, R12, and R19. Resistor R10 provides a discharge path for C6 with a time constant much longer than that of the rectified AC to prevent the V pin current being modulated at the line frequency (which would degrade power factor).

To extend the dimming range R13 disables the line brown-out function of the V pin by supplying a current >I_{UV-} into the V pin. The current is determined by the BYPASS (BP) pin, V pin voltages and the value of R13 and is ~30 μA for this design.

The line overvoltage shutdown function, sensed via the V pin current, extends the rectified line voltage withstand (during surges and line swells) to the 725 BV_{DSS} rating of the internal power MOSFET.

The V pin current and the FEEDBACK (FB) pin current are used internally to control the average output LED current. For phase angle dimming applications a 49.9 kΩ resistor is used on the REFERENCE (R) pin (R14) and 4 MΩ (R11+R12+R19+R13) on the V pin to

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provide a linear relationship between input voltage and the output current. This maximizes the dimming range when used with TRIAC dimmers. The value of R14 is used to select between two values of internal line input brown-in and brown-out thresholds.

During the power MOSFET off-time, D3, R15, R16, and C7 clamp the drain voltage to a safe level which would otherwise rise due to the effects of leakage inductance. Diode D4 is necessary to prevent reverse current from flowing through U1 while the voltage across C5 (rectified input AC) falls to below the reflected output voltage (V_{OR}).

Capacitor C8 provides local decoupling for the BP pin of U1 which is the supply pin for the internal controller. During start-up, C8 is charged to ~6 V from an internal high-voltage current source connected to the D pin. Once charged U1 starts switching at which point the operating supply current is provided from the output via R17. Diode D6 isolates the BP pin from the output capacitance C16 to prevent the start-up time increasing due to charging of both C8 and C16.

4.3 Feedback

A current sense resistor (R32 parallel with R33) and a shunt regulator U2 is employed to enable very tight output current regulation for this design. Output current sensed by R32 and R33 is filtered by R31 and C12, with values chosen to have a time constant greater than the line frequency in order to remove the line frequency harmonics and thus enable the slow loop response necessary to maintain high power factor and low THD. This voltage is then compared with the internal reference of U2 to provide a regulated output current of 112 mA. Capacitor C11 and R30 provide feedback compensation for the shunt regulator U2.

During normal operation without a dimmer, the cathode voltage of U2 adjusts the feedback current fed to I_{FB} of U1 thru R28 to maintain a constant output current. Resistor R18 provides bias supply to U2, D7 blocks the current from R18 being fed to I_{FB} and disengages U2 during dimming. The maximum output power (output current) is dictated by the sum of resistances R28 and R29. Total combined resistance of R28 and R29 is selected to match the I_{FB} current requirement of the design

$$I_{FB} = {V_{OUT} - V_{FB}}/{R28 + R29} \approx 140\mu A$$

The maximum operating I_{FB} also dictates the maximum overshoot of the output current during line transients. This overshoot happens because of the slow loop response of the current sense feedback network to maintain high power factor. On this design maximum output peak current is below 175 mA as shown below.

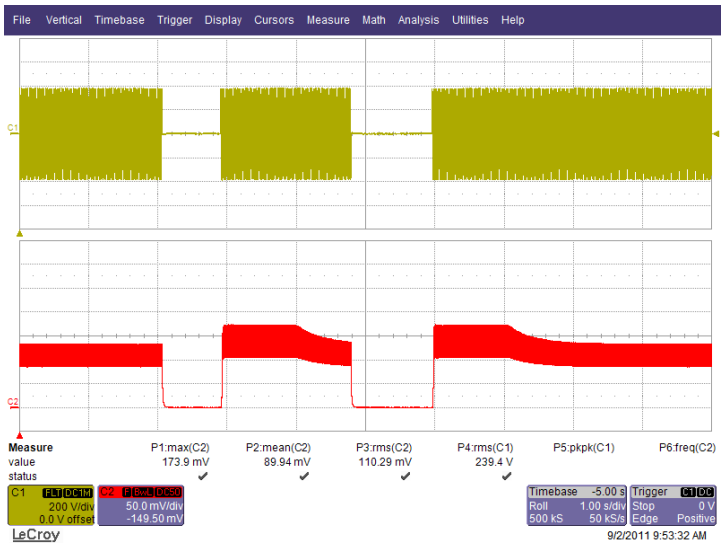

Figure 4 – 265 VAC - 0 - 265 VAC Line Transient.
Upper: V_{IN} 200 V / div., Lower: I_{OUT} 50 mA / div.

This condition is not present during normal start-up condition when C11 is still discharged as shown on the waveforms of section 12.8.

Zener diode VR1 limits the maximum voltage on the cathode to anode of U2 which has a maximum rating of 30 V. The ratio of R28 and R29 is then selected to have a voltage at the anode of D7 to be less than VR1. This is to ensure that during dimming condition, D7 is reverse biased and natural dimming through I_{FB} and I_V current feedbacks takeover the control of the output current.

Zener diode VR2 is an optional component that is used to protect the current sense resistors R32 and R33 during output short condition. The network formed by D8, R34, R35, and VR3 forms the OVP circuit. During open load condition, VR3 will be forward biased and inject a current on the V pin through D8 and R35. This will increase I_V current and will eventually trigger the OV protection of the IC and stop the switching, thus limiting the output voltage to ~ VR3 + V_V.

4.4 Output Rectification

The transformer secondary winding is rectified by D12 and filtered by C16. Capacitor C16 was selected to give an LED ripple current equal to ±30% of the mean value. For designs where higher ripple is acceptable, the output capacitance value can be reduced (and for lower ripple increased).

4.5 TRIAC Phase Dimming Control Compatibility

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduced a number of tradeoffs in the design.

Due to the much lower power consumed by LED based lighting the current drawn by the lamp can fall below the holding current of the TRIAC within the dimmer. This causes

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undesirable behavior such as the lamp turning off before the end of the dimmer control range and/or flickering as the TRIAC fires inconsistently. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero.

To overcome these issues, passive damper and passive bleeder circuits were added. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply. For non-dimming applications these components can simply be omitted.

The passive damper consists of components R20 and R21 which dampen ringing of the input network during TRIAC dimming.

The passive bleeder circuit is comprised of C9 and parallel combination of R1, R2, and R3. This keeps the input current above the TRIAC holding current while the driver input current increases during each AC half-cycle preventing the TRIAC switch from oscillating at the start of each conduction angle period.

This arrangement provided flicker-free dimming operation with phase angle dimmers from Europe, China, Korea, both leading-edge and lagging-edge types.

5 PCB Layout

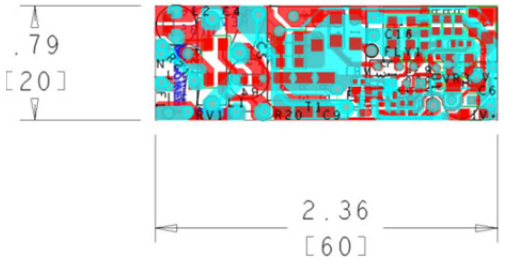

Figure 5 – PCB Layout and Outline (60 mm x 20 mm).

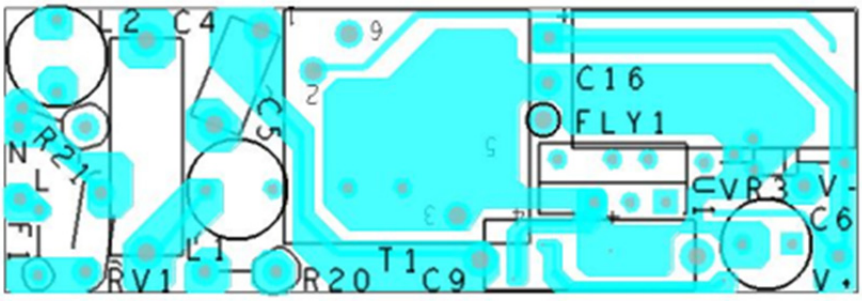

Figure 6 – Top Side.

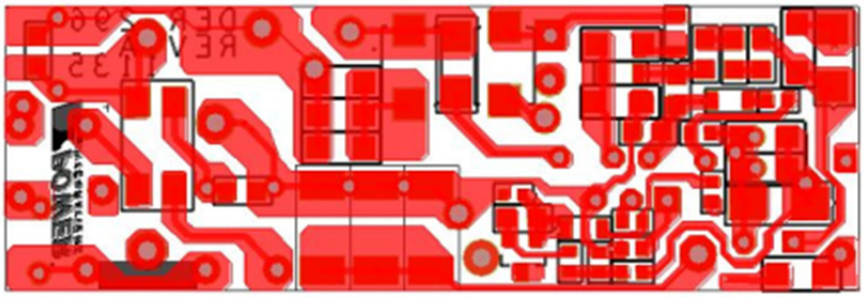

Figure 7 – Bottom Side.

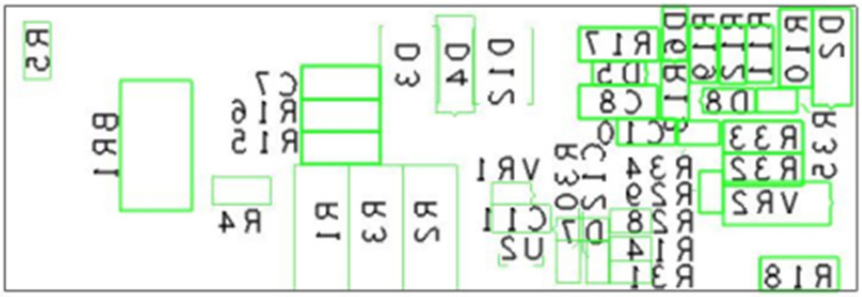

Figure 8 – Bottom Side Component Placement.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Technology
2	1	C4	68 nF, 630 V, Film	ECQ-E6683KF	Panasonic
3	1	C5	33 nF, 400 V, Film	ECQ-E4333KF	Panasonic
4	1	C6	2.2 μF, 400 V, Electrolytic, (8 x 11.5)	SMG400VB2R2M8X11LL	Nippon Chemi-Con
5	1	C7	1000 pF, 630 V, Ceramic, X7R, 1206	ECJ-3FB2J102K	Panasonic
6	1	C8	10 μF, 16 V, Ceramic, X7R, 1206	C3216X7R1C106M	TDK
7	1	C9	100 nF, 630 V, Film	ECQ-E6104KF	Panasonic
8	1	C10	100 nF, 25 V, Ceramic, X7R, 0805	ECJ-2VB1E104K	Panasonic
9	1	C11	1 μF, 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX
10	1	C12	1 μF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
11	1	C16	100 μF, 100 V, Electrolytic, Gen. Purpose, (10 x 20)	UVZ2A101MPD	Nichicon
12	2	D2 D4	DIODE ULTRA FAST, SW 600 V, 1 A, SMA	US1J-13-F	Diodes, Inc.
13	2	D3 D12	600 V, 1 A, Ultrafast Recovery, 35 ns, SMB Case	MURS160T3G	On Semi
14	4	D5 D6 D7 D8	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
15	1	F1	Fuse, Pico, 2 A, 250 V, Fast, Axial	0263002.MXL	Littlefuse
16	2	L1 L2	2.2 mH, 0.16 A, Ferrite Core	CTSCH875DF-222K	CT Parts
17	3	R1 R2 R3	1.5 kΩ, 5%, 1 W, Thick Film, 2512	ERJ-1TYJ152U	Panasonic
18	2	R4 R5	4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
19	1	R10	510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
20	3	R11 R12 R19	1.3 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1304V	Panasonic
21	1	R13	100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
22	1	R14	49.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4992V	Panasonic
23	2	R15 R16	390 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ394V	Panasonic
24	1	R17	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
25	1	R18	39 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ393V	Panasonic
26	2	R20 R21	47 Ω, 5%, 2 W, Metal Film	NFR0200004709JR500	Vishay
27	1	R28	100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
28	1	R29	357 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3573V	Panasonic
29	2	R30 R35	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
30	1	R31	47 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
31	2	R32 R33	22.1 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF22R1V	Panasonic
32	1	R34	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
33	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
34	1	T1	Bobbin, RM6, Vertical, 6 pins	B65808-N1006-D1	Epcos
35	1	U1	LinkSwitch-PH, eSIP	LNK403EG	Power Integrations
36	1	U2	1.24 V Shunt Regulator IC, 1%, -40 to 85 C, SOT23-3	LMV431AIMF	National Semi
37	1	VR1	27.0 V, 5%, 150 mW, SOD-323	MAZS2700ML	Panasonic
38	1	VR2	TVS 5.0 V 4002 UNI 5% SMD	SMAJ5.0A	Diodes, Inc.
39	1	VR3	75 V, 500 mW, 5%, DO-35	BZX55C75	Vishay

7 Transformer Specification

7.1 Electrical Diagram

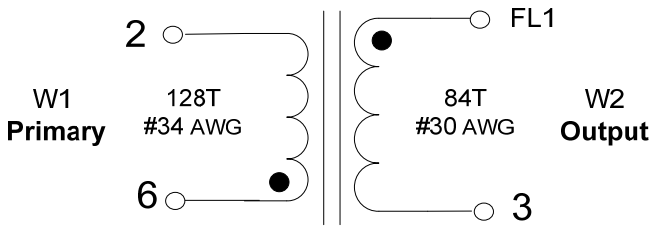

Figure 9 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 2, 6 to FL1, 3.	3000 VAC
Primary Inductance	Pins 2-6, all other windings open, measured at 66 kHz, 0.4 V_{RMS}.	3320 μH ±7%
Resonant Frequency	Pins 2-6, all other windings open.	500 kHz (Min.)
Primary Leakage Inductance	Pins 2-6, with FL1-pin 3 shorted, measured at 100 kHz, 0.4 V_{RMS}.	70 μH ±10%

7.3 Materials

Item	Description
[1]	Core: PC40RM6Z-12.
[2]	Bobbin: B-RM6-V-6 pins-(3/3) With mounting clip, CLIP-RM6.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 6.4 mm wide.
[4]	Wire: Magnet, #34 AWG, solderable double coated.
[5]	Wire: Magnet, #30 AWG, solderable double coated.
[6]	Transformer Varnish, Dolph BC-359 or equivalent.

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7.4 Transformer Build Diagram

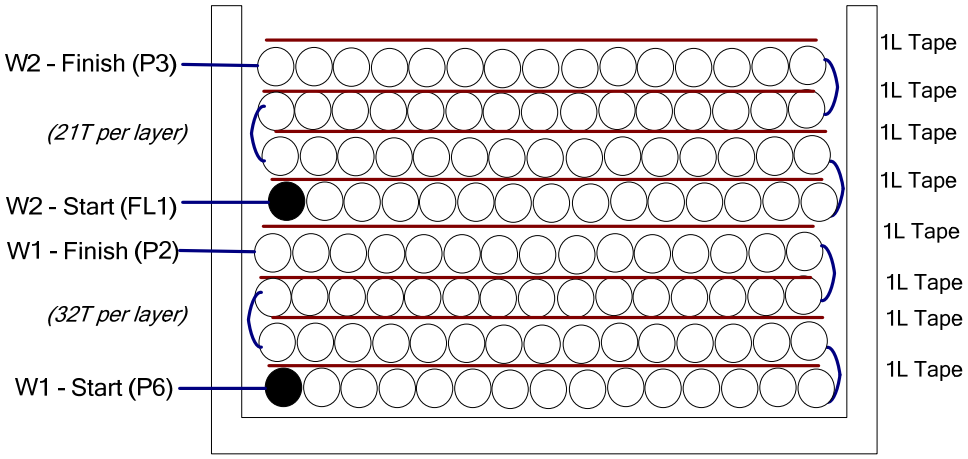

Figure 10 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
Primary Winding (W1)	Starting at pin 6, wind 128 turns of wire item [4] in four layers. Apply one layer of tape item [3] per layer. Finish at pin 2.
Output Winding (W2)	Leave about 1” of wire item [5], use small tape to mark as FL1, enter into slot of secondary side of bobbin, wind 84 turns in four layers. Apply one layer of tape item [3] per layer. Finish at pin 3.
Final Assembly	Grind core to get 3.32 mH inductance. Assemble and secure core halves. Dip impregnate using varnish item [5].

8 Transformer Design Spreadsheet

ACDC_LinkSwitch-PH_032511; Rev.1.3; Copyright Power Integrations 2011	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_032511: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**YES**	*Info*	**YES**		!!! Info. When configured for dimming, best output current line regulation is achieved over a single input voltage range.
VACMIN	176		176	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	66.00			V	Typical output voltage of LED string at full load
VO_MAX			72.60	V	Maximum expected LED string Voltage.
VO_MIN			59.40	V	Minimum expected LED string Voltage.
V_OVP			79.86	V	Over-voltage protection setpoint
IO	0.11			A	Typical full load LED current
PO			7.3	W	Output Power
n			0.8		Estimated efficiency of operation
VB	66		66	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK403**			Universal	115 Doubled/230V
Chosen Device		LNK403	Power Out	6.5W	2.5W
Current Limit Mode	**RED**		RED		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			0.74	A	Minimum current limit
ILIMITMAX			0.85	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			80.6	uA	V pin current
RV			4	M-ohms	Upper V pin resistor
RV2			1E+012	M-ohms	Lower V pin resistor
IFB	141.00		141.0	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			446.8	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.50			V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.70			V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	1.00		1		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			3324	uH	Primary Inductance
VOR	101.33		101.33	V	Reflected Output Voltage.
Expected IO (average)			0.11	A	Expected Average Output Current
KP_VACMAX			1.04		Expected ripple current ratio at VACMAX
TON_MIN			2.28	us	Minimum on time at maximum AC input voltage
PCLAMP			0.07	W	Estimated dissipation in primary clamp
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM6S/I**		**RM6S/I**		
Bobbin		*RM6S/I_BOBBIN*		*P/N:*	*
AE			0.37	cm^2	Core Effective Cross Sectional Area
LE			2.92	cm	Core Effective Path Length
AL			2150	nH/T^2	Ungapped Core Effective Inductance
BW			6.4	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4		Number of Primary Layers
NS	84		84		Number of Secondary Turns

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DC INPUT VOLTAGE PARAMETERS					
VMIN			249	V	Peak input voltage at VACMIN
VMAX			375	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.30		Minimum duty cycle at peak of VACMIN
IAVG			0.06	A	Average Primary Current
IP			0.43	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.12	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			3324	uH	Primary Inductance
NP			128		Primary Winding Number of Turns
NB			84		Bias Winding Number of Turns
ALG			203	nH/T^2	Gapped Core Effective Inductance
BM			3012	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3645	Gauss	Peak Flux Density (BP<3700)
BAC			1506	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1350		Relative Permeability of Ungapped Core
LG			0.21	mm	Gap Length (Lg > 0.1 mm)
BWE			25.6	mm	Effective Bobbin Width
OD			0.20	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.16	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32	Cmils	Bare conductor effective area in circular mils
CMA			270	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
LP_TOL	7		7		Tolerance of primary inductance
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			0.65	A	Peak Secondary Current
ISRMS			0.25	A	Secondary RMS Current
IRIPPLE			0.23	A	Output Capacitor RMS Ripple Current
CMS			51	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			33	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.18	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.08	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN			584	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			326	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			327	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			4.00	M-ohms	Upper V Pin Resistor Value
RV2			1000000000000.00	M-ohms	Lower V Pin Resistor Value
VAC1			115.0	V	Test Input Voltage Condition1
VAC2			230.0	V	Test Input Voltage Condition2
IO_VAC1			0.11	A	Measured Output Current at VAC1

IO_VAC2			0.11	A	Measured Output Current at VAC2
RV1 (new)			4.00	M-ohms	New RV1
RV2 (new)			20911.63	M-ohms	New RV2
V_OV			319.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			66.3	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			447	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+012	k-ohms	Lower FB Pin Resistor Value
VB1			59.4	V	Test Bias Voltage Condition1
VB2			72.6	V	Test Bias Voltage Condition2
IO1			0.11	A	Measured Output Current at Vb1
IO2			0.11	A	Measured Output Current at Vb2
RFB1 (new)			446.8	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

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9 Performance Data

All measurements performed at room temperature using an LED load. The following data were measured using 3 sets of loads to represent a voltage of 97 V ~ 103 V. The table in Section 9.6 shows complete test data values.

9.1 Efficiency

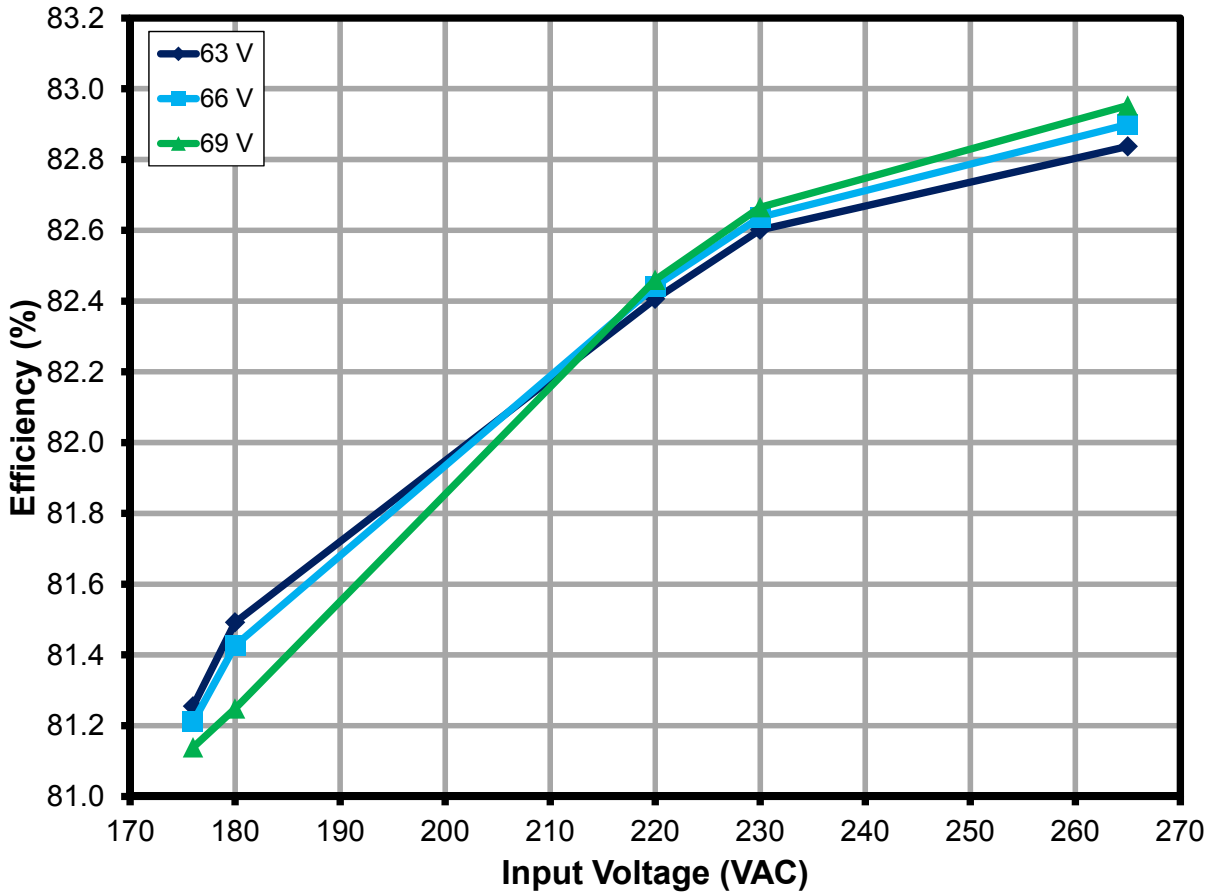

Figure 11 – Efficiency vs. Line and Load.

9.2 Line and Load Regulation

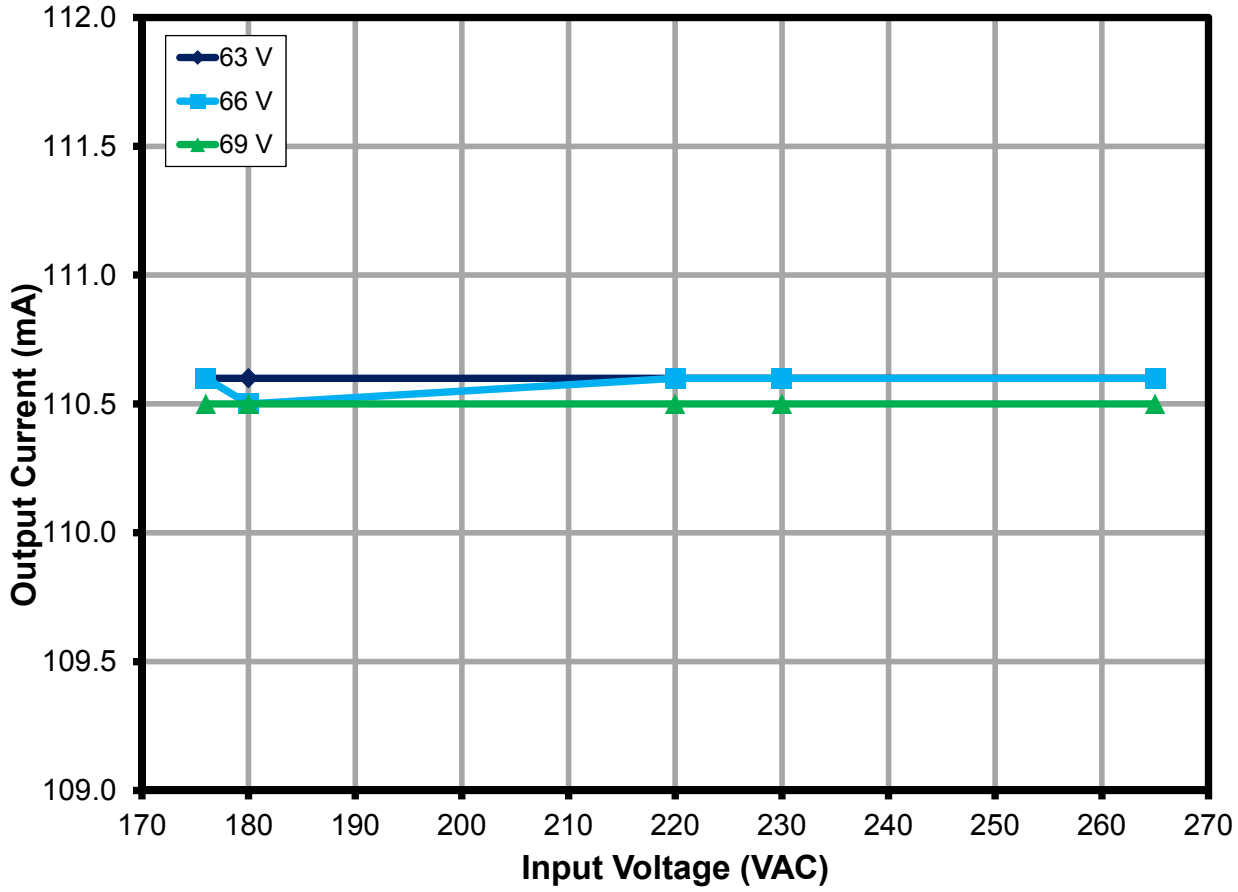

Figure 12 – Regulation vs. Line and Load.

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9.3 Power Factor

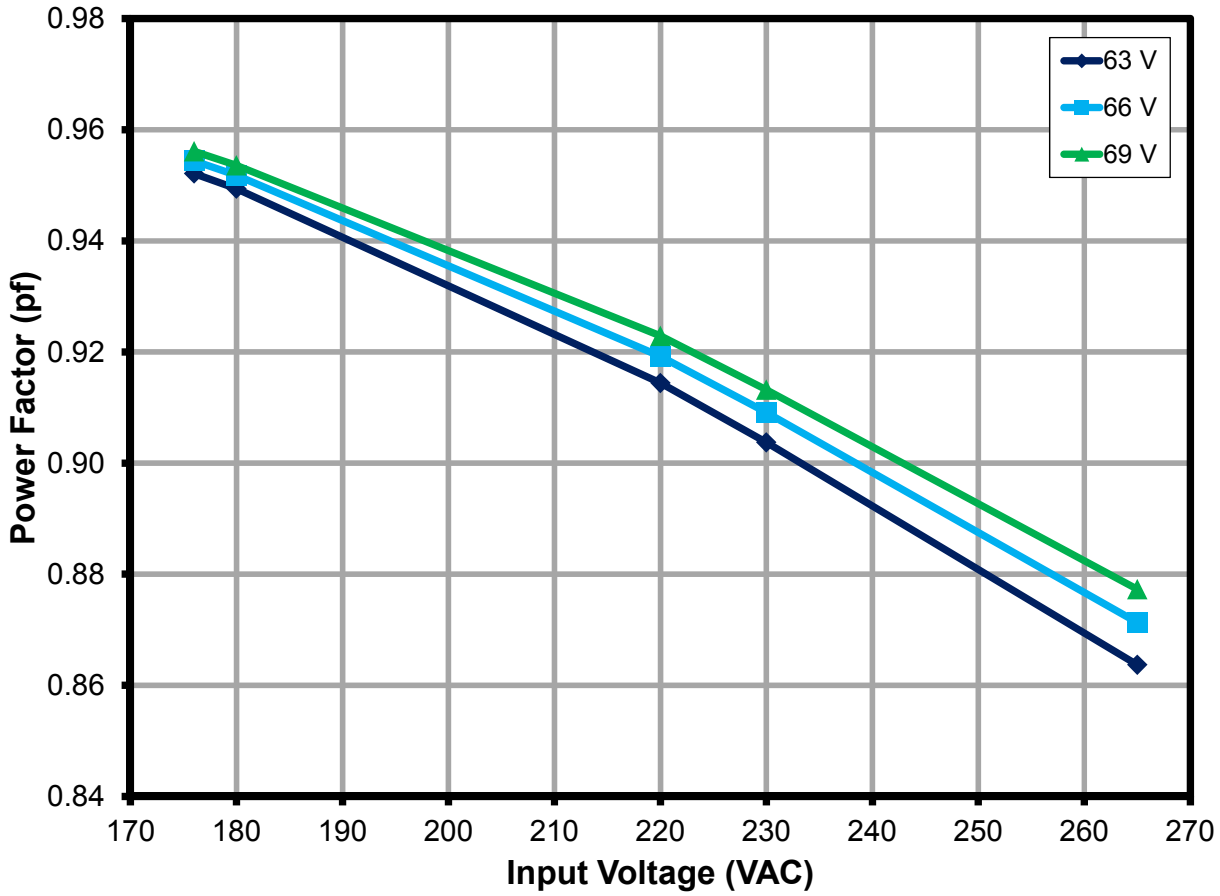

Figure 13 – Power Factor vs. Line and Load.

9.4 A-THD

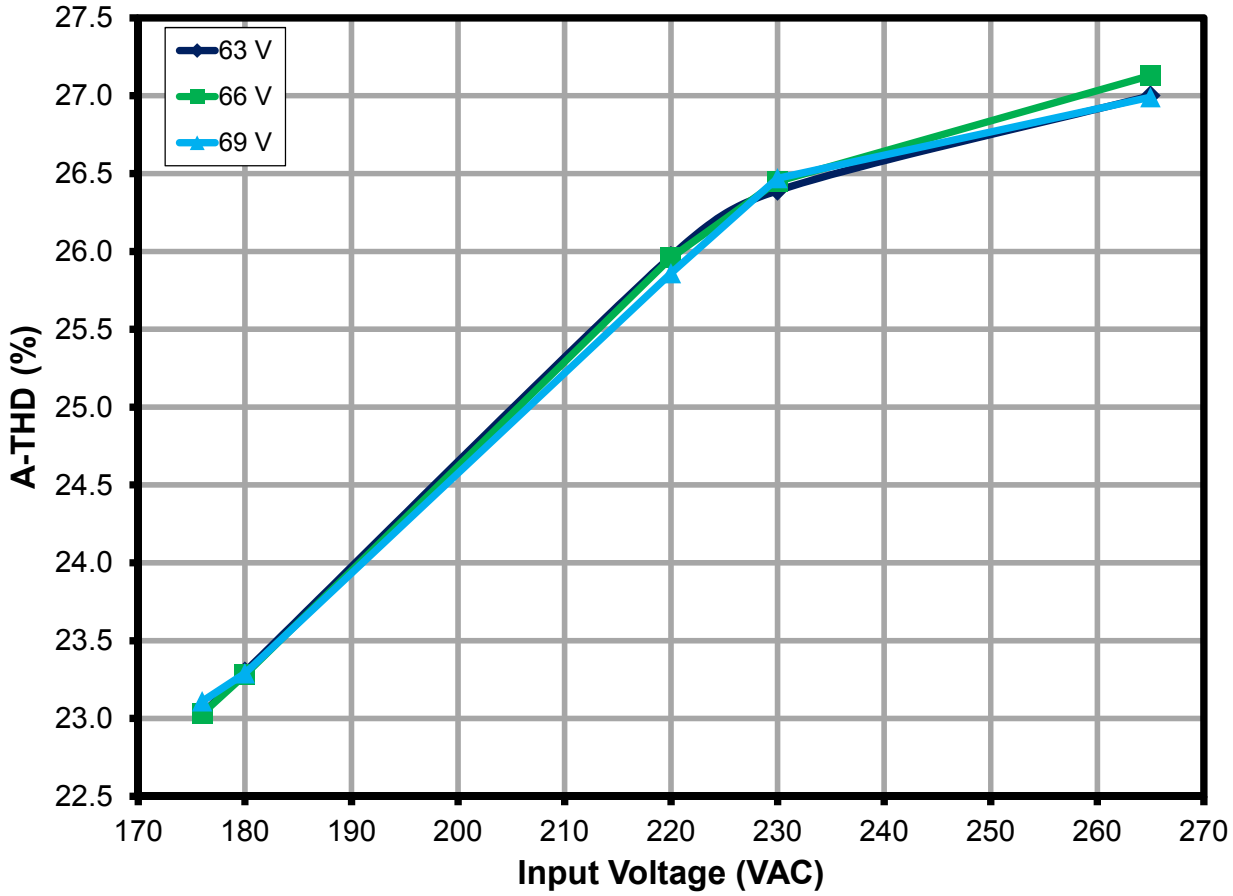

Figure 14 – A-THD vs. Line and Load.

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9.5 Harmonic Currents

The design met the limits for Class C equipment for an active input power of <25 W. In this case IEC61000-3-2 specifies that harmonic currents shall not exceed the limits of Class D equipment[1]. Therefore the limits shown in the charts below are Class D limits which must not be exceeded to meet Class C compliance.

9.5.1 63 V LED Load

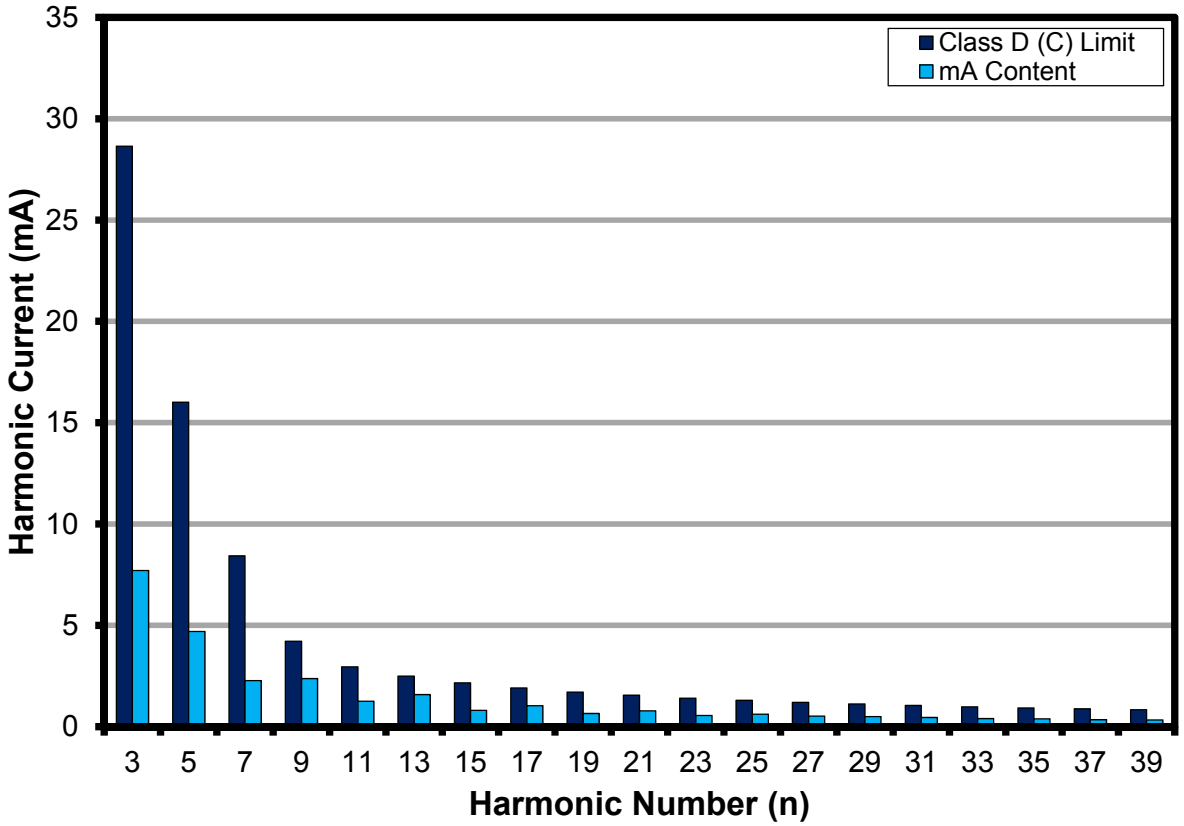

Figure 15 – 63 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

[1] IEC6000-3-2 Section 7.3, table 2, column 2.

9.5.3 66 V LED Load

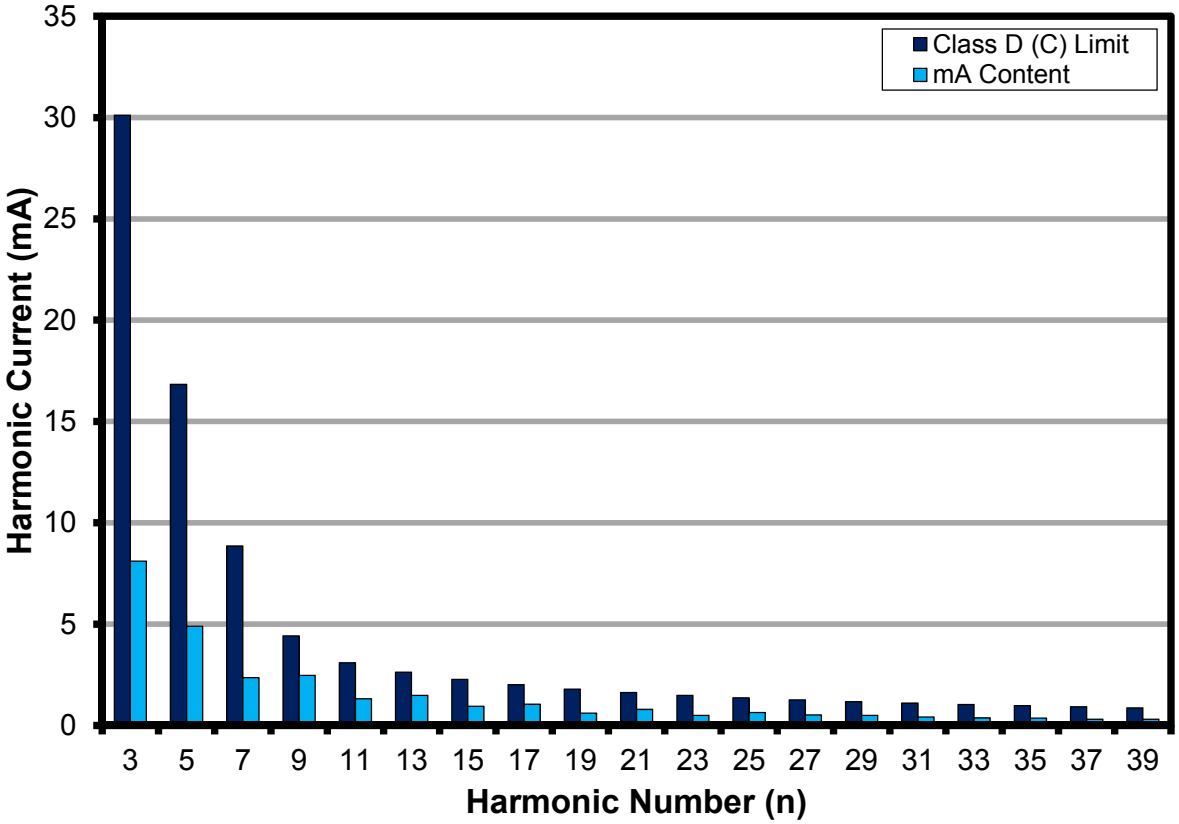

Figure 16 – 66 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

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9.5.4 69 V LED Load

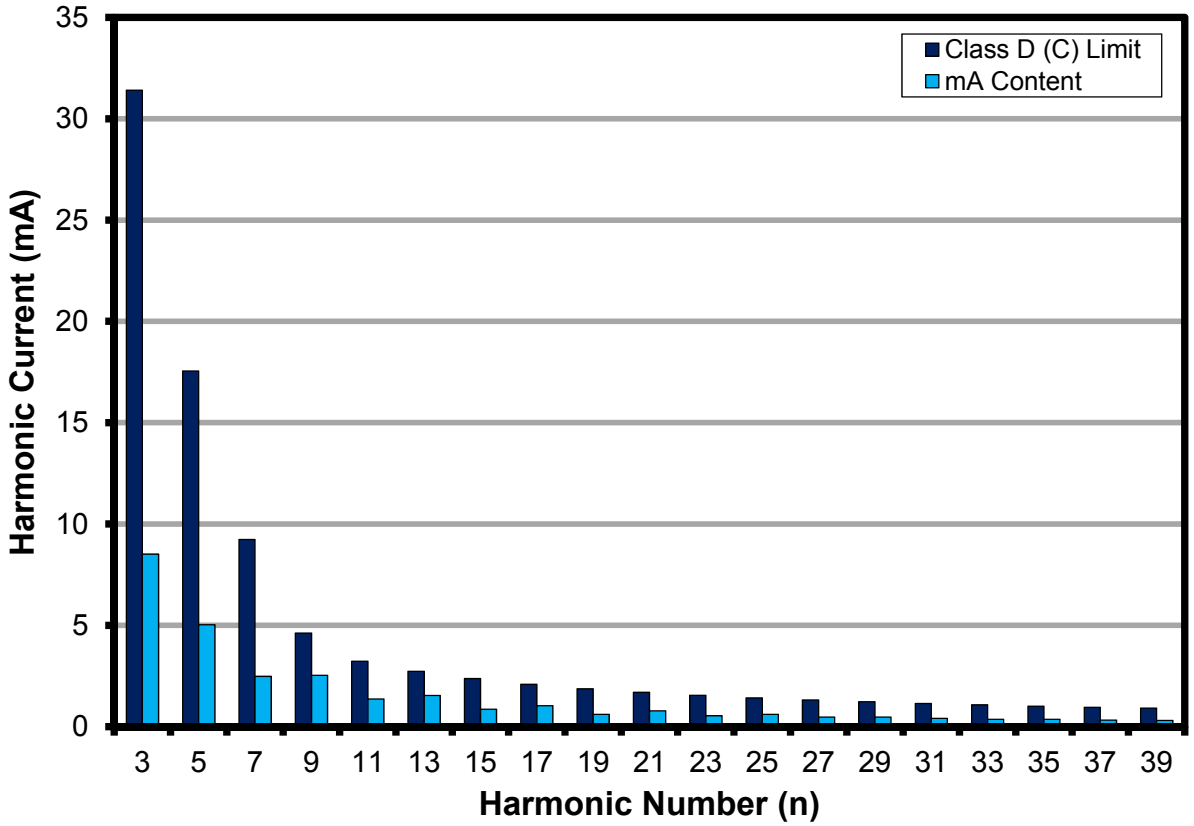

Figure 17 – 69 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.

9.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient, and 50 Hz line frequency.

9.6.1 Test Data, 63 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
176.01	51.18	8.58	0.952	23.0	62.90	110.60	6.97	6.96	81.25	1.61
180.05	50.04	8.55	0.949	23.3	62.90	110.60	6.97	6.96	81.49	1.58
220.08	41.97	8.45	0.914	26.0	62.80	110.60	6.96	6.95	82.41	1.49
230.14	40.51	8.43	0.904	26.4	62.80	110.60	6.96	6.95	82.60	1.47
265.12	36.69	8.40	0.864	27.0	62.80	110.60	6.96	6.95	82.84	1.44

9.6.2 Test Data, 66 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
176.00	53.74	9.03	0.954	23.03	66.20	110.60	7.33	7.32	81.21	1.70
180.04	52.53	9.00	0.952	23.28	66.20	110.50	7.33	7.32	81.43	1.67
220.08	43.89	8.88	0.919	25.96	66.10	110.60	7.32	7.31	82.44	1.56
230.13	42.34	8.86	0.909	26.45	66.10	110.60	7.32	7.31	82.64	1.54
265.11	38.23	8.83	0.871	27.13	66.10	110.60	7.32	7.31	82.90	1.51

9.6.3 Test Data, 69 V LED Load

Input Measurement					Load Measurement			Calculation		
V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	P_{CAL} (W)	Efficiency (%)	Loss (W)
176.00	55.95	9.416	0.956	23.11	69.00	110.50	7.64	7.62	81.14	1.78
180.04	54.70	9.391	0.954	23.29	69.00	110.50	7.63	7.62	81.25	1.76
220.08	45.55	9.253	0.923	25.86	68.90	110.50	7.63	7.61	82.46	1.62
230.13	43.92	9.230	0.913	26.47	68.90	110.50	7.63	7.61	82.67	1.60
265.11	39.55	9.198	0.877	26.99	68.90	110.50	7.63	7.61	82.95	1.57

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9.6.4 230 VAC 50 Hz, 63 V LED Load Harmonics Data

nth Order	mA Content	Base Limit mA/W	Actual Limit	Remarks
1	39.16			
3	7.70	3.40000	28.6450	Pass
5	4.70	1.90000	16.0075	Pass
7	2.27	1.00000	8.4250	Pass
9	2.37	0.50000	4.2125	Pass
11	1.25	0.35000	2.9488	Pass
13	1.58	0.29615	2.4951	Pass
15	0.80	0.25667	2.1624	Pass
17	1.03	0.22647	1.9080	Pass
19	0.65	0.20263	1.7072	Pass
21	0.78	0.18333	1.5446	Pass
23	0.55	0.16739	1.4103	Pass
25	0.62	0.15400	1.2975	Pass
27	0.52	0.14259	1.2013	Pass
29	0.50	0.13276	1.1185	Pass
31	0.45	0.12419	1.0463	Pass
33	0.40	0.11667	0.9829	Pass
35	0.39	0.11000	0.9268	Pass
37	0.34	0.10405	0.8767	Pass
39	0.33	0.09872	0.8317	Pass

9.6.5 230 VAC 50 Hz, 66 V LED Load Harmonics Data

nth Order	mA Content	Base Limit mA/W	Actual Limit	Remarks
1	40.93			
3	8.11	3.40000	30.1104	Pass
5	4.89	1.90000	16.8264	Pass
7	2.36	1.00000	8.8560	Pass
9	2.47	0.50000	4.4280	Pass
11	1.32	0.35000	3.0996	Pass
13	1.48	0.29615	2.6227	Pass
15	0.95	0.25667	2.2730	Pass
17	1.04	0.22647	2.0056	Pass
19	0.61	0.20263	1.7945	Pass
21	0.79	0.18333	1.6236	Pass
23	0.50	0.16739	1.4824	Pass
25	0.64	0.15400	1.3638	Pass
27	0.52	0.14259	1.2628	Pass
29	0.50	0.13276	1.1757	Pass
31	0.42	0.12419	1.0999	Pass
33	0.38	0.11667	1.0332	Pass
35	0.36	0.11000	0.9742	Pass
37	0.31	0.10405	0.9215	Pass
39	0.31	0.09872	0.8742	Pass

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9.6.6 230 VAC 50 Hz, 69 V LED Load Harmonics Data

nth Order	mA Content	Base Limit mA/W	Actual Limit	Remarks
1	42.44			
3	8.51	3.40000	31.4058	Pass
5	5.03	1.90000	17.5503	Pass
7	2.48	1.00000	9.2370	Pass
9	2.54	0.50000	4.6185	Pass
11	1.36	0.35000	3.2330	Pass
13	1.54	0.29615	2.7356	Pass
15	0.86	0.25667	2.3708	Pass
17	1.03	0.22647	2.0919	Pass
19	0.61	0.20263	1.8717	Pass
21	0.78	0.18333	1.6935	Pass
23	0.54	0.16739	1.5462	Pass
25	0.61	0.15400	1.4225	Pass
27	0.47	0.14259	1.3171	Pass
29	0.47	0.13276	1.2263	Pass
31	0.41	0.12419	1.1472	Pass
33	0.37	0.11667	1.0777	Pass
35	0.36	0.11000	1.0161	Pass
37	0.32	0.10405	0.9611	Pass
39	0.31	0.09872	0.9119	Pass

10 Dimming Performance Data

TRIAC dimming results were taken at an input voltage of 230 VAC, 50 Hz line frequency, room temperature, and a nominal 66 V LED load.

10.1 Performance with Dimmers from China

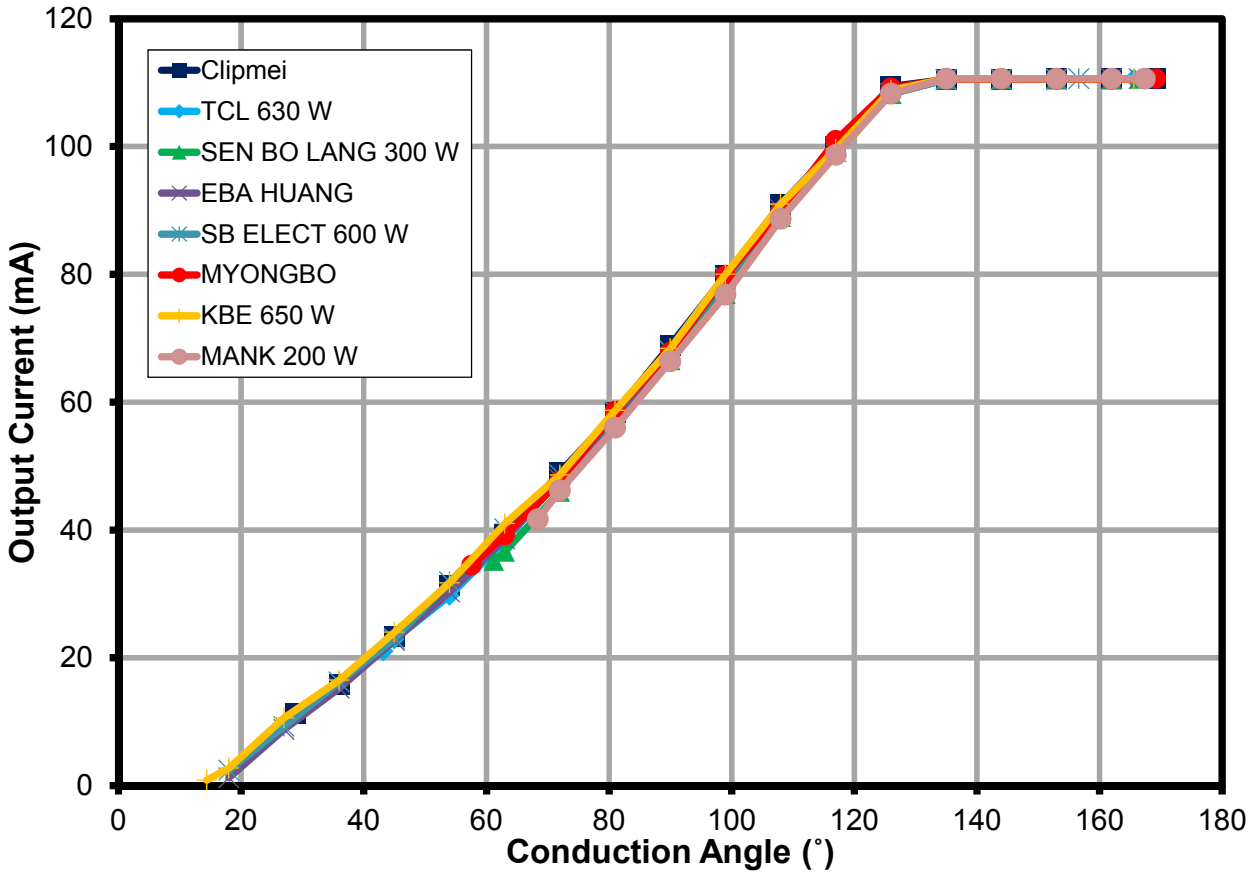

Figure 18 – China Dimmers Dimming Curve.

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Dimmer	Minimum Conduction Angle (˚)	Minimum I_{OUT} (mA)	Maximum Conduction Angle (˚)	Maximum I_{OUT} (mA)
CLIPMEI	28.8	11.28	169.2	110.6
TCL 630 W	43.2	21	165.6	110.6
SEN BO LANG 300 W	61.2	35.2	166.5	110.6
EBA HUANG	18	1.2	166.5	110.6
SB ELECT 600 W	18	2.4	156.6	110.6
MYONGBO	57.6	34.5	169.2	110.6
KBE 650 W	14.4	0.87	165.6	110.6
MANK 200 W	68.4	41.7	167.4	110.6

Figure 19 – China Dimmers Minimum and Maximum Dimming Characteristic.

10.2 Performance with Dimmers from Germany

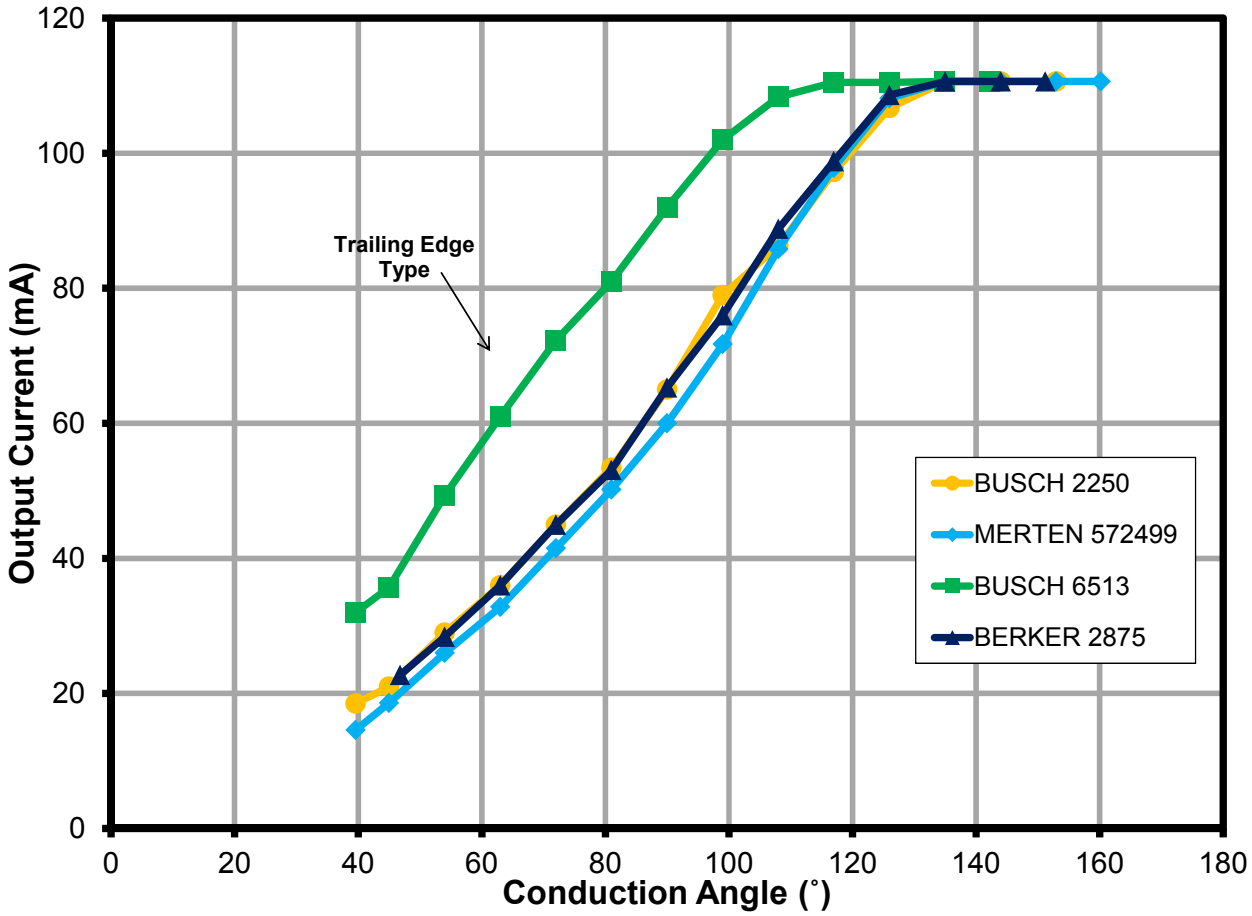

Figure 20 – German Dimmers Dimming Curve.

Dimmer	Minimum Conduction Angle (˚)	Minimum I_{OUT} (mA)	Maximum Conduction Angle (˚)	Maximum I_{OUT} (mA)
BUSCH 2250	39.6	18.5	153	110.6
MERTEN 572499	39.6	14.57	160.2	110.6
BUSCH 6513	39.6	32	142.2	110.6
BERKER 2875	46.8	22.75	151.2	110.6

Figure 21 – German Dimmers Minimum and Maximum Dimming Characteristics.

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10.3 Minimum Dimming Waveforms

The following waveforms were taken with the dimmer at low dim position and with the LED Load still conducting.

Input: 230 VAC, 50 Hz (Agilent 6812B AC Source)
Load: 66 V LED Load

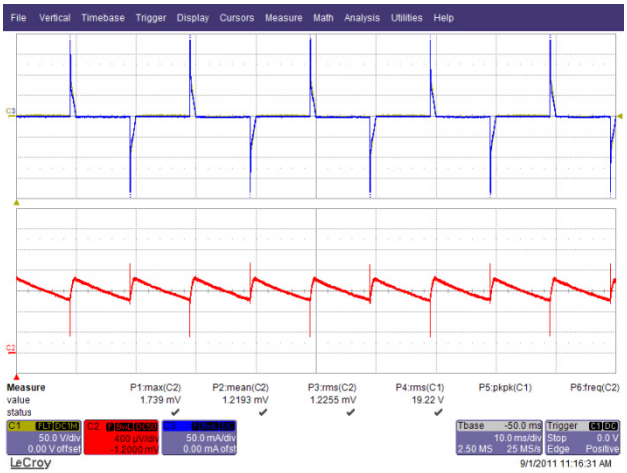

Figure 22 – Dimmer: EBA HUANG.
Conduction Angle: 18˚.
I_{OUT}: 1.2 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 400 µA / div., 10 ms / div.

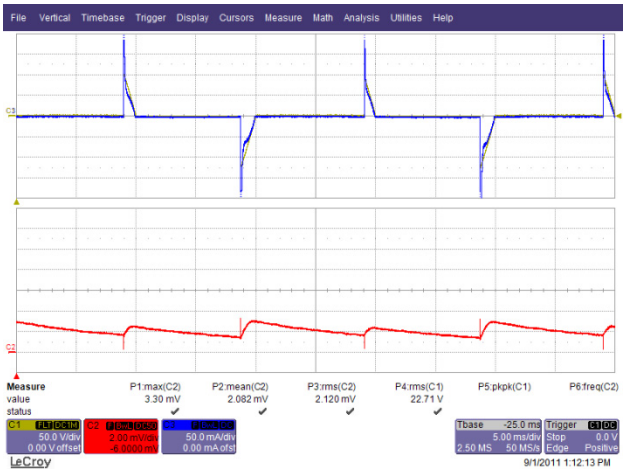

Figure 23 – Dimmer: KBE 650 W.
Conduction Angle: 18˚.
I_{OUT}: 2 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 2 mA / div., 5 ms / div.

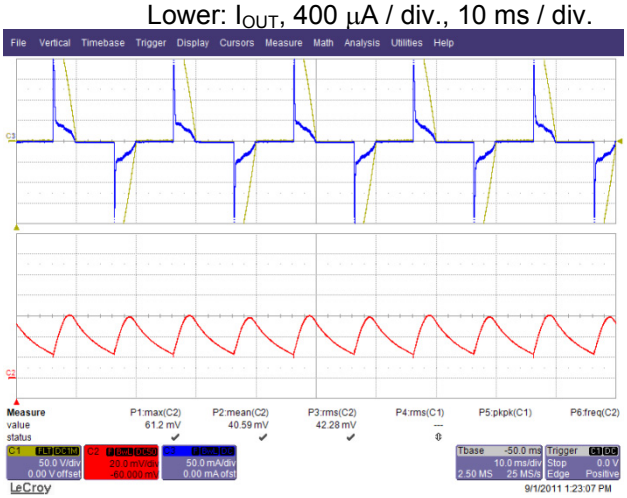

Figure 24 – Dimmer: MANK 200 W.
Conduction Angle: 68.4˚.
I_{OUT}: 45 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 10 ms / div.

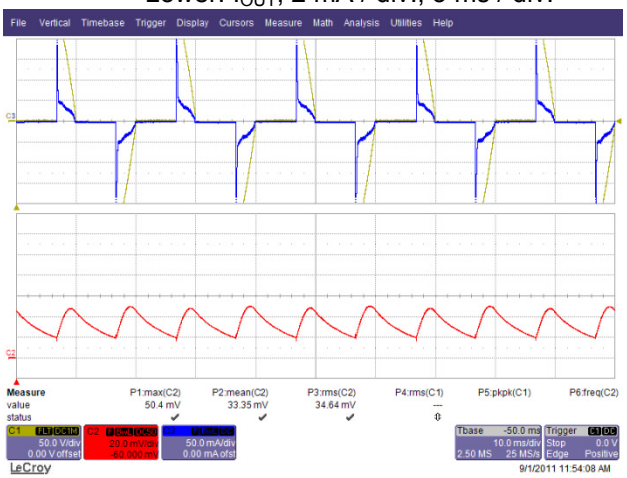

Figure 25 – Dimmer: MYONGBO.
Conduction Angle: 57.6˚.
I_{OUT}: 33 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 10 ms / div.

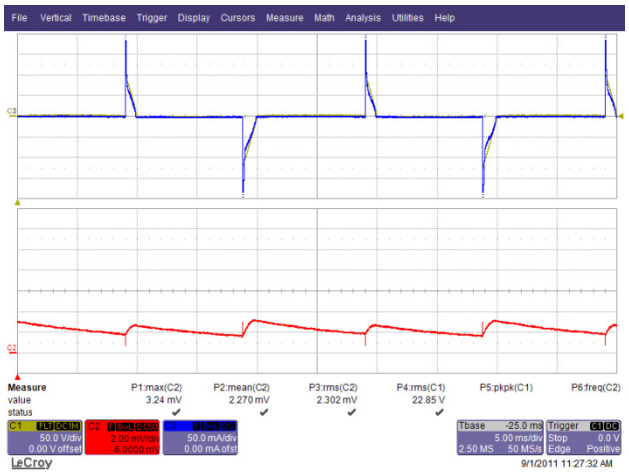

Figure 26 – Dimmer: SB ELECT 600 W.
Conduction Angle: 18˚.
I_{OUT}: 2 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 2 mA / div., 5 ms / div.

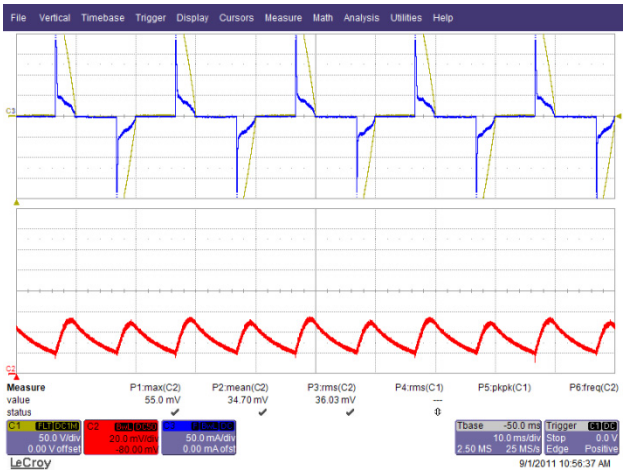

Figure 27 – Dimmer: SEN BO LANG 300 W.
Conduction Angle: 61.2˚.
I_{OUT}: 35 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 10 ms / div.

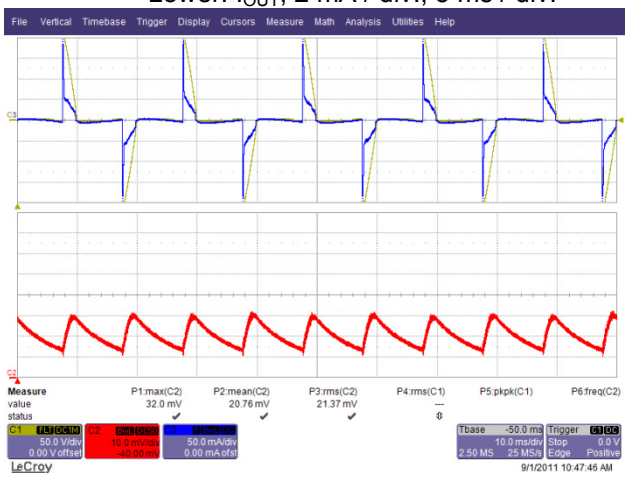

Figure 28 – Dimmer: TCL 630 W.
Conduction Angle: 28.8˚.
I_{OUT}: 21 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 10 mA / div., 10 ms / div.

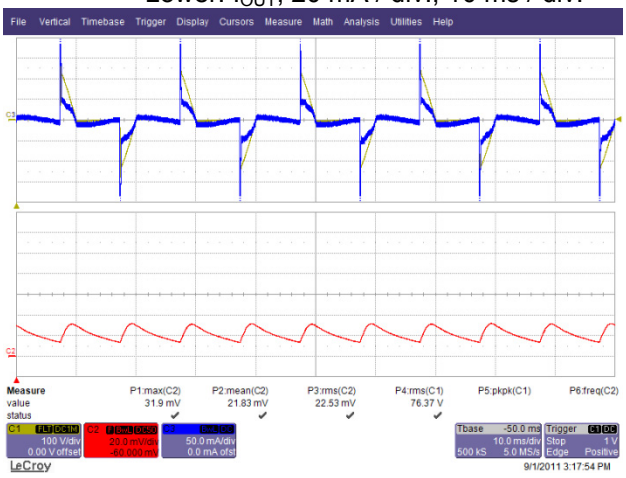

Figure 29 – Dimmer: BERKER 2875.
Conduction Angle: 47˚.
I_{OUT}: 22 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 10 ms / div.

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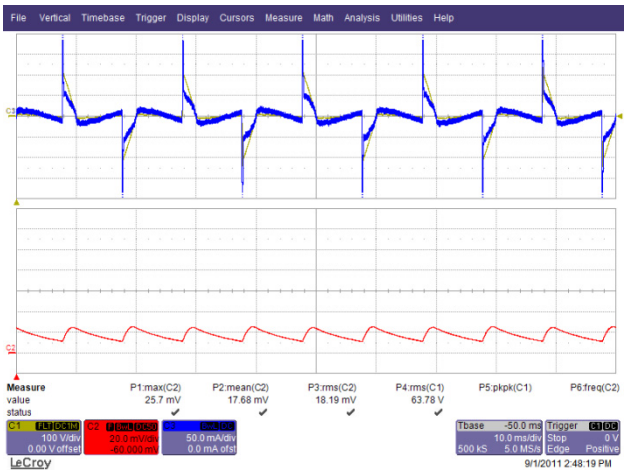

Figure 30 – Dimmer: BUSCH 2250.
Conduction Angle: 40˚.
I_{OUT}: 18 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 5 ms / div.

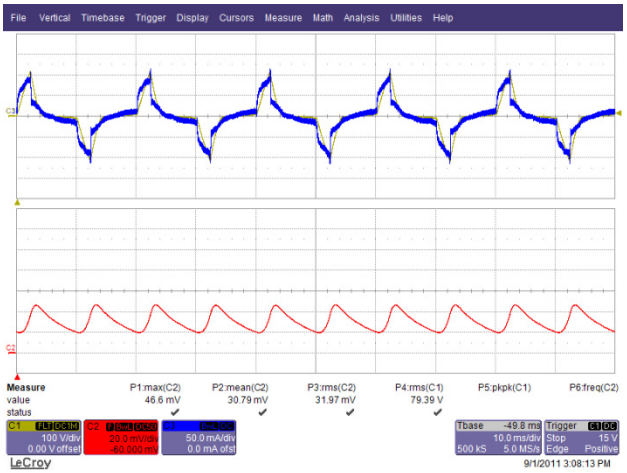

Figure 31 – Dimmer: BUSCH 6513.
Conduction Angle: 39˚.
I_{OUT}: 31 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 20 mA / div., 10 ms / div.

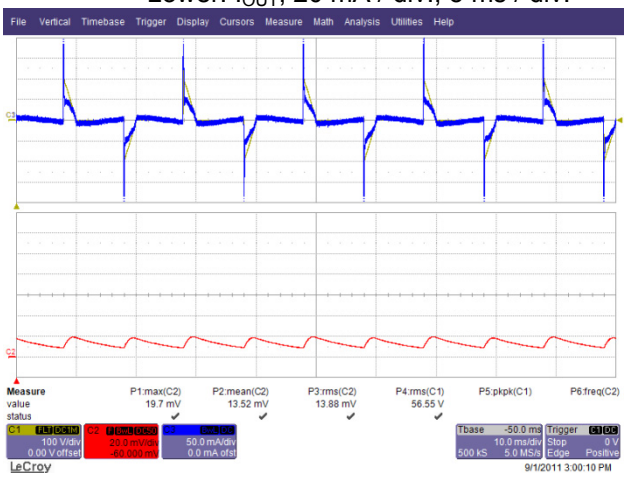

Figure 32 – Dimmer: MERTEN 572499.
Conduction Angle: 40˚.
I_{OUT}: 14 mA.
Upper: V_{IN}, 50 V / div., I_{IN}, 50 mA / div.
Lower: I_{OUT}, 10 mA / div., 10 ms / div.

11 Thermal Performance

Images captured after running for >30 minutes at room temperature (25 °C), open frame for the conditions specified.

11.1 Non-Dimming V_{IN} = 230 VAC, 50 Hz, 66 V LED Load

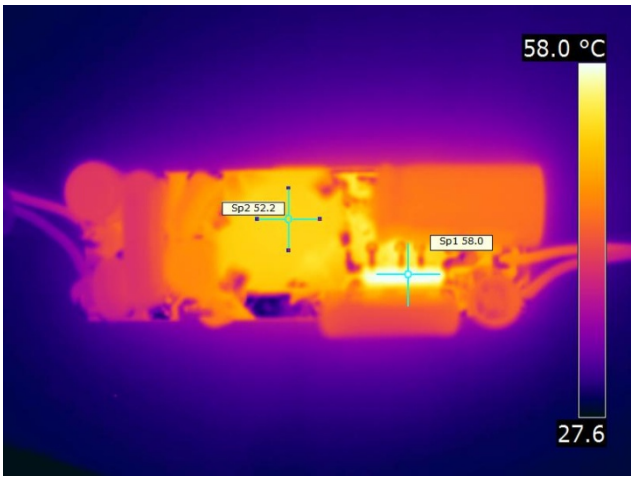

Figure 33 – Top Side.

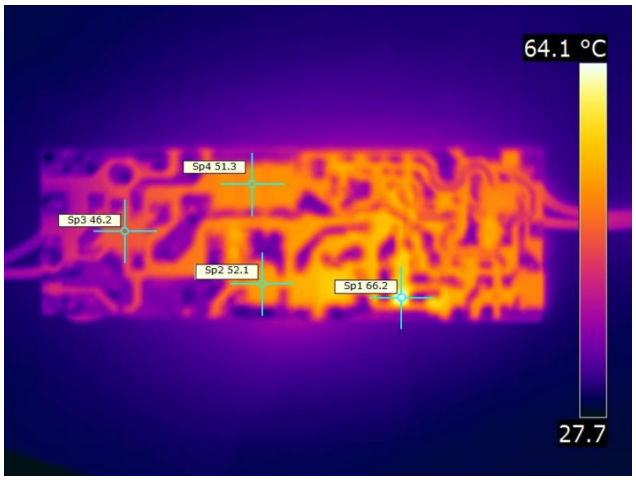

Figure 34 – Bottom Side.

11.2 Dimming V_{IN} = 230 VAC 50 Hz, 90˚ Conduction Angle, 66 V LED Load

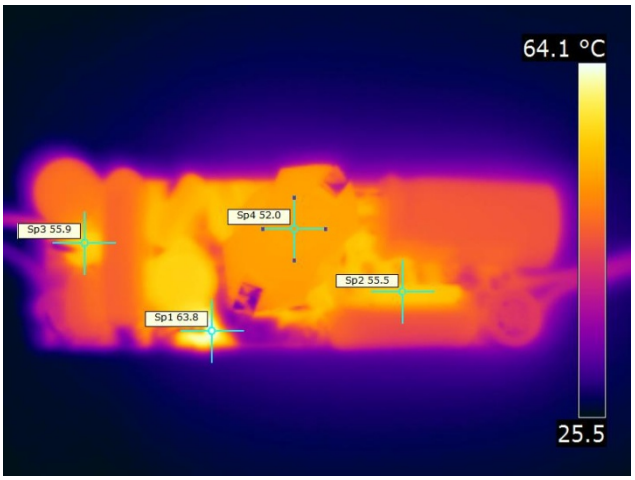

Figure 35 – Top Side.

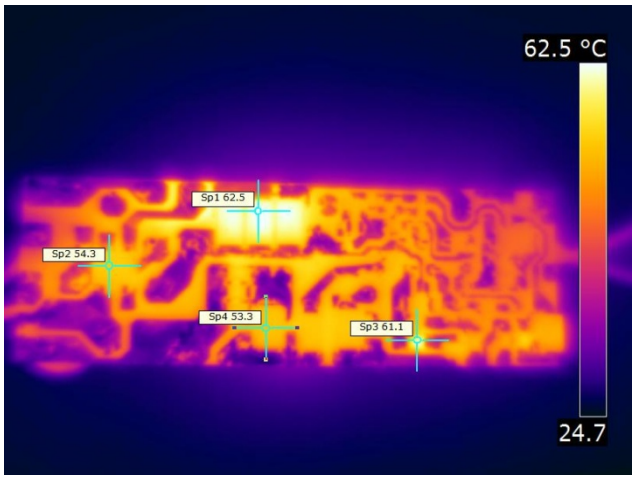

Figure 36 – Bottom Side.

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11.3 Dimming V_{IN} = 265 VAC 50 Hz, 90˚ Conduction Angle, 66 V LED Load

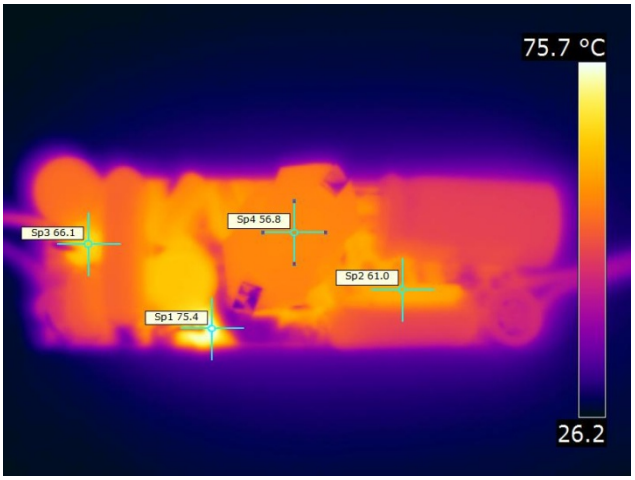

Figure 37 – Top Side.

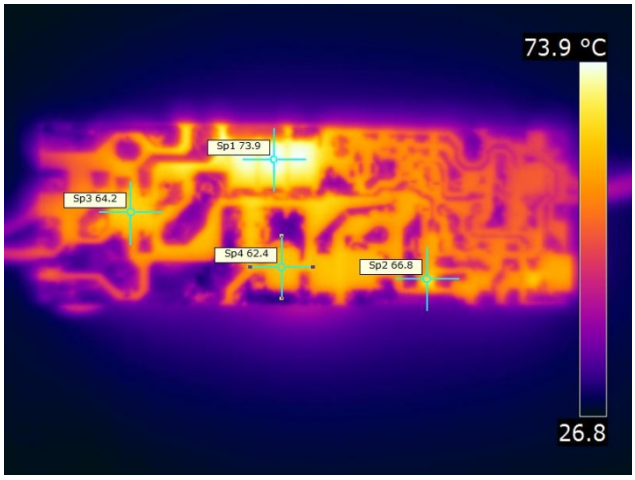

Figure 38 – Bottom Side.

12 Waveforms

12.1 Input Line Voltage and Current without Dimmer

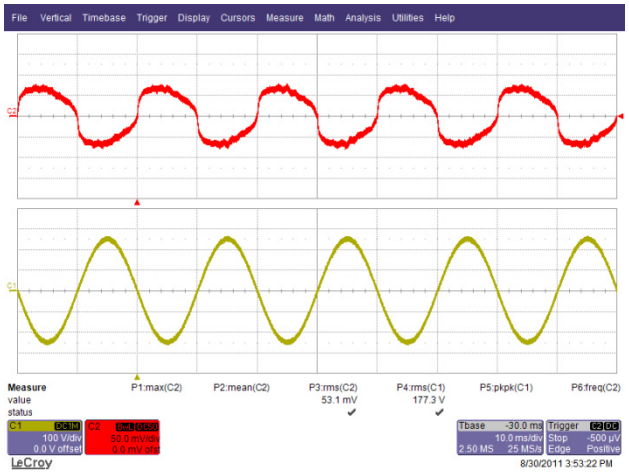

Figure 39 – 176 VAC, Full Load.
Upper: I_{IN}, 50 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

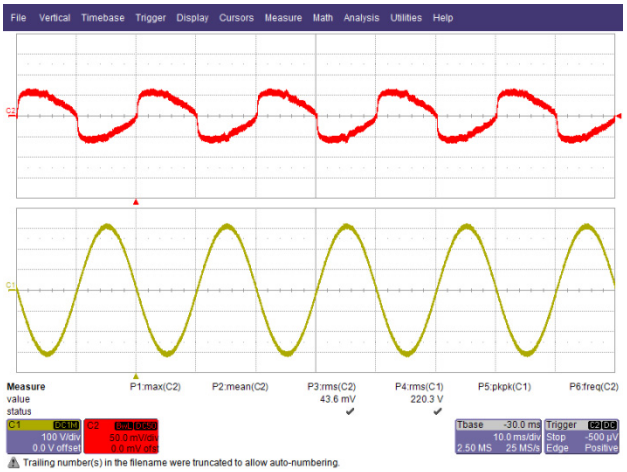

Figure 40 – 220 VAC, Full Load.
Upper: I_{IN}, 50 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

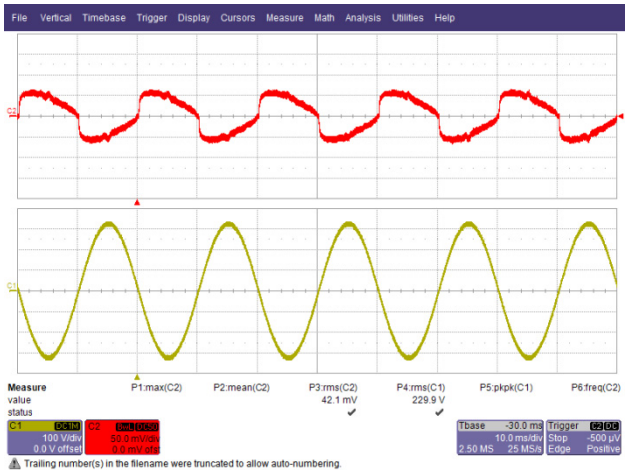

Figure 41 – 230 VAC, Full Load.
Upper: I_{IN}, 50 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

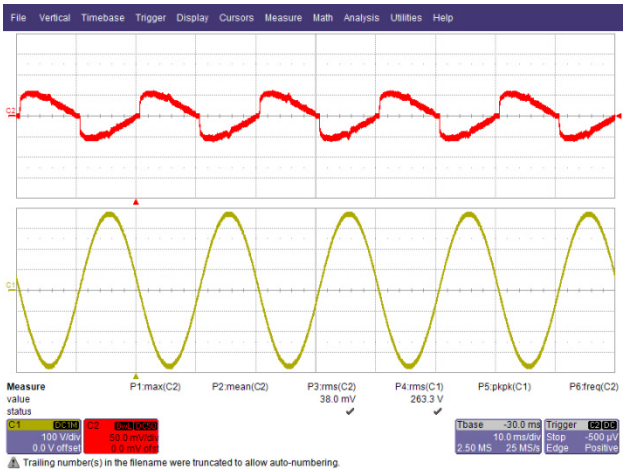

Figure 42 – 265 VAC, Full Load.
Upper: I_{IN}, 50 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

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12.2 Input Line Voltage and Current During Dimming

12.2.1 Dimmer: CLIPMEI-CHINA

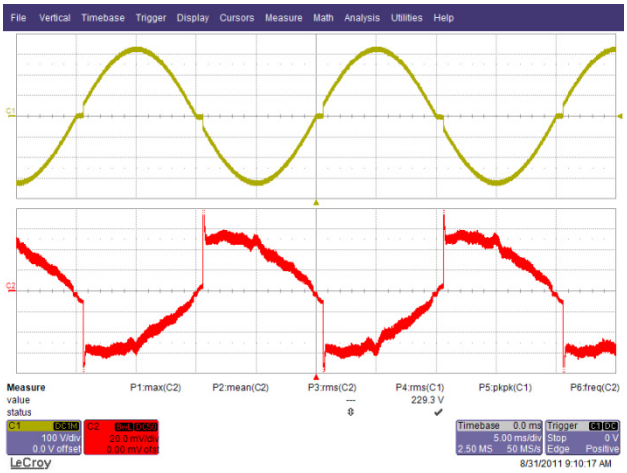

Figure 43 – 230 VAC, 50 Hz 169.2˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 20 mA, 5 ms / div.

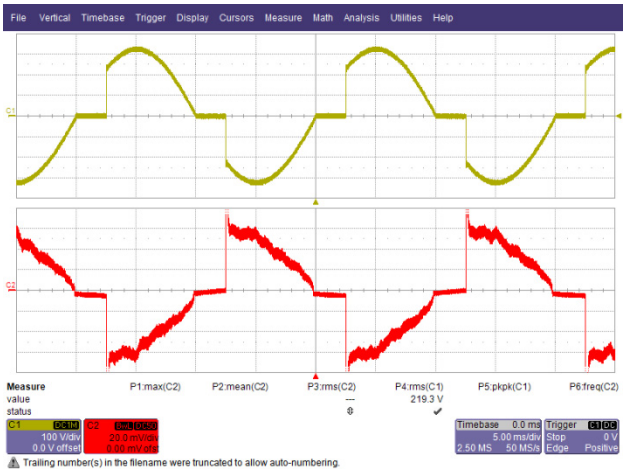

Figure 44 – 230 VAC, 50 Hz 135˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 20 mA, 5 ms / div.

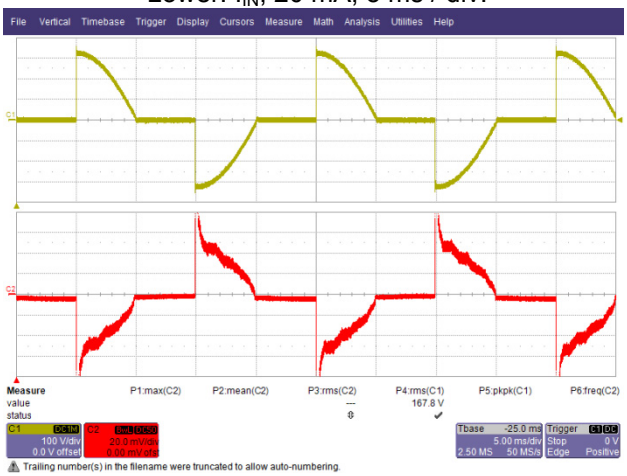

Figure 45 – 230 VAC, 50 Hz 90˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 20 mA, 5 ms / div.

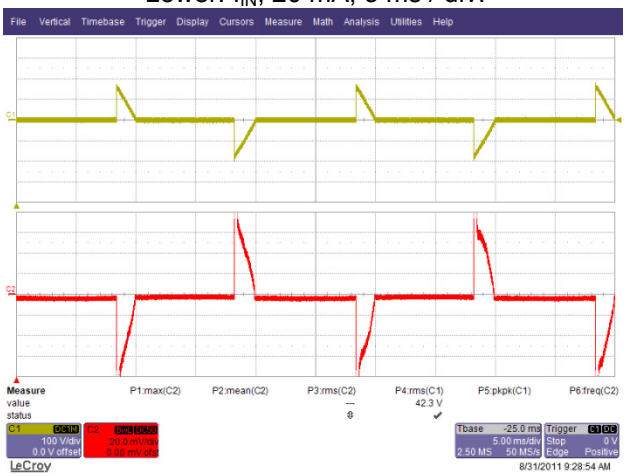

Figure 46 – 230 VAC, 50 Hz 28.8˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 20 mA, 5 ms / div.

12.3 Output Current at Normal Operation

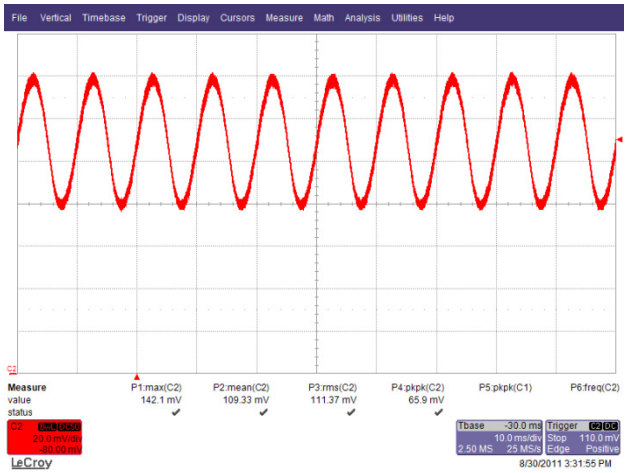

Figure 47 – 176 VAC, Full Load.
I_{OUT}, 20 mA / div.

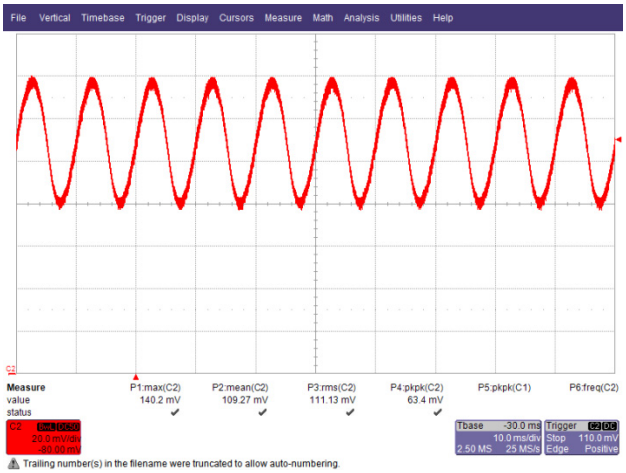

Figure 48 – 220 VAC, Full Load.
I_{OUT}, 20 mA / div.

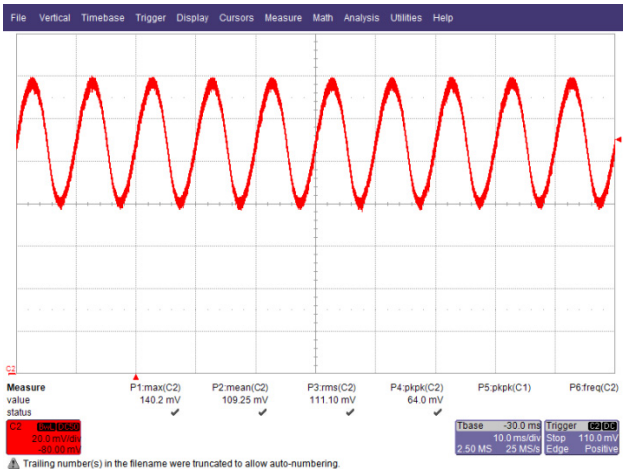

Figure 49 – 230 VAC, Full Load.
I_{OUT}, 20 mA / div.

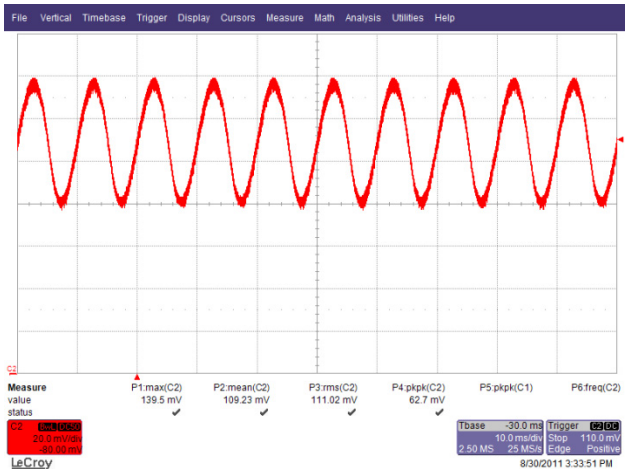

Figure 50 – 265 VAC, Full Load.
I_{OUT}, 20 mA / div.

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12.4 Output Current During Dimming Operation

12.4.1 Dimmer: CLIPMEI-CHINA

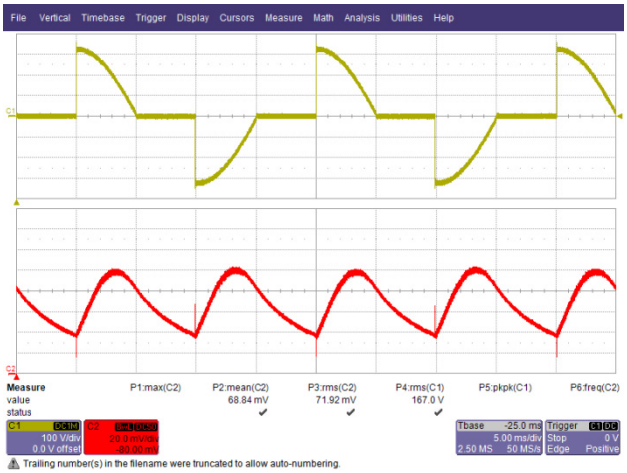

Figure 51 – 230 VAC, 50 Hz 90 ˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 20 mA, 5 ms / div.

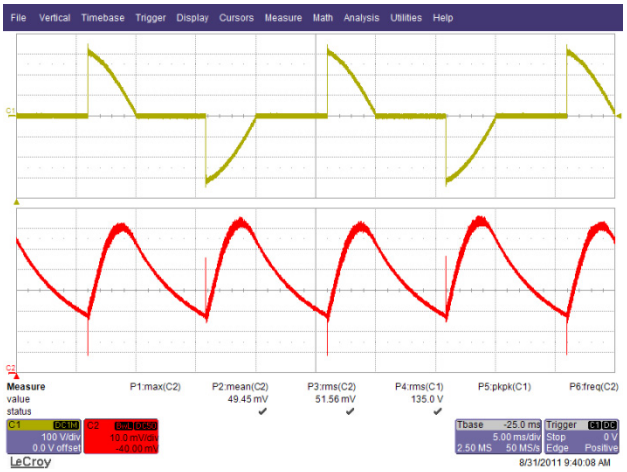

Figure 52 – 230 VAC, 50 Hz 72˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 10 mA, 5 ms / div.

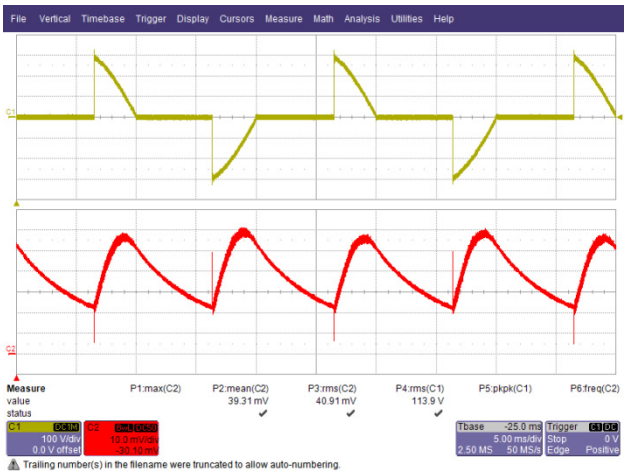

Figure 53 – 230 VAC, 50 Hz 60˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 10 mA, 5 ms / div.

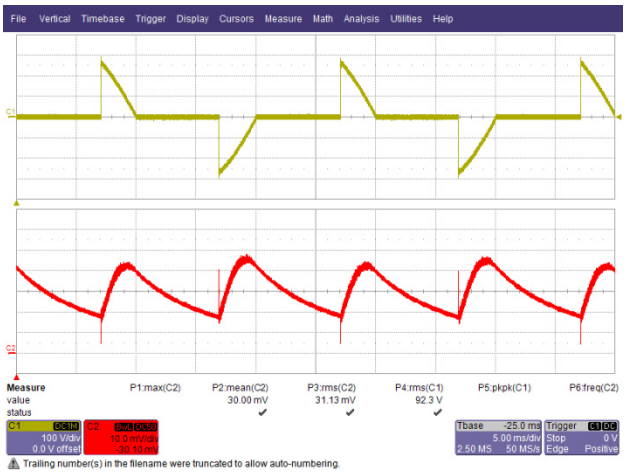

Figure 54 – 230 VAC, 50 Hz 52.2˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 10 mA, 5 ms / div.

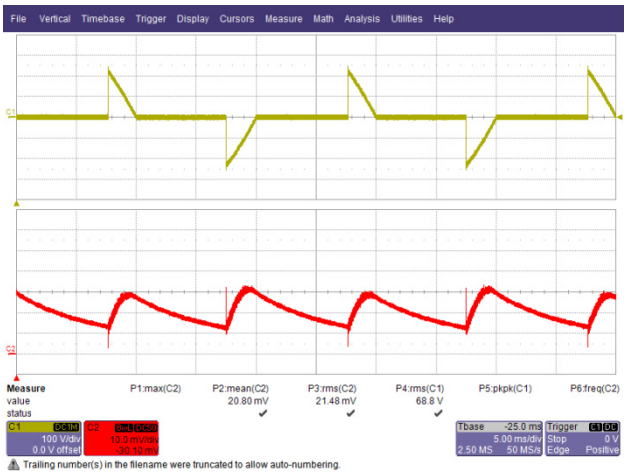

Figure 55 – 230 VAC, 50 Hz 43.2˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 10 mA, 5 ms / div.

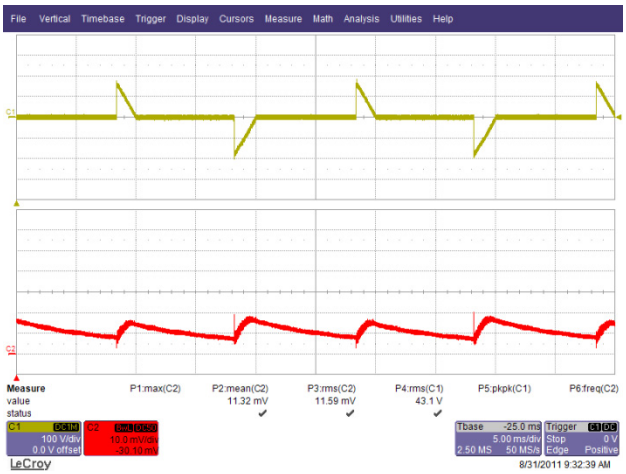

Figure 56 – 230 VAC, 50 Hz 28.8˚ Conduction Angle.
Upper: V_{IN}, 100 V / div.
Lower: I_{IN}, 10 mA, 5 ms / div.

12.5 Drain Voltage and Current at Normal Operation

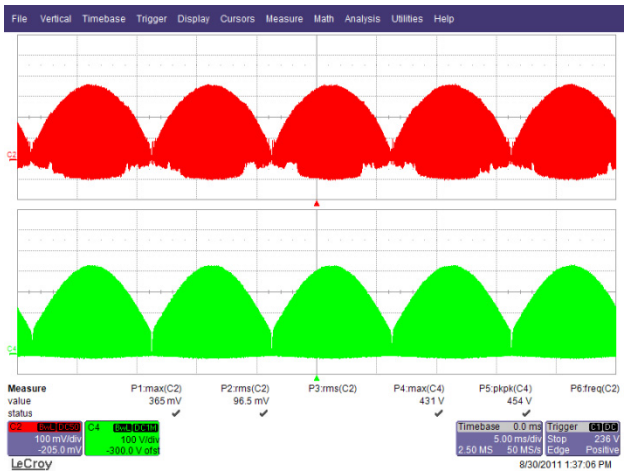

Figure 57 – 176 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

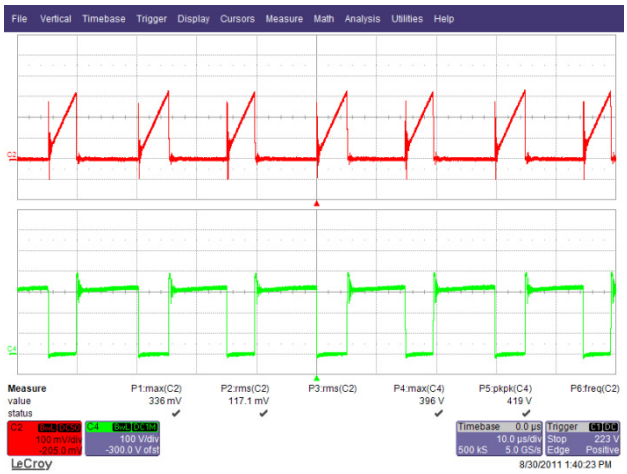

Figure 58 – 176 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 µs / div.

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Figure 59 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

Figure 60 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 μs / div.

12.6 Start-Up Drain Voltage and Current

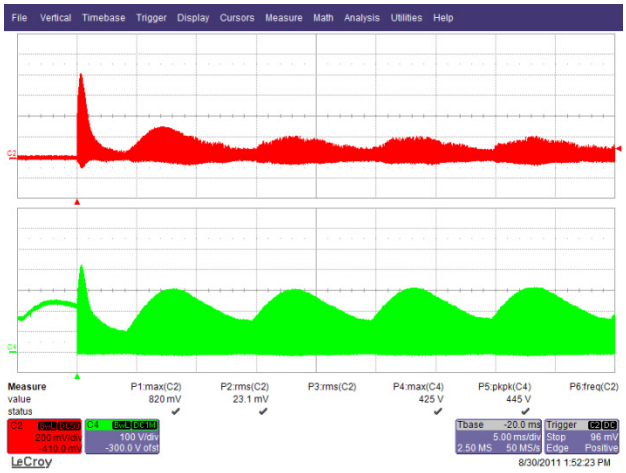

Figure 61 – 176 VAC, 50 Hz.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 5 ms / div.

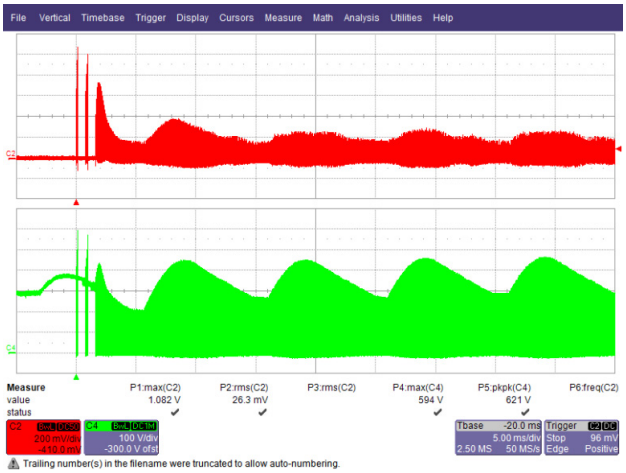

Figure 62 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 200 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 5 ms / div.

12.7 Output Diode PIV

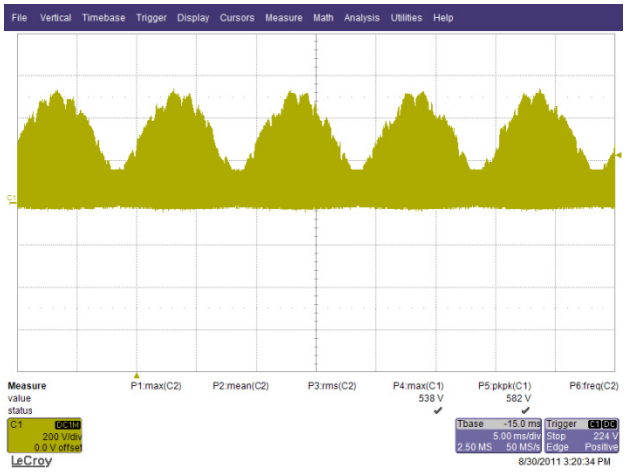

Figure 63 – 265 VAC, 50 Hz Normal Operation.
PIV: 200 V, 5 ms / div.

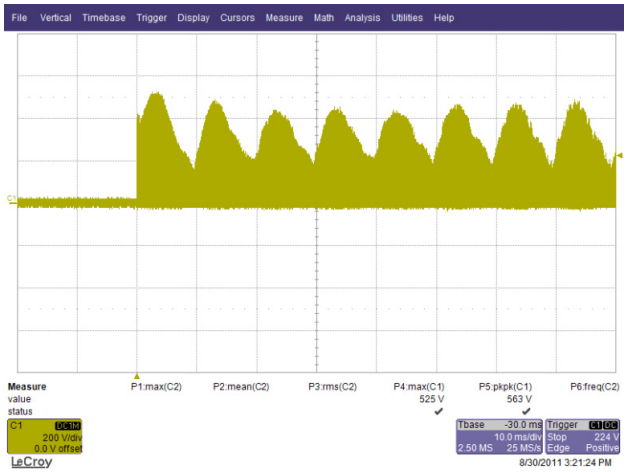

Figure 64 – 265 VAC, 50 Hz Start-up.
PIV: 200 V, 5 ms / div.

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12.8 Output Current/Voltage Rise and Fall

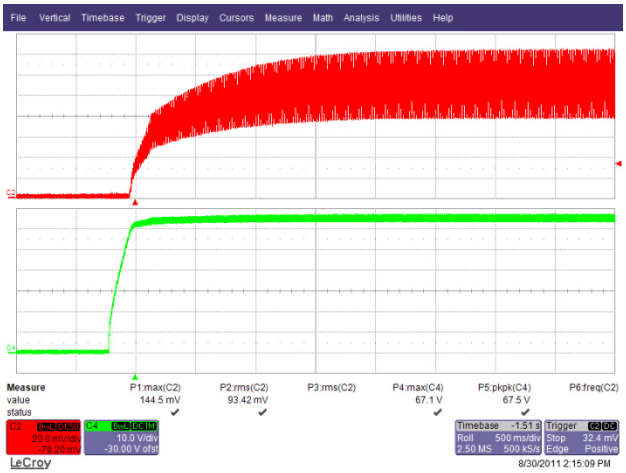

Figure 65 – 176 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V, 500 ms / div.

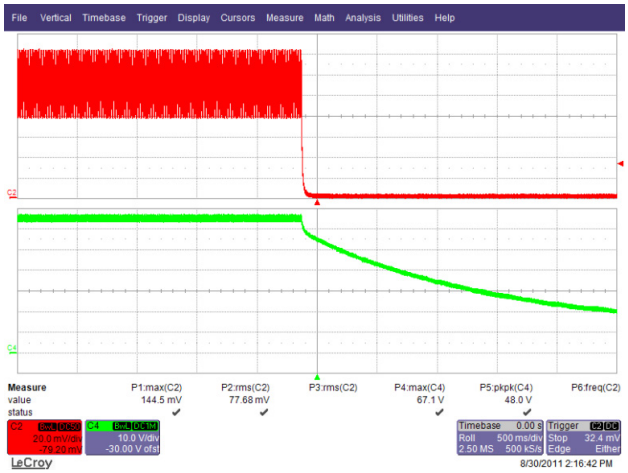

Figure 66 – 176 VAC Output Fall.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V, 500 ms / div.

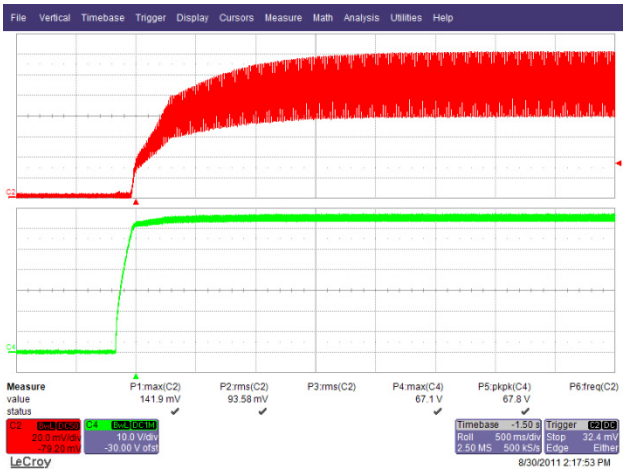

Figure 67 – 265 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V, 500 ms / div.

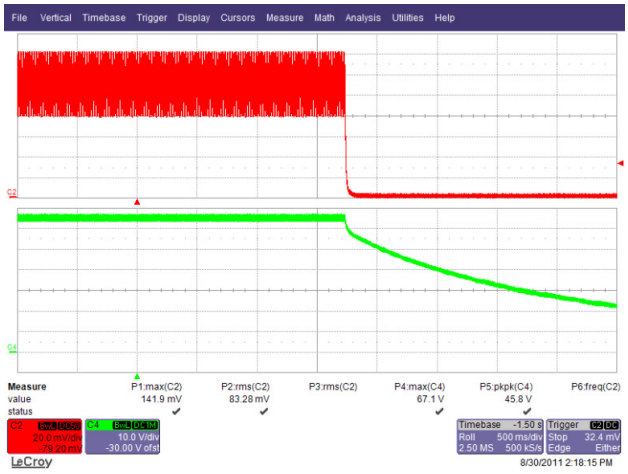

Figure 68 – 265 VAC Output Fall.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 10 V, 500 ms / div.

12.9 Output Current and Drain Voltage During Output Short Condition

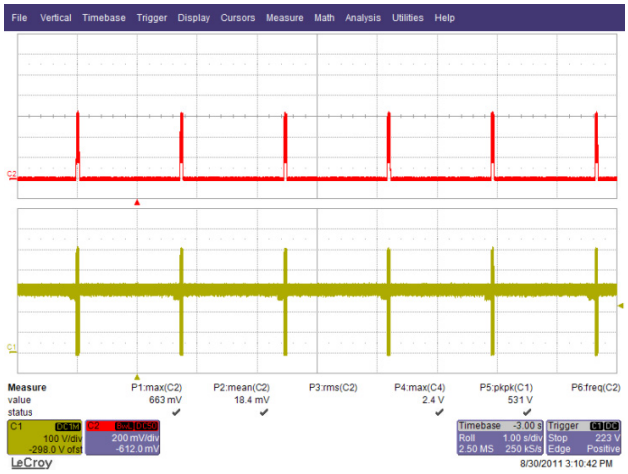

Figure 69 – 230 VAC, 50 Hz Output Short Condition.
Upper: I_{OUT}, 200 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 1 s / div.

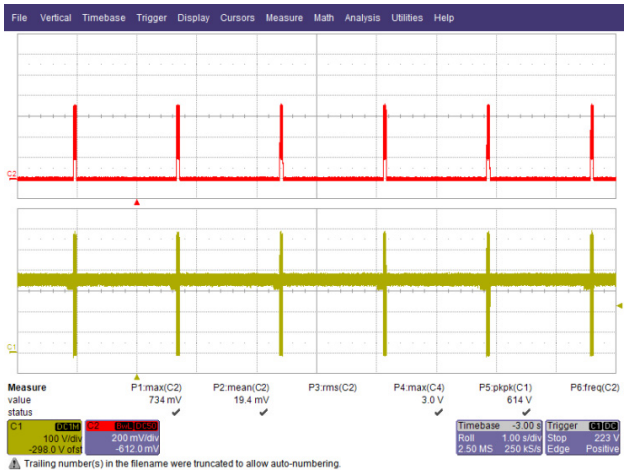

Figure 70 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{OUT}, 200 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 1 s / div.

12.10 Open Load Output Voltage

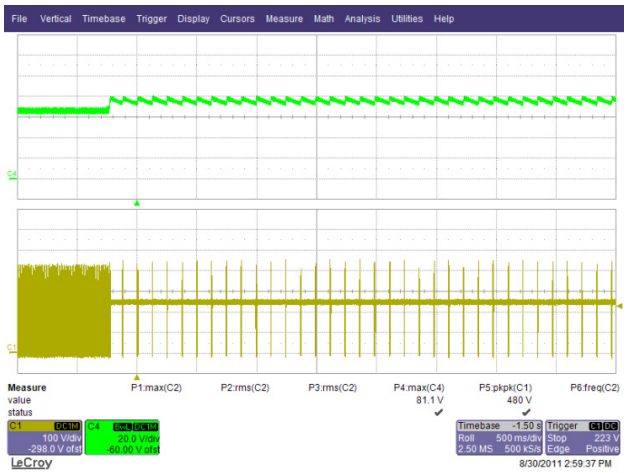

Figure 71 – 176 VAC, 50 Hz Open Load Characteristic.
Upper: V_{OUT}, 10 V / div., 1 s / div.
Lower: V_{DRAIN}, 100 V / div., 1 s / div.

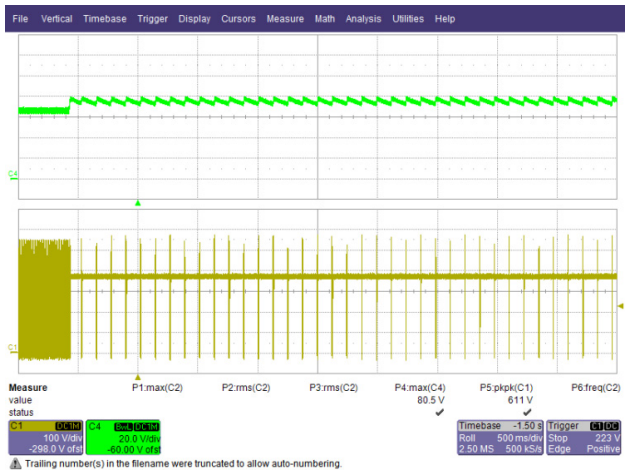

Figure 72 – 265 VAC, 50 Hz Open Load Characteristic.
Upper : V_{OUT}, 10 V / div., 1 s / div.
Lower: V_{DRAIN}, 100 V / div., 1 s / div.

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13 Conducted EMI

13.1 Test Set-up

The unit was tested using LED load (~66 V V_{OUT}) with input voltage of 230 VAC, 60 Hz at room temperature.

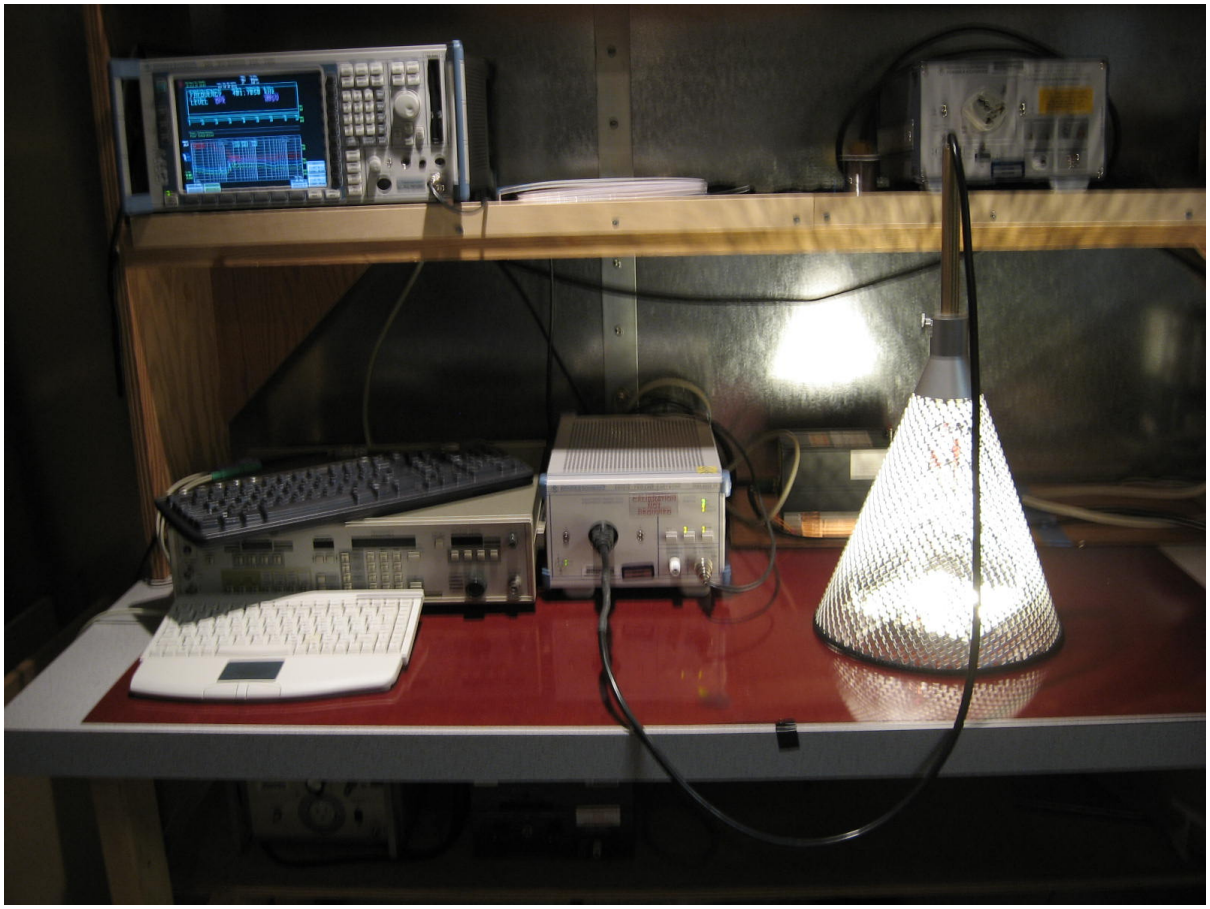
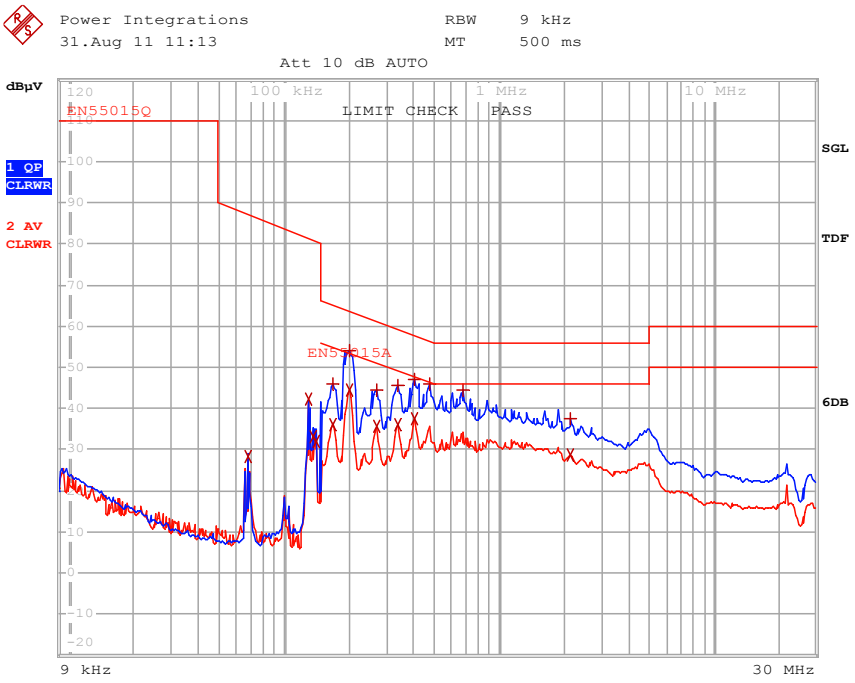


Figure 73 – EMI Test Set-up with the Unit and LED Load Placed Inside the Cone.

13.2 Test Result



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	67.1676282959 kHz	28.21	L1 gnd	
2	Average	129.530094744 kHz	42.22	N gnd	
2	Average	136.137431366 kHz	33.05	N gnd	
2	Average	140.262531674 kHz	32.16	L1 gnd	
1	Quasi Peak	169.02375452 kHz	45.80	N gnd	-19.20
2	Average	169.02375452 kHz	36.07	L1 gnd	-18.92
1	Quasi Peak	202.1773373 kHz	54.12	N gnd	-9.39
2	Average	202.1773373 kHz	44.63	L1 gnd	-8.88
1	Quasi Peak	269.806440381 kHz	44.59	N gnd	-16.53
2	Average	269.806440381 kHz	35.57	N gnd	-15.55
1	Quasi Peak	335.832355405 kHz	45.42	N gnd	-13.88
2	Average	335.832355405 kHz	36.16	N gnd	-13.14
1	Quasi Peak	401.705024172 kHz	46.96	N gnd	-10.85
2	Average	401.705024172 kHz	37.53	N gnd	-10.28
1	Quasi Peak	471.030732902 kHz	45.79	N gnd	-10.69
1	Quasi Peak	673.936068749 kHz	44.54	N gnd	-11.45
1	Quasi Peak	2.1588349124 MHz	37.50	N gnd	-18.49
2	Average	2.1588349124 MHz	28.73	N gnd	-17.26

Figure 74 – Conducted EMI, 66 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.

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14 Line Surge

The unit was subjected to ±2500 V 100 kHz ring wave and ±500 V Differential Surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
-2500	230	L1, L2	0	100 kHz Ring Wave (200 A)	Pass
+2500	230	L1, L2	90	100 kHz Ring Wave (200 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (200 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	0	Surge (2Ω)	Pass
+500	230	L1, L2	90	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
03-Nov-11	CA	1.0	Initial Release	Apps & Mktg

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