Design Example Report

Title	***350 W PFC Front-end Using HiperPFS™-2 PFS7328H***
Specification	90 VAC – 264 VAC Input; 385 VDC Output
Application	PFC Front End
Author	Applications Engineering Department
Document Number	DER-294
Date	June 4, 2013
Revision	1.0

Summary and Features

- Highly integrated, low component count, low-cost PFC
- Ultra-low reverse recovery loss diode (Qspeed™)
- Power Integrations eSIP low-profile controller package
- New “Cool-Pad” package reduces IC mounting hardware
  - Eliminates insulating pad/heat-spreader
- EN61000-3-2 Class-D compliant
- High PFC efficiency enables up to 80+ Platinum PC Main design
- Enhanced light load power factor (PF)
  - PF >0.9 at 20% Load and 230 VAC, 50 Hz input
  - PF >0.95 at 50% Load
- Frequency sliding maintains high efficiency across load range
  - >94.5% from 10 to 100% load (115 VAC and 230 VAC input)
- Feed forward line sense gain – maintains relatively constant loop gain over entire operating voltage range
- Excellent transient load response
- Frequency adjusted over input line voltage and load
  - Spread-spectrum across >60 kHz window simplifies EMI filtering requirements
- Integrated QSpeed switching diode reduces component count and simplifies assembly

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com

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Important Note:
All testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a PFC power supply utilizing a HiperPFS2 PFS7328H PFC controller with integrated MOSFET and switching diode. This power supply is intended as a general purpose platform that operates from universal input line voltage and provides a regulated 385 V DC output voltage and continuous output power of 350 W.

This power supply is designed to operate with forced air cooling for all conditions. It can deliver rated power at an ambient temperature of 25 ºC using forced air cooling.

This document contains the power supply specification, schematic, bill of materials, inductor documentation, printed circuit layout, and performance data.

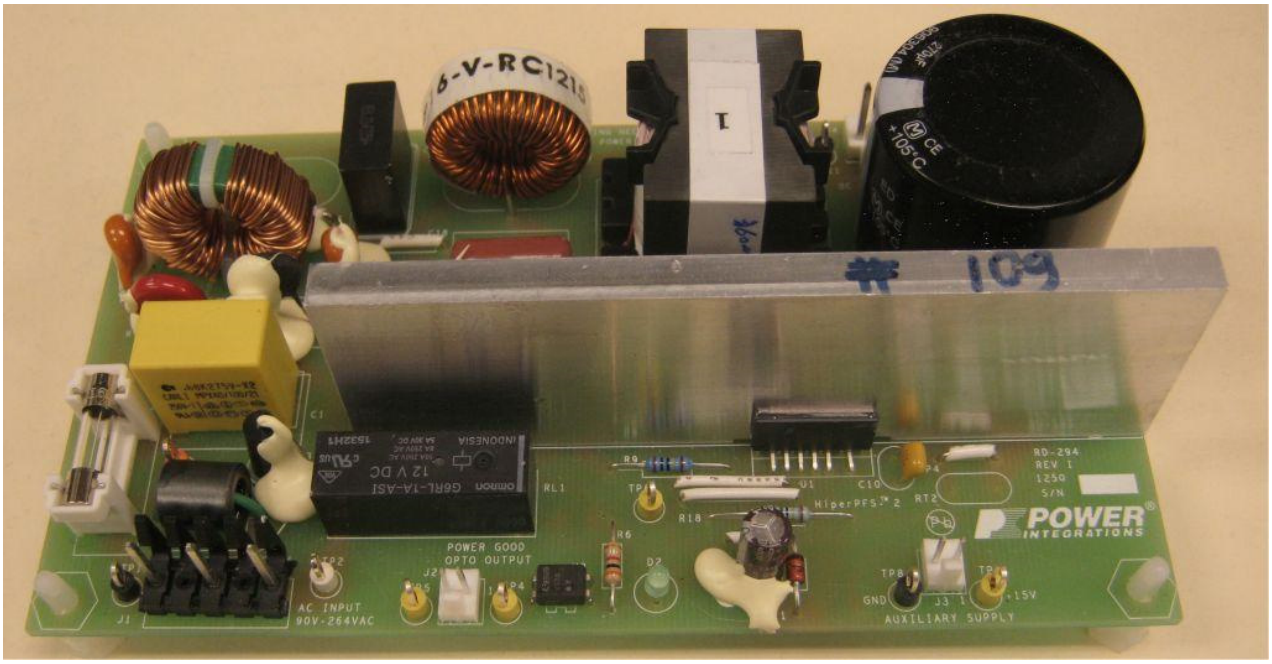

Figure 1 – Populated Circuit Board Photograph [Front View].

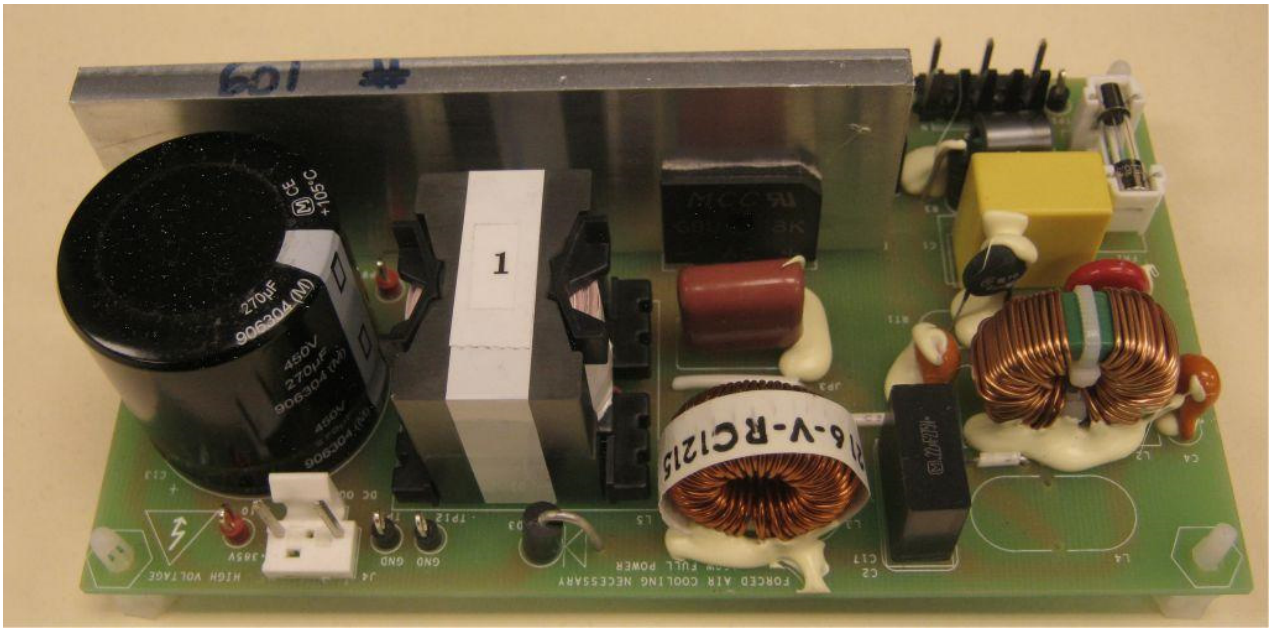

Figure 2 – Populated Circuit Board Photograph [Rear View].

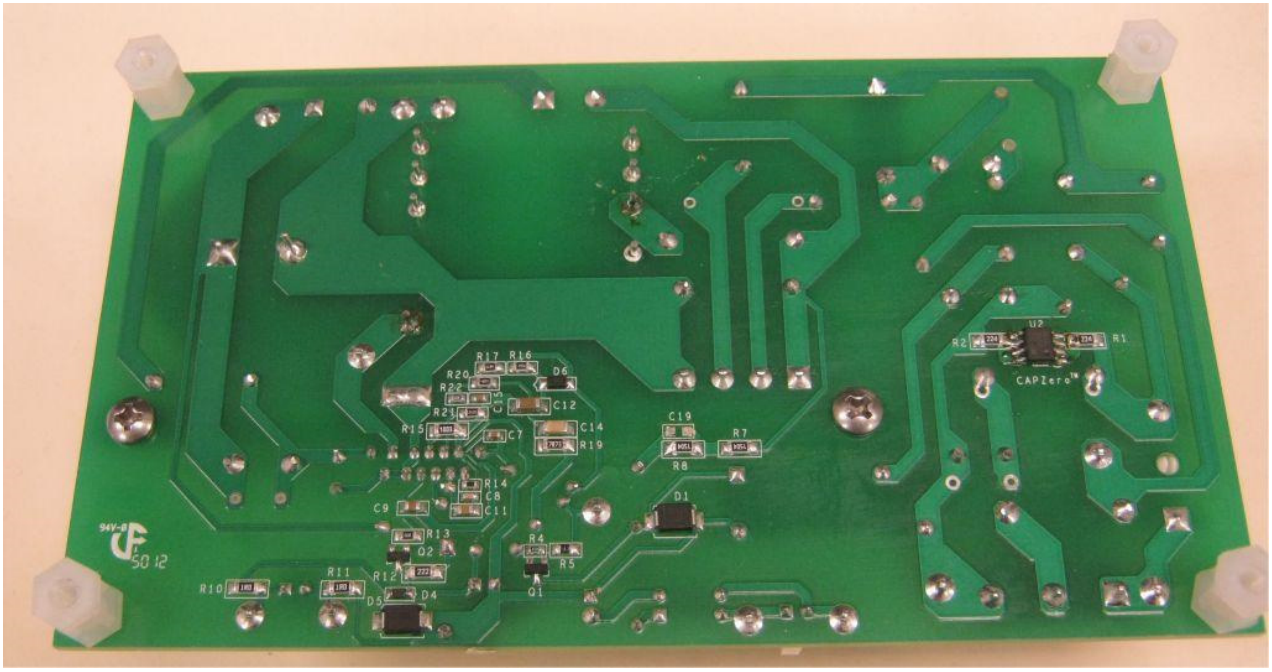

Figure 3 – Populated Circuit Board Photograph [Back View].

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		264	VAC	3 Wire
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	375	385	395	V	
Output Ripple Voltage p-p	V_{RIPPLE}			30	V	20 MHz bandwidth
Output Current	I_{OUT}		0.91		A	
Total Output Power						
Continuous Output Power	P_{OUT}		350		W	
Efficiency						
Full Load	η	94			%	Measured at P_{OUT} 25 °C
Minimum efficiency at 20, 50 and 100 % of P_{OUT}	η_{80+}	94			%	Measured at 115 VAC Input
Environmental						1.2/50us surge, IEC1000-4-5, Series impedance:
Line Surge						
Differential Mode (L1-L2)			1		kV	Differential mode: 2 Ω
Common mode (L1/L2-PE)			2		kV	Common mode: 12 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Forced convection required at T_{AMB} >25 ºC and/or V_{IN} <15 V, sea level
Auxiliary Supply Input Auxiliary Supply	V_{aux}	15		17	V	DC supply

3 Schematic

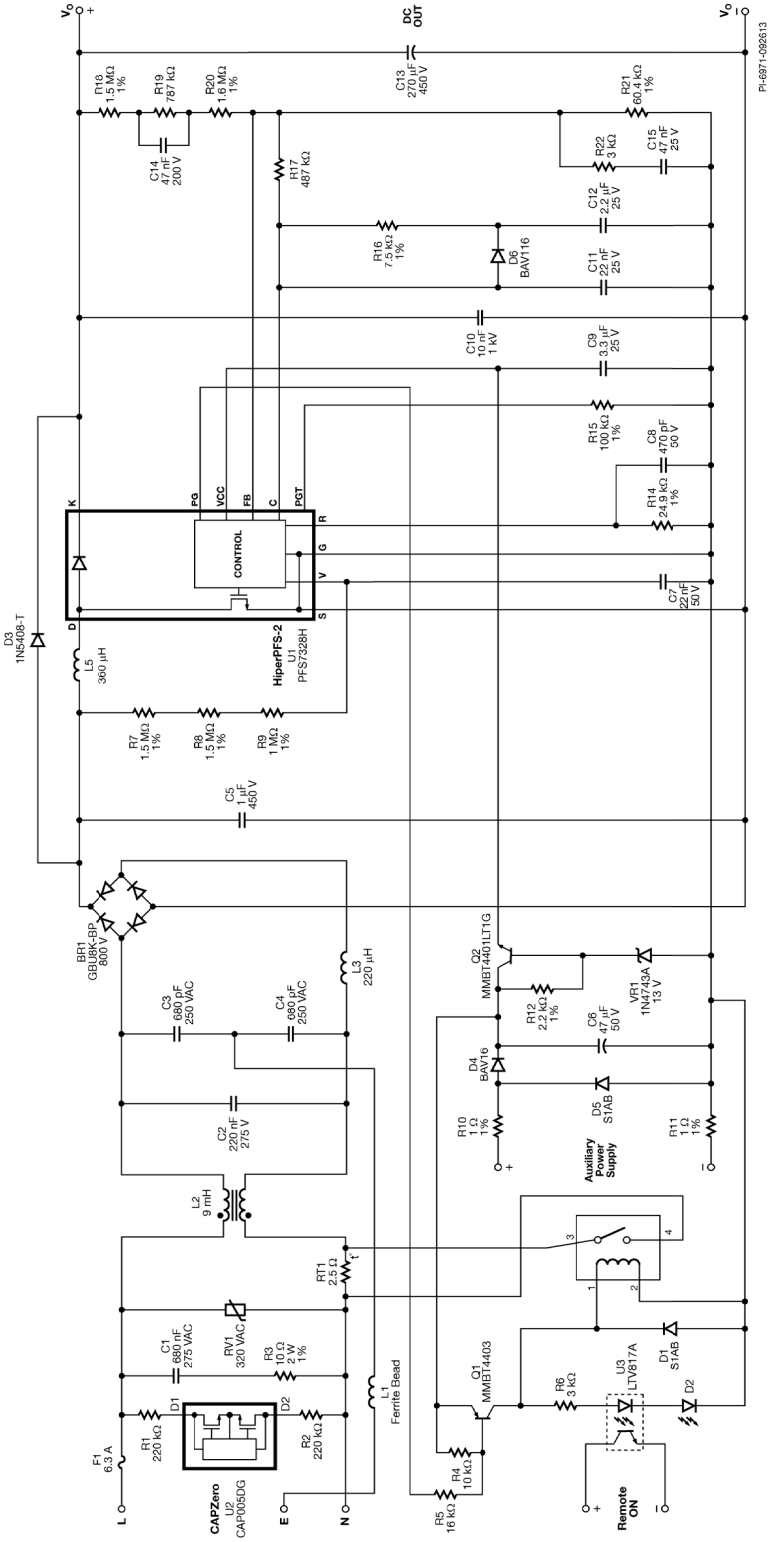

Figure 4 – PFC Circuit Schematic.

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4 Circuit Description

This PFC is designed around the Power Integrations PFS7328H Integrated PFC controller. This design is rated for a continuous output power of 350 W and provides a regulated output voltage of 385 VDC nominal, maintaining a high input power factor and overall efficiency over line and load, while remaining low in cost.

4.1 Input EMI Filter and Rectifier

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, and C4 in conjunction with inductors L1, L2 and L3, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitor C5 provides input decoupling charge storage to reduce input ripple current at the switching frequency and its harmonics.

Resistors R1, R2 and CAPZero™ IC U2 are provided to discharge the EMI filter capacitors after line voltage has been removed from the circuit, while dissipating zero power during operation.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

Only one differential inductor has been used in this design. However, there is provision on the board to configure a filter with two differential inductors, one in series with the “line” and another in series with the “neutral”.

4.2 PFS7328H Boost Converter

The boost converter stage consists of the boost inductor L5 and the PFS7328H IC U1. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

During start-up, diode D3 provides an inrush current path to the output capacitor C13, bypassing the switching inductor L5 and switch U1 in order to prevent a resonant interaction between the switching inductor and output capacitor.

NTC thermistor RT1 limits inrush current of the supply when line voltage is first applied. Thermistor RT1 is bypassed by the electro-mechanical relay RL1 after the output voltage is in regulation. R4, R5, D1 and Q1 drive relay RL1, while R6 and D2 provide visual indication that the supply is in regulation. IC U3 provides optocoupler output through connector J2.

Capacitor C10 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U1 MOSFET drain voltage overshoot after turn-off. Capacitor C9 decouples and bypasses the U1 VCC pin.

Resistor R15 programs the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD (PG) pin will go into a high-impedance state.

Resistor R14 programs the output power for either full mode, 100% of rated power [R14 = 24.9 kΩ] or efficiency mode, 80% [R14 = 49.9 kΩ] of rated power. Capacitor C8 decouples U1 R pin. For full mode, C8 is 470 pF, for efficiency mode, C8 is 1 nF.

4.3 Input Feed Forward Sense Circuit

The input voltage of the power supply is sensed by the IC U1 using resistors R7, R8 and R9. The capacitor C7 bypasses the V pin on IC U1.

4.4 Output Feedback

An output voltage resistive divider network consisting of resistors R18, R19, R20 and R21 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U1. The capacitor C14 provides fast dv/dt feedback to the U1 FB pin for undershoot and overshoot response of the PFC circuit.

Resistor R17 and capacitor C12 provide the control loop dominant pole. C11, C15 and R22 attenuate high-frequency noise.

The resistor R16 in series with capacitor C12 provides a low frequency compensation zero while diode D4 protects against error operation caused by an accidentally shorted C12.

4.5 Bias Supply Series Regulator

The PFS7328H IC requires a regulated V_{CC} supply of 12 V nominal for operation, with an absolute maximum voltage rating of 15 V. V_{CC} levels in excess of this maximum could result in failure of the IC. Resistor R12, Zener diode VR1, and transistor Q2 form a shunt regulator that prevents the supply voltage to IC U1 from exceeding 13 V. Capacitor C6 decouples the input auxiliary supply voltage to ensure reliable operation of IC U1.

Resistors R10, R11 provide filtering of the external V_{CC} voltage source and provide reverse polarity protection in conjunction with diodes D4 and D5.

The +15 V auxiliary supply is applied on connector J3.

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5 PCB Layout

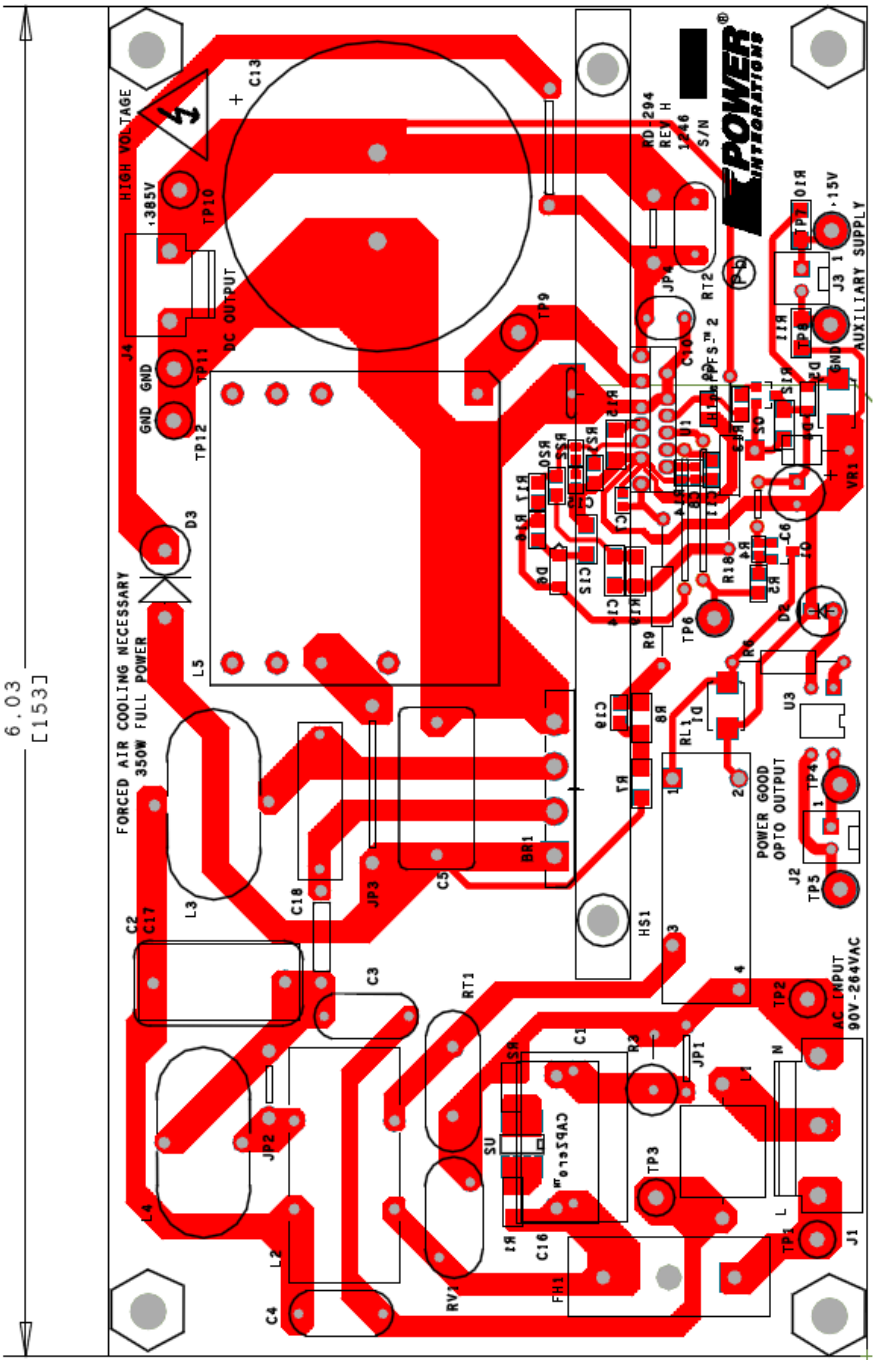

Figure 5 – Printed Circuit Layout.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	1	C1	680 nF, 275 VAC, Film, MPX Series, X2	PX684K3ID6	Carli
3	1	C2	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
4	2	C3 C4	680 pF, Ceramic, Y1	440LT68-R	Vishay
5	1	C5	1.0 µF, 450 V, Disc Ceramic	ECQ-E2W105KH	Panasonic
6	1	C6	47 µF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11)	EKMG500ELL470MF11D	Nippon Chemi-Con
7	1	C7	22 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H223K	TDK
8	1	C8	470 pF 50 V, Ceramic, X7R, 0603	ECJ-1VC1H471J	Panasonic
9	1	C9	3.3 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
10	1	C10	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
11	1	C11	22 nF, 25 V, Ceramic, X7R, 0805	C0805C223K3RACTU	Kemet
12	1	C12	2.2 µF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
13	1	C13	270 µF, 450 V, Electrolytic, (35 x 35)	EET-ED2W271EA	Panasonic
14	1	C14	47 nF, 200 V, Ceramic, X7R, 1206	12062C473KAT2A	AVX
15	1	C15	47 nF 25 V, Ceramic, X7R, 0603	C1608X7R1E473K	TDK
16	2	D1 D5	50 V, 1 A, Standard Recovery, GPP, SMB	S1AB-13-F	Diodes, Inc.
17	1	D2	LED, Green, 3 mm, 565 nm, 40 mcd	SSL-LX3044GD	Lumex Opto
18	1	D3	1000 V, 3 A, Recitifier, DO-201AD	1N5408-T	Diodes, Inc.
19	1	D4	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diodes, Inc.
20	1	D6	130 V, 5%, 250 mW, SOD-123	BAV116W-7-F	Diodes, Inc.
21	1	F1	6.3 A, 250 V, Normal, 5 mm x 20 mm, Cartridge	023206.3MXP	Littlefuse
22	1	FH1	FUSE HOLDER OPEN 5 mm X 20 mm PC MNT	64900001039	Wickmann
23	1	HS1	HEAT SINK, DER-294, Al,3003, 0.250 " Thk		Custom
24	1	J1	5 Position (1 x 5) header, 0.156 pitch, Vertical	26-64-4050	Molex
25	2	J2 J3	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
26	1	J4	CONN HEADER 3POS (1x3).156 VERT TIN	26-64-4030	Molex
27	2	JP2 JP4	Wire Jumper, Insulated, TFE, #18 AWG, 0.3 in	C2052A-12-02	Alpha
28	1	JP3	Wire Jumper, Insulated, TFE, #18 AWG, 0.7 in	C2052A-12-02	Alpha
29	1	L1	43 Shield Bead, 0.375 (9.5 mm) Dia x 0.410 (10.40 mm) L x 0.193 (4.75 mm) I.D. with PCBFP #22 AWG	2643006302	Fair-Rite Products
30	1	L2	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine Technologies
31	1	L3	220 µH, 3.6 A, Vertical Toroidal	2216-V-RC	Bourns
32	1	L5	Custom, FD-294 PFC Output Inductor, 360 µH, PQ32/30, Vertical, 12 pins	BQ32/30-1112CPFR	TDK
33	2	MTG_HOLE1 &2	Mounting Hole _156 Mils		
34	4	POST-CRKT_BRD_6-32_HEX1~4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
35	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
36	1	Q2	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.

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37	2	R1 R2	220 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ224V	Panasonic
38	1	R3	10 Ω, 1%, 2 W, Wire Wound	WHC10RFET	Ohmite
39	1	R4	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
40	1	R5	16 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ163V	Panasonic
41	1	R6	3 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-3K0	Yageo
42	2	R7 R8	1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
43	1	R9	1 MΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-1M00	Yageo
44	2	R10 R11	1 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF1R0V	Panasonic
45	1	R12	2.2 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ222V	Panasonic
46	1	R13	0 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEY0R00V	Panasonic
47	1	R14	24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
48	1	R15	100 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
49	1	R16	7.50 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7501V	Panasonic
50	1	R17	487 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4873V	Panasonic
51	1	R18	1 .5 MΩ, 1%, 1/4 W, Metal Film	RNF14FTD1M50	Stackpole
52	1	R19	787 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7873V	Panasonic
53	1	R20	1.6 MΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1604V	Panasonic
54	1	R21	60.4 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6042V	Panasonic
55	1	R22	3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
56	1	RL1	RELAY GEN PURPOSE SPST 8 A 12 V	G6RL-1A-ASI-DC12	OMRON
57	1	RT1	NTC Thermistor, 2.5 Ohms, 5 A	SL10 2R505	Ametherm
58	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
59	2	THERMAL EPOXY1& 2	Thermal Adhesive, Bergquist LBSA3005	LBSA3005	Bergquist
60	4	TP1 TP8 TP11 TP12	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
61	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
62	1	TP3	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
63	4	TP4 TP5 TP6 TP7	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
64	2	TP9 TP10	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
65	1	U1	HiperPFS-2, ESIP16/13	PFS7328H	Power Integrations
66	1	U2	CAPZero, SO-8C	CAP005DG	Power Integrations
67	1	U3	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
68	1	VR1	13 V, 5%, 1 W, DO-41	1N4743A	Microsemi

Note: Inductor L4 has not been used in this design.

7 PIXIs Design Spreadsheet

Hiper_PFS-II_Boost_042413; Rev.1.0; Copyright Power Integrations 2013	INPUT	INFO	OUTPUT	UNITS	Hiper_PFS-II_Boost_042413_Rev1-0.xls; Continuous Mode Boost Converter Design Spreadsheet
Enter Applications Variables					
Input Voltage Range			**Universal**		Select Universal or High_Line option
VACMIN			90	V	Minimum AC input voltage
VACMAX			265	V	Maximum AC input voltage
VBROWNIN			76.69		Expected Minimum Brown-in Voltage
VBROWNOUT			68.33	V	Specify brownout voltage.
VO			385.00	V	Nominal Output voltage
PO			350.00	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	deg C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN
KP	0.443		0.443		Ripple to peak inductor current ratio at the peak of VACMIN
VO_MIN			365.75	V	Minimum Output voltage
VO_RIPPLE_MAX			20	V	Maximum Output voltage ripple
tHOLDUP			20	ms	Holdup time
VHOLDUP_MIN			310	V	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	**Yes**		**Yes**		Enter "Yes" for Forced air cooling. Otherwise enter "No"
PFS Parameters					
PFS Part Number	**Auto**		**PFS7328H**		Selected PFS device
MODE	**FULL**		**FULL**		Mode of operation of PFS. For full mode enter "FULL" otherwise enter "EFFICIENCY" to indicate efficiency mode
R_RPIN			24.9	k-ohms	R pin resistor value
C_RPIN			0.47	nF	R pin capacitor value
IOCP min			9.00	A	Minimum Current limit
IOCP typ			9.50	A	Typical current limit
IOCP max			9.90	A	Maximum current limit
RDSON			0.46	ohms	Typical RDSon at 100 'C
RV1			1.50	Mohms	Line sense resistor 1
RV2			1.50	Mohms	Line sense resistor 2
RV3			1.00	Mohms	Line sense resistor 3
C_VCC			3.30	uF	Supply decoupling capacitor
R_VCC			15.00	ohms	VCC resistor
C_V			22.00	nF	V pin decoupling capacitor
C_C			22.00	nF	Feedback C pin decoupling capacitor
Power good Vo lower threshold VPG(L)			333.00	V	Power good Vo lower threshold voltage
PGT set resistor			103.79	kohm	Power good threshold setting resistor
FS_PK			70.3	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			57.0	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
IP			6.96	A	MOSFET peak current
PFS_IRMS			3.48	A	PFS MOSFET RMS current
PCOND_LOSS_PFS			5.56	W	Estimated PFS conduction losses
PSW_LOSS_PFS			1.88	W	Estimated PFS switching losses

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PFS_TOTAL			7.44	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			2.94	degC/W	Maximum thermal resistance of heatsink
Basic Inductor Calculation					
LPFC			360	uH	Value of PFC inductor at peak of VACMIN and Full Load
LPFC (0 Bias)			360	uH	Value of PFC inductor at No load. This is the value measured with LCR meter
LP_TOL	5.00		5	%	Tolerance of PFC Inductor Value
LPFC_RMS			4.13	A	Inductor RMS current (calculated at VACMIN and Full Load)
Inductor Construction Parameters					
Core Type	**Ferrite**		**Ferrite**		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	**Auto**		**PC44**		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44 or equivalent for Ferrite cores. Fixed at 52 material for Pow Iron cores.
Core Geometry	**Auto**		**PQ**		Select from Toroid or EE for Sendust cores and from EE, or PQ for Ferrite cores
Core	**Auto**		**PQ32/30**		Core part number
AE			161	mm^2	Core cross sectional area
LE			74.6	mm	Core mean path length
AL			5140	nH/t^2	Core AL value
VE			12	cm^3	Core volume
HT			5.12	mm	Core height/Height of window
MLT			67.1	cm	Mean length per turn
BW			18.6	mm	Bobbin width
NL			60		Inductor turns
LG			2.59	mm	Gap length (Ferrite cores only)
ILRMS			4.13	A	Inductor RMS current
Wire type	**LITZ**		**LITZ**		Select between "Litz" or "Regular" for double coated magnet wire
AWG	38		38	AWG	Inductor wire gauge
Filar	60		60		Inductor wire number of parallel strands
OD			0.102	mm	Outer diameter of single strand of wire
AC Resistance Ratio			1.01		Ratio of AC resistance to the DC resistance (using Dowell curves)
J		*Warning*	8.48	A/mm^2	!!! Warning Current density is too high and may cause heating in the inductor wire. Reduce J
BP_TARGET	3900		3900	Gauss	Target flux density at VACMIN (Ferrite cores only)
BM			2596	Gauss	Maximum operating flux density
BP			3875	Gauss	Peak Flux density (Estimated at VBROWNOUT)
LPFC_CORE_LOSS			0.11	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			3.00	W	Estimated Inductor copper losses
LPFC_TOTAL LOSS			3.10	W	Total estimated Inductor Losses
FIT			79.64%	%	Estimated FIT factor for inductor
Layers			3.6		Estimated layers in winding
Critical Parameters					
IRMS			4.18	A	AC input RMS current
IO_AVG			0.91	A	Output average current
Output Diode (DO)					
Part Number	**Auto**		**INTERNAL**		PFC Diode Part Number
Type			SPECIAL		Diode Type - Special - Diodes specially

					catered for PFC applications, SiC - Silicon Carbide type, UF - Ultrafast recovery type
Manufacturer			PI		Diode Manufacturer
VRRM			600	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
TRR			31	ns	Diode Reverse recovery time
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			1.34	W	Estimated Diode conduction losses
PSW_DIODE			1.34	W	Estimated Diode switching losses
P_DIODE			2.67	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.85	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			2.94	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
CO	**Auto**		**270.00**	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			11.5	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			20.1	ms	Expected holdup time with selected Output capacitor
ESR_LF			0.68	ohms	Low Frequency Capacitor ESR
ESR_HF			0.27	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.64	A	Low Frequency Capacitor RMS current
IC_RMS_HF			1.85	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.28	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.92	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			1.20	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
I^2t Rating			18.96	A^2s	Minimum I^2t rating for fuse
Fuse Current rating			6.55	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			4.08	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
PCOND_LOSS_BRIDGE			6.78	W	Estimated Bridge Diode conduction loss
CIN			1.00	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT			9.37	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
Feedback Components					
R1			1.50	Mohms	Feedback network, first high voltage divider resistor
R3			1.60	Mohms	Feedback network, third high voltage divider resistor
R2			787.00	kohms	Feedback network, second high voltage divider resistor
C1			47.00	nF	Feedback network, loop speedup capacitor
R4			60.40	kohms	Feedback network, lower divider resistor
R6			487.00	kohms	Feedback network - pole setting resistor
R7			7.15	kohms	Feedback network - zero setting resistor
C2			47.00	nF	Feedback component- noise suppression capacitor
R5			3.00	kohms	Damping resistor in serise with C3
C3			2.20	uF	Feedback network - compensation capacitor

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D1			BAV116		Feedback network - capacitor failure detection Diode
Loss Budget (Estimated at VACMIN)					
PFS Losses			7.44	W	Total estimated losses in PFS
Boost diode Losses			2.67	W	Total estimated losses in Output Diode
Input Bridge losses			6.78	W	Total estimated losses in input bridge module
Inductor losses			3.10	W	Total estimated losses in PFC choke
Output Capacitor Loss			1.20	W	Total estimated losses in Output capacitor
Total losses			21.19	W	Overall loss estimate
Efficiency			0.94		Estimated efficiency at VACMIN. Verify efficiency at other line voltages
CAPZero component selection recommendation					
CAPZero Device			CAP005DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
Total Series Resistance (R1+R2)			0.48	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN			1000.00	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2			680.00	nF	X capacitor after differencial mode choke and before bridge, ratio with Po
LDM_calc			150.93	uH	estimated minimum differencial inductance to avoid <10kHz resonance in input current
CX1			470.00	nF	X capacitor before common mode choke, ratio with Po
LCM			10.00	mH	typical common mode choke value
LCM_leakage			30.00	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220.00	pF	typical Y capacitance for common mode noise suppression
LDM_Actual			120.93	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM chock.
Note: CX2 can be placed between CM chock and DM choke depending on EMI design requirement.					

Note: If current density is higher than 6 A / mm^2 on forced air cooling case, a “warning” will be generated. Need for a higher cross section of the wire should be made based on the thermal test result. With sufficient cooling, higher current densities can be used safely.

8 Switching Inductor Specification

8.1 Electrical Diagram

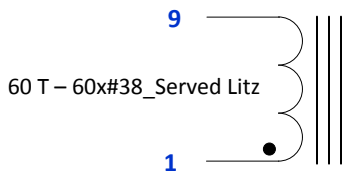

Figure 6 – Inductor Electrical Diagram.

8.2 Electrical Specifications

Inductance	Pins 1-9, measured at 100 kHz, 0.4 $V_{RMS.}$	360 µH
Resonant Frequency	Pins 1-9.	1300 kHz (Min.)

8.3 Materials

Item	Description
[1]	Core: TDK PC44PQ32/30-Z-12.
[2]	Bobbin: PQ32/30-Vertical, 12 pins (6/6). AllStar P/N: BPQ32/30-112CPFR, ROHS.
[3]	Magnet wire: 60/#38 Served Litz wire.
[4]	Tape: 3M 1298 Polyester Film, 18.4 mm wide, 2.0 mils thick, or equivalent.
[5]	Varnish: Dolph BC-359, or equivalent.

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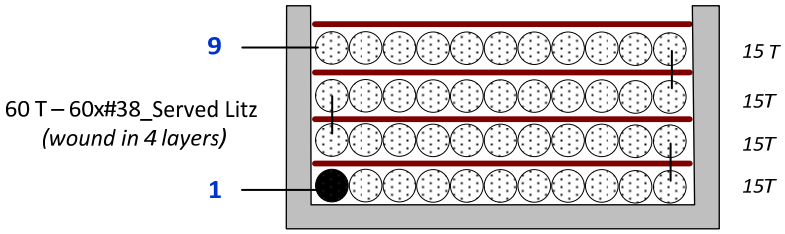
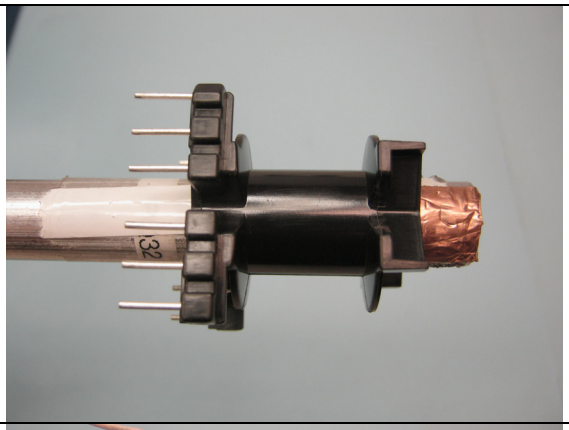
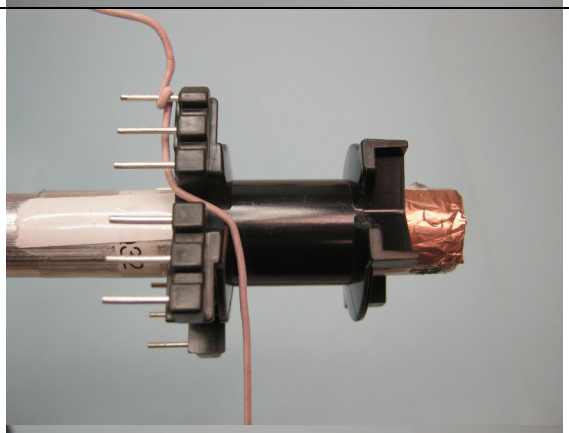
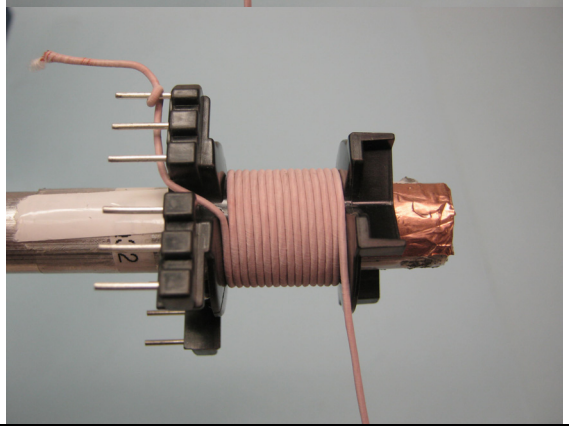


Figure 7 – Transformer Build Diagram.

8.4 Inductor Winding Instruction

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding	Start at pin 1, wind 60 turns of wire item [3] in 4 layers (15T/layer), place tape item [4] between layers. At the last turn, continue winding past the primary side ½ turn in order to terminate at pin 9. Wrap 2 layers of tape item [4] to hold the winding in place.
Final Assembly	Grind both center legs of core equally to get 360 μH. Assemble and secure core halves with tape. Remove pins: 2, 3, 11, and 12. Varnish with item [5].

8.5 Inductor Build Illustrations

Winding Preparation		Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding	 	Start at pin 1, wind 60 turns of wire item [3] in 4 layers (15T/layer),

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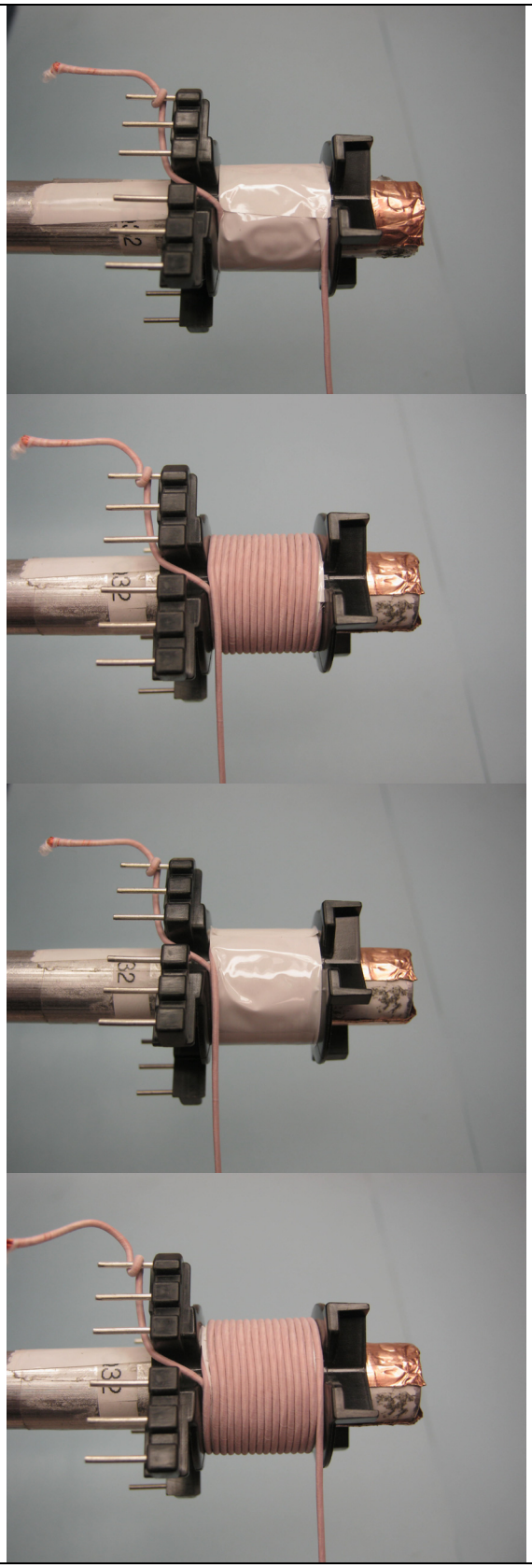
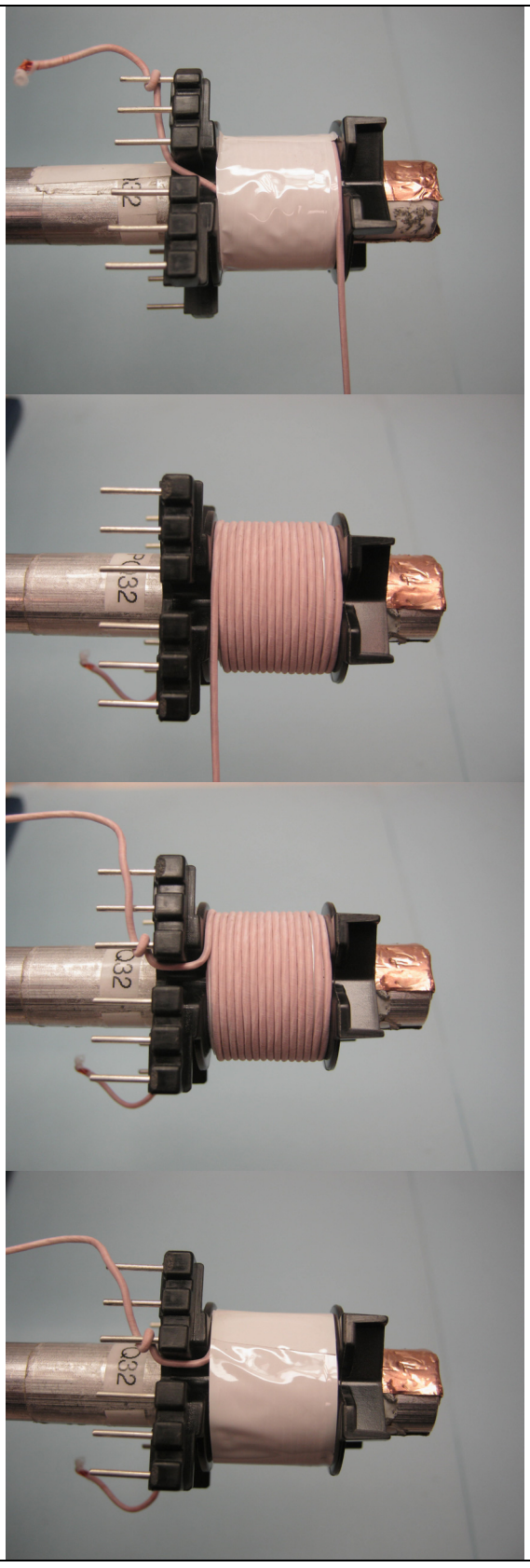
		place tape item [4] between layers.

		At the last turn, continue winding past the side ½ turn in order to terminate at pin 9.

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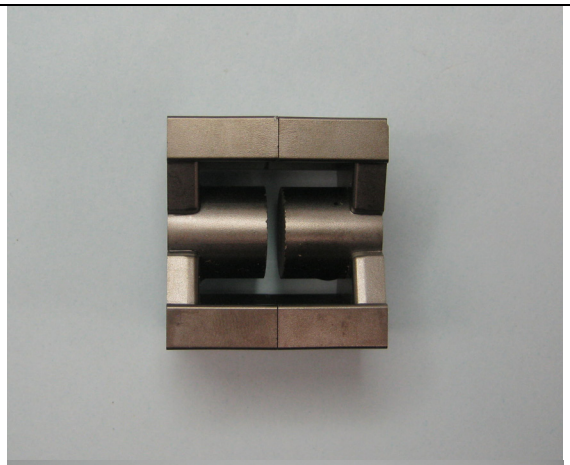
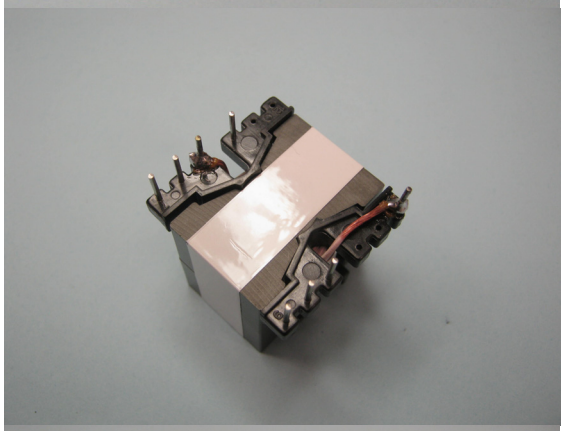
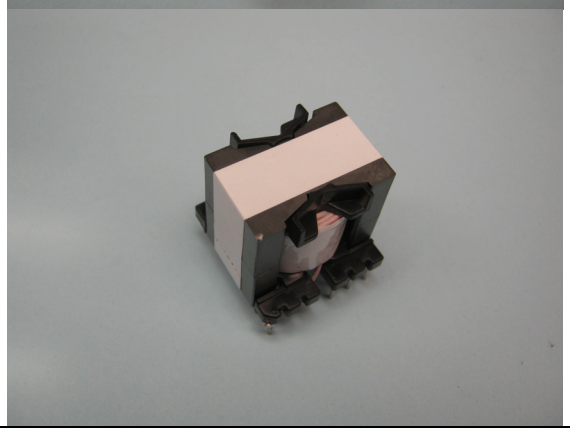
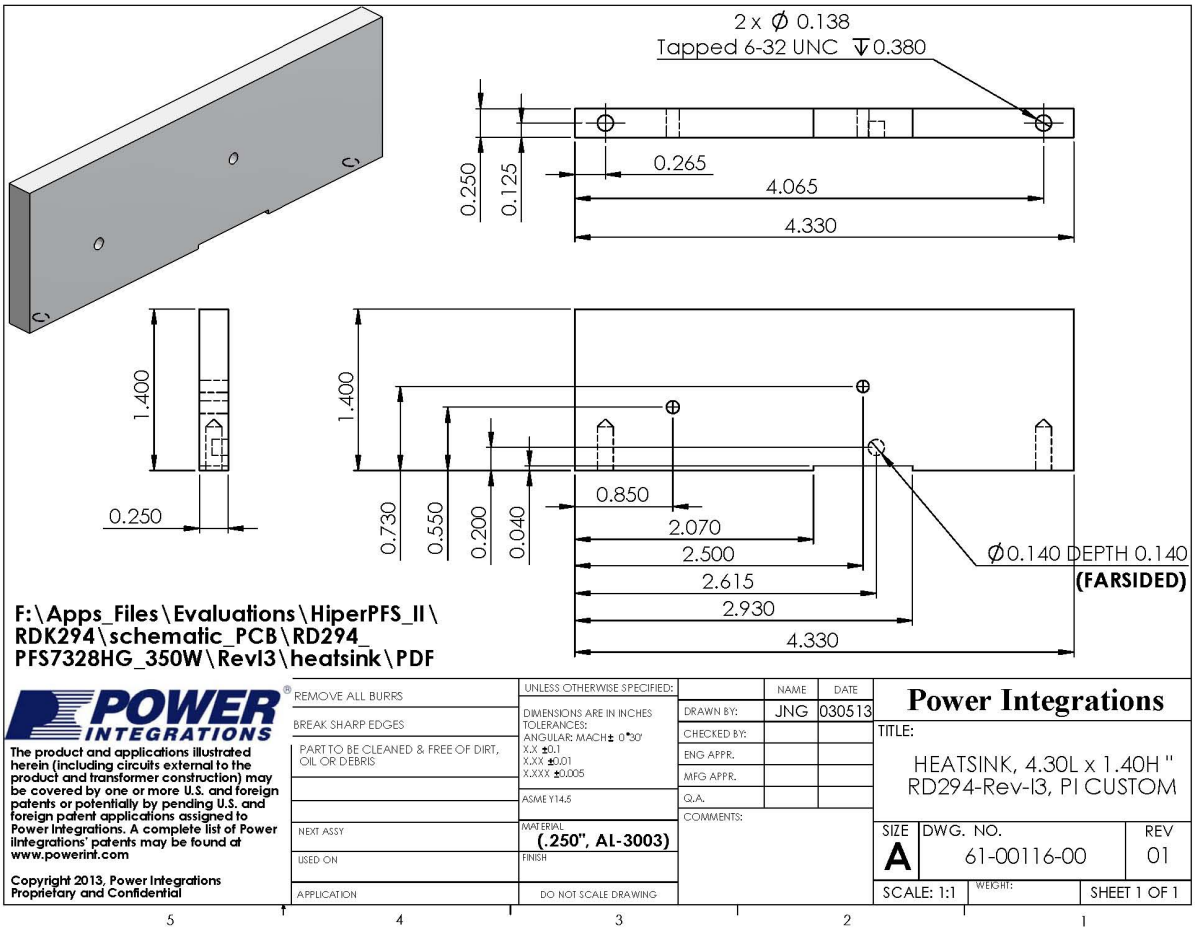
Final Assembly	  	Grind both core center legs equally to get 360 μH. Secure core halves with tape. Remove pins 2, 3, 11, and 12. Varnish with item [5].

9 eSIP U1 and Bridge BR1 Heat Sink

(Note: The heat sink was designed for operation with forced air cooling for all operation conditions.)

9.1 eSIP U1 and Bridge BR1 Heat Sink Fabrication Drawing



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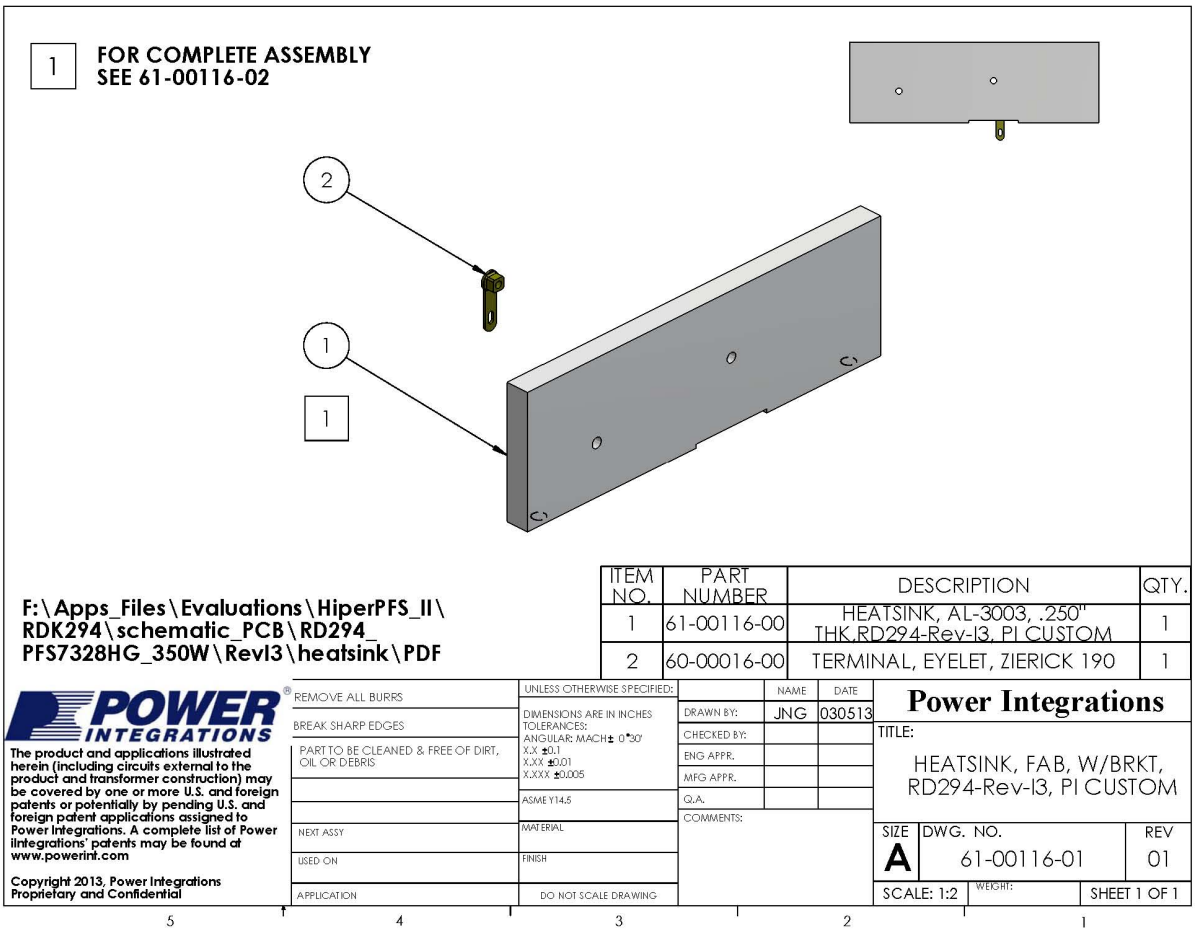
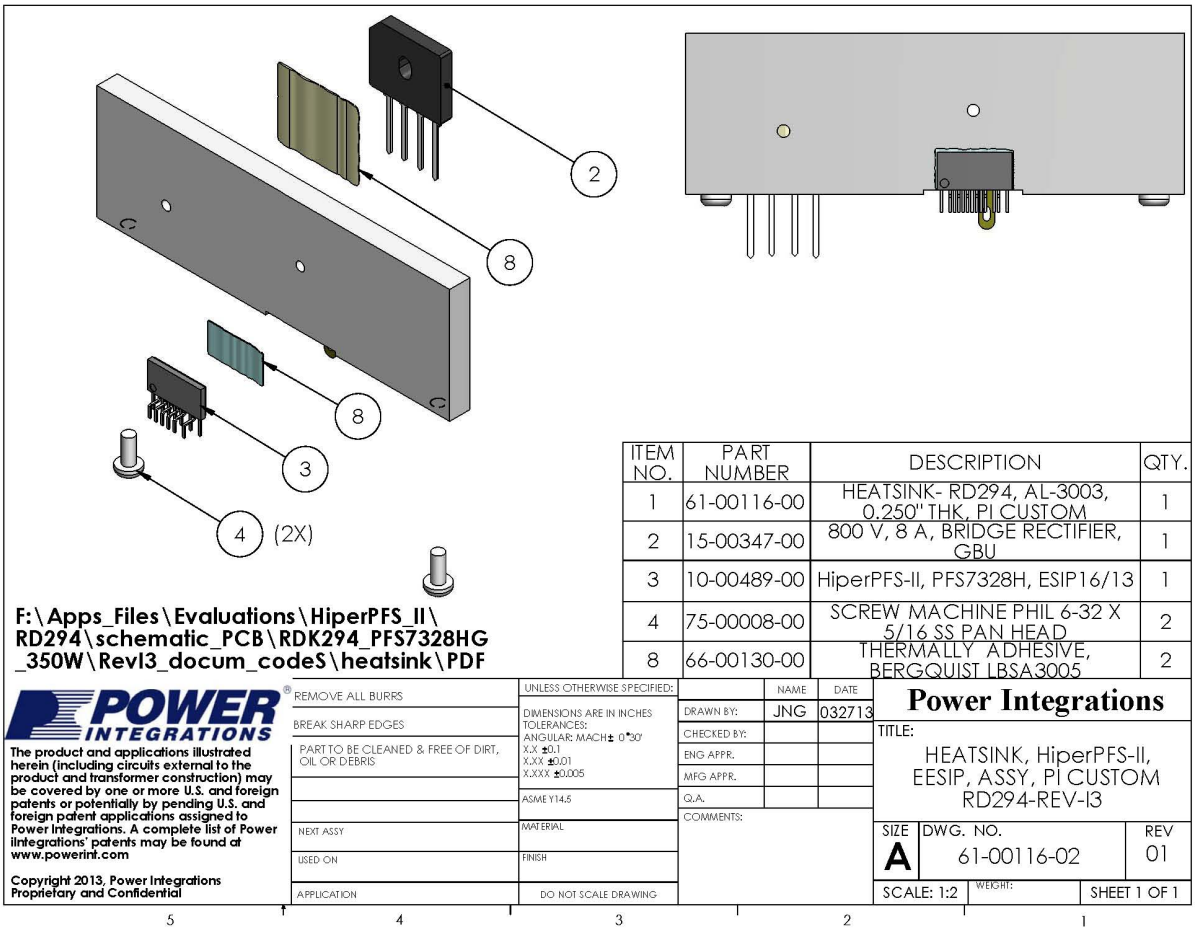
9.2 eSIP U1 and Bridge BR1 Heat Sink Assembly Drawing



9.3 eSIP U1 and Bridge BR1 Assembly to Heat Sink Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00116-00	HEATSINK- RD294, AL-3003, 0.250" THK, PI CUSTOM	1
2	15-00347-00	800 V, 8 A, BRIDGE RECTIFIER, GBU	1
3	10-00489-00	HiperPFS-II, PFS7328H, ESIP16/13	1
4	75-00008-00	SCREW MACHINE PHIL 6-32 X 5/16 SS PAN HEAD	2
8	66-00130-00	THERMALLY ADHESIVE, BERGQUIST LBSA3005	2

F:\Apps_Files\Evaluations\HiperPFS_II\RD294\schematic_PCB\RDK294_PFS7328HG_350W\Revl3_docum_codeS\heatsink\PDF

POWER INTEGRATIONS

REMOVE ALL BURRS
BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	032713
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE: HEATSINK, HiperPFS-II, EESIP, ASSY, PI CUSTOM RD294-REV-I3

SIZE	DWG. NO.	REV
A	61-00116-02	01

SCALE: 1:2 WEIGHT: SHEET 1 OF 1

5 4 3 2 1

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10 Performance Data

All measurements performed at room temperature, 60 Hz input frequency for voltages below 150 VAC and input frequency of 50 Hz for 150 VAC and higher.

During operation, an 80 mm fan was placed next to the board. Picture of measurement set up can be found in appendix A.

10.1 No-Load Input Power

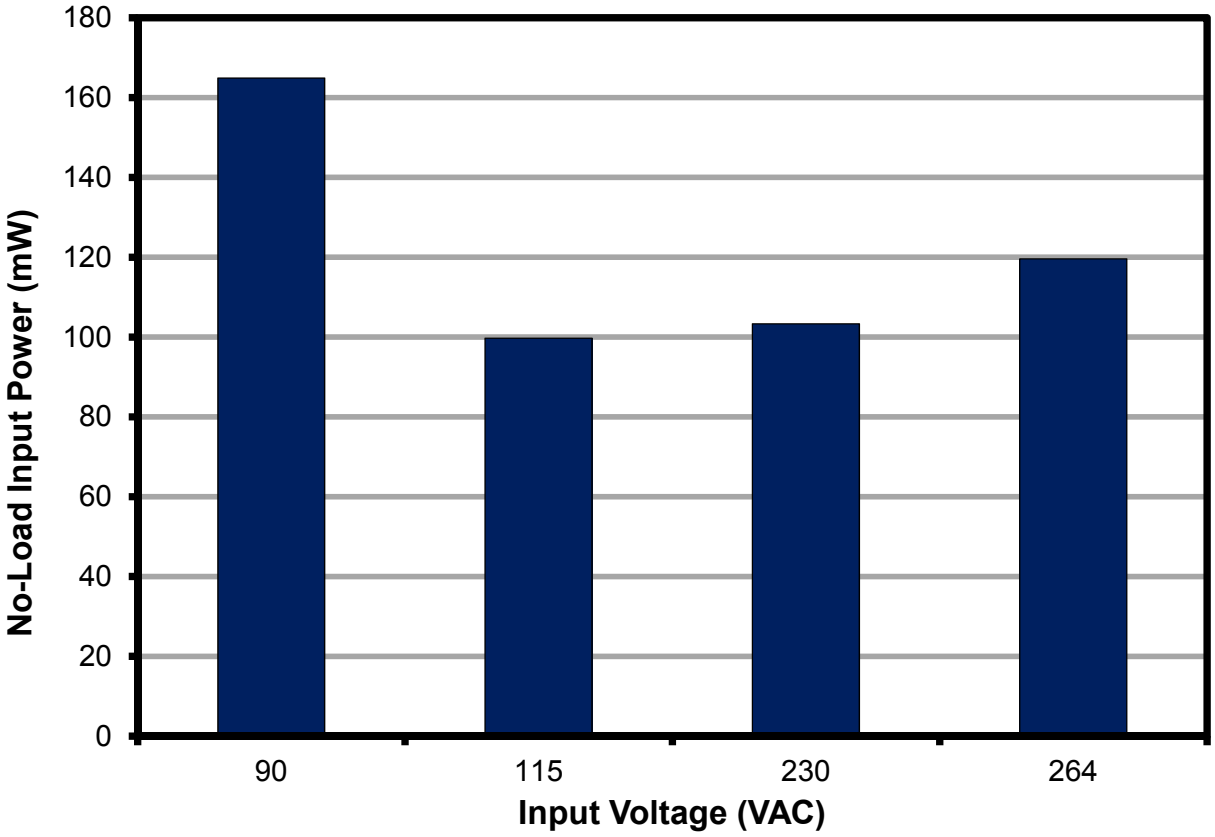

Figure 8 – No-Load Input Power.

Note: Power consumption from the V_{CC} auxiliary power supply is not included. The measurement integral time is 30 minutes.

10.2 PFC Efficiency

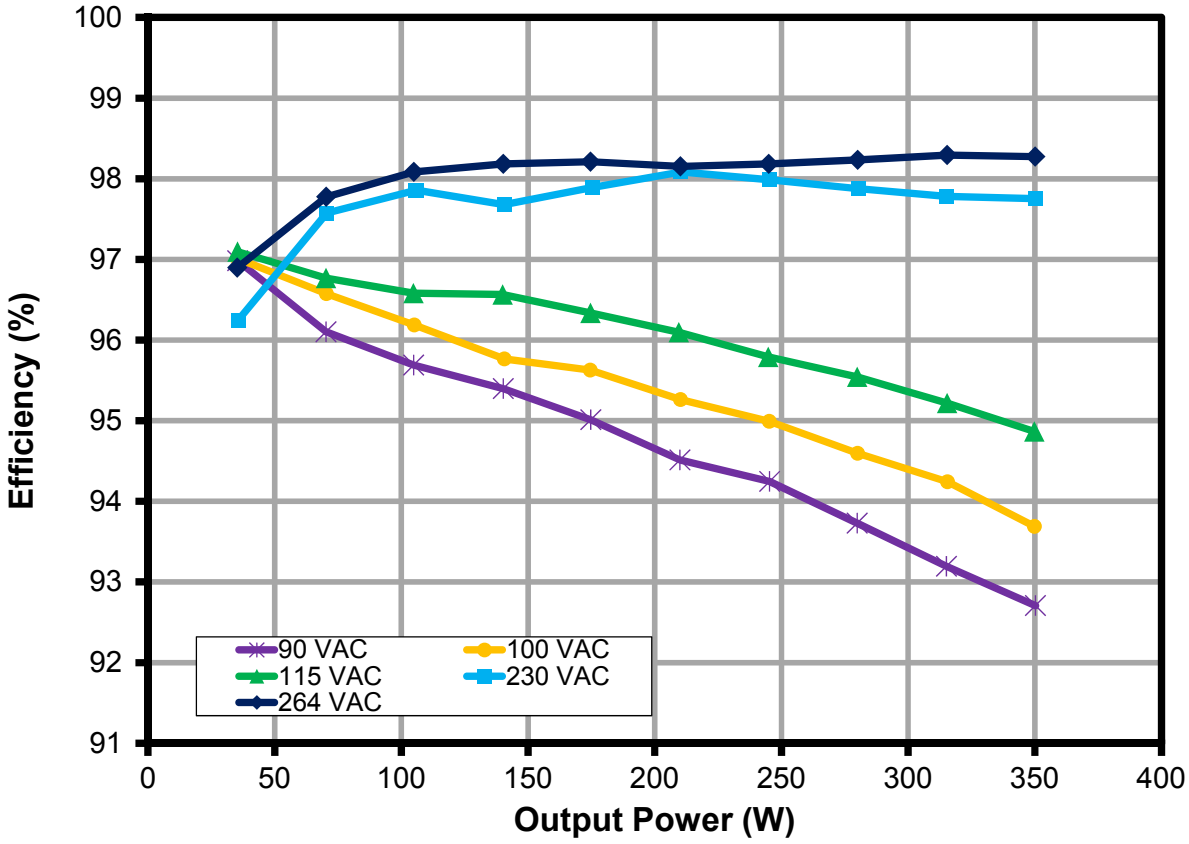

Figure 9 – Efficiency vs. Output Power.

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10.3 Input Power Factor

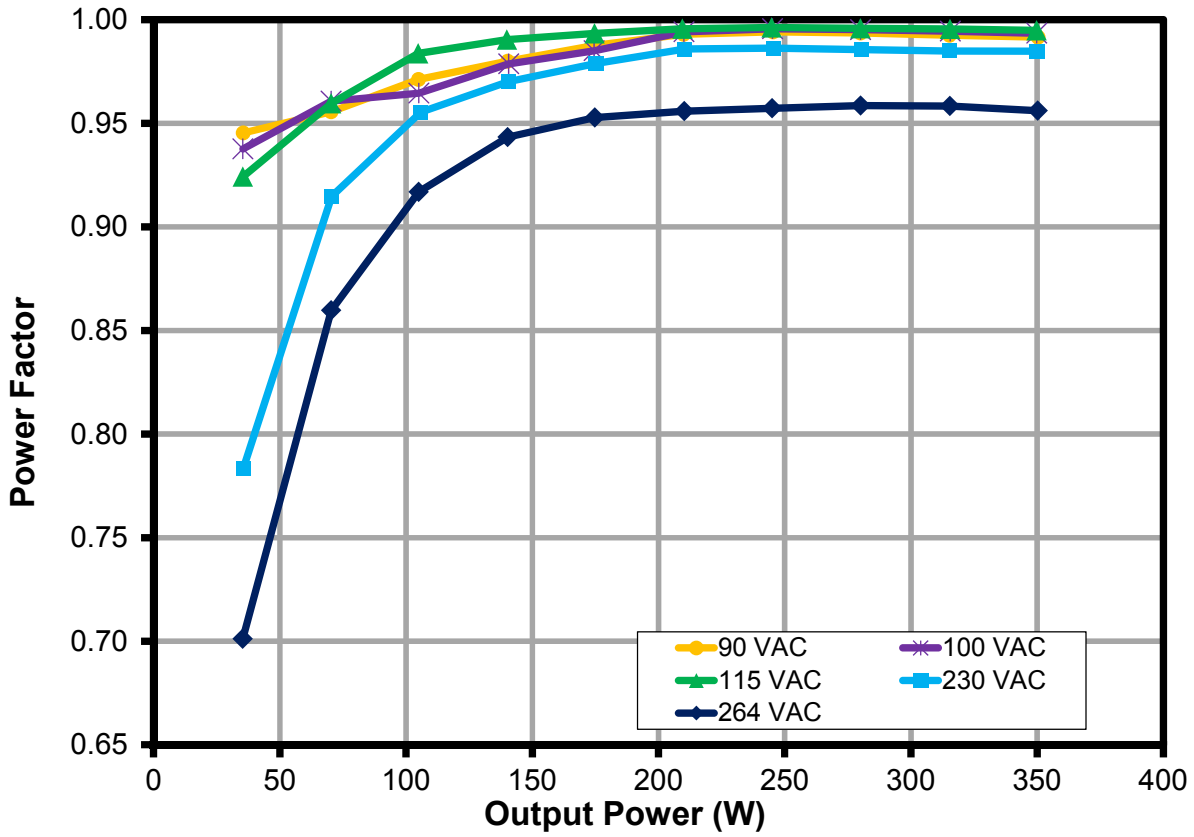

Figure 10 – Input Power Factor vs. Output Power.

10.4 Regulation

10.4.1 Load

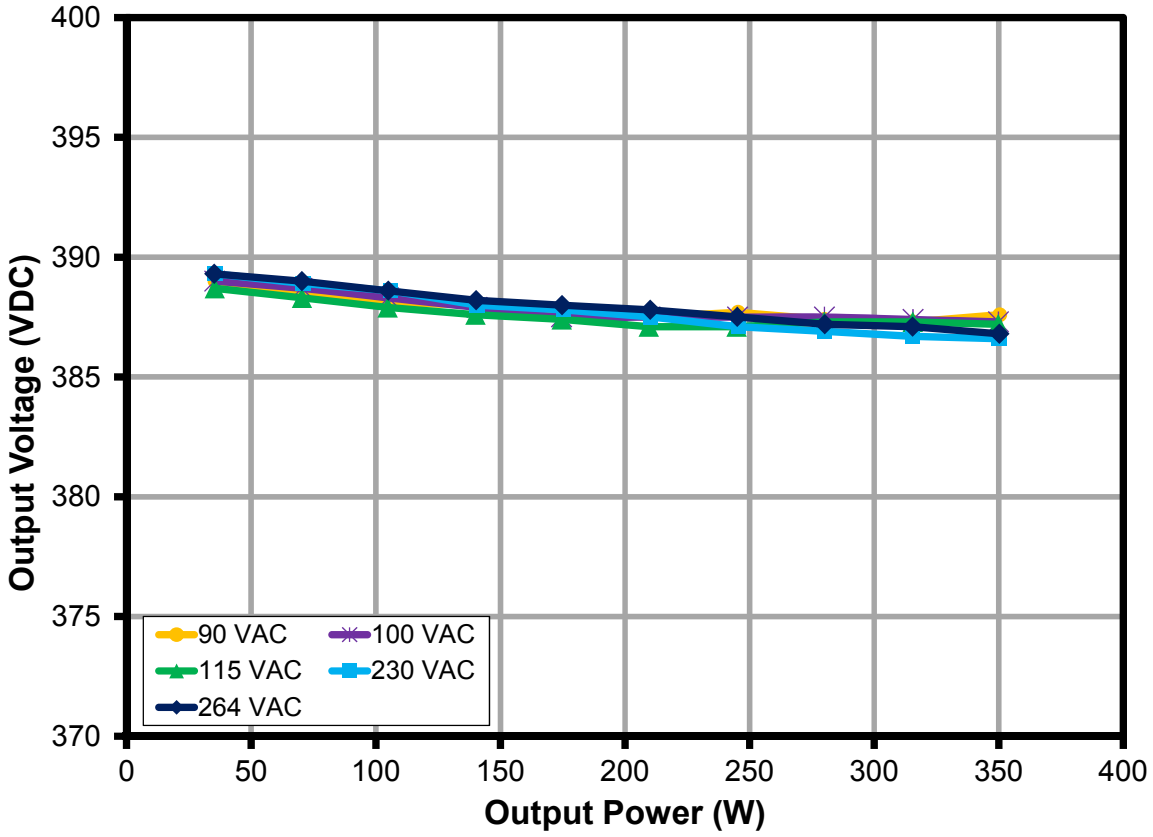

Figure 11 – Load Regulation.

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10.4.2 Line

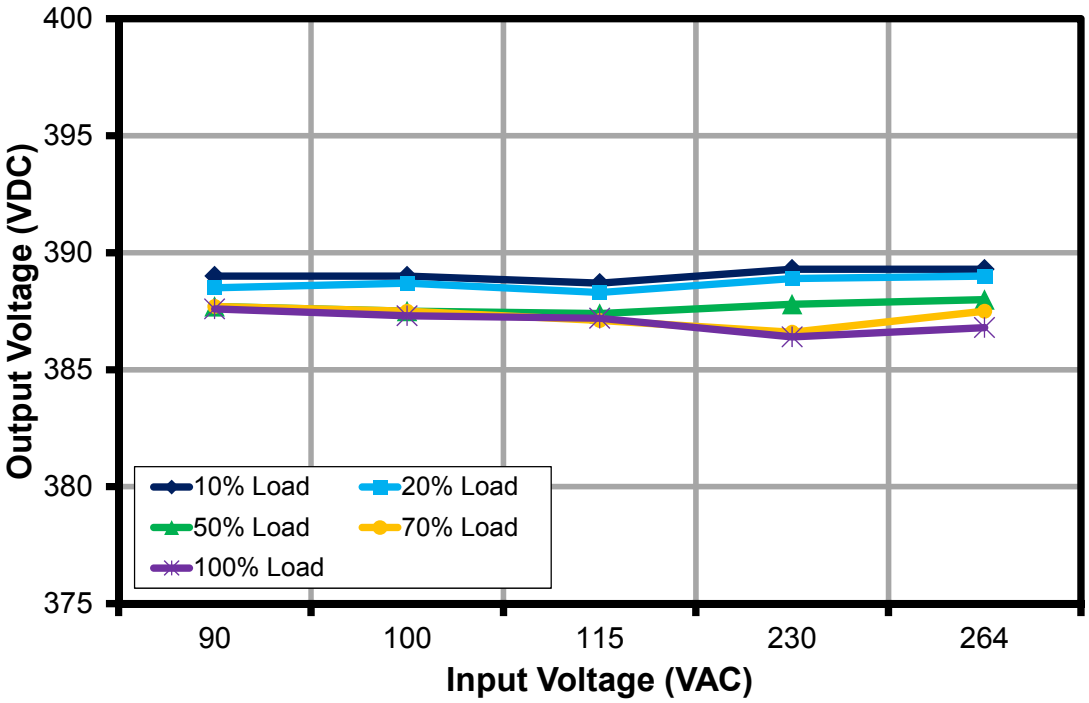

Figure 12 – Line Regulation.

10.4.3 Overload

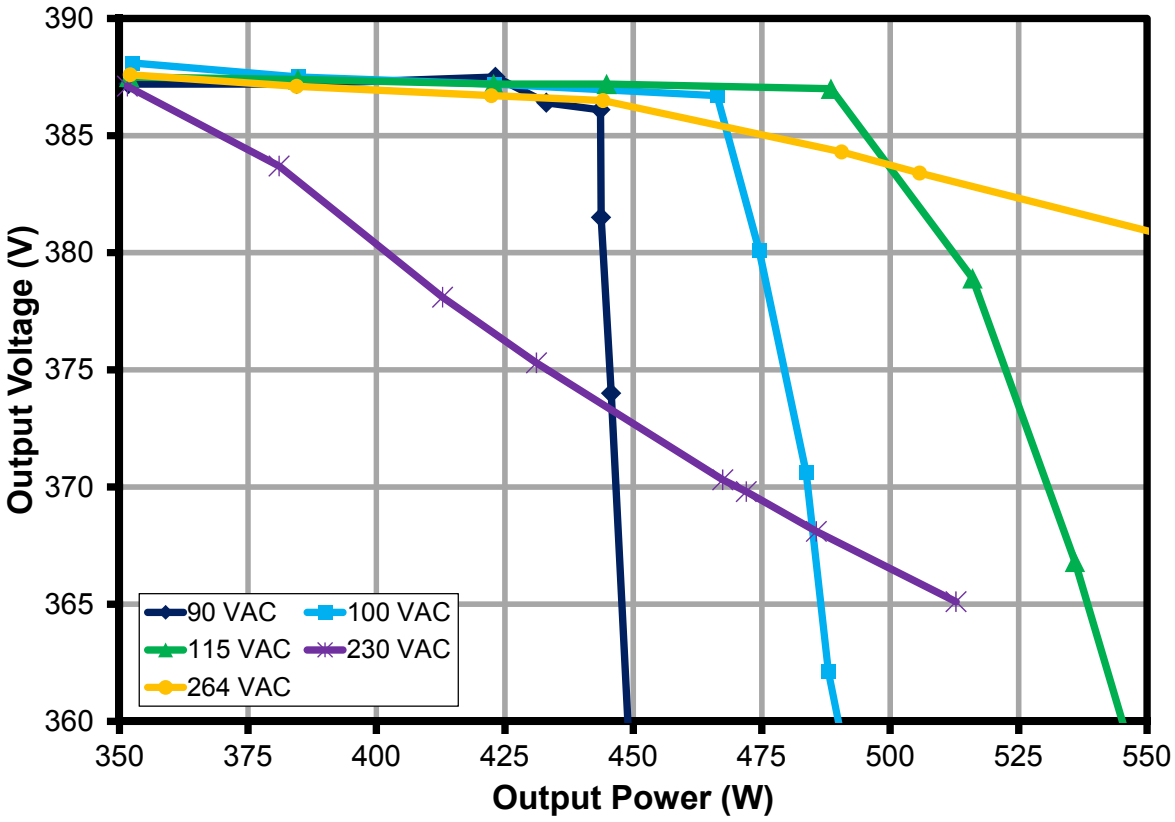

Figure 13 – Overload Regulation.

Note: 350 W is rated full load for this board design.

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10.5 THDi

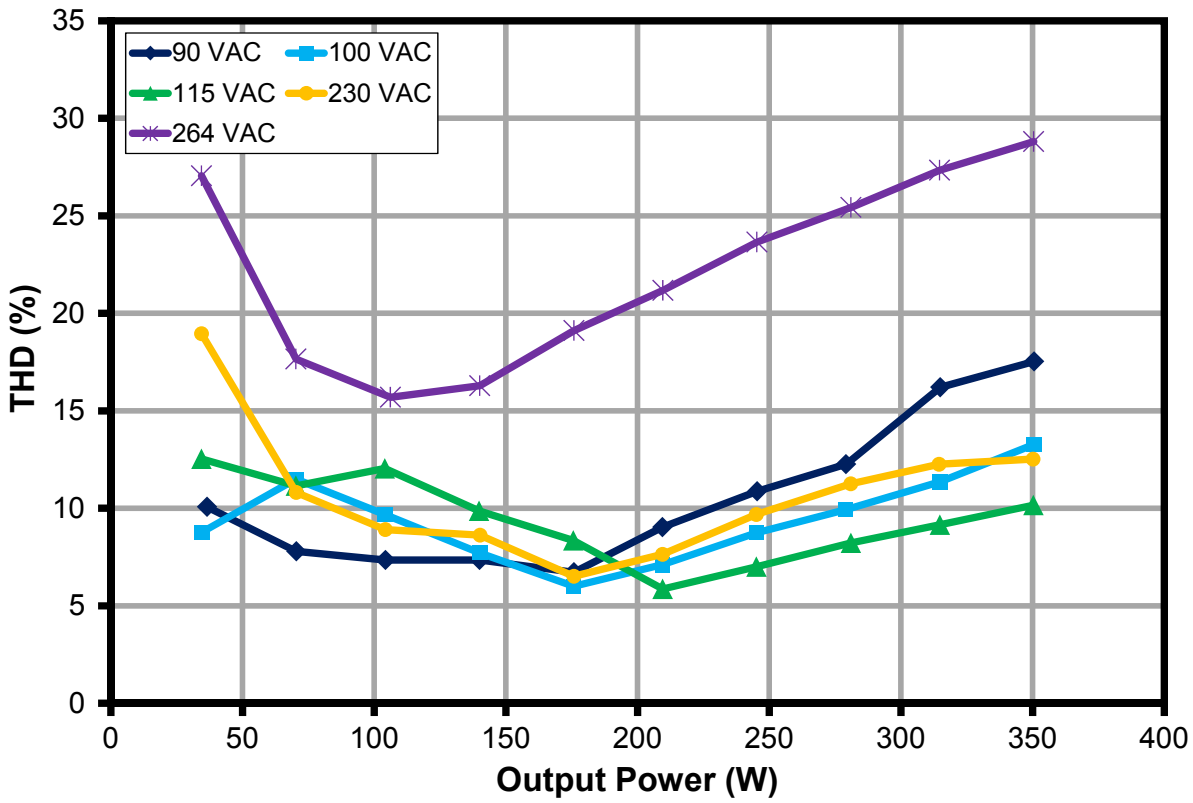

Figure 14 – Input Current THD vs. Load.

10.6 Input Current Harmonic Distortion (IEC 61000-3-2 Class-D)

Measured at 230 VAC Input 50 Hz.

10.6.1 50% Load at Output

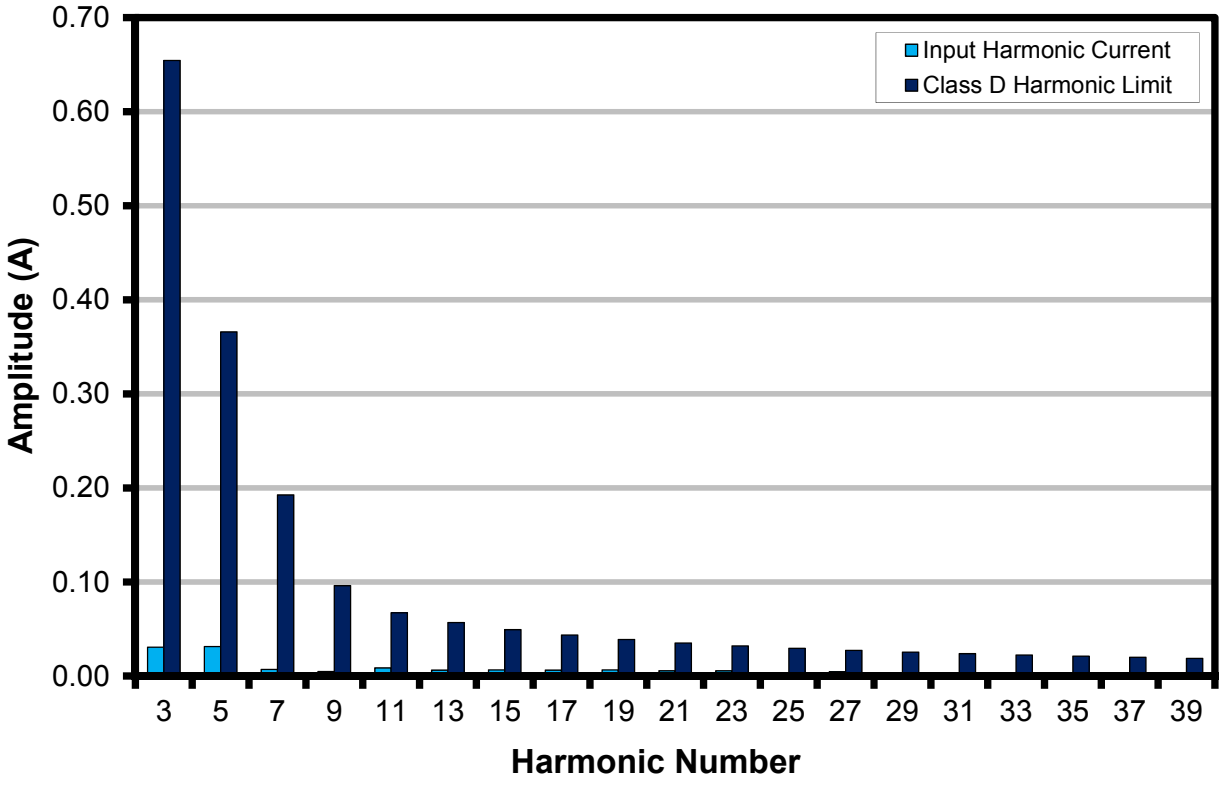

Figure 15 – Amplitude of Input Current Harmonics for 50% Load at 230 VAC Input.

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10.6.2 100% Load at Output

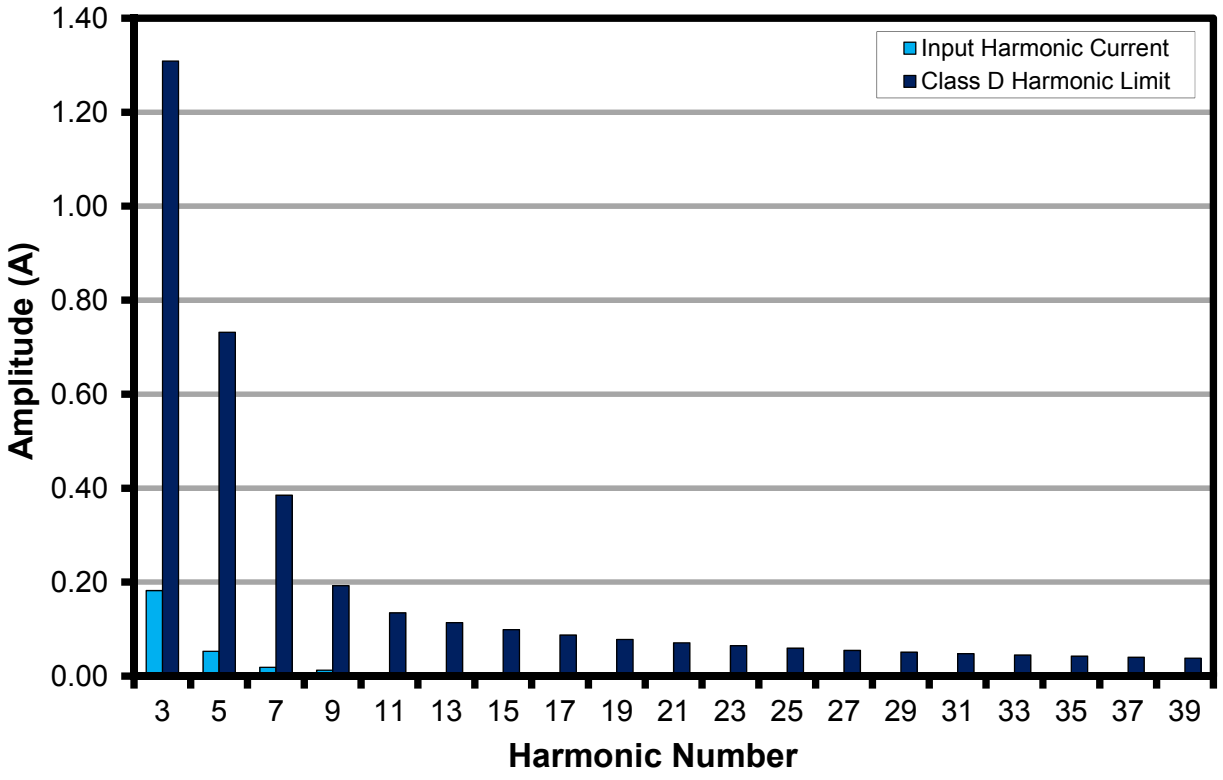

Figure 16 – Amplitude of Input Current Harmonics for 100% Load at 230 VAC Input.

11 Thermal Performance

An 80 mm fan powered by 12 VDC supply was placed right next to the board's right-side edge when the PFC system was running full load. The unit was allowed to reach thermal equilibrium [~2 hrs.] prior to thermal measurement with a FLIR camera. Table 1 shows full load temperature of key components measured at equilibrium, room temperature and with forced air cooling.

Temperature (ºC) 350 W Load			
Component		**115 VAC**	**230 VAC**
Ambient (measured by Flir)		26.3	25.6
CM Inductor	L2	46	32
DM Inductor	L3	42	31
Main Inductor	L5 Wire	54	36.3
	L5 Core	42	33.5
X1 Capacitor	C1	30	28
X2 Capacitor	C2	28	28
Bridge Capacitor	C5	32	29
Bride Rectifier	BR1	62.9	43.8
Output Capacitor	C13	31	28
Heat Sink Top (close to PFS IC)		47	37
PFS7328H	U1 MOSFET	60.2	45.3
	U1 Diode	57.2	45.4

Table 1 – Steady State Thermal Performance

Note: Ambient temperature is measured using a thermocouple. The rest of temperature measurements are made using a thermal camera.

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11.1 115 VAC Thermal Measurements

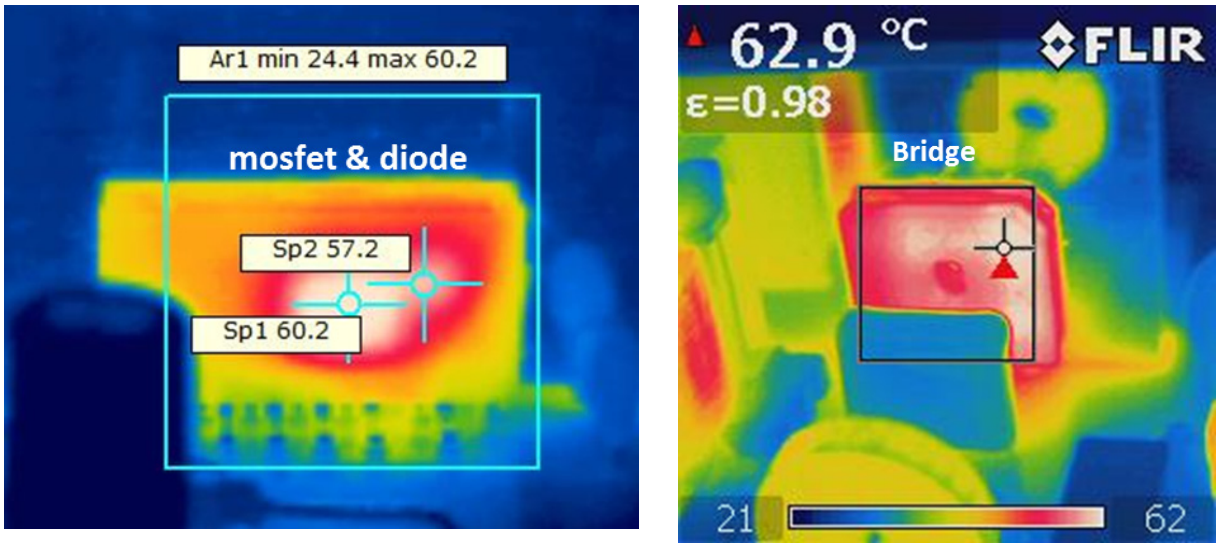

Figure 17 – Infra-Red Images of PFS MOSFET and Diode [left] and Bridge [right] at Thermal Equilibrium, 115 VAC, Full Load, with Forced-Air Flow, 26.3 ºC Ambient, Heat Sink Temperature 47 ºC.

11.2 230 VAC Thermal Measurements

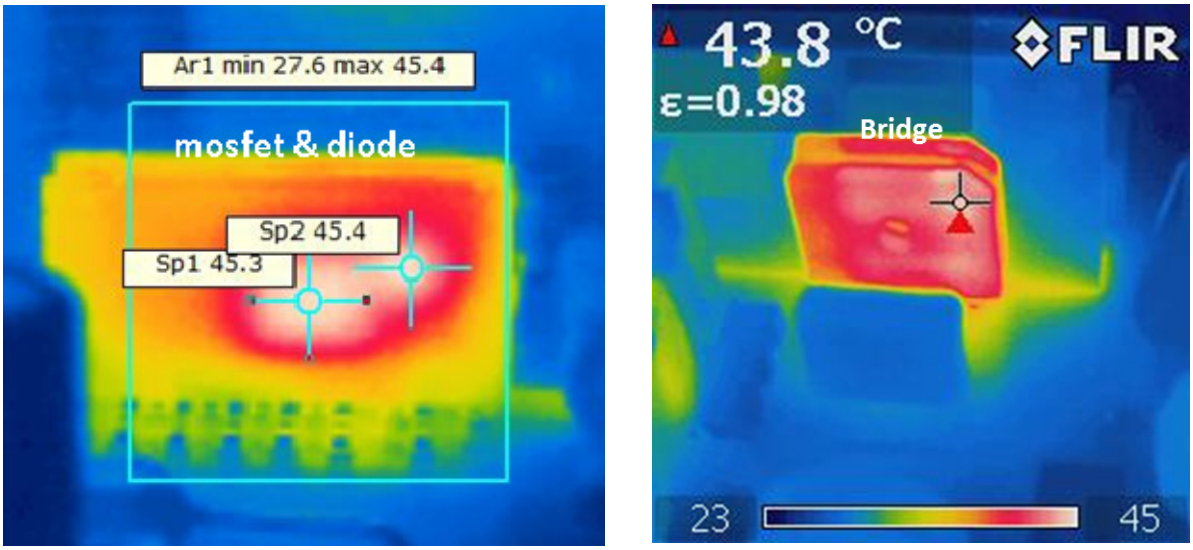

Figure 18 – Infra-Red Images of PFS MOSFET and Diode [left] and Bridge [right] at Thermal Equilibrium, 230 VAC, Full Load, with Forced-Air Flow, 25.6 ºC Ambient, Heat Sink Temperature 37 ºC.

12 Waveforms

12.1 Input Current at 115 VAC and 60 Hz

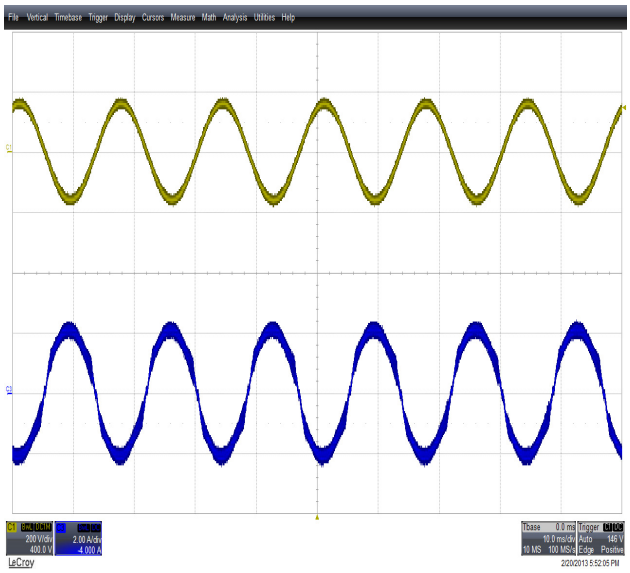

Figure 19 – 115 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 2 A / div., 10 ms / div.

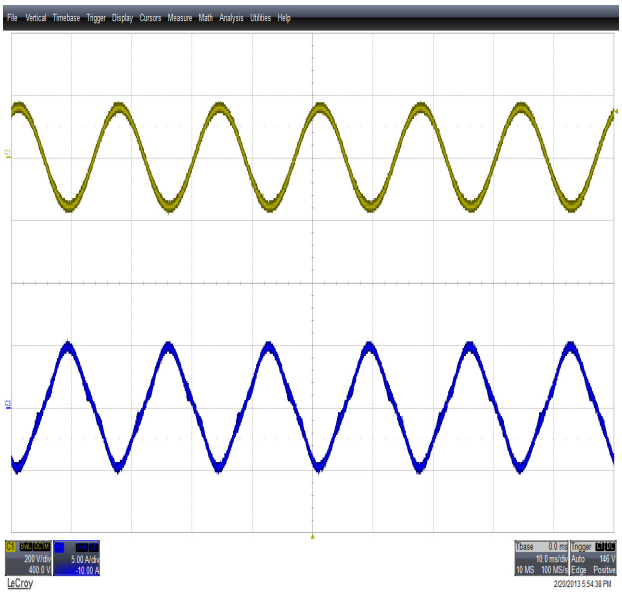

Figure 20 – 115 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Lower: I_{IN}, 5 A / div., 10 ms / div.

12.2 Input Current at 230 VAC and 50 Hz

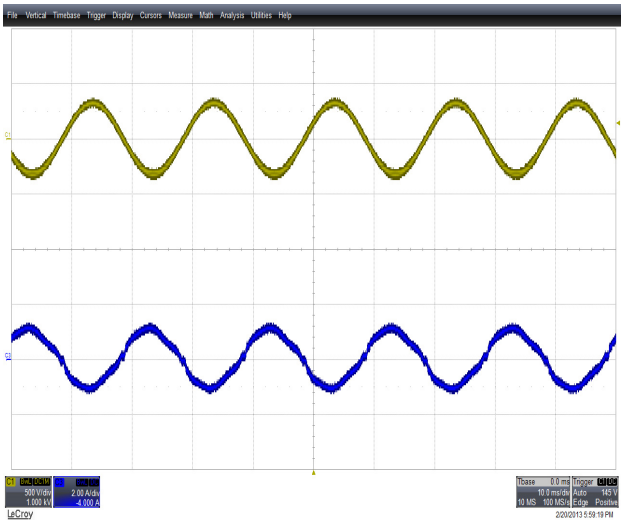

Figure 21 – 230 VAC, 50% Load.
Upper: V_{IN}, 500 V / div.
Lower: I_{IN}, 2A / div., 10 ms / div.

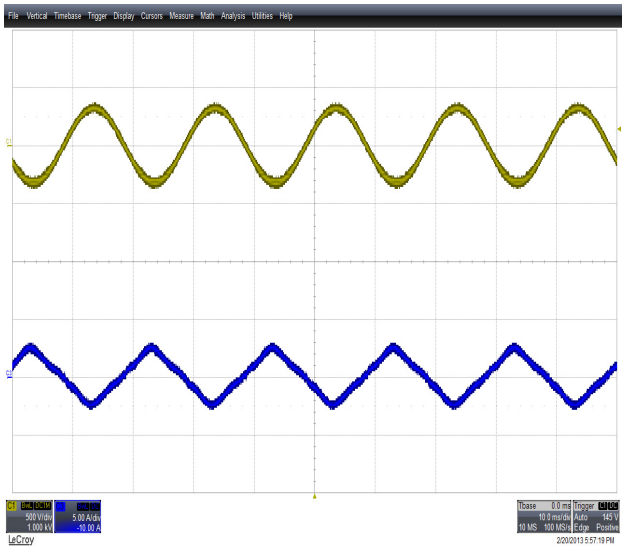

Figure 22 – 230 VAC, 100% Load.
Upper: V_{IN}, 500 V / div.
Lower: I_{IN}, 5 A / div., 10 ms / div.

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12.3 Start-up at 90 VAC and 60 Hz

.

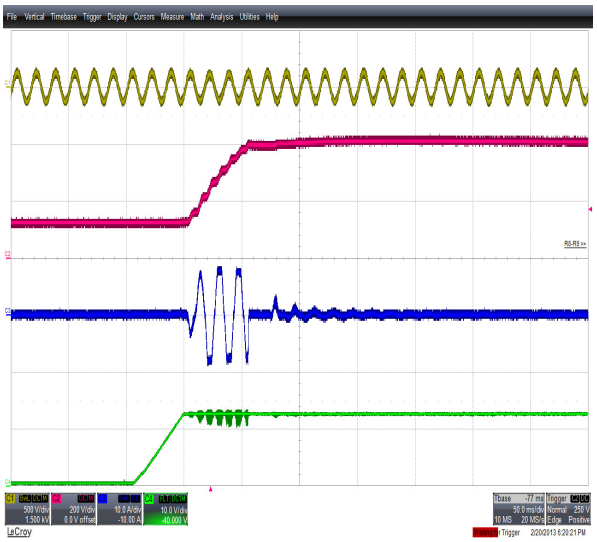

Figure 23 – 90 VAC, No-Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

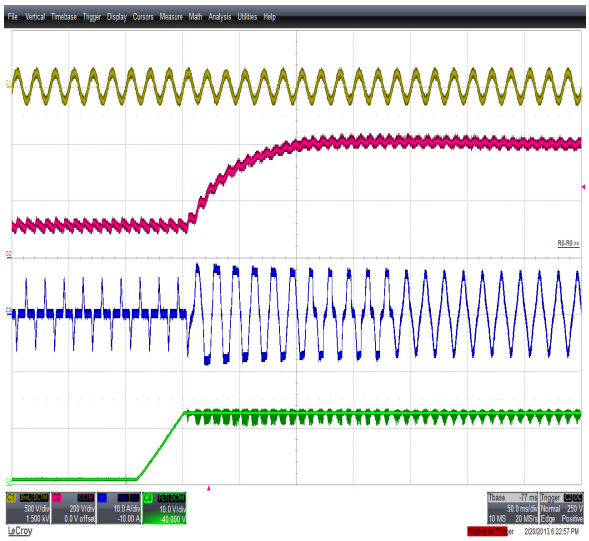

Figure 24 – 90 VAC, Full Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

12.4 Start-up at 115 VAC and 60 Hz

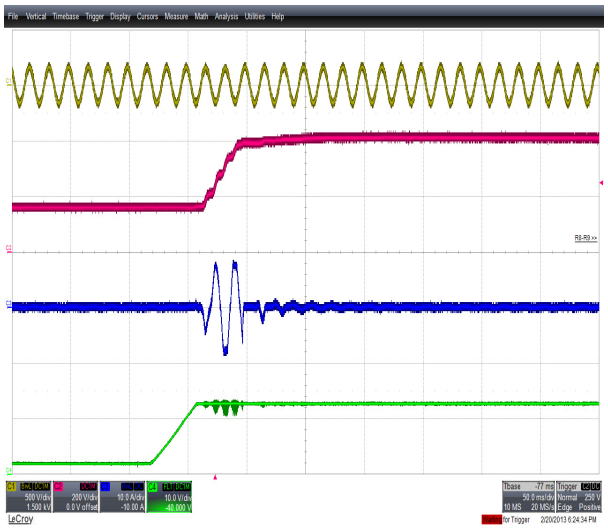

Figure 25 – 115 VAC, No-Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

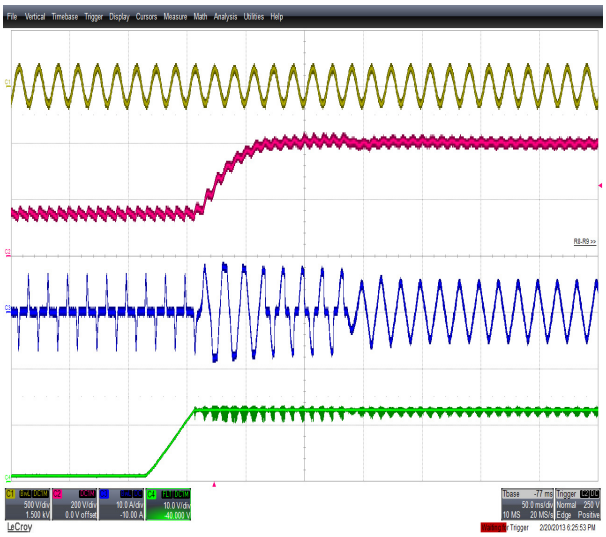

Figure 26 – 115 VAC, Full Load.
Upper: V_{IN}, 500 V / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

12.5 Start-up at 230 VAC and 50 Hz

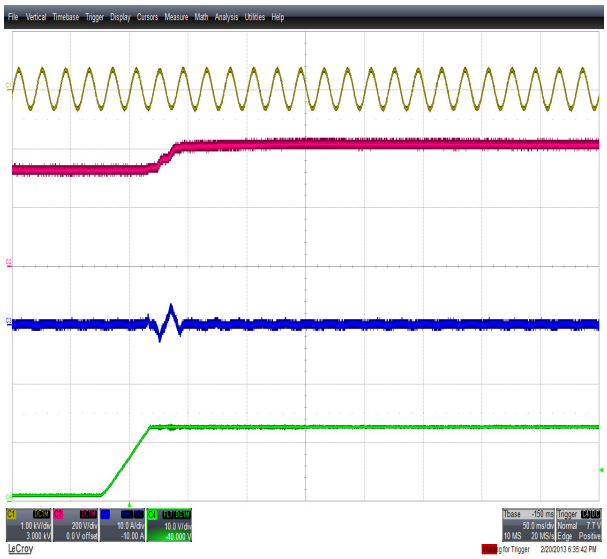

Figure 27 – 230 VAC, No-Load.
Upper: V_{IN}, 1 kV / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

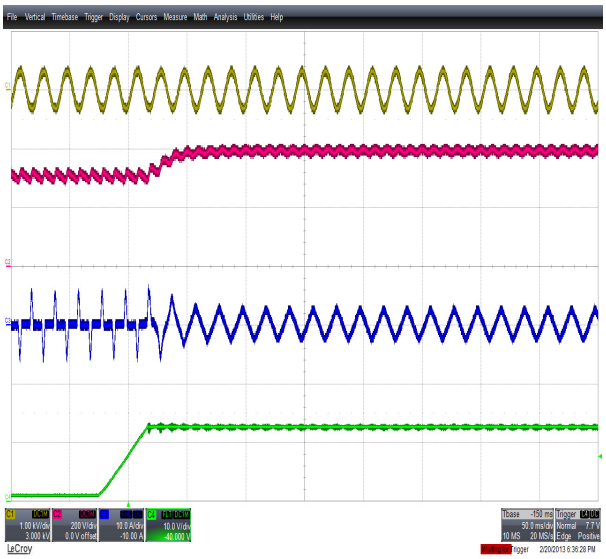

Figure 28 – 230 VAC, Full Load.
Upper: V_{IN}, 1 kV / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

12.6 Start-up at 264 VAC and 50 Hz

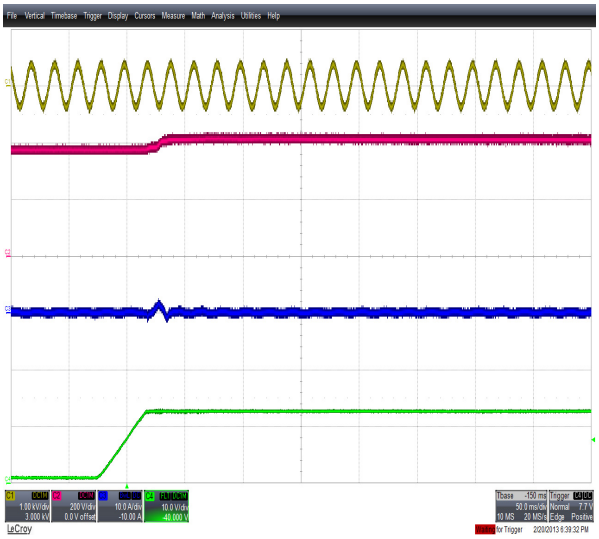

Figure 29 – 264 VAC, No-load.
Upper: V_{IN}, 1 kV / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

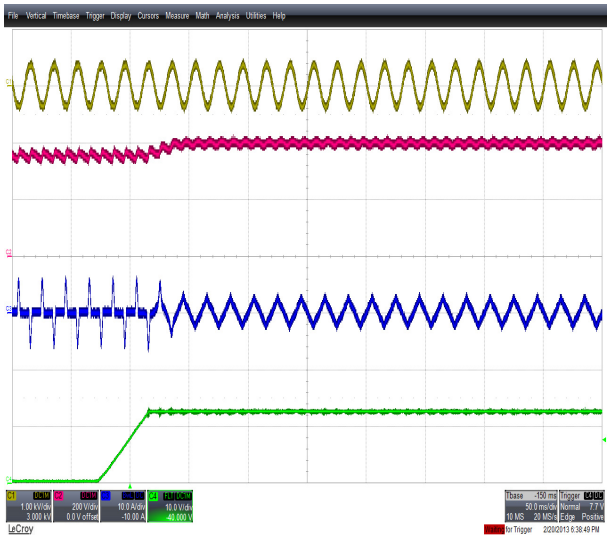

Figure 30 – 264 VAC, Full Load.
Upper: V_{IN}, 1 kV / div.
Second: V_{OUT}, 200 V / div.
Third: I_{IN}, 10 A / div.
Lower: V_{CC}, 10 V / div., 50 ms / div.

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12.7 Load Transient Response (90 VAC, 60 Hz)

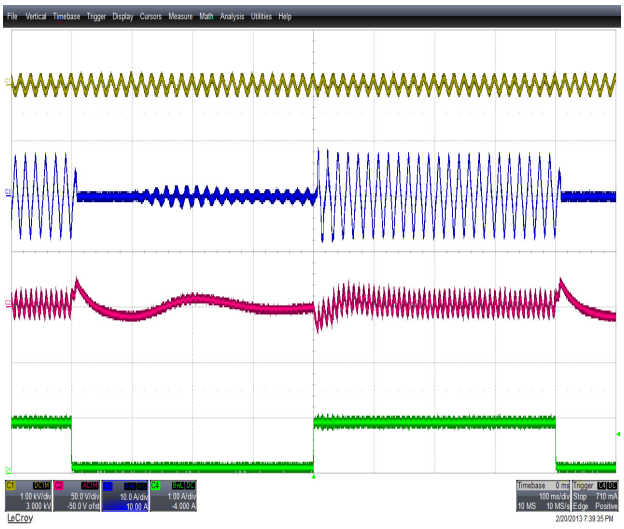

Figure 31 – Transient Response, 90 VAC,
10-100-10% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

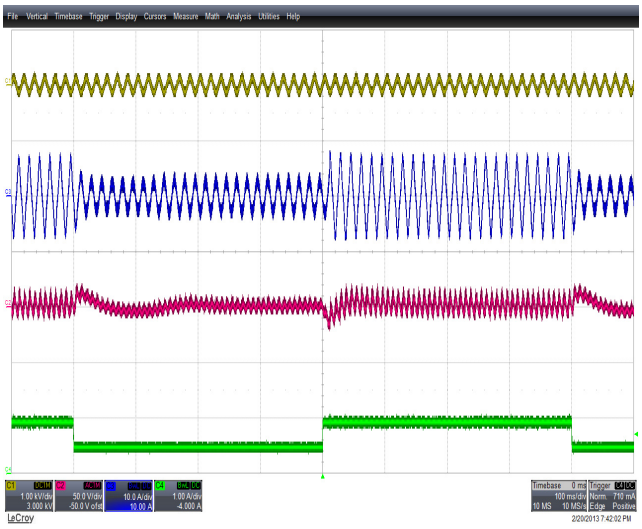

Figure 32 – Transient Response, 90 VAC,
50-100-50% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

12.8 Load Transient Response (115 VAC, 60 Hz)

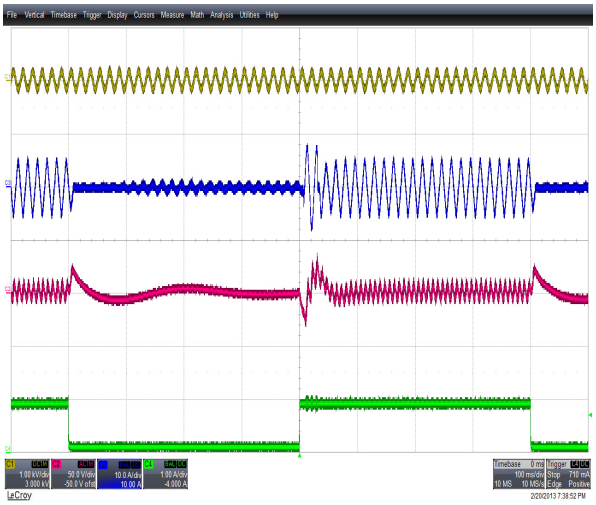

Figure 33 – Transient Response, 115 VAC, 10-100-10% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

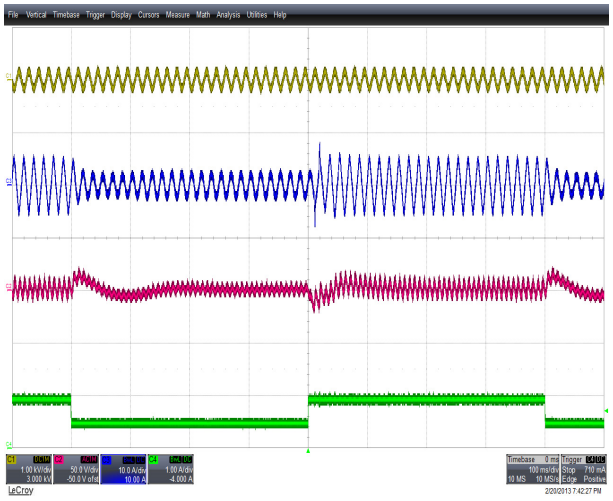

Figure 34 – Transient Response, 115 VAC, 50-100-50% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 10 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

12.9 Load Transient Response (230 VAC, 50 Hz)

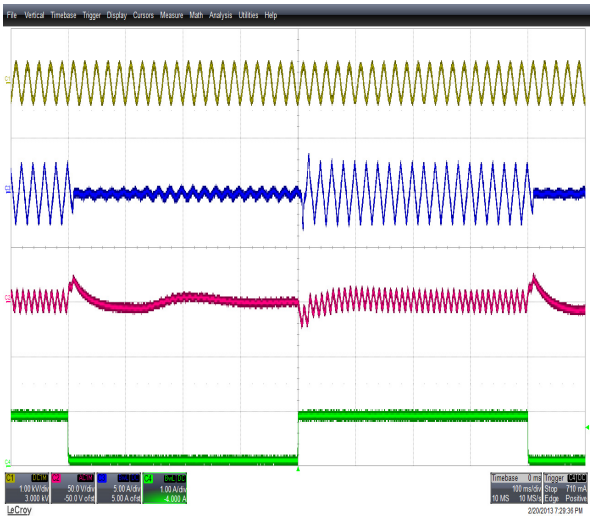

Figure 35 – Transient Response, 230 VAC, 10-100-10% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 5 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

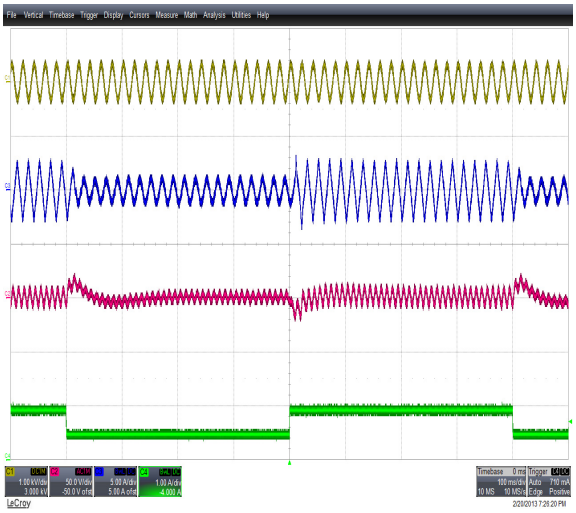

Figure 36 – Transient Response, 230 VAC, 50-100-50% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 5 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

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12.10 Load Transient Response (264 VAC, 50 Hz)

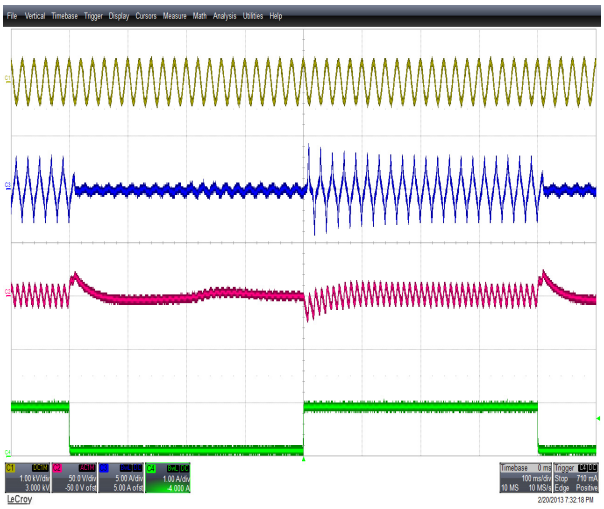

Figure 37 – Transient Response, 264 VAC, 10-100-10% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 5 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

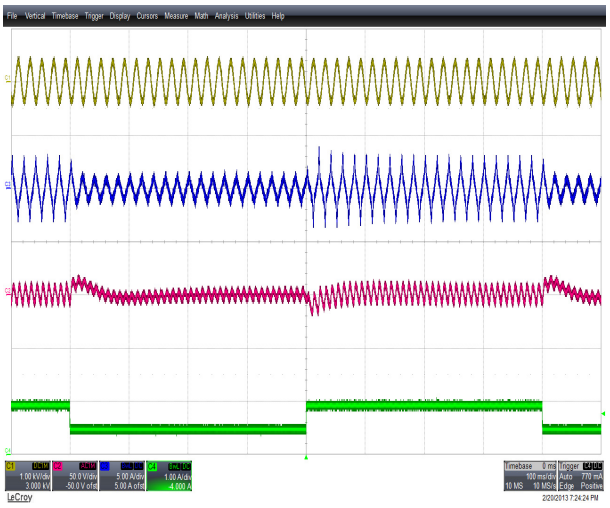

Figure 38 – Transient Response, 264 VAC, 50-100-50% Load Step.
Upper: V_{IN}, 1 kV / div.
Second: I_{IN}, 5 A / div.
Third: V_{OUT} (AC Coupled), 50 V / div.
Lower: I_{OUT}, 1 A / div., 100 ms / div.

12.11 1000 ms Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

12.11.1 50% Load at Output

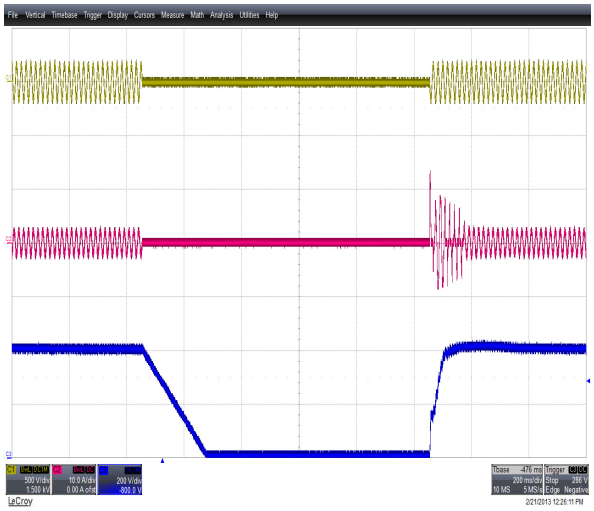

Figure 39 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

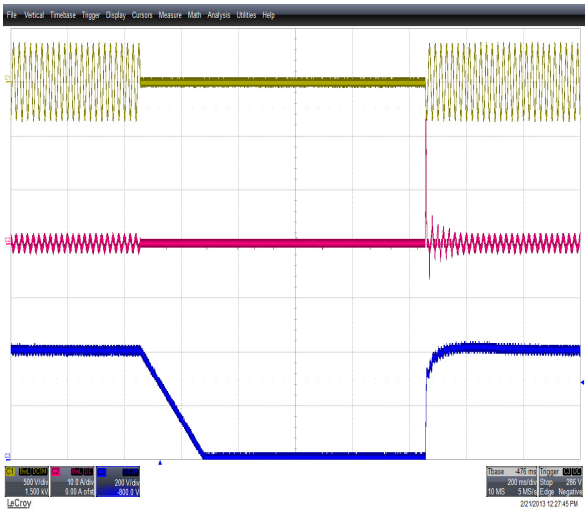

Figure 40 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

12.11.2 Full Load at Output

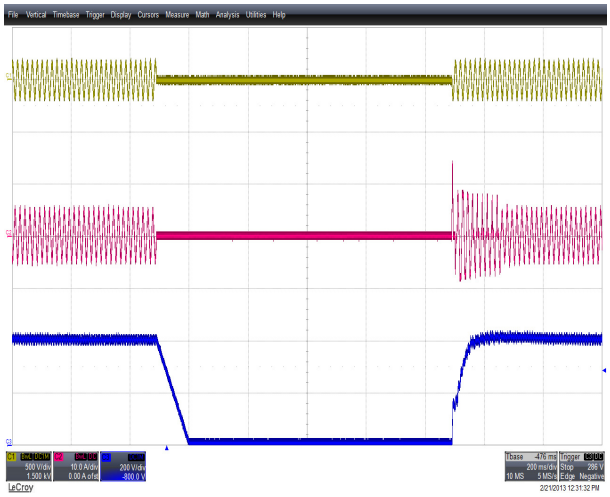

Figure 41 – Line Dropout 115 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

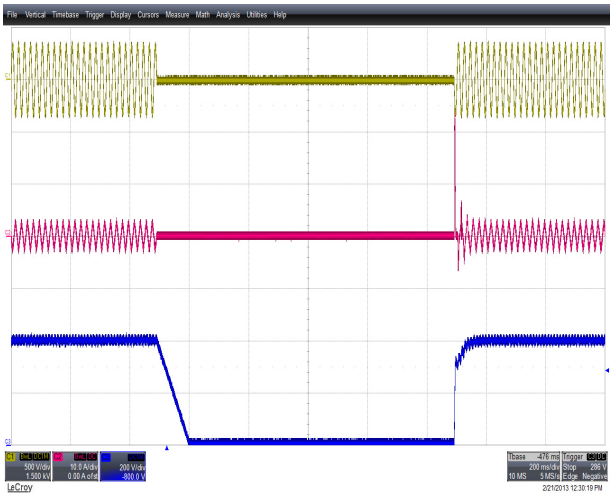

Figure 42 – Line Dropout 230 VAC, 1000 ms.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT}, 200 V / div., 200 ms / div.

12.12 One Cycle Line Dropout (115 VAC / 60 Hz and 230 VAC / 50 Hz)

12.12.1 Full Load at Output

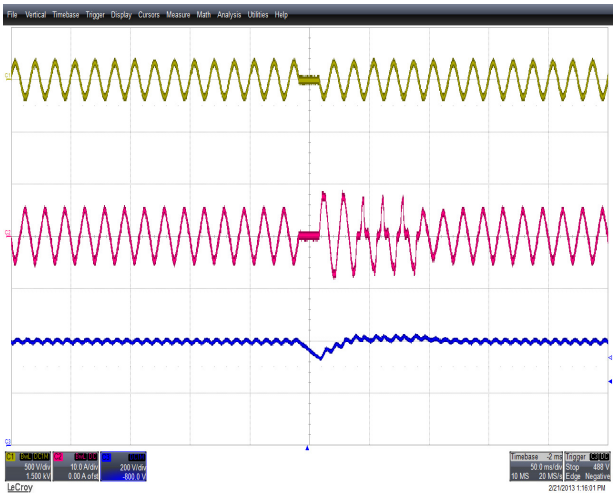

Figure 43 – Line Dropout 115 VAC, 60 Hz.
Upper: V_{IN}, 500 V / div.
Middle:. I_{IN}, 10 A /div.
Lower:, V_{OUT}, 200 V / div., 50 ms / div.

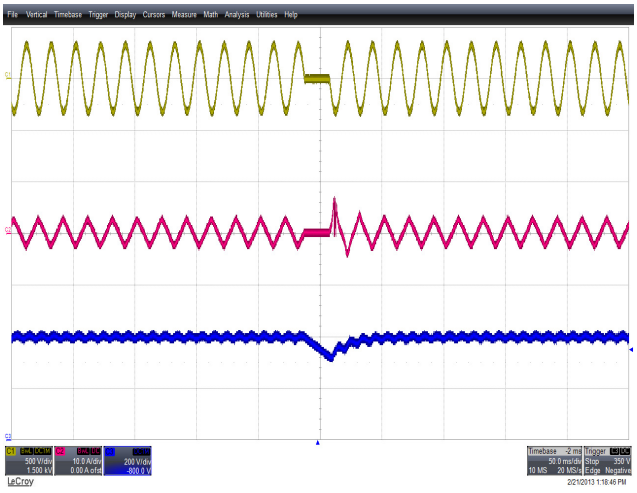

Figure 44 – Line Dropout 230 VAC, 50 Hz.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A /div.
Lower: V_{OUT}, 200 V / div., 50 ms /div.

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12.13 Line Sag (115 VAC ~ 85 VAC ~ 115 VAC, 60 Hz)

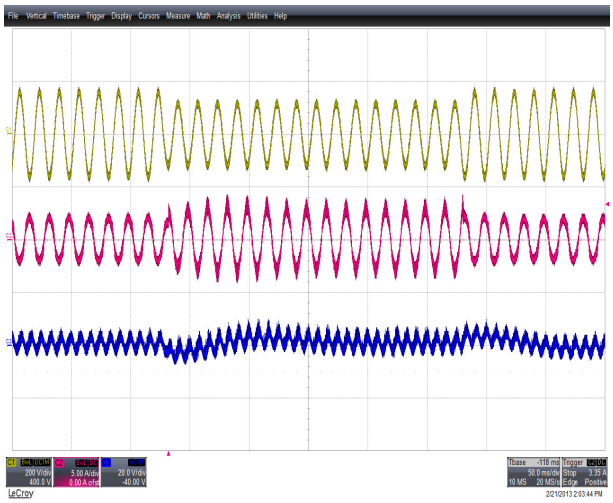

Figure 45 – Line Sag 115 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

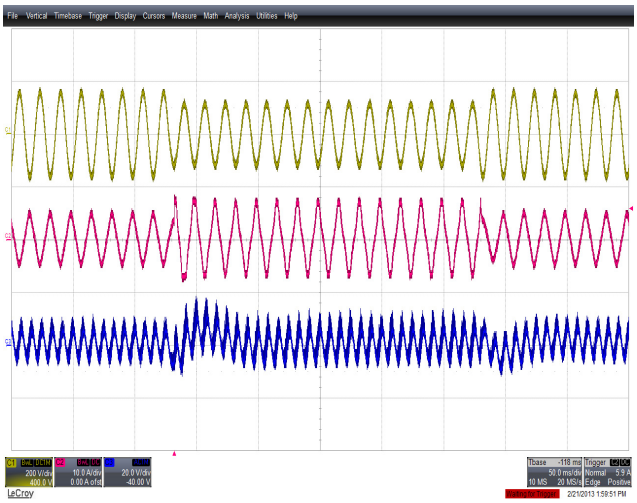

Figure 46 – Line Sag 115 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

12.14 Line Swell (132 VAC ~ 147 VAC ~ 132 VAC, 60 Hz)

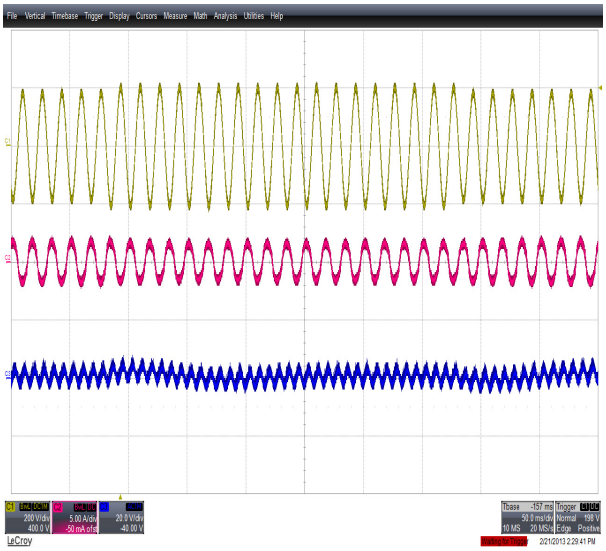

Figure 47 – Line Surge 132 VAC, 50% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

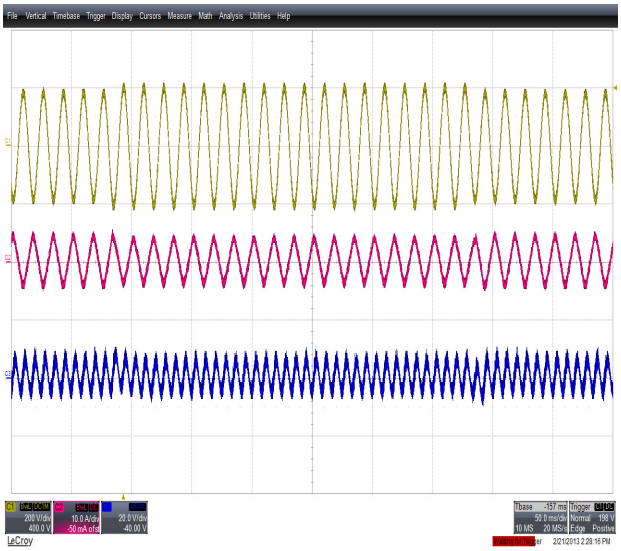

Figure 48 – Line Surge 132 VAC, 100% Load.
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

12.15 Line Sag (230 VAC ~ 170 VAC ~ 230 VAC, 50 Hz)

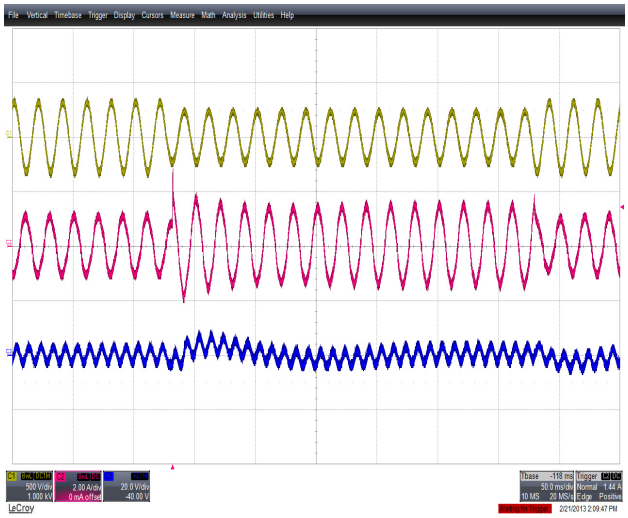

Figure 49 – Line Sag 230 VAC, 50% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 2 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

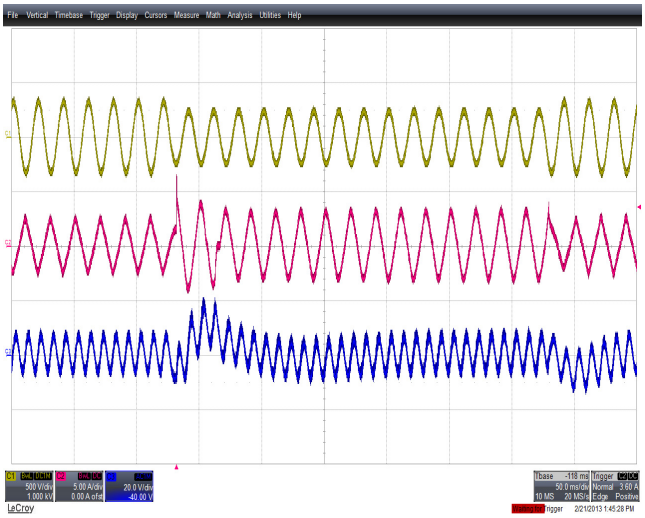

Figure 50 – Line Sag 230 VAC, 100% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT} (AC Coupled), 20 V / div., 50 ms / div.

12.16 Line Swell (264 VAC ~ 293 VAC ~ 264 VAC, 50 Hz)

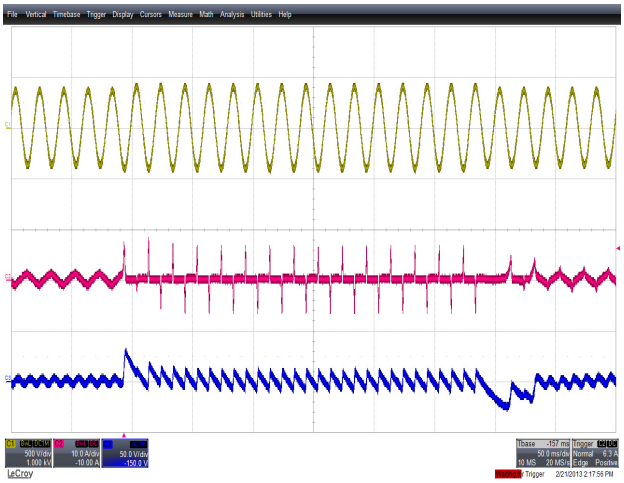

Figure 51 – Line Surge 264 VAC, 50% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT} (AC Coupled), 50 V / div., 50 ms / div.

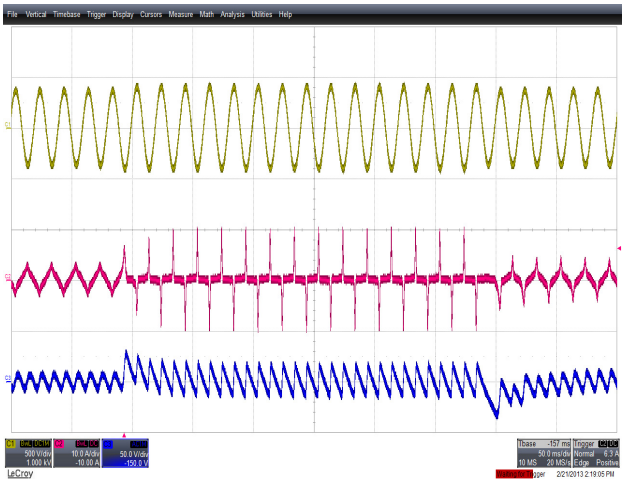

Figure 52 – Line Surge 264 VAC, 100% Load.
Upper: V_{IN}, 500 V / div.
Middle: I_{IN}, 10 A / div.
Lower: V_{OUT} (AC Coupled), 50 V / div., 50 ms / div.

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12.17 Power Good (PG) Signal at 115 VAC and 60 Hz

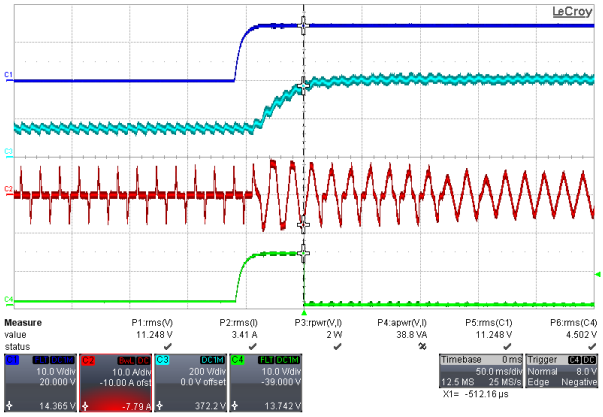

Figure 53 – 115 VAC, Full Load, V_{OUT} Rising Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 10 A / div.
4th: PG, 10 V / div, 50 ms / div.

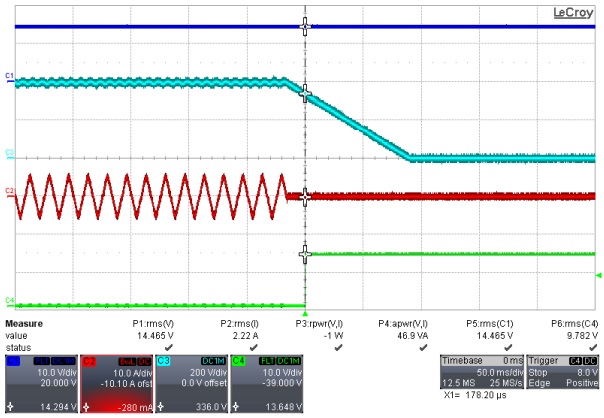

Figure 54 – 115 VAC, Full Load, V_{OUT} Falling Edge.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 10 A / div.
4th: PG, 10 V / div, 50 ms / div.

12.18 Power Good (PG) Signal at 230 VAC and 50 Hz

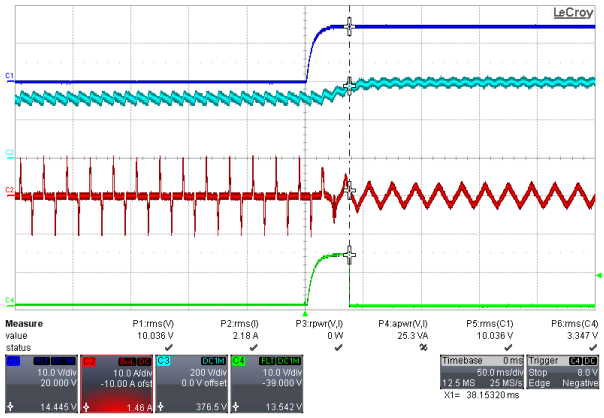

Figure 55 – 230 VAC, No-load.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 10 A / div.
4th: PG, 10 V / div, 50 ms / div.

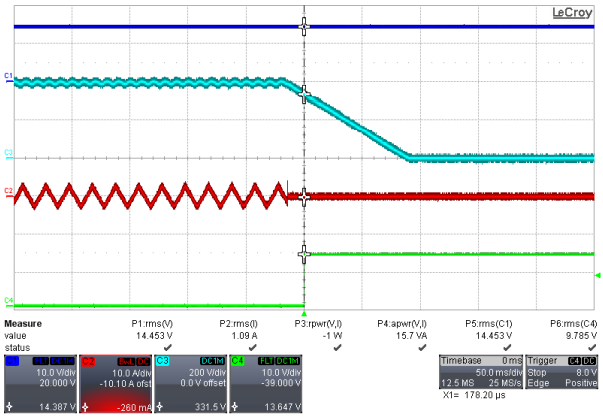

Figure 56 – 230 VAC, Full Load.
1st: V_{CC}, 10 V / div.
2nd: V_{OUT}, 200 V / div.
3rd: I_{IN}, 10 A / div.
4th: PG, 10 V / div, 50 ms / div.

Note: For Figures 54 and 56, input voltage was turned off to verify PG transition threshold.

12.19 Brown-In and Brown-Out at 6 V / Minute Rate

Test conducted by first reducing, followed by increasing input AC voltage source at a rate of 6 V / min. The PFC converter DC output was loaded to 100% of rated load (electronic load), which was programmed to release the load when the DC output of the PFC dropped below 310 V [at brown-out]. The auxiliary +15 V supply is connected to the output of the PFC and discharges the output capacitor of the PFC after the dynamic load is released at brown-out.

Measured PFC Brown-Out Threshold	71 VAC
Measured PFC Brown-In Threshold	80 VAC

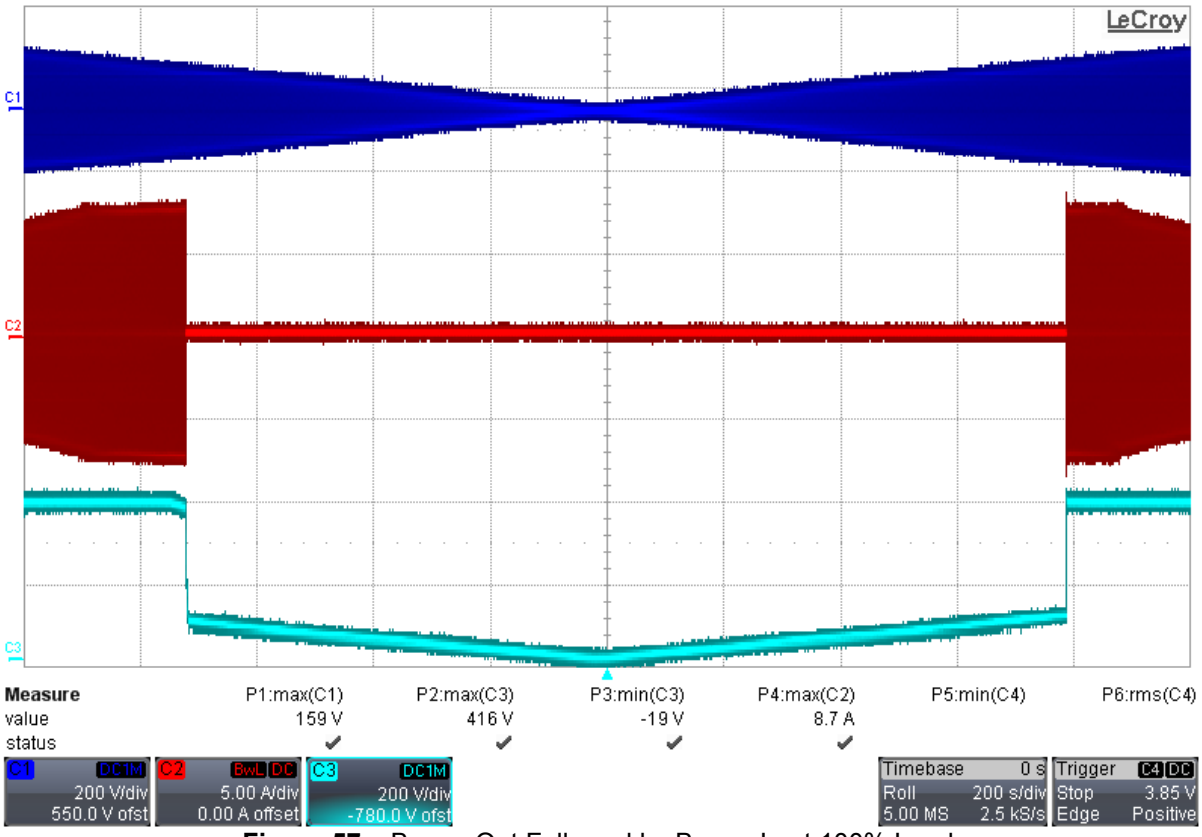

Figure 57 – Brown-Out Followed by Brown-In at 100% Load.
Top: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div., 200 s / div.

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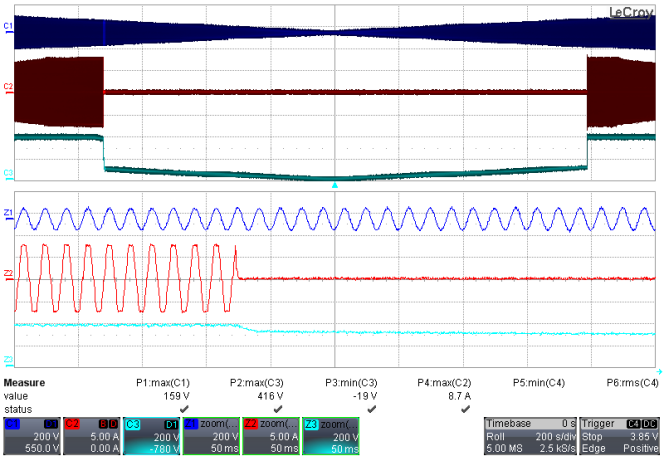

Figure 58 – Brown-out with 100% Load, Zoom-in
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div, 50 ms / div.

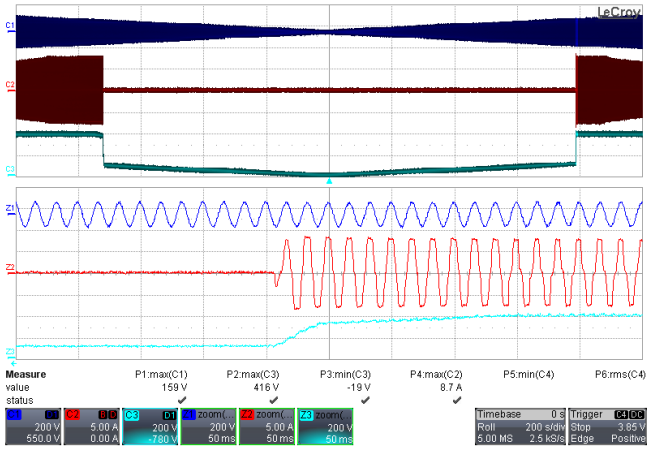

Figure 59 – Brown-in with 100% Load, Zoom-in
Upper: V_{IN}, 200 V / div.
Middle: I_{IN}, 5 A / div.
Lower: V_{OUT}, 200 V / div, 50 ms / div.

12.20 Drain Voltage and Inductor Current

Since PFC output diode is integrated into the package, there is no direct access of the MOSFET drain current. Therefore inductor current was measured at jumper JP1 location by replacing JP1 with a short wire loop in order to insert the current probe. The Drain voltage was measured at the DRAIN and SOURCE pins of IC U1.

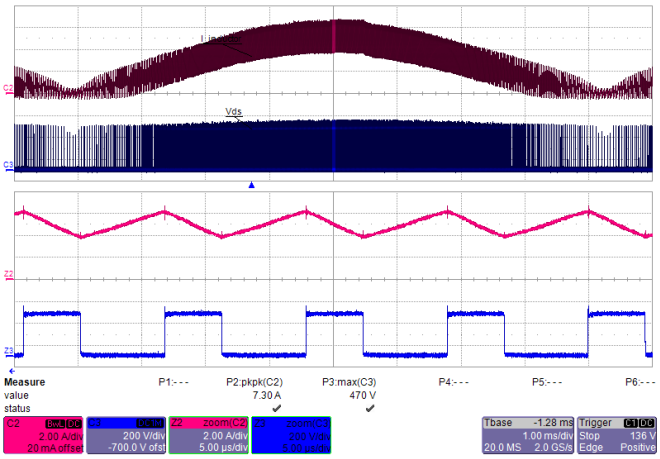

Figure 60 – Input Voltage 115 VAC, 100% Load.
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN}, 200 V / div., 1 ms / div.
Zoom Upper: $I_{INDUCTOR}$, 2 A / div.
Zoom Lower: V_{DRAIN}, 200 V / div., 5 µs / div.

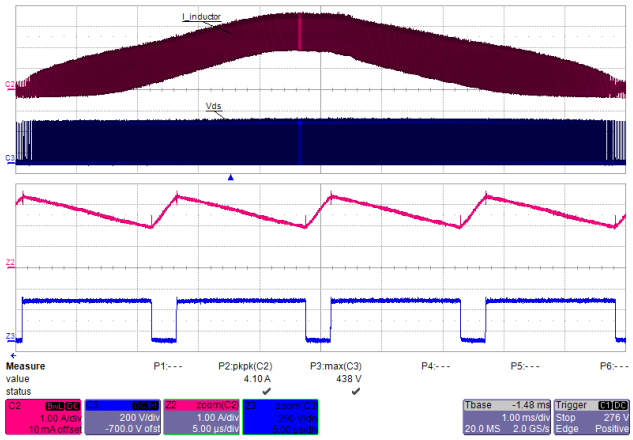

Figure 61 – Input Voltage 230 VAC, 100% Load.
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN}, 200 V / div., 1 ms / div.
Zoom Upper: $I_{INDUCTOR}$, 1 A / div.
Zoom Lower: V_{DRAIN}, 200 V / div., 5 µs / div.

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12.21 Output Ripple Measurements

12.21.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with one capacitor 0.02 μF/1 kV ceramic disc type tied in parallel across the probe tip.

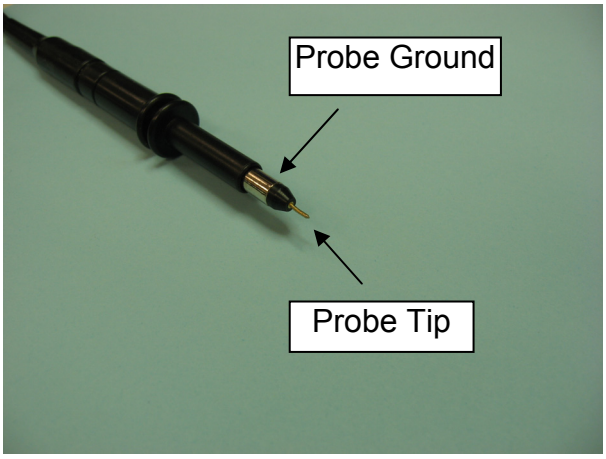

Figure 62 – Oscilloscope Probe Prepared for Ripple Measurement (End cap and ground lead removed.)

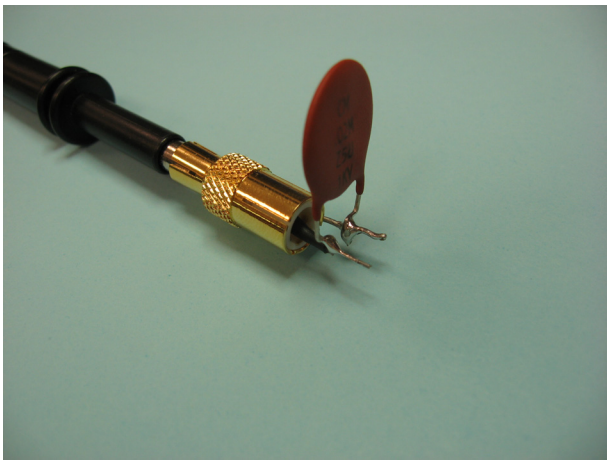

Figure 63 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter (Modified with wires for ripple measurement, and one parallel decoupling capacitor added.)

12.21.2 Measurement Results

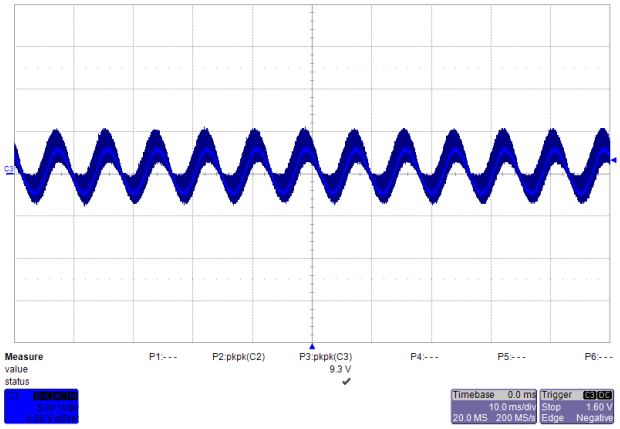

Figure 64 – Ripple, 90 VAC, 50% Load.
10 ms, 5 V / div.

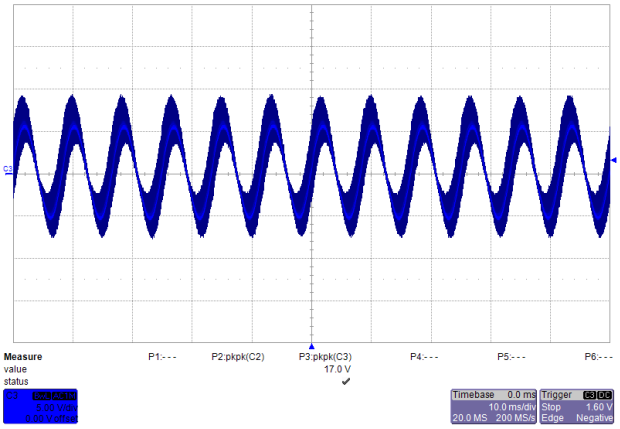

Figure 65 – Ripple, 90 VAC, 100% Load.
10 ms, 5 V / div.

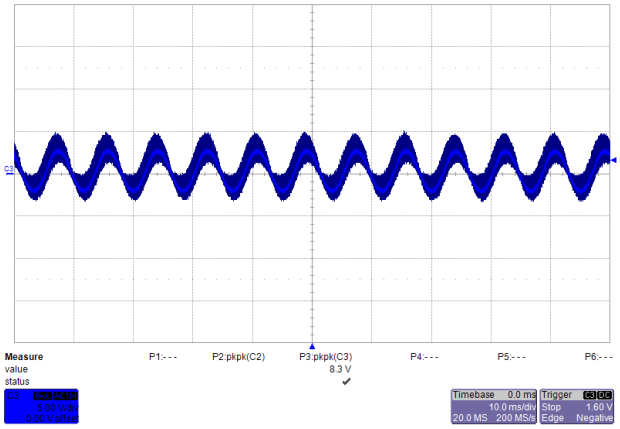

Figure 66 – Ripple, 115 VAC, 50% Load.
10 ms, 5 V / div.

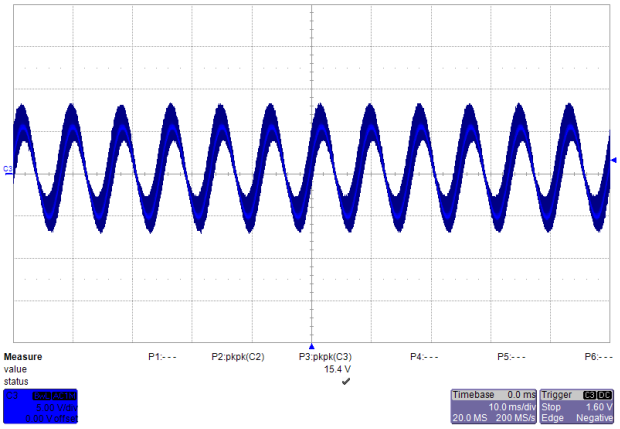

Figure 67 – Ripple, 115 VAC, 100% Load.
10 ms, 5 V / div.

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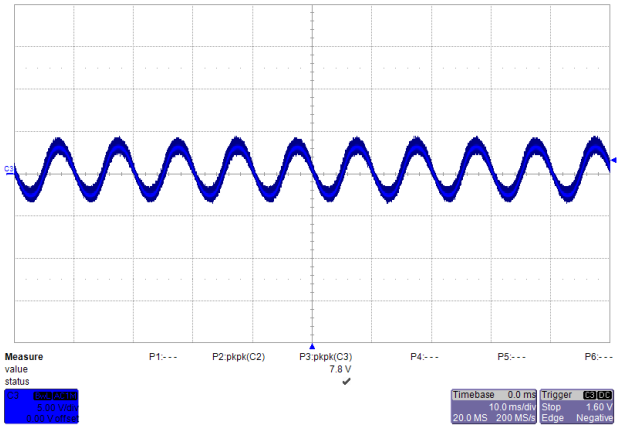

Figure 68 – Ripple, 230 VAC, 50% Load.
10 ms, 5 V / div.

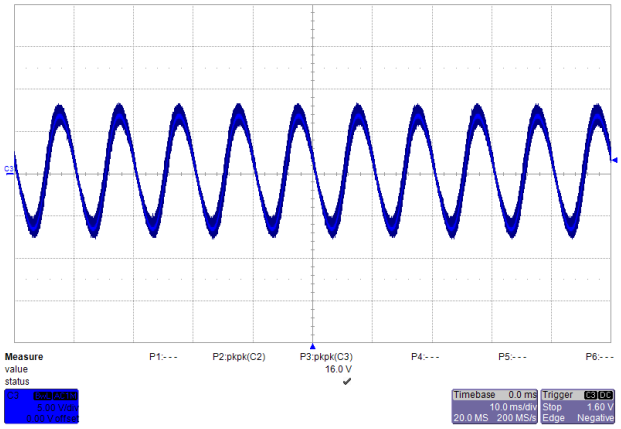

Figure 69 – Ripple, 230 VAC, 100% Load.
10 ms, 5 V / div.

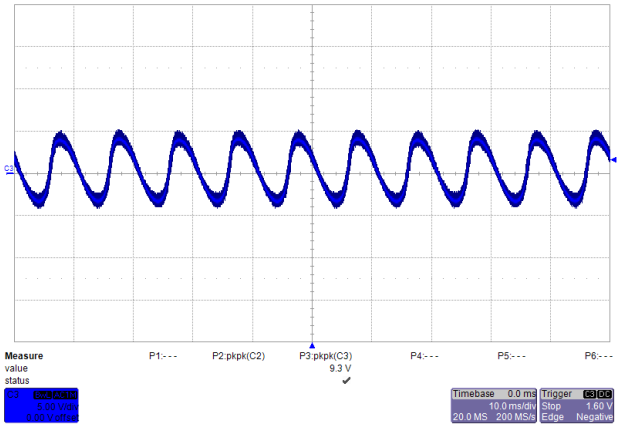

Figure 70 – Ripple, 264 VAC, 50% Load.
10 ms, 5 V / div.

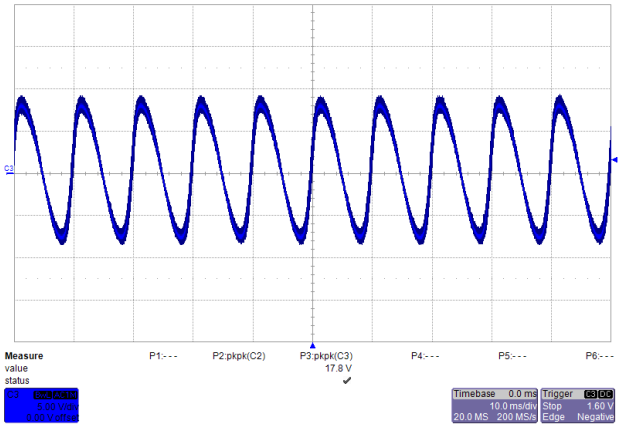

Figure 71 – Ripple, 264 VAC, 100% Load.
10 ms, 5 V / div.

13 Gain-Phase Measurement Procedure and Results

- The PFC stage is supplied from an adjustable DC source for this test. Connect the circuit as shown in figure below. Open the top end of the feedback divider network and insert a 100 Ω–2 W resistor in series as shown. The signal injected in the loop for gain–phase measurement will be injected across this resistor.
- Nodes A and B (two ends of the injection resistor) are connected to Channel 1 and Channel 2 of the frequency response analyzer using high voltage x100 attenuator probes. GND leads of both probes are connected to output return as shown.
- The signal to be injected is isolated using the Bode–Box injection transformer model – 200–000 from Venable Industries.
- Test Procedure:
- Adjust the input voltage to 150 VDC and confirm that the PFC output voltage is within regulation limits.
- Inject a signal from the frequency response analyzer.
- The injected signal can be seen in the output voltage ripple of the PFC.
- Plot the gain phase pot by sweeping the injected signal frequency from 2 Hz to 1000 Hz.

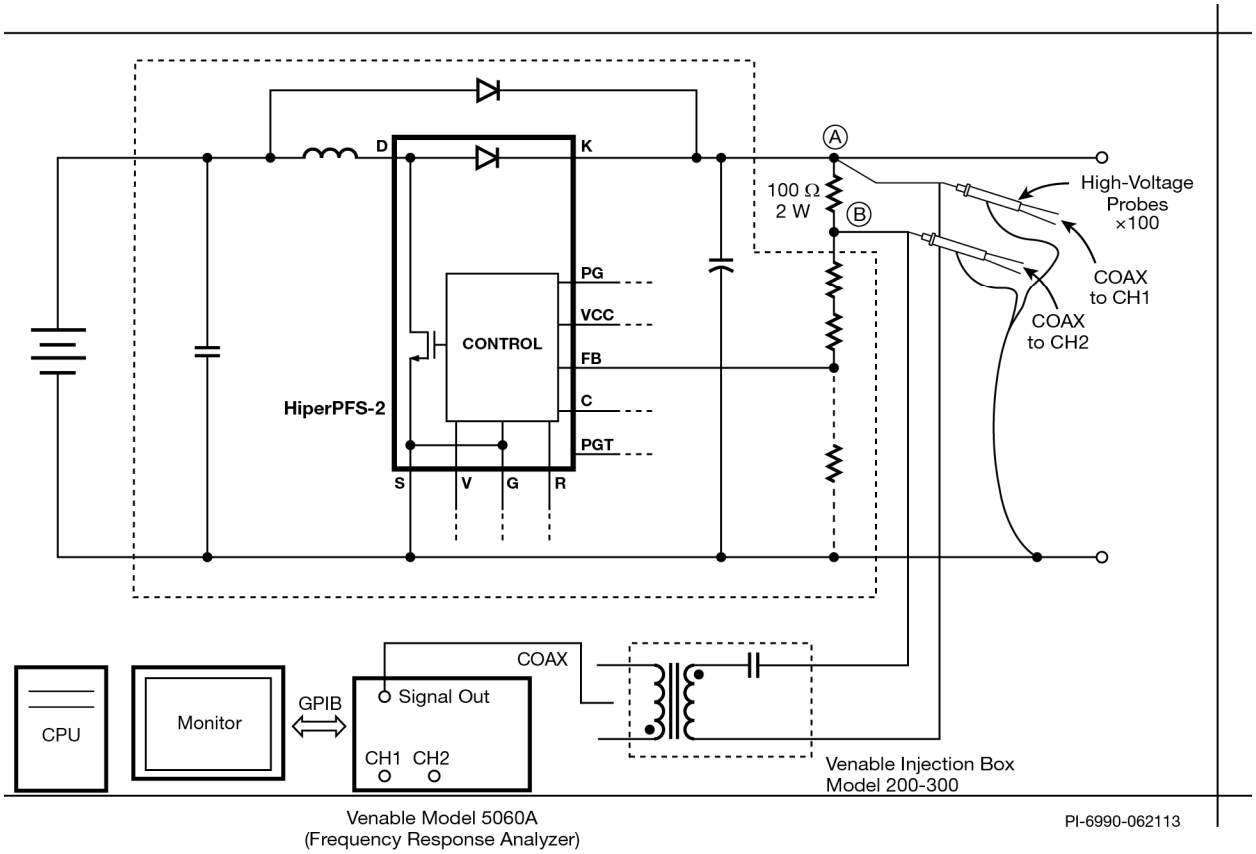

Figure 72 – System Test Set-up for Loop Gain-Phase Measurement.

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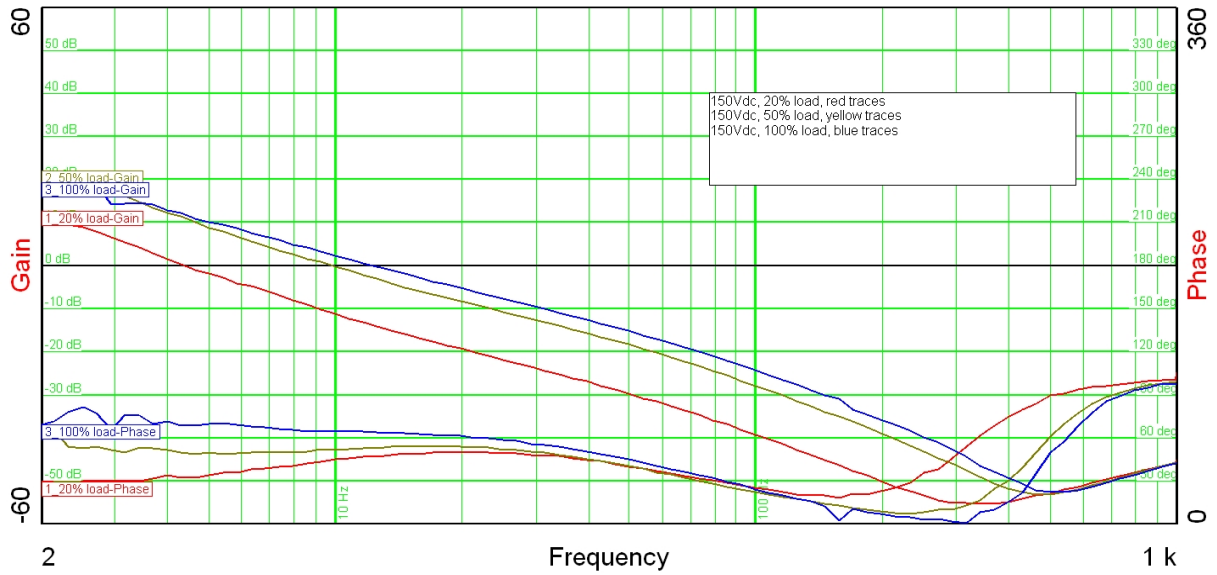

Figure 73 – Bode Plot with V_{IN} = 150 VDC at 100%, 50% and 20% Load.

14 Line Surge Test

Differential input line 1.2 kV / 50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 50 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail; # strikes)
C.M.		**(12Ω source)**		**10 strikes each level**
+500	230	L1 to PE	90	Pass
-500	230	L1 to PE	270	Pass
+500	230	L2 to PE	270	Pass
-500	230	L2 to PE	90	Pass
+500	230	L1,L2 to PE	90[1]	Pass
-500	230	L1,L2 to PE	90	Pass
D.M.		**(2Ω source)**		
+500	230	L1 to L2	90[2]	Pass
-500	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		
+1000	230	L1 to PE	90	Pass
-1000	230	L1 to PE	270	Pass
+1000	230	L2 to PE	270	Pass
-1000	230	L2 to PE	90	Pass
+1000	230	L1,L2 to PE	90[1]	Pass
-1000	230	L1,L2 to PE	90	Pass
D.M.		**(2Ω source)**		
+1000	230	L1 to L2	90[2]	Pass
-1000	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		**10 strikes each level**
+1500	230	L1 to PE	90	Pass
-1500	230	L1 to PE	270	Pass
+1500	230	L2 to PE	270	Pass
-1500	230	L2 to PE	90	Pass
+1500	230	L1,L2 to PE	90[1]	Pass
-1500	230	L1,L2 to PE	90	Pass
C.M.		**(12Ω source)**		**10 strikes each level**
+2000	230	L1 to PE	90	Pass
-2000	230	L1 to PE	270	Pass
+2000	230	L2 to PE	270	Pass
-2000	230	L2 to PE	90	Pass
+2000	230	L1,L2 to PE	90[1]	Pass
-2000	230	L1,L2 to PE	90	Pass

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15 EMI Scans

15.1 EMI Test Set-up

Using a plexi-glass board with the underside copper coated, electrically connect the copper side of the board to the capacitor side of ferrite bead L1 with a wire clip. The evaluation board should be placed on top of the plexi-glass board. Connect output connector J4 to a high-voltage resistive DC load. Supply auxiliary power to J3 with an RDR-91 supply powered from the PFC output voltage. All interconnections should be made as short as possible. See below figure for set-up.

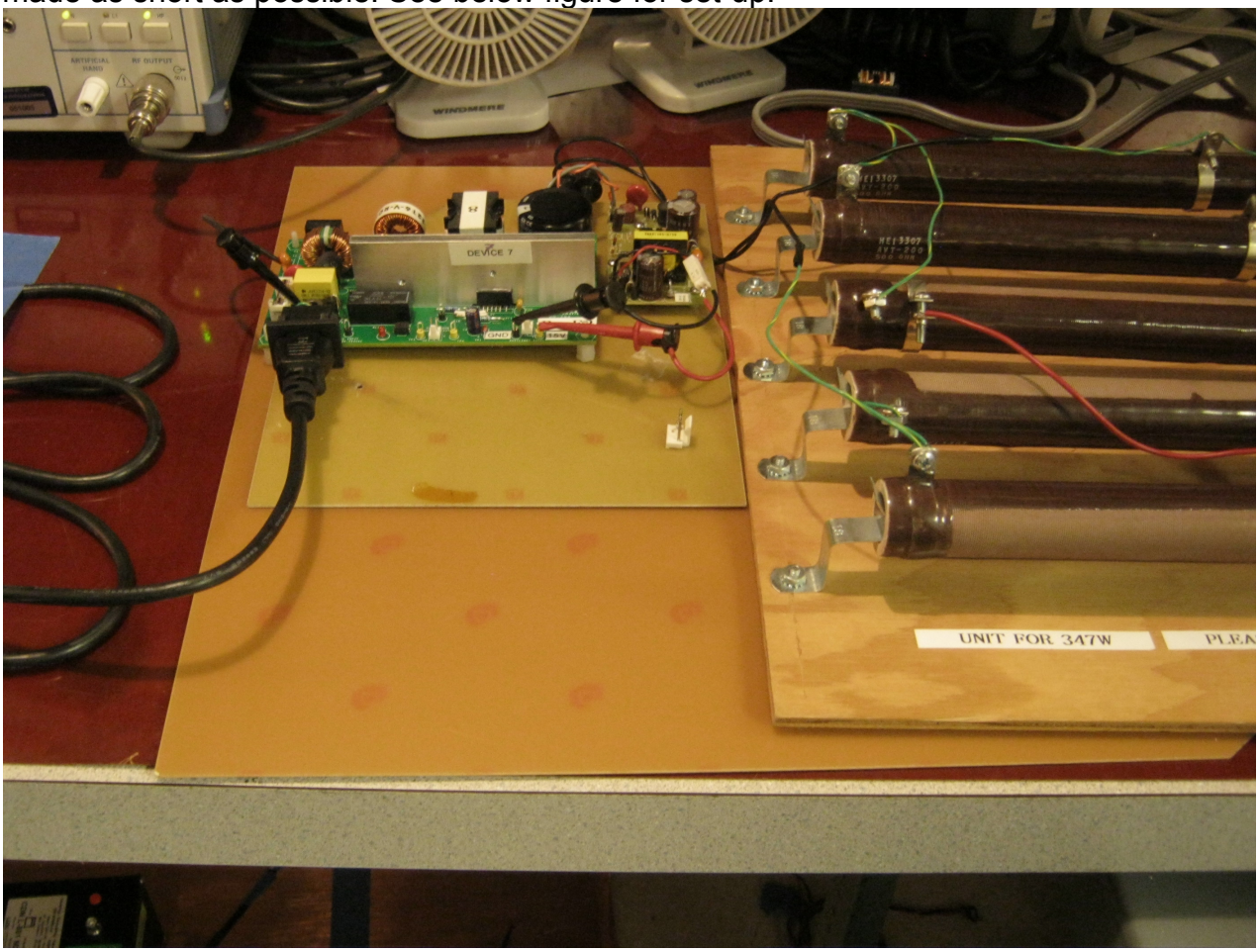

Figure 74 – EMI Test Set-Up.

15.2 EMI Scans

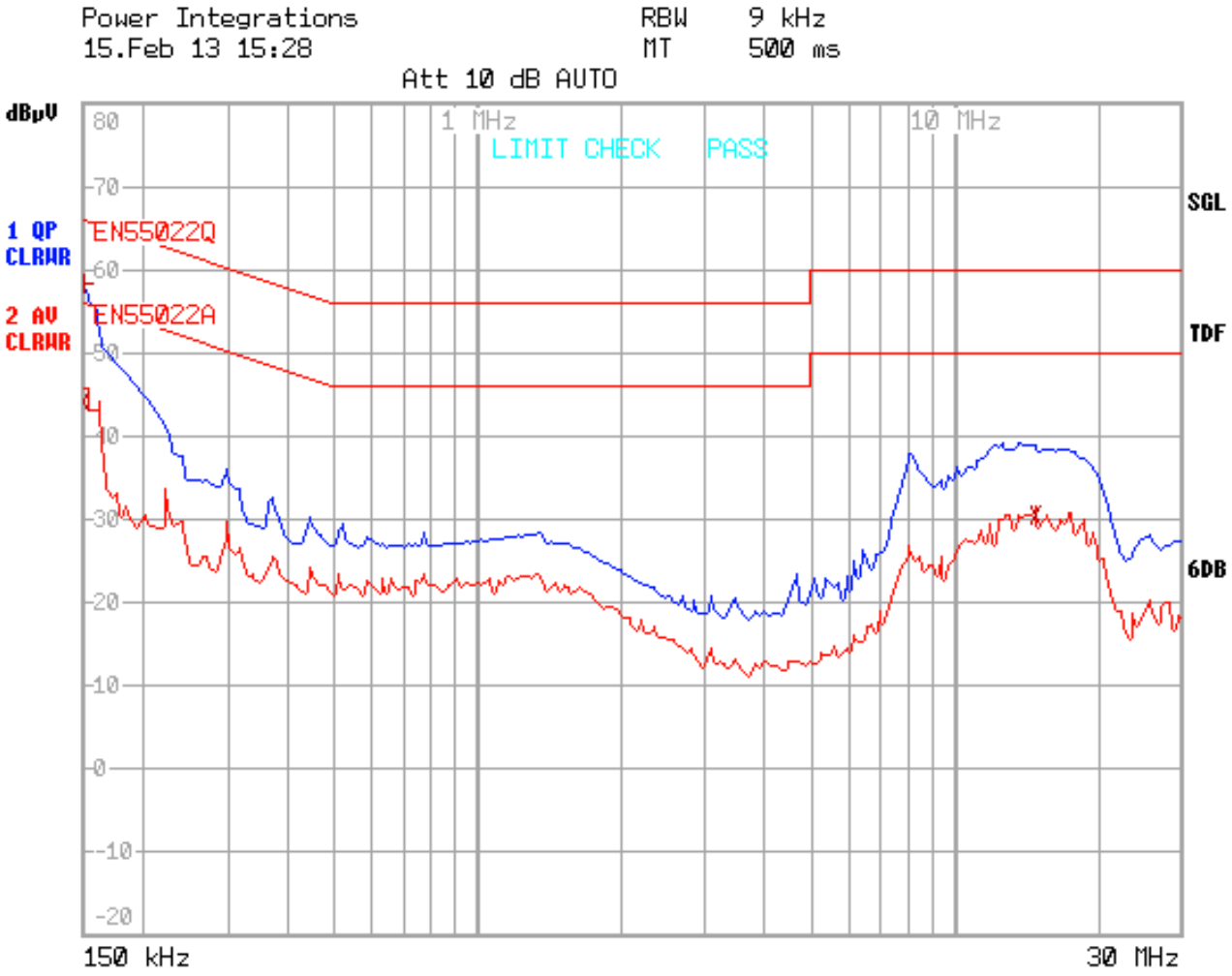

Figure 75 – 115 VAC, 100% Load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	150 kHz	58.27	L1 gnd	-7.72
2	Average	150 kHz	44.23	L1 gnd	-11.76
2	Average	14.8364879374 MHz	30.61	L1 gnd	-19.38

Figure 76 – 115 VAC, 100% Load EMI Measurement Results.

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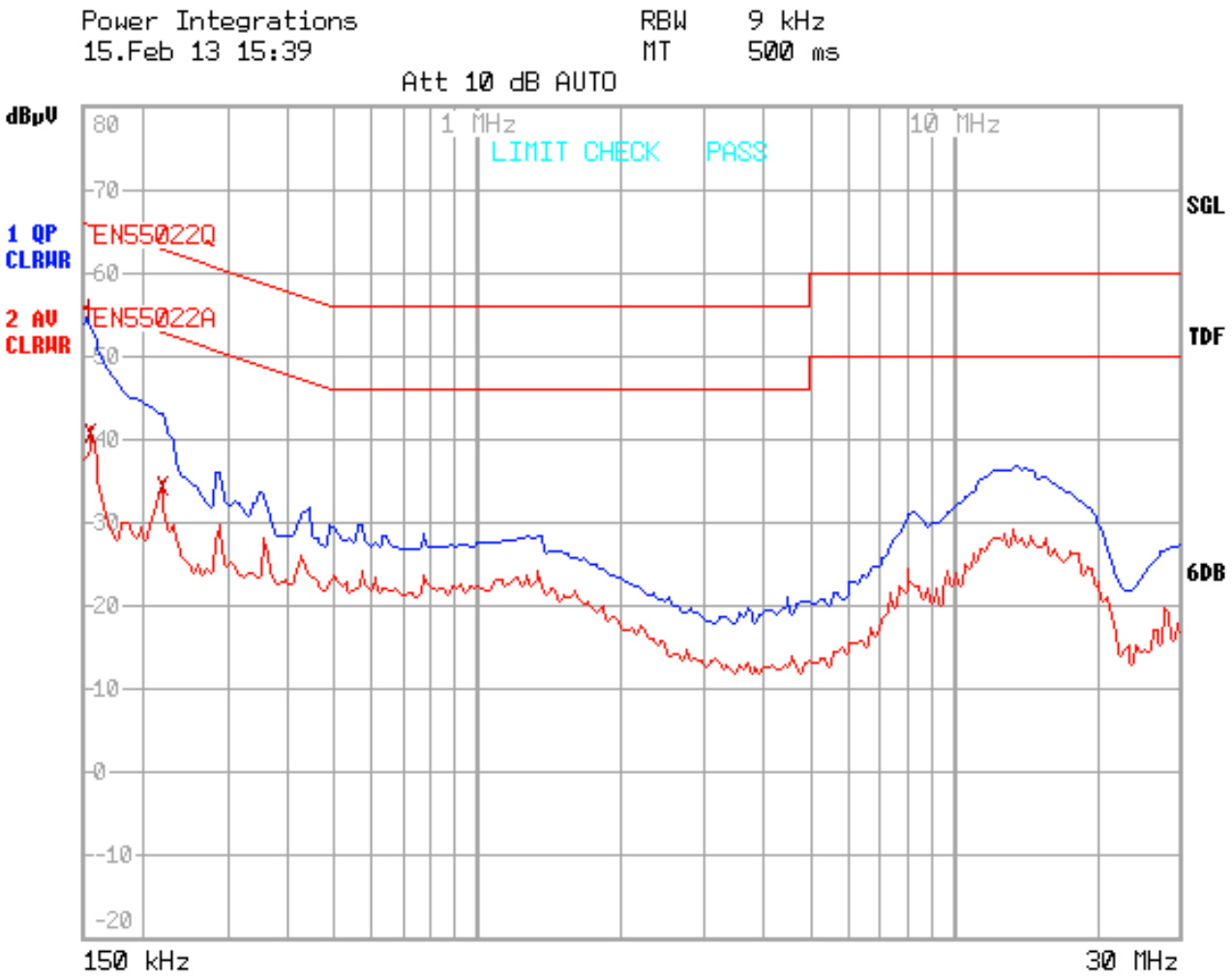

Figure 77 – 230 VAC, 100% Load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
1	Quasi Peak	153 kHz	55.74	L1 gnd	-10.09
2	Average	156.06 kHz	40.70	L1 gnd	-14.97
2	Average	218.521675879 kHz	34.52	L1 gnd	-18.35

Figure 78 – 230 VAC, 100% Load EMI Measurement Results.

16 Appendix A - Test Set-up for Efficiency Measurement

The following setup is recommended for system efficiency, PF and THDi measurements. Use of high resolution meters is recommended for output current and output voltage measurements. An 80 mm fan powered by 12 VDC is attached to the board edge for forced air cooling. See figure below for a typical equipment set-up.

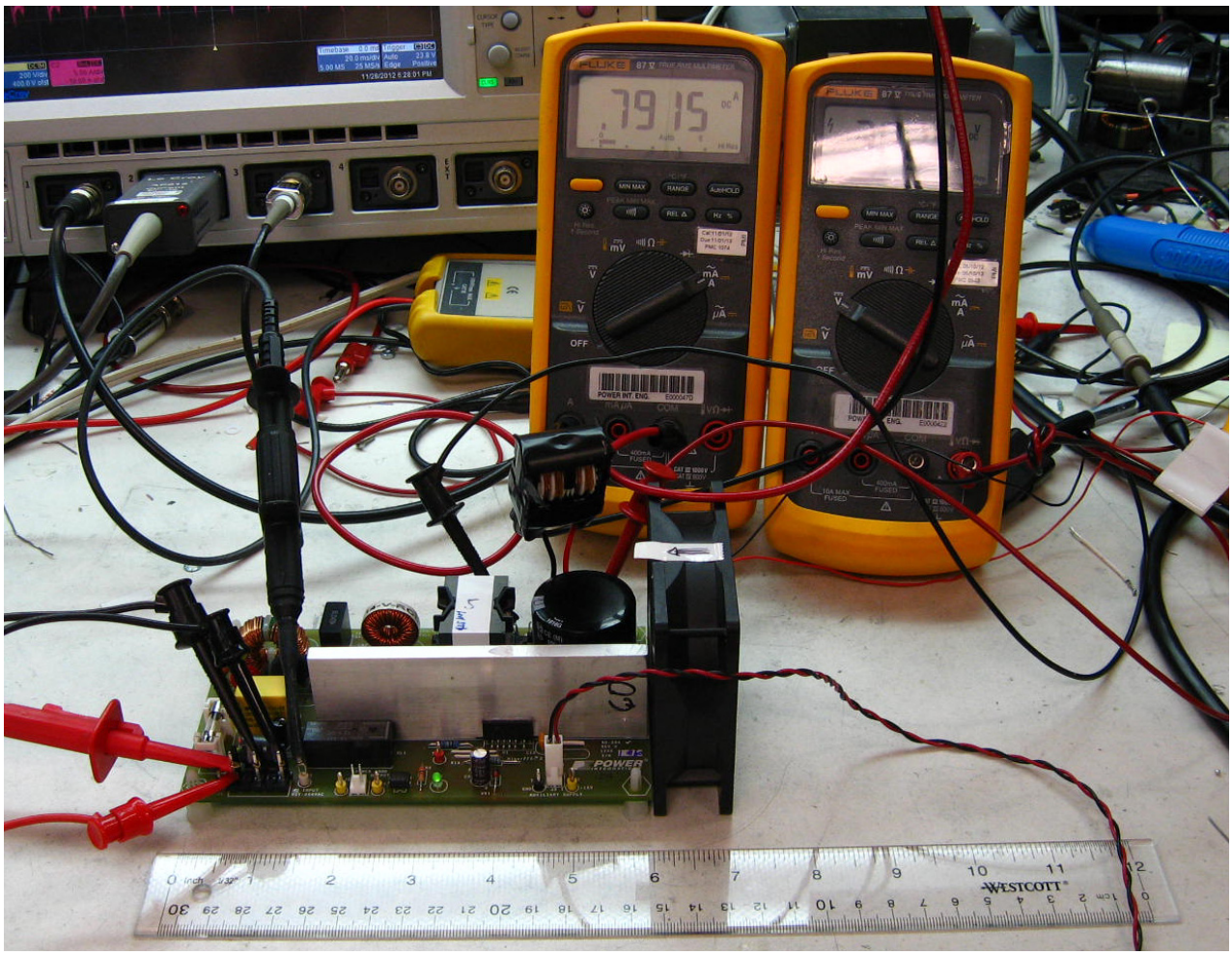

Figure 79 – Front View of the Test Set-Up for Efficiency, PF and THDi Measurements.

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17 Revision History

Date	Author	Revision	Description & changes	Reviewed
04-Jun-13	NZ	1.0	Initial Release	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail:
eurosales@powerint.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail:
taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail:
indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

EUROPE HQ
1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail:
eurosales@powerint.com

CHINA (SHENZHEN)
3rd Floor, Block A,
Zhongtou International Business
Center, No. 1061, Xiang Mei Rd,
FuTian District, ShenZhen,
China, 518040
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail:
eurosales@powerint.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com