

































## 8 Transformer Design Spreadsheet

ACDC_LinkSwitch-PH_061010; Rev.1.1; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_061010: Flyback Transformer Design Spreadsheet
<b>ENTER APPLICATION VARIABLES</b>					
Dimming required	NO		NO		Select 'YES' option if dimming is required. Otherwise select 'NO'.
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	50.00			V	Typical output voltage of LED string at full load
VO_MAX			55.00	V	Maximum expected LED string Voltage.
VO_MIN			45.00	V	Minimum expected LED string Voltage.
V_OVP			60.50	V	Over-voltage protection setpoint
IO	0.30				Typical full load LED current
PO			15.0	W	Output Power
n	0.80		0.8		Estimated efficiency of operation
VB	20		20	V	Bias Voltage
<b>ENTER LinkSwitch-PH VARIABLES</b>					
LinkSwitch-PH	LNK406			Universal	115 Doubled/230V
Chosen Device		LNK406	Power Out	22.5W	22.5W
Current Limit Mode	FULL		FULL		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			1.48	A	Minimum current limit
ILIMITMAX			1.69	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			38.7	uA	V pin current
RV			3.909	M-ohms	Upper V pin resistor
RV2			1.402	M-ohms	Lower V pin resistor
IFB	130.00		130.0	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			130.8	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.50			V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.70			V	Bias Winding Diode Forward Voltage Drop
<b>Key Design Parameters</b>					
KP	1.05		1.05		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			809	uH	Primary Inductance
VOR	90.00		90	V	Reflected Output Voltage.
Expected IO (average)			0.29	A	Expected Average Output Current
KP_VACMAX		Info	1.28		!!! Info. PF at high line may be less than 0.9. Decrease KP for higher PF
TON_MIN			1.62	us	Minimum on time at maximum AC input voltage
PCLAMP			0.11	W	Estimated dissipation in primary clamp
<b>ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES</b>					
Core Type	EER2510		EER2510		
Bobbin		#N/A		P/N:	#N/A
AE	0.5400		0.54	cm^2	Core Effective Cross Sectional Area
LE	3.6000		3.6	cm	Core Effective Path Length
AL			#N/A	nH/T^2	Ungapped Core Effective Inductance
BW	4.2		4.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4		Number of Primary Layers
NS	30		30		Number of Secondary Turns
<b>DC INPUT VOLTAGE PARAMETERS</b>					
VMIN			127	V	Peak input voltage at VACMIN





VMAX			375	V	Peak input voltage at VACMAX
<b>CURRENT WAVEFORM SHAPE PARAMETERS</b>					
DMAX			0.42		Minimum duty cycle at peak of VACMIN
IAVG			0.18	A	Average Primary Current
IP			1.04	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.31	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
<b>TRANSFORMER PRIMARY DESIGN PARAMETERS</b>					
LP			809	uH	Primary Inductance
NP			53		Primary Winding Number of Turns
NB			12		Bias Winding Number of Turns
ALG			283	nH/T^2	Gapped Core Effective Inductance
BM			2917	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3530	Gauss	Peak Flux Density (BP<3700)
BAC			1459	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			#N/A		Relative Permeability of Ungapped Core
LG		#N/A	#N/A	mm	#N/A
BWE			16.8	mm	Effective Bobbin Width
OD			0.31	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.26	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			325	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
LP_TOL			10		Tolerance of primary inductance
<b>TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)</b>					
<b>Lumped parameters</b>					
ISP			1.86	A	Peak Secondary Current
ISRMS			0.60	A	Secondary RMS Current
IRIPPLE			0.52	A	Output Capacitor RMS Ripple Current
CMS			120	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			29	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.14	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
<b>VOLTAGE STRESS PARAMETERS</b>					
VDRAIN			563	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			271	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			110	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
<b>FINE TUNING (Enter measured values from prototype)</b>					
<b>V pin Resistor Fine Tuning</b>					
RV1			3.91	M-ohms	Upper V Pin Resistor Value
RV2			1.40	M-ohms	Lower V Pin Resistor Value
VAC1			115.0	V	Test Input Voltage Condition1
VAC2			230.0	V	Test Input Voltage Condition2
IO_VAC1			0.30	A	Measured Output Current at VAC1
IO_VAC2			0.30	A	Measured Output Current at VAC2
RV1 (new)			3.91	M-ohms	New RV1
RV2 (new)			1.40	M-ohms	New RV2
V_OV			318.3	V	Typical AC input voltage at which OV shutdown will be triggered



V_UV			70.8	V	Typical AC input voltage beyond which power supply can startup
<b>FB pin resistor Fine Tuning</b>					
RFB1			131	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+012	k-ohms	Lower FB Pin Resistor Value
VB1			18.0	V	Test Bias Voltage Condition1
VB2			22.0	V	Test Bias Voltage Condition2
IO1			0.30	A	Measured Output Current at Vb1
IO2			0.30	A	Measured Output Current at Vb2
RFB1 (new)			130.8	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

Note: Actual values used for  $R_{V1} = 3.4 \text{ M}\Omega$ ,  $R_{V2} = 1.8 \text{ M}\Omega$ . Measured PF at 230 VAC was 0.9.



## 9 Performance Data

All measurements performed at room temperature. Yokogawa WT210 power meter was used for input power and output power measuring.

### 9.1 Efficiency vs. Line

$V_{IN}$ (VAC)	$P_{IN}$ (W)	$V_o$ (V)	$I_o$ (A)	$P_o$ (W)	Efficiency (%)
90	16.63	49.53	0.286	14.17	85.18
100	16.97	49.54	0.293	14.52	85.53
110	17.30	49.77	0.300	14.93	86.31
120	17.57	49.87	0.305	15.21	86.57
130	17.72	49.93	0.308	15.38	86.79
140	17.78	49.96	0.310	15.49	87.11
150	17.81	49.97	0.311	15.54	87.26
160	17.78	49.96	0.311	15.54	87.39
170	17.68	49.92	0.310	15.48	87.53
180	17.55	49.87	0.308	15.36	87.52
190	17.39	49.8	0.306	15.24	87.63
200	17.23	49.74	0.304	15.12	87.76
210	17.04	49.68	0.301	14.95	87.76
220	16.83	49.6	0.298	14.78	87.82
230	16.62	49.52	0.294	14.56	87.60
240	16.39	49.53	0.290	14.36	87.64
250	16.12	49.33	0.286	14.11	87.52
265	15.71	49.17	0.279	13.72	87.32



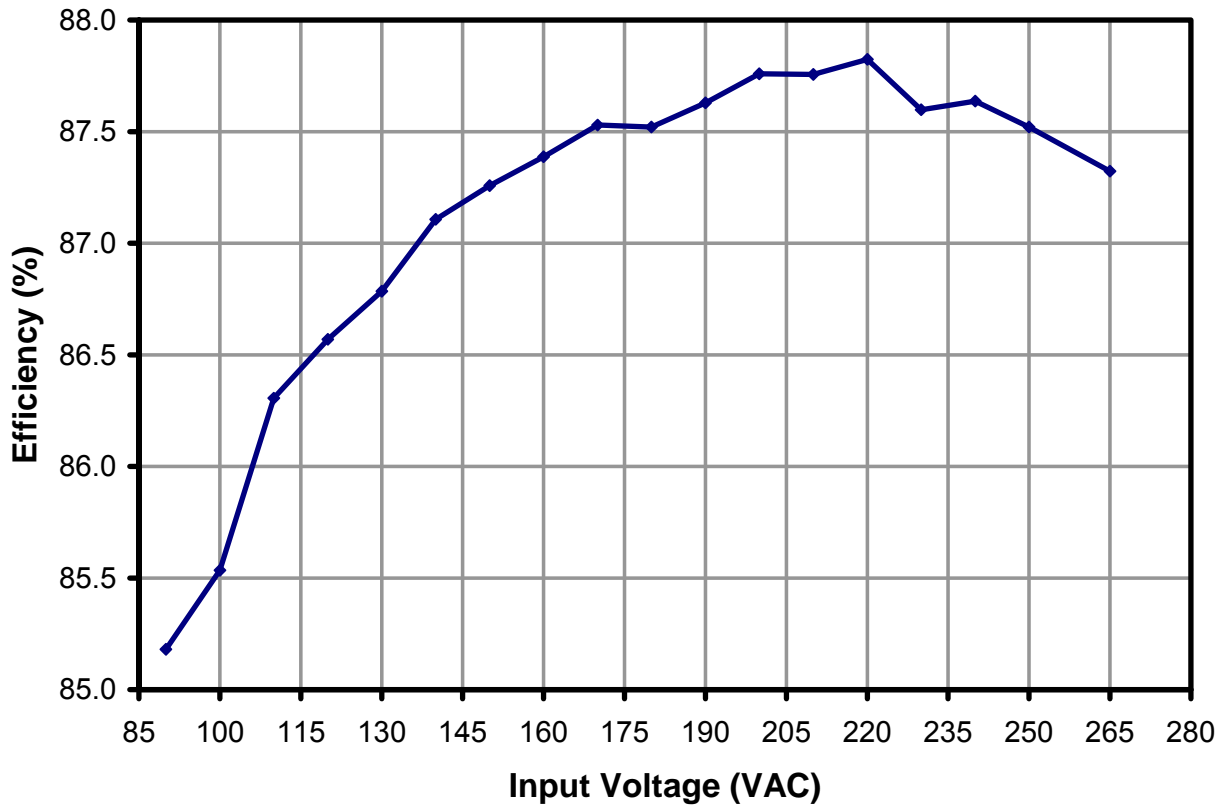


Figure 9 – Efficiency vs. Input Voltage, Room Temperature.



9.2 Constant Current vs. Line

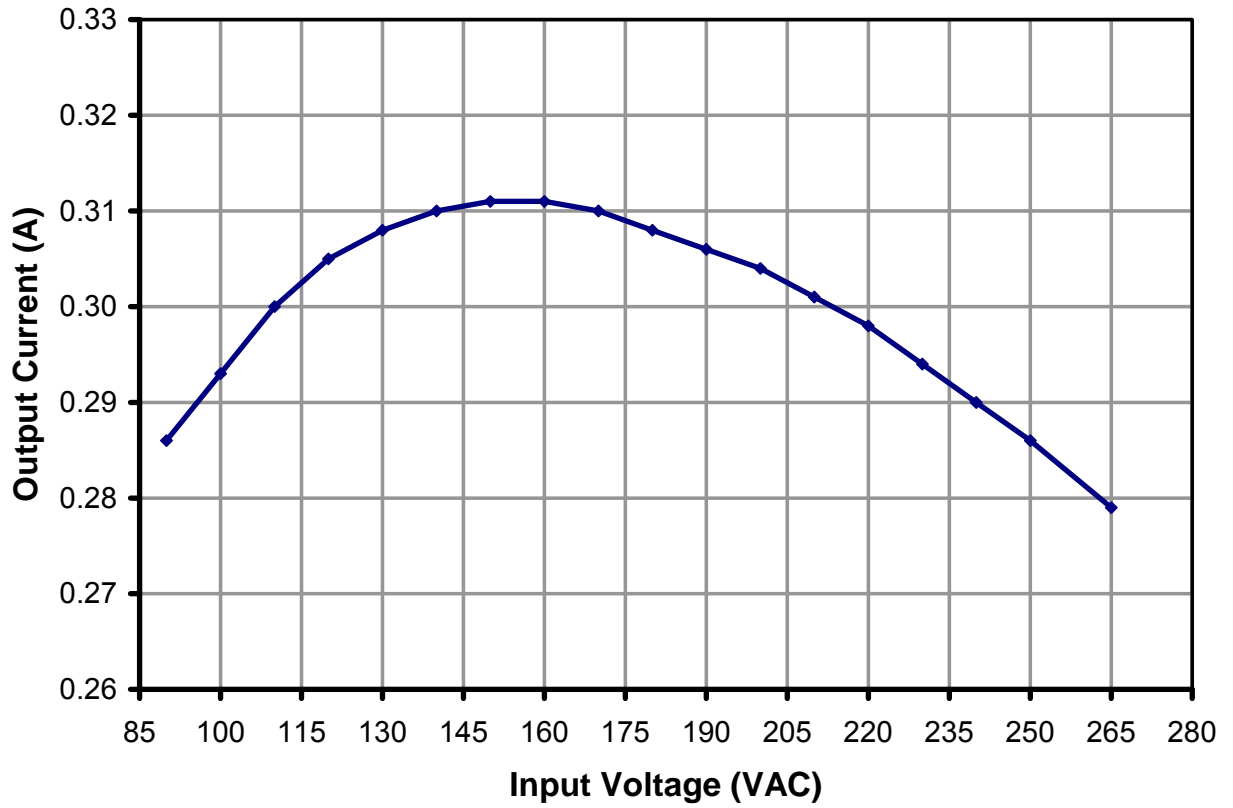


Figure 10 – Output Current vs. Line, Room Temperature.



### 9.3 Power Factor vs. Line, Full Load

$V_{IN}$ (VAC)	$P_{IN}$ (W)	$V_o$ (V)	$I_o$ (A)	$P_o$ (W)	PF
90	16.63	49.53	0.286	14.17	0.9796
100	16.97	49.54	0.293	14.52	0.9745
110	17.30	49.77	0.300	14.93	0.9715
120	17.57	49.87	0.305	15.21	0.9687
130	17.72	49.93	0.308	15.38	0.966
140	17.78	49.96	0.310	15.49	0.9638
150	17.81	49.97	0.311	15.54	0.9615
160	17.78	49.96	0.311	15.54	0.9592
170	17.68	49.92	0.310	15.48	0.9571
180	17.55	49.87	0.308	15.36	0.955
190	17.39	49.8	0.306	15.24	0.9528
200	17.23	49.74	0.304	15.12	0.9505
210	17.04	49.68	0.301	14.95	0.9484
220	16.83	49.6	0.298	14.78	0.9459
230	16.62	49.52	0.294	14.56	0.9431
240	16.39	49.53	0.290	14.36	0.9401
250	16.12	49.33	0.286	14.11	0.9362
265	15.71	49.17	0.279	13.72	0.9279



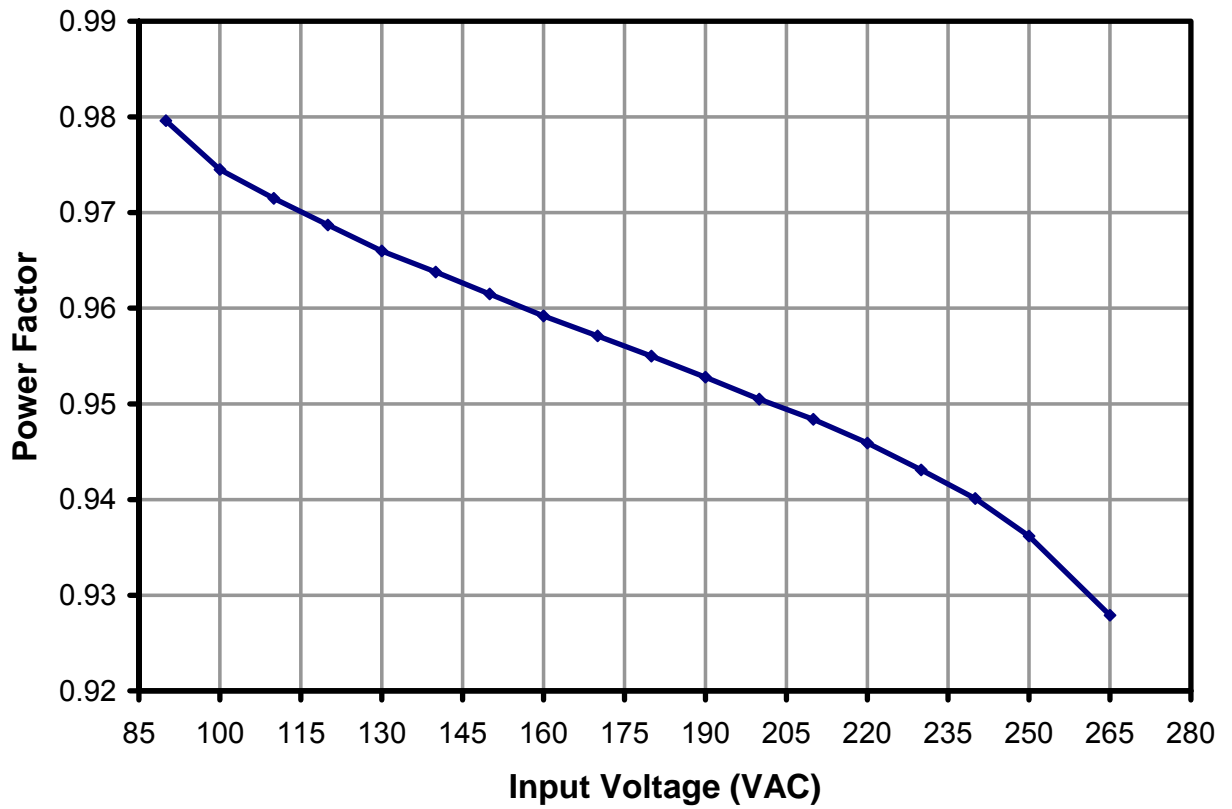


Figure 11 – Power Factor vs. Input Voltage, Room Temperature, Full Load.



### 10 Thermal Performance

Images captured after running for 30 minutes at room temperature (25 °C), full load (50 V, 0.3 A). This indicates a LinkSwitch-PH (U1) operating temperature of ~80°C at an external board ambient of 40°C. As U1 is the highest temperature component on the board it provides effective thermal protection for the entire system via its internal thermal shutdown. Since there are no components on the bottom side, all the data below are for the top side.

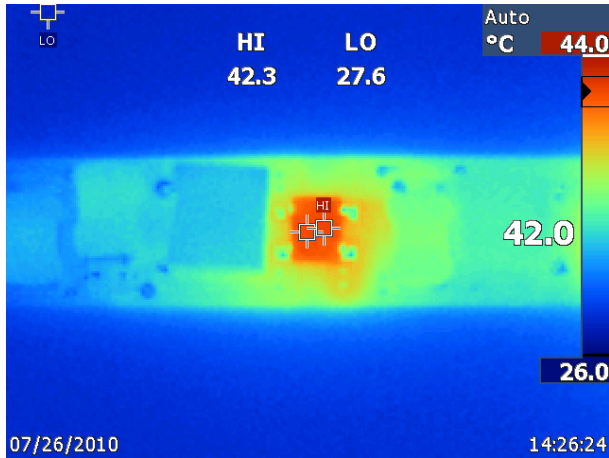


Figure 12 – 115 VAC EMI and Rectifier.

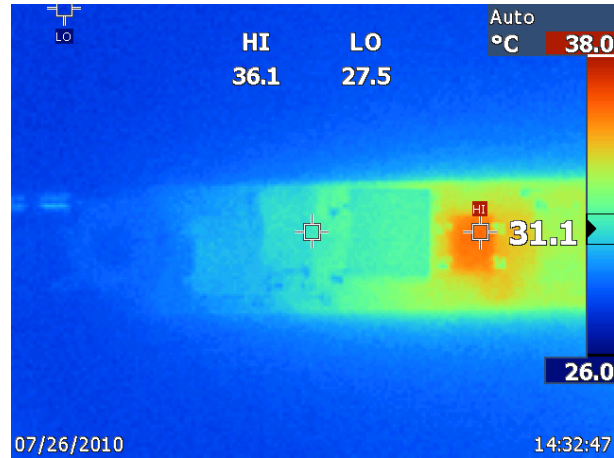


Figure 13 – 230 VAC EMI and Rectifier.

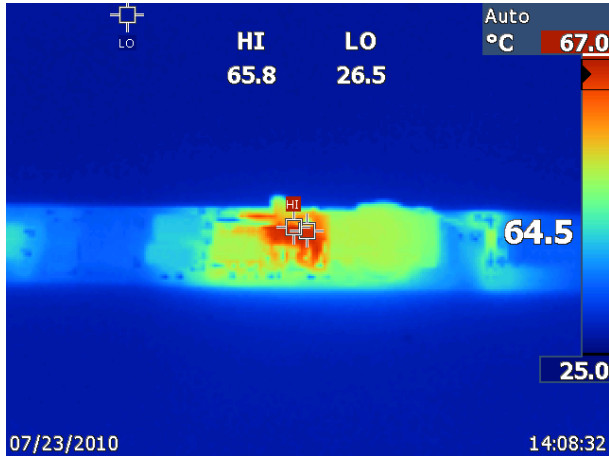


Figure 14 – 115 VAC Main Switching and Transformer.

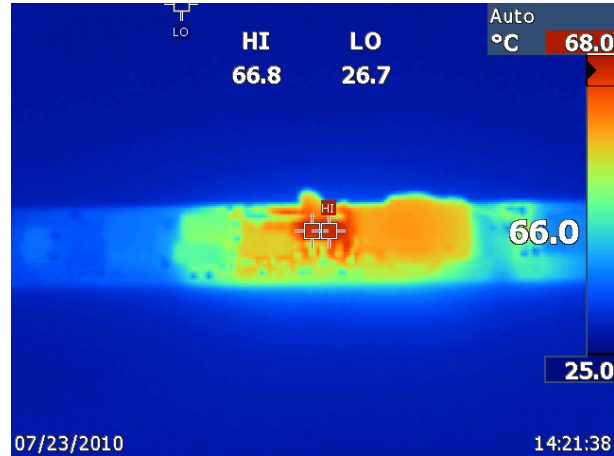


Figure 15 – 230 VAC Main Switching and Transformer.



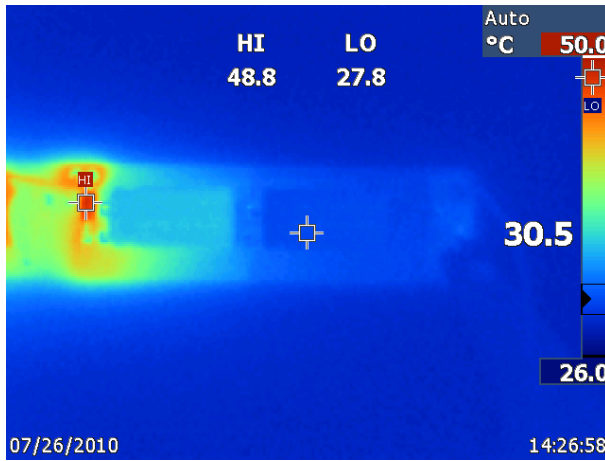


Figure 16 – 115 VAC Output Rectifier.

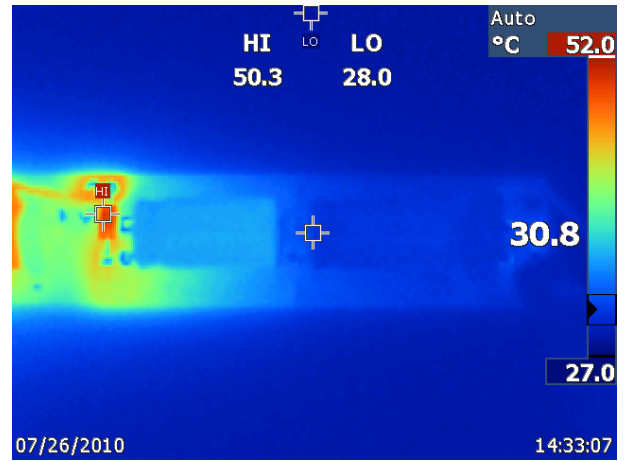


Figure 17 – 230 VAC Output Rectifier.



### 11 Harmonic Data

The design passes IEC61000-3-2 Class C requirement.

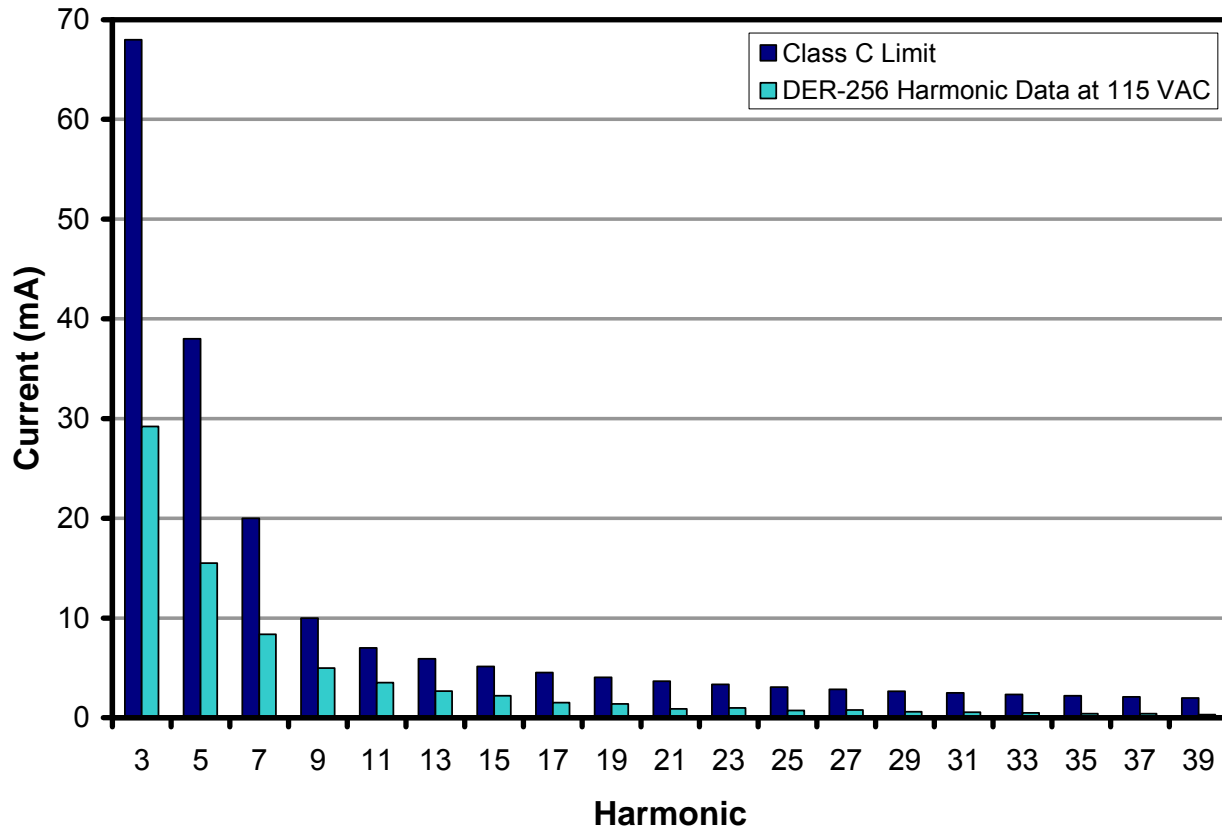


Figure 18 – 115 VAC Harmonic, Room Temperature, Full Load.



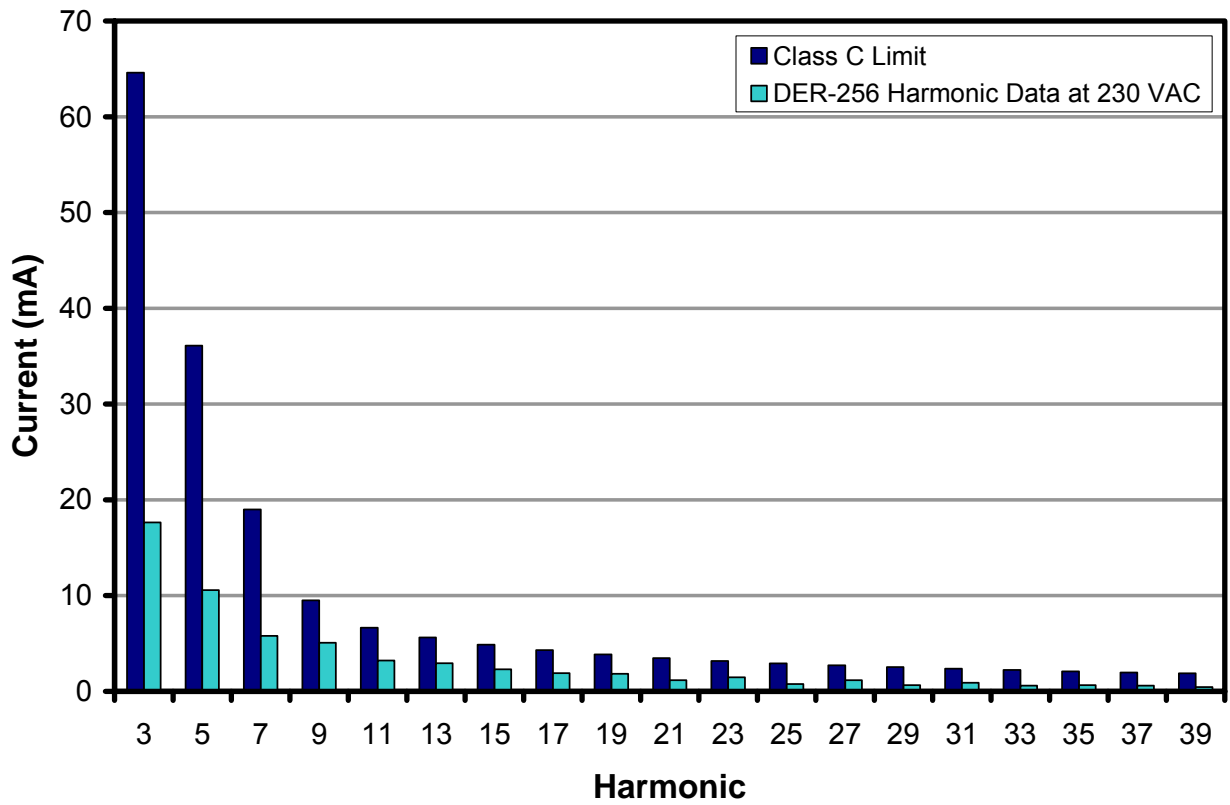
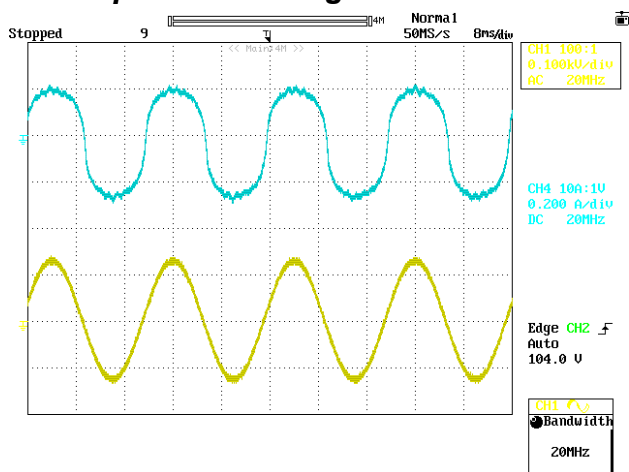


Figure 19 – 230 VAC Harmonic, Room Temperature, Full Load.

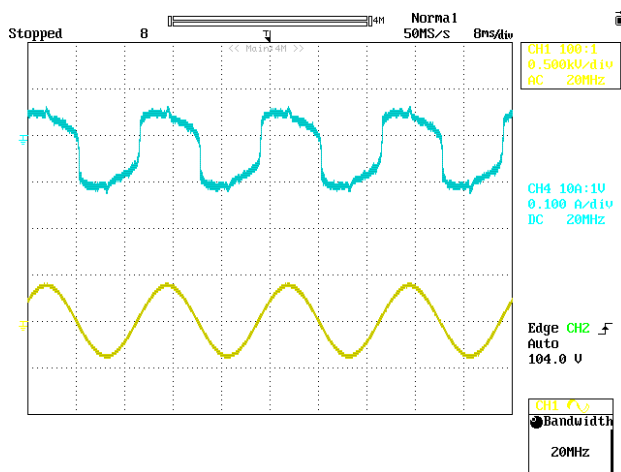


## 12 Waveforms

### 12.1 Input Line Voltage and Current

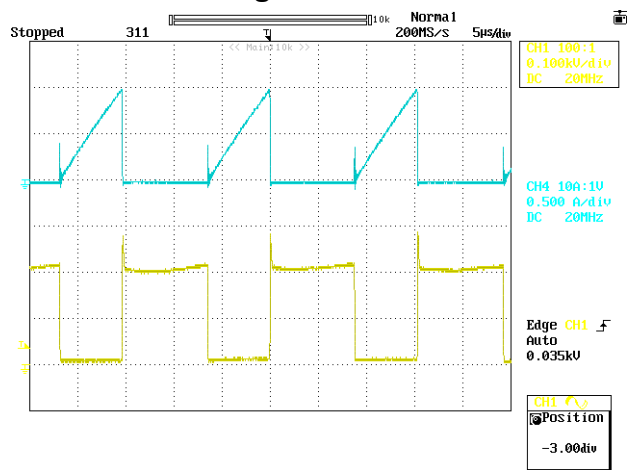


**Figure 20** – 90 VAC, Full Load.  
Upper:  $I_{IN}$ , 0.2 A / div.  
Lower:  $V_{IN}$ , 100 V, 8 ms / div.

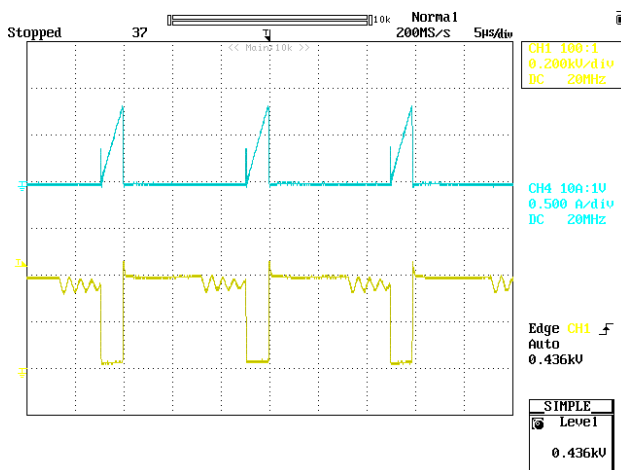


**Figure 21** – 265 VAC, Full Load.  
Upper:  $I_{IN}$ , 0.1 A / div.  
Lower:  $V_{IN}$ , 500 V / div., 8 ms / div.

### 12.2 Drain Voltage and Current

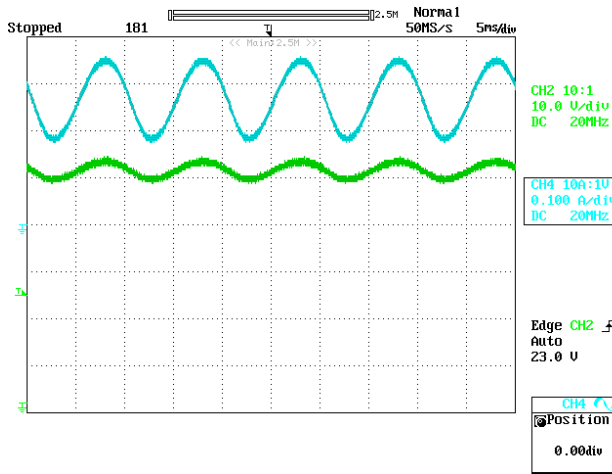


**Figure 22** – 90 VAC, Full Load.  
Upper:  $I_{DRAIN}$ , 0.5 A / div.  
Lower:  $V_{DRAIN}$ , 100 V, 5  $\mu$ s / div.

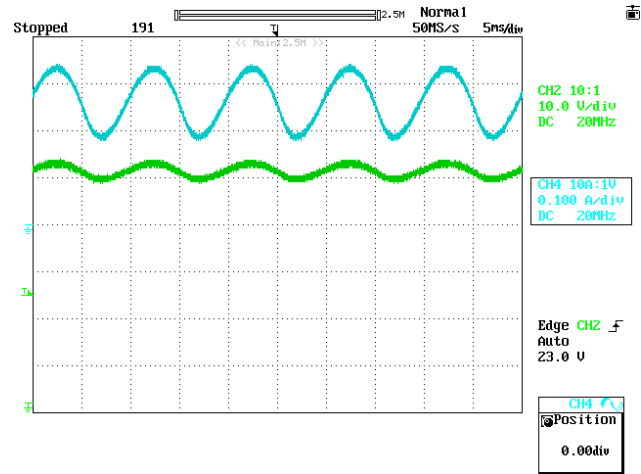


**Figure 23** – 265 VAC, Full Load.  
Upper:  $I_{DRAIN}$ , 0.5 A / div.  
Lower:  $V_{DRAIN}$ , 200 V / div., 5  $\mu$ s / div.

### 12.3 Output Voltage and Ripple Current

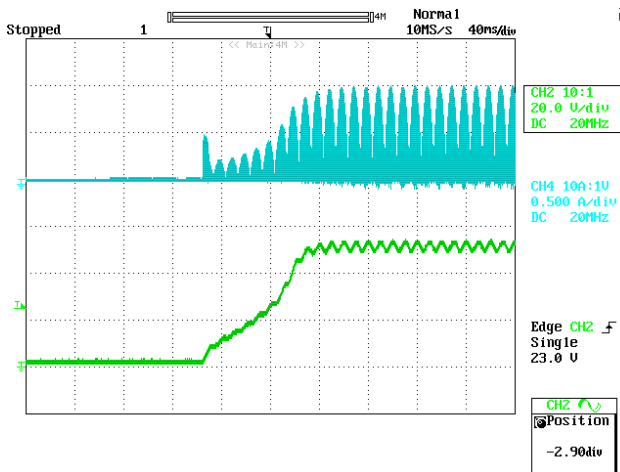


**Figure 24** – 90 VAC, Full Load.  
 Upper:  $I_{RIPPLE}$ , 0.1 A / div.  
 Lower:  $V_{OUTPUT}$  10 V, 5 ms / div.

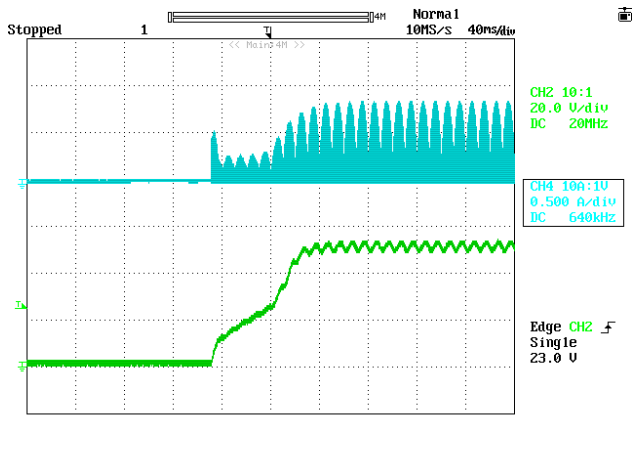


**Figure 25** – 265 VAC, Full Load.  
 Upper:  $I_{RIPPLE}$ , 0.1 A / div.  
 Lower:  $V_{OUTPUT}$  10 V, 5 ms / div.

### 12.4 Drain Voltage and Current Start-up Profile



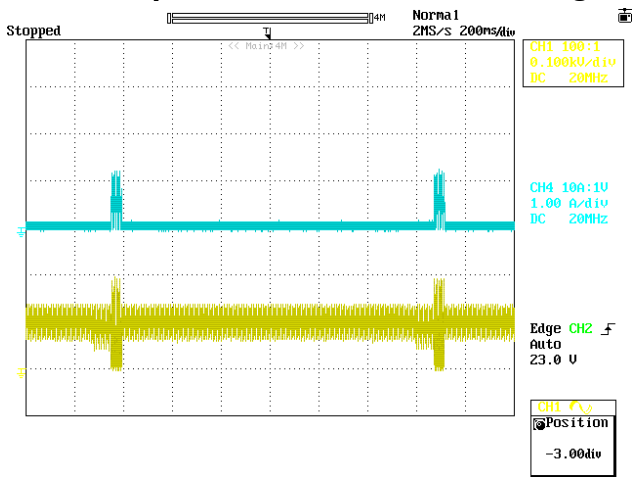
**Figure 26** – 90 VAC, Full Load.  
 Upper:  $I_{DRAIN}$ , 0.5 A / div.  
 Lower:  $V_{OUTPUT}$ , 20 V, 40 ms / div.



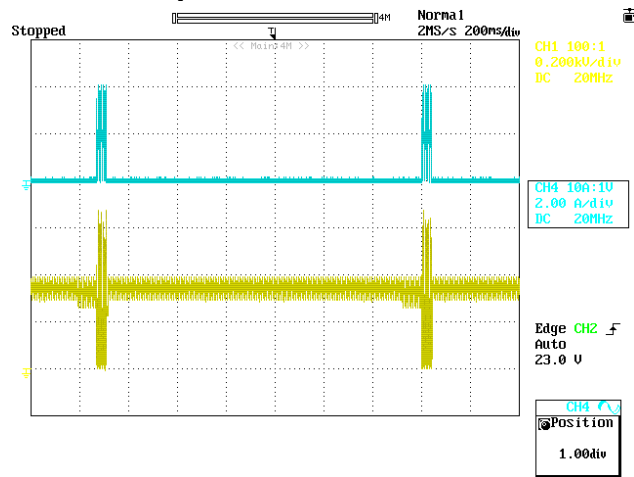
**Figure 27** – 265 VAC, Full Load.  
 Upper:  $I_{RIPPLE}$ , 0.5 A / div.  
 Lower:  $V_{OUTPUT}$ , 20 V, 40 ms / div.



### 12.5 Output Current and Drain Voltage at Shorted Output

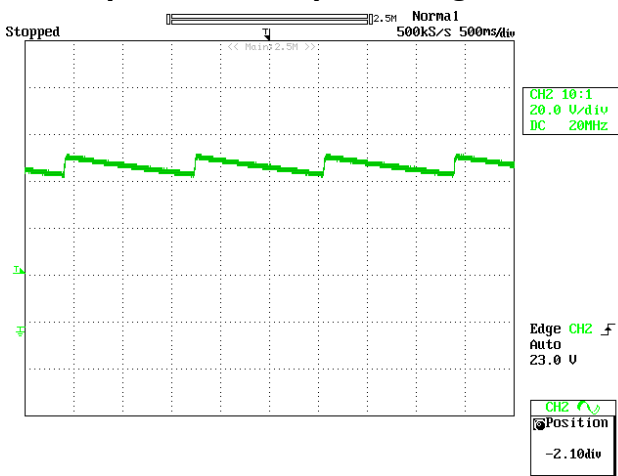


**Figure 28** – 90 VAC, Full Load.  
Upper:  $I_{OUTPUT}$ , 1 A / div.  
Lower:  $V_{DRAIN}$ , 100 V, 200 ms / div.

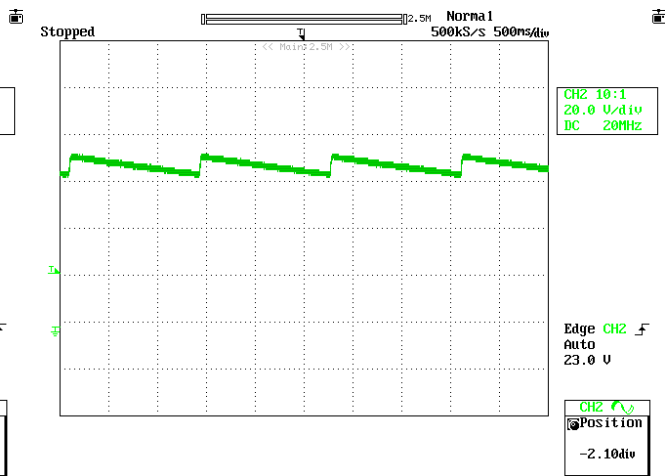


**Figure 29** – 265 VAC, Full Load.  
Upper:  $I_{OUTPUT}$ , 2 A / div.  
Lower:  $V_{DRAIN}$ , 200 V, 200 ms / div.

### 12.6 Open Load Output Voltage



**Figure 30** – Output Voltage: 115 VAC.  
 $V_{OUT}$ , 20 V / div., 500 ms / div.



**Figure 31** – Output Voltage: 230 VAC.  
 $V_{OUT}$ , 20 V / div., 500 ms / div.



### 13 Conducted EMI

The measurement was taken with the supply operating at full load with the board placed 10 mm away and oriented at 90 degrees to a metal plate connected to AC ground.

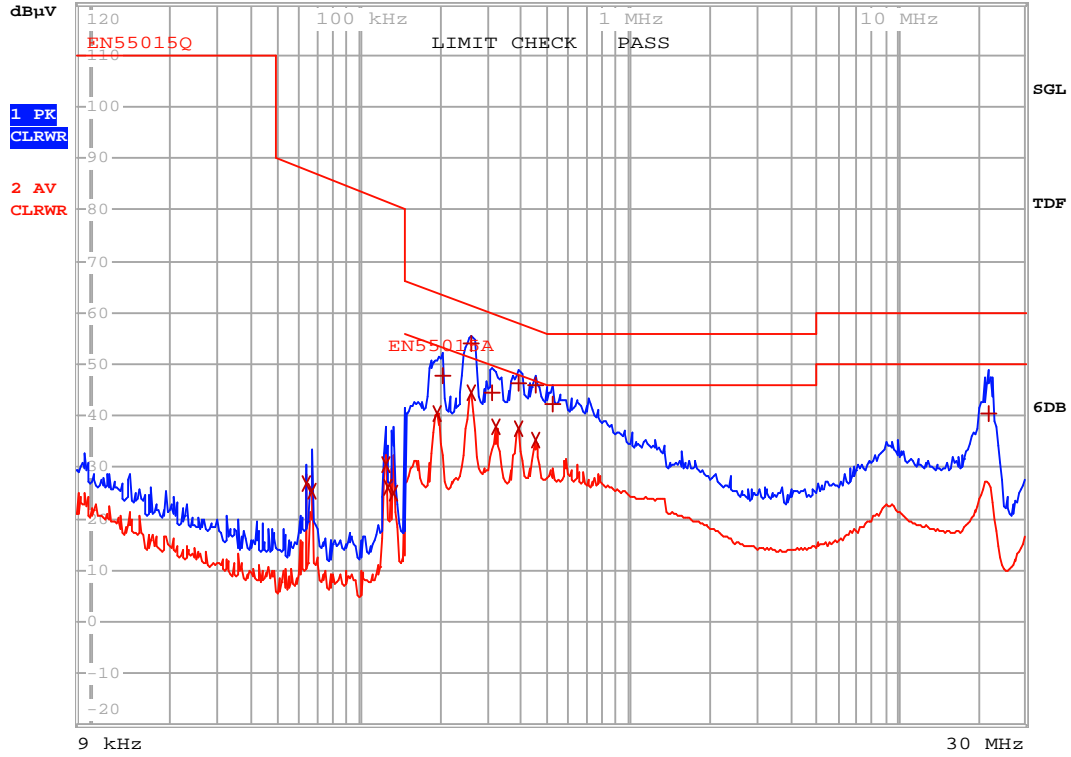


Figure 32 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz



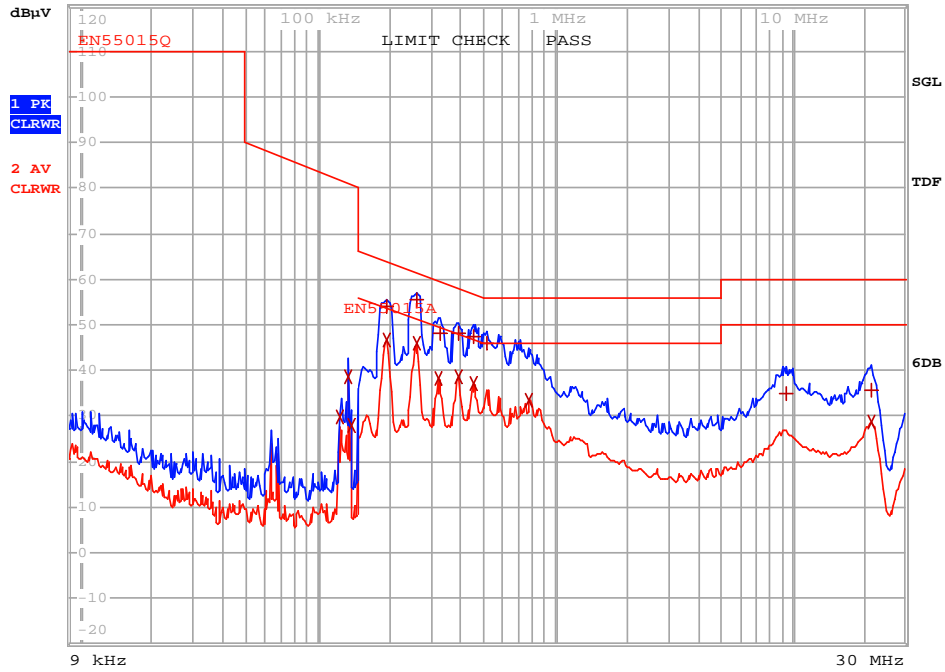


Figure 33 – Conducted EMI, Maximum Steady State Load, 230 VAC, 50 Hz.





### 14 Radiated EMI

Note: Refer to table for margin to standard – red line is peak measurement but limit line is quasi peak. RFI test data is for whole system, the demo board is assembly into T8 LED with aluminum shell, maximum steady state load.

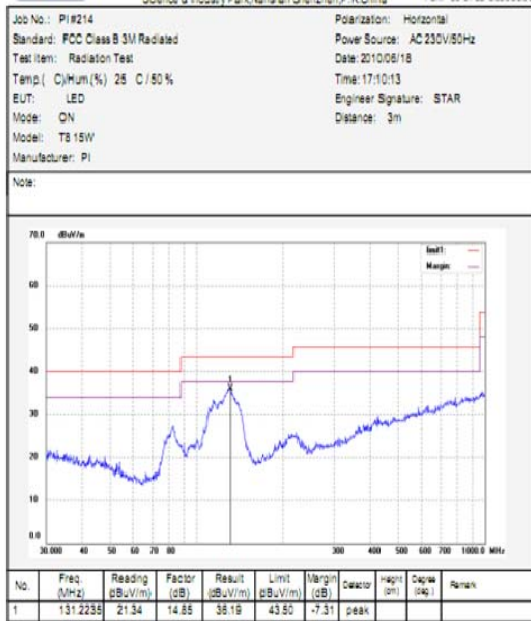


Figure 34 – 115 V / 60 Hz, Horizontal.

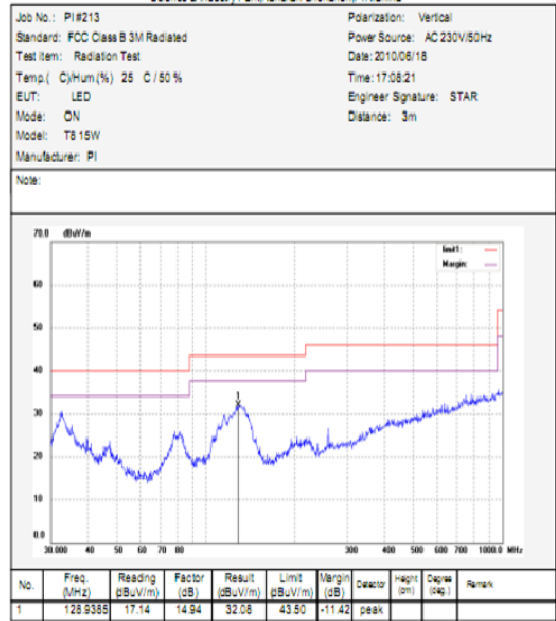


Figure 35 – 115 V / 60 Hz, Vertical.

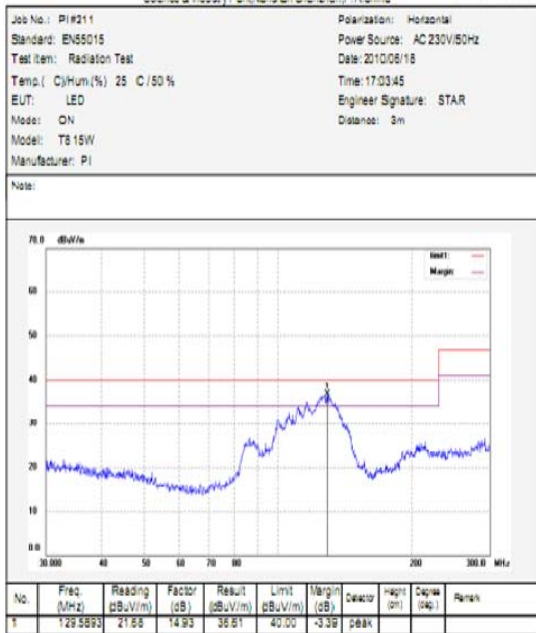


Figure 36 – 230 V / 50 Hz, Horizontal.

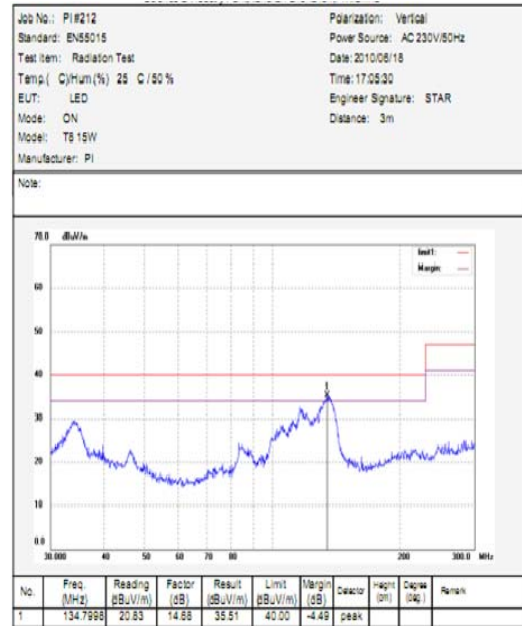


Figure 37 – 230 V / 50 Hz, Vertical.



## 15 Revision History

Date	Author	Revision	Description & changes	Reviewed
07-Oct-10	KM	1.2	Initial Release	Apps & Mktg



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