9.3 Regulation

9.3.1 Load

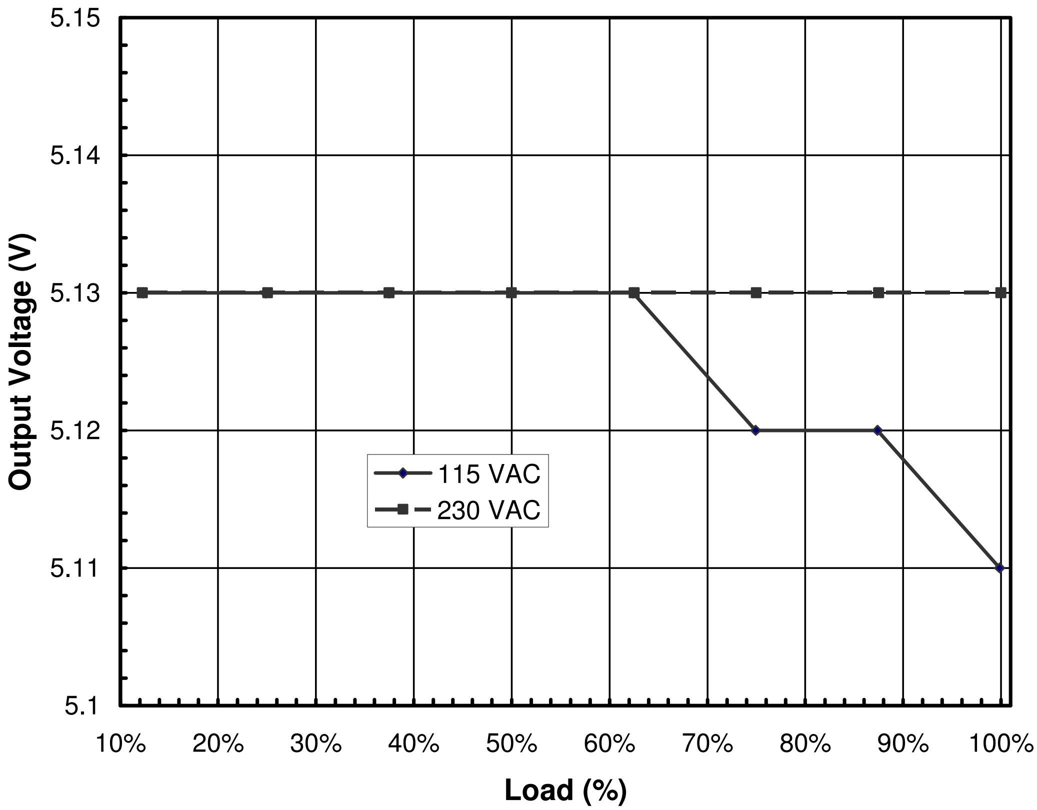

Figure 8 – Load Regulation, Room Temperature.

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9.3.2 Line

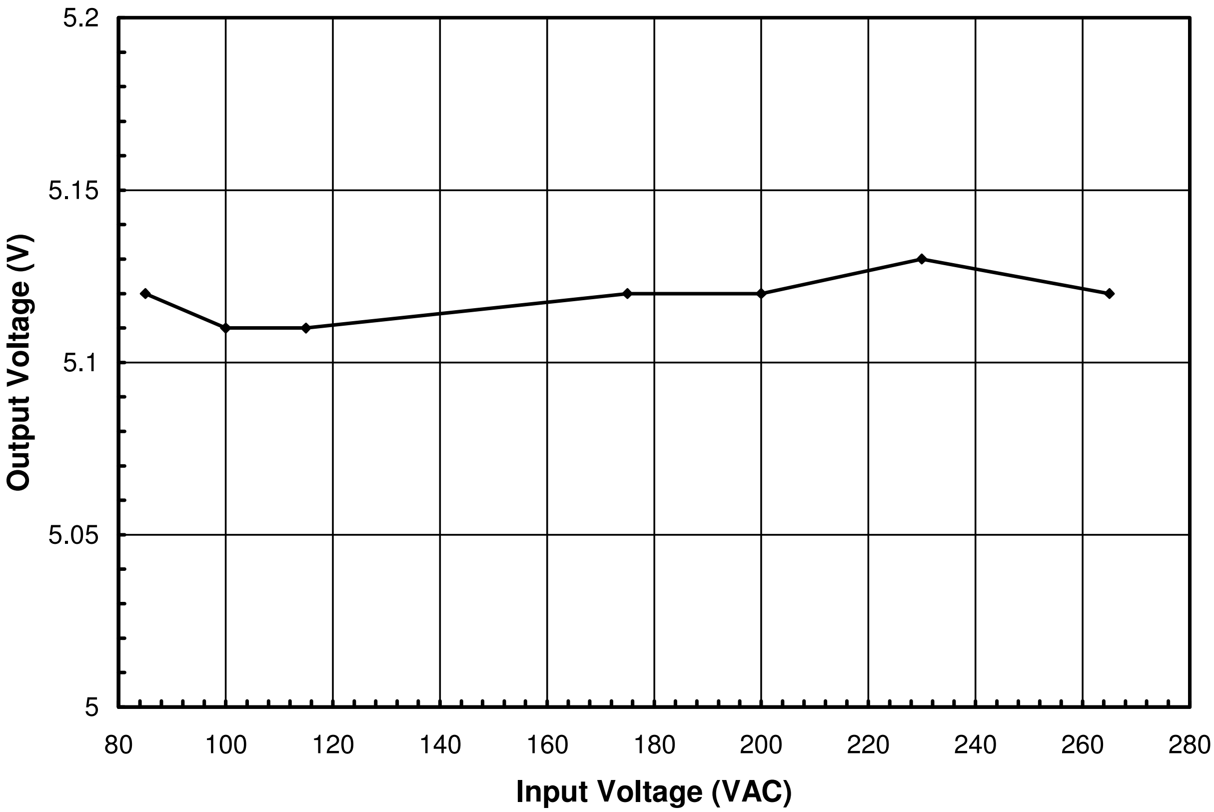

Figure 9 – Line Regulation, Room Temperature, Full Load.

10 Thermal Performance

The temperature of key components (three in this case) was recorded to ensure satisfactory thermal performance. Two of the thermocouples were soldered into place; one was soldered to U1 at its source (for measuring its source temperature) and the other was soldered to output diode D5. The third thermocouple, monitoring the transformer core temperature, was taped in place.

The supply was operated at full load using an external electronic load. The supply was placed in a small enclosure to prevent air circulation (within the chamber) from affecting the test. The ambient temperature within the enclosure was monitored via another, free-hanging, thermocouple.

Item	Temperature (°C)
	85 VAC
Ambient	30
Device Source (U1)	41
Output Diode (D5)	39
Transformer Core (T1)	38

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

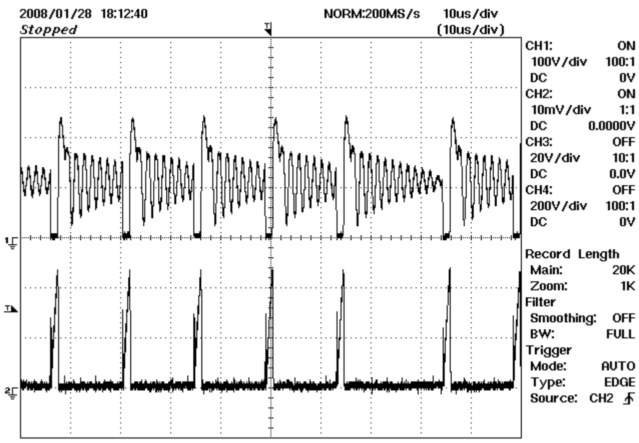

Figure 10 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA / div.
Timebase: 10 µs / div.

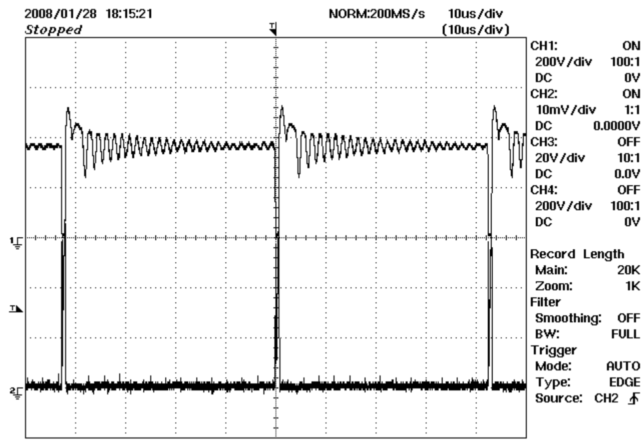

Figure 11 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 100 mA / div.
Timebase: 10 µs / div.

11.2 Output Voltage Start-up Profile

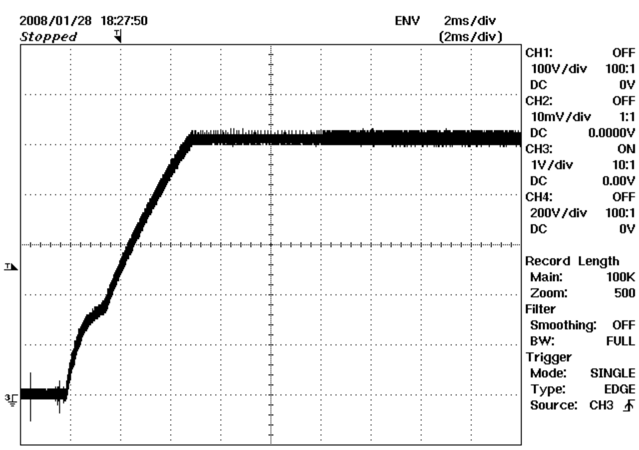

Figure 12 – Start-up Profile, 85 VAC.
1 V / div, 2 ms / div.

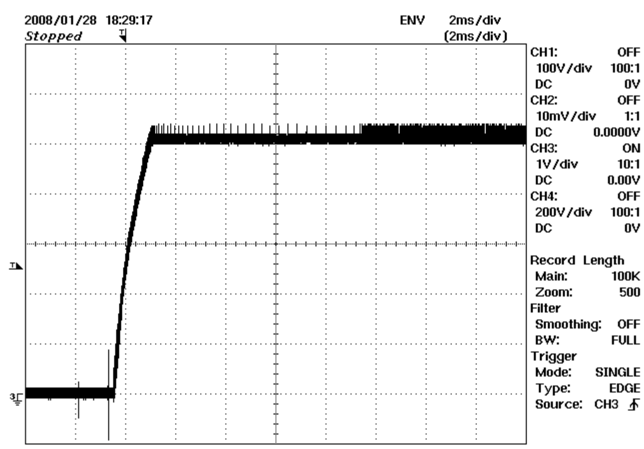

Figure 13 – Start-up Profile, 265 VAC.
1 V, 2 ms / div.

11.3 Drain Voltage and Current Start-up Profile

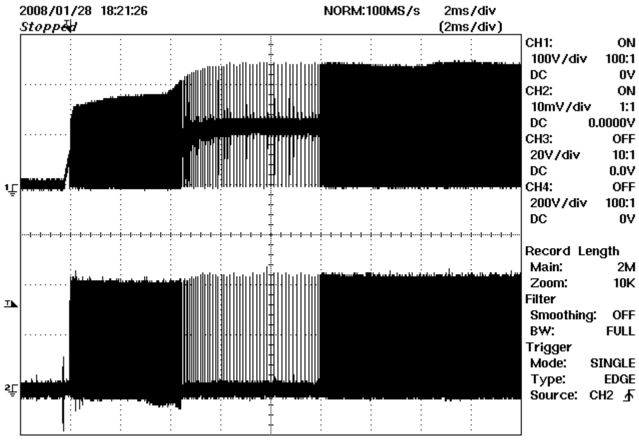

Figure 14 – 85 VAC Input and Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 100 mA / div.
Timebase: 2 ms / div.

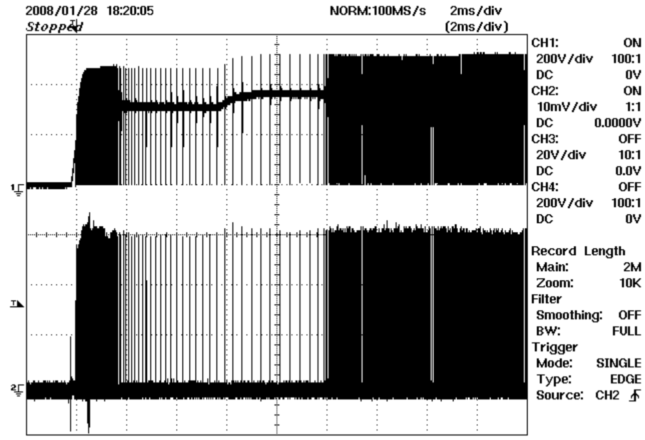

Figure 15 – 265 VAC Input and Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 100 mA / div.
Timebase: 2 ms / div.

11.4 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load's current step as a trigger source. Since the output switching and line frequency changes occur essentially at random with respect to load transients, contributions to the output ripple from these sources average out, leaving the contribution only from the load step response.

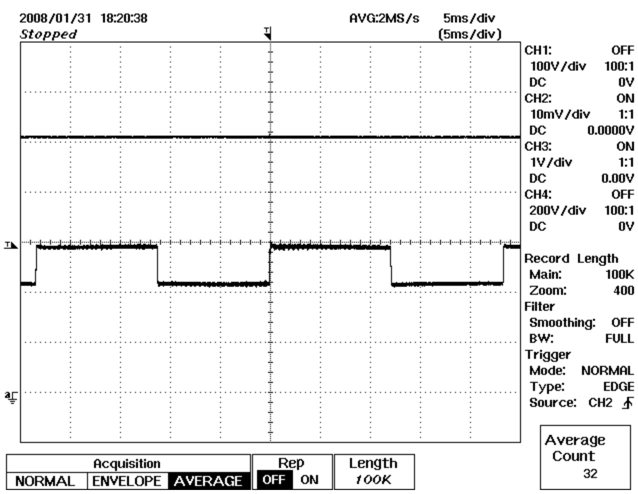

Figure 16 – Transient Response, 85 VAC.
75-100-75% Load Step.
Top: Output Voltage, 1 V / div.
Bottom: Output Current, 100 mA / div.
Timebase: 5 ms / div.

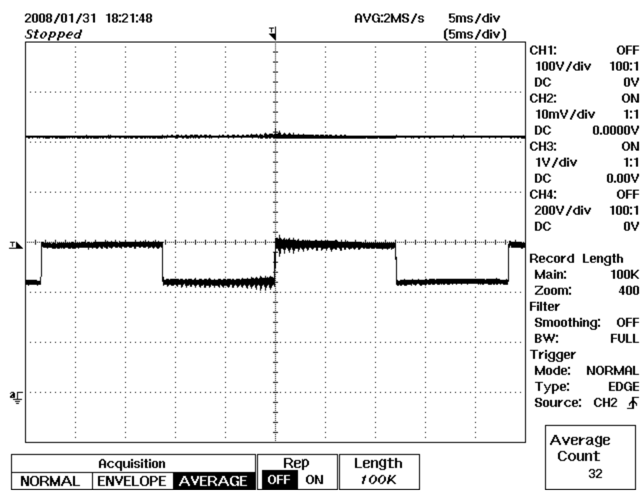

Figure 17 – Transient Response, 265 VAC.
75-100-75% Load Step.
Top: Output Voltage, 1 V / div.
Bottom: Output Current, 100 mA / div.
Timebase: 5 ms / div.

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11.5 External Magnetic Field Influence

The transformer core was subjected to a strong magnetic field by placing a strong magnet dipole on the core halves. As can be seen in Figure 18, no saturation was observed.

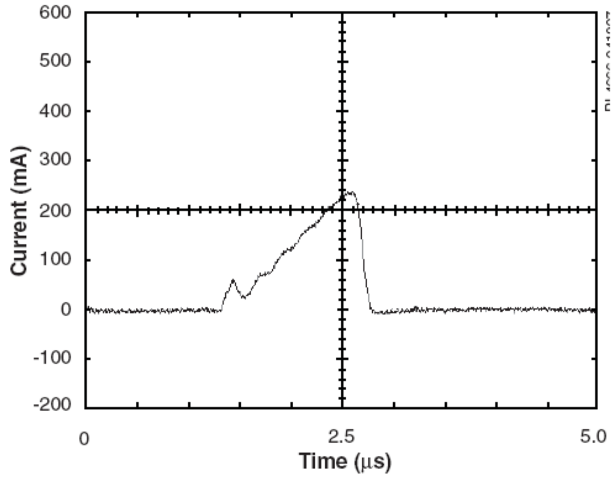

Figure 18 – Drain Current Under Influence of a Magnetic Dipole Indicating no Core Saturation
100 mA / div.

11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. The capacitors include a 0.1 µF / 50 V ceramic type and 1.0 µF / 50 V aluminum electrolytic. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs. (Refer to Figure 19 and Figure 20).

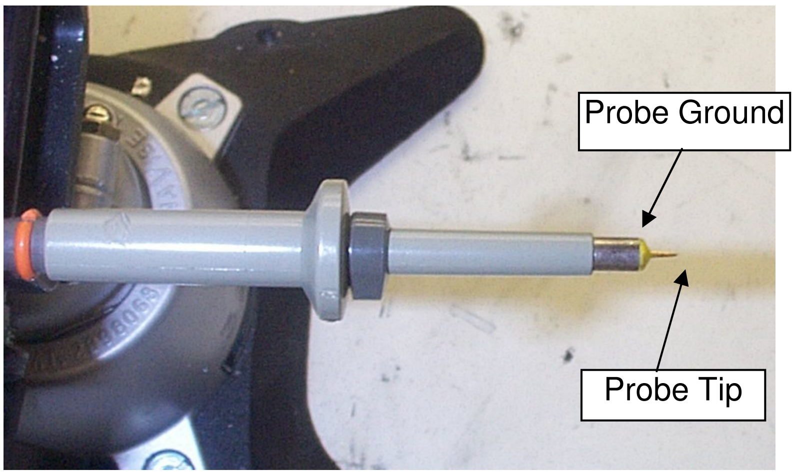

Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

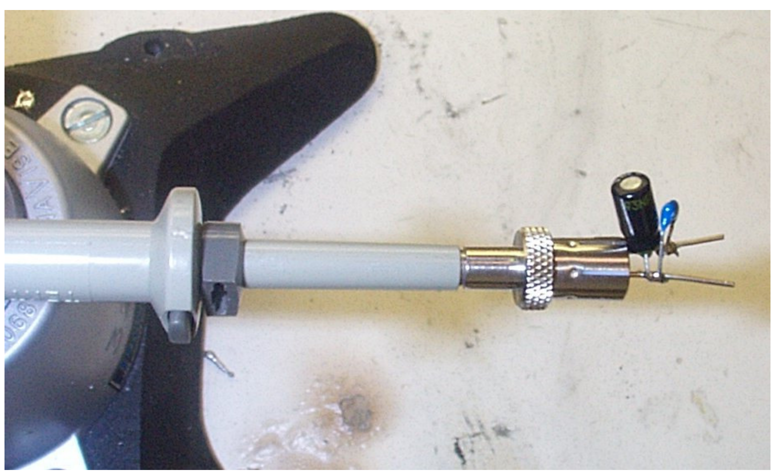

Figure 20 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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11.6.2 Measurement Results

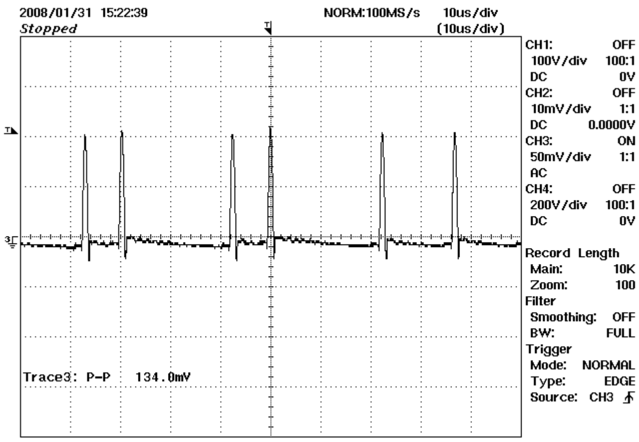

Figure 21 – Ripple, 85 VAC, Full Load.
10 µs / div, 50 mV / div.

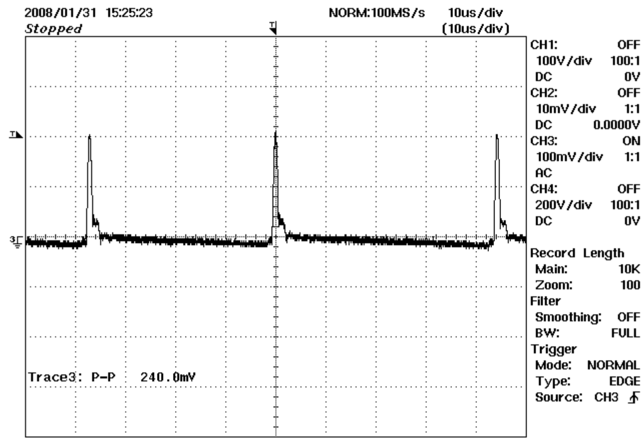

Figure 22 – Ripple, 265 VAC, Full Load.
10 µs / div, 100 mV / div.

12 Conducted EMI

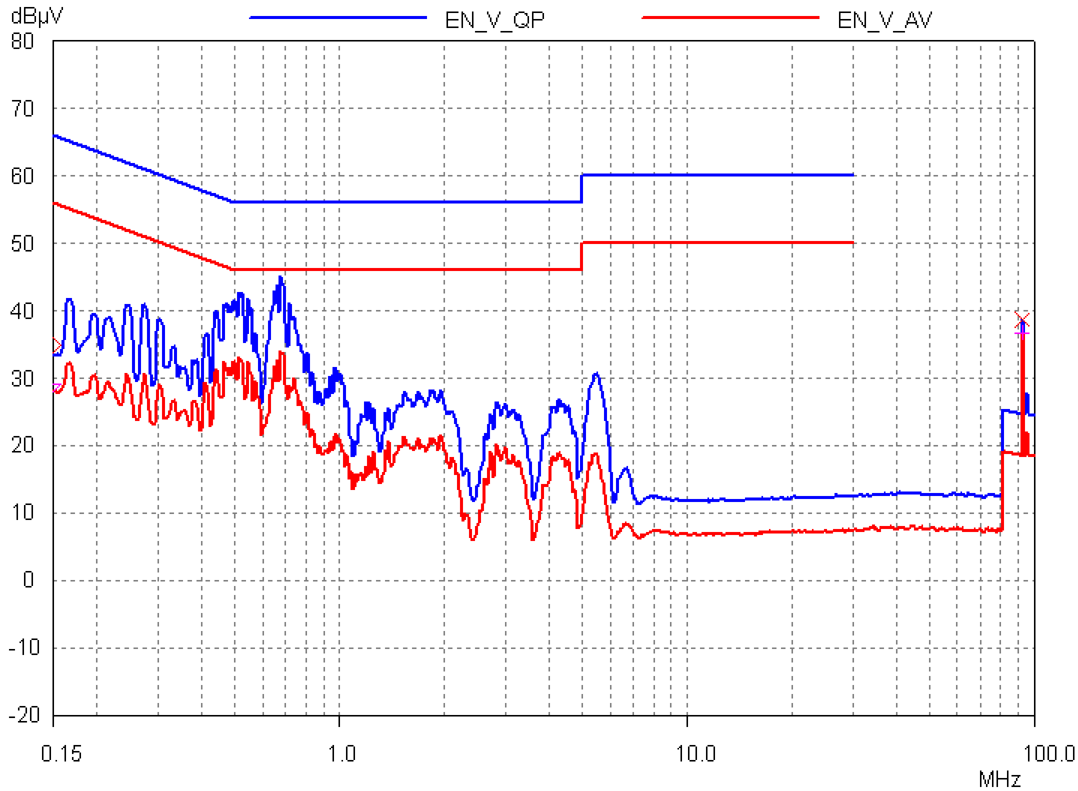

Figure 23 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55022 B Limits.

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
17-Apr-08	JD	1.0	Final Release	SGK

Notes

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