# Reference Design Report for a 2.5 W Universal Input, Non-Isolated Buck Converter with Zero Crossing Detection Using LinkSwitch™-TNZ LNK3307D

<table>
<thead>
<tr>
<th>Title</th>
<th>Reference Design Report for a 2.5 W Universal Input, Non-Isolated Buck Converter with Zero Crossing Detection Using LinkSwitch™-TNZ LNK3307D</th>
</tr>
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<tbody>
<tr>
<td>Specification</td>
<td>90 VAC – 300 VAC Input; 5 V / 500 mA Output</td>
</tr>
<tr>
<td>Application</td>
<td>Home Building Automation &amp; IoT</td>
</tr>
<tr>
<td>Author</td>
<td>Applications Engineering Department</td>
</tr>
<tr>
<td>Document Number</td>
<td>RDR-866</td>
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<td>Date</td>
<td>June 3, 2021</td>
</tr>
<tr>
<td>Revision</td>
<td>1.0</td>
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## Summary and Features
- 5 V / 500 mA output for wireless (WiFi, NB IoT etc.) and relay power
- Low cost and component count buck converter using off-the-shelf inductor
- Compact solution 1.25" x 1.25" x 0.6"
- AC zero crossing signal output
- Optimized for <10 dB audible noise performance
- No-load input power <50 mW
- Excellent output voltage line regulation (<2% 5 V TYP)
- Reduced dissipation during output short-circuit fault
- Low output voltage ripple <100 mV PK-PK
- >6 dB conducted EMI margin

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**PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at [https://www.power.com/company/intellectual-property-licensing/](https://www.power.com/company/intellectual-property-licensing/).
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.
1 Introduction

This engineering report describes a non-isolated buck converter power supply with an input line Zero Crossing Detection (ZCD) output signal. The nominal output is 5 V, 500 mA across the input range of 90-300 VAC. The PSU is powered by the LinkSwitch-TNZ IC controller.

The LinkSwitch-TNZ family of ICs combine power conversion with lossless generation of AC zero crossing signal used typically for system clock and timing functions. The device incorporates a 725 V power MOSFET, oscillator, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and input overvoltage protection circuitry onto a monolithic IC. Designs using the highly integrated LinkSwitch-TNZ ICs are more flexible than discrete implementations reducing component count by 40% or higher.

The key design goal is low cost, low audible noise and compact form factor intended for wireless (WiFi, NBioT etc.) and relay power.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, performance and test data.
Figure 1 – Populated Circuit Board, Top View.

Figure 2 – Populated Circuit Board, Bottom View.
## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Comment</th>
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<tbody>
<tr>
<td>Input Voltage</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>90</td>
<td></td>
<td>300</td>
<td>VAC</td>
<td>2 Wire – no P.E.</td>
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<tr>
<td>Frequency</td>
<td>f&lt;sub&gt;LINE&lt;/sub&gt;</td>
<td>47</td>
<td>50/60</td>
<td>63</td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>No-load Input Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Current</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>500</td>
<td></td>
<td>100</td>
<td>mA</td>
<td>Full Load Condition.</td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>V&lt;sub&gt;RIPPLE&lt;/sub&gt;</td>
<td>2.5</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Rated Output Power</td>
<td>P&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>2.5</td>
<td></td>
<td></td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>η</td>
<td>65%</td>
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<td>Full Load.</td>
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<td>Environmental</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Conducted EMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CISPR22B / EN55022B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6 dB Margin Using Resistive</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Load Floating</td>
</tr>
<tr>
<td>Line Surge</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>kV</td>
<td>Combination Wave: 2 Ω.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>kV</td>
<td>Ring Wave: 12 Ω.</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>T&lt;sub&gt;AMB&lt;/sub&gt;</td>
<td>0</td>
<td></td>
<td>40</td>
<td>°C</td>
<td>Free Convection, Sea Level.</td>
</tr>
</tbody>
</table>
3 Schematic

Figure 3 – Schematic.
4 Circuit Description

4.1 Input Stage
Fuse F1 provides safety protection in case of component failure in the power supply circuitry. Varistor RV1 limits the voltage to protect the circuitry during line transient voltage surge events. The bridge rectifier diode BR1 converts AC input to DC voltage by full wave rectification. Bulk capacitors C1, C2 and differential inductor L1 form a Pi filter to minimize bulk ripple voltage and provide differential mode EMI noise filtering.

To improve conducted EMI, power inductor L2 must be placed away from the input side to reduce switching noise coupling. The ZCD line sense resistor R1 and R2 are very high impedance components connected directly to the input side. These resistors must be placed away from the IC or close to the input side to prevent coupling of switching noise.

4.2 LinkSwitch-TNZ Circuit Operation
The power supply circuit is a high-side buck converter topology where the power MOSFET inside U1 (LinkSwitch-TNZ) is connected at the positive bulk rail. The main buck converter circuitry comprises of U1, freewheeling diode D2, buck inductor L2 and output capacitor C7. When the MOSFET internal to LinkSwitch-TNZ U1 turns on, the current through the inductor L2 starts to ramp up producing an opposing voltage across its terminal. With respect to the input voltage, the opposing voltage across inductor L2 reduces the output voltage that is delivered to the load. At this point, the freewheeling diode D2 is reverse bias. When U1 MOSFET turns off, the voltage across inductor L2 commutates forward biasing the freewheeling diode D2. The current through inductor L2 starts to ramp down supporting the current flow to the load.

Capacitor C3 with a value of 100 nF sets the current limit to Standard mode. At power-up, the IC is initially powered from the DRAIN (D) pin. The 5V regulator internal to the IC, charges the BYPASS (BP) pin capacitor C3 to power the IC. When the MOSFET turns on, the external bias resistor R3 charges the BP pin capacitor C3 easing up the powering of LinkSwitch-TNZ. The bias voltage must be higher than the BP pin voltage to effectively help power the LinkSwitch-TNZ. For a 5 V output application, adding resistor R6 in series with bias capacitor C5 increases the output voltage at no-load, lowering the no-load input power. Bias resistor R3 must be optimized with respect to the bias voltage to deliver the best efficiency and minimal no-load input power. To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than IS1. For the best full-load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than the IS2 Max value.

During normal operation, the switching of the power MOSFET is controlled by the FEEDBACK pin through LinkSwitch-TNZ On/Off control engine. MOSFET switching is terminated when a current greater than IFB (49 μA) is delivered into this pin. The feedback voltage is sampled by resistors R4 and R5 across the bias supply voltage, which
track the output voltage. R6 is added in series with C5 to reduce ripple voltage and audible noise.

Pre-load resistor R10 limits the output voltage during a no-load condition.

### 4.3 Zero Crossing Detection Circuit

The LinkSwitch-TNZ IC integrates a low power consumption Zero Cross Detection circuit with Z1 and Z2 as Zero-Detect pins. Z2 is connected to one of the input AC lines through sense resistors R1 and R2, while Z1 forms the ZCD signal output. The Zero Cross Detection circuit internal to the IC senses the high-voltage AC input via R1 and R2 and drives the external ZCD signal generator circuit. For conducted EMI consideration, R1 and R2 which are high-impedance components must be connected near the input line terminal or away from the IC to minimize noise coupling.

During the input AC positive half-cycle with respect to NEUTRAL, Z1 and Z2 allow current flow to drive MOSFET Q1 at the on-state, pulling down the ZCD voltage to GND. During the negative half-cycle of the input AC, Z1 and Z2 block the current flow turning off Q1. At this point, resistor R8 pulls up the ZCD voltage equal to the output voltage. Zener diode VR1 protects Q1 from high voltage stress. Resistor R9 discharges residual gate voltage stored from Q1 parasitic capacitances and C6 to turn off the MOSFET Q1 completely.

Passive components C3, C6 and R7 provide noise filtering to deliver a clean ZCD signal. These capacitors are sized for minimal effect to the delay of the ZCD signal.
5 PCB Layout

Material: FR4
Copper: 2 oz

Figure 4 – Top Side.

Figure 5 – Bottom Side.
6  Bill of Materials

6.1  Electrical Parts

<table>
<thead>
<tr>
<th>Item</th>
<th>Ref Des</th>
<th>Qty</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Manufacturer</th>
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<tr>
<td>1</td>
<td>BR1</td>
<td>1</td>
<td>1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC</td>
<td>B10S-G</td>
<td>Comchip</td>
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<tr>
<td>2</td>
<td>C1</td>
<td>1</td>
<td>2.2 µF, 450 V, Electrolytic, (8 x 11.5)</td>
<td>UVK2W2WE2MD1T</td>
<td>Nichicon</td>
</tr>
<tr>
<td>3</td>
<td>C6</td>
<td>1</td>
<td>100 µF, 100 V, Ceramic, COG, 0805</td>
<td>C0805C01J1GACTU</td>
<td>Kemet</td>
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<tr>
<td>4</td>
<td>C4</td>
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<td>100 nF, 25 V, Ceramic, X7R, 0805</td>
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<td>AVX</td>
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<tr>
<td>5</td>
<td>C5</td>
<td>1</td>
<td>10 µF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805</td>
<td>CL21B106KOQNNNE</td>
<td>Samsung</td>
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<tr>
<td>6</td>
<td>C7</td>
<td>1</td>
<td>220 µF, ±20%, 16 V, Electrolytic, Gen. Purpose, 2000 Hrs @ 105°C, (6.3 x 9)</td>
<td>A750EK227M1CAAE016</td>
<td>Nichicon</td>
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<tr>
<td>7</td>
<td>D1</td>
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<td>600 V, 1 A, Rectifier, Glass Passivated, POWERDI123</td>
<td>DFLR1600-7</td>
<td>Diodes Inc</td>
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<td>8</td>
<td>D2</td>
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<td>600 V, 2 A, Superfast, 35 ns, DO-214AC, SMA</td>
<td>ES2J-LTP</td>
<td>Micro Commercial</td>
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<tr>
<td>9</td>
<td>F1</td>
<td>1</td>
<td>1 A, 250 V, Slow, Long Time Lag, RST 1</td>
<td>RST 1</td>
<td>Belfuse</td>
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<tr>
<td>10</td>
<td>L1</td>
<td>1</td>
<td>680 µH, 0.25 A, 5.5 x 10.5 mm</td>
<td>SBCI-681-251</td>
<td>Tokin</td>
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<tr>
<td>11</td>
<td>L2</td>
<td>1</td>
<td>680 µH, 0.8 A, 20%</td>
<td>RL-5480-4-680</td>
<td>Renco</td>
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<tr>
<td>12</td>
<td>Q1</td>
<td>1</td>
<td>60 V, 115 mA, SOT23-3</td>
<td>2N7002-7-F</td>
<td>Diodes Inc</td>
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<td>13</td>
<td>R1</td>
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<td>RES, 499 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6ENF4993V</td>
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<tr>
<td>14</td>
<td>R3</td>
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<td>RES, 4.32 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
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<td>Panasonic</td>
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<tr>
<td>15</td>
<td>R4</td>
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<td>RES, 24.3 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6ENF2432V</td>
<td>Panasonic</td>
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<td>16</td>
<td>R5</td>
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<td>RES, 20.0 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
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<td>R6</td>
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<td>RES, 30 kΩ, 5%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6GHEY300V</td>
<td>Panasonic</td>
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<td>18</td>
<td>R7</td>
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<td>Panasonic</td>
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<td>19</td>
<td>R10</td>
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<td>Panasonic</td>
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<tr>
<td>20</td>
<td>RV1</td>
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<td>300 VAC, 25 J, 7 mm, RADIAL</td>
<td>V300LA4P</td>
<td>Littlefuse</td>
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<tr>
<td>21</td>
<td>U1</td>
<td>1</td>
<td>LinkSwitch-TNZ, SO8</td>
<td>LNK3307D</td>
<td>Power Integrations</td>
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<td>22</td>
<td>VR1</td>
<td>1</td>
<td>DIODE, ZENER, 7.5 V, ±5%, 500 mW, SOD123</td>
<td>MMSZ4693T1G</td>
<td>ON Semi</td>
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6.2  Miscellaneous Part

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<tr>
<th>Item</th>
<th>Part Reference</th>
<th>QTY</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Manufacturer</th>
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<td>TP1 TP5 TP6</td>
<td>3</td>
<td>Test Point, BLK, Miniature THRU-HOLE MOUNT</td>
<td>Keystone</td>
<td>5001</td>
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<tr>
<td>2</td>
<td>TP2</td>
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<td>Test Point, WHT, Miniature THRU-HOLE MOUNT</td>
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<td>Test Point, BLUE, Miniature THRU-HOLE MOUNT</td>
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7 PI Expert Design Spreadsheet

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<th>INPUT</th>
<th>INFO</th>
<th>OUTPUT</th>
<th>UNIT</th>
<th>ACDC LinkSwitch-TNZ Buck</th>
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<td>ENTER APPLICATION VARIABLES</td>
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<tr>
<td>3</td>
<td>LINE VOLTAGE RANGE</td>
<td>Custom</td>
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<td>AC line voltage range</td>
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<td>VACMIN</td>
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<td>Minimum AC line voltage</td>
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<td>V</td>
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<td>5</td>
<td>VACMAX</td>
<td>305.00</td>
<td>Info</td>
<td>The maximum AC line voltage is too high</td>
<td>305.00</td>
<td>V</td>
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<tr>
<td>6</td>
<td>FL</td>
<td>60.00</td>
<td>Hz</td>
<td>AC mains frequency</td>
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<tr>
<td>7</td>
<td>LINE RECTIFICATION TYPE</td>
<td>F</td>
<td>F</td>
<td>Line rectification type: select &quot;F&quot; if full wave rectification or &quot;H&quot; if half wave rectification</td>
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<td>8</td>
<td>VOUT</td>
<td>5.00</td>
<td>5.00</td>
<td>V</td>
<td>Output voltage</td>
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<td>9</td>
<td>IOUT</td>
<td>0.500</td>
<td>0.500</td>
<td>A</td>
<td>Average output current</td>
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<tr>
<td>10</td>
<td>EFFICIENCY_ESTIMATED</td>
<td>0.80</td>
<td></td>
<td>Efficiency estimate at output terminals</td>
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<td>11</td>
<td>EFFICIENCY_CALCULATED</td>
<td>0.69</td>
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<td>Calculated efficiency based on real components and operating point</td>
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<td>12</td>
<td>POUT</td>
<td>2.50</td>
<td>W</td>
<td>Continuous output power</td>
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<td>13</td>
<td>CIN</td>
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<td>VMIN</td>
<td>87.7</td>
<td>V</td>
<td>Valley voltage of the rectified minimum AC line voltage</td>
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<td>VMAX</td>
<td>431.3</td>
<td>V</td>
<td>Peak voltage of the maximum AC line voltage</td>
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<td>16</td>
<td>INPUT STAGE RESISTANCE</td>
<td>0</td>
<td>0</td>
<td>Ohms</td>
<td>Input stage resistance in ohms (includes thermistor, filtering components, etc)</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>PLOSS_INPUTSTAGE</td>
<td>0.000</td>
<td>W</td>
<td>Maximum input stage loss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>ENTER LINKSWITCH-TNZ VARIABLES</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>22</td>
<td>OPERATION MODE</td>
<td>MCM</td>
<td></td>
<td>Mostly continuous mode of operation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>CURRENT LIMIT MODE</td>
<td>STD</td>
<td>STD</td>
<td>Choose 'RED' for reduced current limit or 'STD' for standard current limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>XCAP REQUIRED</td>
<td>NO</td>
<td>NO</td>
<td>Select whether an X-capacitor is required or not</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PACKAGE</td>
<td>SO-8C</td>
<td></td>
<td>Device package</td>
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<td></td>
</tr>
<tr>
<td>26</td>
<td>DEVICE SERIES</td>
<td>LNK3307</td>
<td>LNK3307</td>
<td>Generic LinkSwitch-TNZ device</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>DEVICE CODE</td>
<td>LNK3307D</td>
<td>LNK3307</td>
<td>Required LinkSwitch-TNZ device</td>
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<td></td>
</tr>
<tr>
<td>28</td>
<td>ILIMITMIN</td>
<td>0.725</td>
<td>A</td>
<td>Minimum current limit of the device</td>
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<td></td>
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<tr>
<td>29</td>
<td>ILIMITTYP</td>
<td>0.780</td>
<td>A</td>
<td>Typical current limit of the device</td>
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<td></td>
</tr>
<tr>
<td>30</td>
<td>ILIMITMAX</td>
<td>0.835</td>
<td>A</td>
<td>Maximum current limit of the device</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>RDSON</td>
<td>12.90</td>
<td>ohms</td>
<td>Primary switch on-time drain to source resistance at 100degC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>FSMIN</td>
<td>62000</td>
<td>Hz</td>
<td>Minimum switching frequency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>FSTYP</td>
<td>66000</td>
<td>Hz</td>
<td>Typical switching frequency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>FSMAX</td>
<td>70000</td>
<td>Hz</td>
<td>Maximum switching frequency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>BVDSS</td>
<td>725</td>
<td>V</td>
<td>Device breakdown voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>BUCK INDUCTOR PARAMETERS</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>INDUCTANCE_MIN</td>
<td>6120</td>
<td>uH</td>
<td>Minimum design inductance required for current delivery</td>
<td></td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>INDUCTANCE_TYP</td>
<td>6800</td>
<td>uH</td>
<td>Typical design inductance required for current delivery</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>INDUCTANCE_MAX</td>
<td>7480</td>
<td>uH</td>
<td>Maximum design inductance required for current delivery</td>
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<tr>
<td>56</td>
<td>TOLERANCE_INDUCTANCE</td>
<td>10</td>
<td>%</td>
<td>Tolerance of the design inductance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>DC RESISTANCE OF INDUCTOR</td>
<td>2.0</td>
<td>ohms</td>
<td>DC resistance of the buck inductor</td>
<td></td>
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</tr>
<tr>
<td>58</td>
<td>FACTOR_KLOSS</td>
<td>0.50</td>
<td></td>
<td>Factor that accounts for &quot;off-state&quot; power loss to be supplied by inductor (usually between 50% to 66%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>IRMS_INDUCTOR</td>
<td>0.533</td>
<td>A</td>
<td>Maximum inductor RMS current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>PLOSS_INDUCTOR</td>
<td>0.568</td>
<td>W</td>
<td>Maximum inductor losses</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>FREEWHEELING DIODE PARAMETERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>VF_FREEWHEELING</td>
<td>0.70</td>
<td>V</td>
<td>Forward voltage drop across the</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Column 1</td>
<td>Column 2</td>
<td>Column 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>----------</td>
<td>----------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>freewheeling diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIV_RATING</td>
<td>600.0 V</td>
<td>Peak inverse voltage rating of the freewheeling diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRR</td>
<td>30 ns</td>
<td>Reverse recovery time of the freewheeling diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIV_CALCULATED</td>
<td>539.2 V</td>
<td>Computed peak inverse voltage across the freewheeling diode</td>
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<td></td>
<td></td>
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<tr>
<td>I_RMS_DIODE</td>
<td>0.529 A</td>
<td>Maximum diode RMS current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLOSS_DIODE</td>
<td>0.356 W</td>
<td>Maximum freewheeling diode loss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RECOMMENDED_DIODE</td>
<td>BYV26C</td>
<td>Recommended freewheeling diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VF_BIAS</td>
<td>0.70 V</td>
<td>Forward voltage drop of the bias diode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_BIAS</td>
<td>2490 Ohms</td>
<td>Bias resistor (connected across FB and S pin). Results into IFB_BIAS value of 803.213 uA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_BP</td>
<td>N/A Ohms</td>
<td>No BP pin resistor required when output voltage is lower than 5.2V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_BP</td>
<td>0.1 uF</td>
<td>BP pin capacitor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_FB</td>
<td>3480 Ohms</td>
<td>Feedback resistor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_FB</td>
<td>10 uF</td>
<td>Feedback capacitor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_SOFTSTART</td>
<td>N/A uF</td>
<td>No soft-start capacitor required</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLOSS_FEEDBACK</td>
<td>0.004 W</td>
<td>Maximum feedback component losses</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
8 Performance Data

Electrical tests are done at room temperature otherwise specified.

8.1 *Full Load Efficiency vs. Input Line Voltage*

![Graph showing Efficiency vs. Line Voltage](image)

*Figure 6 – Efficiency vs. Line Voltage.*
8.2 **Efficiency vs. Load**

Measured using an E-load at CC mode loading Set-up. Output voltage is measured at the PCB side output terminal.

![Efficiency vs. Load](image)

**Figure 7** – Efficiency vs. Load.
8.3 *No-Load Input Power*

![Graph showing no-load input power vs. input line voltage.](image)

**Figure 8** – No Load Input Power vs. Input Line Voltage.
8.4 **Line and Load Regulation**

8.4.1 Line Regulation

Measured using an E-load at CC mode loading set-up. Output voltage is measured at the PCB side output terminal.

![Graph showing output voltage vs input voltage at full load.](image)

**Figure 9** – Output Voltage vs Input Voltage at Full Load.
8.4.2 Load Regulation
Measured using an E-load at CC mode loading set-up. Output voltage is measured at the PCB side output terminal.

![Graph showing output voltage vs load](image-url)

**Figure 10** – Output Voltage vs Load.
9 Electrical Test Data

9.1 Full Load Line Regulation and Efficiency

<table>
<thead>
<tr>
<th>Input</th>
<th>Input Measurement</th>
<th>Output Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAC (RMS)</td>
<td>Freq (Hz)</td>
<td>V\textsubscript{IN} (RMS)</td>
</tr>
<tr>
<td>90</td>
<td>60</td>
<td>89.97</td>
</tr>
<tr>
<td>100</td>
<td>60</td>
<td>100.00</td>
</tr>
<tr>
<td>115</td>
<td>60</td>
<td>115.01</td>
</tr>
<tr>
<td>120</td>
<td>60</td>
<td>119.99</td>
</tr>
<tr>
<td>132</td>
<td>60</td>
<td>131.99</td>
</tr>
<tr>
<td>180</td>
<td>60</td>
<td>180.00</td>
</tr>
<tr>
<td>200</td>
<td>50</td>
<td>199.96</td>
</tr>
<tr>
<td>230</td>
<td>50</td>
<td>229.96</td>
</tr>
<tr>
<td>240</td>
<td>50</td>
<td>239.99</td>
</tr>
<tr>
<td>265</td>
<td>50</td>
<td>264.96</td>
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<tr>
<td>277</td>
<td>60</td>
<td>276.99</td>
</tr>
<tr>
<td>300</td>
<td>60</td>
<td>300.06</td>
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</table>

9.2 No-Load Regulation and Standby Power

<table>
<thead>
<tr>
<th>Input</th>
<th>Input Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAC (RMS)</td>
<td>Freq (Hz)</td>
</tr>
<tr>
<td>90</td>
<td>60</td>
</tr>
<tr>
<td>100</td>
<td>60</td>
</tr>
<tr>
<td>115</td>
<td>60</td>
</tr>
<tr>
<td>120</td>
<td>60</td>
</tr>
<tr>
<td>132</td>
<td>60</td>
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<tr>
<td>180</td>
<td>60</td>
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<tr>
<td>200</td>
<td>50</td>
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<tr>
<td>230</td>
<td>50</td>
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<tr>
<td>240</td>
<td>50</td>
</tr>
<tr>
<td>265</td>
<td>50</td>
</tr>
<tr>
<td>277</td>
<td>60</td>
</tr>
<tr>
<td>300</td>
<td>60</td>
</tr>
</tbody>
</table>
10 Waveforms

10.1 Output Voltage Ripple

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 \( \mu \text{F} / 50 \text{ V} \) ceramic type and one (1) 10 \( \mu \text{F} / 50 \text{ V} \) aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

Figure 11 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.1.1 Output Ripple Voltage Test Data

<table>
<thead>
<tr>
<th>Input Voltage (V)</th>
<th>Line Frequency (Hz)</th>
<th>Ripple Voltage (V&lt;sub&gt;P-P&lt;/sub&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>100% Load</td>
</tr>
<tr>
<td>90</td>
<td>60</td>
<td>64</td>
</tr>
<tr>
<td>115</td>
<td>60</td>
<td>66</td>
</tr>
<tr>
<td>230</td>
<td>50</td>
<td>68</td>
</tr>
<tr>
<td>265</td>
<td>50</td>
<td>88</td>
</tr>
<tr>
<td>277</td>
<td>60</td>
<td>84</td>
</tr>
<tr>
<td>300</td>
<td>60</td>
<td>92</td>
</tr>
</tbody>
</table>
10.1.2 Output Ripple Voltage Waveform at Full Load

Figure 12 – 90 VAC 60 Hz.
Condition: 5 V, 500 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 64 mV.

Figure 13 – 115 VAC 60 Hz.
Condition: 5 V, 500 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 66 mV.

Figure 14 – 230 VAC 50 Hz.
Condition: 5 V, 500 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 68 mV.

Figure 15 – 265 VAC 50 Hz.
Condition: 5 V, 500 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 88 mV.
Figure 16 – 277 VAC 60 Hz.
Condition: 5 V, 500 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 84 mV.

Figure 17 – 265 VAC 50 Hz.
Condition: 5 V, 500 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 92 mV.

10.1.3 Output Ripple Voltage Waveform at 50% Load

Figure 18 – 90 VAC 60 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 96 mV.

Figure 19 – 115 VAC 60 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 107 mV.
**Figure 20** – 230 VAC 50 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 132 mV.

**Figure 21** – 265 VAC 50 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 150 mV.

**Figure 22** – 277 VAC 60 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 155 mV.

**Figure 23** – 300 VAC 60 Hz.
Condition: 5 V, 250 mA.
\( V_{\text{RIPPLE}} \), 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
\( V_{\text{RIPPLE(PK-PK)}} \): 161 mV.
10.1.4 Output Ripple Voltage Waveform at 25% Load

**Figure 24** – 90 VAC 60 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(\text{PK-PK})}}$: 93 mV.

**Figure 25** – 115 VAC 60 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(\text{PK-PK})}}$: 98 mV.

**Figure 26** – 230 VAC 50 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(\text{PK-PK})}}$: 124 mV.

**Figure 27** – 265 VAC 50 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(\text{PK-PK})}}$: 129 mV.
Figure 28 – 277 VAC 60 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 130 mV.

10.2 Start-up Profile
Tested using an E-load set at CC mode.

Figure 29 – 300 VAC 60 Hz.
Condition: 5 V, 125 mA.
$V_{\text{RIPPLE}}$, 50 mV / div., 10 ms / div.
Zoom, 200 µs / div.
$V_{\text{RIPPLE(PK-PK)}}$: 134 mV.

Figure 30 – 90 VAC 60 Hz, 500 mA Load.
Upper: $V_{\text{OUT}}$, 2 V / div., 5 ms / div.
Middle: $I_{\text{OUT}}$, 500 mA / div.
Lower: $V_{\text{OUT}}$, 100 V / div.
Rise Time: 5.8 ms.

Figure 31 – 115 VAC 60 Hz, 500 mA Load.
Upper: $V_{\text{OUT}}$, 2 V / div., 5 ms / div.
Middle: $I_{\text{OUT}}$, 500 mA / div.
Lower: $V_{\text{OUT}}$, 200 V / div.
Rise Time: 4.8 ms.
Figure 32 – 230 VAC 50 Hz, 500 mA Load.
Upper: $V_{OUT}$, 2 V / div., 5 ms / div.
Middle: $I_{OUT}$, 500 mA / div.
Lower: $V_{OUT}$, 500 V / div.
Rise Time: 3.7 ms.

Figure 33 – 265 VAC 50 Hz, 500 mA Load.
Upper: $V_{OUT}$, 2 V / div., 5 ms / div.
Middle: $I_{OUT}$, 500 mA / div.
Lower: $V_{OUT}$, 500 V / div.
Rise Time: 3.6 ms.

Figure 34 – 277 VAC 60 Hz, 500 mA Load.
Upper: $V_{OUT}$, 2 V / div., 5 ms / div.
Middle: $I_{OUT}$, 500 mA / div.
Lower: $V_{OUT}$, 1 kV / div.
Rise Time: 5.8 ms.

Figure 35 – 300 VAC 60 Hz, 500 mA Load.
Upper: $V_{OUT}$, 2 V / div., 5 ms / div.
Middle: $I_{OUT}$, 500 mA / div.
Lower: $V_{OUT}$, 1 kV / div.
Rise Time: 4.8 ms.
10.3 **Drain Voltage and Current Waveforms at Normal Operation**

**Figure 36** – 90 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: $V_{DS}$, 50 V / div., 2 ms / div.
Lower: $I_{DS}$, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(\text{MAX})}$: 133 V.
$I_{DS(\text{MAX})}$: 1.18 A.

**Figure 37** – 115 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: $V_{DS}$, 50 V / div., 2 ms / div.
Lower: $I_{DS}$, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(\text{MAX})}$: 173 V.
$I_{DS(\text{MAX})}$: 1.16 A.

**Figure 38** – 230 VAC 50 Hz, 500 mA.
Normal Operation at Full Load.
Upper: $V_{DS}$, 100 V / div., 2 ms / div.
Lower: $I_{DS}$, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(\text{MAX})}$: 343 V.
$I_{DS(\text{MAX})}$: 1.29 A.

**Figure 39** – 265 VAC 50 Hz, 500 mA.
Normal Operation at Full Load.
Upper: $V_{DS}$, 100 V / div., 2 ms / div.
Lower: $I_{DS}$, 500 mA / div.
Zoom in: 20 µs / div.
$V_{DS(\text{MAX})}$: 394 V.
$I_{DS(\text{MAX})}$: 1.41 A.
10.4 *Drain Voltage and Current Waveforms at Start-up Operation*

**Figure 40** – 277 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: \( V_{DS} \), 200 V / div., 2 ms / div.
Lower: \( I_{DS} \), 500 mA / div.
Zoom in: \( 20 \mu s / \text{div} \).
\( V_{DS(MAX)} \): 420 V.
\( I_{DS(MAX)} \): 1.41 A.

**Figure 41** – 300 VAC 60 Hz, 500 mA.
Normal Operation at Full Load.
Upper: \( V_{DS} \), 200 V / div., 2 ms / div.
Lower: \( I_{DS} \), 500 mA / div.
Zoom in: \( 20 \mu s / \text{div} \).
\( V_{DS(MAX)} \): 447 V.
\( I_{DS(MAX)} \): 1.41 A.

**Figure 42** – 90 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: \( V_{DS} \), 50 V / div., 2 ms / div.
Lower: \( I_{DS} \), 500 mA / div.
Zoom in: \( 10 \mu s / \text{div} \).
\( V_{DS(MAX)} \): 145 V.
\( I_{DS(MAX)} \): 1.62 A.

**Figure 43** – 115 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: \( V_{DS} \), 50 V / div., 2 ms / div.
Lower: \( I_{DS} \), 500 mA / div.
Zoom in: \( 10 \mu s / \text{div} \).
\( V_{DS(MAX)} \): 188 V.
\( I_{DS(MAX)} \): 1.69 A.
Figure 44 – 230 VAC 50 Hz, 500 mA.  
Start-up at Full Load.  
Upper: \( V_{DS} \), 100 V / div., 2 ms / div.  
Lower: \( I_{DS} \), 500 mA / div.  
Zoom in: 10 \( \mu \)s / div.  
\( V_{DS(\text{MAX})} \): 347 V.  
\( I_{DS(\text{MAX})} \): 2.06 A.

Figure 45 – 265 VAC 50 Hz, 500 mA.  
Start-up at Full Load.  
Upper: \( V_{DS} \), 100 V / div., 2 ms / div.  
Lower: \( I_{DS} \), 500 mA / div.  
Zoom in: 10 \( \mu \)s / div.  
\( V_{DS(\text{MAX})} \): 400 V.  
\( I_{DS(\text{MAX})} \): 2.21 A.

Figure 46 – 277 VAC 60 Hz, 500 mA.  
Start-up at Full Load.  
Upper: \( V_{DS} \), 100 V / div., 2 ms / div.  
Lower: \( I_{DS} \), 500 mA / div.  
Zoom in: 10 \( \mu \)s / div.  
\( V_{DS(\text{MAX})} \): 429 V.  
\( I_{DS(\text{MAX})} \): 2.64 A.

Figure 47 – 300 VAC 60 Hz, 500 mA.  
Start-up at Full Load.  
Upper: \( V_{DS} \), 100 V / div., 2 ms / div.  
Lower: \( I_{DS} \), 500 mA / div.  
Zoom in: 10 \( \mu \)s / div.  
\( V_{DS(\text{MAX})} \): 456 V.  
\( I_{DS(\text{MAX})} \): 2.77 A.
10.5 Freewheeling Diode Voltage and Current Waveform at Normal Operation

Figure 48 – 90 VAC 60 Hz, 500 mA.
Normal at Full Load.
Upper: $V_D$, 50 V / div., 2 ms / div.
Lower: $I_D$, 1 A / div.
Zoom in: 20 µs / div.
$V_D(\text{MAX})$: 139 V.
$I_D(\text{MAX})$: 0.829 A.

Figure 49 – 300 VAC 60 Hz, 500 mA.
Normal at Full Load.
Upper: $V_D$, 200 V / div., 2 ms / div.
Lower: $I_D$, 1 A / div.
Zoom in: 20 µs / div.
$V_D(\text{MAX})$: 484 V.
$I_D(\text{MAX})$: 0.962 A.

10.6 Freewheeling Diode Voltage and Current Waveform at Start-up Operation

Figure 50 – 90 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Upper: $V_D$, 50 V / div., 500 µs / div.
Lower: $I_D$, 1 A / div.
Zoom in: 20 µs / div.
$V_D(\text{MAX})$: 122 V.
$I_D(\text{MAX})$: 0.929 A.

Figure 51 – 115 VAC 60 Hz, 500 mA.
Start-up at Full Load.
Lower: $I_D$, 1 A / div.
Zoom in: 10 µs / div.
$V_D(\text{MAX})$: 470 V.
$I_D(\text{MAX})$: 2.29 A.
10.7 **Dynamic Load Response**
Tested using an e-load set at 50 Hz, 50% duty cycle and slew rate of 0.08 mA/s.

Voltage Overshoot and Undershoot During Dynamic Loading

<table>
<thead>
<tr>
<th>V&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>10-100%, 50 Hz Dynamic Load Response</th>
<th>Voltage Overshoot / Undershoot (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90 VAC 60 Hz</td>
<td>115 VAC 60 Hz</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(MAX)&lt;/sub&gt;</td>
<td>5.4</td>
<td>5.4</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(MIN)&lt;/sub&gt;</td>
<td>4.95</td>
<td>4.84</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>V&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>50-100%, 50 Hz Dynamic Load Response</th>
<th>Voltage Overshoot / Undershoot (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90 VAC 60 Hz</td>
<td>115 VAC 60 Hz</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(MAX)&lt;/sub&gt;</td>
<td>5.26</td>
<td>5.26</td>
</tr>
<tr>
<td>V&lt;sub&gt;OUT(MIN)&lt;/sub&gt;</td>
<td>4.87</td>
<td>4.86</td>
</tr>
</tbody>
</table>
10.7.1 10-100% 50 Hz Dynamic Load

**Figure 52** – 90 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{\text{OUT}}$, 1 V / div., 10 ms / div.
Lower: $I_{\text{OUT}}$, 200 mA / div.
$V_{\text{OUT(\text{MAX})}}$: 5.39 V.
$V_{\text{OUT(\text{MIN})}}$: 4.81 V.

**Figure 53** – 115 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{\text{OUT}}$, 1 V / div., 10 ms / div.
Lower: $I_{\text{OUT}}$, 200 mA / div.
$V_{\text{OUT(\text{MAX})}}$: 5.39 V.
$V_{\text{OUT(\text{MIN})}}$: 4.77 V.

**Figure 54** – 230 VAC 50 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{\text{OUT}}$, 1 V / div., 10 ms / div.
Lower: $I_{\text{OUT}}$, 200 mA / div.
$V_{\text{OUT(\text{MAX})}}$: 5.39 V.
$V_{\text{OUT(\text{MIN})}}$: 4.81 V.

**Figure 55** – 265 VAC 50 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{\text{OUT}}$, 1 V / div., 10 ms / div.
Lower: $I_{\text{OUT}}$, 200 mA / div.
$V_{\text{OUT(\text{MAX})}}$: 5.39 V.
$V_{\text{OUT(\text{MIN})}}$: 4.77 V.
**Figure 56** – 277 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.4 V.
$V_{OUT(MIN)}$: 4.68 V.

**Figure 57** – 300 VAC 60 Hz.
10-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.39 V.
$V_{OUT(MIN)}$: 4.8 V.

### 10.7.2 50-100% 50 Hz Dynamic Load

**Figure 58** – 90 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.26 V.
$V_{OUT(MIN)}$: 4.87 V.

**Figure 59** – 115 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.26 V.
$V_{OUT(MIN)}$: 4.86 V.
Figure 60 – 230 VAC 50 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.82 V.

Figure 61 – 265 VAC 50 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.84 V.

Figure 62 – 277 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.84 V.

Figure 63 – 300 VAC 60 Hz.
50-100% Load Dynamic Loading.
Upper: $V_{OUT}$, 1 V / div., 10 ms / div.
Lower: $I_{OUT}$, 200 mA / div.
$V_{OUT(MAX)}$: 5.25 V.
$V_{OUT(MIN)}$: 4.82 V.
10.8 **Output Short-Circuit Protection**

Short the main output (5 V) and monitor $I_{DS}$, output voltage, and output current. The first time fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

![Figure 64](image1)  
**Figure 64** – 90 VAC 60 Hz, Output Short.  
Upper: $V_{DS}$, 100 V / div.  
Middle: $I_{DS}$, 1 A / div., 1 s / div.  
$V_{DS(MAX)}$: 139 V.  
$I_{DS(MAX)}$: 1.75 A.

![Figure 65](image2)  
**Figure 65** – 300 VAC 60 Hz, Output Short.  
Upper: $V_{DS}$, 200 V / div.  
Middle: $I_{DS}$, 1 A / div., 1 s / div.  
$V_{DS(MAX)}$: 445 V.  
$I_{DS(MAX)}$: 2.59 A.
10.9 **Zero Crossing Detection Measurement**

The ZCD signal is sensitive to common mode noise introduced by voltage probes or other sources. Following are specific guidelines in probing and measuring the ZCD signal without compromising its signal integrity.

10.9.1 Current Measurement Set-up (Recommended Set-up)

![Image of ZCD Signal using Current Measurement Set-up.](image)

For ZCD current measurement set-up, the following steps are recommended for bench testing procedure:

- Use 10 Ω fixed resistor load instead of an E-load.
- Remove SMD resistor R8 and replace with 100 Ω axial resistor using a small wire to mount the current probe easily. Lower the resistance value if needed to increase the resolution.
- Place current probe away from the IC or PCB as shown in above figure.
- Use differential voltage probe to monitor the input voltage. Using voltage probe could distort the ZCD signal due to ground connection.
10.9.1.1 ZCD Signal Waveforms Using Current Measurement

ZCD Waveforms gathered at full load (5 V 500 mA)

Figure 67 – 115 VAC 60 Hz.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 300 µs.

Figure 68 – 115 VAC 60 Hz.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 100 µs.

Figure 69 – 230 VAC 50 Hz.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 212 µs.

Figure 70 – 230 VAC 50 Hz.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 500 µs / div.
ZCD Delay: 40.4 µs.
10.9.2 ZCD Voltage Measurement Set-up (Alternative Set-up)

As an alternate set-up, the ZCD voltage can be measured using the following recommendations:

- Connect input directly to AC mains line – do not use an electronic AC source
- Make sure that the oscilloscope ground (earth) line is connected
- Use differential voltage probes
- Use fixed resistor load instead of using e-load
10.9.2.1  ZCD Voltage Waveforms

10.9.2.1.1  ZCD Waveforms Gathered at No-Load Condition

**Figure 74** – 100 VAC Input, No-Load.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 27.16 µs.

**Figure 75** – 100 VAC Input, No-Load.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 251 µs.

10.9.2.1.2  ZCD Waveforms Gathered at Full Load (5 V 500 mA)

**Figure 76** – 100 VAC Input, No-Load.
ZCD Rising Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 23 µs.

**Figure 77** – 100 VAC Input, No-Load.
ZCD Falling Edge.
Time / div: 5 ms / div.
Zoom: 200 µs / div.
ZCD Delay: 223 µs.
Thermal Performance at Room Temperature
Thermal measurement done at room temperature.

11.1 Set-up
Open frame unit in vertical position was placed inside the acrylic box to eliminate the effect of ambient air flow. FLIR camera was used to measure components case temperature.

![Thermal Test Set-up Picture.](image)

Figure 78 – Thermal Test Set-up Picture.

11.2 Thermal Test Data Based from IR Thermal Camera Scan

<table>
<thead>
<tr>
<th>Component</th>
<th>Temperature(°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>90 V 60 Hz</td>
</tr>
<tr>
<td>U1 - LNK3307D</td>
<td>67.1</td>
</tr>
<tr>
<td>D2 - Freewheeling Diode</td>
<td>71.3</td>
</tr>
<tr>
<td>L4 - Buck Inductor</td>
<td>61.3</td>
</tr>
</tbody>
</table>
11.3 **Thermal Scan**

**Figure 79** – 90 VAC 60 Hz, 500 mA.
Ambient: 25 °C.
SP1: U1 – 67.1 °C.
SP2: D2 – 71.3 °C.

**Figure 80** – 90 VAC 60 Hz, 500 mA.
Ambient: 25 °C.
SP1: L4 – 61.3 °C.
**Figure 81** – 115 VAC 60 Hz, 500 mA.
Ambient: 25 °C.
SP1: U1 – 71.4 °C.
SP2: D2 – 73.3 °C.

**Figure 82** – 115 VAC 60 Hz, 500 mA.
Ambient: 25 °C.
SP1: L4 – 59.6 °C.
Figure 83 – 230 VAC 50 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 78.4 ºC.
SP2: D2 – 77.5 ºC.

Figure 84 – 230 VAC 50 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.1 ºC.

Figure 85 – 265 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76.5 ºC.
SP2: D2 – 76.5 ºC.

Figure 86 – 265 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 66.5 ºC.
Figure 87 – 277 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76 ºC.
SP2: D2 – 76.6 ºC.

Figure 88 – 277 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.2 ºC.

Figure 89 – 300 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: U1 – 76.2 ºC.
SP2: D2 – 77.1 ºC.

Figure 90 – 300 VAC 60 Hz, 500 mA.
Ambient: 25 ºC.
SP1: L4 – 68.3 ºC.
12 **Conducted EMI**

![Figure 91](image)

**Figure 91** – Conducted EMI Set-up Picture.

12.1 **Test Set-up Equipment**

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. 10 Ω resistor load.
4. Variac input voltage source set at 115 VAC and 230 VAC.
12.2 *Conducted Emission Scan*

Unit passed conducted EMI EN55022 limit with >10 dB uV margin at low line and > 6 dBuV at high line.

*Figure 92 – Conducted EMI Scan at 115 VAC.*
Figure 93 – Conducted EMI Scan at 230 VAC.
13 **Line Surge**

13.1 **Combination Wave Surge**
The unit was subjected to ±1000 V, combination wave surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

<table>
<thead>
<tr>
<th>DM Surge Level (V)</th>
<th>Input Voltage (VAC)</th>
<th>Injection Location</th>
<th>Injection Phase (°)</th>
<th>Test Result (Pass/Fail)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+1000</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
<tr>
<td>-1000</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
<tr>
<td>+1000</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>-1000</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>+1000</td>
<td>230</td>
<td>L to N</td>
<td>180</td>
<td>Pass</td>
</tr>
<tr>
<td>-1000</td>
<td>230</td>
<td>L to N</td>
<td>180</td>
<td>Pass</td>
</tr>
<tr>
<td>+1000</td>
<td>230</td>
<td>L to N</td>
<td>270</td>
<td>Pass</td>
</tr>
<tr>
<td>-1000</td>
<td>230</td>
<td>L to N</td>
<td>270</td>
<td>Pass</td>
</tr>
</tbody>
</table>

13.2 **Ring Wave Surge**
The unit was subjected to ±2500 V, combination wave surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

<table>
<thead>
<tr>
<th>DM Surge Level (V)</th>
<th>Input Voltage (VAC)</th>
<th>Injection Location</th>
<th>Injection Phase (°)</th>
<th>Test Result (Pass/Fail)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
<tr>
<td>-2500</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>-2500</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>180</td>
<td>Pass</td>
</tr>
<tr>
<td>-2500</td>
<td>230</td>
<td>L to N</td>
<td>180</td>
<td>Pass</td>
</tr>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>270</td>
<td>Pass</td>
</tr>
<tr>
<td>-2500</td>
<td>230</td>
<td>L to N</td>
<td>270</td>
<td>Pass</td>
</tr>
</tbody>
</table>
14 **Audible Noise**

The LNK3307D IC has a built-in state machine to minimize audible noise at light load condition. The current limit is automatically reduced at light load condition to minimize power inductor vibration. To reduce audible noise further, an off-the-shelf dog-bone or barrel type inductor is recommended. Horizontal mounting helps minimize PCB vibration that may amplify audible noise. Adding hot melt type glue around the power inductor L2 helps reduce audible noise at light load condition but will slightly increase audible noise at full load.

14.1 **Audible Noise Test Set-up**

![Figure 94](image-url) — Audible Noise Measurement Set-up Pictures.

![Figure 95](image-url) — Glue Point Locations.

<table>
<thead>
<tr>
<th>Glue application points</th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Location 1: L2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Location 2: Between L2 and C1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Glue material: Digikey Part no:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDL4062-ND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
14.2 **Audible Noise Measurements**

Audible noise measured from full load to no-load.

14.2.1 Audible Noise with No Glue Applied on the Board

---

**Figure 96** – Audible Noise Measurements at 120 VAC.

**Figure 97** – Audible Noise Measurements at 230 VAC.
14.2.2 Audible Noise with Glue Applied on the Board

Figure 98 – Audible Noise Measurements at 120 VAC.

Figure 99 – Audible Noise Measurements at 230 VAC.
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Author</th>
<th>Revision</th>
<th>Description and Changes</th>
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<td>1.0</td>
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<td>Apps &amp; Mktg</td>
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