Design Example Report

Title	***30 W Isolated Flyback Power Supply with StackFET Using InnoSwitch™3-AQ INN3977CQ***
Specification	30 VDC – 921 VDC Input; 30 VDC – 12 V / 0.3 A; 60 VDC – 12 V / 1 A; 400 VDC – 12 V / 2.5 A Outputs
Application	High Input Voltage For Automotive
Author	Applications Engineering Department
Document Number	DER-859Q
Date	March 25, 2020
Revision	1.1

Summary and Features

- High input voltage: up to 921 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >82 % efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
    - Insensitive to transformer variation
    - Extremely fast transient response independent of load timing

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 30 VDC to 921 VDC input, 12 V output, 30 W (maximum) power supply utilizing INN3977CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

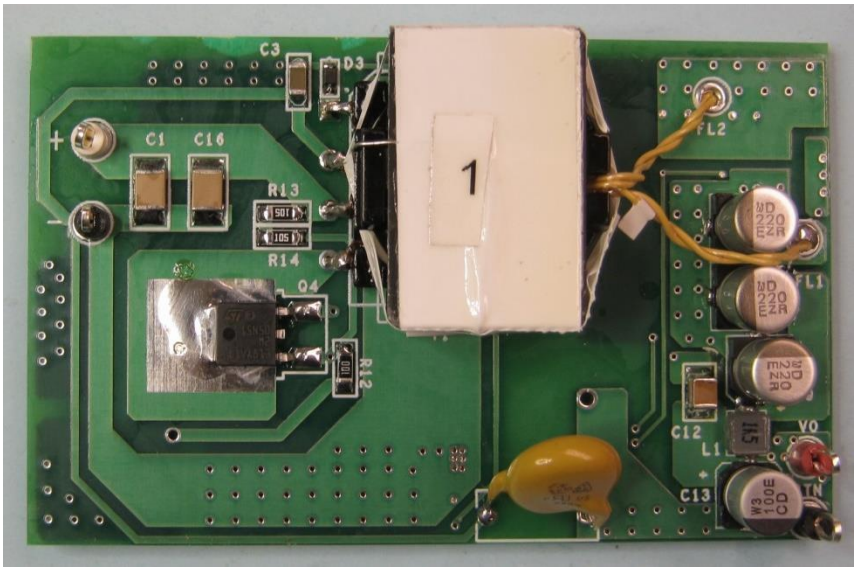

Figure 1 – Populated Circuit Board Photograph, Top.

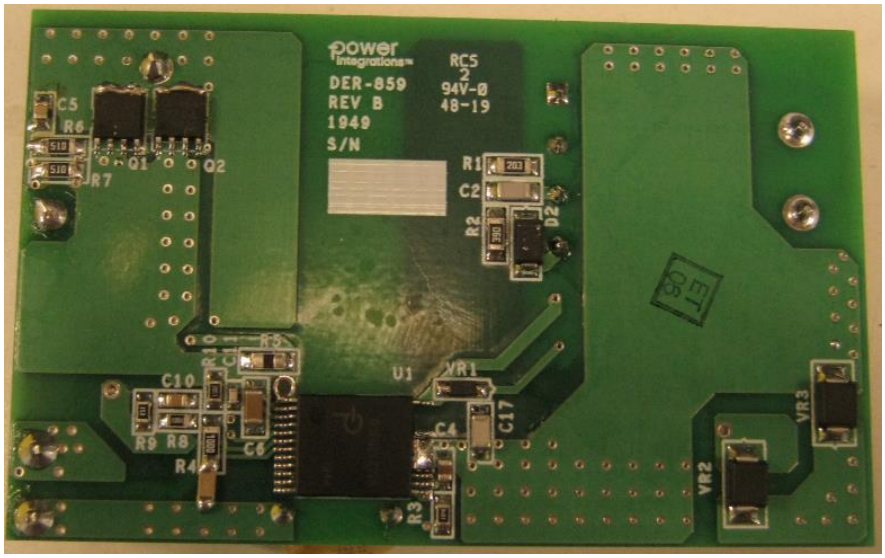

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	30	800	921	VDC	For Electric Vehicle Emergency PSU
Maximum Output Power						
	$\mathbf{P_{OUT}}$			10	W	V_{IN} of 30 VDC to 60 VDC.
	$\mathbf{P_{OUT}}$			20	W	V_{IN} of 60 VDC to 130 VDC.
	$\mathbf{P_{OUT}}$			30	W	V_{IN} of 400 VDC to 921 VDC.
Output						
Output Voltage	$\mathbf{V_{OUT}}$		12		V	±5% (V_{IN} > 400 VDC)
Output Current	$\mathbf{I_{OUT}}$			2.5	A	
Output Ripple Voltage	$\mathbf{V_{RIPPLE}}$			300	mV	On Board
Isolation						Meets IEC 60664-1 as a Minimum. Reinforce Better.
Ambient Temperature	$\mathbf{T_{AMB}}$	-40			W	V_{IN} 400 VDC to 921 VDC

3 Schematic

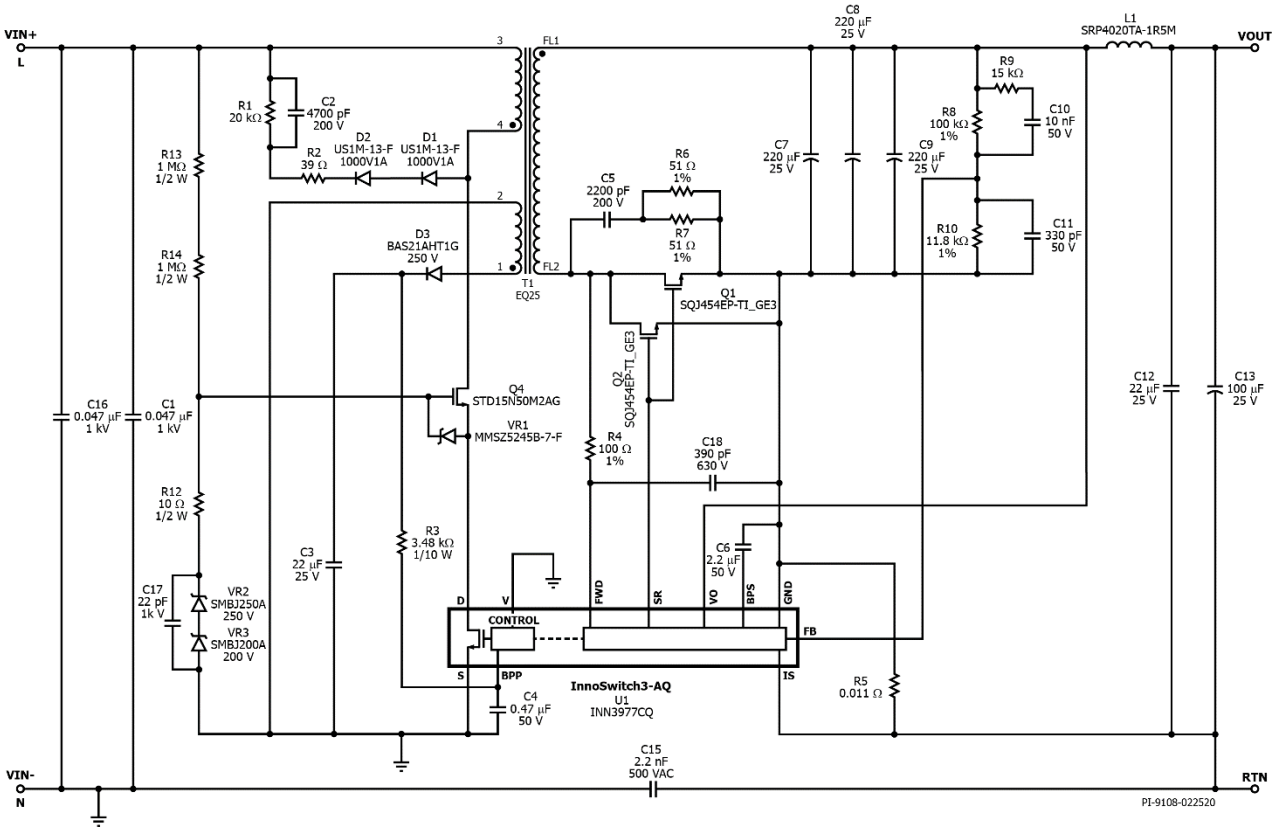

Figure 3 – Schematic.

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4 Circuit Description

4.1 *INN3977CQ IC Primary*

One end of the transformer primary is connected to the DC bus. The other is connected to a high-voltage (500 V) MOSFET (Q4) that is a cascode connected to the Drain of the integrated power MOSFET inside the INN3977CQ IC (U1). In this configuration the effective Drain-Source voltage rating of the primary is 1250 V_{PK}.

High-voltage ceramic capacitors C1 and C16 are used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D1, D2, R1, R2, and C2 limits the peak StackFET drain voltage to about 1100 V at 921 VDC input due to the effects of transformer leakage inductance. Capacitor C15, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D3 and capacitor C3, and fed in the BPP pin via a current limiting resistor R3.

Zener diode VR2 and VR3 clamp the maximum drain-source voltage across the INN3977CQ IC (U1) to below 650 V. VR1 ensures that the maximum gate-source voltage of Q4 does not exceed 15 V. Resistor R13, R14, and C17 provide bias to enhance the gate of Q4 when its source is switched low by the drain of U1.

4.2 *INN3977CQ IC Secondary*

The secondary-side of the INN397CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FETs Q1 and Q2. Low ESR capacitors, C7, C8, C9, C12, C13 and output inductor L1 provide filtering. RC snubber network comprising R6, R7, and C5 for Q1 and Q2 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R4 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the

device, fed into the VO pin. It will charge the decoupling capacitor C6 via an internal regulator.

Resistors R8 and R10 form a voltage divider network that senses the output voltage. INN3977CQ IC has an internal reference of 1.265 V. Capacitor C11 provides decoupling from high frequency noise affecting power supply operation, and C10 and R9 is the feedforward network to speed up the response time to lower the output ripple. The output current is sensed by R5 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.

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5 PCB Layout

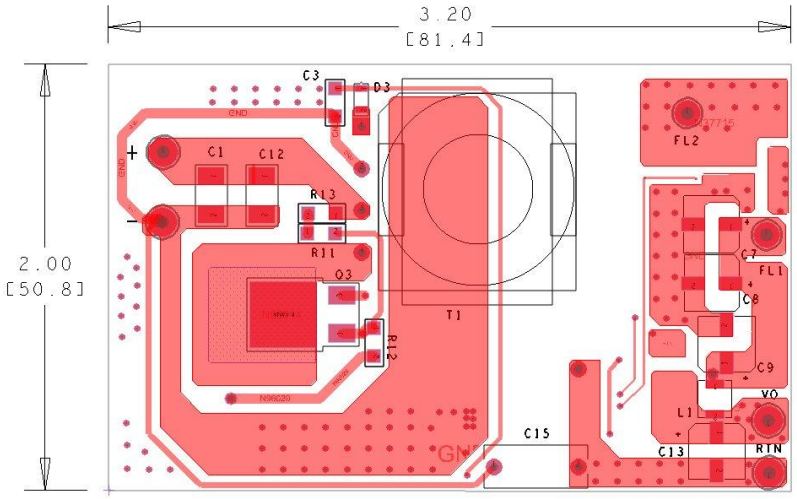

Figure 4 – Printed Circuit Board Layout (Top).

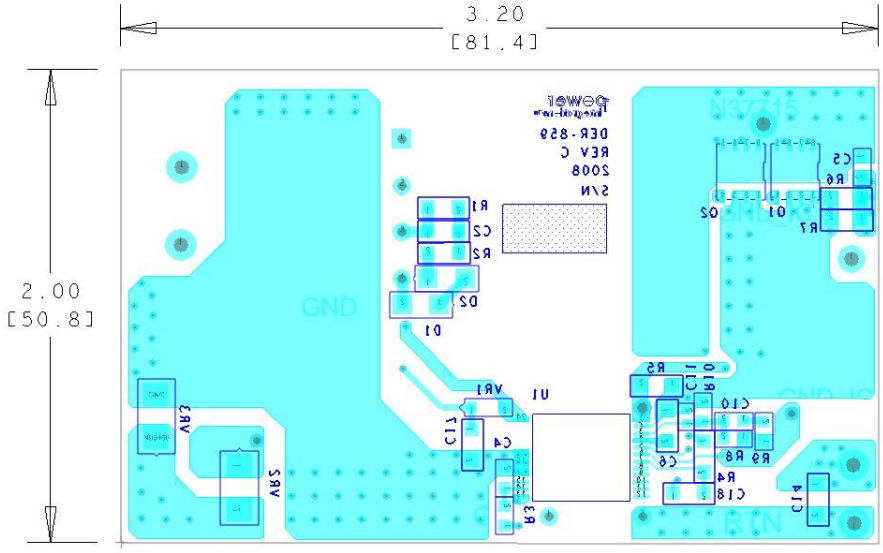

Figure 5 – Printed Circuit Board Layout (Bottom).

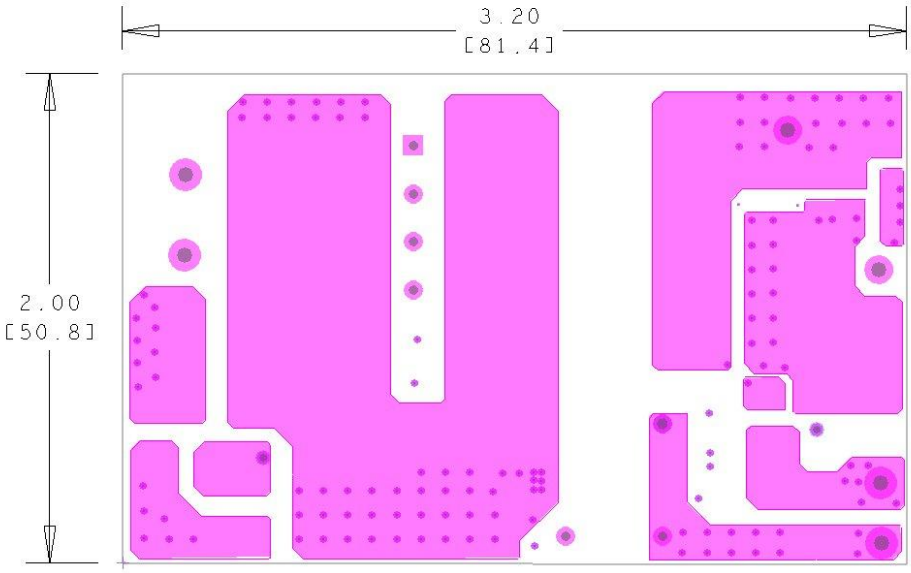

Figure 6 – Printed Circuit Board Layout (Internal layer 1).

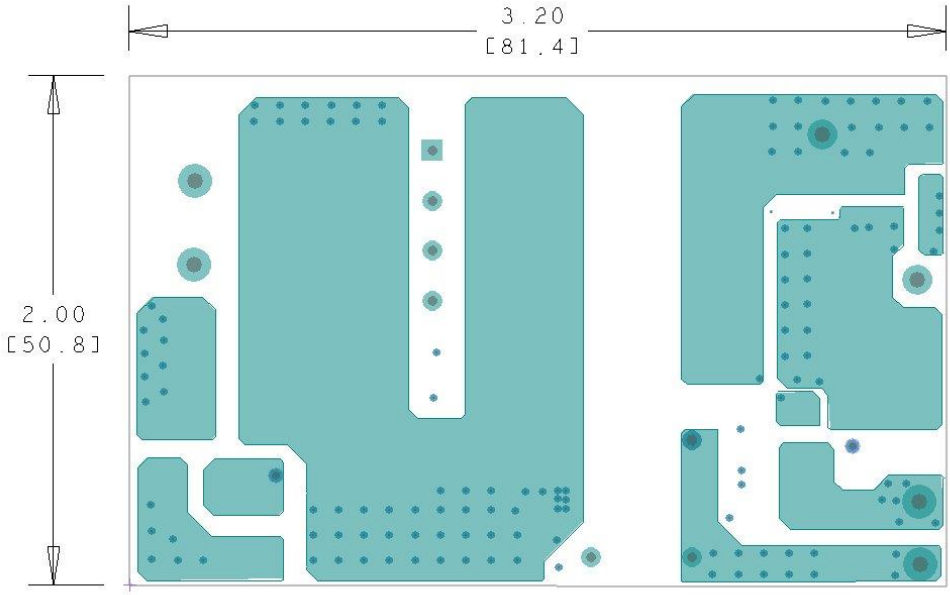

Figure 7 – Printed Circuit Board Layout (Internal layer 2).

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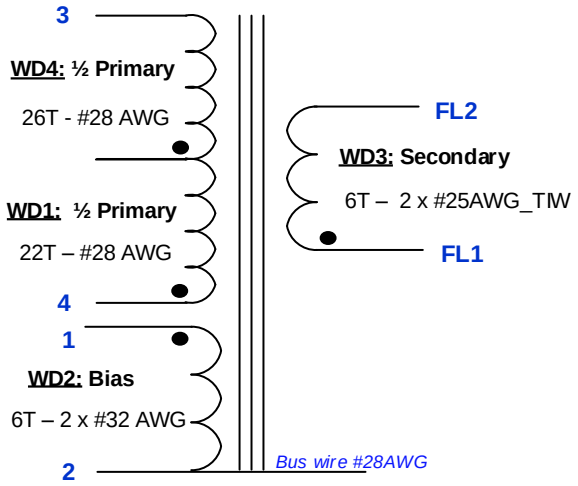
6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C16	0.047 μF, ±10%, 1000V (1kV), Ceramic, X7R, 1812	1812Y1K00473KST	Knowles Syfer
2	1	C2	4700 pF ±5% 200 V Ceramic C0G, NP0 1206	CGJ5H3C0G2D472J115AA	TDK
3	1	C3	22 μF, ±20%, 25 V, Ceramic, X5R, 1206	12063D226MAT2A	AVX
4	1	C4	0.47 μF,±10% ,50 V, Ceramic, X7R, 0805,-55°C ~ 125°C	CGA4J3X7R1H474K125AB	TDK
5	1	C5	2200 pF, ±10%, 200V, Ceramic, X7R, 0805	08052C222K4T2A	AVX
6	1	C6	2.2 μF, ±10%, 50 V, Ceramic, X7R, Bypass, Decoupling, 1206	C1206C225K5RACAUTO7210	KEMET
7	3	C7 C8 C9	220 μF, 25 V, Electrolytic, 0.260" L x 0.260" W x 0.315" H ,	EMZR250ARA221MF80G	United Chemi-Con
8	1	C10	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
9	1	C11	330 pF, ±5%, 50V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
10	1	C12	22 μF, 25 V, Ceramic, X7R, 1210	GRM32ER71E226KE15L	Murata
11	1	C13	100 μF, ±20%,25 V, Z=320 mΩ, Electrolytic, 0.260" L x 0.260" W x 0.315" H , SMD	UCD1E101MCL1GS	Nichicon
12	1	C15	2.2 nF, 500 Vac, Ceramic, Y1	VY1222M47Y5UG63V0	Vishay
13	1	C17	22 pF, 1000 V, Ceramic, COG, 1206	C1206C220KDGACTU	Kemet
14	1	C18	390 pF, 630 V, Ceramic, NP0, 1206	C3216C0G2J391J	TDK
15	2	D1 D2	1000 V, 1 A, Ultrafast Recovery, GPP, DO-214AC SMA	US1M-13-F	Diodes, Inc.
16	1	D3	Diode, General Purpose, Power, Switching, SS SWCH DIO, 250V,SC-76, SOD-323	BAS21HT1G	ON Semi
17	1	L1	1.5 μH, ±20%,Shielded, Wirewound, Inductor, 4.5 A, 42 mΩ Max, Automotive, AEC-Q200	SRP4020TA-1R5M	Bourns
18	2	Q1 Q2	MOSFET, N-Channel, 200 V, 13A (Tc), 68W (Tc), Automotive, AEC-Q101, PowerPAK SO-8	SQJ454EP-T1_GE3	Vishay
19	1	Q4	MOSFET, N-Channel 500 V, 10A (Tc), 85W (Tc), DPAK TO-252-3, DPak (2 Leads + Tab), SC-63	STD15N50M2AG	ST Micro
20	1	R1	RES, 20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
21	1	R2	RES, 39 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ390V	Panasonic
22	1	R3	RES, 3.48 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3481V	Panasonic
23	1	R4	RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
24	1	R5	0.011 Ω, ±1%, ±75ppm/°C, 1W, 1206, Automotive AEC-Q200, Current Sense,	ERJ-8CWFR011V	Panasonic
25	2	R6 R7	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
26	1	R8	RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
27	1	R9	RES, 15 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
28	1	R10	RES, 11.8 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
29	1	R12	RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
30	2	R13 R14	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
31	1	T1	Bobbin, EQ25, 4 pins, 4pri, 0sec	EQ-2506	Shen Zhen Xin Yu Jia
32	1	U1	InnoSwitch3-AQ Switch Integrated Circuit, InSOP24D	INN3977CQ	Power Integrations
33	1	VR1	Diode ZENER 15 V 500 mW SOD123	MMSZ5245B-7-F	Diodes, Inc.
34	1	VR2	TVS DIODE, UNIDIRECTIONAL, 250VWM, DO214AA	SMBJ250A	Littlefuse
35	1	VR3	200 V, 224V breakdown, 1.9 A peak Pulse,600 W peak pulse, DO214AA	SMBJ200A	Littlefuse

7 Transformer Design

7.1 *Electrical Diagram*



7.2 *Electrical Specification*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	1250 µH ±5%
Resonant Frequency	Between pin 3 and 4, other windings open.	1,200 kHz (Min.)
Primary Leakage Inductance	Between pin 3 and 4, with pins: FL1-FL2 shorted.	7.0 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EQ27, ACP-95.
[2]	Bobbin: EQ2506 – Vertical – 4pins (4/0); PI#: 25-01095-00.
[3]	Magnet Wire: **#**28 AWG, Double Coated.
[4]	Magnet Wire: **#**32 AWG, Double Coated.
[5]	Magnet Wire: #25 AWG, Triple Insulated Wire.
[6]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 4.25 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 27.5 mm x 52 mm.
[9]	Varnish: Dolph BC-359.

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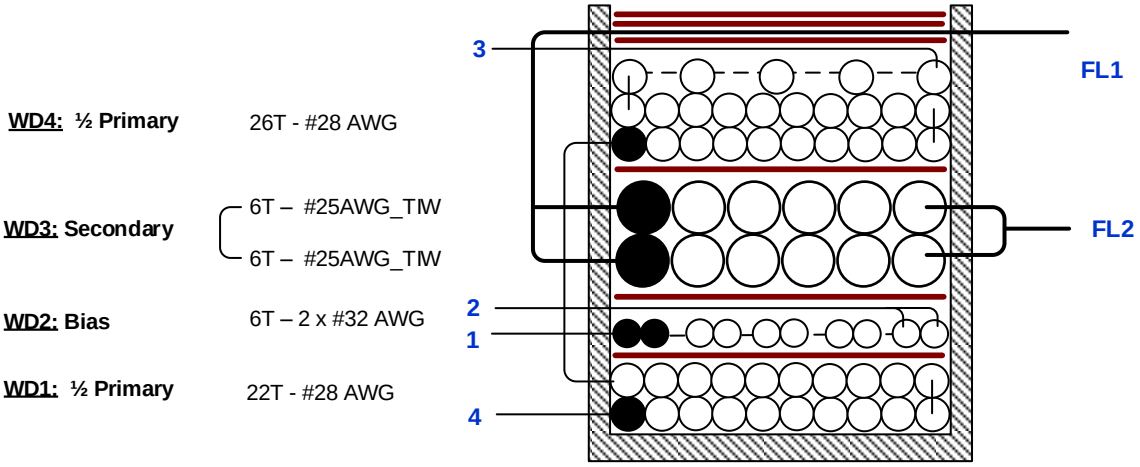
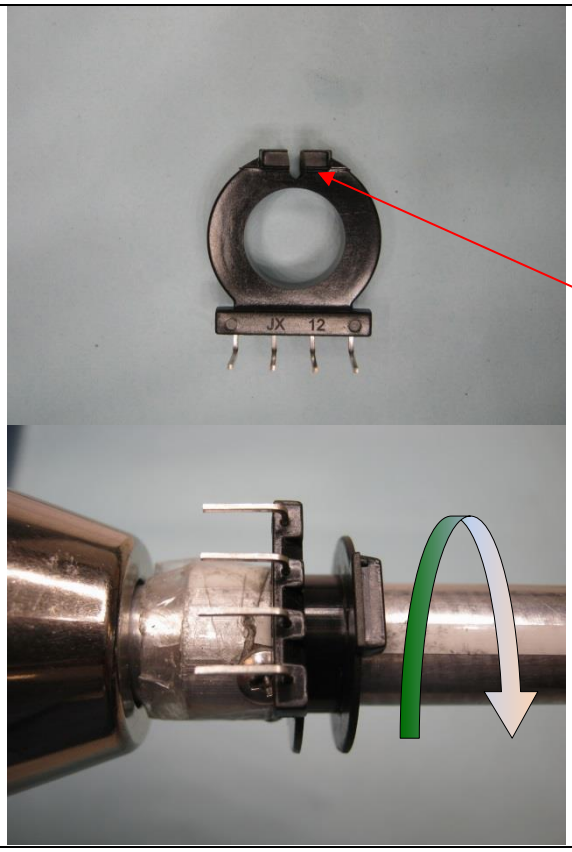
7.4 *Transformer Build Diagram*



7.5 *Transformer Instruction*

Winding Preparation	Make 2 slots with 2 mm width on flanges of secondary side of bobbin Item [2], (see illustration below). Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 4, wind 22 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias	Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.
Insulation	1 layer of tape Item [7].
WD3 Secondary	Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1", mark as FL1, and wind 6 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1" and mark as FL2. Repeat same winding above and on top, also start as FL1 and end FL2.
Insulation	1 layer of tape Item [7].
WD4 2nd Primary	Using wire floating from WD1, continue winding 26 turns in 2 ½ layers, and terminate at pin 3.
Insulation	Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.
Finish Assembly	Gap core halves to get 1250 μH. Use 50 mm of bus wire Item [6], solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9]. Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration below).

7.6 *Winding Illustrations*

Winding Preparation		Make <u>2 slots</u> with 2 mm width on flanges of secondary side of bobbin Item [2]. Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.

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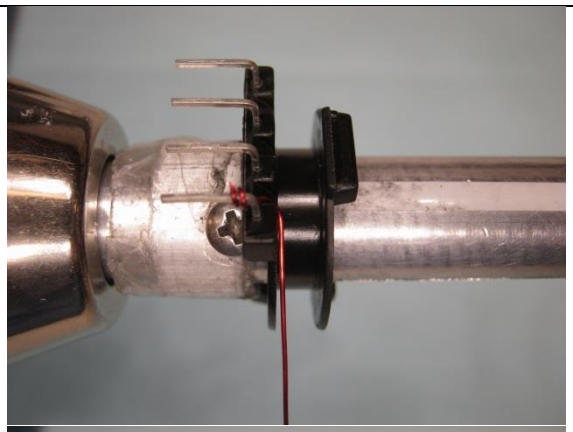
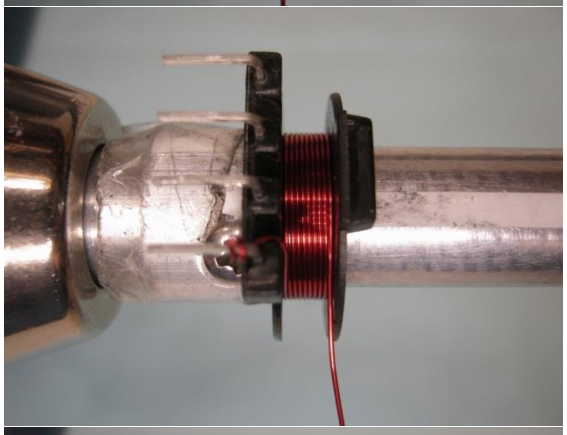
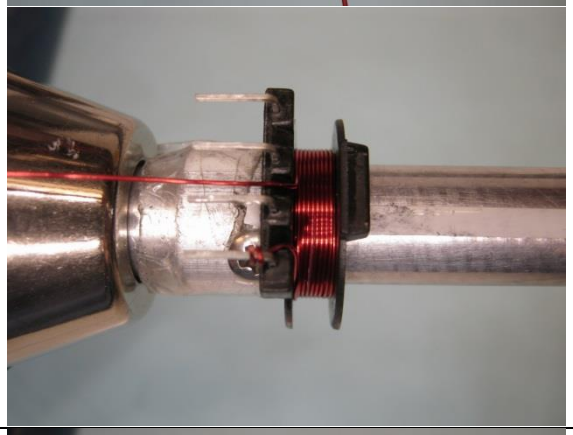
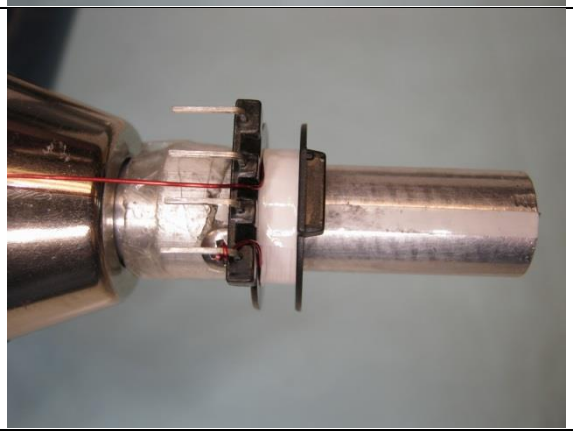
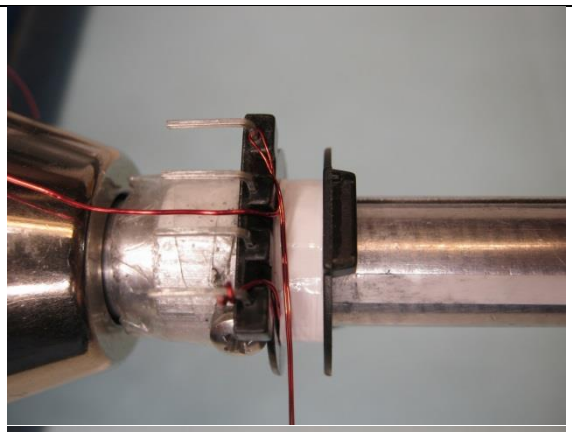
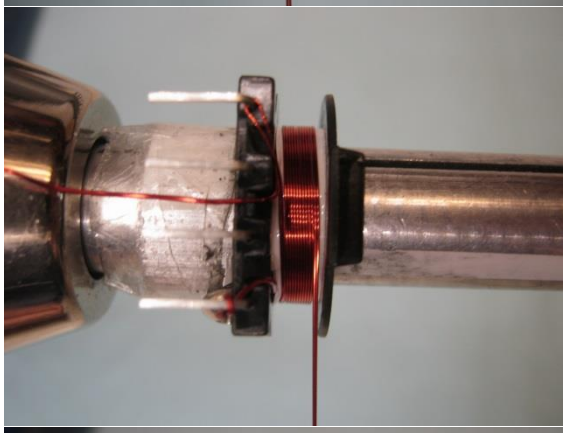
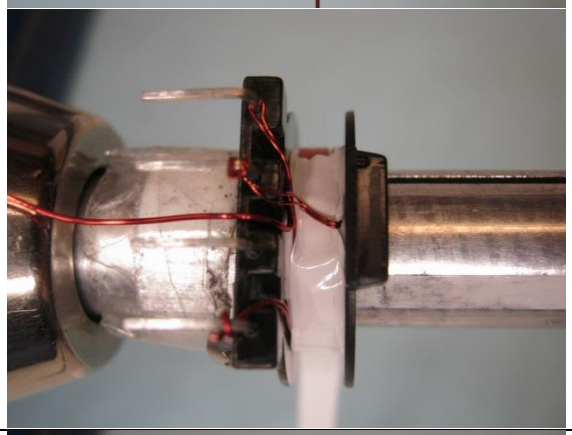
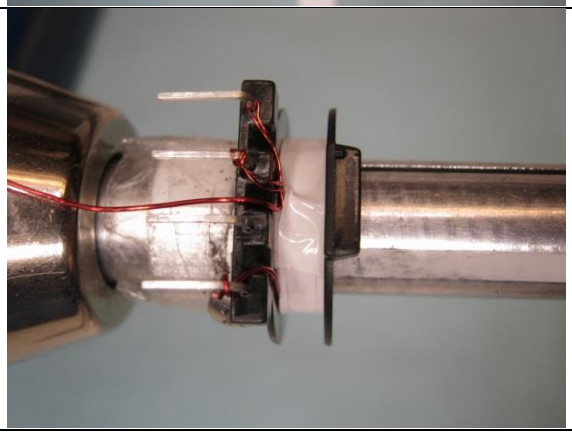
WD1 **1st Primary**	  	Start at pin 4, wind 22 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.
Insulation		1 layer of tape Item [7].

WD2: Bias	  	Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.
Insulation		1 layer of tape Item [7].

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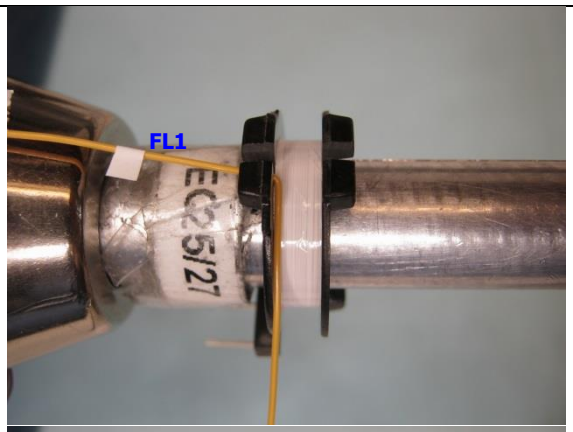
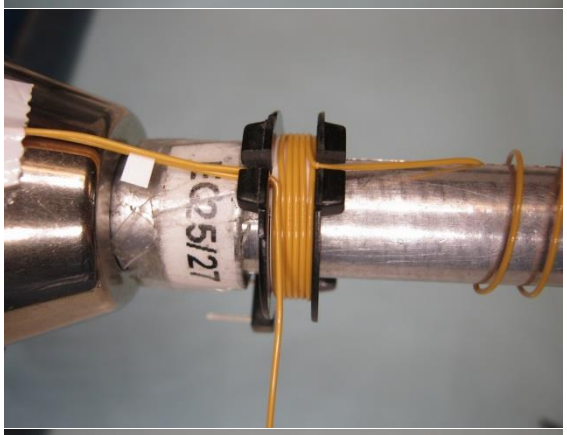
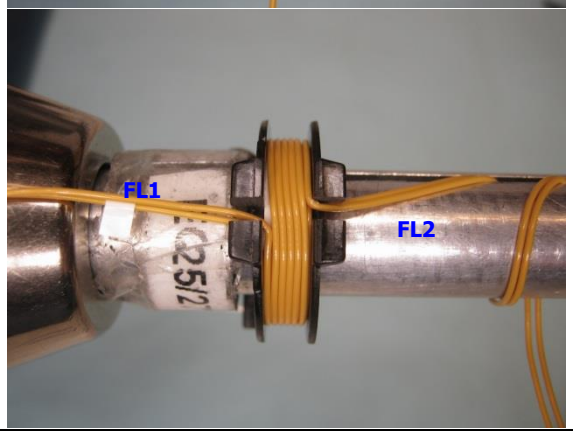
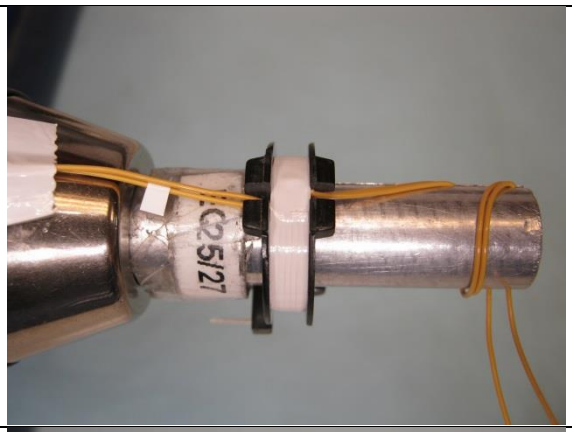
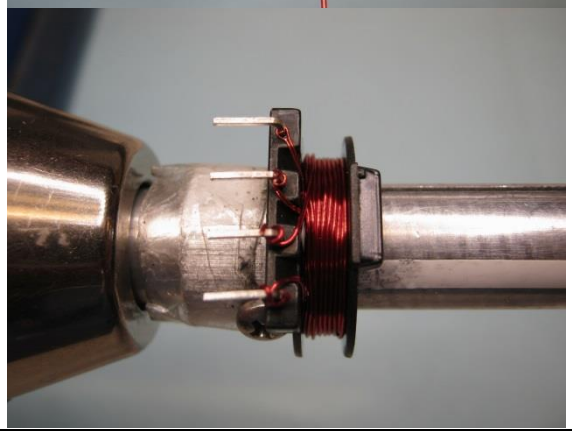
WD3 **Secondary**	   	Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1”, mark as FL1, and wind 6 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1” and mark as FL2. Repeat same winding above and on top, also start as FL1 and end FL2.

Insulation		1 layer of tape Item [8].
WD4 **2nd Primary**	  	Using wire floating from WD1, continue winding 26 turns in 2 ½ layers, and terminate at pin 3.

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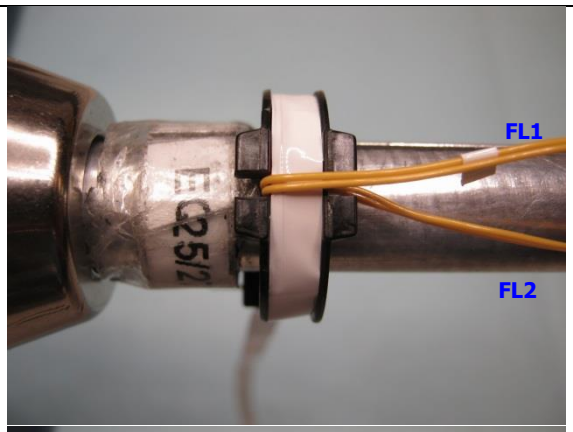
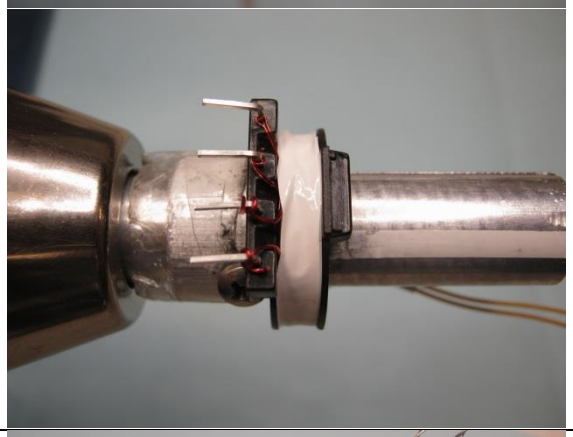
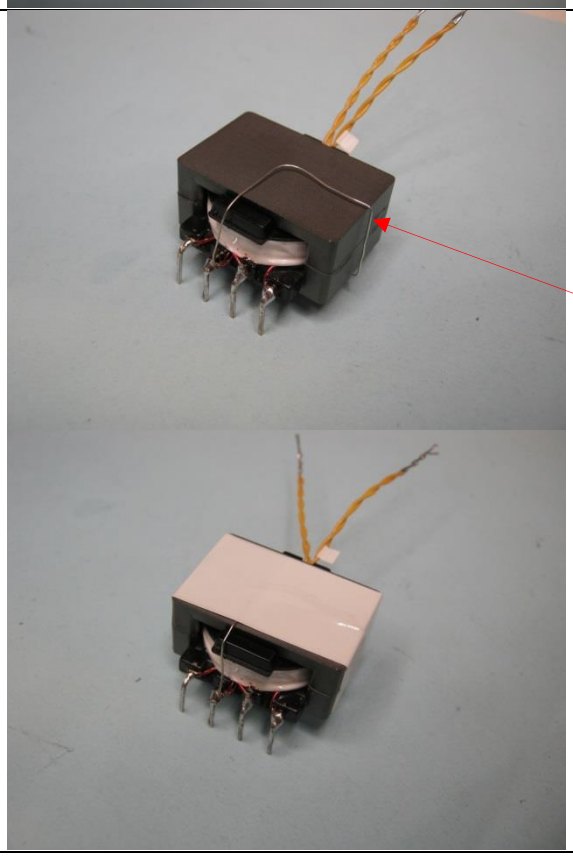
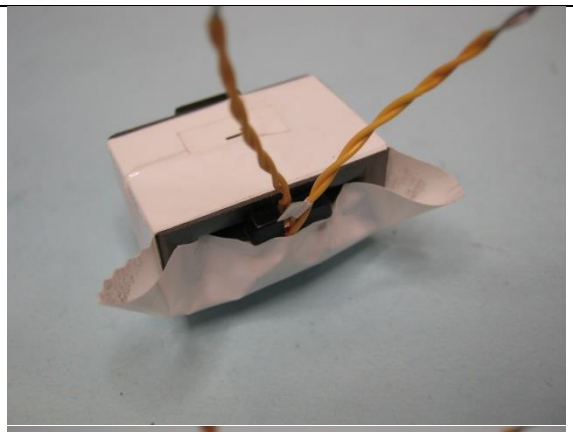
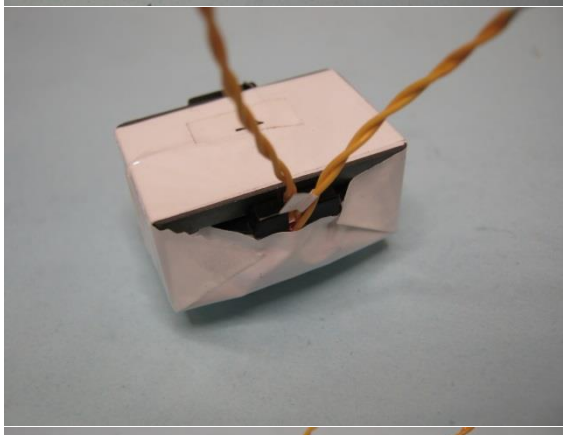
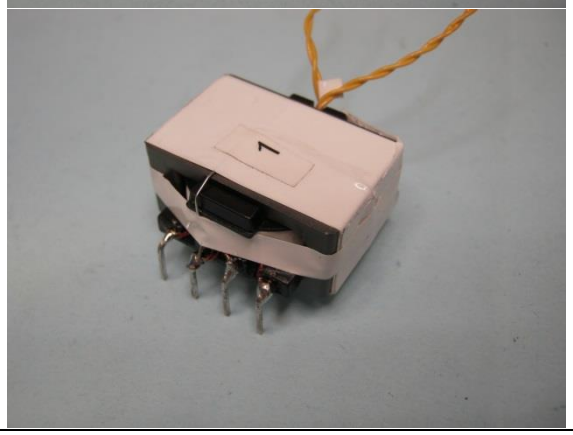
Insulation	 	Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.
Finish		Gap core halves to get 1250 μH. Use 50 mm of <u>bus wire Item [6]</u>, solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9]. Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration beside).







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8 Performance Data

All measurements performed with room ambient temperature. Measured at PCB output terminal.

8.1 *Efficiency vs. Load and Input Voltage*

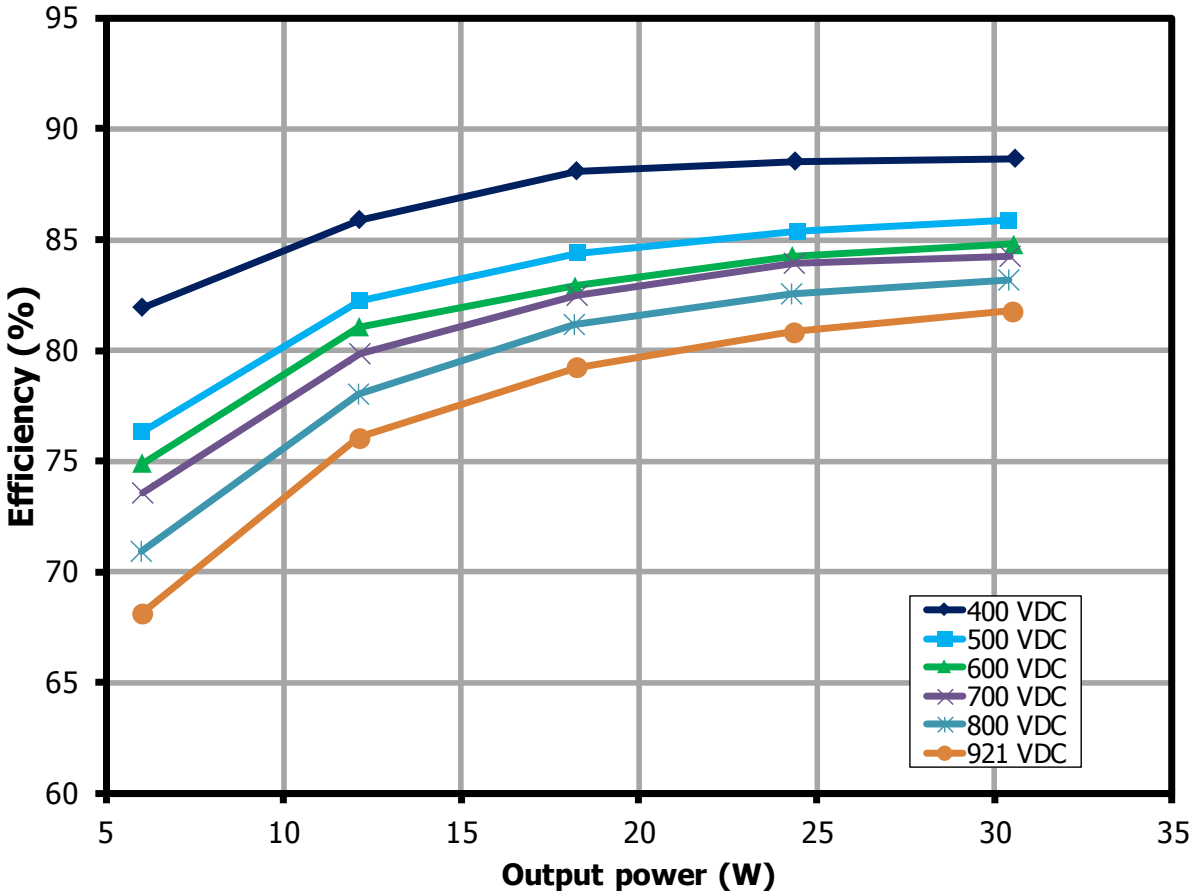

Figure 8 – Efficiency vs. Load and Input Voltage, Room Temperature.

8.2 *Full Load Efficiency vs. Line*

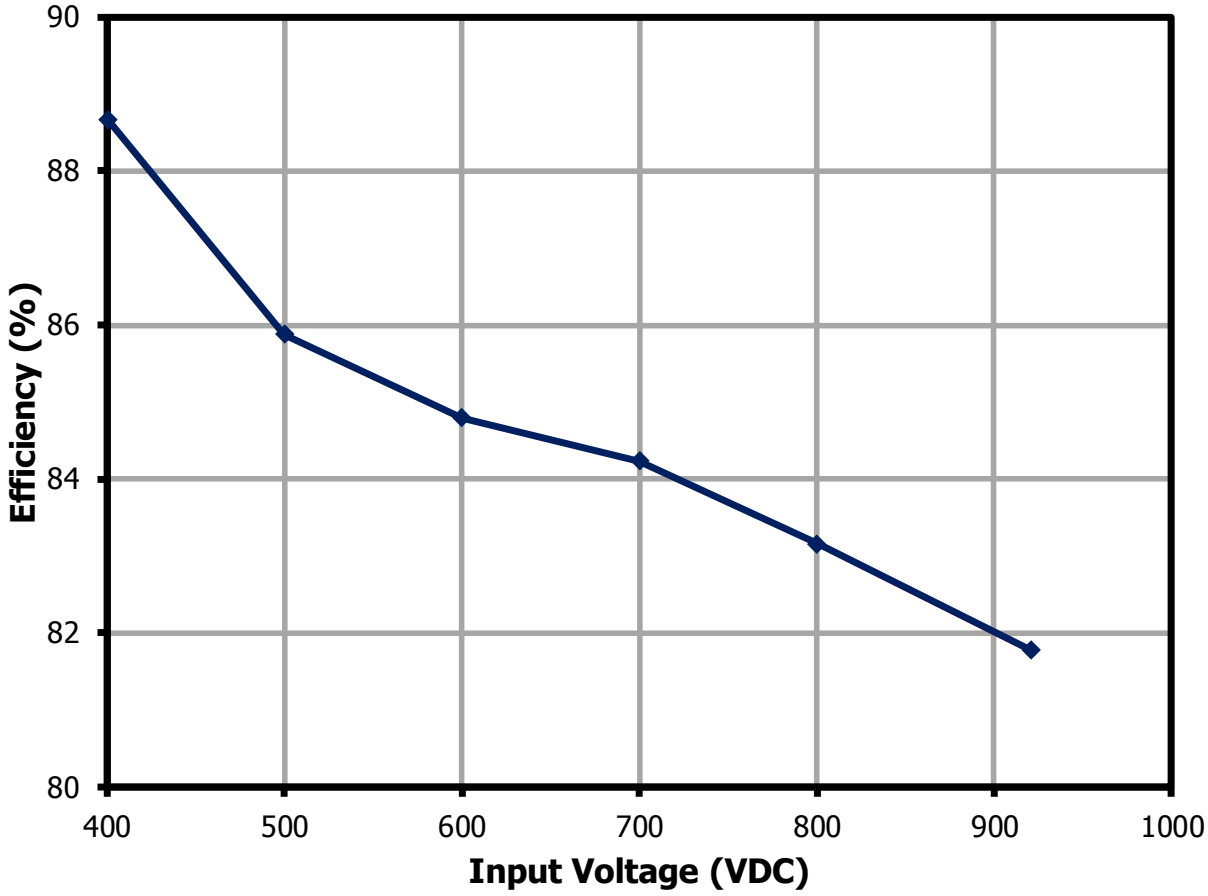

Figure 9 – Efficiency vs. Line (VDC), Room Temperature.

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8.3 *No-Load Input Power*

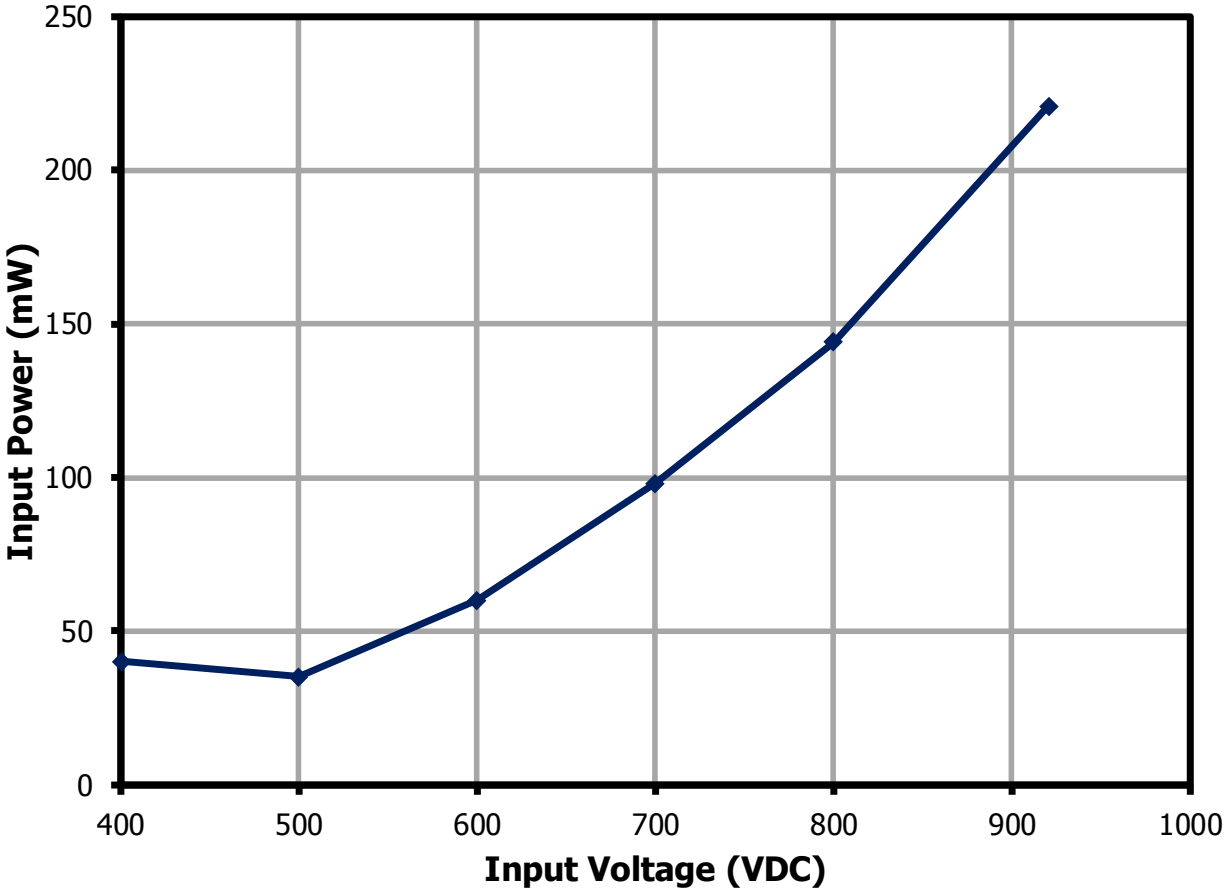

Figure 10 – No-Load Input Power, Room Temperature.

8.4 *Load and Line Regulation*

Measurements taken at 0% to 100% of rated load

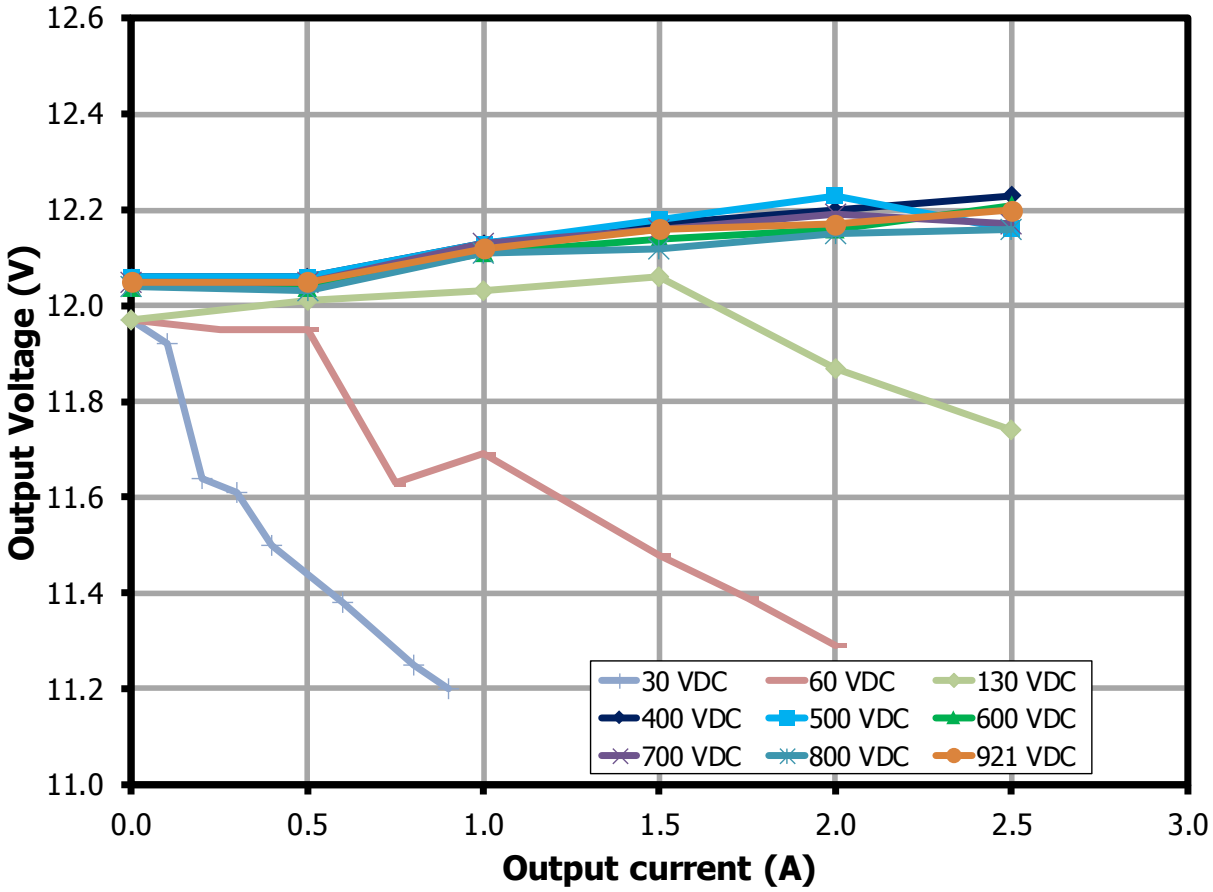

Figure 11 – Output Voltage vs. Output Current and Input Voltage (VDC), Room Temperature.

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9 Waveforms

9.1 *INN3977CQ Drain Voltage and Current, Steady-State*

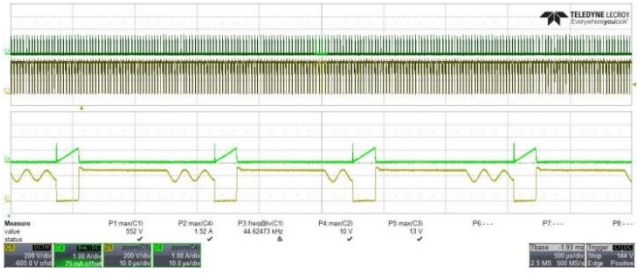

Figure 12 – Drain Voltage and Current Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 552 V.
Upper: I_{DRAIN}, 1 A, 500 µs / div.
Lower: V_{DRAIN}, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

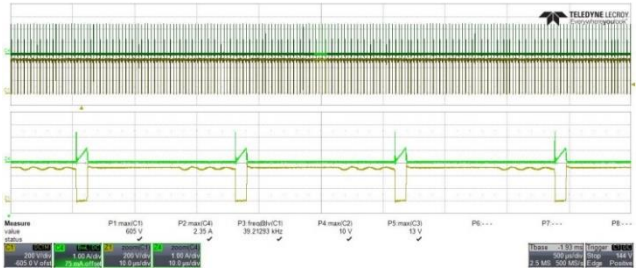

Figure 13 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 605 V.
Upper: I_{DRAIN}, 1 A, 500 µs / div.
Lower: V_{DRAIN}, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

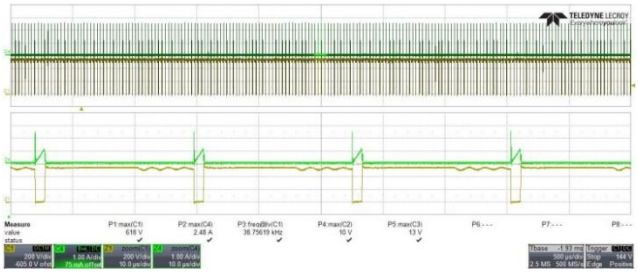

Figure 14 – Drain Voltage and Current Waveforms.
V_{IN} = 921 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 618 V.
Upper: I_{DRAIN}, 1 A, 500 µs / div.
Lower: V_{DRAIN}, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

9.2 *Total and StackFET Drain to Source Voltage, Steady-State*

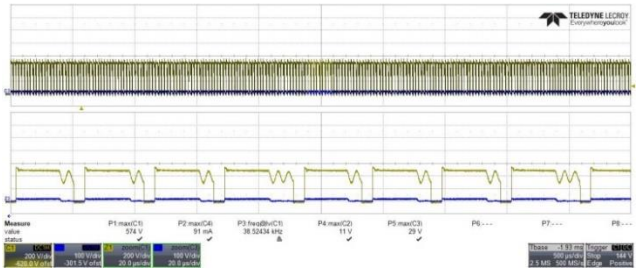

Figure 15 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 2.5 A.
$V_{STACKFETDS(MAX)}$ = 29 V, $V_{TOTAL(MAX)}$ = 574 V.
Yellow: V_{TOTAL}, 200 V , 500 µs / div.
Blue: $V_{STACKFET}$, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

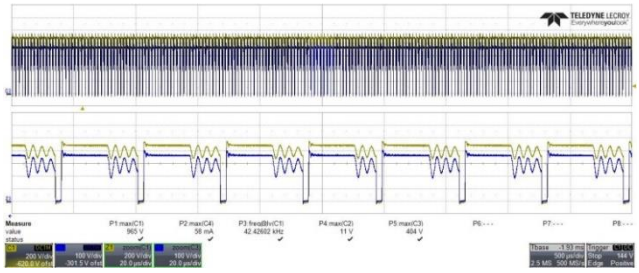

Figure 16 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
$V_{STACKFETDS(MAX)}$ = 404 V, $V_{TOTAL(MAX)}$ = 965 V.
Yellow: V_{TOTAL}, 200 V , 500 µs / div.
Blue: $V_{STACKFET}$, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

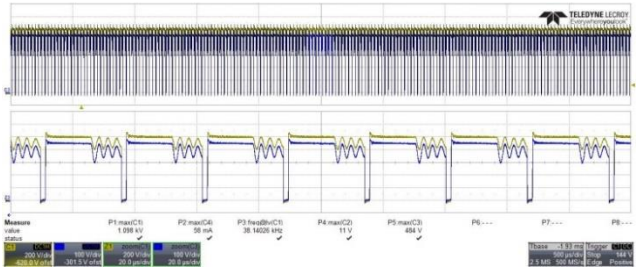

Figure 17 – Total and STACKFET Drain to Source Voltage Waveforms.
V_{IN} = 921 VDC, I_{OUT} = 2.5 A.
$V_{STACKFETDS(MAX)}$ = 484 V, $V_{TOTAL(MAX)}$ =1098 V.
Yellow: V_{TOTAL}, 200 V , 500 µs / div.
Blue: $V_{STACKFET}$, 200 V, 500 µs / div.
Bottom Half: Zoom @ 10 µs / div.

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9.3 *SR FET Waveforms, Steady-State*

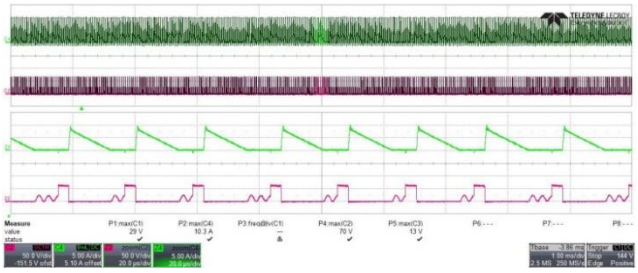

Figure 18 – Drain Voltage and Current Waveforms.
V_{IN} = 400 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 70 V, $I_{DRAIN(MAX)}$= 10.3 A.
Upper: I_{DRAIN}, 5 A, 1 ms / div.
Lower: $V_{DRAIN-SOURCE}$, 50 V, 1 ms / div.
Bottom Half: Zoom @ 20 µs / div.

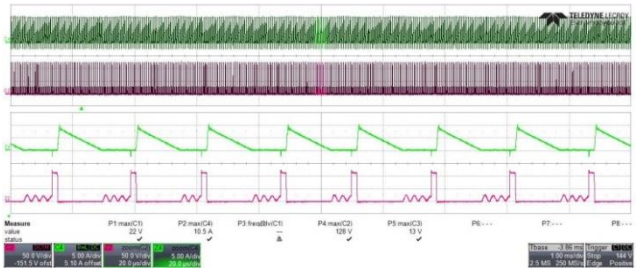

Figure 19 – Drain Voltage and Current Waveforms.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 128 V, $I_{DRAIN(MAX)}$= 10.5 A.
Upper: I_{DRAIN}, 5 A, 1 ms / div.
Lower: $V_{DRAIN-SOURCE}$, 50 V, 1 ms / div.
Bottom Half: Zoom @ 20 µs / div

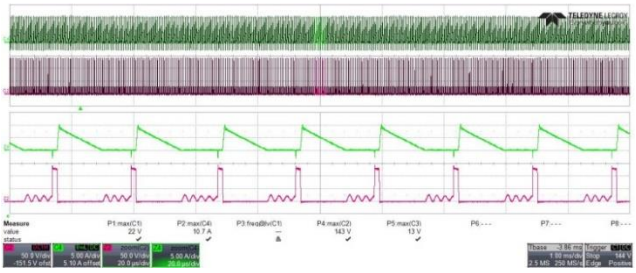

Figure 20 – Drain Voltage and Current Waveforms.
V_{IN} = 921 VDC, I_{OUT} = 2.5 A.
$V_{DS(MAX)}$ = 143 V, $I_{DRAIN(MAX)}$= 10.7 A.
Upper: I_{DRAIN}, 5 A, 1 ms / div.
Lower: $V_{DRAIN-SOURCE}$, 50 V, 1 ms / div.
Bottom Half: Zoom @ 20 µs / div.

9.4 *Output Ripple Measurements*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor includes one (1) 1 μF/50 V ceramic type.

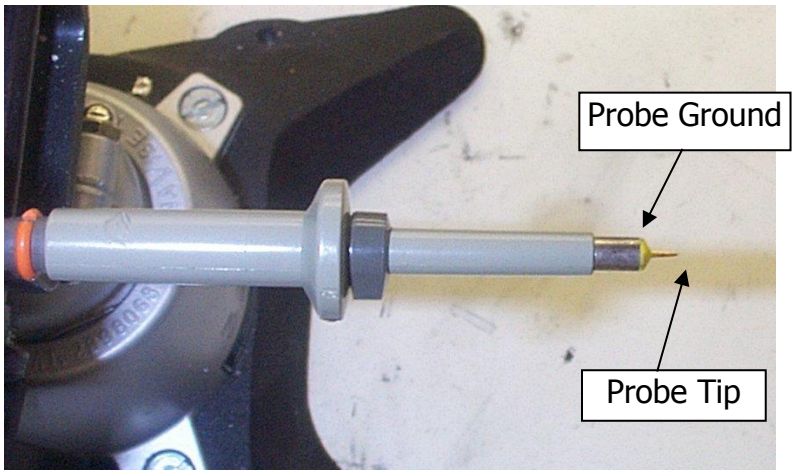

Figure 21 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

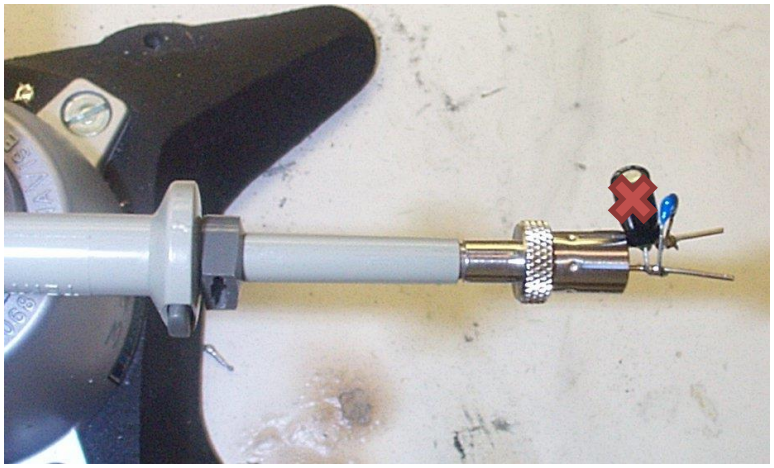

Figure 22 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)

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9.5 *100% Loading Condition*

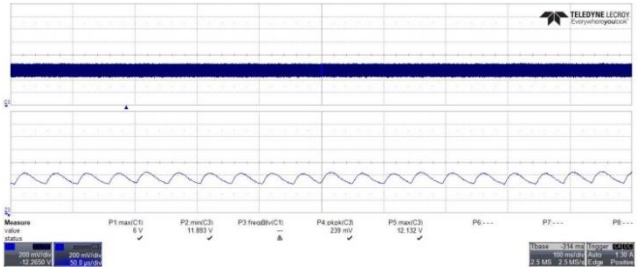

Figure 23 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 2.5 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 239 mV_{P-P}.

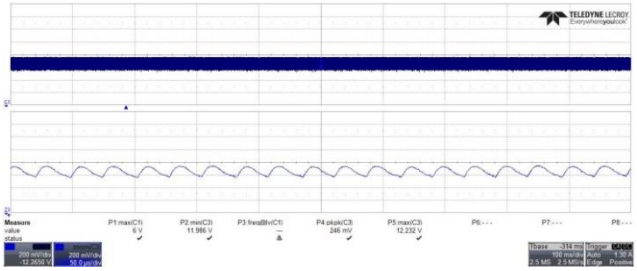

Figure 24 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 246 mV_{P-P}.

9.6 *75 % Loading Condition*

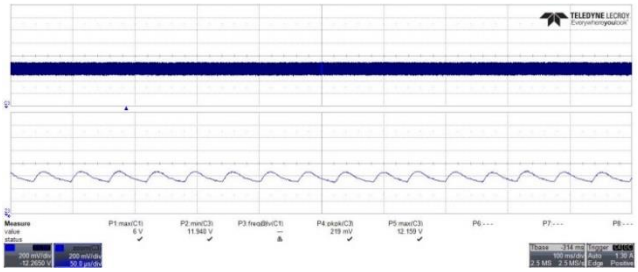

Figure 25 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 1.8 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 219 mV_{P-P}.

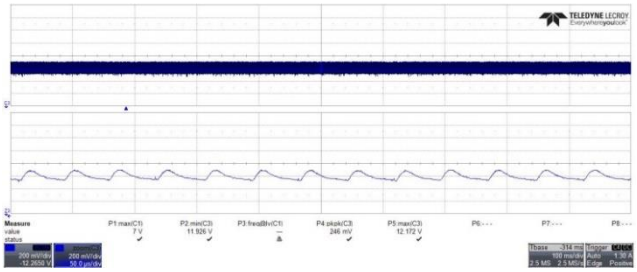

Figure 26 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.8 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 246 mV_{P-P}.

9.7 *50% Loading Condition*

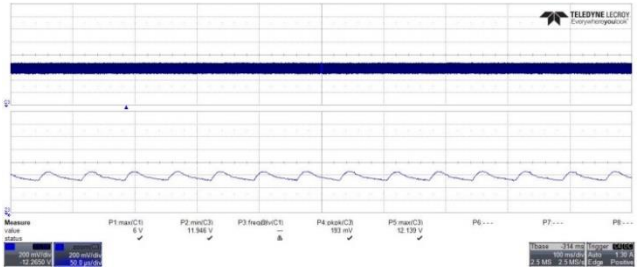

Figure 27 – Output Voltage Ripple.
V_{IN} =400 VDC, I_{OUT} = 1.25 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 193 mV_{P-P}.

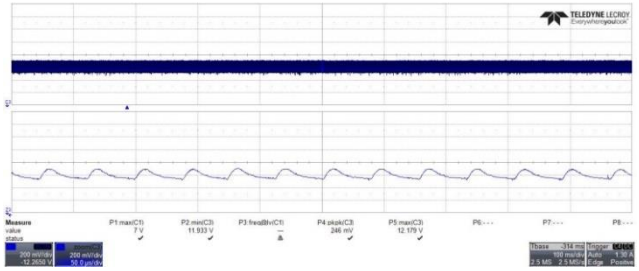

Figure 28 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 1.25 A.
Top Half: V_{OUT}, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 246 mV_{P-P}.

9.8 *25% Loading Condition*

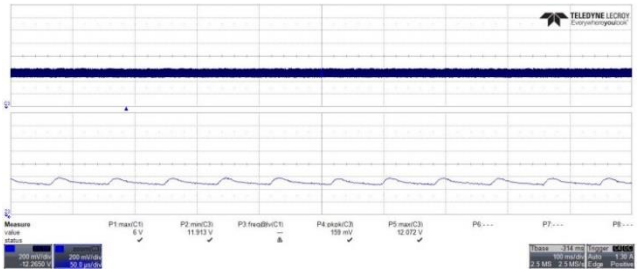

Figure 29 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 0.62 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 159 mV_{P-P}.

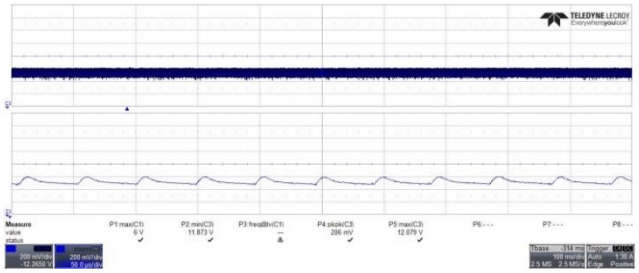

Figure 30 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0.62 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 206 mV_{P-P}.

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9.9 *0% Loading Condition*

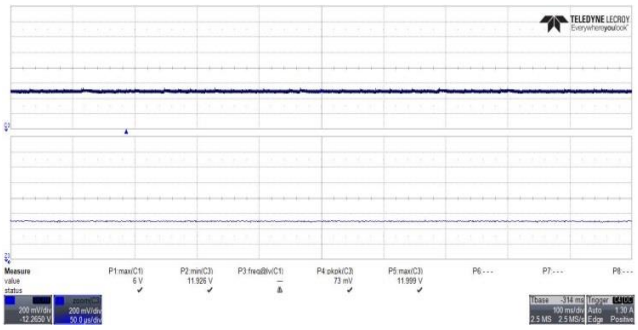

Figure 31 – Output Voltage Ripple.
V_{IN} = 400 VDC, I_{OUT} = 0 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 73 mV_{P-P}.

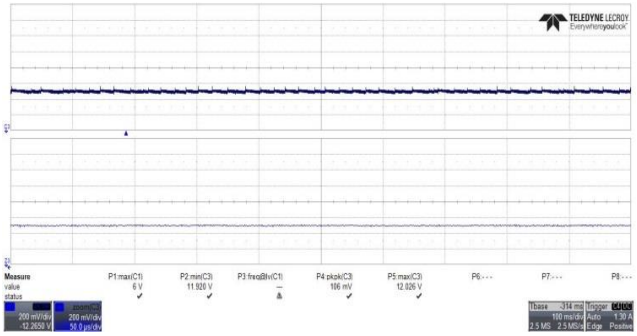

Figure 32 – Output Voltage Ripple.
V_{IN} = 800 VDC, I_{OUT} = 0 A.
Top Half: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 50 μs / div.
V_{RIPPLE} = 106 mV_{P-P}.

9.10 *Output Load Transient*

9.10.1 Output Load Transient, 100% to 0% Load

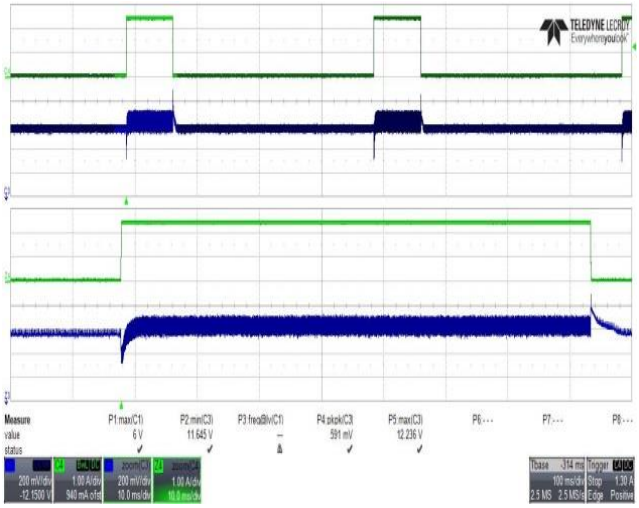

Figure 33 – Output Load Transient, 100% to 0% Load.
V_{IN} = 400 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 11.79 V, $V_{OUT(MIN)}$= 11.25 V.
Upper: $I_{OUT,}$ 1 A, 100 ms / div.
Lower: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 10 ms / div.

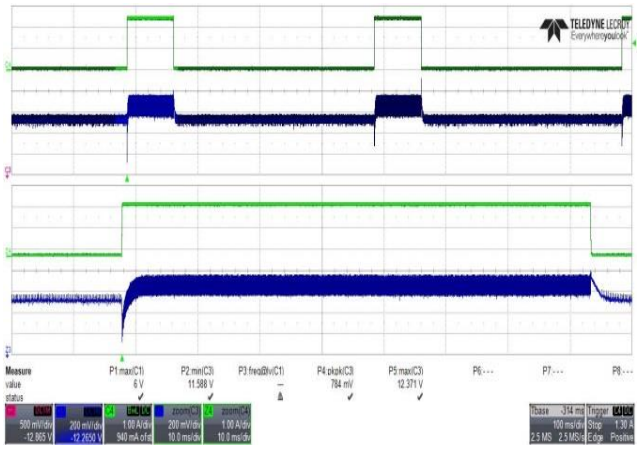

Figure 34 – Output Load Transient, 100 % to 0 % Load.
V_{IN} = 800 VDC, I_{OUT} = 2.5 A to 0 A.
$V_{OUT(MAX)}$ = 12.37 V, $V_{OUT(MIN)}$= 11.59 V.
Upper: $I_{OUT,}$ 1 A, 100 ms / div.
Lower: V_{OUT}, 200 mV, 100 ms / div.
Bottom Half: Zoom @ 10 ms / div.

9.11 *FWD Waveforms During Shorted Output*

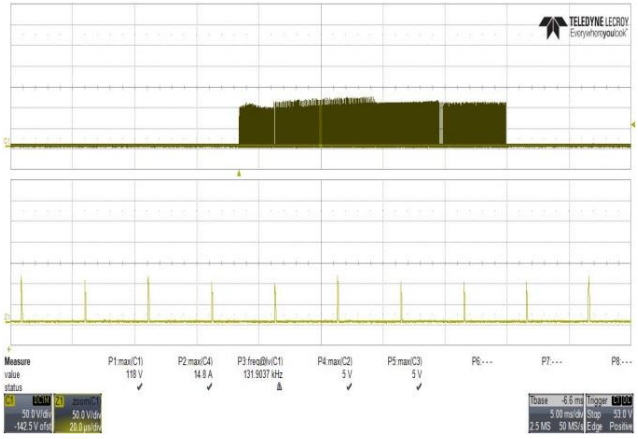

Figure 35 – FWD Voltage During Shorted Output.
V_{IN} = 800 VDC $V_{FWD(MAX)}$ = 118 V.
Top: V_{FWD}, 50 V, 5 ms / div.
Bottom: Zoom @ 20 μs / div.

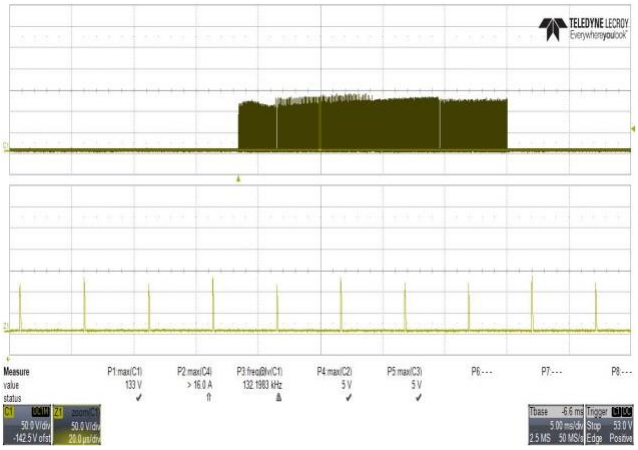

Figure 36 – FWD Voltage During Shorted Output.
V_{IN} = 921 VDC $V_{FWD(MAX)}$ = 133 V.
Top: V_{FWD}, 50 V, 5 ms / div.
Bottom: Zoom @ 20 μs / div.

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10 Thermal Performance

All measurements have been done at room ambient temperature after 1 hours of continuous operation.

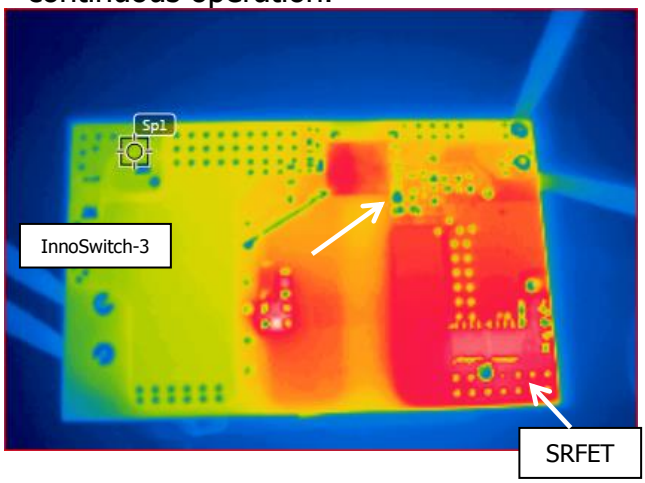

Figure 37 – 400 VDC 2.5 A Full Load.
Temperature of INN3977CQ: 65 ºC.
Temperature of SR FET: 72 ºC.
Ambient Temperature: 25 ºC.

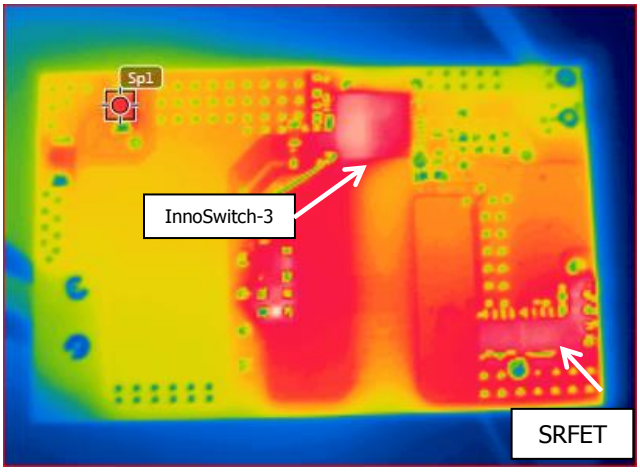

Figure 38 – 800 VDC 2.5 A Full Load.
Temperature of INN3977CQ: 102 ºC.
Temperature of SR FET: 88 ºC.
Ambient Temperature: 26 ºC.

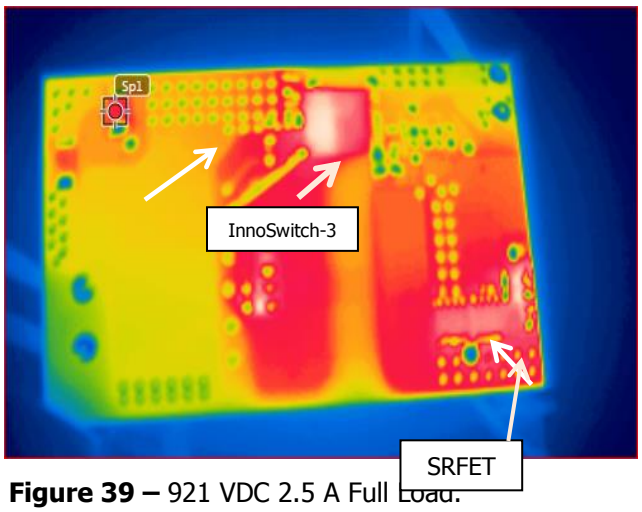

Figure 39 – 921 VDC 2.5 A Full Load.
Temperature of INN3977CQ: 113 ºC.
Temperature of SR FET: 96 ºC.
Ambient Temperature: 25 ºC.

10.1 *Temperature vs. Output Power*

400 VDC					
P_{OUT} (W)	INN3977CQ (°C)	SR FET (°C)	TVS (°C)	STACKFET (°C)	AMB (°C)
30.6	65	72	46	51	25
24.4	59	62	44	45	23
18.3	54	54	44	44	25
12.1	46	46	34	38	23
6.0	42	42	32	34	24

800 VDC					
P_{OUT} (W)	INN3977CQ (°C)	SR FET (°C)	TVS (°C)	STACKFET (°C)	AMB (°C)
30.6	102	88	79	74	26
24.3	93	76	68	67	25
18.1	82	65	61	62	24
12.1	73	53	50	58	24
6.0	63	45	46	50	24

921 VDC					
P_{OUT} (W)	INN3977CQ (°C)	SR FET (°C)	TVS (°C)	STACKFET (°C)	AMB (°C)
30.6	113	96	85	79	25
24.1	100	80	75	70	25
18.1	88	65	65	65	25
12.1	78	57	60	59	25
6.0	68	46	49	54	23

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10.2 *Maximum Output Power vs. Ambient Temperature*

(Based on 125 °C junction temperature of INN3977CQ)

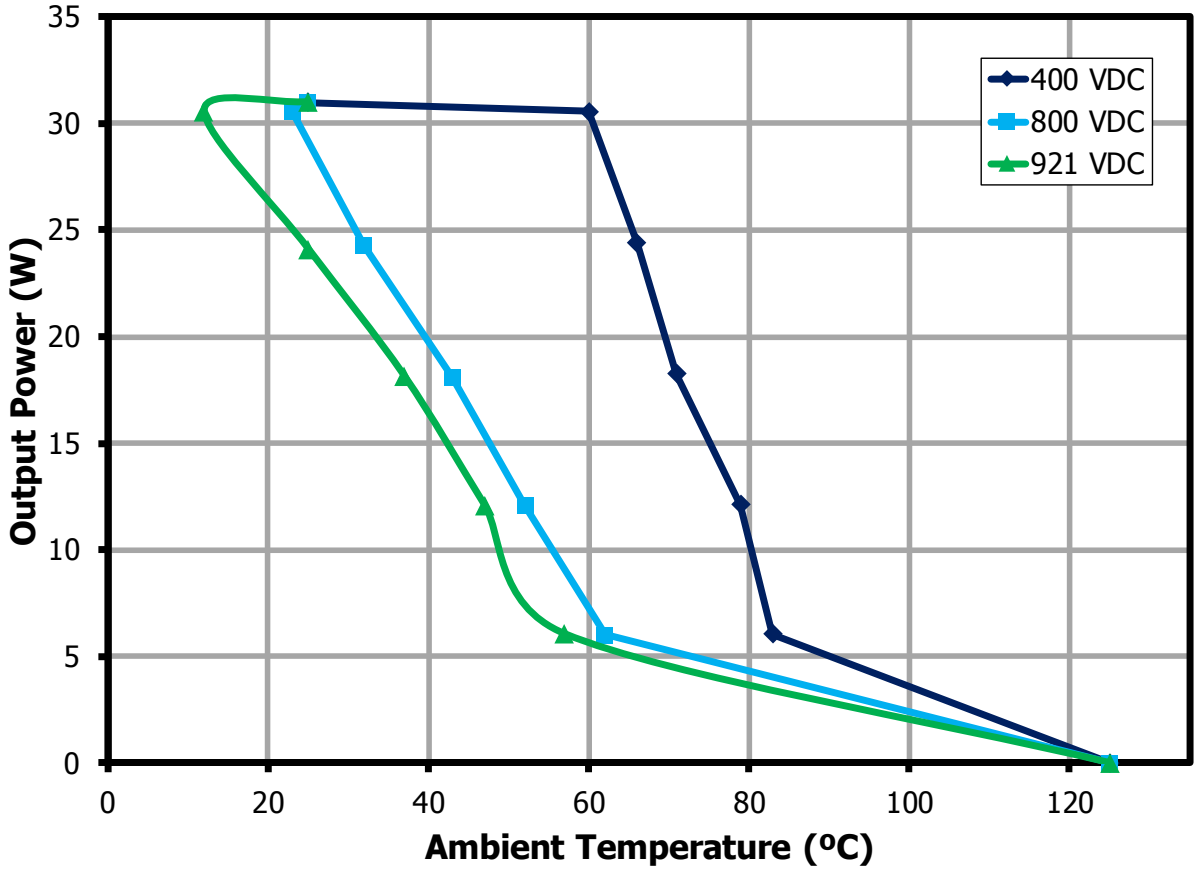

Figure 40 – Maximum Output Power vs. Ambient Temperature.

11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
04-Feb-20	DK	1.0	Initial Release	Mktg & Apps
25-Mar-20	DK	1.1	Updated Schematic, BOM and PCB with D1.	Mktg & Apps

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