

---

## Design Example Report

<b>Title</b>	<b>80 W, 28 V CV Isolated Flyback with 420 W Peak Power Using TOPSwitchGaN (TOP7078E)</b>
<b>Specification</b>	180 – 265 VAC Input; 28 V / 2.89 A <sub>NOM</sub> / 15 A <sub>PK</sub>
<b>Application</b>	Garage Door Opener
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	DER-1113
<b>Date</b>	June 06, 2026
<b>Revision</b>	A

### Summary and Features

- 80 W continuous output power
- 420 W peak power
- >92% full load efficiency at 230 VAC
- >91% average efficiency at 230 VAC
- Low component count: 78 parts
- Excellent transient load response
- Comprehensive protection:
  - Over temperature protection (OTP)
  - Line undervoltage and overvoltage protection
  - Output overvoltage protection
  - Output short-circuit protection
- Robust 800 V rated PowiGaN™ for high surge withstand
- Meets 2 kV Combination wave, and Ring wave surge test
- Class B conducted EMI with > 6 dB margin

---

#### Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.  
Tel: +1 408 414 9200 Fax: +1 408 414 9201  
[www.power.com](http://www.power.com)

**PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.power.com](http://www.power.com). Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.



## Table of Contents

1	Introduction .....	5
2	Power Supply Specification .....	7
3	Schematic .....	8
4	Circuit Description.....	9
4.1	Input Rectification and EMI Filtering .....	9
4.2	Zero Loss Automatic X-Capacitor Discharge CAPZero™-3.....	9
4.3	Flyback Converter Circuit Using TOPSwitchGaN .....	9
4.4	Secondary Feedback Circuit .....	10
5	PCB Layout.....	11
5.1	PCB Specification .....	11
6	Bill of Materials .....	13
7	Flyback Transformer Design Spreadsheet.....	15
8	Flyback Transformer (T1) Specification .....	23
8.1	Electrical Diagram .....	23
8.2	Electrical Specifications.....	23
8.3	Materials .....	24
8.4	Transformer Build Diagram .....	24
8.5	Winding Instructions .....	25
8.6	Winding Illustrations .....	26
9	Common Mode Choke (L2) Specification .....	32
9.1	Electrical Diagram .....	32
9.2	Electrical Specifications.....	32
9.3	Materials .....	32
9.4	Build Diagram.....	33
9.5	Winding Instructions .....	33
10	Common Mode Choke (L5) Specification .....	34
10.1	Electrical Diagram .....	34
10.2	Electrical Specifications.....	34
10.3	Materials .....	34
10.4	Build Diagram.....	35
10.5	Winding Instructions .....	35
11	Heatsink Assembly .....	36
11.1	TOPSwitchGaN IC Heatsink Assembly .....	36
11.2	Output Diode (D4) Heatsink Assembly .....	38
11.3	Additional TOPSwitchGaN IC Heatsink Assembly Instructions.....	40
11.4	Additional Diode Heatsink Assembly Instructions .....	40
12	Performance Data .....	41
12.1	Efficiency at Full Load .....	41
12.2	Efficiency vs. Line Voltage .....	42
12.3	Efficiency vs. Output Load .....	43
12.4	Output Voltage Regulation vs. Input Line .....	44
12.5	Output Voltage Regulation vs. Output Load.....	45



12.6	Energy Efficiency Performance .....	46
12.6.1	Average Efficiency .....	46
12.6.2	No Load Input Power Consumption.....	47
12.7	Output Ripple Voltage vs. Output Load .....	48
12.8	Thermal Performance at 60 °C Ambient.....	49
12.8.1	Thermal Test Data Summary at 60 °C Ambient.....	50
12.8.2	Component Thermal Profile at 60 °C Ambient.....	51
13	Waveforms.....	54
13.1	Output Voltage Profile at Full-Load Start-Up.....	54
13.2	Output Voltage During Step Line Transient.....	54
13.3	Output Voltage Profile During 1 s AC On/Off Cycling (Ambient = 60 °C).....	55
13.4	Output Voltage Profile During 500 ms AC On/Off Cycling (Ambient = 60 °C) .....	55
13.5	Primary Drain Voltage and Current .....	56
13.5.1	Steady State Operation.....	56
13.5.2	Step-Load Transient .....	57
13.5.3	Input Line Transient .....	57
13.5.4	Dynamic Peak Power Load Step.....	58
13.6	Flyback Output Diode Voltage Stress .....	59
13.6.1	Output Diode Voltage Stress at Steady State .....	59
13.6.2	Output Diode Voltage Stress During Start-up Full Load .....	60
13.6.3	Output Diode Voltage Stress During No Load to Full Load Transient .....	61
13.6.4	Output Diode Voltage Stress During Dynamic Peak Power Load Step.....	62
13.6.5	Start-up Operation .....	63
13.7	Output Voltage Ripple .....	64
13.7.1	Ripple Voltage Measurement Set-up .....	64
13.7.2	Output Ripple Voltage Waveforms .....	64
13.8	Brown-in /Brown-out Test.....	66
13.8.1	Brown-in /Brown-out Test.....	66
14	Conducted EMI .....	67
14.1	Test Set-up .....	67
14.2	Conducted EMI Scan .....	67
15	Line Surge Immunity.....	68
15.1	Combination Wave Differential Mode Surge.....	68
15.2	Ring Wave Surge .....	69
15.2.1	Ring Wave Differential Mode .....	69
16	Revision History .....	70

**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



## 1 Introduction

This engineering report describes a flyback converter that provides an isolated output voltage of 28 V at 80 W for a garage door opener which is also capable of delivering up to 420 W peak power. This power supply utilizes the TOP7078E from the TOPSwitchGaN™ family of ICs.

The TOPSwitchGaN IC integrates an 800 V PowiGaN switch with a multi-mode flyback controller that operates in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), enabling high efficiency across.

The power supply delivers a regulated 28 V constant voltage output with 80 W continuous power capability and up to 420 W peak power. It operates over an input voltage range of 180 VAC to 265 VAC and is optimized for high efficiency.

This document includes the power supply specifications, bill of materials (BOM), transformer construction information, circuit schematic, and printed circuit board (PCB) layout, along with performance data and electrical waveforms.



**Figure 1** – Oblique View.



## 2 Power Supply Specification

The table represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	$V_{IN}$	180	230	265	VAC	2 wire – no P.E.
Frequency	$f_{LINE}$	47	50/60	63	Hz	
<b>Charger Output</b>						
Output Voltage	$V_{OUT}$		28		V	±3%
Output Current	$I_{OUT}$		2.8		A	For 5 seconds
Peak Output Current	$I_{OUT, pk}$		15		A	
Output Power	$P_{OUT}$		80		W	For 5 seconds 25 °C Ambient, 20 MHz BW
Peak Output Power	$P_{OUT, pk}$		420		W	
Output Ripple Voltage (CV)	$V_{Ripple}$			100	mVpp	
<b>Efficiency</b>						
Full Load	$\eta_{FL}$	92			%	230 VAC
Average Efficiency	$\eta_{AVE}$	91			%	230 VAC
No Load Input Power	$P_{NL}$			250	mW	230 VAC
<b>Immunity</b>						
Conducted EMI		CISPR22B / EN55022B				Fixed Resistive Load (floating) Source impedance: 2 $\Omega$ Source impedance: 12 $\Omega$
Combination Wave Surge (L/N)				±2	kV	
Ring Wave				±2	kV	
Operating Ambient Temperature	$T_{AMB}$	0		60	°C	Free convection, sea level

**Table 1** – Power Supply Specification.

### 3 Schematic

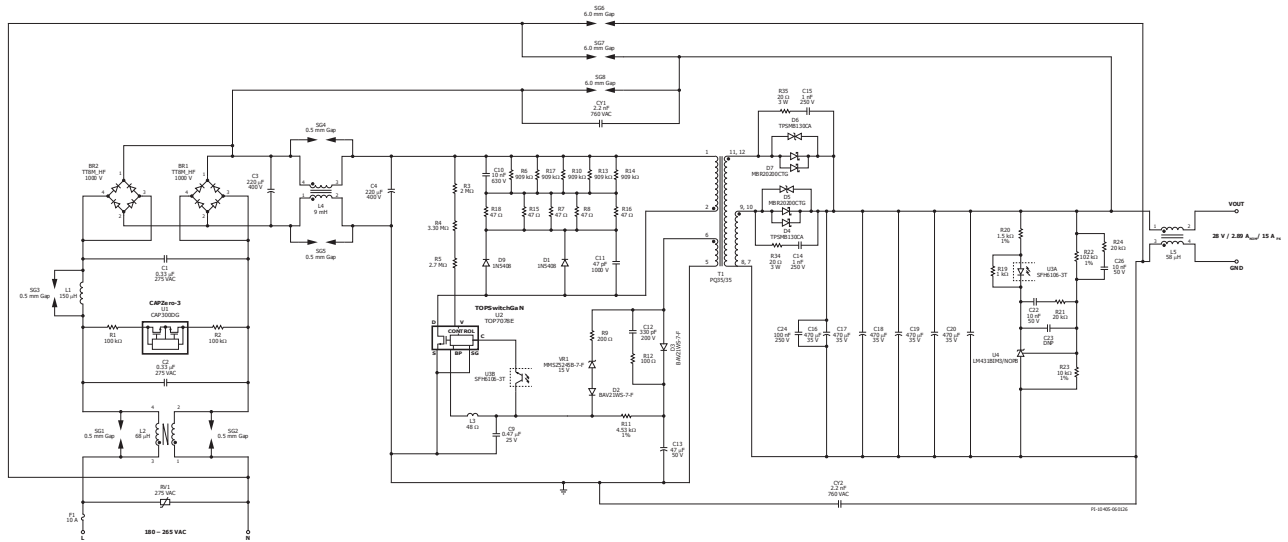


Figure 4 – Schematic Diagram.

## 4 Circuit Description

### 4.1 Input Rectification and EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure. RV1 protects the circuit against high-voltage line surges. The NTC thermistor RT1 limits inrush current during start-up. X-capacitors C1 and C2, together with the common-mode choke (CMC) L2 forms an  $\pi$ -filter that attenuates both common-mode and differential-mode noise in the >5 MHz region of the conducted EMI spectrum. Differential inductor L1 suppresses differential-mode noise within the same spectrum. Bridge rectifier BR1 provides full-wave AC rectification. Capacitors C3 and C4, along with inductor L4, form a  $\pi$ -filter that reduces the flyback converter's DC-bus ripple voltage and attenuates both differential-mode and common-mode noise generated by switching. The TOPSwitchGaN frequency-jitter feature further reduces conducted EMI.

### 4.2 Zero Loss Automatic X-Capacitor Discharge CAPZero™-3

To satisfy the Safety Extra-Low Voltage (SELV) requirements the AC supply is disconnected, the CAP300DG (U1) automatically discharges the X capacitors C2 and C1 to a safe (SELV) level by connecting discharge resistors R1 and R2. When AC voltage is applied, the CAP300DG (U1) blocks current flow in the X capacitor safety discharge resistors, reducing power loss.

### 4.3 Flyback Converter Circuit Using TOPSwitchGaN

Line undervoltage and overvoltage thresholds are determined by the current supplied from resistors R3, R4, and R5 to the V pin, while the primary RCD snubber, composed of D1, D9, R18, R15, R7, R8, R16, R6, R17, R10, R13, R14, and C10, minimizes primary side voltage spikes caused by the transformer's leakage inductance; additionally, a small ceramic capacitor C11 is placed across snubber diodes D1 and D9 to reduce high frequency ringing that would otherwise contribute to radiated EMI.

The TOPSwitchGaN IC (U2) is self-powered at start-up through an internal high-voltage current source connected to the DRAIN (D), which supplies current to the internal primary bypass regulator to charge the BYPASS pin capacitor (C9) when AC input is first applied. A ferrite bead (L3) is added to improve noise immunity from ring wave, EFT and ESD. During normal operation, the controller is powered from the bias winding of transformer T1. The bias winding output is rectified by diode D3 and filtered by C13. Resistor R11 limits the current supplied to the BYPASS pin of the TOPSwitchGaN IC (U2), disabling the internal high-voltage current source once sufficient bias voltage is reached.

Primary-side sensed overvoltage protection (OVP) is implemented using Zener diode VR1, current-limiting resistor R9, and blocking diode D2 connected from the bias winding to the BYPASS pin. If an output overvoltage occurs, the increased bias winding voltage causes VR1 to conduct, injecting additional current into the BYPASS pin. When this current exceeds the



shutdown threshold ( $I_{SD}$ ), the TOPSwitchGaN IC stops switching and enters auto-restart mode. Auto-restart will continue until the output voltage returns to within regulation.

When the primary switch is off (flyback phase), output rectifier diodes D7 and D5 conduct transformer flyback current from the secondary winding, delivering energy to the output. Output capacitors C16, C17, C18, C19, C20, and C24 filter the rectified waveform to produce a stable DC output voltage.

The snubber networks, composed of C15, R35, and D6 (TVS), and C14, R34, and D5 (TVS), limit the voltage stress across diodes D7 and D5, respectively, while also suppressing high frequency ringing and improving both conducted and radiated EMI performance.

#### 4.4 Secondary Feedback Circuit

Optocoupler U3 provides the isolated feedback path that delivers the regulation signal to the primary-side controller in the TOPSwitchGaN IC. Current flowing through the U3A optocoupler is limited by resistor R20, which protects the diode.

Constant-voltage regulation is controlled by the 2.5V precision shunt regulator, U4, which monitors the output voltage through the divider formed by R22 and R23. When the voltage at the reference pin reaches 2.5V, U4 sinks current, driving the U3A optocoupler LED and sending the regulation signal to the primary-side control IC.

The RC compensation network, R21 and C22, stabilizes the feedback loop by limiting the TL431 (U4) high-frequency gain, improving phase margin, and slowing the output start-up ramp. This compensation also prevents oscillation that would otherwise increase output-voltage ripple and degrade transient load response.

A phase-boost RC network (R24, C26) connected across the upper divider resistor, R22, provides phase advancement to improve transient response. This network also slows the output-voltage rise at full load, ensuring that the primary switch has sufficient time to deliver full power during start-up.

Resistor R19, connected across optocoupler U3A, slows the optocoupler LED turn-on during startup, allowing additional time for the feedback loop to stabilize before regulation begins.

## 5 PCB Layout

### 5.1 PCB Specification

- Layer: 2
- Board Thickness: 1.6 mm.
- Copper Thickness: 2 oz.
- Surface finish: LF HASL
- Material: FR-4
- Solder Mask: Green
- Silkscreen: White

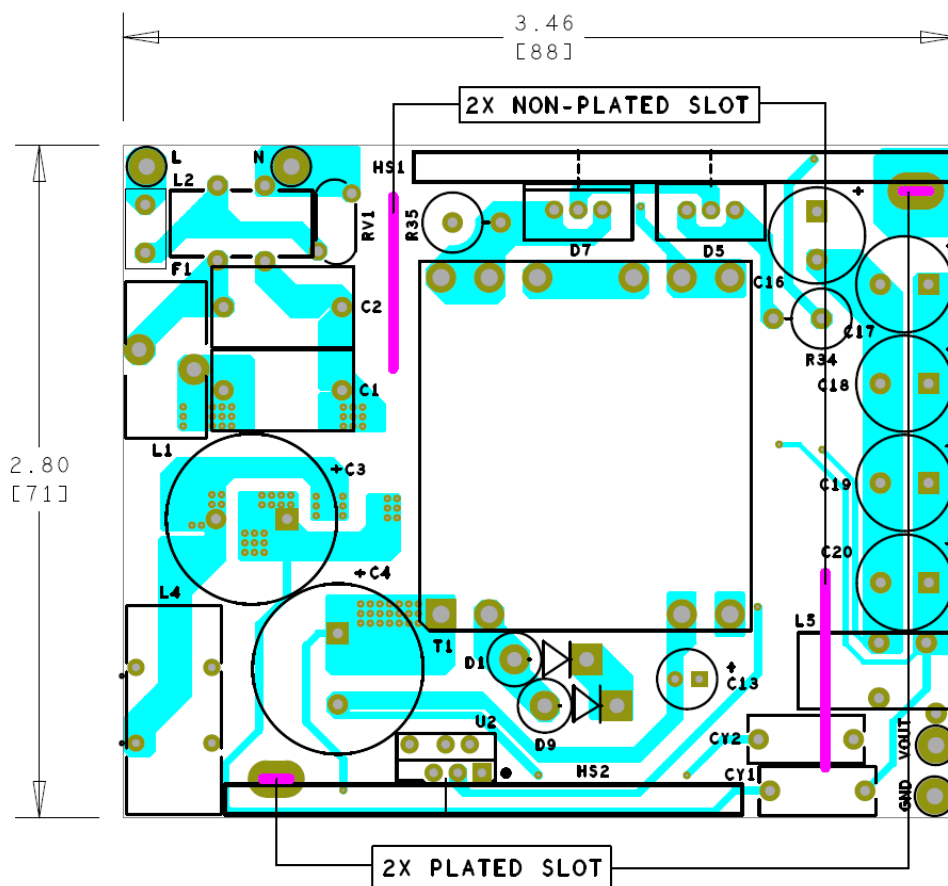


Figure 5 – Printed Circuit Layout, Top.

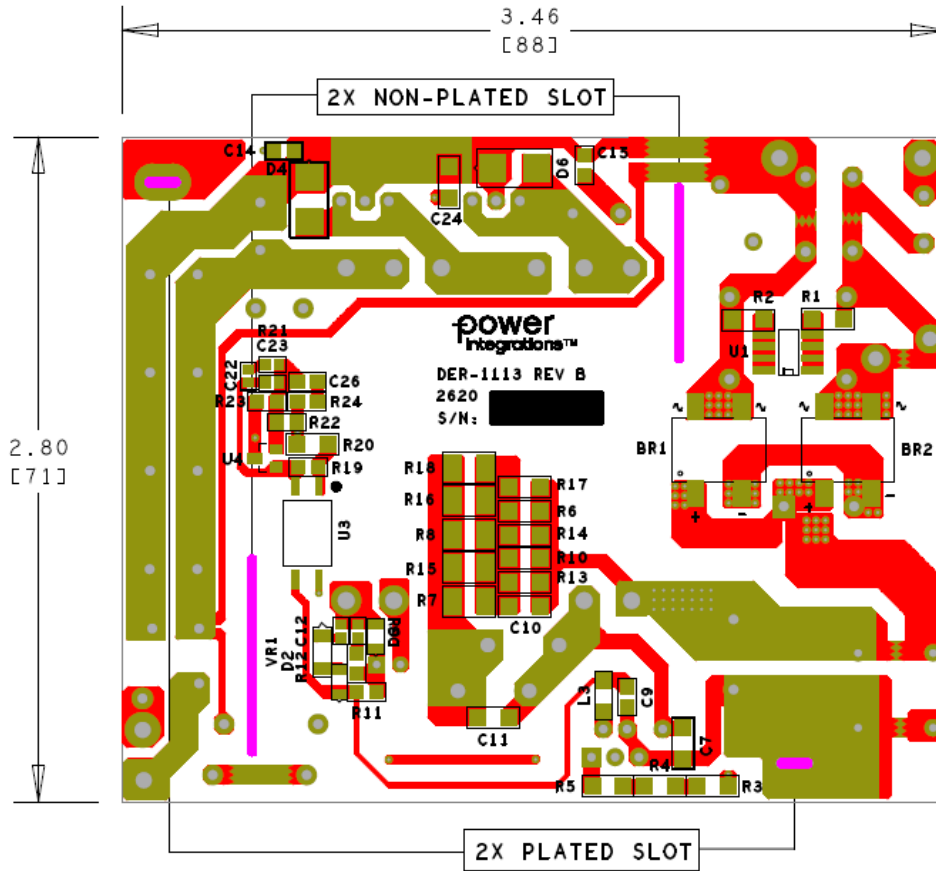


Figure 6 – Printed Circuit Layout, Bottom.

## 6 Bill of Materials

Item	Ref Des.	Qty.	Description	Manufacturer	Mfr. Part Number
1	BR1 BR2	2	Bridge Rectifier, Single Phase Standard, 1 kV, 8 A, Surface Mount TT	Diodes Incorporated	TT8M_HF
2	C1 C2	2	0.33 $\mu$ F, Film Capacitor, 275 V, Polypropylene (PP), Metallized Radial, X2, 15.00 mm x 8.50 mm	Würth Electronics Inc.	890324024003
3	C3 C4	2	220 $\mu$ F, 400 V, Electrolytic, General Purpose, (18 x 40)	Rubycon	400HXW220MEFR18X40
4	C11	1	47 pF, 1000 V, Ceramic, NP0, 1206	Kemet	C1206C470JDGACTU
5	C9	1	0.47 $\mu$ F, $\pm$ 10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	TDK Corporation	CGA4J2X7R1E474K125AA
6	C10	1	10 nF, 630 V, Ceramic, X7R, 1206	Kemet	C1206C103KBRACU
7	C12	1	330 pF, $\pm$ 5%, 200 V, Ceramic Capacitor, COG, NP0, 0603 (1608 Metric)	TDK Corp	CGJ3E3COG2D331J080AA
8	C13	1	47 $\mu$ F, 50 V, Electrolytic, General Purpose, (6.3 x 11)	United Chemi-Con	EKMG500ELL470MF11D
9	C14 C15	2	1 nF, 250 V, Ceramic, X7R, 0805	Murata	GRM21AR72E102KW01D
10	C16-C20	5	470 $\mu$ F, 35 V, Electrolytic, Very Low ESR, 23 mOhm, (10 x 20)	Nippon Chemi-Con	EKZE350ELL471MJ20S
11	C22	1	10 nF, 50 V, Ceramic, X7R, 0603	Kemet	C0603C103K5RACTU
12	C23	1	1000 pF, $\pm$ 10%, 100 V, Ceramic, X7R, 0603	Kemet	C0603C102K1RACTU
13	C24	1	100 nF, 250 V, Ceramic, X7R, 1206	TDK Corp	C3216X7R2E104M
14	C26	1	10 nF, 50 V, Ceramic, X7R, 0805	Kemet	C0805X103K5RAC7210
15	CY1 CY2	2	CAP, Ceramic Disc, 2.2 nF, $\pm$ 20%, 760 VAC (X1), 500 VAC (Y1), Y5U (E), -40°C ~ 125°C, X1, Y1, Safety	Vishay/ BC Components	VY1222M47Y5UQ63V0
16	D1 D9	2	Diode, 1000 V, 3 A, Through Hole, DO-201, DO-201AA, DO-27, Axial	Diotec Semiconductor	1N5408
17	D2 D3	2	200 V, 200 mA, Fast Switching, 50 ns, SOD-323	Diode Inc.	BAV21WS-7-F
18	D4 D6	2	Diode, TVS, 179 V Clamp, 3.4 A Ipp, TVS Diode, Automotive, AEC-Q101, Surface Mount, DO-214AA (SMBJ), (SMB)	Littelfuse Inc	TPSMB130CA
19	D5 D7	2	200 V, 20 A, Dual Schottky, TO-220AB	ON Semiconductor	MBR20200CTG
20	F1	1	10 A, 300 VAC, Fuse, Board Mount, Through Hole, MST, 8.35 x 4.30 x 7.7 mm	Conquer	MST 10A 300V
21	L1	1	150 $\mu$ H, 20%, 2.5 A, Rdc = 0.01, Inductor, Toroid, High Amp, Vertical, 16.5 mm Diam, 8.5 mm Thick, 8.5 mm LS	Würth Elect Inc	7447018
22	L2	1	CMC, 68 $\mu$ H @ 100 kHz, Toroidal, wound on Mfg P/N: 5943000321 (Green Color) toroidal core, using 10 turns #23 AWG wire per side	Power Integrations	32-00489-00
23	L3	1	Ferrite Bead, 48 $\Omega$ @ 100 MHz, 1 Power Line, 6 A, 5 mOhm, 1206 (3216 Metric)	Würth Elektronik	782763480
24	L4	1	9 mH, 2 A, Common Mode Choke	Fontaine Technologies	T18107V-902S P.I. Custom
25	L5	1	CMC, 58 $\mu$ H @ 100 kHz, Toroidal, wound on Mfg P/N: 5943000321 (Green Color) toroidal core, using 9 turns #21 AWG wire per side	Power Integrations	32-00490-00
26	R1 R2	2	RES, 100 k, 5%, 2/3 W, Thick Film, 1206	Panasonic	ERJ-P08J104V
27	R3	1	RES, 2 M, 1%, 1/4 W, Moisture Resistant, Thick Film, 1206 (3216 Metric)	Yageo	AC1206FR-072ML
28	R4	1	RES, 3.30 M, 1%, 1/4 W, Thick Film, 1206	Rohm Semiconductor	KTR18EZPF3304
29	R5	1	RES, 2.7 M, 5%, 1/4 W, Thick Film, 1206	YAGEO	RC1206FR-072M7L
30	R6 R10 R13 R14 R17	5	RES, 909 k, 1%, 1/4 W, Thick Film, 1206	Panasonic	ERJ-8ENF9093V
31	R7 R8 R15 R16 R18	5	RES, 47 Ohm, $\pm$ 5%, 0.75 W, 1210 (3225 Metric), Pulse Withstanding, Thick Film	Vishay Dale	CRCW121047R0JNEAHP



32	R9	1	RES, 200 $\Omega$ , 1%, 1/10 W, Thick Film, 0603	Panasonic	ERJ-3EKF2000V
33	R11	1	RES, 4.53 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF4531V
34	R12	1	RES, 100 $\Omega$ , $\pm$ 1%, 0.125 W, 1/8 W, Chip Resistor, 0805 (2012 Metric), Thick Film	Stackpole Electronics Inc	RMCF0805FT100R
35	R19	1	RES, 1 k, 5%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6GEYJ102V
36	R20	1	RES, 1.5 k, 1%, 1/4 W, Thick Film, 1206	Panasonic	ERJ-8ENF1501V
37	R21	1	RES, 20 k, 5%, 1/10 W, Thick Film, 0603	Panasonic	ERJ-3GEYJ203V
38	R22	1	RES, 102 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF1023V
39	R23	1	RES, 10.0 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF1002V
40	R24	1	RES, 20 k, 5%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6GEYJ203V
41	R34 R35	2	RES, 20 Ohms, $\pm$ 5%, 3 W, Through Hole Resistor, Axial, Flame Retardant Coating, Pulse Withstanding, Safety Metal Film	TE Connectivity Passive Product	RR03J20RTB
42	RV1	1	275 VAC, 23 J, 7 mm, Radial	Littelfuse	V275LA4P
43	T1	1	Bobbin, PQ35/35, Vertical, 12 pins	TDK	B65882B0012T001
44	U1	1	CAPZero-3, CAP300DG, SO-8C	Power Integrations	CAP300DG
45	U2	1	TOPSwitch-GaN, TOP7078E, eSIP-7C	Power Integrations	TOP7078E
46	U3	1	Optoisolator, Transistor Output, 5300 Vrms, 1 Channel, 4-SMD, Gull Wing	Vishay Semiconductor Opto Division	SFH6106-3T
47	U4	1	IC, REG Zener Shunt Adj, SOT-23	National Semiconductor	LM431BIM3/NOPB
48	VR1	1	Diode Zener, 15 V, 500 mW, SOD-123	Diodes, Inc	MMSZ5245B-7-F

Table 2 – Electrical Parts.

Item No.	Part Reference	Qty.	Description	Manufacturer	Mfr. Part Number
1	VOUT	1	Test Point, RED, THRU-HOLE MOUNT	Keystone	5010
2	GND L	2	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
3	N	1	Test Point, WHT, THRU-HOLE MOUNT	Keystone	5012
4	HS1	1	SHTM, Heatsink for Diodes, DER1113_RevA, Composition: AL, 3003, 0.125" thick	Custom	61-00427-00
5	HS2	1	SHTM, Heatsink for TopSwitch, DER1113_RevA, Composition: AL, 3003, 0.125" thick	Custom	61-00428-00

Table 3 – Miscellaneous Parts.



## 7 Flyback Transformer Design Spreadsheet

1	ACDC_TOPSwitchGaN_Flyback_051 426; Rev.1.0; Copyright Power Integrations 2026	INPUT	INFO	OUTPUT	UNITS	TOPSwitchGaN Single/Multi Output Flyback Design Spreadsheet
2	<b>APPLICATION VARIABLES</b>					<b>Design Title</b>
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	180		180	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			230VAC (±30%)		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	440.0		440.0	uF	Input capacitor
9	VOUT	28.00		28.00	V	Output voltage at the board
10	IOUT	15.000		15.000	A	Output current
11	POUT		Info	420.00	W	The specified output power exceeds the device power capability: Verify thermal performance if no other warnings
12	EFFICIENCY	0.89		0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.60		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
18	<b>PRIMARY CONTROLLER SELECTION</b>					
19	PACKAGE_DEVICE	eSIP		eSIP		Device Package
20	ILIMIT_MODE			STANDARD		Device current limit mode
21	DEVICE_GENERIC	TOP7078		TOP7078		Generic device code
22	DEVICE_CODE			TOP7078E		Actual device code
23	POUT_MAX		Warning	400	W	Power output desired is more than the power capability of device. Please select a different device or reduce power output desired.
24	RDSON_100DEG			0.46	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			7.900	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			8.500	A	Typical current limit of the primary switch
27	ILIMIT_MAX			9.100	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			800	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.93	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW		Warning	653.4	V	The peak repetitive drain voltage on the switch is higher than 650V: Decrease the device VOR
34	<b>WORST CASE ELECTRICAL PARAMETERS</b>					



35	FSWITCHING_MAX	131500	Info	131500	Hz	The operating frequency is close to the maximum allowable switching frequency. FALSE
36	VOR	120.0		120.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			224.47	V	Valley of the minimum input AC voltage at full load
38	KP			0.56		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.349		Primary switch duty cycle
41	TIME_ON_MAX			5.31	us	Primary switch on-time
42	TIME_ON_AT_FSWITCHING_MAX			2.66	us	Primary switch on-time at FSWITCHING_MAX
43	TIME_OFF			4.95	us	Primary switch off-time at 180 VAC, 420 W, and 131500 Hz.
44	LPRIMARY_MIN			128.8	uH	Minimum primary inductance
45	LPRIMARY_TYP			135.5	uH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			142.3	uH	Maximum primary inductance
49	PRIMARY CURRENT					
50	IPEAK_PRIMARY			9.038	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			3.519	A	Primary switch current pedestal
52	IAVG_PRIMARY			2.018	A	Primary switch average current
53	IRIPPLE_PRIMARY			6.520	A	Primary switch ripple current
54	IRMS_PRIMARY			3.591	A	Primary switch RMS current
56	SECONDARY CURRENT					
57	IPEAK_SECONDARY			37.958	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			14.781	A	Secondary winding current pedestal
59	IRMS_SECONDARY			20.587	A	Secondary winding RMS current
<b>63</b>	<b>TRANSFORMER CONSTRUCTION PARAMETERS</b>					
64	CORE SELECTION					
65	CORE	PQ35		PQ35		Core selection. Refer to the Magnetics Designer tab to see the detailed report
66	CORE CODE			PQ35/35-3C95		Core code
67	AE			190.00	mm <sup>2</sup>	Core cross sectional area
68	LE			86.10	mm	Core magnetic path length
69	AL			6600	nH/turn <sup>2</sup>	Ungapped core effective inductance
70	VE			16300.0	mm <sup>3</sup>	Core volume
71	BOBBIN			CPV-PQ35/35-1S-12P-Z		Bobbin
72	AW			146.64	mm <sup>2</sup>	Window area of the bobbin



73	BW			20.80	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
<b>76</b>	<b>PRIMARY WINDING</b>					
77	NPRIMARY			21	turns	Primary turns
78	BPEAK			3350	Gauss	Peak flux density
79	BMAX		Warning	3197	Gauss	The maximum flux density of the core has exceeded the recommended limit for maximum flux density (3000 Gauss): Increase the number of secondary turns
80	BAC			1136	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			307	nH/turns <sup>2</sup>	Typical gapped core effective inductance
82	LG			0.741	mm	Core gap length
<b>84</b>	<b>PRIMARY BIAS WINDING</b>					
85	NBIAS_PRIMARY			3	turns	Primary bias winding number of turns
<b>87</b>	<b>SECONDARY WINDING</b>					
88	NSECONDARY	5		5	turns	Secondary winding number of turns
<b>90</b>	<b>SECONDARY BIAS WINDING</b>					
91	NBIAS_SECONDARY			NA	turns	Secondary bias winding number of turns
<b>95</b>	<b>PRIMARY COMPONENTS SELECTION</b>					
96	LINE UNDERVOLTAGE					
97	BROWN-IN REQUIRED			140.40	V	Required AC RMS/DC line voltage brown-in threshold
98	RLS			14.64	MΩ	Connect two 7.32 MΩ resistors to the V-pin for the required UV/OV threshold
99	BROWN-IN ACTUAL			114.8V - 142.2V	V	Actual AC RMS/DC brown-in range
100	BROWN-OUT ACTUAL			97.4V - 122.3V	V	Actual AC RMS/DC brown-out range
101						
102	LINE OVERVOLTAGE					
103	OVERVOLTAGE_LINE		Warning	548.3V - 615.8V	V	The device voltage stress will be higher than 800V when overvoltage is triggered
104						
105	PRIMARY BIAS DIODE					
106	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
107	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE_PRIMARY			70.14	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
110	CBP			0.47	uF	BP pin capacitor
<b>114</b>	<b>SECONDARY COMPONENTS</b>					



115	VREF_REG			1.25	V	Reference voltage of the feedback
116	RFB_UPPER			215.00	k $\Omega$	Upper feedback resistor (connected to the first output voltage)
117	RFB_LOWER			10.00	k $\Omega$	Lower feedback resistor
<b>119</b>	<b>SECONDARY BIAS</b>					
120	USE_SECONDARY_BIAS	AUTO		NO		Use secondary bias winding for the design
121	SEC_BIAS_FORWARD	NO		NA		Secondary bias in-phase with primary. A Linear voltage regulator is connected after the secondary bias rectification capacitor. Select "YES" to enable this configuration
122	VZ_LINEAR_REGULATOR			NA	V	Zener voltage for linear regulator. Only applicable if SEC_BIAS_FORWARD is enabled.
123	VBIAS_SECONDARY_TARGET			NA	V	Target secondary bias rectified voltage (Affects Secondary Bias turns value)
124	VBIAS_SECONDARY_ACTUAL			NA	V	Secondary bias rectified voltage (Calculated using actual secondary bias winding turns).
125	OUTPUT_VBIAS_SECONDARY			NA	V	Secondary bias output voltage
126	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
127	VREVERSE_BIASDIODE_SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
128	CBIAS_SECONDARY			NA	$\mu$ F	Bias winding rectification capacitor
<b>131</b>	<b>MULTIPLE OUTPUT PARAMETERS</b>					
132	OUTPUT 1					
133	VOUT1			28.00	V	Output 1 voltage
134	IOUT1			15.00	A	Output 1 current
135	POUT1			420.00	W	Output 1 power
136	VD1			0.70	V	Forward voltage drop of diode for output 1
137	NS1			5	turns	Number of turns for output 1
138	ISPEAK1			37.96	A	Instantaneous peak value of the secondary current for output 1
139	ISRMS1			20.587	A	Root-mean-squared value of the secondary current for output 1
140	ISRIPPLE1			14.101	A	Current ripple on the secondary waveform for output 1
141	PIV1_CALCULATED			140.01	V	Computed peak inverse voltage stress on the diode for output 1
142	OUTPUT_RECTIFIER1	MBR20200C TG		MBR20200C TG		Selected diode for output 1
143	PIV1_RATING			200.00	V	Peak inverse voltage rating on the diode for output 1



144	TRR1			0.00	ns	Reverse recovery time of the diode for output 1
145	IFM1		Warning	10.00	A	The maximum continuous forward current rating of the diode for output 1 should be at least twice the output 1 current. Select a diode with higher forward current rating
146	PLOSS_DIODE1			7.34	W	Maximum diode power loss for output 1
148	OUTPUT 2					
149	VOUT2			0.00	V	Output 2 voltage
150	IOUT2			0.000	A	Output 2 current
151	POUT2			0.00	W	Output 2 power
152	VD2			N/A	V	Forward voltage drop of diode for output 2
153	NS2			N/A	turns	Number of turns for output 2
154	ISPEAK2			N/A	A	Instantaneous peak value of the secondary current for output 2
155	ISRMS2			N/A	A	Root mean squared value of the secondary current for output 2
156	ISRIPPLE2			N/A	A	Current ripple on the secondary waveform for output 2
157	PIV2			N/A	V	Computed peak inverse voltage stress on the diode for output 2
158	OUTPUT_RECTIFIER2	AUTO		N/A		Recommended diode for output 2.
159	PIV2_RATING			N/A	V	Peak inverse voltage rating on the diode for output 2
160	TRR2			N/A	ns	Reverse recovery time of the diode for output 2
161	IFM2			N/A	A	Maximum forward continuous current of the diode for output 2
162	PLOSS_DIODE2			N/A	W	Maximum diode power loss for output 2
164	OUTPUT 3					
165	VOUT3			0.00	V	Output 3 voltage
166	IOUT3			0.000	A	Output 3 current
167	POUT3			0.00	W	Output 3 power
168	VD3			N/A	V	Forward voltage drop of diode for output 3
169	NS3			N/A	turns	Number of turns for output 3
170	ISPEAK3			N/A	A	Instantaneous peak value of the secondary current for output 3
171	ISRMS3			N/A	A	Root mean squared value of the secondary current for output 3
172	ISRIPPLE3			N/A	A	Current ripple on the secondary waveform for output 3



173	PIV3			N/A	V	Computed peak inverse voltage stress on the diode for output 3
174	OUTPUT_RECTIFIER3	AUTO		N/A		Recommended diode for output 3.
175	PIV3_RATING			N/A	V	Peak inverse voltage rating on the diode for output 3
176	TRR3			N/A	ns	Reverse recovery time of the diode for output 3
177	IFM3			N/A	A	Maximum forward continuous current of the diode for output 3
178	PLOSS_DIODE3			N/A	W	Maximum diode power loss for output 3
180	PO_TOTAL			420.00	W	Total power of all outputs
181	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number, e.g. If VO2 is negative output, select 2
<b>185</b>	<b>DESIGN EVALUATION - COMPENSATION AND STABILITY ANALYSIS</b>					
186	COMPONENT SELECTION					
187	COUT			4950.0	uF	Output capacitor
188	RESR_COUT			0.64	mΩ	ESR of output capacitor
189						
190	SHUNT REGULATOR NETWORK					
191	VREF_REG			1.25	V	Reference voltage of the feedback. To change this parameter, go to "SECONDARY COMPONENTS" section
192	IKA_MIN			0.10	mA	Minimum cathode current required on the shunt regulator. Use datasheet value
193	R_COMP			20.00	kΩ	Resistor connected from shunt regulator cathode to RFB_LOWER; in series with C_COMP
194	C_COMP			5.60	nF	Capacitor connected from shunt regulator cathode to RFB_LOWER; in series with R_COMP
198	FEEDBACK NETWORK					
199	RFB_LOWER			10.00	kΩ	Lower feedback resistor
200	RFB_UPPER			215.00	kΩ	Upper feedback resistor
201	USE_RC_RFB_UPPER	AUTO		YES		Select "YES" to use series resistor-capacitor network across RFB_UPPER
202	RRFB_UPPER			20.00	kΩ	Resistor across RFB_UPPER; in series with CRFB_UPPER
203	CRFB_UPPER			10.00	nF	Capacitor across RFB_UPPER; in series with RRFB_UPPER
205	OPTOCOUPLER NETWORK					
206	RREF_BIAS			5.00	kΩ	Resistor across optocoupler LED



207	C_OPTO			13.0	pF	Parasitic capacitance of the optocoupler primary side. Use datasheet value
208	VF_LED			1.25	V	LED maximum forward voltage. Use datasheet value
211	RLED_COMP			470.0	$\Omega$	LED resistor. Resistor connected from VOUT to optocoupler
216	OPERATING CONDITIONS (PIXIs Charts)					
217	USER_VIN			230	V	Input voltage corner to be evaluated in the Bode plot in PIXIs Charts tab
218	POUT			420.00	W	Output power to be evaluated
219	OUTPUT RIPPLE			2.00	%	Estimated output voltage percentage ripple seen by the compensation network. Decrease to add DC offset to the Bode Magnitude Plot and vice-versa
220	EFFICIENCY			0.89		ACDC efficiency estimate to be evaluated
221	Z FACTOR			0.60		Z-factor to be evaluated
222	FSWITCHING			97984	Hz	Maximum switching frequency at the output power to be evaluated
223	KP			0.76		Measure of continuous/discontinuous mode of operation
224	MODE_OPERATION			CCM		Mode of operation
225	DUTYCYCLE			0.284		Primary switch duty cycle
226	TIME_ON			2.90	us	Primary switch on-time
227	TIME_OFF			7.31	us	Primary switch off-time
229	BODE STABILITY PARAMETERS (PIXIs Charts)					
230	F_CO			3646	Hz	Crossover frequency
231	DC GAIN			51.0	dB	DC gain
232	PHASE_MARGIN			80.9	degrees	Phase margin
233	GAIN_MARGIN			26.6	dB	Gain margin
235	INPUT VOLTAGE CORNER ANALYSIS - BODE PARAMETER RANGE					
236	VIN_1			230	V	Input voltage 1 to be evaluated in determining the range of Bode stability parameters (nominal voltage, by default)
237	VIN_2			230	V	Input voltage 2 to be evaluated in determining the range of Bode stability parameters (nominal voltage, by default)
238	F_CO_RANGE			3646 - 3646	Hz	Range of crossover frequency across the input voltage range defined
239	DC_GAIN_RANGE			51 - 51	dB	Range of DC gain across the input voltage range defined
240	PHASE_MARGIN_RANGE			80.9 - 80.9	degrees	Range of phase margin across the input voltage range defined



---

241	GAIN_MARGIN_RANGE			26.6 - 26.6	dB	Range of gain margin across the input voltage range defined
243	Note: Bode plot estimates shown in the tool can be used as starting point. Actual results may vary. Power supply designed using the tool should be tested to verify actual parameter values.					

**Table 4** – TOPSwitchGaN Flyback Transformer Design Spreadsheet.

## 8 Flyback Transformer (T1) Specification

### 8.1 Electrical Diagram

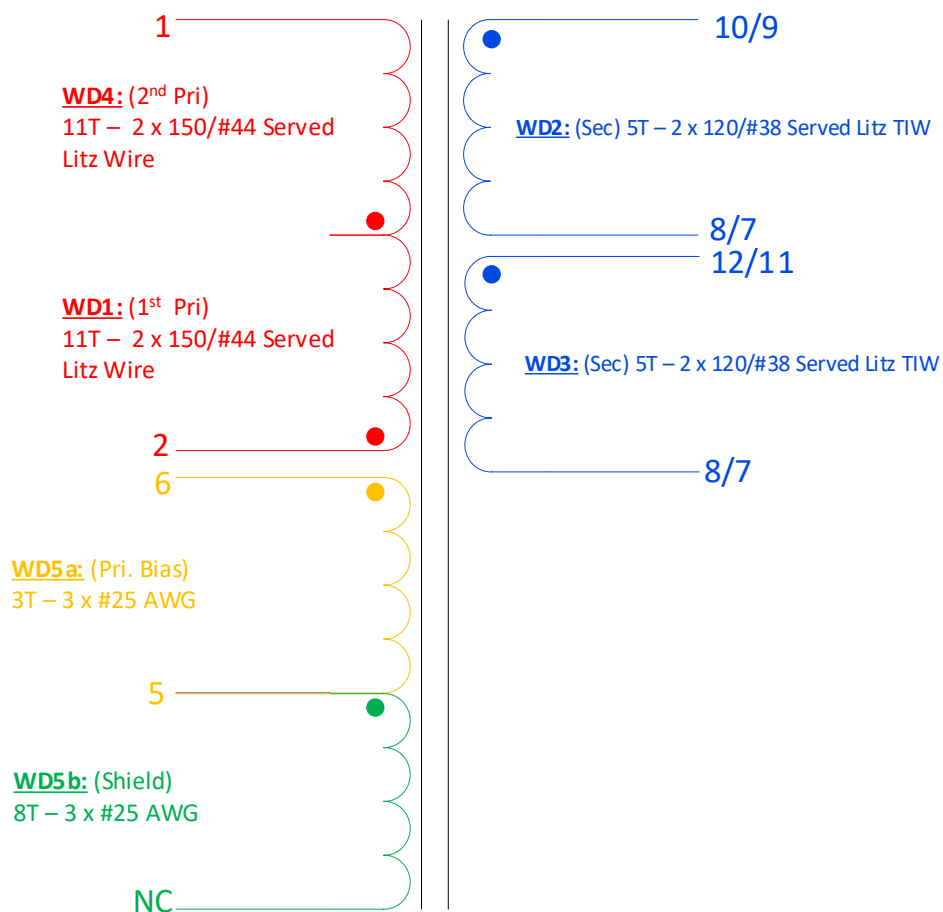


Figure 7 – Transformer Electrical Diagram.

### 8.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 2 to pin 1, with all other windings open.	135.5 $\mu$ H +/-5.0%
Maximum Primary Leakage	Measured between Pin 2 to Pin 1, with all other windings shorted.	<2.2 $\mu$ H

Table 5 – Transformer Electrical Specification.

### 8.3 Materials

Item	Description
[1]	Core: PQ35, 3C95, gapped for ALG of 323 nH / T <sup>2</sup>
[2]	Bobbin: PQ35/35-Vert-12pins (6/6); TDK, PI#: 25-01223-00; or equivalent.
[3]	Magnet wire: #25 AWG, double coated.
[4]	Magnet wire: 150/#44 Served Litz Wire.
[5]	Magnet wire: 120/#38 Served Litz Wire TIW.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 12.0 mm width.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 22.0 mm width.
[8]	Copper foil: 2 mil thick, 12m wide.
[9]	Varnish: Dolph BC-359.
[10]	Bus wire

Table 6 – Transformer Materials List.

### 8.4 Transformer Build Diagram

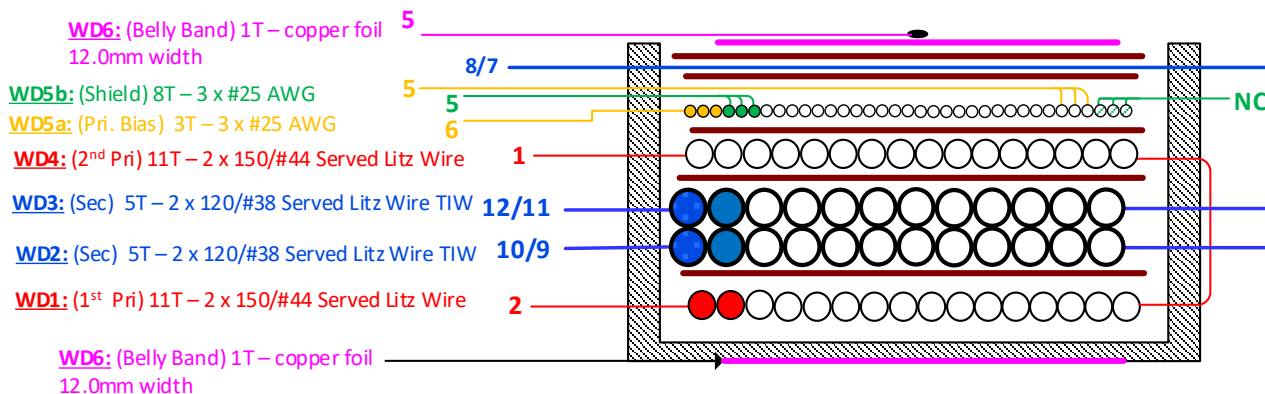
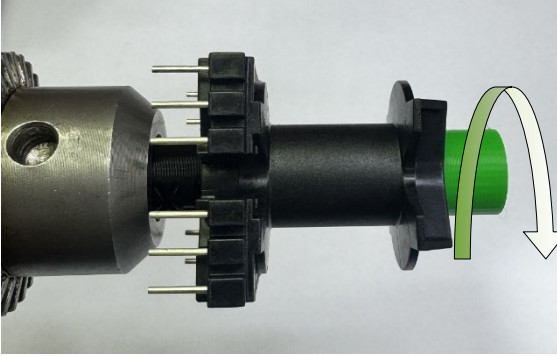
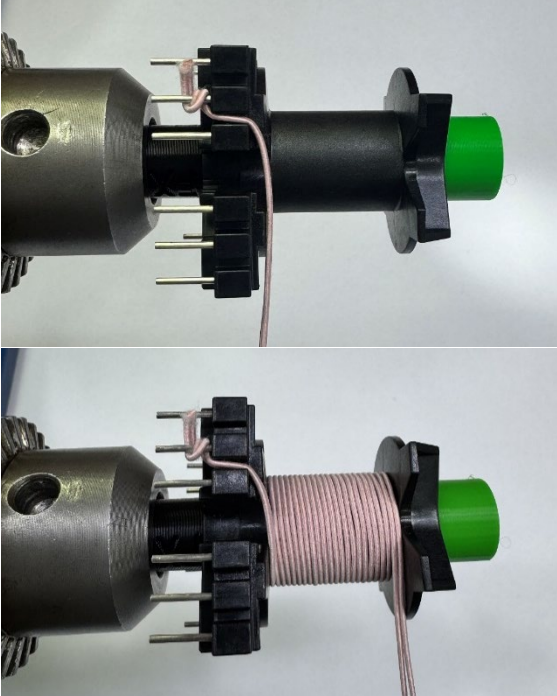
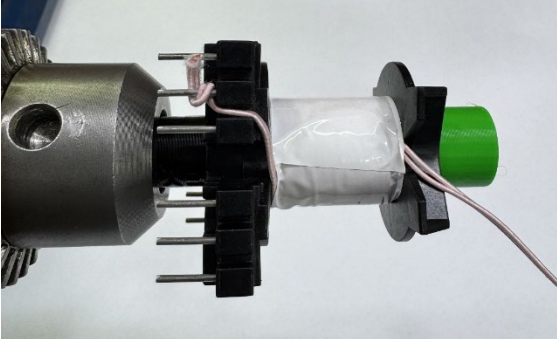


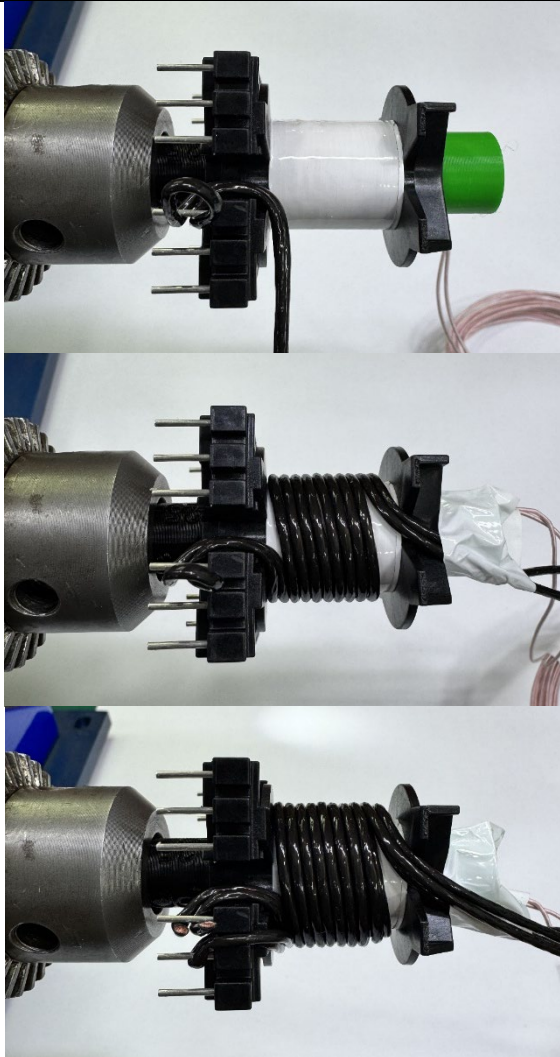
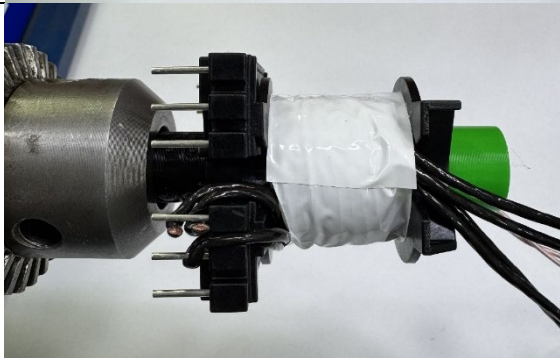
Figure 8 – Transformer Build Diagram.

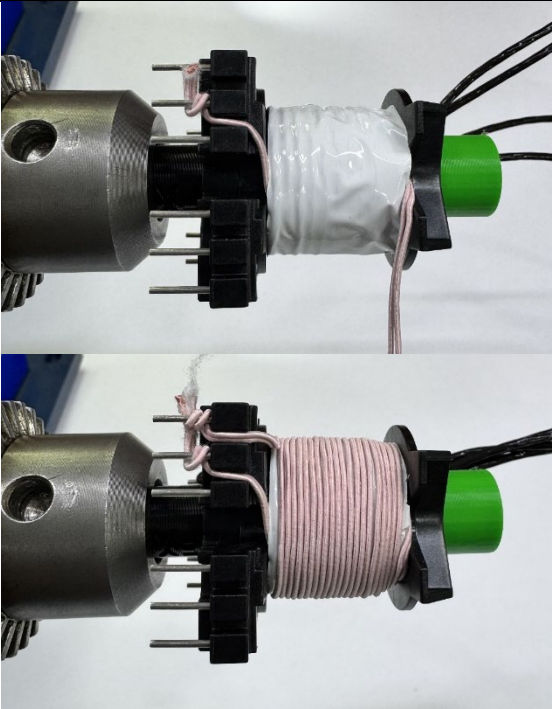
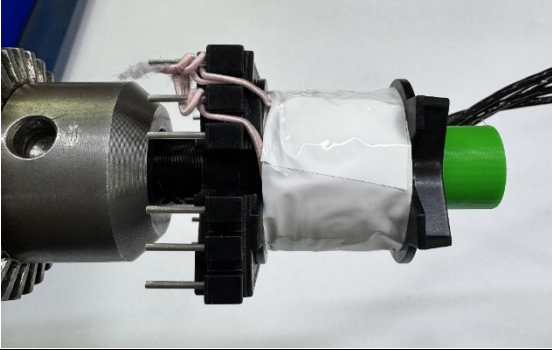
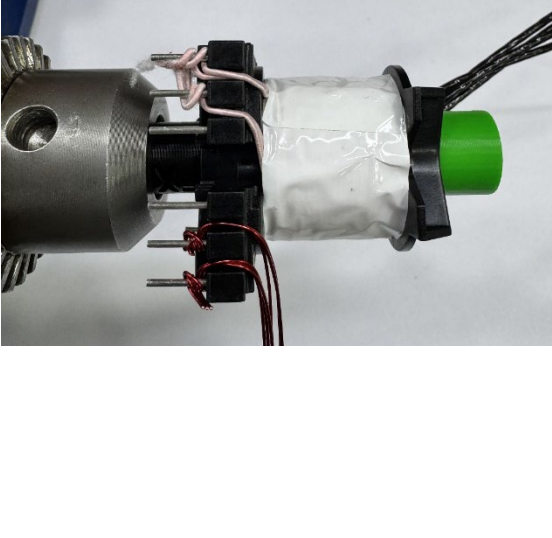
## 8.5 Winding Instructions

<b>Winding preparation</b>	Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
<b>WD1 1st Primary</b>	Start at pin 2, use 2 wires item [4] wind 11 turns in 1 layer, from left to right, spread the wires evenly across the width of bobbin. At the last turn, exit the wires, and leave enough length of wire-floating for WD4 - 2nd Primary.
<b>Insulation</b>	1 layer of tape item [7].
<b>WD2, WD3 Secondary</b>	Use 2 wires item [5], start at pin 10, wind 5 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40mm floating for WD2.  Use 2 wires item [5], start at pin 11, wind 5 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40mm floating for WD3.
<b>WD3 Sec-Bias</b>	Start at pin 12, wind 1 turn of wire item [6] and end at pin 11, should cross or twist end lead with start lead before termination to pins.
<b>Insulation</b>	1 layer of tape item [7].
<b>WD4 2nd Primary</b>	Use floating wires from WD1-1st Primary, wind 11 turns from right to left, spread the wires evenly across the width of bobbin, and finish at pin 1.
<b>Insulation</b>	1 layer of tape item [7].
<b>WD5a: Bias &amp; WD5b: Shield</b>	Use 3 wires item [3] start at pin 6 for Bias winding, also use 3 wires same item [3] start at pin 5 for Shield winding.  Wind all 8 wires in parallel, <ul style="list-style-type: none"> <li>- At the 3rd turn, place 1 small pcs of tape to hold all wires, bring 3 wires for Bias winding to the left and terminate at pin 5,</li> <li>- continue winding to 8th turn., cut short 34 wires for Shield1 Winding as No-Connect</li> </ul>
<b>Insulation</b>	1 layer of tape item [7] and bring fly wires from Secondary windings to left and terminate at pin 7, 8.
<b>Finish</b>	Gap core halves to get 135.5 uH. Place 2 layers of tape item [6] inside and 1 layer outside on core which place on pin side of bobbin.  Secure cores with tape. Place 1 turn copper foil of tape item [8] around body of transformer for WD6, solder at join to make close loop. Solder wire item [10] to copper foil and pin 5. Wrap around the body of transformer 2 layers of tape item [8] Varnish with item [9]. Soak transformer for 10 mins, then heat in oven at 100 °C for 1 hr.

### 8.6 Winding Illustrations


<p><b>Winding preparation</b></p>		<p>Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.</p>
<p><b>WD1 1<sup>st</sup> Primary</b></p>		<p>Start at pin 2, use 2 wires item [4] wind 11 turns in 1 layer, from left to right, spread the wires evenly across the width of bobbin. At the last turn, exit the wires, and leave enough length of wire-floating for WD4 - 2<sup>nd</sup> Primary.</p>
<p><b>Insulation</b></p>		<p>1 layer of tape item [7].</p>

<p><b>WD2, WD3 Secondary</b></p>		<p>Use 2 wires item [5], start at pin 10, wind 5 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40mm floating for WD2.</p> <p>Use 2 wires item [5], start at pin 11, wind 5 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40mm floating for WD3.</p>
<p><b>Insulation</b></p>		<p>1 layer of tape item [7].</p>

<p><b>WD4 2<sup>nd</sup> Primary</b></p>		<p>Use floating wires from WD1-1<sup>st</sup> Primary, wind 11 turns from right to left, spread the wires evenly across the width of bobbin, and finish at pin 1.</p>
<p><b>Insulation</b></p>		<p>1 layer of tape item [7].</p>
<p><b>WD5a: Bias &amp; WD5b: Shield</b></p>		<p>Use 3 wires item [3] start at pin 6 for Bias winding, also use 3 wires same item [3] start at pin 5 for Shield winding.</p> <p>Wind all 8 wires in parallel,</p> <ul style="list-style-type: none"> <li>- At the 3<sup>rd</sup> turn, place 1 small pcs of tape to hold all wires, bring 3 wires for Bias winding to the left and terminate at pin 5,</li> <li>- continue winding to 8<sup>th</sup> turn., cut short 34 wires for Shield1 Winding as No-Connect</li> </ul>

<p><b>Insulation</b></p>		<p>1 layer of tape item [7] and bring fly wires from Secondary windings to left and terminate at pin 7, 8.</p>

		
<p><b>Finish</b></p>		<p>Gap core halves to get 135.5 uH. Place 2 layers of tape item [6] inside and 1 layer outside on core which place on pin side of bobbin. <i>(see pictures beside).</i></p>

<p><b>Finish (cont'd)</b></p>		<p>Secure cores with tape.          Place 1 turn copper foil of tape item [8] around body of transformer for WD6, solder at join to make close loop.          Solder wire item [10] to copper foil and pin 5.          Wrap around the body of transformer 2 layers of tape item [8]          Varnish with item [9]. Soak transformer for 10 mins, then heat in oven at 100 °C for 1 hr.</p>
-------------------------------	---	--

**Table 7** – Transformer Winding Illustrations.

## 9 Common Mode Choke (L2) Specification

### 9.1 Electrical Diagram

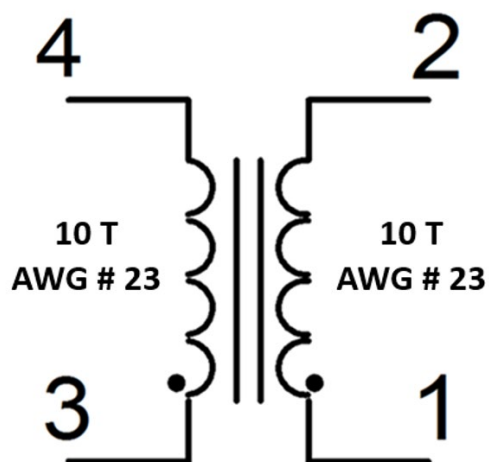


Figure 9 – Electrical Diagram.

### 9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Inductance	Measured at 1 V pk-pk and 100 kHz across pin pairs 1–2 or 3–4, with all remaining windings open-circuit.	68 $\mu$ H
Tolerance	Tolerance of inductance.	$\pm$ 20%

Table 8 – Electrical Specification.

### 9.3 Materials

Item	Description
[1]	Toroid Core: Mfg P/N 5943000321 (Green Color); PI P/N: 32-00488-00
[2]	Magnet Wire: #23 AWG.
[3]	TIW Wire: #23 AWG.

Table 9 – Materials List.

## 9.4 Build Diagram



Figure 10 – Build Diagram.

## 9.5 Winding Instructions

Winding 1 – Starting from the left and proceeding clockwise, wind 10 turns of items 2 and 3 together in a bifilar configuration, as illustrated in Figure 10.

## 10 Common Mode Choke (L5) Specification

### 10.1 Electrical Diagram

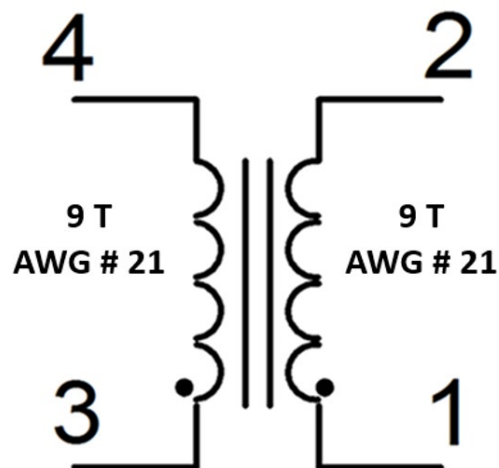


Figure 11 – Electrical Diagram.

### 10.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Inductance	Measured at 1 V pk-pk and 100 kHz across pin pairs 1–2 or 3–4, with all remaining windings open-circuit.	58 $\mu$ H
Tolerance	Tolerance of inductance.	$\pm$ 20%

Table 10 – Electrical Specification.

### 10.3 Materials

Item	Description
[1]	Toroid Core: Mfg P/N 5943000321 (Green Color); PI P/N: 32-00488-00
[2]	Magnet Wire: #21 AWG.
[3]	TIW Wire: #21 AWG.

Table 11 – Materials List.

## 10.4 Build Diagram

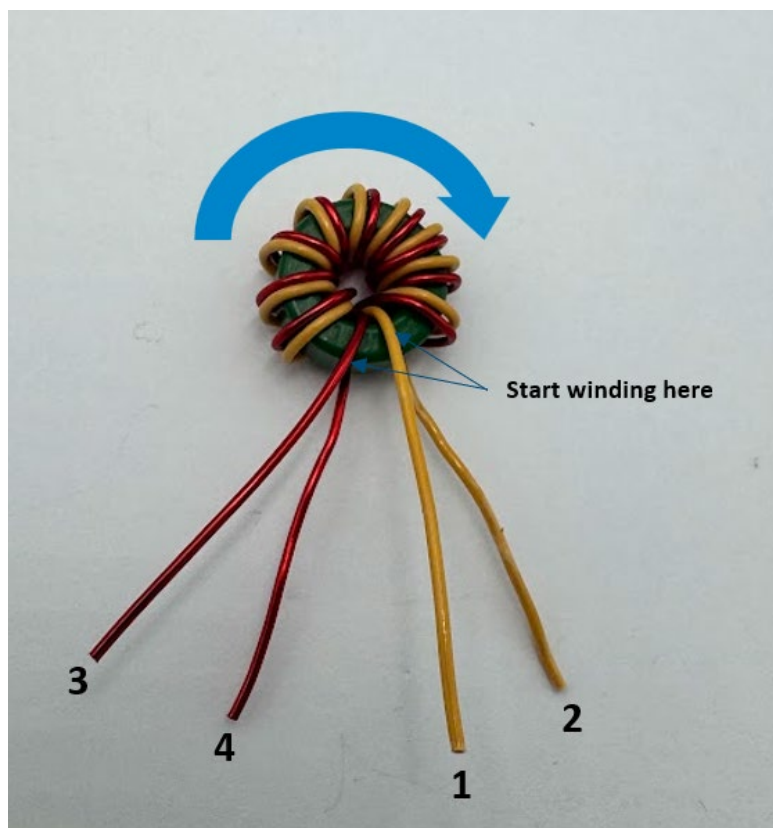


Figure 12 – Build Diagram.

## 10.5 Winding Instructions

Winding 1 – Starting from the left and proceeding clockwise, wind 9 turns of items 2 and 3 together in a bifilar configuration, as illustrated in Figure 12.

# 11 Heatsink Assembly

## 11.1 TOPSwitchGaN IC Heatsink Assembly

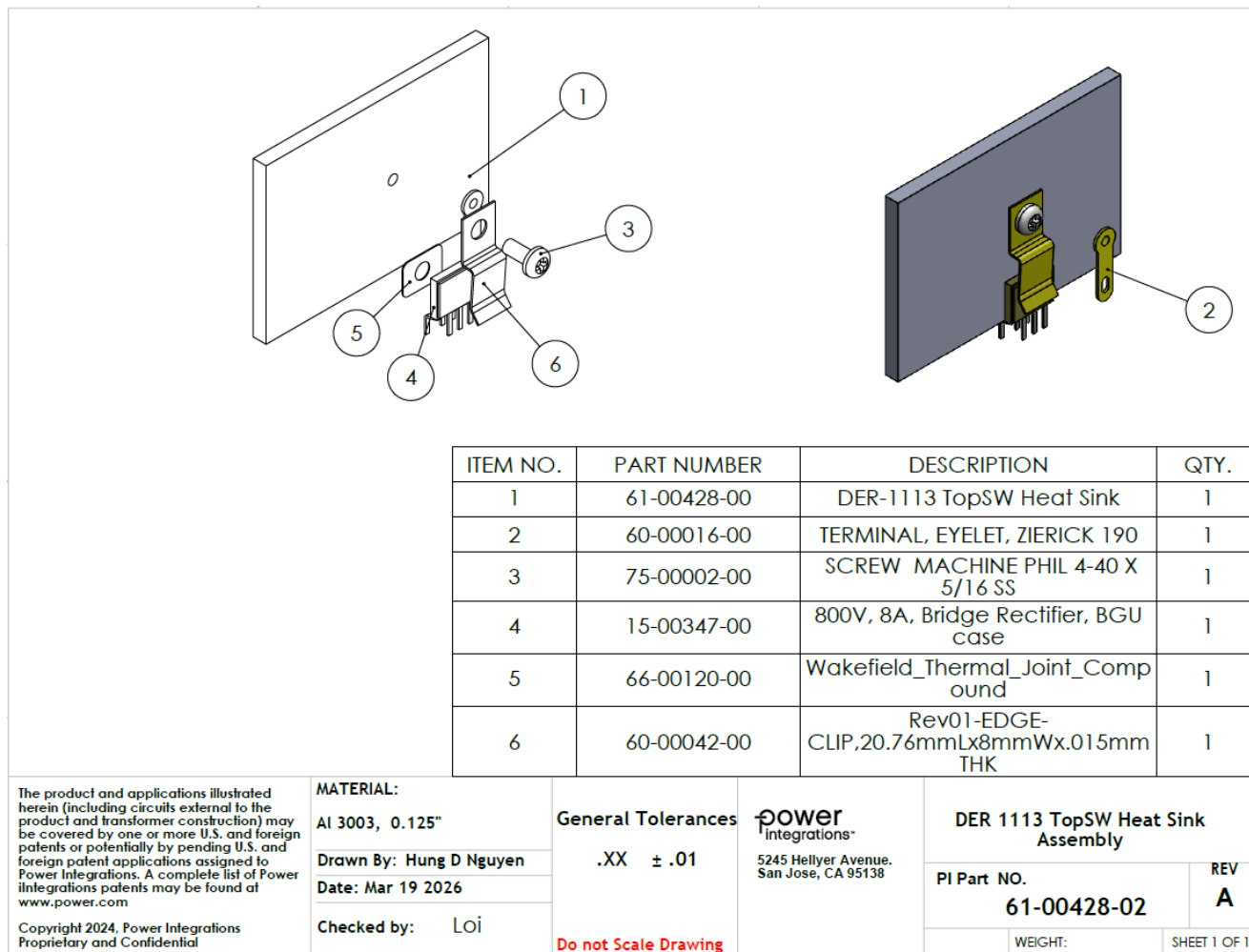
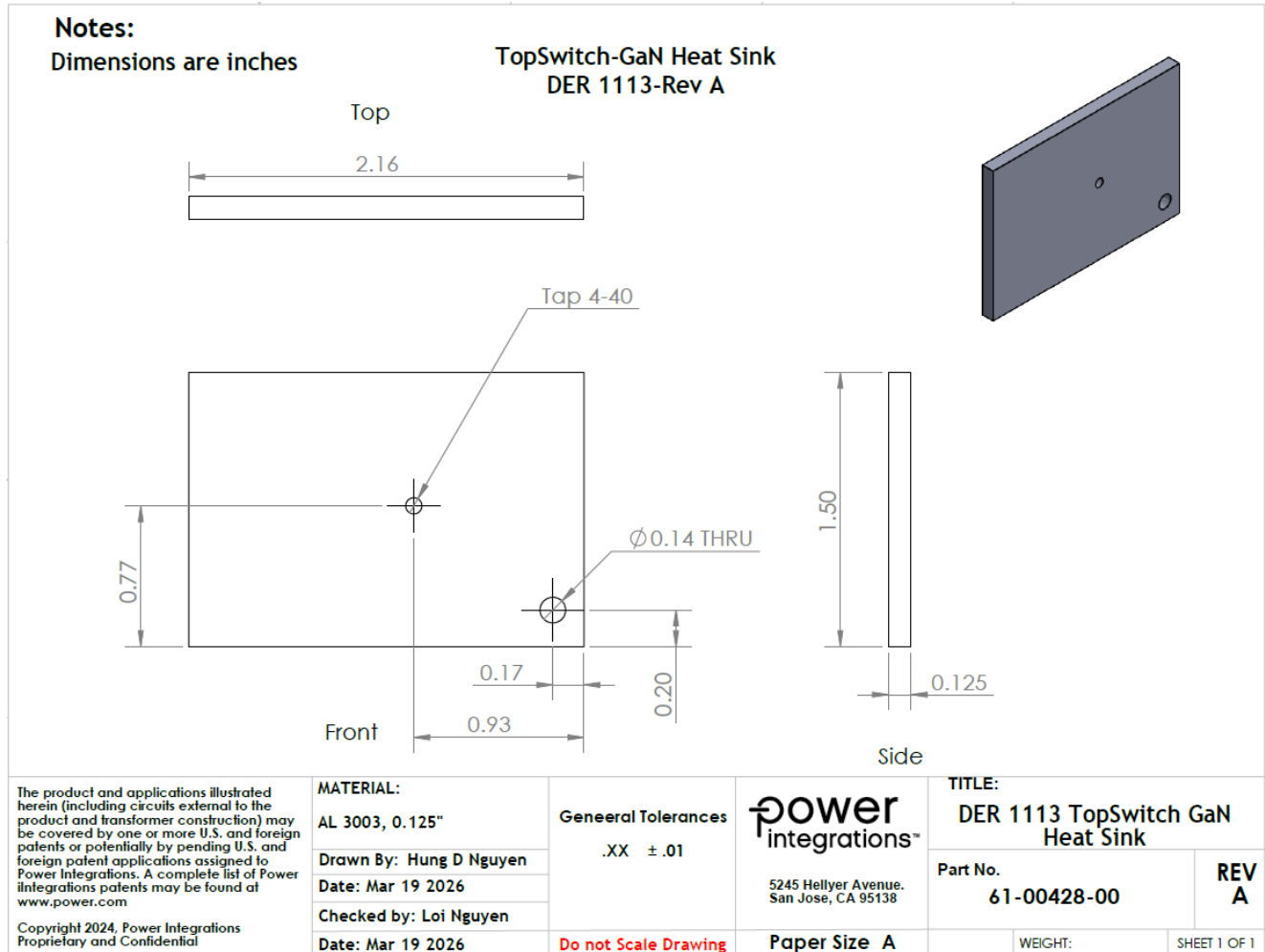


Figure 13 – TOPSwitchGaN IC Heatsink Assembly and BOM.



**Figure 14** – TOPSwitchGaN IC Heatsink Drawing.

### 11.2 Output Diode (D4) Heatsink Assembly

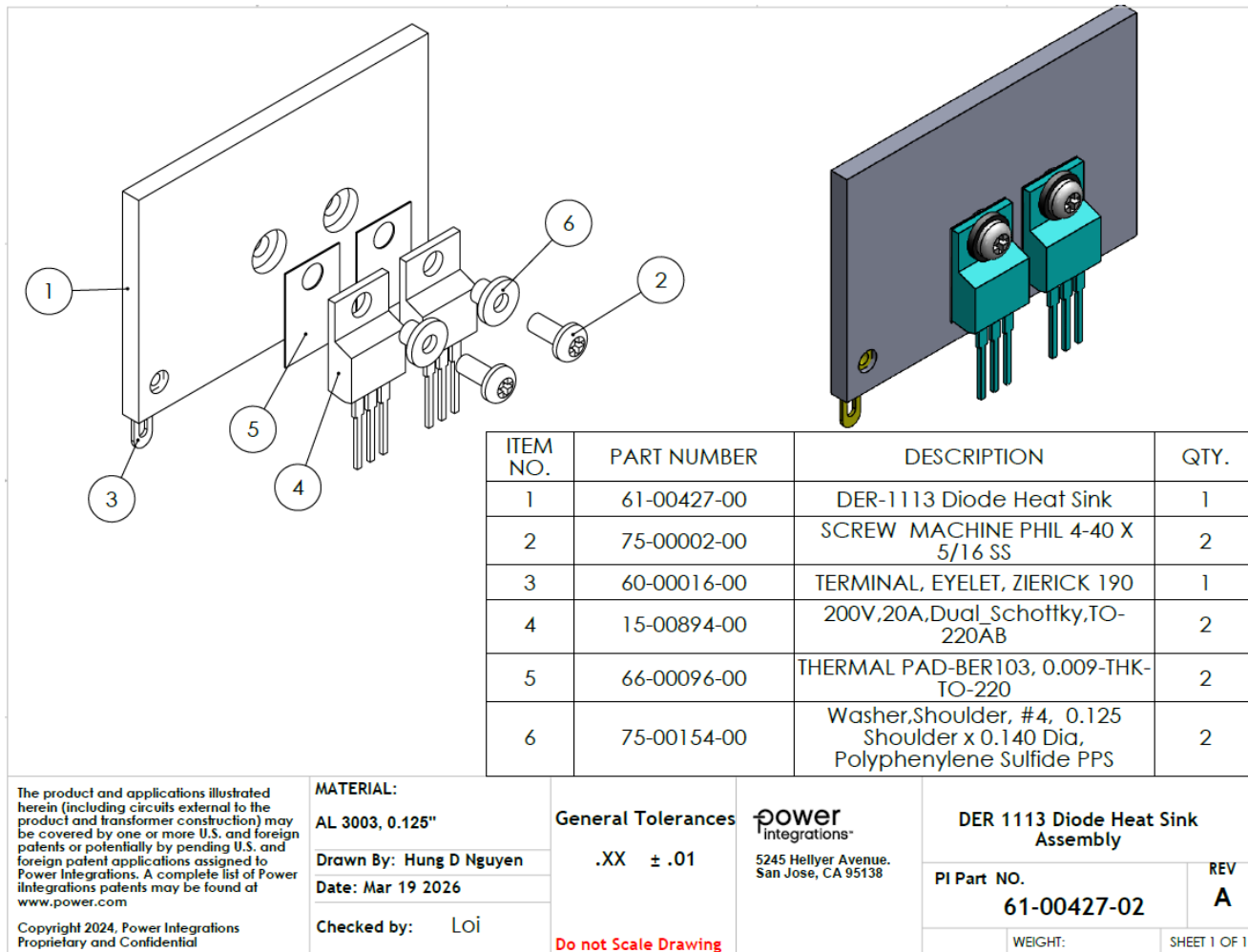


Figure 15 – Heatsink Diode Assembly and BOM.

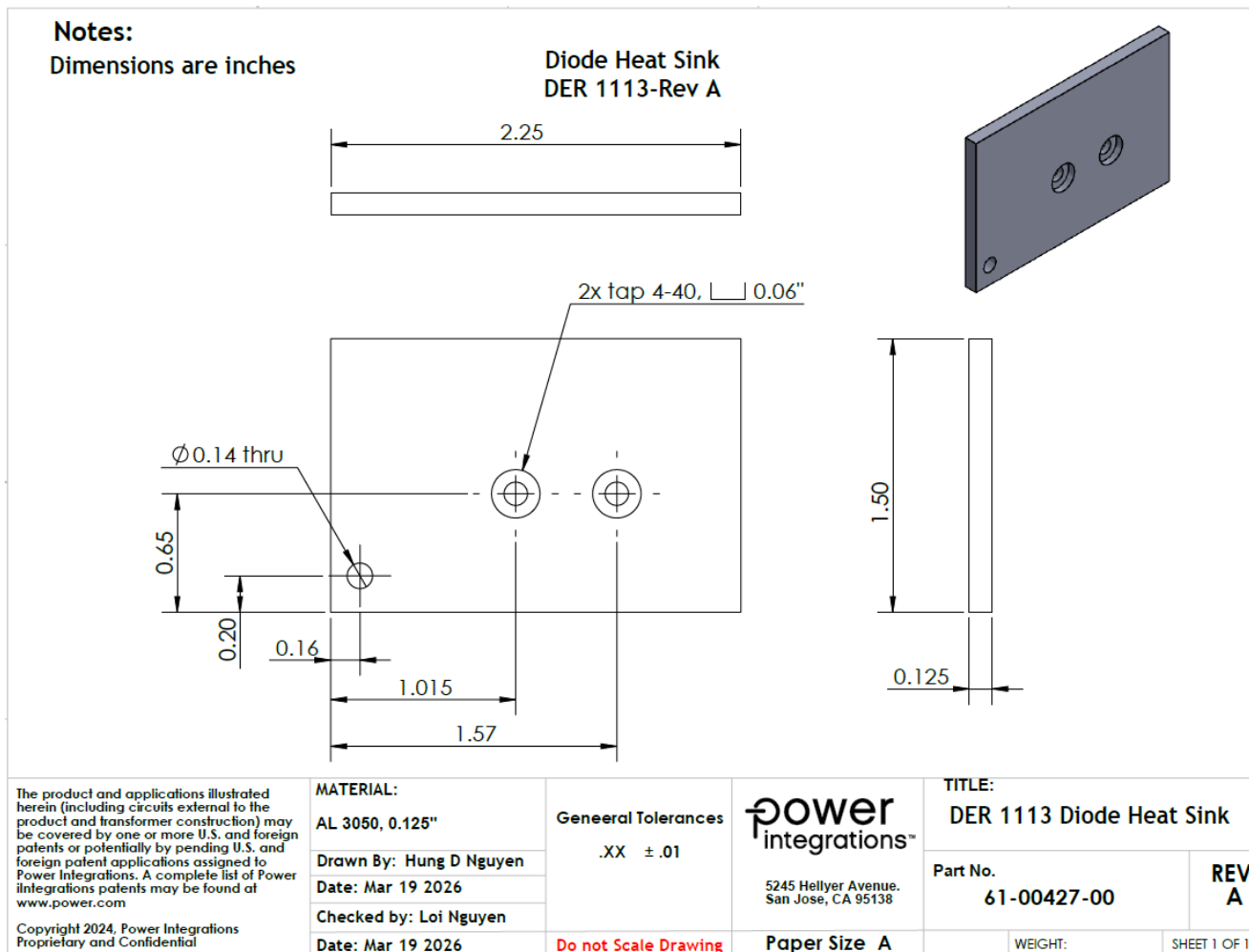


Figure 16 – Diode Heatsink Drawing.

### 11.3 Additional TOPSwitchGaN IC Heatsink Assembly Instructions

Note: Apply two layers of Kapton tape to the heatsink, following the dimensions specified in the image.

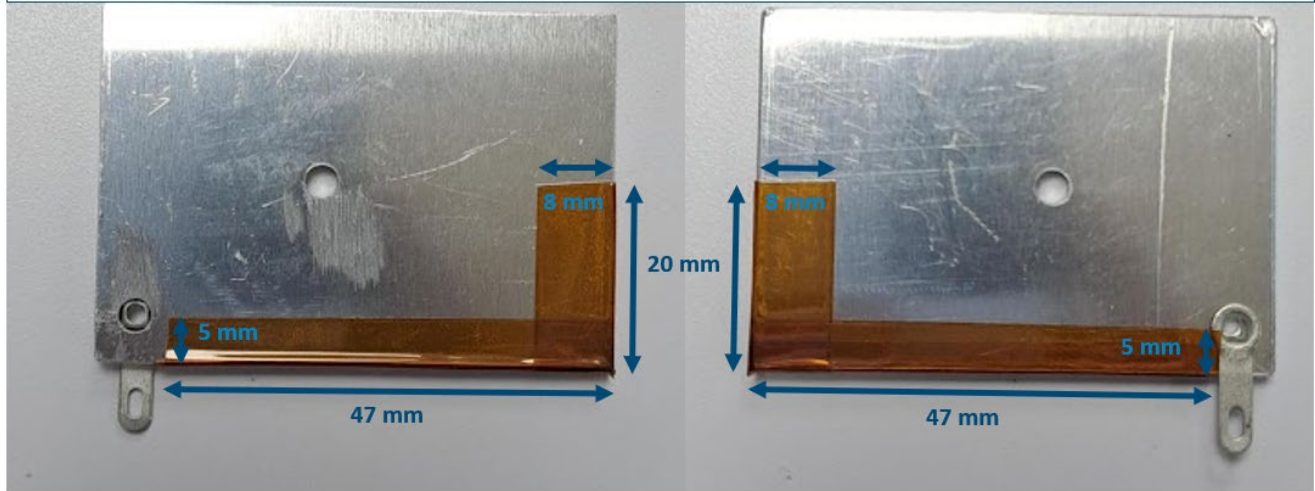


Figure 17 – Additional TOPSwitchGaN IC Heatsink Assembly Instructions.

### 11.4 Additional Diode Heatsink Assembly Instructions

Note: Apply two layers of Kapton tape to the heatsink, following the dimensions specified in the image.

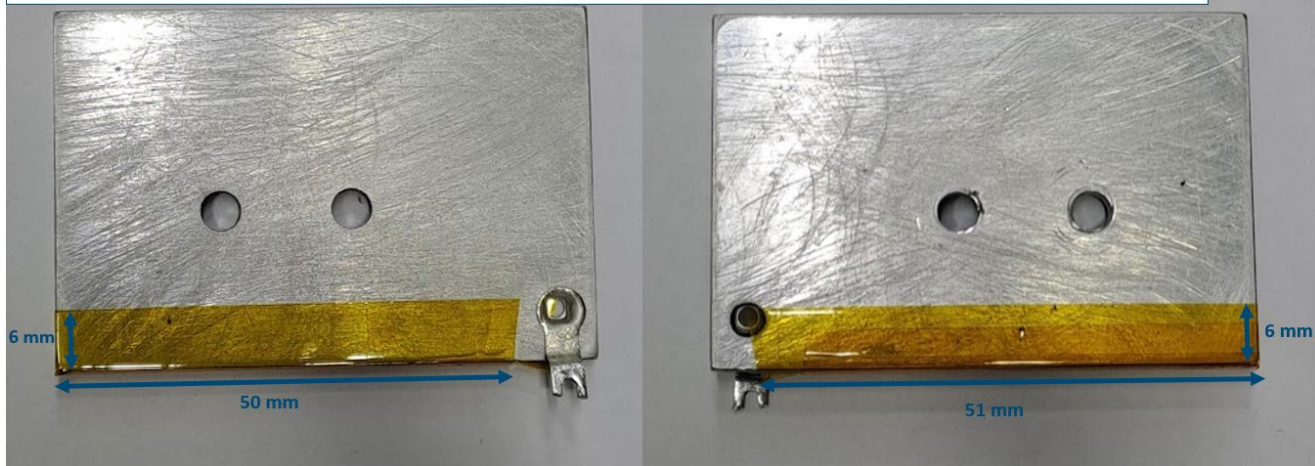
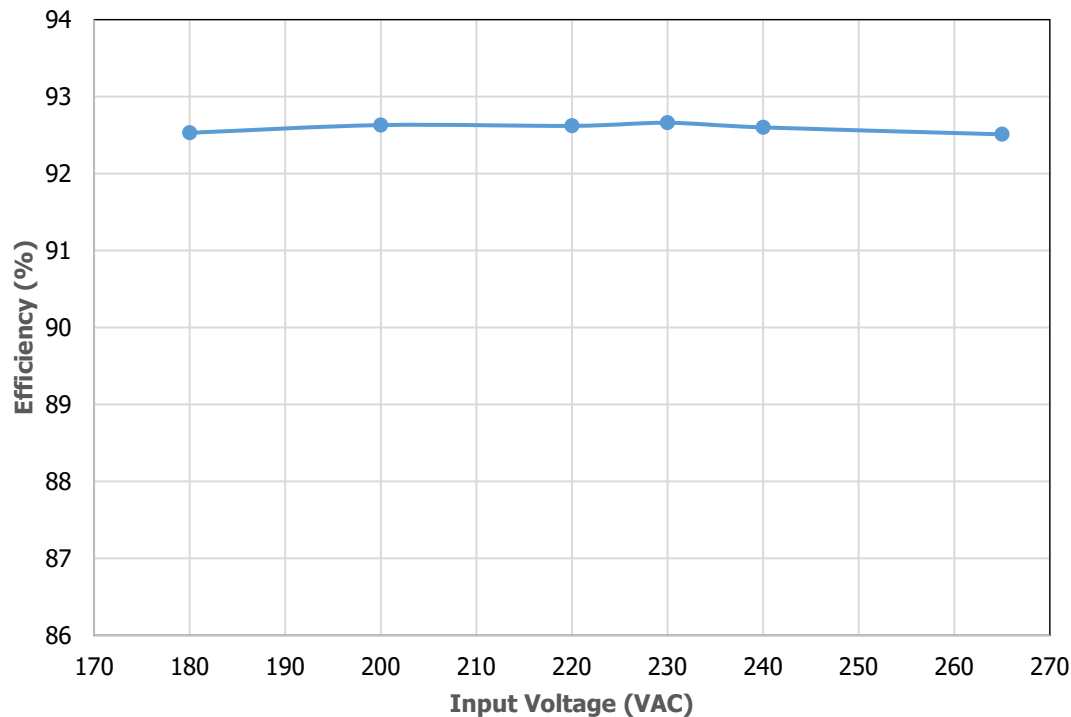


Figure 18 – Additional Diode Heatsink Assembly Instructions.

## 12 Performance Data

### 12.1 Efficiency at Full Load

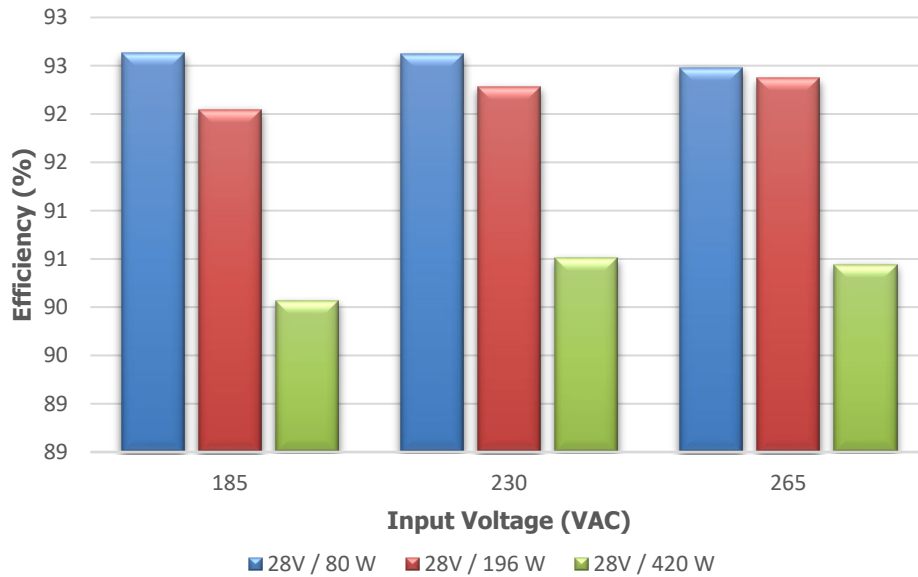
**Note:** Tests were conducted to evaluate efficiency versus input line voltage. The input voltage was varied from 180 VAC to 265 VAC. The output power was set to 80 W, and measurements were taken at an ambient of 25 °C.



**Figure 19** – Efficiency vs. Input Line Voltage at Full Load.

## 12.2 Efficiency vs. Line Voltage

**Note:** Tests were conducted to evaluate efficiency versus input line voltage. The input voltage was varied from 180 VAC to 265 VAC. Output power levels were set to 80 W, 196 W and 420 W with a soak at 5 seconds at each line condition. All measurements were taken at an ambient of with a 25 °C.



**Figure 20** – Efficiency vs Line.

### 12.3 Efficiency vs. Output Load

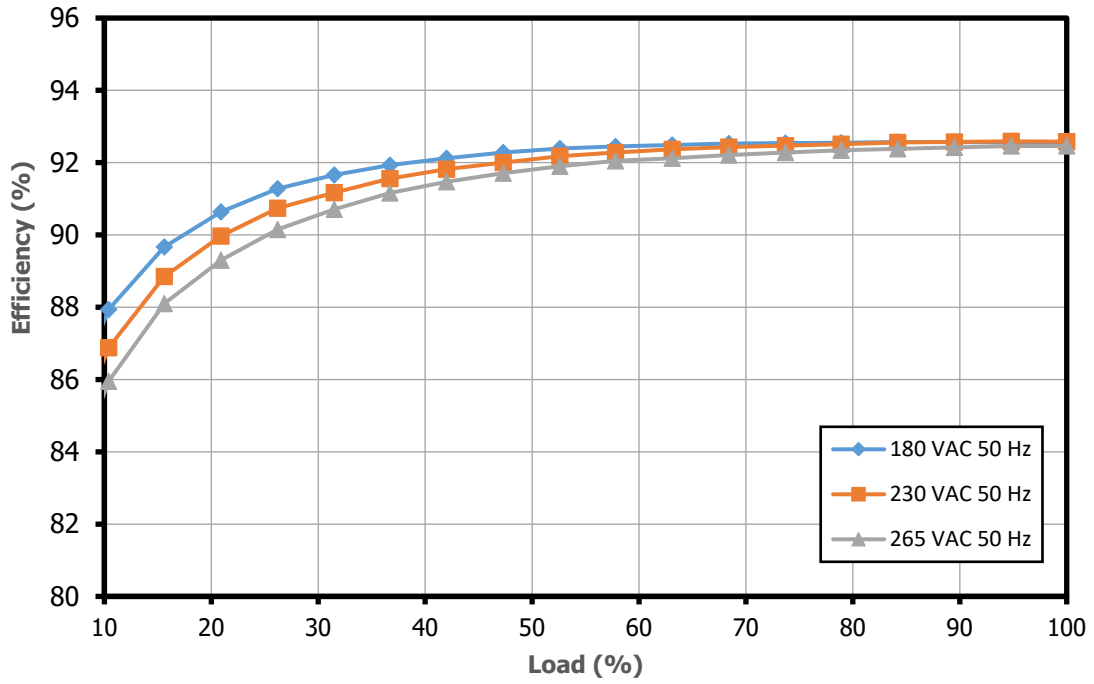


Figure 21 – Efficiency vs. Output Load.

### 12.4 Output Voltage Regulation vs. Input Line

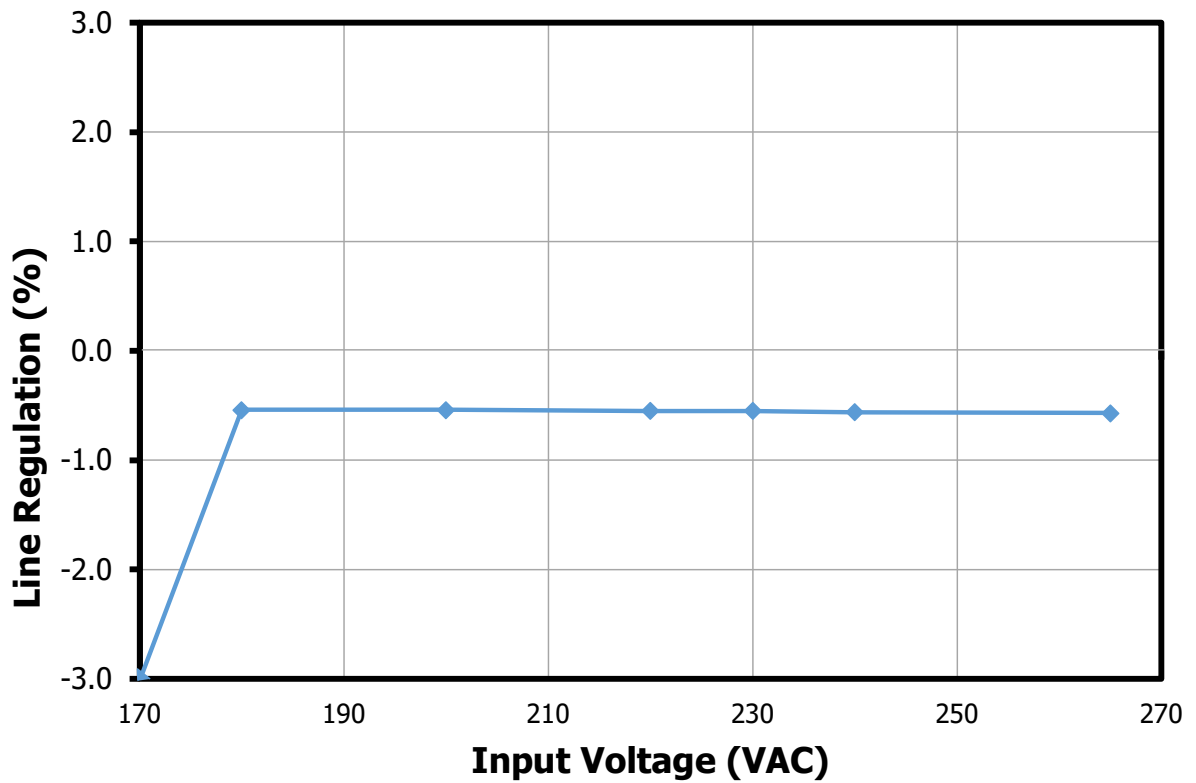


Figure 22 – Output Voltage Regulation vs Input Line at Full Load.

### 12.5 Output Voltage Regulation vs. Output Load

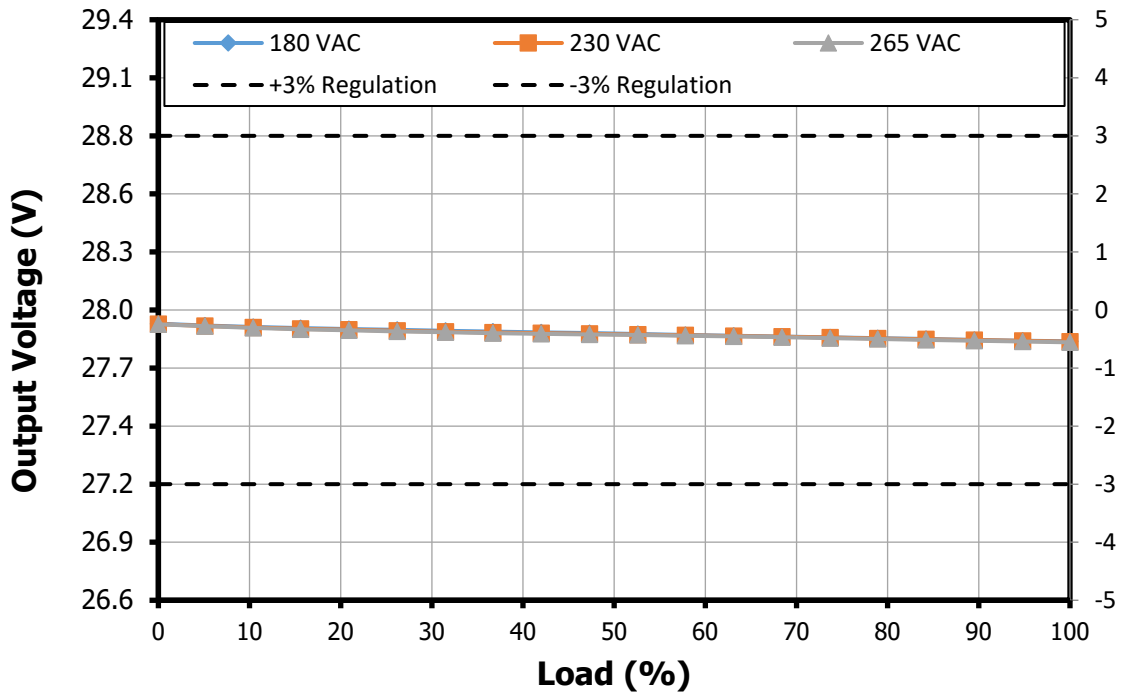


Figure 23 – Output Voltage Regulation vs Output Load.

## 12.6 Energy Efficiency Performance

### 12.6.1 Average Efficiency

This design easily meets the DOE Level VI average-efficiency requirements, with approximately 4% margin.

Input: 180 VAC							
Load	P <sub>IN</sub>	V <sub>o</sub>	I <sub>o</sub>	P <sub>o</sub>	Efficiency	Average Efficiency	DOE6
(%)	(W)	(V)	(A)	(W)	(%)	(%)	(%)
100	86.5	27.8	2.9	80.1	92.6	<b>92.2</b>	87.5
75	64.8	27.8	2.1	60.0	92.6		
50	43.3	27.8	1.4	40.1	92.4		
25	21.8	27.9	0.7	19.9	91.2		
10	8.82	27.9	0.28	7.73	87.6	---	---
Input: 230 VAC							
Load	P <sub>IN</sub>	V <sub>o</sub>	I <sub>o</sub>	P <sub>o</sub>	Efficiency	Average Efficiency	DOE6 Limit
(%)	(W)	(V)	(A)	(W)	(%)	(%)	(%)
100	86.5	27.8	2.90	80.1	92.6	<b>91.9</b>	87.5
75	64.9	27.8	2.15	60.0	92.5		
50	43.5	27.9	1.43	40.1	92.1		
25	22.0	27.9	0.71	19.9	90.6		
10	8.93	27.9	0.28	7.73	86.6	---	---
Input: 265 VAC							
Load	P <sub>IN</sub>	V <sub>o</sub>	I <sub>o</sub>	P <sub>o</sub>	Efficiency	Average Efficiency	DOE6 Limit
(%)	(W)	(V)	(A)	(W)	(%)	(%)	(%)
100	86.6	27.8	2.88	80.1	92.5	<b>91.6</b>	87.5
75	65.0	27.8	2.15	60.0	92.3		
50	43.6	27.9	1.44	40.1	91.8		
25	22.1	27.9	0.71	19.9	90.0		
10	9.04	27.9	0.28	7.73	85.5	---	---

**Table 12** – Average Efficiency.

### 12.6.2 No Load Input Power Consumption

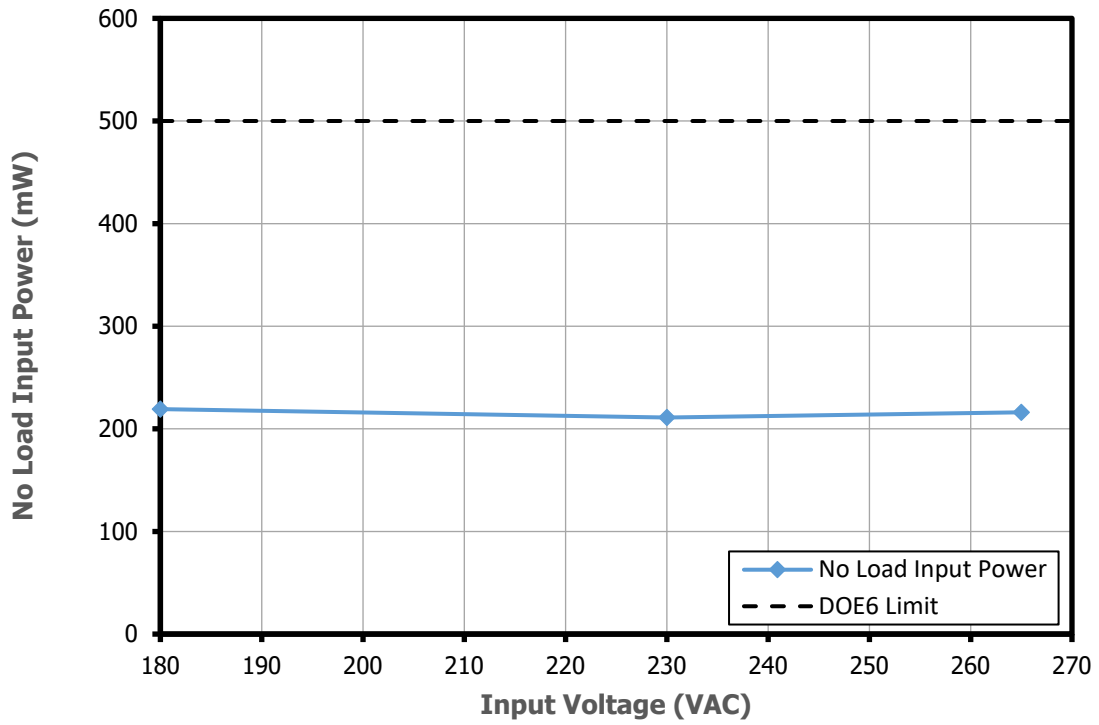


Figure 24 – No Load Input Power vs. Input Voltage.

## 12.7 Output Ripple Voltage vs. Output Load

Output ripple voltage is measured on the board using a voltage probe which has an added 47  $\mu\text{F}$  electrolytic capacitor and a 100 nF ceramic capacitor connected across the probe tip to reduce periodic and random noise. See section 13.7.1 for the test setup and ripple voltage waveforms.

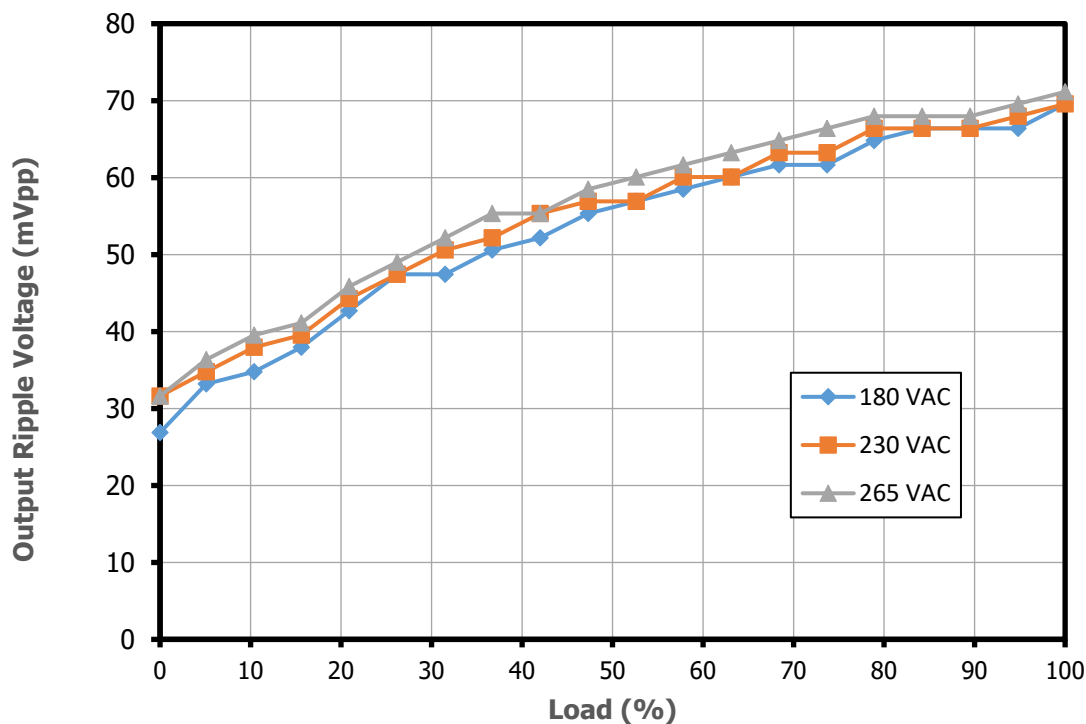


Figure 25 – Output Ripple Voltage vs Output Load Current.

## 12.8 Thermal Performance at 60 °C Ambient

The power supply unit (PSU) was enclosed within a plastic housing and placed inside an environmental chamber set to a static ambient of 60 °C. The unit was operated using an electronic load (E-load) delivering 420W output peak power. The component thermal profile was recorded until the unit reached thermal stabilization.



Type K Thermocouples

**Figure 26** – Thermal Scan Test Set-up at 60 °C Ambient.  
(DER-1113 board is enclosed within an isolated enclosure and placed inside a thermal chamber)

### 12.8.1 Thermal Test Data Summary at 60 °C Ambient

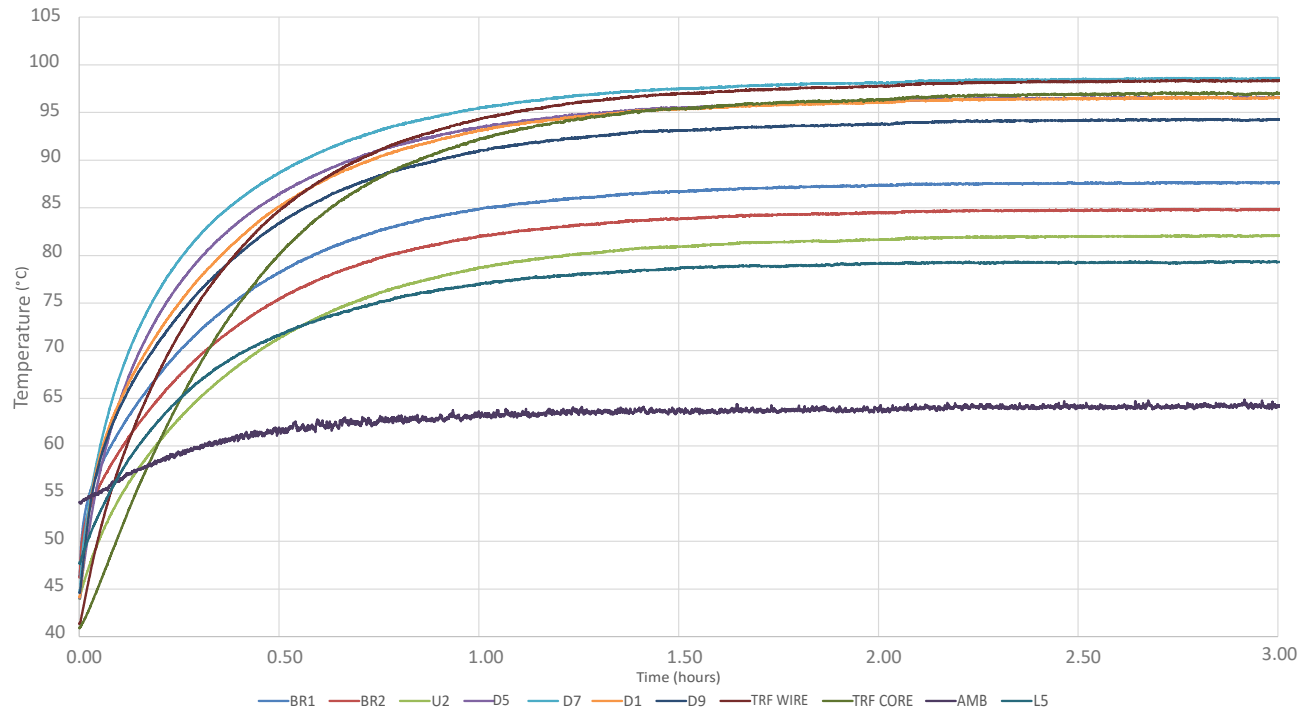
The thermal scan data in Table 13 shows that components remained well below their maximum temperature ratings across the entire input voltage range.

Component	Continuous Load: 28 V / 80 W		Dynamic Loading: 28 V / 80 W (50 s) - 420 W (5 s), for 3 hours, Ambient = 60 °C	
	180 VAC	265 VAC	180 VAC	265 VAC
<b>BR1</b>	87.7	82.7	97.1	97.0
<b>BR2</b>	84.9	79.9	93.5	93.4
<b>U2</b>	82.1	82.6	95.2	95.0
<b>D5</b>	96.6	96.3	114	113
<b>D7</b>	98.6	98.6	119	119
<b>D1</b>	96.6	94.6	109	109
<b>D9</b>	94.3	92.8	106	106
<b>TRF WIRE</b>	98.4	96.9	115	115
<b>TRF CORE</b>	97.1	94.8	111	111
<b>Ambient</b>	64.8	64.8	67.0	68.5
<b>L5</b>	79.4	80.0	103	103

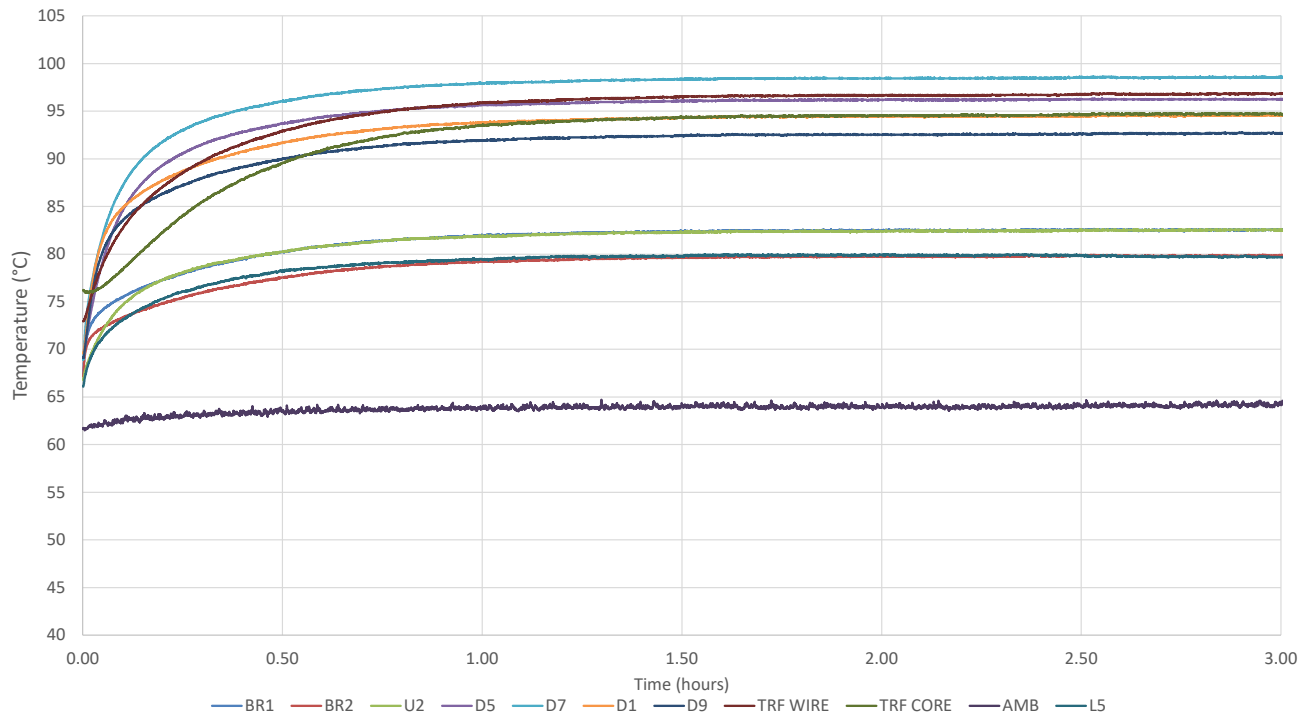
**Table 13** – Thermal Test Data at 60 °C Ambient.

### 12.8.2 Component Thermal Profile at 60 °C Ambient

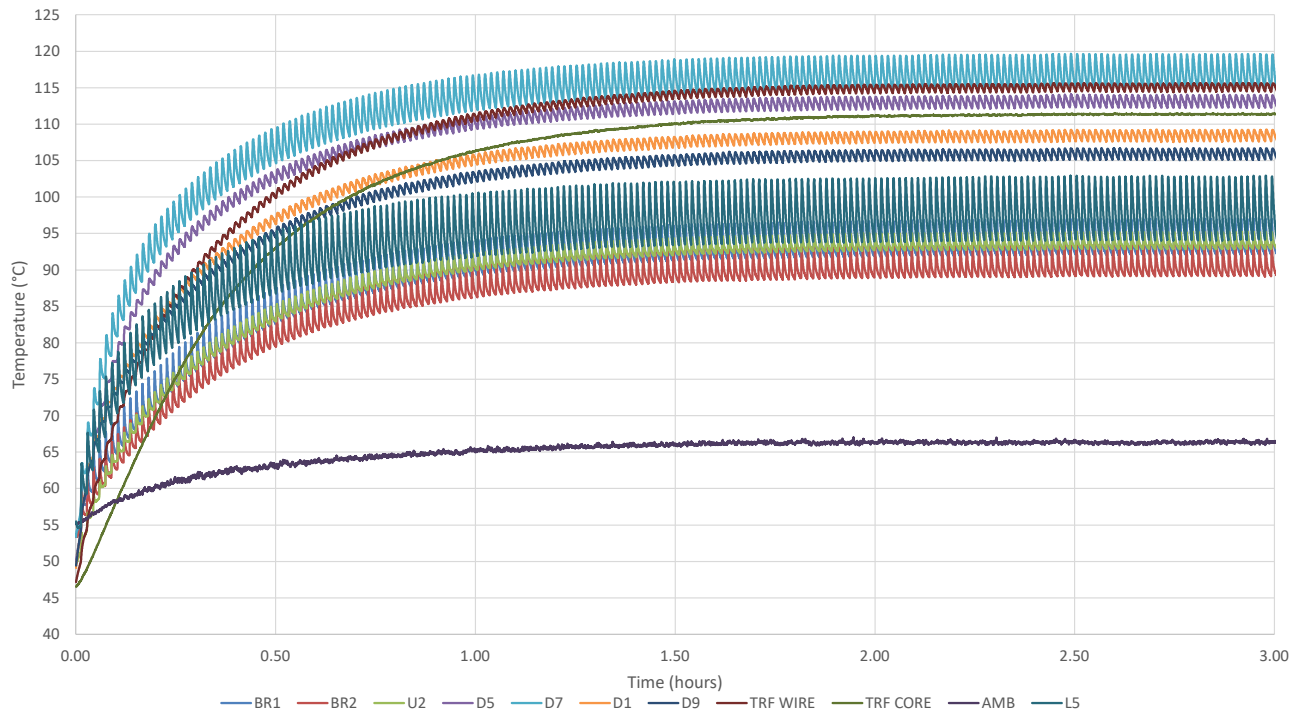
The thermal charts in the following figures illustrate the temperature profile of the DER-1113 heating components. All component temperatures stabilized after 3 hours, and the measured values remained well below their specified limits.



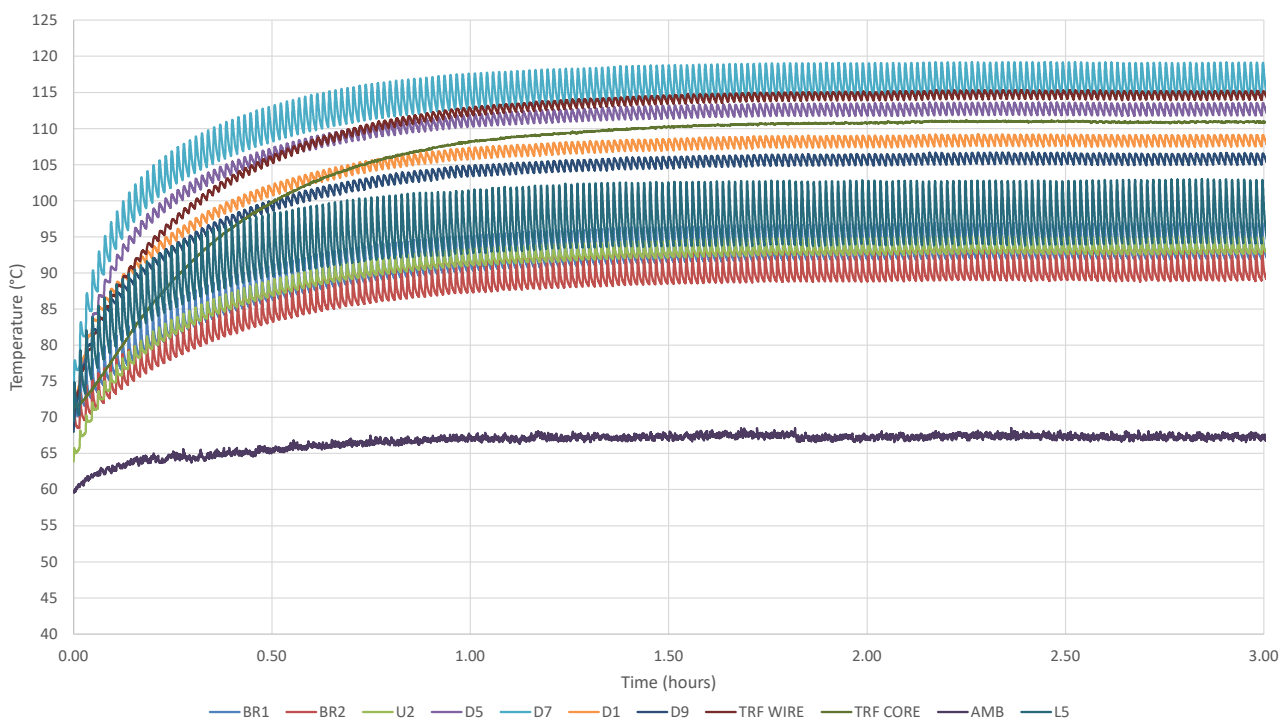
**Figure 27** – Thermal Profile at 180 VAC, Continuous Load at 28 V / 80 W, Ambient = 60 °C.



**Figure 28** – Thermal Profile at 265 VAC, Continuous Load at 28 V / 80 W, Ambient = 60 °C.



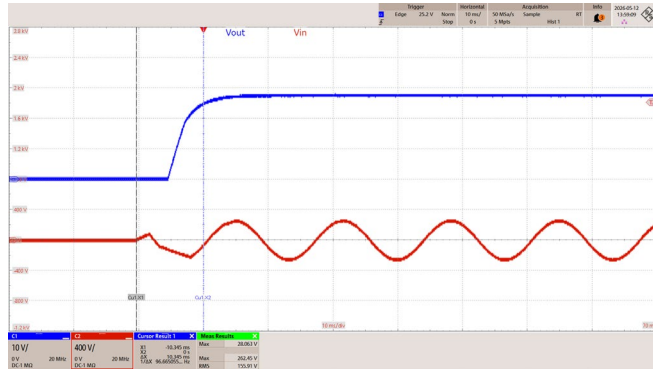
**Figure 29** – Thermal Profile at 180 VAC, Dynamic Loading: 28 V / 80 W (50 s) - 420 W (5 s), Ambient = 60 °C.



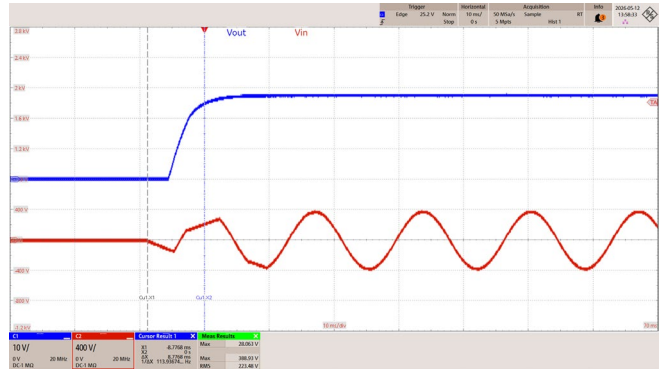
**Figure 30** – Thermal Profile at 265 VAC, Dynamic Loading: 28 V / 80 W (50 s) - 420 W (5 s), Ambient = 60 °C.

### 13 Waveforms

#### 13.1 Output Voltage Profile at Full-Load Start-Up

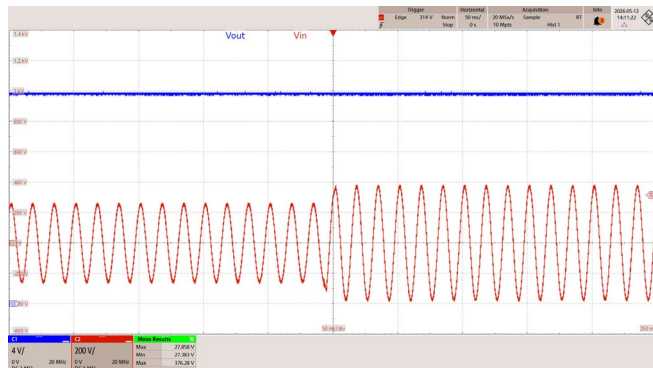


**Figure 31** – 180 VAC, 50 Hz, Full-Load Start-Up.  
 CH1:  $V_{OUT}$ , 10 V / div., 10 ms / div.  
 CH2:  $V_{IN}$ , 400 V / div., 10 ms / div.  
 $t_{ON}$  Delay = 10.3 ms  
 $V_{OUT}$  Max = 28 V

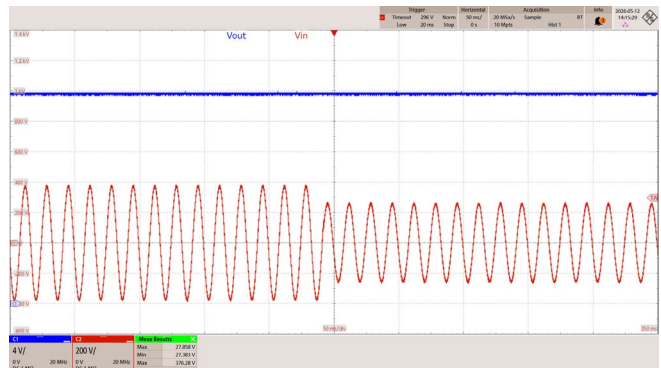


**Figure 32** – 265 VAC, 50 Hz, Full-Load Start-Up.  
 CH1:  $V_{OUT}$ , 10 V / div., 10 ms / div.  
 CH2:  $V_{IN}$ , 400 V / div., 10 ms / div.  
 $t_{ON}$  Delay = 8.78 ms  
 $V_{OUT}$  Max = 28 V

#### 13.2 Output Voltage During Step Line Transient

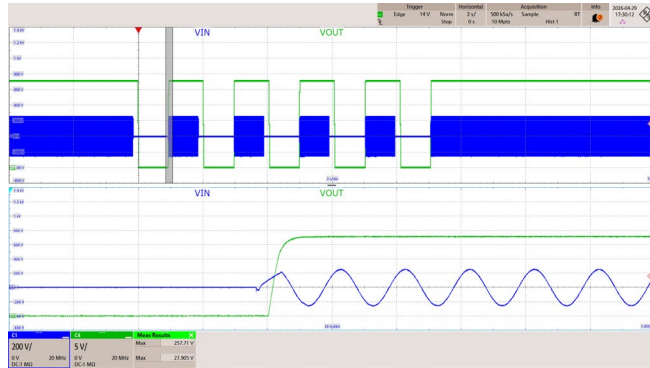


**Figure 33** – 180 VAC – 265 VAC, Step Line Transient.  
 CH1:  $V_{OUT}$ , 4 V / div., 50 ms / div.  
 CH2:  $V_{IN}$ , 200 V / div., 50 ms / div.  
 $V_{OUT}$  Max = 27.8 V  
 $V_{OUT}$  Min = 27.4 V



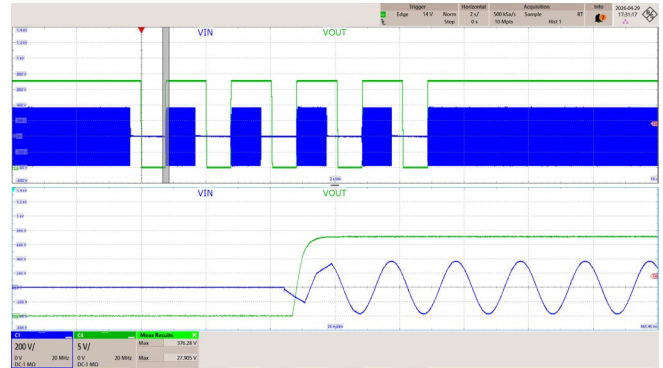
**Figure 34** – 265 VAC – 180 VAC, Step Line Transient.  
 CH1:  $V_{OUT}$ , 4 V / div., 50 ms / div.  
 CH2:  $V_{IN}$ , 200 V / div., 50 ms / div.  
 $V_{OUT}$  Max = 27.8 V  
 $V_{OUT}$  Min = 27.4 V

### 13.3 Output Voltage Profile During 1 s AC On/Off Cycling (Ambient = 60 °C)



**Figure 35** – 180 VAC, 50 Hz, 80 W, 1s On/Off Cycling.

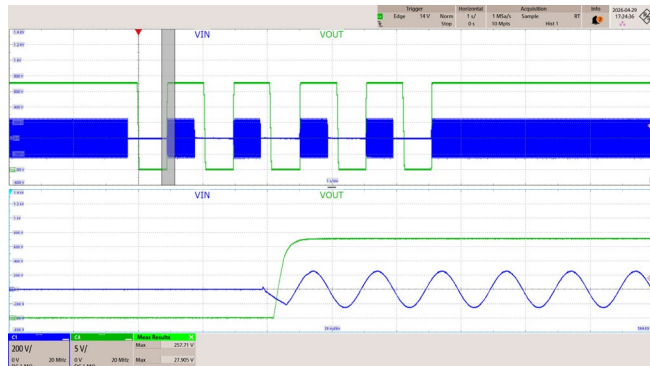
CH1:  $V_{IN}$ , 200 V / div., 2 s / div.  
 CH4:  $V_{OUT}$ , 5 V / div., 2 s / div.  
 Zoom-in: 20 ms / div.  
 $V_{OUT\ Max} = 27.9\ V$   
 $V_{IN\ Max} = 257\ V$



**Figure 36** – 265 VAC, 50 Hz, 80 W, 1s On/Off Cycling.

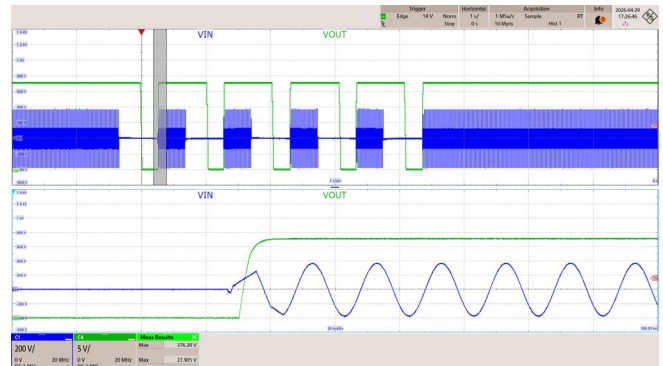
CH1:  $V_{IN}$ , 200 V / div., 2 s / div.  
 CH4:  $V_{OUT}$ , 5 V / div., 2 s / div.  
 Zoom-in: 20 ms / div.  
 $V_{OUT\ Max} = 27.9\ V$   
 $V_{IN\ Max} = 376\ V$

### 13.4 Output Voltage Profile During 500 ms AC On/Off Cycling (Ambient = 60 °C)



**Figure 37** – 180 VAC, 50 Hz, 80 W, 500 ms On/Off Cycling.

CH1:  $V_{IN}$ , 200 V / div., 1 s / div.  
 CH4:  $V_{OUT}$ , 5 V / div., 1 s / div.  
 Zoom-in: 20 ms / div.  
 $V_{OUT\ Max} = 27.9\ V$   
 $V_{IN\ Max} = 257\ V$

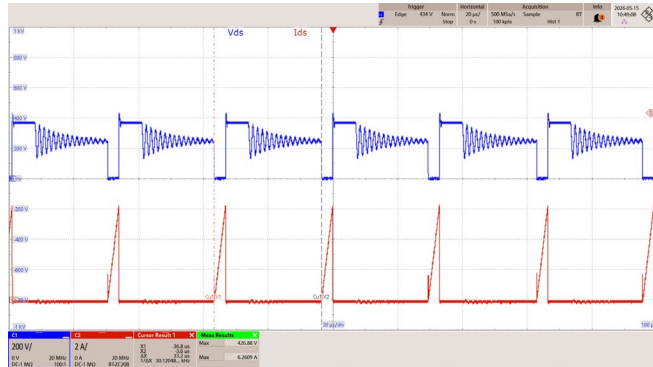


**Figure 38** – 265 VAC, 50 Hz, 80 W, 500 ms On/Off Cycling.

CH1:  $V_{IN}$ , 200 V / div., 1 s / div.  
 CH4:  $V_{OUT}$ , 5 V / div., 1 s / div.  
 Zoom-in: 20 ms / div.  
 $V_{OUT\ Max} = 27.9\ V$   
 $V_{IN\ Max} = 376\ V$

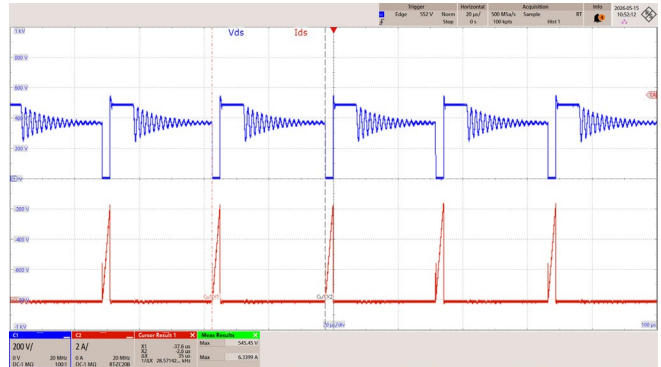
### 13.5 Primary Drain Voltage and Current

#### 13.5.1 Steady State Operation



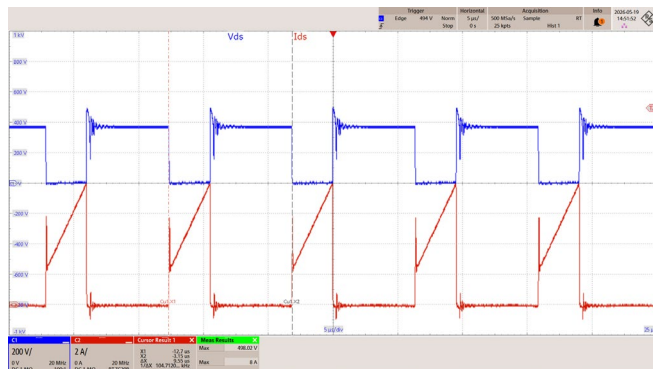
**Figure 39** – 180 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Steady-State Operation

CH1:  $V_{DS}$ , 200 V / div., 20  $\mu$ s / div.  
 CH2:  $I_{DS}$ , 2 A / div., 20  $\mu$ s / div.  
 $V_{DS}$  Max = 427 V  
 $I_{DS}$  Max = 6.2 A  
 $F_{sw}$  = 30.1 kHz



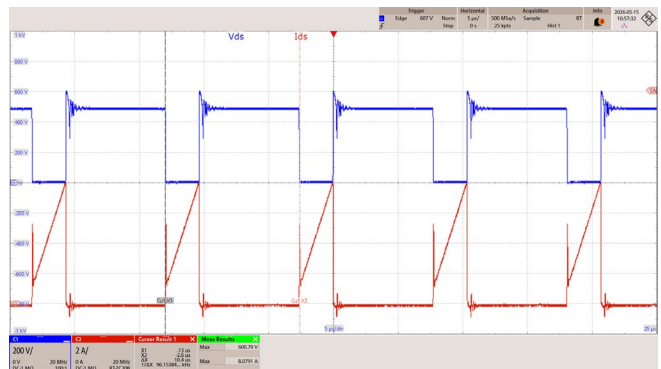
**Figure 40** – 265 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Steady-State Operation

CH1:  $V_{DS}$ , 200 V / div., 20  $\mu$ s / div.  
 CH2:  $I_{DS}$ , 2 A / div., 20  $\mu$ s / div.  
 $V_{DS}$  Max = 545 V  
 $I_{DS}$  Max = 6.34 A  
 $F_{sw}$  = 28.5 kHz



**Figure 41** – 180 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Steady-State Operation

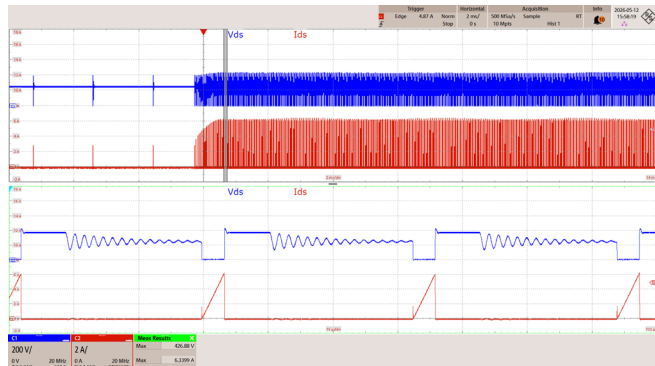
CH1:  $V_{DS}$ , 200 V / div., 20  $\mu$ s / div.  
 CH2:  $I_{DS}$ , 2 A / div., 20  $\mu$ s / div.  
 $V_{DS}$  Max = 498 V  
 $I_{DS}$  Max = 8 A  
 $F_{sw}$  = 105 kHz



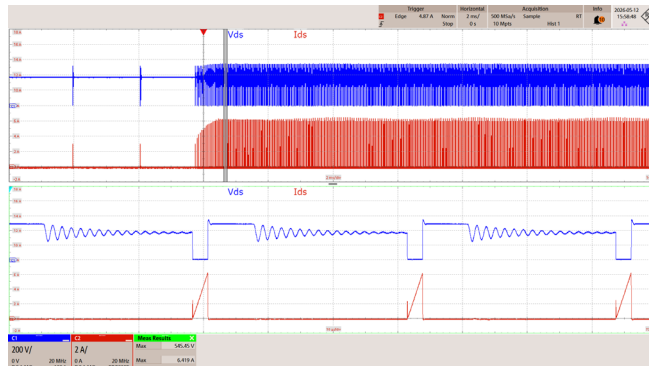
**Figure 42** – 265 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Steady-State Operation

CH1:  $V_{DS}$ , 200 V / div., 5  $\mu$ s / div.  
 CH2:  $I_{DS}$ , 2 A / div., 5  $\mu$ s / div.  
 $V_{DS}$  Max = 601 V  
 $I_{DS}$  Max = 8.08 A  
 $F_{sw}$  = 96.1 kHz

### 13.5.2 Step-Load Transient

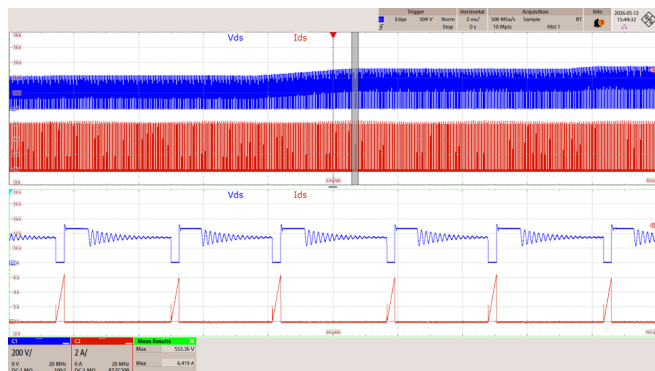


**Figure 43** – 180 VAC, 50 Hz, 0-100% Step Load.  
 CH1:  $V_{DS}$ , 200 V / div., 2 ms / div.  
 CH2:  $I_{DS}$ , 2 A / div., 2 ms / div.  
 Zoom in: 10  $\mu$ s / div.  
 $V_{DS}$  Max = 427 V  
 $I_{DS}$  Max = 6.34 A

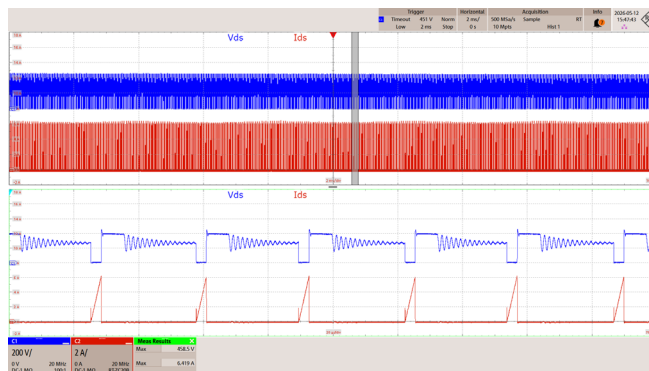


**Figure 44** – 265 VAC, 50 Hz, 0-100% Step Load.  
 CH1:  $V_{DS}$ , 200 V / div., 2 ms / div.  
 CH2:  $I_{DS}$ , 2 A / div., 2 ms / div.  
 Zoom in: 10  $\mu$ s / div.  
 $V_{DS}$  Max = 545 V  
 $I_{DS}$  Max = 6.42 A

### 13.5.3 Input Line Transient

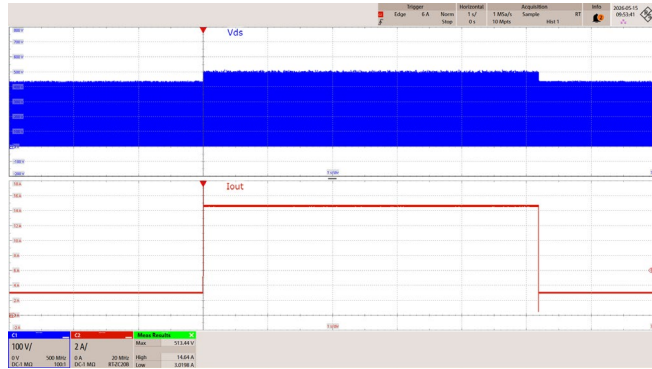


**Figure 45** – 180 VAC – 265 VAC, Step Line Transient.  
 CH1:  $V_{DS}$ , 200 V / div., 2 ms / div.  
 CH2:  $I_{DS}$ , 2 A / div., 2 ms / div.  
 Zoom in: 20  $\mu$ s / div.  
 $V_{DS}$  Max = 553 V  
 $I_{DS}$  Max = 6.42 A

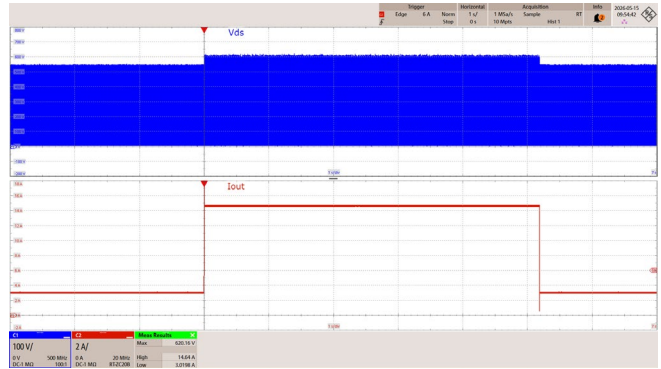


**Figure 46** – 265 VAC – 180 VAC, Step Line Transient.  
 CH1:  $V_{DS}$ , 200 V / div., 2 ms / div.  
 CH2:  $I_{DS}$ , 2 A / div., 2 ms / div.  
 Zoom in: 10  $\mu$ s / div.  
 $V_{DS}$  Max = 458 V  
 $I_{DS}$  Max = 6.42 A

### 13.5.4 Dynamic Peak Power Load Step



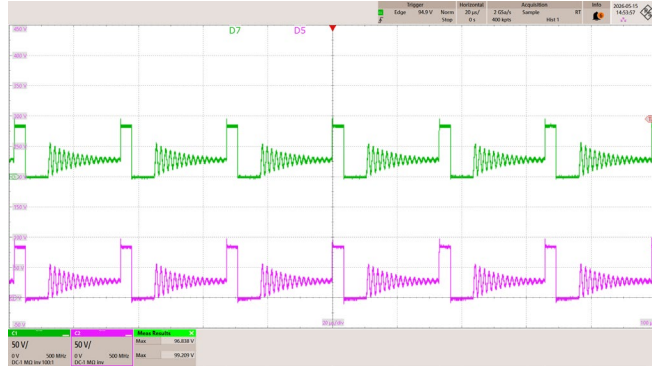
**Figure 47** – 180 VAC, 50 Hz, 28 V Output — Dynamic Load Step: 2.89 A → 15 A (5 s) → 2.89 A  
 CH1:  $V_{DS}$ , 100 V / div., 1 s / div.  
 CH2:  $I_{OUT}$ , 2 A / div., 1 s / div.  
 $V_{DS\ Max} = 513\ V$



**Figure 48** – 265 VAC, 50 Hz, 28 V Output — Dynamic Load Step: 2.89 A → 15 A (5 s) → 2.89 A  
 CH1:  $V_{DS}$ , 100 V / div., 1 s / div.  
 CH2:  $I_{OUT}$ , 2 A / div., 1 s / div.  
 $V_{DS\ Max} = 620\ V$

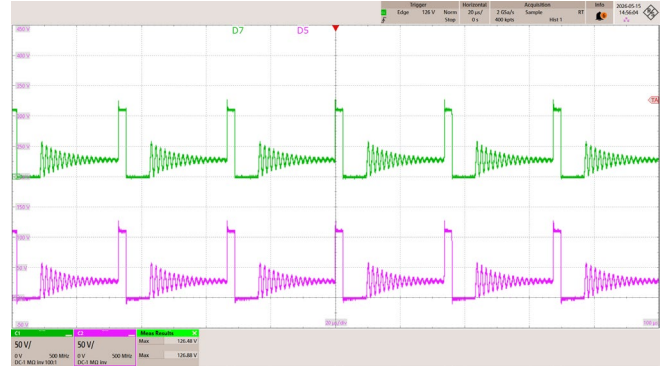
### 13.6 Flyback Output Diode Voltage Stress

#### 13.6.1 Output Diode Voltage Stress at Steady State



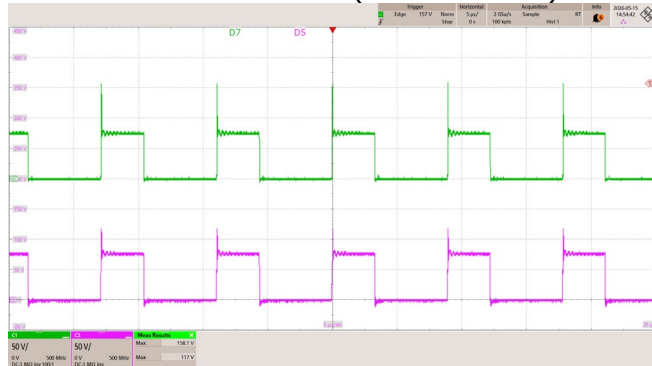
**Figure 49** – 180 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Steady-State Operation.

CH1:  $V_{D7}$ , 50 V / div., 20  $\mu$ s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 20  $\mu$ s / div.  
 $V_{D7}$  Max = 96.8 V (Stress = 48.4%)  
 $V_{D5}$  Max = 99.2 V (Stress = 49.6%)



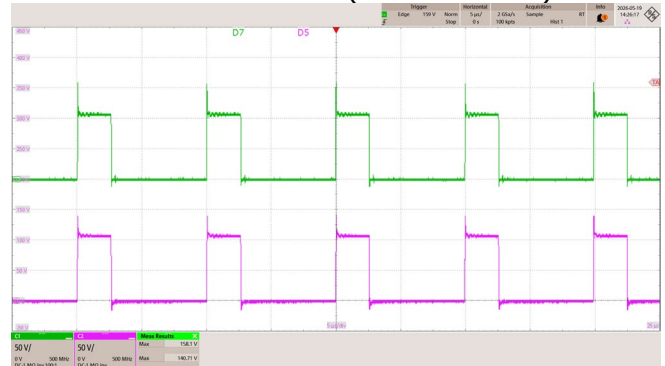
**Figure 50** – 265 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Steady-State Operation.

CH1:  $V_{D7}$ , 50 V / div., 20  $\mu$ s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 20  $\mu$ s / div.  
 $V_{D7}$  Max = 126 V (Stress = 63.2%)  
 $V_{D5}$  Max = 127 V (Stress = 63.4%)



**Figure 51** – 180 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Steady-State Operation.

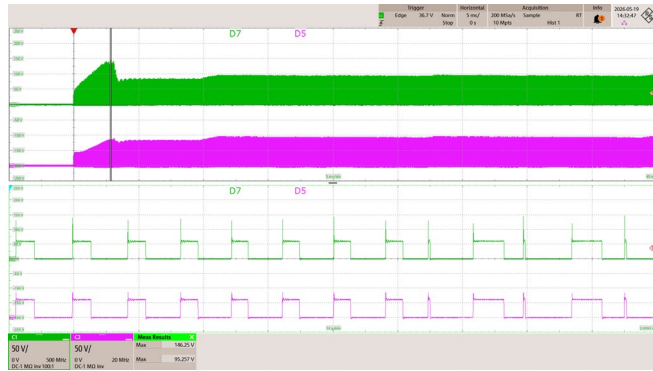
CH1:  $V_{D7}$ , 50 V / div., 5  $\mu$ s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 5  $\mu$ s / div.  
 $V_{D7}$  Max = 158 V (Stress = 79%)  
 $V_{D5}$  Max = 117 V (Stress = 58.5%)



**Figure 52** – 265 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Steady-State Operation.

CH1:  $V_{D7}$ , 50 V / div., 5  $\mu$ s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 5  $\mu$ s / div.  
 $V_{D7}$  Max = 158 V (Stress = 79%)  
 $V_{D5}$  Max = 141 V (Stress = 70.3%)

### 13.6.2 Output Diode Voltage Stress During Start-up Full Load



**Figure 53** – 180 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Start-up Operation.

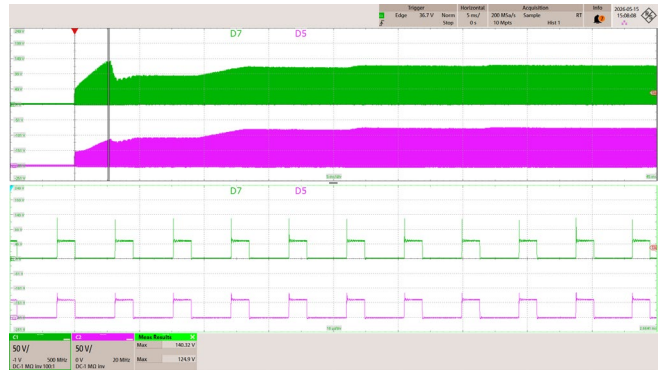
CH1:  $V_{D7}$ , 50 V / div., 5 ms / div.

CH2:  $V_{D5}$ , 50 V / div., 5 ms / div.

Zoom in: 10  $\mu$ s / div.

$V_{D7}$  Max = 146 V (Stress = 73.1%)

$V_{D5}$  Max = 95.2 V (Stress = 47.6%)



**Figure 54** – 265 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Start-up Operation.

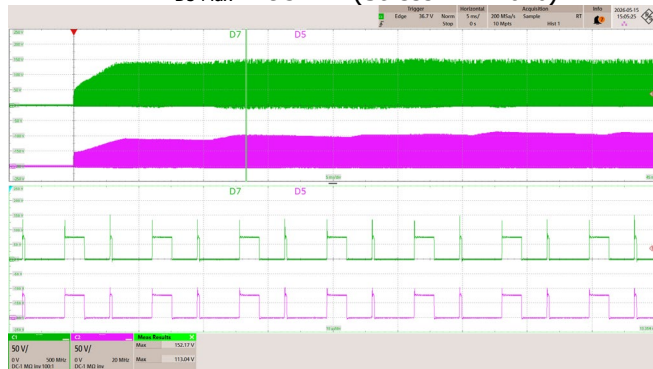
CH1:  $V_{D7}$ , 50 V / div., 20  $\mu$ s / div.

CH2:  $V_{D5}$ , 50 V / div., 20  $\mu$ s / div.

Zoom in: 10  $\mu$ s / div.

$V_{D7}$  Max = 140 V (Stress = 70.1%)

$V_{D5}$  Max = 125 V (Stress = 62.4%)



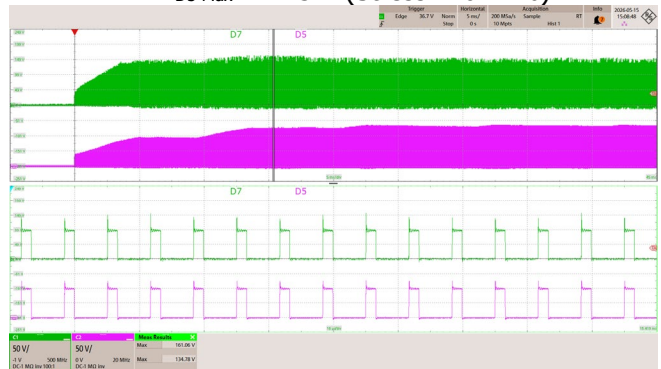
**Figure 55** – 180 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Start-up Operation.

CH1:  $V_{D7}$ , 50 V / div., 5 ms / div.

CH2:  $V_{D5}$ , 50 V / div., 5 ms / div.

$V_{D7}$  Max = 152 V (Stress = 76%)

$V_{D5}$  Max = 113 V (Stress = 56.5%)



**Figure 56** – 265 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Start-up Operation.

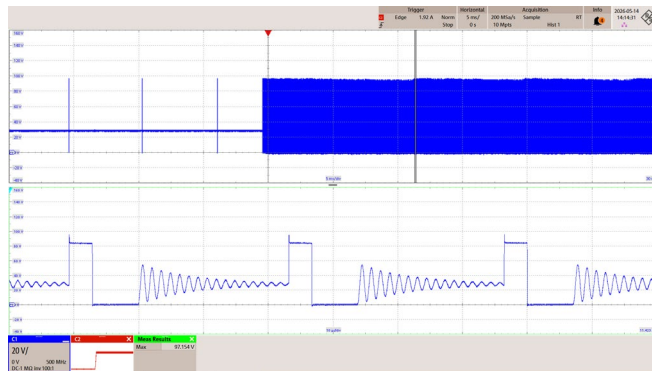
CH1:  $V_{D7}$ , 50 V / div., 5 ms / div.

CH2:  $V_{D5}$ , 50 V / div., 5 ms / div.

$V_{D7}$  Max = 161 V (Stress = 80.5%)

$V_{D5}$  Max = 135 V (Stress = 67.4%)

### 13.6.3 Output Diode Voltage Stress During No Load to Full Load Transient

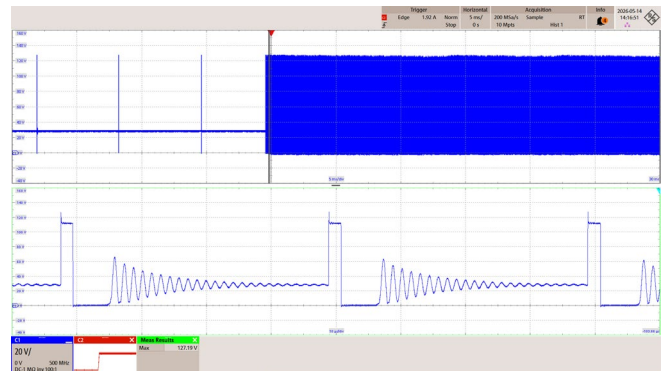


**Figure 57** – D7 at 180 VAC, 50 Hz, No Load to Full Load Transient.

CH1:  $V_{DIODE}$ , 20 V / div., 5 ms / div.

$V_{DIODE Max} = 97.1 V$

Voltage Stress: 48.5%

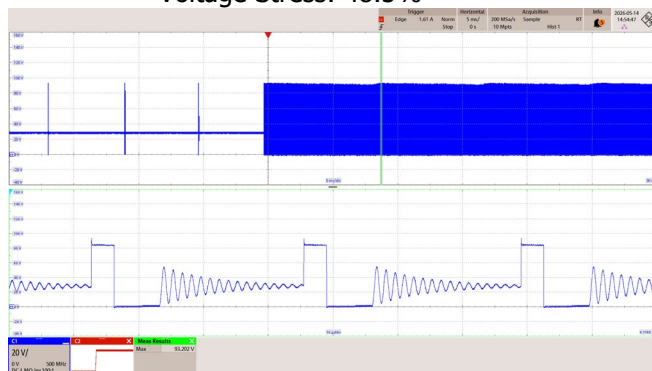


**Figure 58** – D7 at 265 VAC, 50 Hz, No Load to Full Load Transient.

CH1:  $V_{DIODE}$ , 20 V / div., 5 ms / div.

$V_{DIODE Max} = 127 V$

Voltage Stress: 63.6%

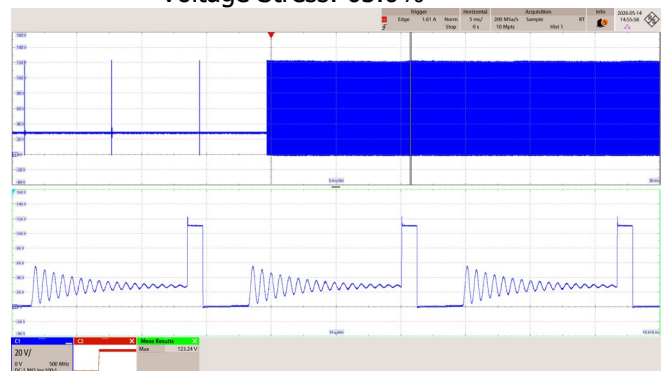


**Figure 59** – D5 at 180 VAC, 50 Hz, No Load to Full Load Transient.

CH1:  $V_{DIODE}$ , 20 V / div., 5 ms / div.

$V_{DIODE Max} = 93.2 V$

Voltage Stress: 46.6%



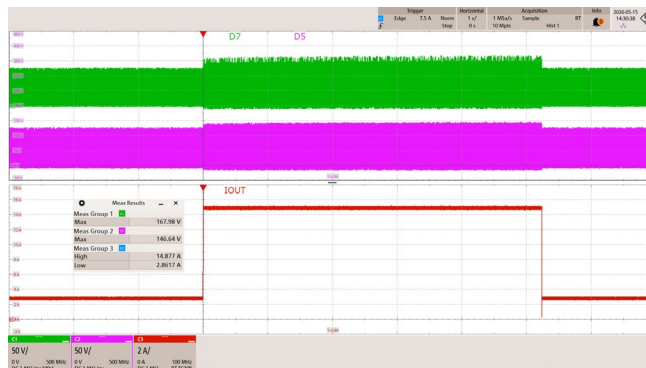
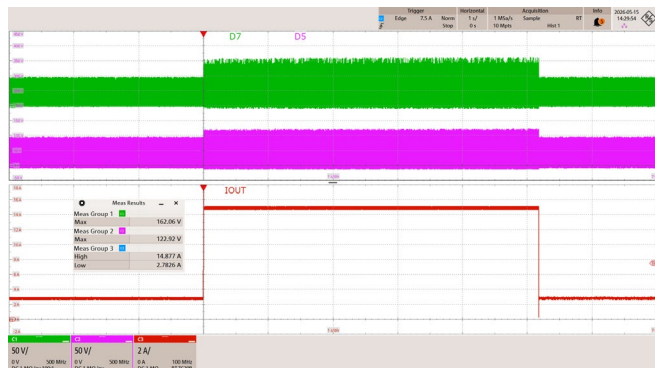
**Figure 60** – D5 at 265 VAC, 50 Hz, No Load to Full Load Transient.

CH1:  $V_{DIODE}$ , 20 V / div., 5 ms / div.

$V_{DIODE Max} = 123 V$

Voltage Stress: 61.6%

### 13.6.4 Output Diode Voltage Stress During Dynamic Peak Power Load Step



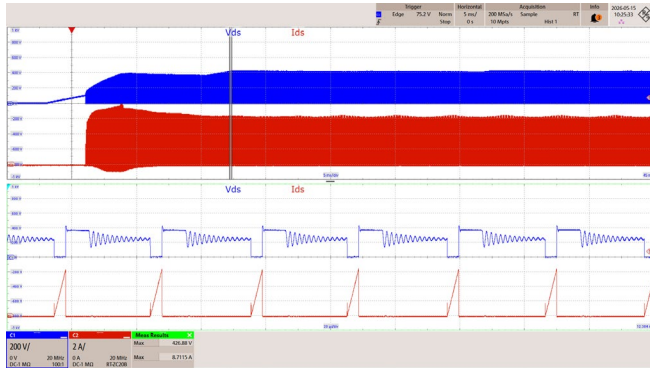
**Figure 61** – 180 VAC, 50 Hz, 28 V Output — Dynamic Load Step: 2.89 A → 15 A (5 s) → 2.89 A

CH1:  $V_{D7}$ , 50 V / div., 1 s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 1 s / div.  
 CH3:  $I_{OUT}$ , 2 A / div., 1 s / div.  
 $V_{D7}$  Max = 162 V (Stress = 81%)  
 $V_{D5}$  Max = 123 V (Stress = 61.4%)

**Figure 62** – 265 VAC, 50 Hz, 28 V Output — Dynamic Load Step: 2.89 A → 15 A (5 s) → 2.89 A

CH1:  $V_{D7}$ , 50 V / div., 1 s / div.  
 CH2:  $V_{D5}$ , 50 V / div., 1 s / div.  
 CH3:  $I_{OUT}$ , 2 A / div., 1 s / div.  
 $V_{D7}$  Max = 168 V (Stress = 83.9%)  
 $V_{D5}$  Max = 146 V (Stress = 73.3%)

### 13.6.5 Start-up Operation



**Figure 63** – 180 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Start-Up Operation

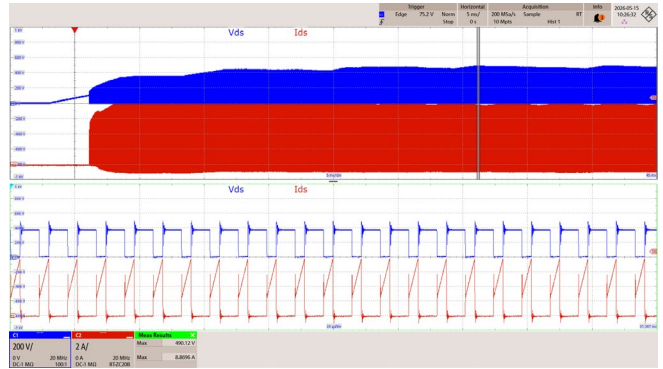
CH1:  $V_{DS}$ , 200 V / div., 5 ms / div.

CH2:  $I_{DS}$ , 2 A / div., 5 ms / div.

Zoom in: 20  $\mu$ s / div.

$V_{DS}$  Max = 427 V

$I_{DS}$  Max = 8.71 A



**Figure 64** – 265 VAC, 50 Hz, 28 V / 2.89 A (Full Load), Start-Up Operation

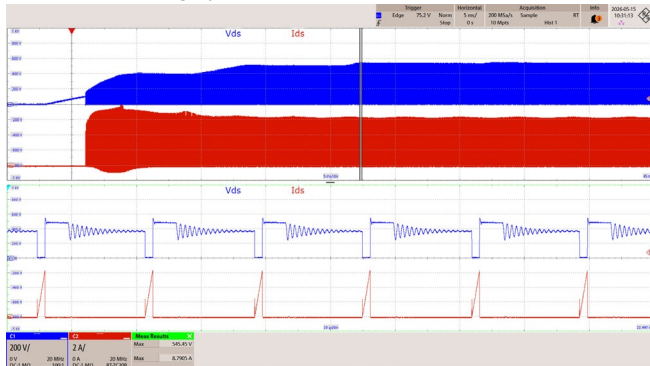
CH1:  $V_{DS}$ , 200 V / div., 5 ms / div.

CH2:  $I_{DS}$ , 2 A / div., 5 ms / div.

Zoom in: 20  $\mu$ s / div.

$V_{DS}$  Max = 490 V

$I_{DS}$  Max = 8.87 A



**Figure 65** – 180 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Start-Up Operation

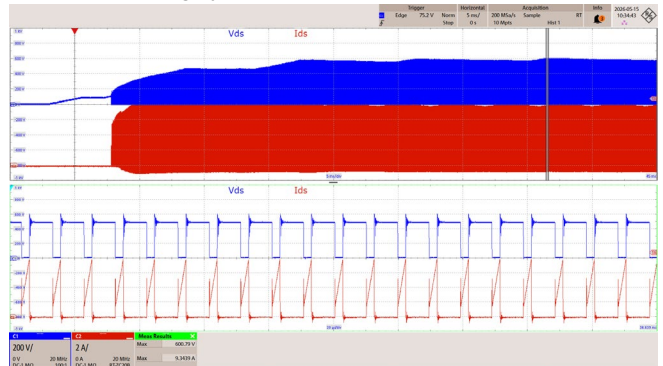
CH1:  $V_{DS}$ , 200 V / div., 5 ms / div.

CH2:  $I_{DS}$ , 2 A / div., 5 ms / div.

Zoom in: 20  $\mu$ s / div.

$V_{DS}$  Max = 545 V

$I_{DS}$  Max = 8.79 A



**Figure 66** – 265 VAC, 50 Hz, 28 V / 15 A (5 s Peak), Start-Up Operation

CH1:  $V_{DS}$ , 200 V / div., 5 ms / div.

CH2:  $I_{DS}$ , 2 A / div., 5 ms / div.

Zoom in: 20  $\mu$ s / div.

$V_{DS}$  Max = 601 V

$I_{DS}$  Max = 9.34 A

## 13.7 Output Voltage Ripple

### 13.7.1 Ripple Voltage Measurement Set-up

Output ripple voltage was measured using a voltage probe with 47  $\mu\text{F}$  electrolytic capacitor and a 100 nF ceramic capacitor connected across the probe tip to reduce periodic and random noise.

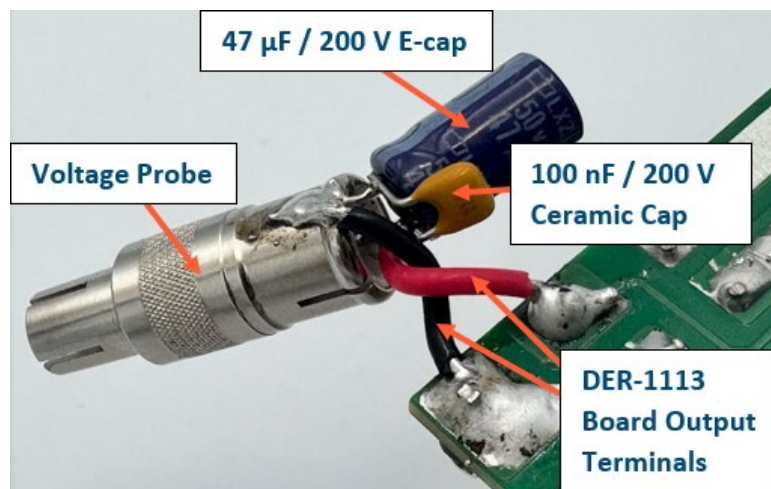


Figure 67 – Ripple Voltage Measurement Set-up Picture.

### 13.7.2 Output Ripple Voltage Waveforms

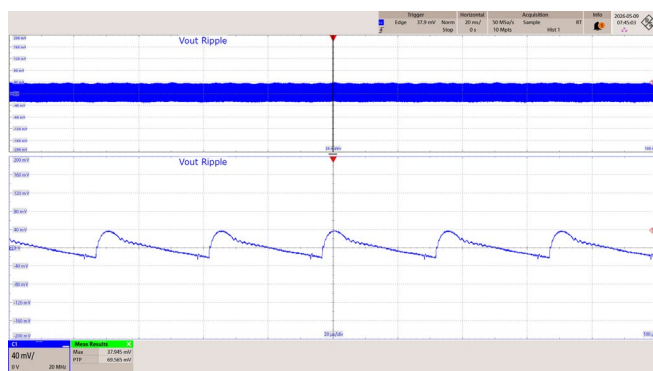


Figure 68 – 180 VAC, 60 Hz,  $I_o = 100\%$  Load.  
 CH1:  $V_{\text{RIPPLE}}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu\text{s}$  / div.  
 $V_{\text{RIPPLE}} = 69.5$  mV pk-pk

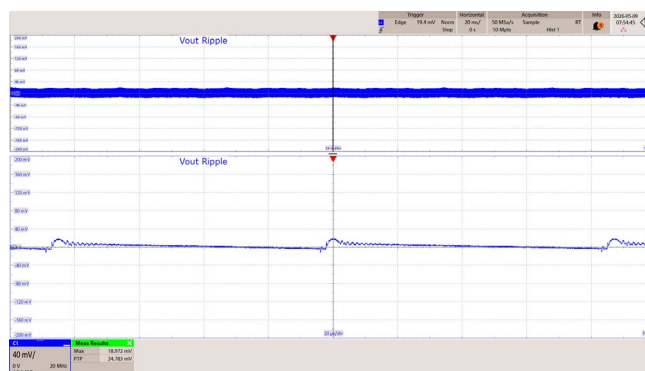
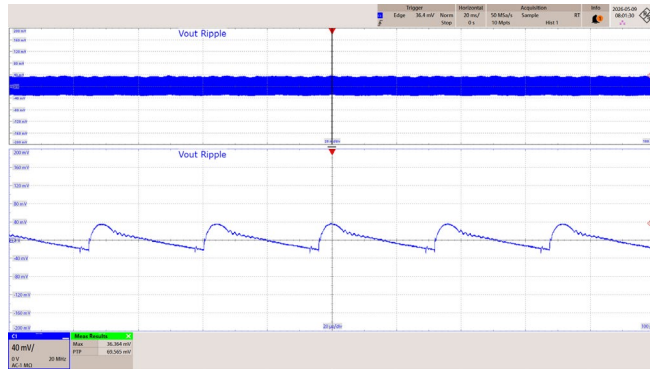
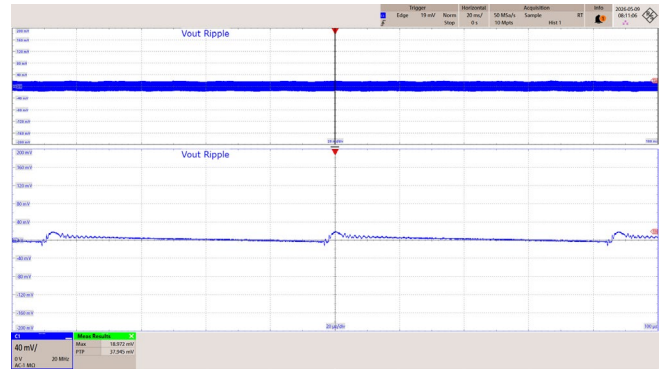


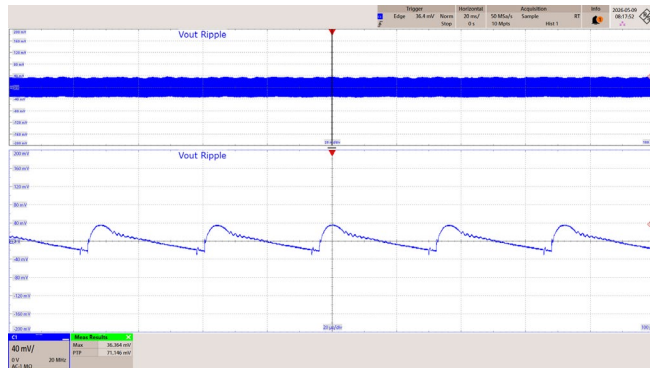
Figure 69 – 180 VAC, 60 Hz,  $I_o = 10\%$  Load.  
 CH1:  $V_{\text{RIPPLE}}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu\text{s}$  / div.  
 $V_{\text{RIPPLE}} = 34.7$  mV pk-pk



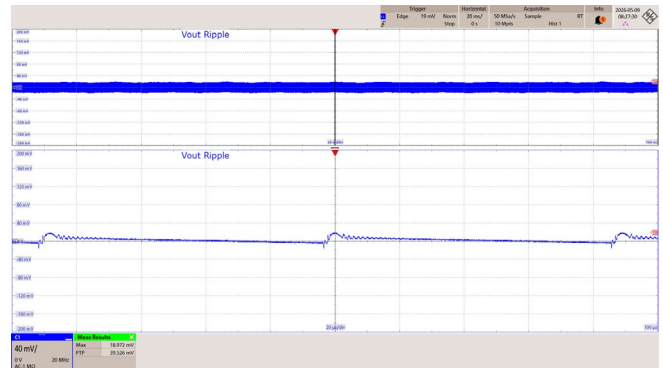
**Figure 70** – 230 VAC, 60 Hz,  $I_o = 100\%$  Load.  
 CH1:  $V_{RIPPLE}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu$ s / div.  
 $V_{RIPPLE} = 69.5$  mV pk-pk



**Figure 71** – 230 VAC, 60 Hz,  $I_o = 10\%$  Load.  
 CH1:  $V_{RIPPLE}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu$ s / div.  
 $V_{RIPPLE} = 37.9$  mV pk-pk



**Figure 72** – 265 VAC, 60 Hz,  $I_o = 100\%$  Load.  
 CH1:  $V_{RIPPLE}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu$ s / div.  
 $V_{RIPPLE} = 71.1$  mV pk-pk

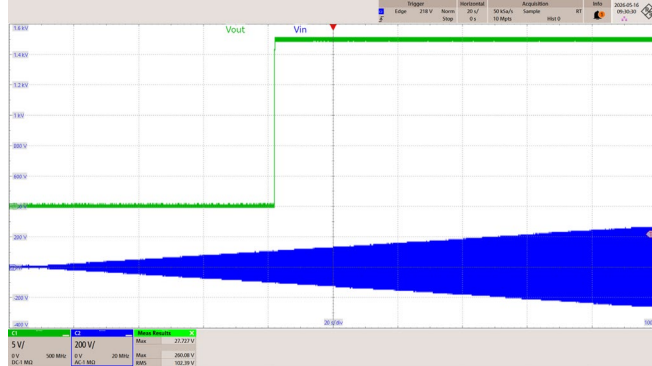


**Figure 73** – 265 VAC, 60 Hz,  $I_o = 10\%$  Load.  
 CH1:  $V_{RIPPLE}$ , 40 mV / div., 20 ms / div.  
 Zoom In: 20  $\mu$ s / div.  
 $V_{RIPPLE} = 39.5$  mV pk-pk

### 13.8 Brown-in /Brown-out Test

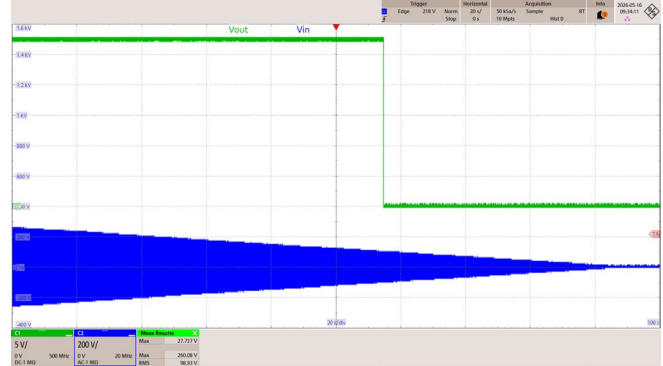
#### 13.8.1 Brown-in /Brown-out Test

No overheating or component damage was observed during brown-in and brown-out testing.



**Figure 74** – Brown in, 0 - 180 VAC, 1 V/s, Vo = 28 V, Io = 2.89 A.

CH1: V<sub>OUT</sub>, 5 V / div., 20 s / div.  
 CH2: V<sub>IN</sub>, 200 V / div., 20 s / div.



**Figure 75** – Brown out, 180 - 0 VAC, 1 V / s, Vo = 28 V, Io = 2.89 A.

CH1: V<sub>OUT</sub>, 5 V / div., 20 s / div.  
 CH2: V<sub>IN</sub>, 200 V / div., 20 s / div.

## 14 Conducted EMI

Conducted emissions test were performed at 230 VAC using a 9.69 Ω fix resistor load.

### 14.1 Test Set-up

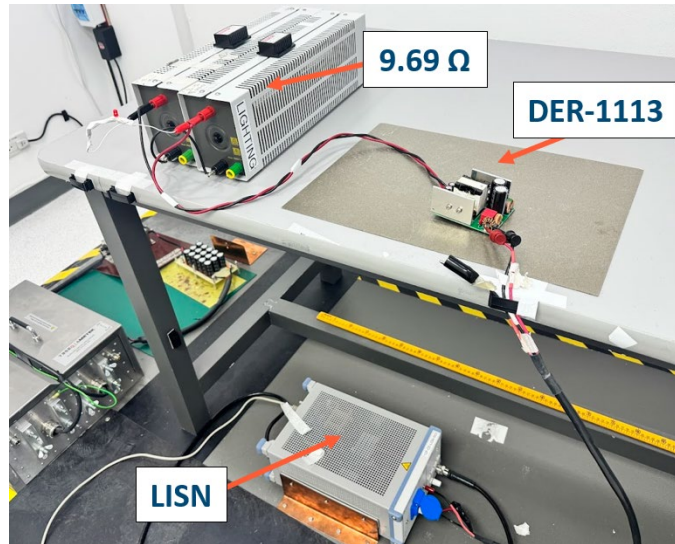


Figure 76 – Conducted EMI Test Set-up.

### 14.2 Conducted EMI Scan

The unit passed EN 55022 Class B with > 6 dB margin on the line / neutral

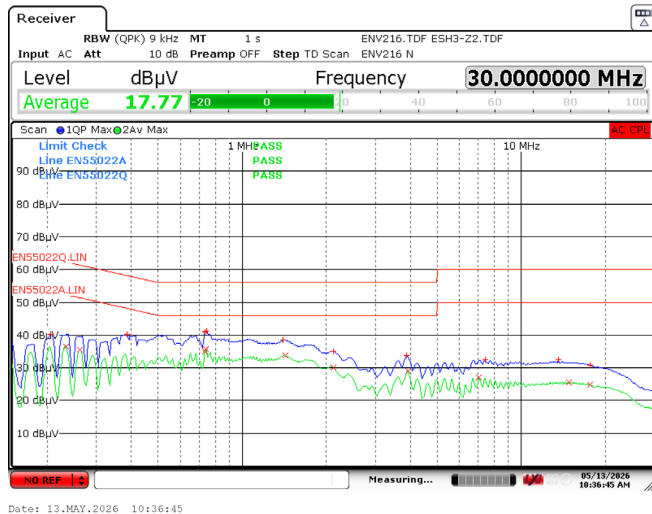


Figure 77 – Conducted EMI Scan.

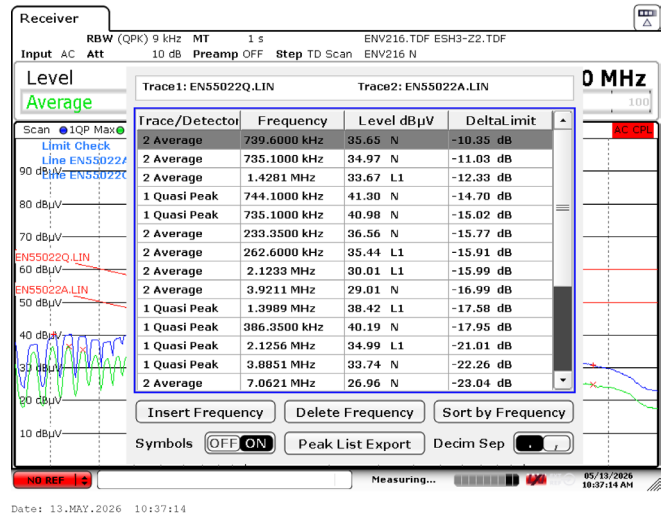


Figure 78 – Conducted EMI Test Data.

### 15 Line Surge Immunity

The unit was powered up at a 230V input and subjected to ±2000V ring wave, and combination-wave, with 10 strikes applied for each condition.

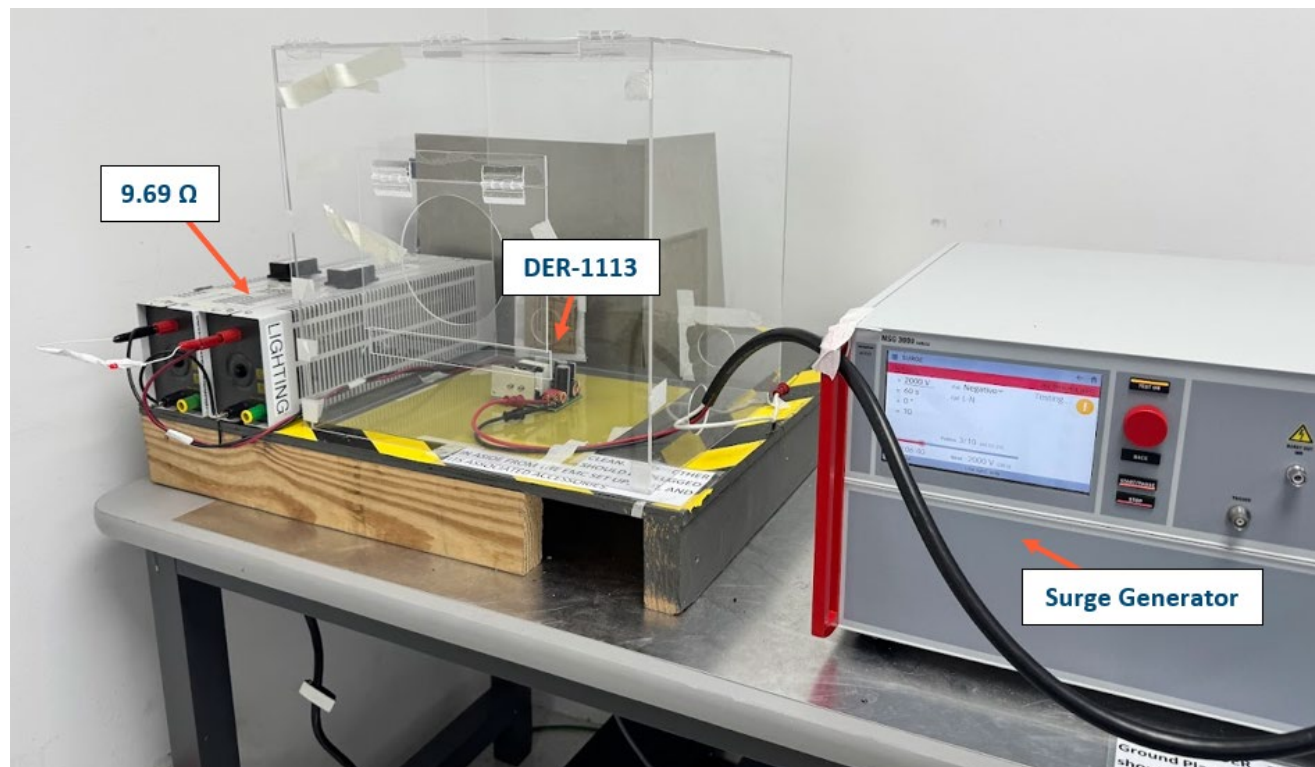


Figure 79 – Surge Immunity Test Set-up.

#### 15.1 Combination Wave Differential Mode Surge

The unit passed the 2 kV differential surge test with no auto restart (AR), no output interruption, and no damaged components observed.

AC Input Voltage (VAC)	Surge Voltage (kV)	Coupling	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2000	L to N	0	2	10	Pass – No AR
230	-2000	L to N	0	2	10	Pass – No AR
230	+2000	L to N	90	2	10	Pass – No AR
230	-2000	L to N	90	2	10	Pass – No AR
230	+2000	L to N	270	2	10	Pass – No AR
230	-2000	L to N	270	2	10	Pass – No AR

Table 14 – Combination Wave Differential Mode Surge.

## 15.2 Ring Wave Surge

The unit passed the 2 kV ring-wave surge test in both differential-mode and common-mode setups, with no auto restart (AR), no output interruption, and no component damage..

### 15.2.1 Ring Wave Differential Mode

AC Input Voltage (VAC)	Surge Voltage (kV)	Coupling	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2000	L to N	0	12	10	Pass – No AR
230	-2000	L to N	0	12	10	Pass – No AR
230	+2000	L to N	90	12	10	Pass – No AR
230	-2000	L to N	90	12	10	Pass – No AR
230	+2000	L to N	270	12	10	Pass – No AR
230	-2000	L to N	270	12	10	Pass – No AR

**Table 15** – Ring Wave Surge-Differential Mode Test Results.

**16 Revision History**

<b>Date</b>	<b>Author</b>	<b>Revision</b>	<b>Description &amp; Changes</b>	<b>Reviewed</b>
06-June-26	CMC	A	Initial Release.	Apps & Mktg



For the latest updates, visit our website: [www.power.com](http://www.power.com)

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.



<https://www.power.com/company/sales/sales-offices>

