Design Example Report

Title	**20 W Low-Profile Dual-Output Flyback Converter Using the 1700 V InnoMux2-EP IC IMX2353F-H418**
Specification	200 VDC – 1000 VDC Input; 16 V / 350 mA Unregulated Output; 24 V / 600 mA Regulated Output
Application	Industrial and Sports Lighting
Author	Applications Engineering Department
Document Number	DER-1104
Date	April 29, 2026
Revision	A

Summary and Features

- Ultra-wide operating voltage range: 200 VDC to 1000 VDC
- Supports high ambient applications: up to 105 °C
- >90% full-load efficiency at 500 VDC input
  - Zero Voltage switching (ZVS)
  - 1700 V PowiGaN™ primary switch
  - Synchronous rectification (SR)
- Low-profile design: 13 mm high
- Very low component count: fewer than 50 parts
- Accurate secondary-side regulation – better than ±1% across line and load
- Safety features
  - Output overvoltage protection (OVP)
  - Accurate thermal protection with wide hysteresis
  - Open SR-FET gate detection
  - LED short/open protection

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Table of Contents

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a dual-output 20 W power supply intended for industrial and sports lighting applications. The design utilizes an IMX2353F-H418 IC from the InnoMux™2-EP family.

The SMPS features two outputs with a combined maximum output power of 20 W. Output 1 delivers an unregulated primary-side 16 V / 350 mA output, while output 2 delivers a regulated secondary-side 24 V / 600 mA constant-voltage (CV) output. This design demonstrates high efficiency, low-profile, wide temperature range and accurate secondary-side output regulation, made possible from the adaptive ZVS switching algorithm employed in InnoMux-2 ICs.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

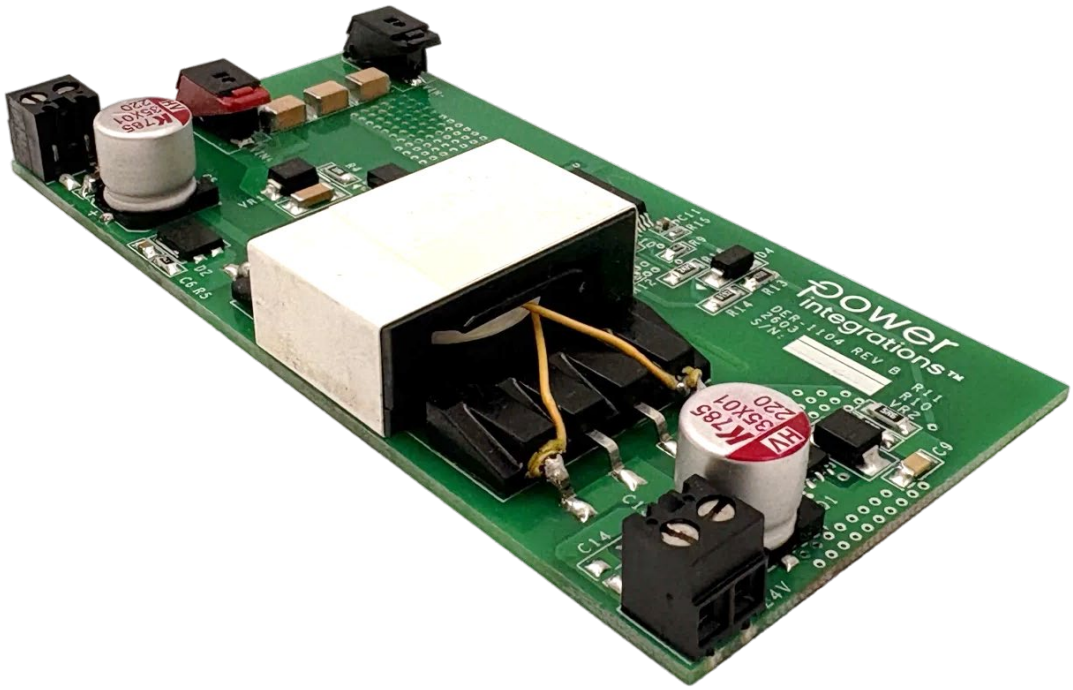


Figure 1 – Populated Circuit Board.

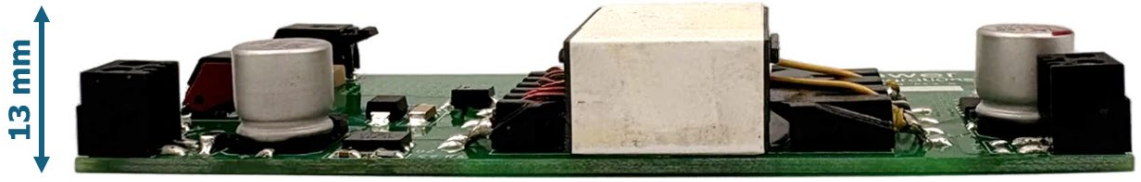


Figure 2 – Populated Circuit Board, Side View.

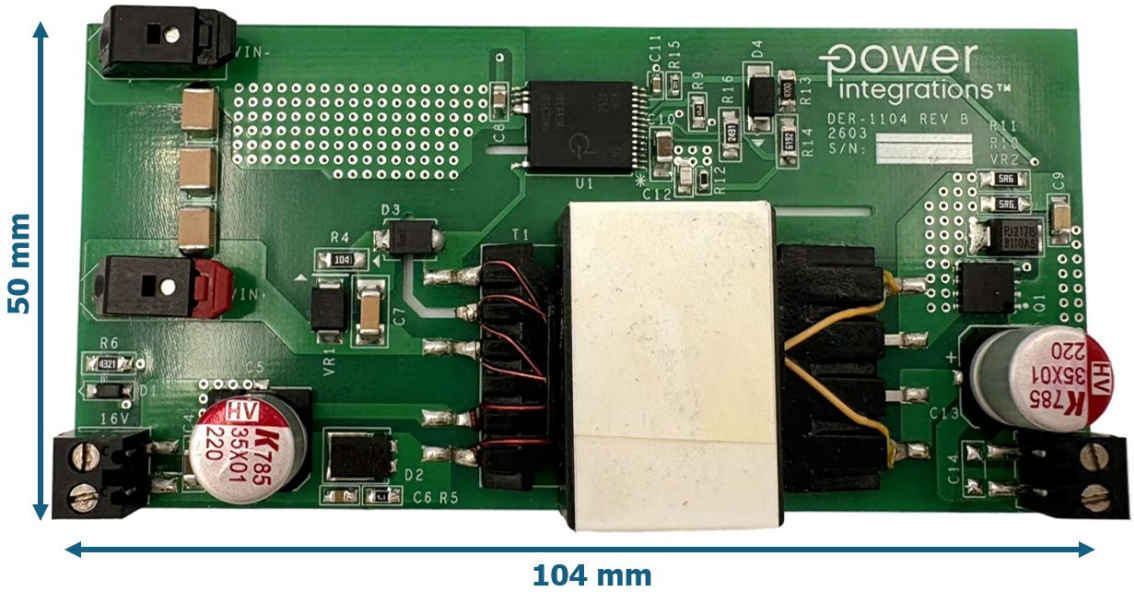


Figure 3 – Populated Circuit Board, Top View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	**V_{IN}**	200		1000	VDC	
Output						
Regulated Output						
Rated Voltage	**24 V_{OUT}**		24.0		V	±1% initial set point tolerance
Line and Load Regulation	**24 V_{REG}**		±1%			Measured from 200 to 1000 VDC, 0% to 100% load
Dynamic Response			±3%			10-100% load step
Ripple Voltage	**24 V_{RIPPLE}**			840	mVpp	20 MHz Bandwidth, at 25 °C Ambient
Rated Current	**24 V I_{OUT}**		600		mA	
Unregulated Output						
Rated Voltage	**16 V_{OUT}**		16.0		V	
Line and Load Regulation	**16 V_{REG}**	-15		+15	%	With minimum load of 60 mA
Dynamic Response		-12		+15	%	10-100% load step
Ripple Voltage	**16 V_{RIPPLE}**			800	mVpp	20 MHz Bandwidth, at 25 °C Ambient
Rated Current	**16 V I_{OUT}**		350		mA	
Total Output Power						
Output Power	**P_{OUT}**		20		W	200 – 1000 VDC input
Efficiency						
Full Load	η		85	85.5	%	Measured at 1000 VDC, 25 °C
			87	87.5	%	Measured at 800 VDC, 25 °C
			90	90.5	%	Measured at 500 VDC, 25 °C
			91	91.9	%	Measured at 200 VDC, 25 °C
Standby Input Power				<0.5	W	Measured at 800 VDC, 25 °C, 24 V 200 mW
Environmental						
Ambient Temperature	**T_{AMB}**	0		105	°C	Free Convection, Sea Level.

Table 1 – Power Supply Specifications.

3 Schematic

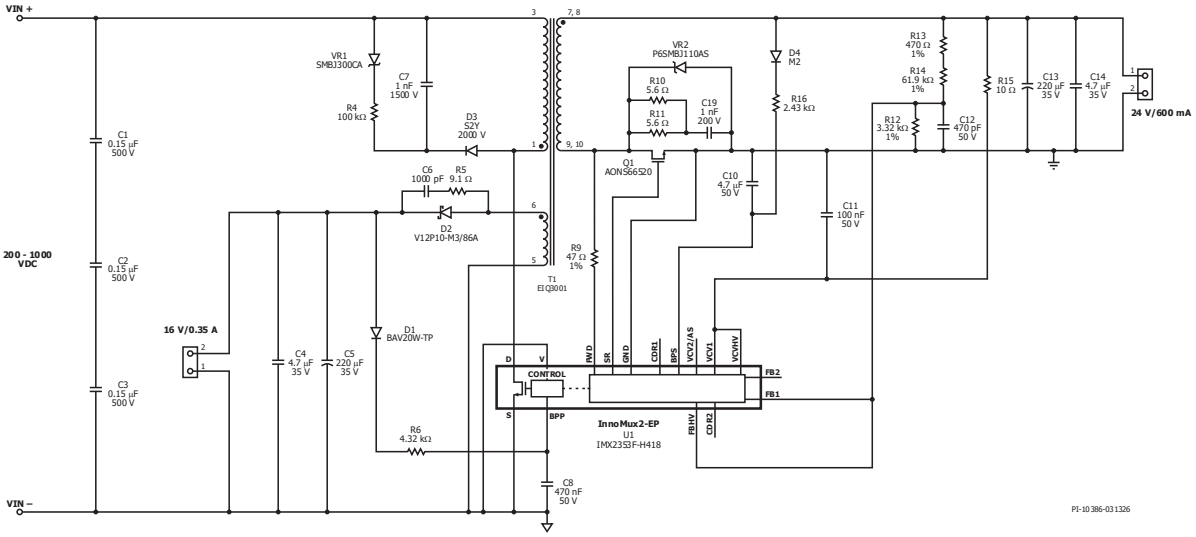


Figure 4 – Full Schematic.

4 Circuit Description

4.1 Primary-Side

4.1.1 Input Capacitor

The series-stacked capacitors C1, C2 and C3 are connected across the DC input and provide filtering input to reduce input ripple.

4.1.2 Primary Switching Circuit

The primary side of the transformer is connected between the input DC bus (T1, pin 3) and the drain of the integrated primary switch of the InnoMux2-EP IC (U1, pin 28). The primary current loop closes at the negative terminal of C8 via the S pin of U1 (pin 18/19). An RCD-type primary clamp (D3, C7, R4, and VR1) is used to limit the peak drain voltage spike on the integrated primary switch, which is caused by the leakage inductance of the transformer when the switch turns off.

4.1.3 Primary-Side Controller Power Source

The primary-side controller is integrated into the InnoMux2-EP IC (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor (C8) when DC voltage is first applied to the converter input. During normal operation (steady-state), the primary-side controller is powered from auxiliary winding on the primary side of the main transformer. This winding provides power for both the controller bias and the 16 V output. The voltage across the auxiliary winding is rectified by diode D2 and filtered by capacitors C4 and C5. The RC snubber network consisting of R5 and C6 serves to damp high-frequency ringing across the rectifier diode (D2). Regulation of the 16 V output requires good coupling to the 24 V output. The rectified and filtered 16 V supply is connected to the BPP pin via a blocking diode D1 and current-limiting resistor, R6.

4.1.4 Primary Peak Current Limit

The value of capacitor C8 is used to set the maximum primary current to either STANDARD or INCREASED level. In this case, a 470 nF capacitor sets the primary-side controller peak current limit to its STANDARD level of 1.85 A.

4.2 Secondary-Side

The secondary side of the InnoMux2-EP IC (U1) is powered from an internal regulator connected to the BPS pin (U1, pin 6). During startup, power for the BPS regulator is provided by the FORWARD pin (U1, pin 10). Capacitor C10 is a decoupling capacitor.

4.2.1 InnoMux2-EP Pin Configuration for 1CV Application

The InnoMux2-EP IC can also be used for single output applications using the same parts intended for multi-output power supplies. To accomplish this, the pin connection configuration shown in Table 2 should be implemented.

Pin Number	Pin Name	Connection
1	FB1	Connected to FBHV
3	FB2	Left floating
5	CDR1	Left floating
8	FBHV	Connected to FB1
11	VCV1	Connected to VCHV
12	VCV2/AS	Left floating
13	VCVHV	Connected to VCV1

Table 2 – InnoMux2-EP Pinout for 1 CV Application.

4.2.2 Primary-Side to Secondary-Side Communication

The secondary side of the InnoMux2-EP IC (U1) instructs the primary-side controller to initiate a switching cycle via the internal safety-isolated FluxLink™ communication channel.

4.2.3 InnoMux2-EP Power Supply

As the 24 V output approaches regulation at the end of the startup sequence, it will take over supplying the secondary side controller in U1 via resistor R15. A local decoupling capacitor, C11, is connected close to the VCVHV/VCV1 pin of U1. Resistor R15 and capacitor C11 provide local decoupling and ESD protection.

In steady-state operation, the secondary side is powered from the 24 V output via blocking diode (D4) and current-limiting resistor (R16). Supplying the BPS pin from the 24 V output reduces power consumption by the BPS regulator reducing thermal stress. This approach is implemented to improve thermal performance, as the power supply is designed to operate in an ambient temperature of up to 105 °C.

4.2.4 Synchronous Rectifier (SR) MOSFET Drive

The SR pin drives the synchronous rectifier (SR) MOSFET (Q1) when the transformer is delivering energy to the secondary circuit. Before the end of secondary discharge, the gate voltage of the SR MOSFET is reduced to maintain a fixed source-to-drain voltage across the SR MOSFET. This prevents the premature turn-off of the SR MOSFET.
In DCM operation, the SR MOSFET (Q1) is turned on for a short period just before the primary switch turns on. This action generates a reverse current in the CV1 secondary winding, which commutates to cause a reverse current flow in the transformer on the primary side. This reverse current discharges the voltage across the primary switch, allowing it to turn on at zero (or near zero) voltage. This mechanism, termed SR-ZVS, substantially minimizes switching loss, significantly reducing the turn-on loss for the primary switch, especially with high input voltage. The timing and duration of the ZVS conduction pulse applied to via the secondary side SR FET is automatically adjusted by the secondary controller in the InnoMux-2 IC.

4.2.5 Output Control

Output rectification for the CV1 output is provided by the SR MOSFET (Q1). The use of low-ESR capacitor C13 minimizes output voltage ripple. A multilayer ceramic capacitor (MLCC), C14, is connected across the CV1 output terminals to provide a low-impedance bypass path for any high-frequency noise.

The RC snubber network consisting of R11, R10 and C19 serves to damp high-frequency ringing across the SR MOSFET (Q1). This ringing results from the oscillation of transformer leakage inductance and secondary trace inductance with the MOSFET body capacitance.

The output voltage on CV1 is controlled by R13, R14, R12 and C12, which provide an analog current signal to FB1/FB2 (U1, pin 1 and pin 8).

5 PCB Layout

Layers: Two (2)
Board Material: FR-4
Board Thickness: 1.6 mm
Copper Thickness: 2 oz

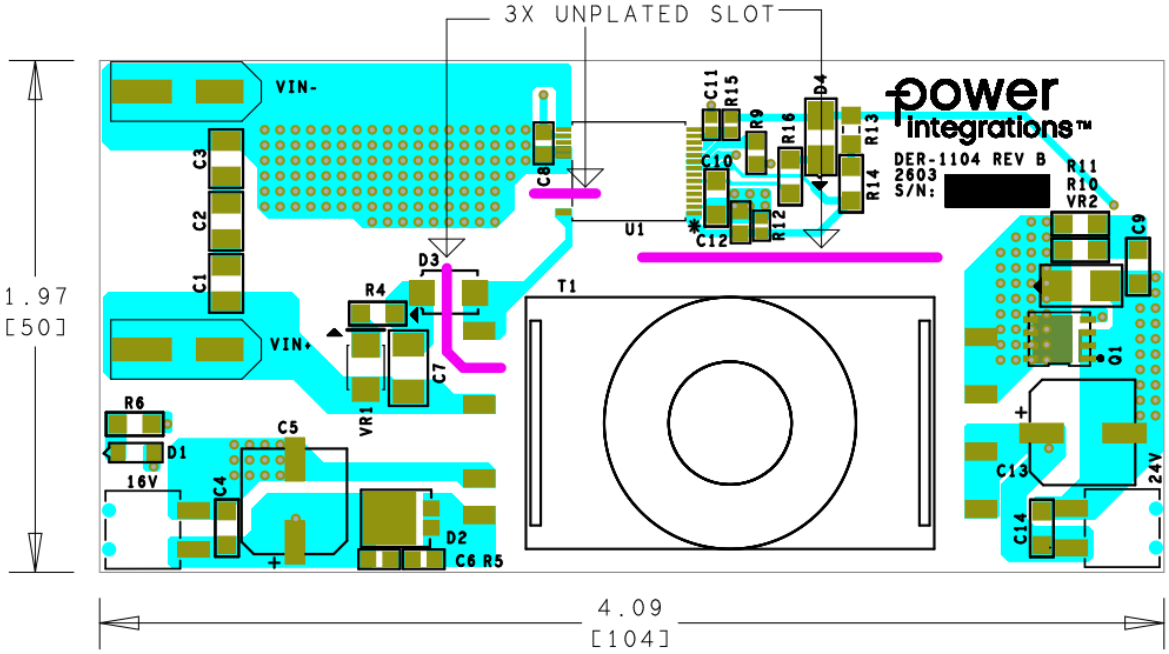


Figure 5 – Printed Circuit Board Layout, Top.

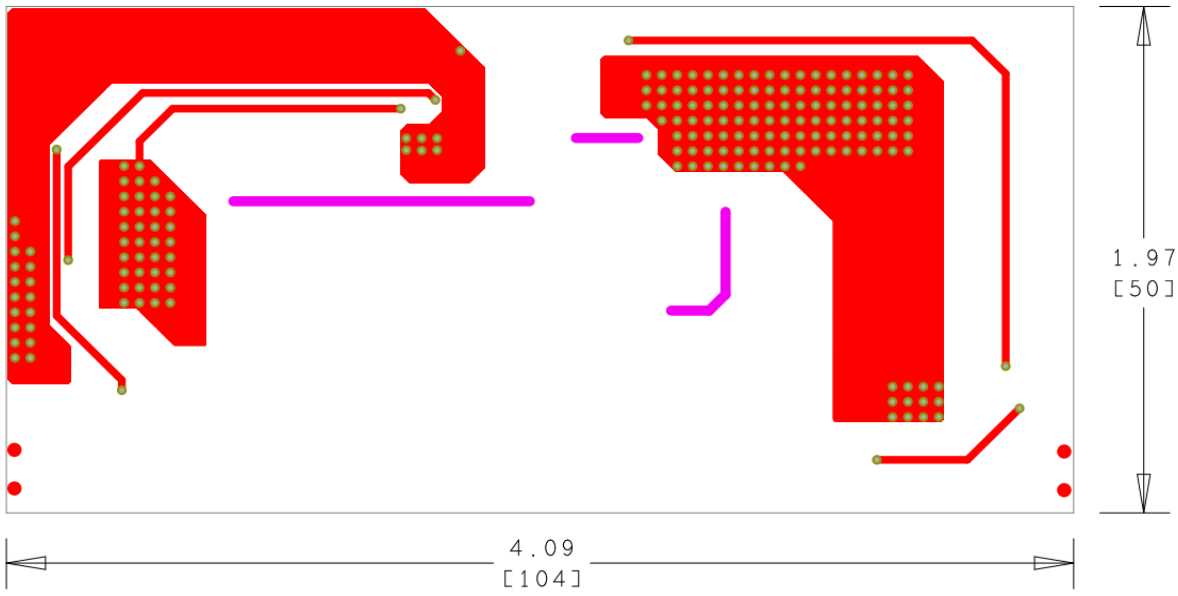


Figure 6 – Printed Circuit Board Layout, Bottom.

6 Bill of Materials

6.1 Electrical BOM

Item	Ref Des.	Qty	Description	Mfr. Part Number	Manufacturer
1	C1 C2 C3	3	0.15 μF, ±10%, 500 V, Ceramic Capacitor X7R, 1210 (3225 Metric), AEC-Q200, Automotive, Boardflex Sensitive	C1210X154KCRACAUTO	Kemet
2	C4 C14	2	4.7 μF, 35 V, Ceramic, X5R, 1206	C3216X5R1V475M085AB	Taiyo Yuden
3	C5 C13	2	220 μF, ±20%, 35 V, Aluminum - Polymer Capacitors, Radial, Can - SMD, 23 mOhm 1000 Hrs @ 150 °C	A785MN227M1VLAS023	KEMET
4	C6	1	1000 pF, ±10%, 100 V, Ceramic Capacitor X7R 0805 (2012 Metric)	CL21B102KC6WPNC	Samsung Electro-Mechanics
5	C7	1	1 nF, 1500 V, Ceramic, X7R, 1808	1808SC102KAT1A	AVX
6	C8	1	470 nF, ±10%, 50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung Electro-Mechanics
7	C9	1	1 nF, 200 V, 10%, Ceramic, X7R, 1206	12062C102KAT2A	AVX Corp
8	C10	1	4.7 μF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
9	C11	1	0.1 μF (100 nF), ±10%, 50 V, Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
10	C12	1	470 pF, ±5%, 50 V, Ceramic Capacitor C0G, NP0, 0805 (2012 Metric)	C0805C471J5GACAUTO	KEMET
11	D1	1	150 V, 0.2 A, SOD-123	BAV20W-TP	Micro Commercial Co
12	D2	1	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay/General Semi
13	D3	1	Diode, 2000 V, 2A, Surface Mount DO-214AA (SMB)	S2Y	Diotec Semiconductor
14	D4	1	Diode, 100 V, 1A, Surface Mount DO-214AC (SMA)	M2	Diotec Semiconductor
15	Q1	1	MOSFET, N-Channel, 150 V 17 A (Ta), 100 A (Tc) 6.2 W (Ta), 215 W (Tc) Surface Mount 8-DFN (5 x 6) N-Channel 150 V 17 A (Ta), 100 A (Tc) 6.2 W (Ta), 215 W (Tc) Surface Mount 8-DFN (5 x 6)	AONS66520	Alpha & Omega Semiconductor
16	R4	1	RES, 100 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J104V	Panasonic
17	R5	1	RES, 9.1 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ9R1V	Panasonic
18	R6	1	RES, 4.32 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4321V	Panasonic
19	R9	1	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
20	R10 R11	2	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
21	R12	1	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
22	R13	1	RES, 470 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	CRGCQ1206F470R	Vishay Dale
23	R14	1	RES, 61.9 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF6192V	Panasonic
24	R15	1	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
25	R16	1	RES, 2.43 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2431V	Panasonic
26	T1	1	TRANS EIQ3001, 10 pins	MCT-EIQ3001	Hefei Mycoil Technology Co., LTD
27	U1	1	InnoMux2-EP, IMX2353F, 1700 V, InSOP-T28G (F)	IMX2353F	Power Integrations
28	VR1	1	486 V Clamp 1.3 A Ipp Tvs Diode Surface Mount DO-214AA (SMBJ)	SMBJ300CA	Littelfuse
29	VR2	1	TRANSIENT VOLTAGE SUPPRESSOR, 177 V Clamp, 3.4 A Ipp, Tvs Diode, Surface Mount SMB (DO-214AA)	P6SMBJ110AS_R1_00001	Panjit International Inc.

6.2 Mechanical BOM

Item	Ref Des.	Qty	Description	Mfr. Part Number	Manufacturer
1	16V 24V	2	2 Position Wire to Board Terminal Block, Horizontal with Board, 0.150" (3.81 mm), Surface Mount	2383945-2	TE Connectivity AMP Connectors
2	VIN+	1	1 Position Wire to Board Terminal Block, Horizontal with Board, Surface Mount, RED	SM99S01VBNN04G7	METZ CONNECT USA Inc.
3	VIN-	1	1 Position Wire to Board Terminal Block, Horizontal with Board, Surface Mount, WHITE	SM99S01VBNN01G7	METZ CONNECT USA Inc.

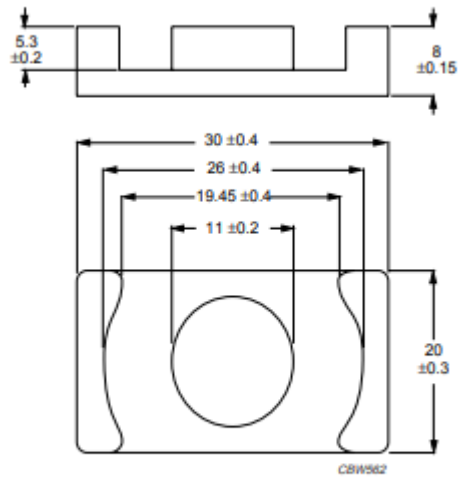
7 Transformer (T1) Specification

7.1 Core Information

CORES

Effective core parameters of a set of EQ cores

SYMBOL	PARAMETER	VALUE	UNIT
Σ(l/A)	core factor (C1)	0.426	mm^{-1}
V_e	effective volume	4970	mm^3
l_e	effective length	46.0	mm
A_e	effective area	108	mm^2
A_{min}	minimum area	95.0	mm^2
m	mass of core half	≈ 13.2	g



Dimensions in mm.

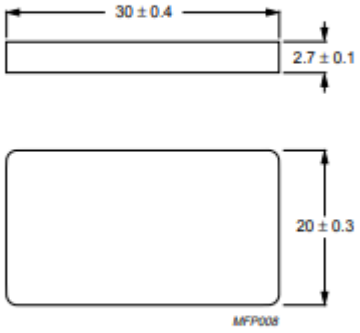
Fig.1 EQ30 core.

Effective core parameters of an EQ/PLT combination

SYMBOL	PARAMETER	VALUE	UNIT
Σ(l/A)	core factor (C1)	0.335	mm^{-1}
V_e	effective volume	3910	mm^3
l_e	effective length	36.2	mm
A_e	effective area	108	mm^2
A_{min}	minimum area	95.0	mm^2
m	mass of plate	≈ 7.6	g

Ordering information for plates

GRADE	TYPE NUMBER
3C94	PLT30/20/3-3C94
3C95 des	PLT30/20/3-3C95
3C96 des	PLT30/20/3-3C96
3F35 des	PLT30/20/3-3F35
3F4 des	PLT30/20/3-3F4
3F45 prot	PLT30/20/3-3F45



Dimensions in mm.

Fig.2 PLT30/20/3.

Figure 7 – EQ30 and PLT30/20/3 Core Information.

7.2 Bobbin Information

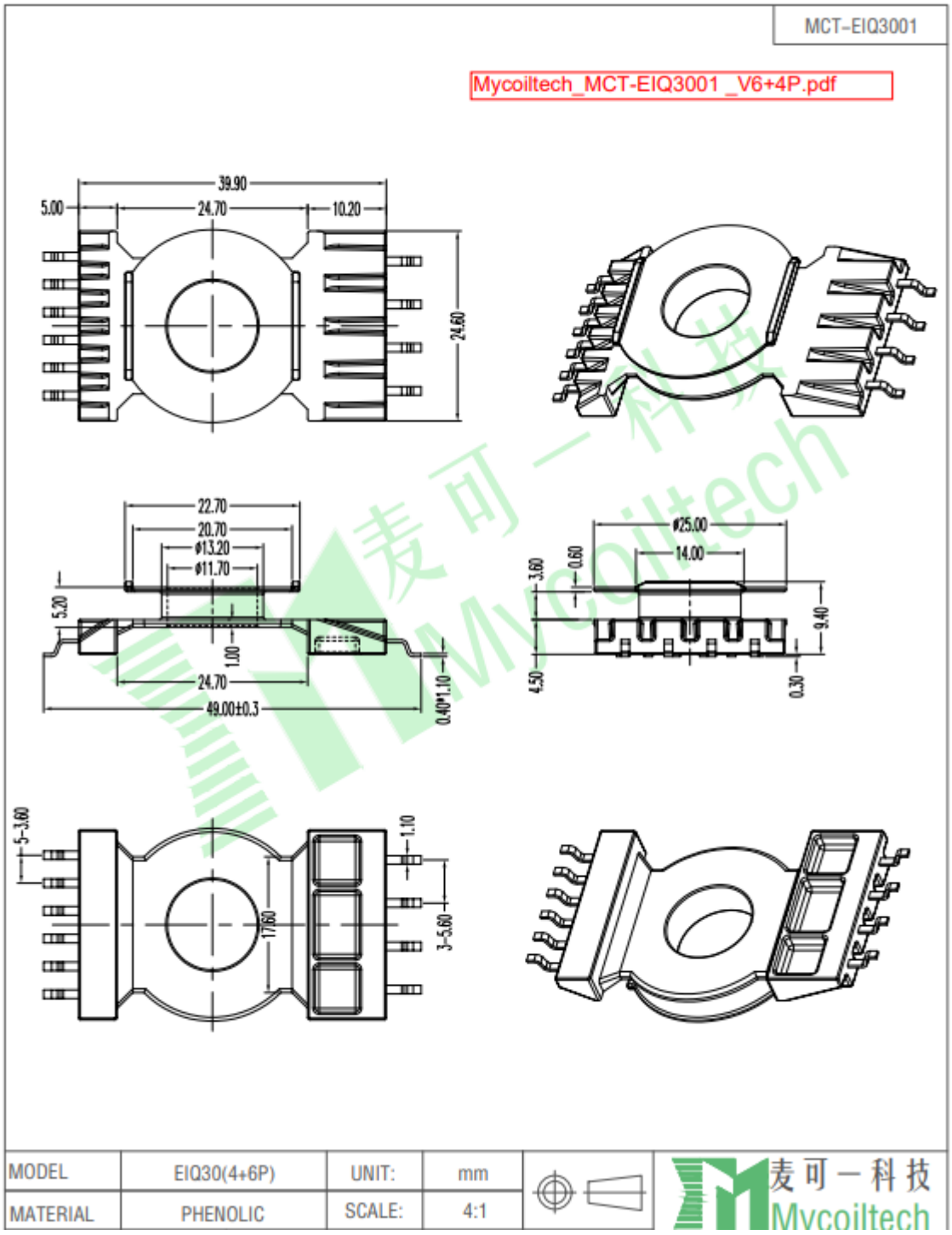


Figure 8 – EIQ30 (4+6P) Bobbin Information.

7.3 Transformer Electrical Diagram

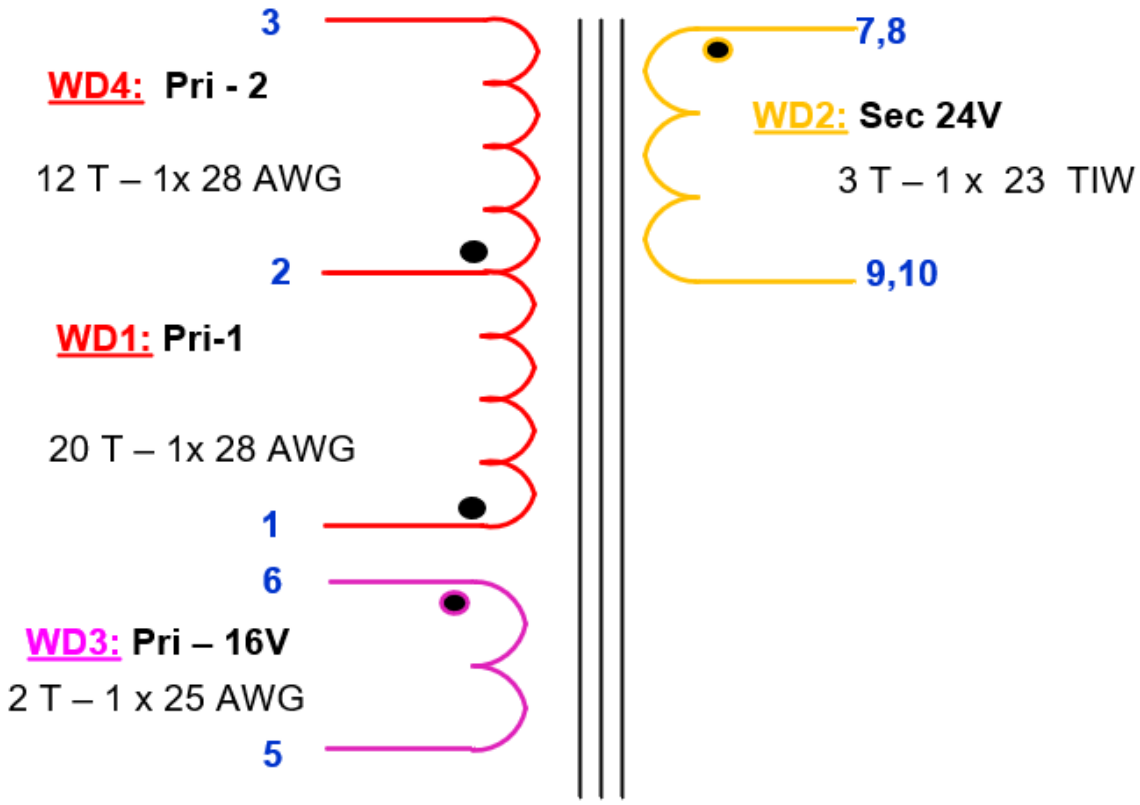


Figure 9 – Transformer Electrical Diagram.

7.4 Transformer Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 3, with all other windings open.	408 µH
Tolerance	Between pin 1 and 3, other windings open.	±5%
Primary Leakage Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 3, with all other windings shorted.	<7.4 µH (Max.)

Table 3 – Transformer Electrical Specifications.

7.5 Winding Stack Diagram

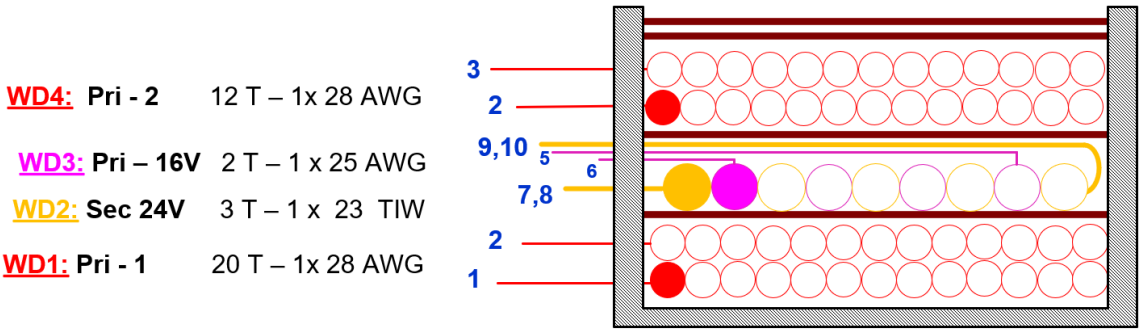


Figure 10 – Transformer Build Diagram.

7.6 List of Materials

Item	Description
[1]	**Core:** EQ3C95 and PLT30/20/3 -3C95S.
[2]	**Bobbin:** MCT-EIQ3001_V6+4P, PN: 25-01235-00.
[3]	**Magnet wire:** #28 AWG, double coated.
[4]	**Magnet wire:** #25 AWG, double coated.
[5]	**Triple Insulated Wire:** #23 AWG.
[6]	**Polyester Tape:** 19 mm.
[7]	**Polyester Tape:** 4 mm.
[8]	**Varnish:** Dolph BC-359.

Table 4 – Transformer Materials List.

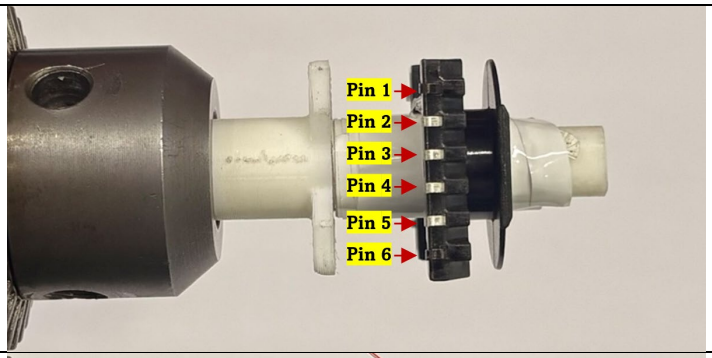
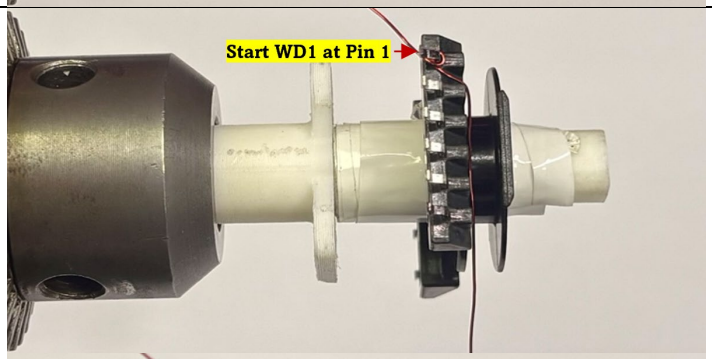
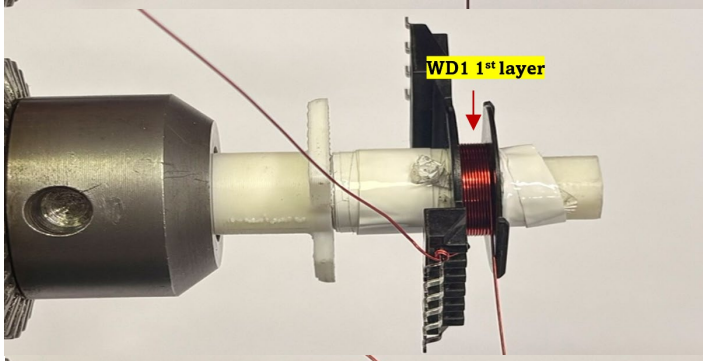
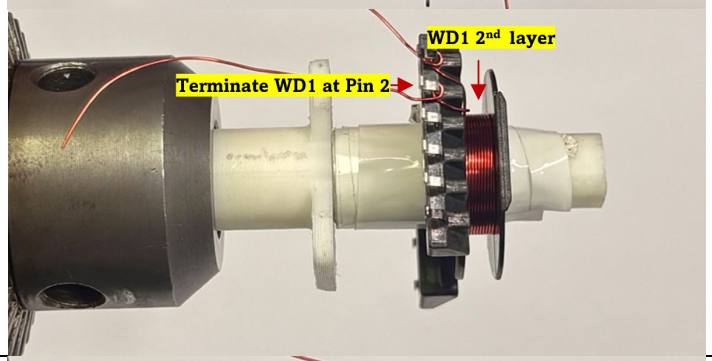
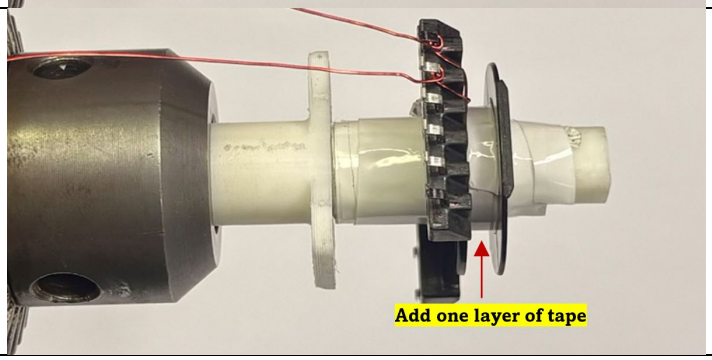
7.7 Transformer Test

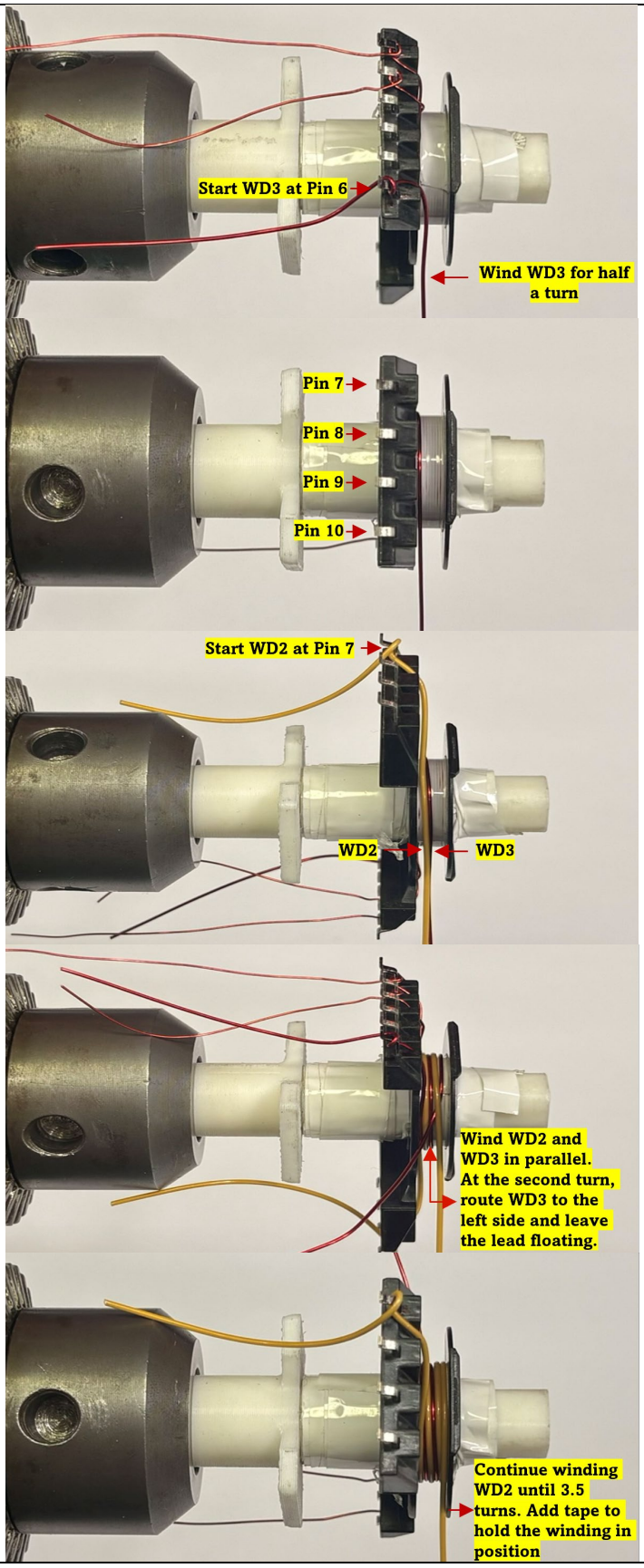
The measured inductances of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

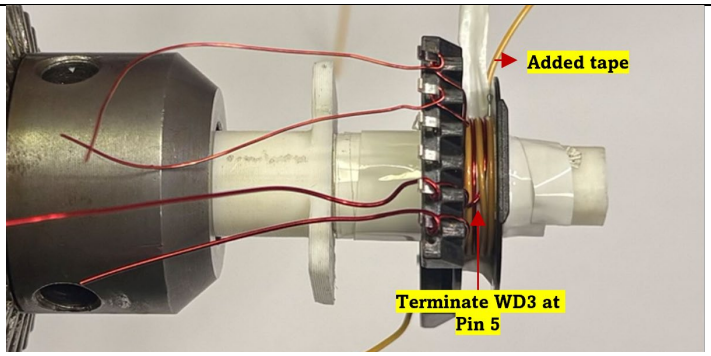
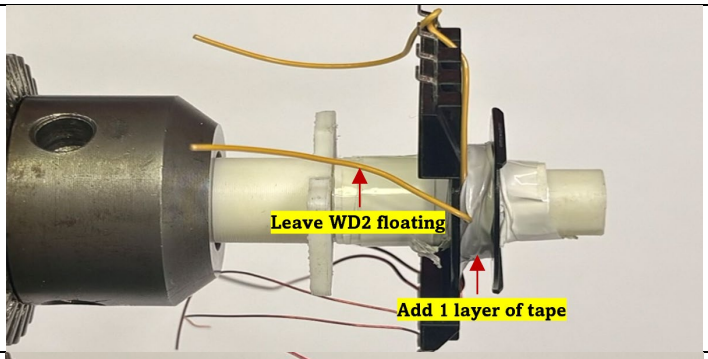
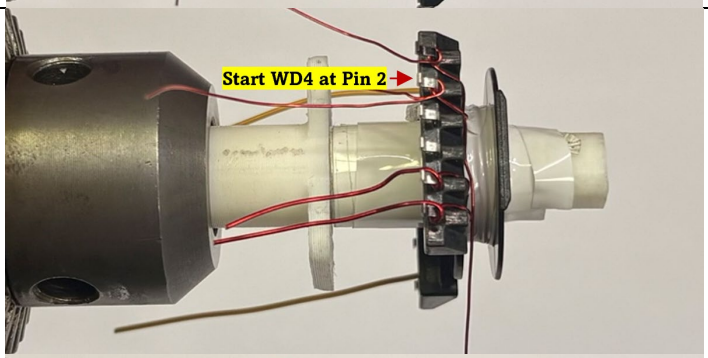
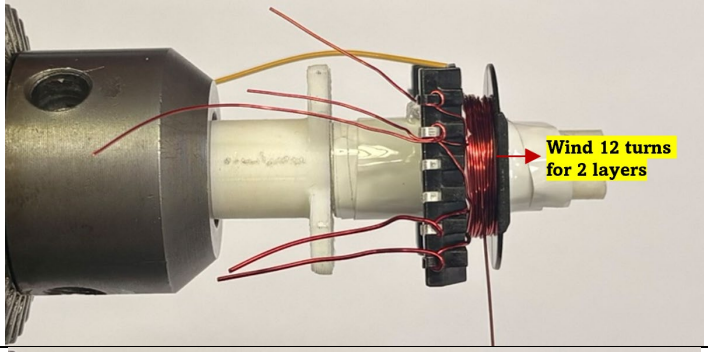
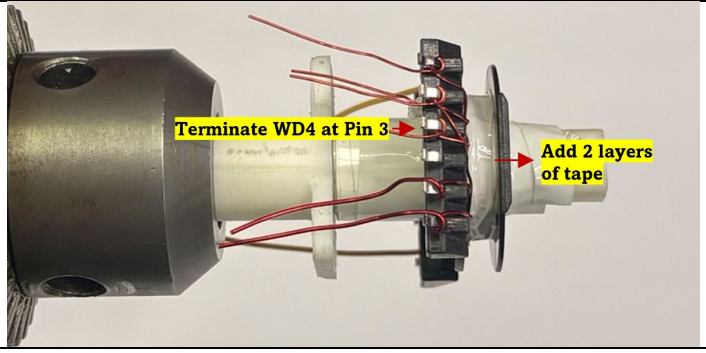
Inductance [µH]		Between Pins	Pins Shorted
L_{pri} [µH]	406	1 - 3	
$L_{16\ V}$ [µH]	1.74	5 - 6	
$L_{24\ V}$ [µH]	3.69	7 - 10	
L_{lkgpri} [µH]	7.01	1 -3	5, 6, 7, 10

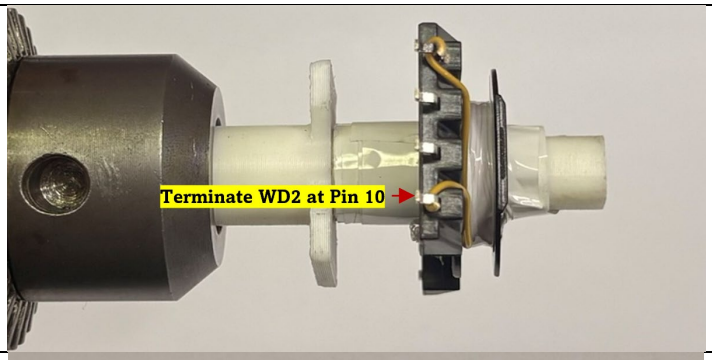
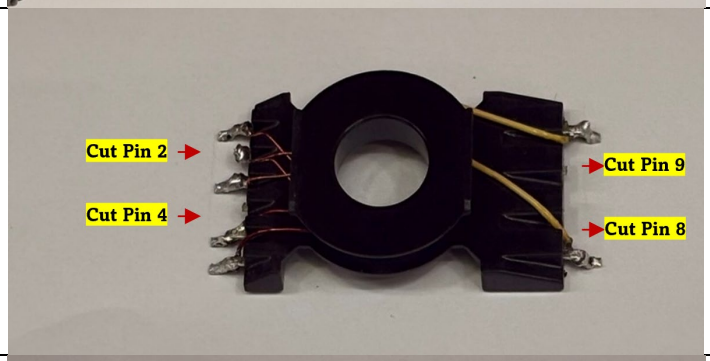
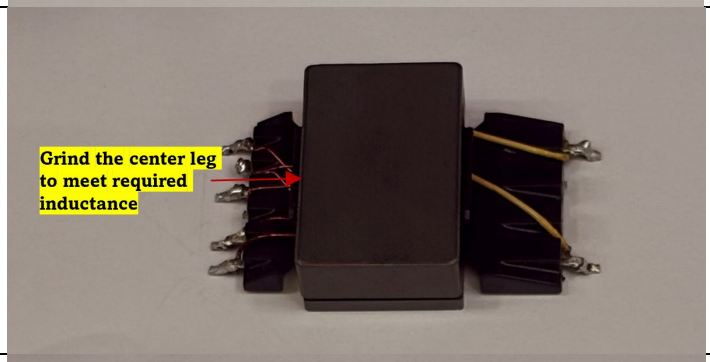
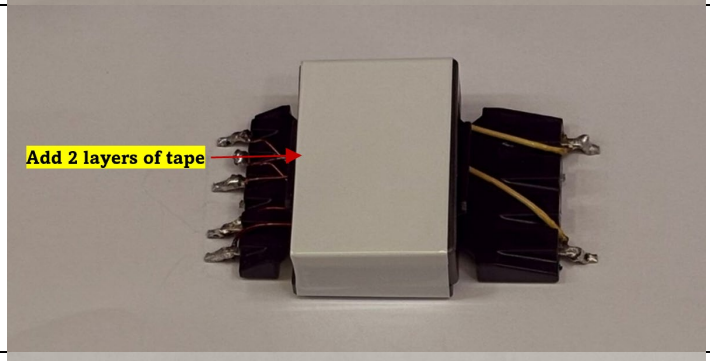
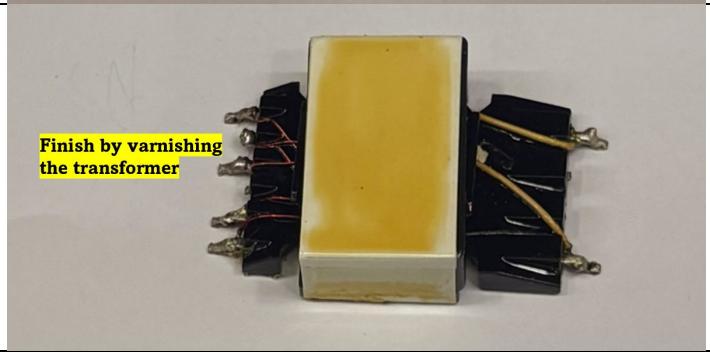
Table 5 – Winding Inductance. All measurements are done in 100 kHz at 1 V_{RMS}.

7.8 Winding Illustration

Bobbin Preparation		Use EIQ3001 bobbin Item [2]. Position bobbin on the winding jig such that pin 1-6 is on the left side. Winding direction is clockwise.
WD1: Pri - 1	  	Use AWG #28 magnet wire Item [3] for WD1 and WD4. Starting at pin 1, wind 20 turns, with tight tension, from left to right, for 2 layers. At the last turn of WD1, terminate it to Pin 2.
Insulation		Apply 4 mm Item [7] 1-layer polyester tape for insulation.

WD2: Sec 24 V and WD3: Pri 16 V		Use AWG #25 magnet wire from Item [4] for WD3. Additionally, use TIW #23 from Item [5] for WD2. • Start WD3 at Pin 6. • Wind WD3 for 0.5 turn, positioning the wire so that Pins 7-10 are visible. • Start WD2 at Pin 7. Keep WD3 positioned on the right side, as it will be terminated first. • Wind WD2 and WD3 in parallel. At the second turn, route WD3 to the left side and leave the lead floating in preparation for termination. • Continue winding WD2 with tight tension until 3.5 turns are completed. • Apply half turn tape to secure the winding in position. • Terminate WD3 at Pin 5.

		
Insulation		Continue applying one layer of 4 mm polyester tape from Item [7] for insulation. Leave WD2 floating in preparation for termination.
WD4: **Pri - 2**	 	Use AWG #28 magnet wire Item [3] for WD4. Starting at pin 2, wind 12 turns, from left to right, for 2 layers.
Insulation		Apply 4 mm Item [7] 1-layer polyester tape for insulation. Terminate WD4 at Pin 3. Terminate WD2 at Pin 10.

		
Bobbin Termination and Pin Preparation		Solder the wires to the leads of the bobbin. Cut pins 2, 4, 8 and 9.
Gap Core and Install		Use EQ3C95 and PLT30/20/3 – 3C95 Item [1]. Grind the center leg of the ferrite evenly until it meets the nominal primary inductance of 408 µH, measured across pins 1 and 3.
Core Insulation		Apply 19 mm Item [6] 2-layer polyester tape for core insulation.
Varnish		Dip the whole transformer in a pure varnish solution Item [8] for 10 minutes. Cure the varnished transformer in hot (100 °C) oven for 30 minutes.

8 Performance

8.1 Full Load Efficiency vs. Line

The Full-load efficiency across line is shown in figure 11.

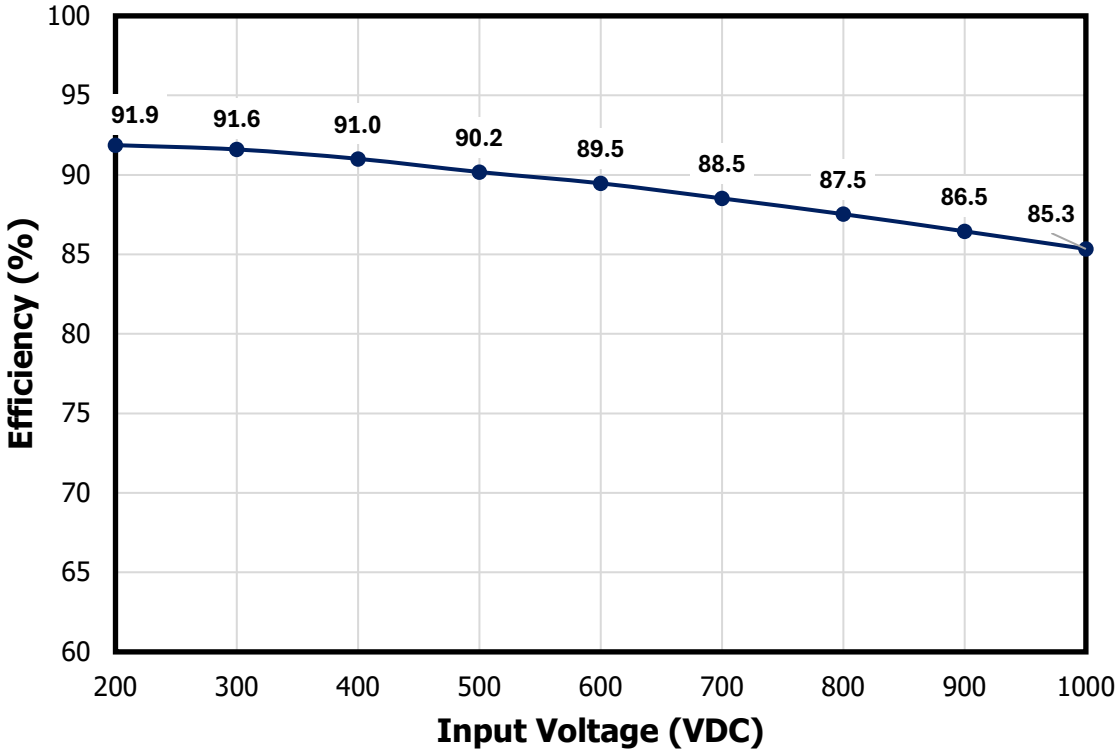


Figure 11 – Full Load Efficiency vs. Line Voltage at Room Temperature.

8.2 Efficiency vs. Load

This section shows efficiency across load and input voltage. The results highlight the impact of load and input voltage on overall conversion efficiency.

Figure 12 focuses on efficiency with respect to normalized output load (0-100%), showing performance from light-load to full-load conditions.

Figures 13 to 15 show the efficiency of the 16 V output under different line and main output load conditions.

- Input line voltages: 200 VDC, 800 VDC, 1000 VDC
- Unregulated output: 16 V full current of 350 mA with 10 steps for each line voltage
- Regulated output: 24 V full current of 600 mA with 10 steps for each line voltage

8.2.1 Efficiency vs 16 V Output Load

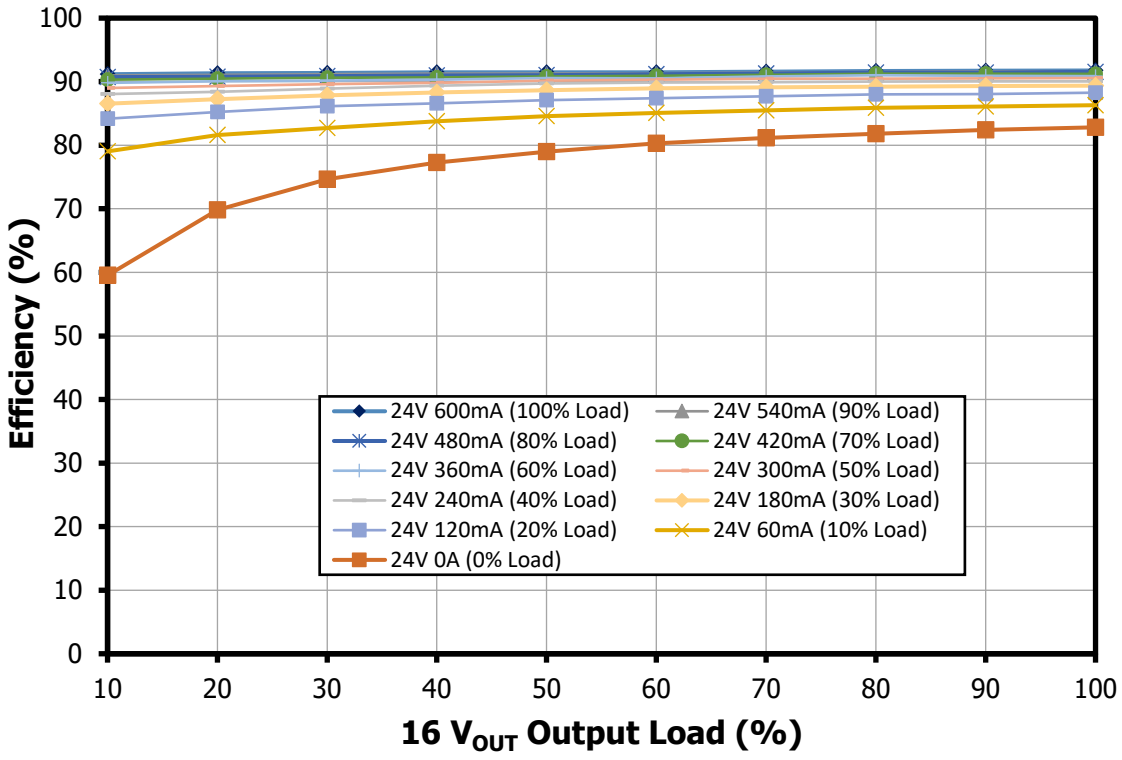


Figure 12 – Efficiency vs. 16 V Output Load at 200 VDC Input Voltage at Room Temperature.

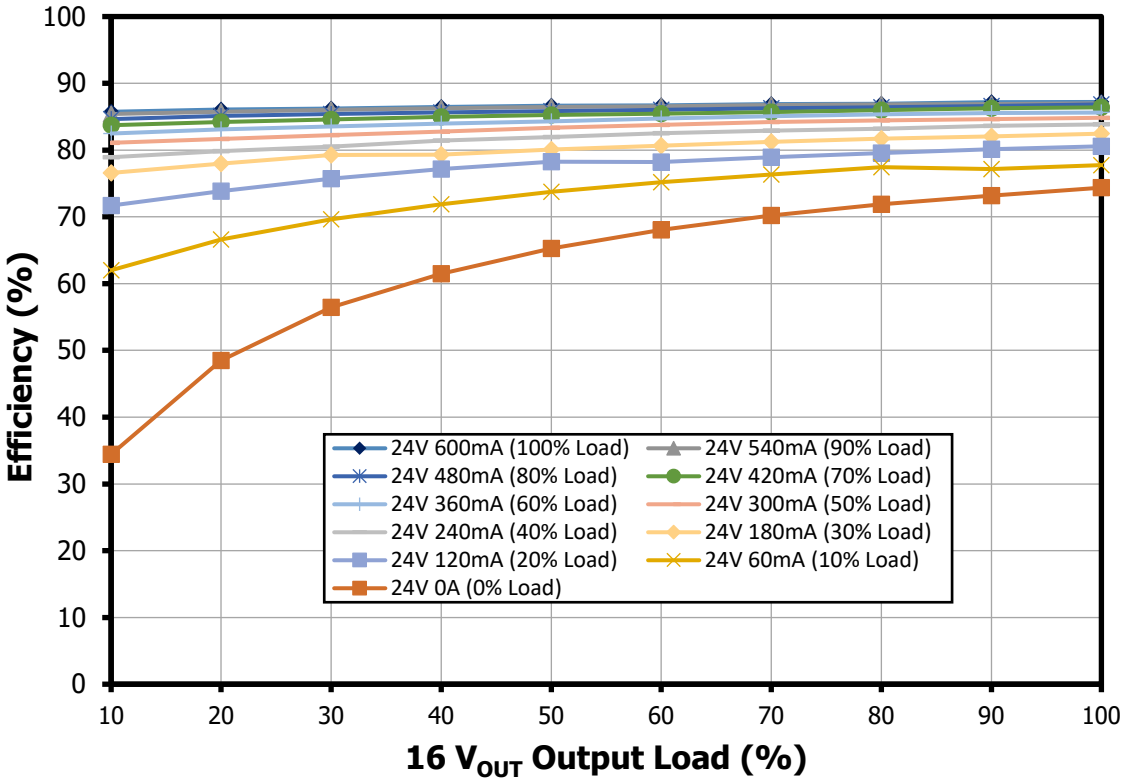


Figure 13 – Efficiency vs. 16 V Output Load at 800 VDC Input Voltage at Room Temperature.

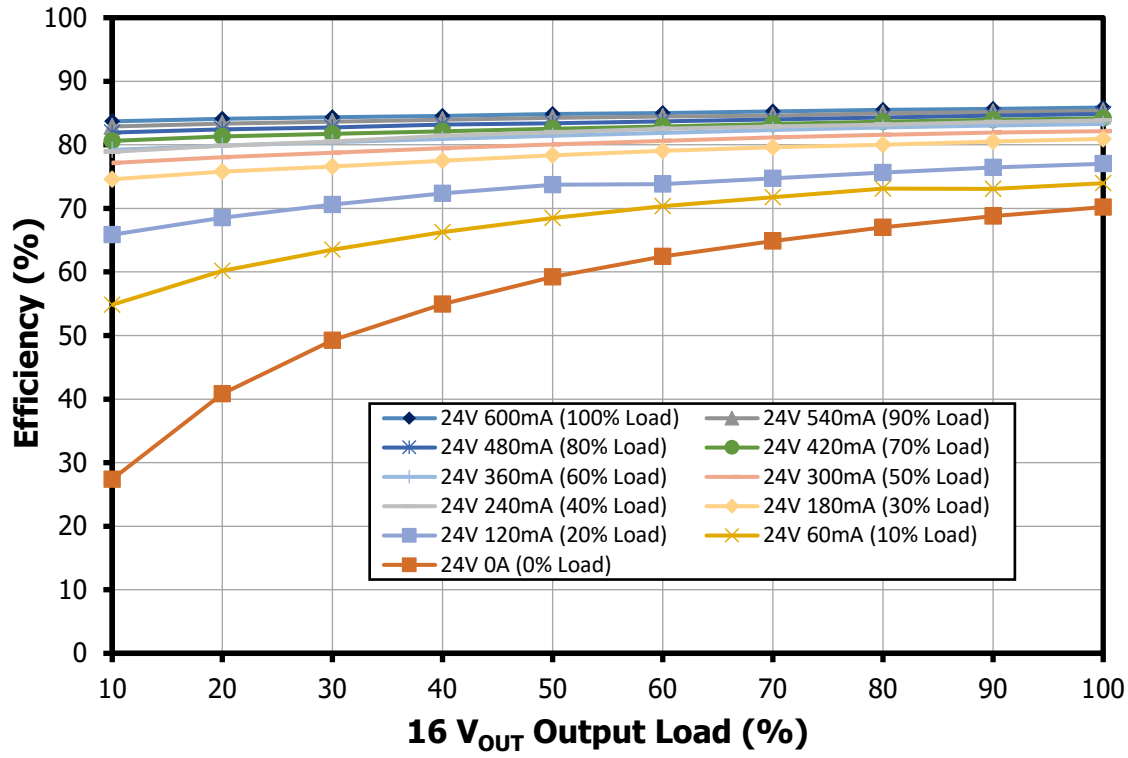


Figure 14 – Efficiency vs. 16 V Output Load at 1000 VDC Input Voltage at Room Temperature.

8.2.2 Efficiency vs $P_{OUT}/P_{OUT(MAX)}$

Test Description: The test sweeps input voltage across three-line conditions (200 V, 800 V, and 1000 V); at each VIN, a full cross-regulation load sweep is performed by fixing the 24 V rail at stepped load levels while sweeping the 16 V rail from full load down to no load. The resulting data are used to generate a plot of efficiency versus normalized output power (Po/Po_{max}).

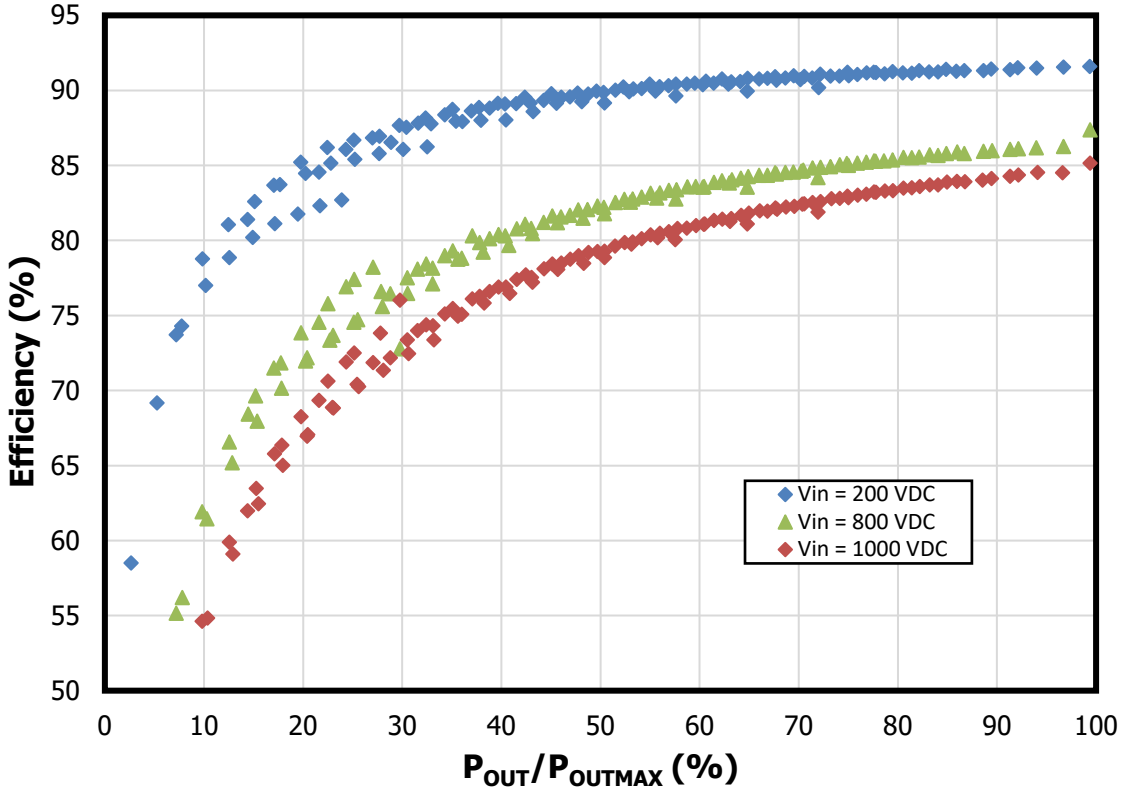


Figure 15 – Efficiency vs. Load at Room Temperature.

8.3 Output Load Regulation

Figures 16-21 describe how a change in load affects output voltage. Each plot represents load regulation vs. load on that output. Both the 16 V and 24 V output loads were varied.

- Input line voltages: 200 VDC, 800 VDC, 1000 VDC
- Unregulated output: 16 V full current of 350 mA with 10 steps for each line voltage
- Regulated output: 24 V full current of 600 mA with 10 steps for each line voltage

8.3.1 16 V Output Load Regulation

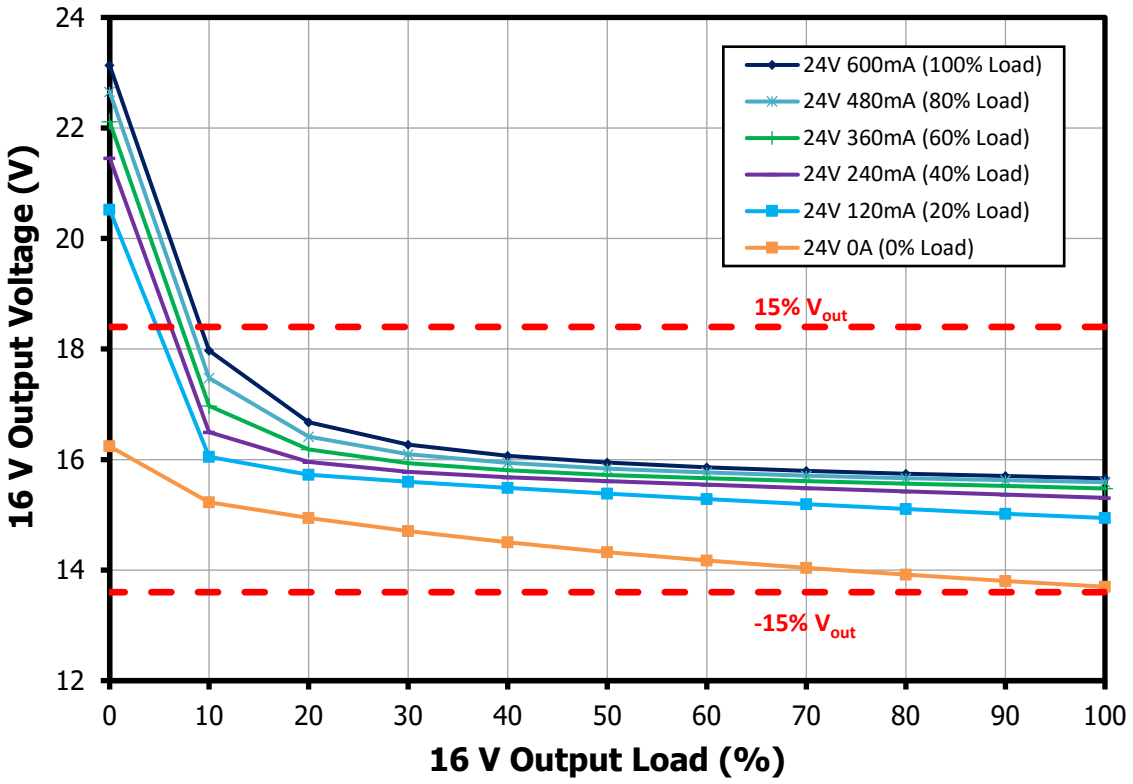


Figure 16 – 16 V Output Regulation vs. Load at 200 VDC Input Voltage at Room Temperature.

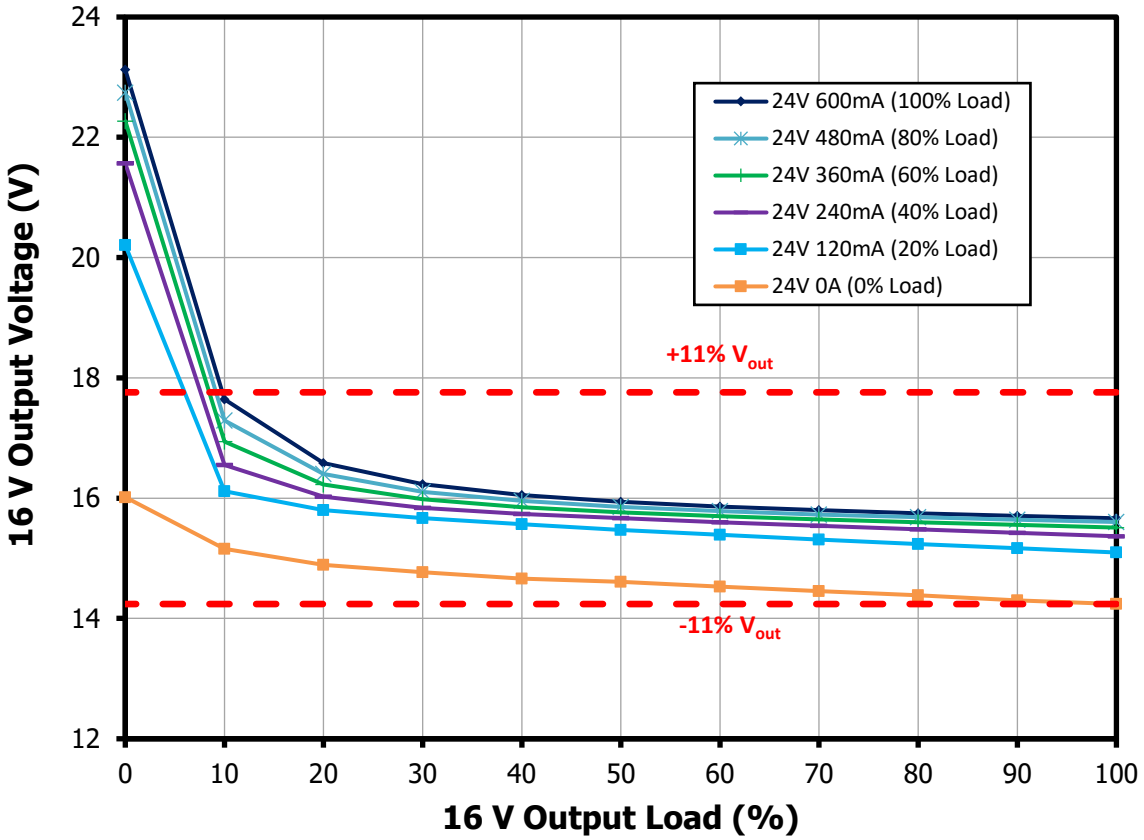


Figure 17 – 16 V Output Regulation vs. Load at 800 VDC Input Voltage at Room Temperature.

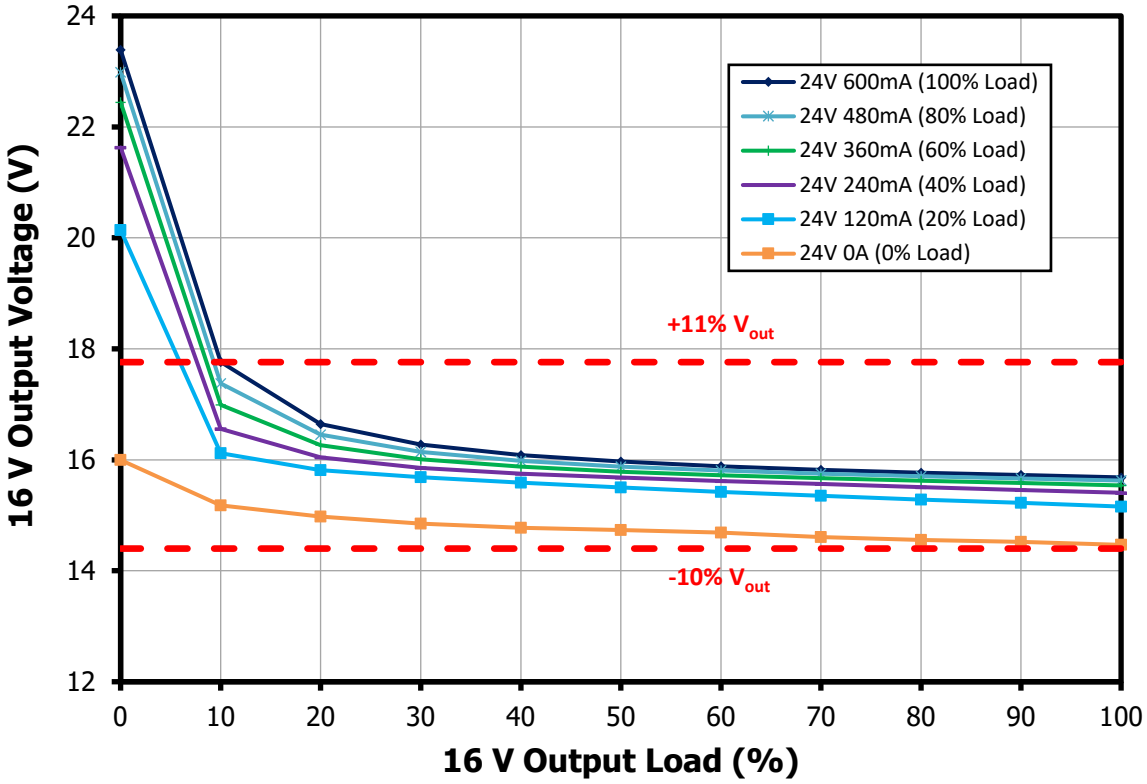


Figure 18 – 16 V Output Regulation vs. Load at 1000 VDC Input Voltage at Room Temperature.

8.3.2 24 V Output Load Regulation

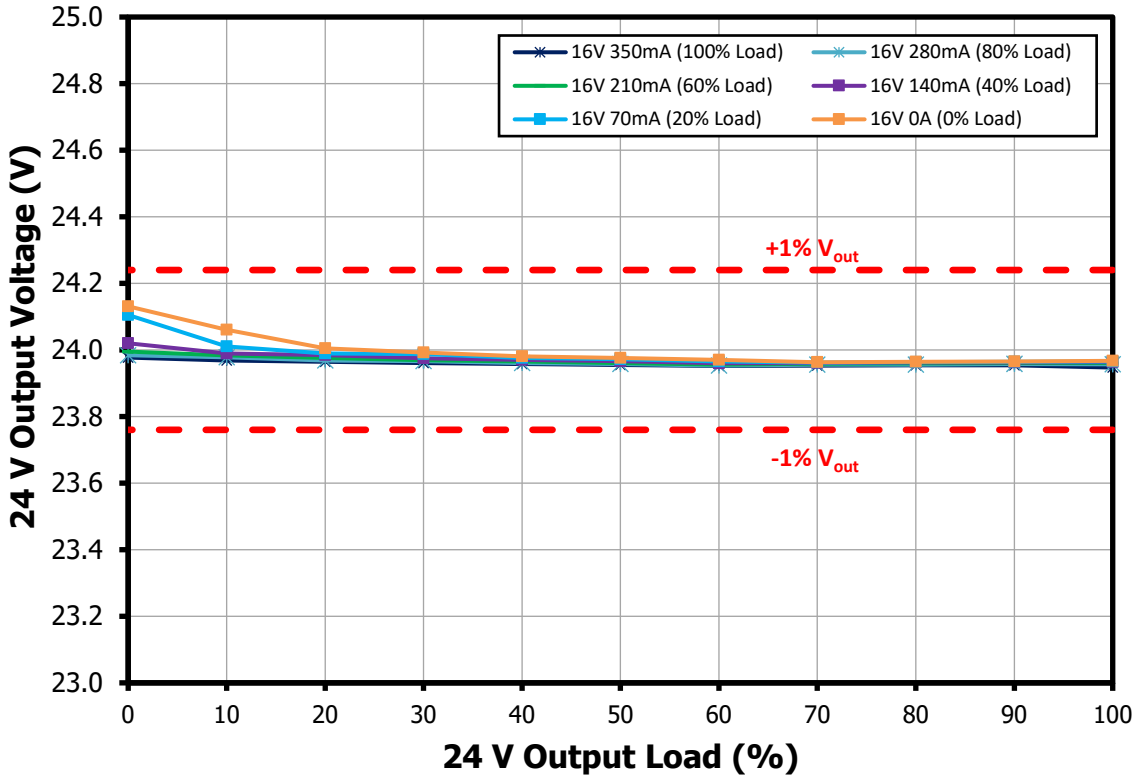


Figure 19 – 24 V Output Regulation vs. Load at 200 VDC Input Voltage at Room Temperature.

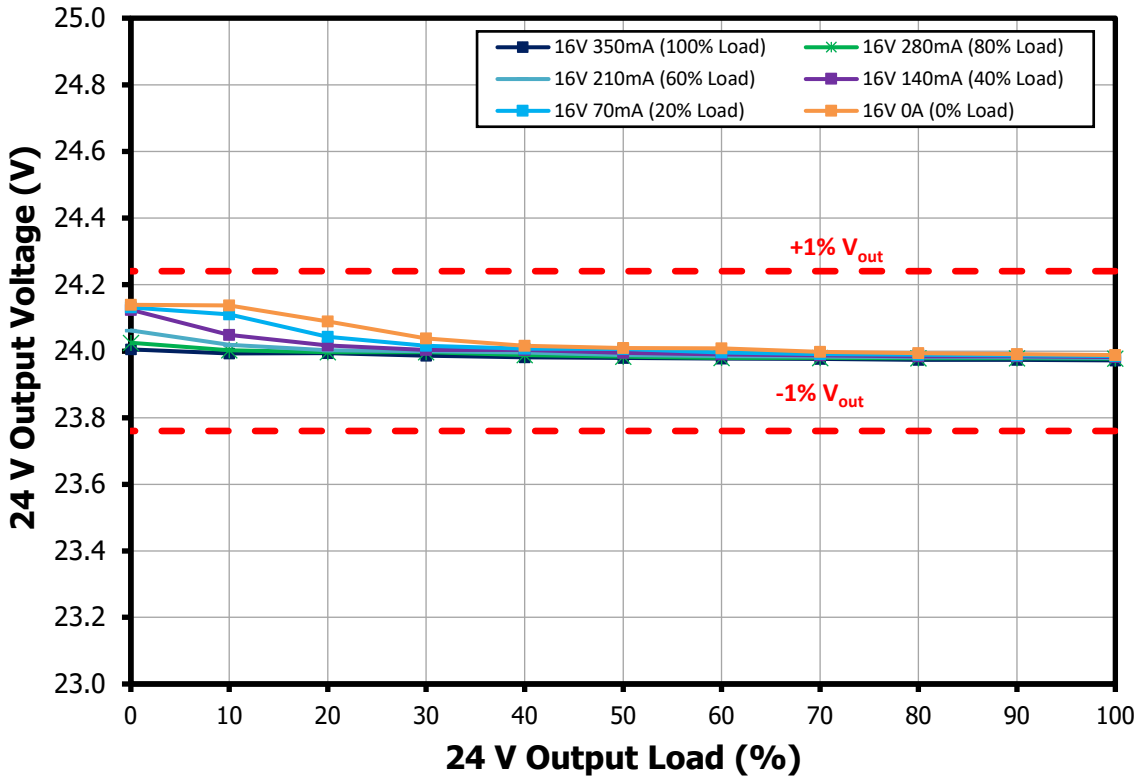


Figure 20 – 24 V Output Regulation vs. Load at 800 VDC Input Voltage at Room Temperature.

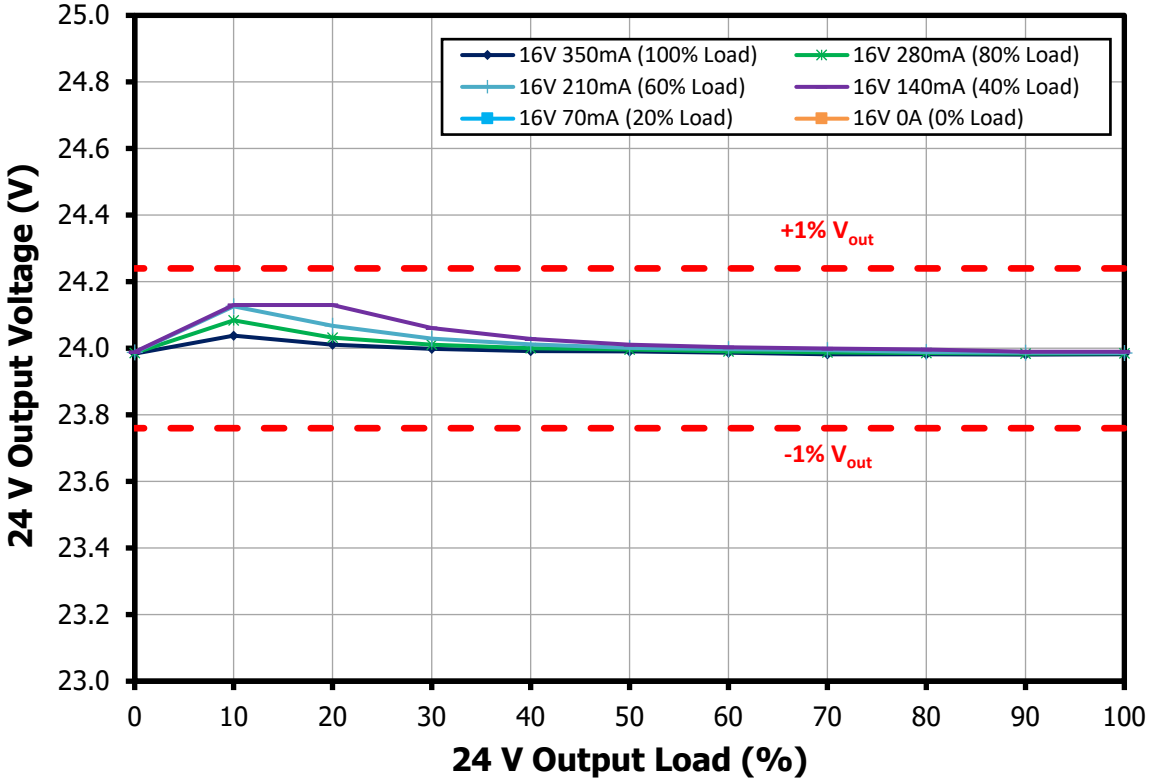


Figure 21 – 24 V Output Regulation vs. Load at 1000 VDC Input Voltage at Room Temperature.

8.4 Full Load Line Regulation

Figures 22 and 23 describe how a change in input voltage affects output voltage. Results were obtained for all combinations of:

- Input line voltage: 200 VDC to 1000 VDC with 100 VDC increment
- Unregulated Output = 16 V @ 350 mA
- Regulated Output = 24 V @ 600 mA

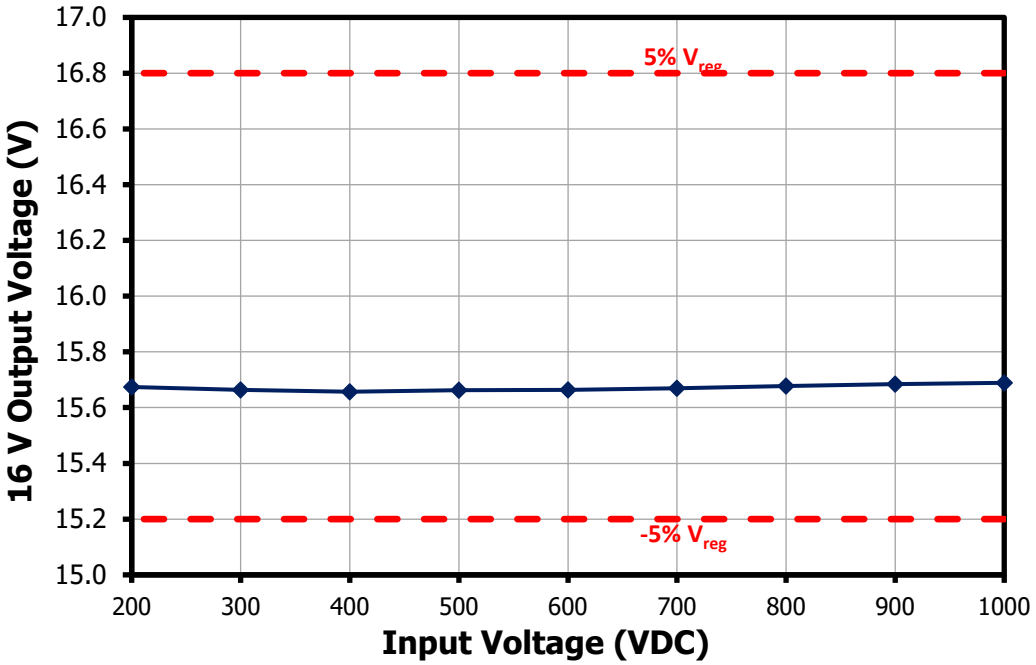


Figure 22 – 16 V Output Regulation vs Input Voltage Full Load at Room Temperature.

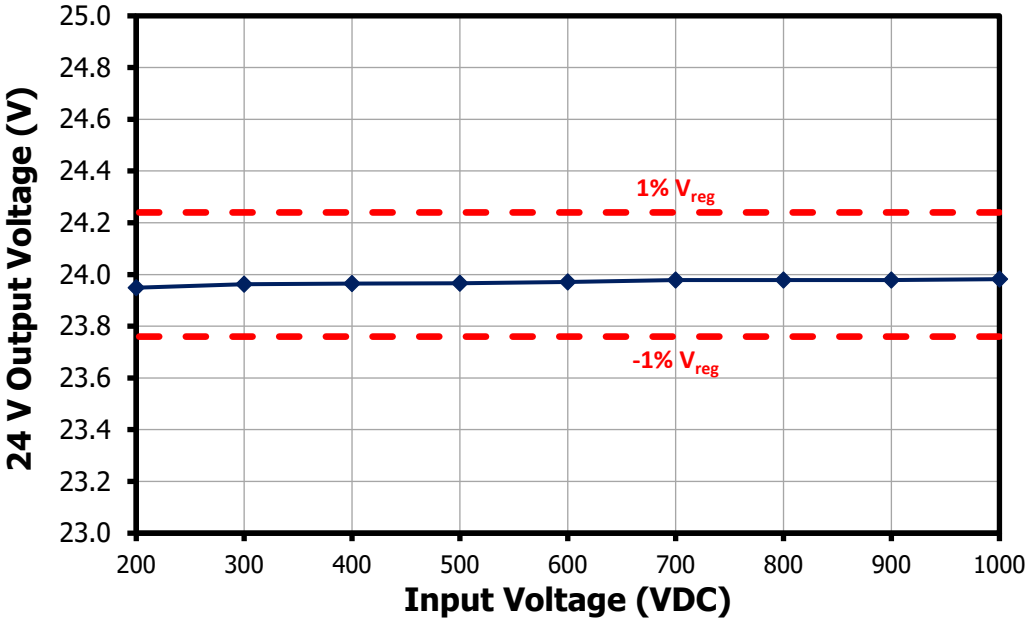


Figure 23 – 24 V Output Regulation vs Input Voltage Full Load at Room Temperature.

8.5 No-Load and Standby Input Power

Figure 24 shows the test circuit used for no-load and standby input power measurement. The voltmeter was placed before the ammeter to prevent the voltmeter bias current from affecting the input current measurements. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

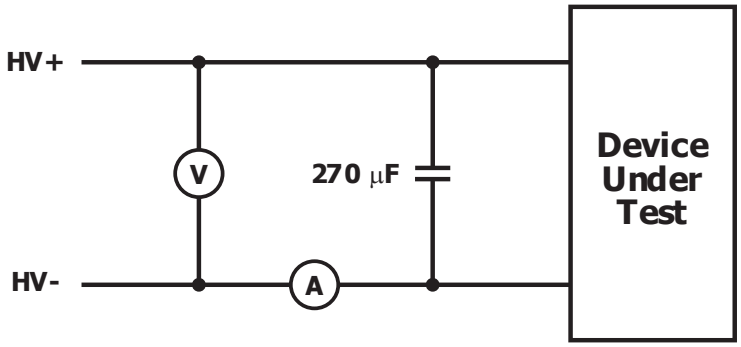


Figure 24 – No-Load and Standby Input Power Measurement Diagram.

The unit was allowed to stabilize for ten minutes for each test before measurements were taken. The leakage current of the DC-link capacitors was measured separately and subtracted from the total measured input current.

Results were obtained under the following test conditions:

- Input line voltages: 200 VDC, 800 VDC, 1000 VDC
- Unregulated Output = 16 V @ 0 W
- Regulated Output = 24 V @ 0 mW to 250 mW; 0 mW to 1000 mW

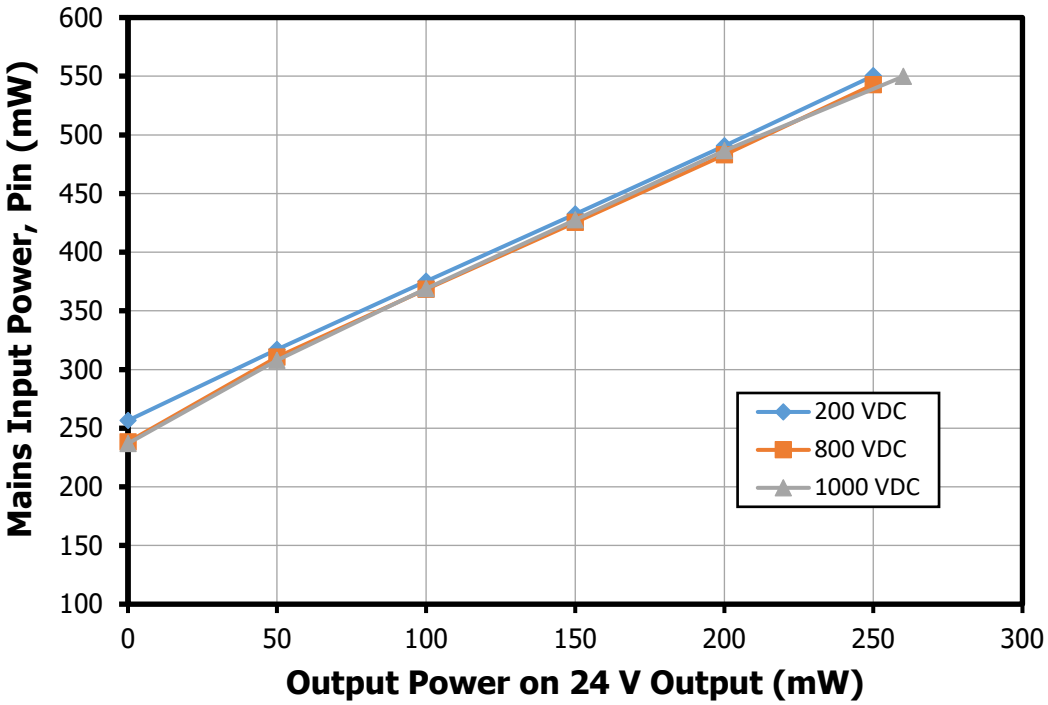


Figure 25 – Available Standby Power Measured against Input Power (0 – 550 mW). Across Input Voltage. Test Performed at Room Temperature.

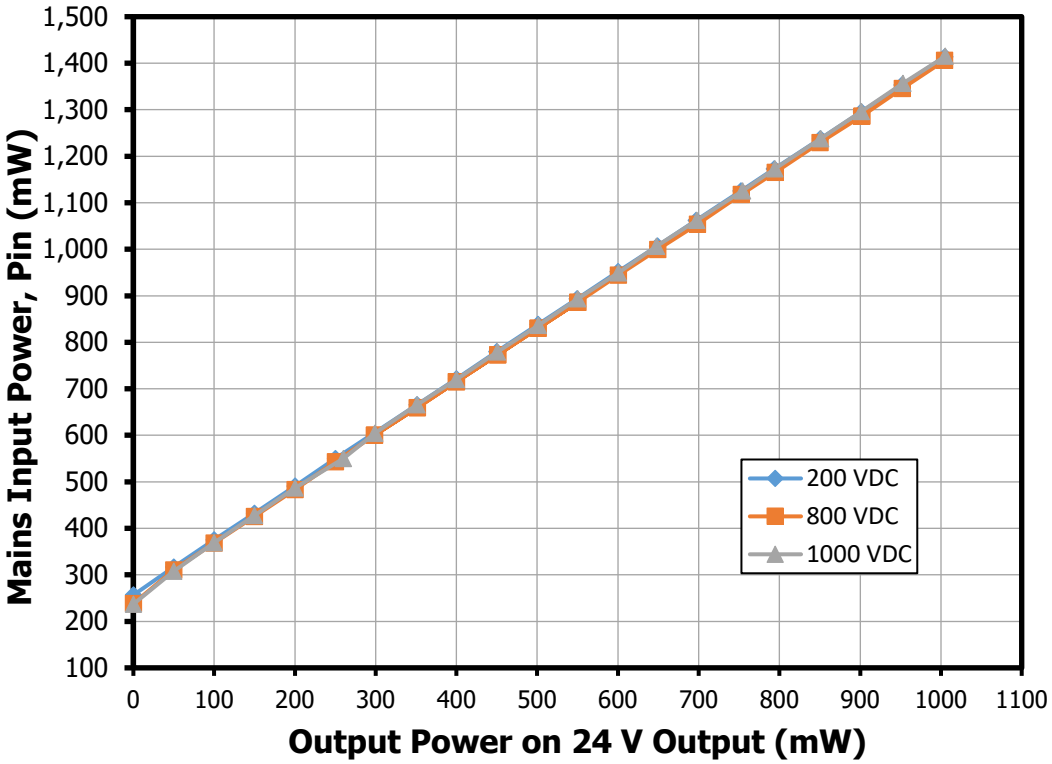


Figure 26 – Available Standby Power Measured against Input Power (0 – 1420 mW). Across Input Voltage. Test Performed at Room Temperature.

9 Waveforms

9.1 Start-up Profile

Measurements were taken by plugging the unit into a fully charged DC link capacitor at different input voltages. A constant resistive load was used for all start up tests.

9.1.1 Full Load Start-Up

The start-up test was performed using the following test conditions:

- Input line voltage: 200 VDC, 800 VDC, 1000 VDC
- Unregulated Output = 16 V @ 20 W (Full Load)
- Regulated Output = 24 V @ 20 W (Full Load)

Figure 27 – 16 V Start-up Profile
200 VDC, Full-Load, Start-up.
CH1: V_{IN}, 40 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

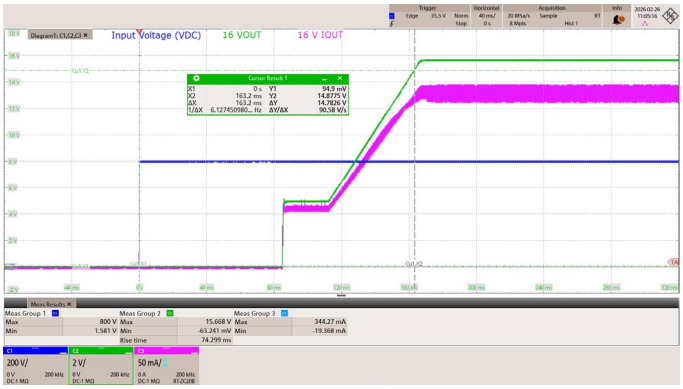


Figure 28 – 16 V Start-up Profile
800 VDC, Full-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

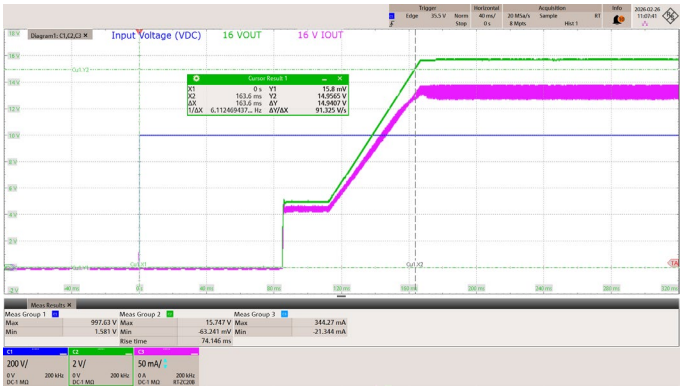


Figure 29 – 16 V Start-up Profile
1000 VDC, Full-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 164 ms

Figure 30 – 24 V Start-up Profile
200 VDC, Full-Load, Start-up.
CH1: V_{IN}, 50 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

Figure 31 – 24 V Start-up Profile
800 VDC, Full-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

Figure 32 – 24 V Start-up Profile
1000 VDC, Full-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

9.1.2 No-Load Start-up

A no load start-up test was performed using the following test conditions:

- Input line voltage: 200 VDC, 800 VDC, 1000 VDC
- Unregulated Output = 16 V @ 0 W (No Load)
- Regulated Output = 24 V @ 0 W (No Load)

Figure 33 – 16 V Start-up Profile
200 VDC, No-Load, Start-up.
CH1: V_{IN}, 40 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 166 ms

Figure 34 – 16 V Start-up Profile
800 VDC, No-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 165 ms

Figure 35 – 16 V Start-up Profile
1000 VDC, No-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_16V}, 2 V / div.
CH3: I_{OUT_16V}, 50 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 165 ms

Figure 36 – 24 V Start-up Profile
200 VDC, No-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 163 ms

Figure 37 – 24 V Start-up Profile
800 VDC, No-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 162 ms

Figure 38 – 24 V Start-up Profile
1000 VDC, No-Load, Start-up.
CH1: V_{IN}, 200 V / div.
CH2: V_{OUT_24V}, 4 V / div.
CH3: I_{OUT_24V}, 200 mA / div.
Time Scale: 40 ms / div.
$t_{ON\ Delay}$: 162 ms

9.2 Switching Waveforms

9.2.1 Flyback Primary Drain Voltage and Current

9.2.1.1 Flyback Primary Drain Voltage and Current at Start-up Full Load

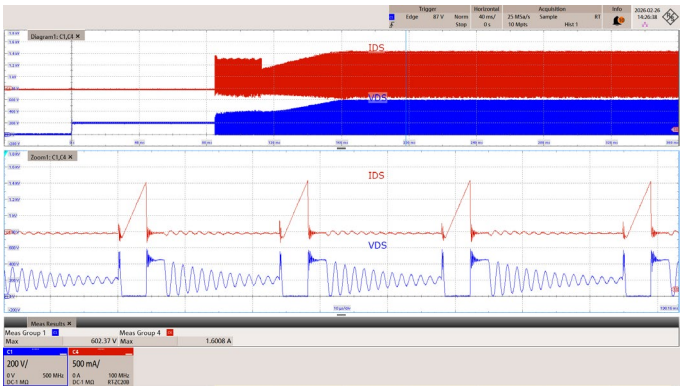


Figure 39 – Primary Drain Voltage and Current
200 VDC, Full-Load, Start-up.
CH1: V_{DRAIN}, 200 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 602 V; I_{DSMAX}: 1.60 A

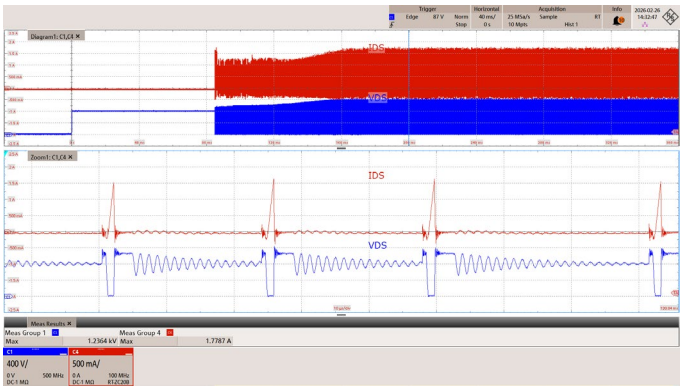


Figure 40 – Primary Drain Voltage and Current
800 VDC, Full-Load, Start-up.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 1.24 kV; I_{DSMAX}: 1.78 A

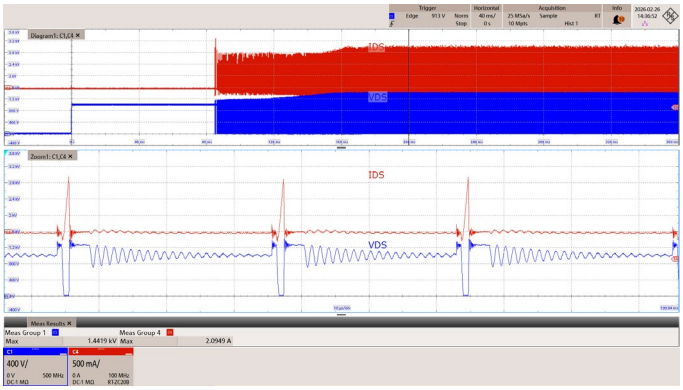


Figure 41 – Primary Drain Voltage and Current
1000 VDC, Full-Load, Start-up.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 1.44 kV; I_{DSMAX}: 2.01 A

9.2.1.2 Flyback Primary Drain Voltage and Current at Start-up No Load

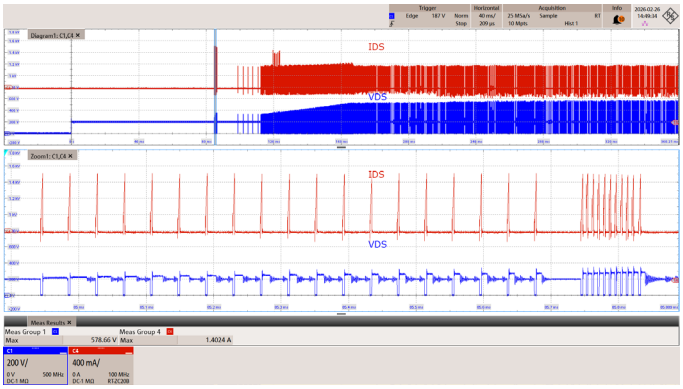


Figure 42 – Primary Drain Voltage and Current
200 VDC, No-Load, Start-up.
CH1: V_{DRAIN}, 200 V / div.
CH4: I_{DRAIN}, 400 mA / div.
Time Scale: 40 ms / div. (100 µs / div. Zoom)
V_{DSMAX}: 579 V; I_{DSMAX}: 1.40 A

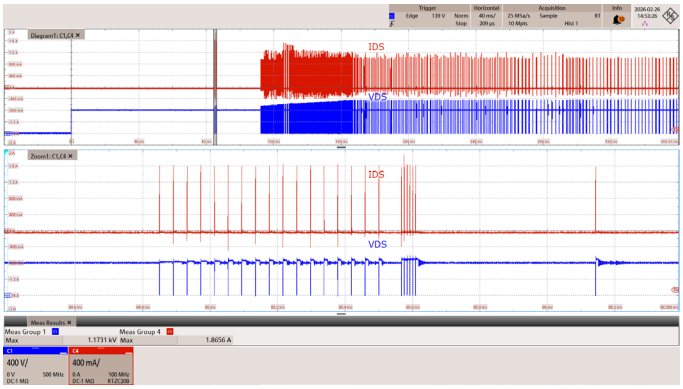


Figure 43 – Primary Drain Voltage and Current
800 VDC, No-Load, Start-up.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 400 mA / div.
Time Scale: 40 ms / div. (200 µs / div. Zoom)
V_{DSMAX}: 1.17 kV; I_{DSMAX}: 1.87 A

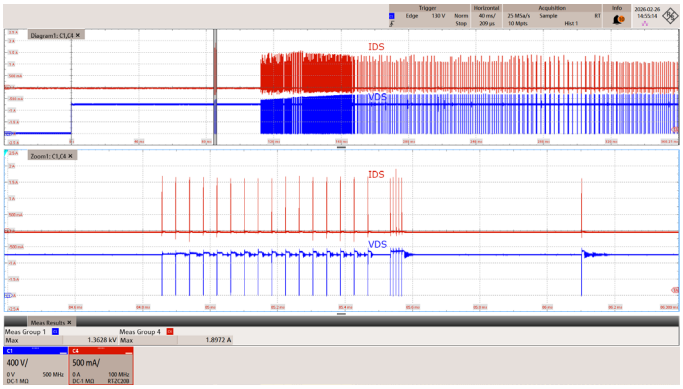


Figure 44 – Primary Drain Voltage and Current
1000 VDC, No-Load, Start-up.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 40 ms / div. (200 µs / div. Zoom)
V_{DSMAX}: 1.36 kV; I_{DSMAX}: 1.90 A

9.2.1.3 Flyback Primary Drain Voltage and Current at Full Load Steady-State

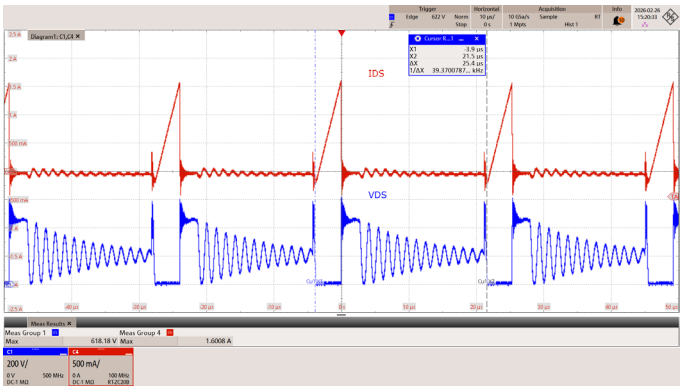


Figure 45 – Primary Drain Voltage and Current
200 VDC, Full-Load, Steady-State.
CH1: V_{DRAIN}, 200 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 10 µs / div.
V_{DSMAX}: 618 V; I_{DSMAX}: 1.60 A

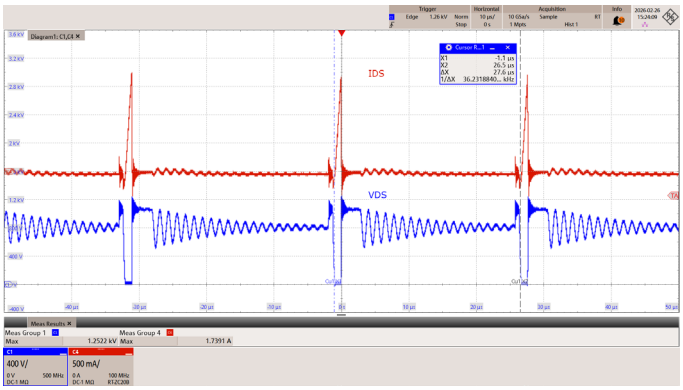


Figure 46 – Primary Drain Voltage and Current
800 VDC, Full-Load, Steady-State.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 10 µs / div.
V_{DSMAX}: 1.25 kV; I_{DSMAX}: 1.74 A

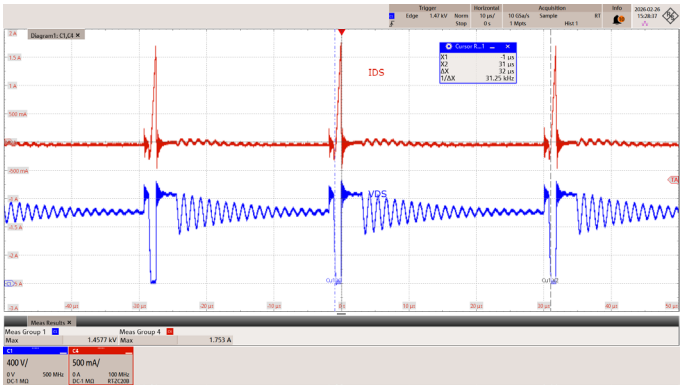


Figure 47 – Primary Drain Voltage and Current
1000 VDC, Full-Load, Steady-State.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 500 mA / div.
Time Scale: 10 µs / div.
V_{DSMAX}: 1.46 kV; I_{DSMAX}: 1.75 A

9.2.1.4 Flyback Primary Drain Voltage and Current at Output Short

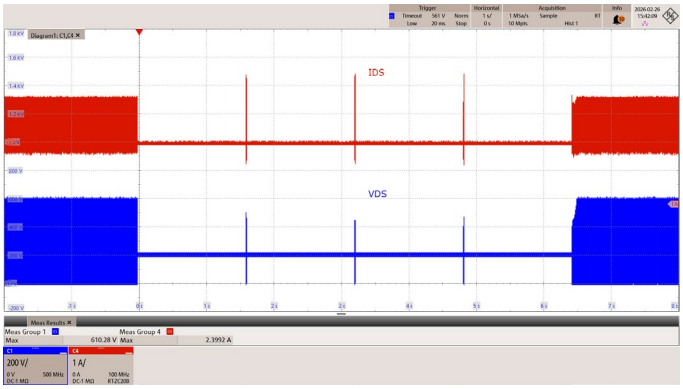


Figure 48 – Primary Drain Voltage and Current
200 VDC, 24 V = Max – Short – Max while 16 V = Max. Output.
CH1: V_{DRAIN}, 200 V / div.
CH4: I_{DRAIN}, 1 A / div.
Time Scale: 1 s / div.
V_{DSMAX}: 610 V; I_{DSMAX}: 2.40 A

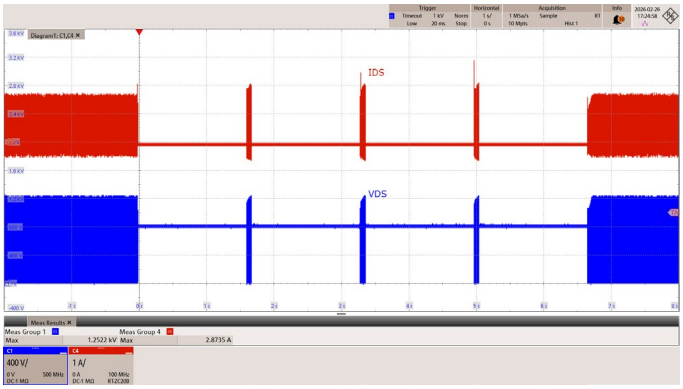


Figure 49 – Primary Drain Voltage and Current
800 VDC, 24 V = Max – Short – Max while 16 V = Max. Output.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 1 A / div.
Time Scale: 1 s / div.
V_{DSMAX}: 1.25 kV; I_{DSMAX}: 2.87 A

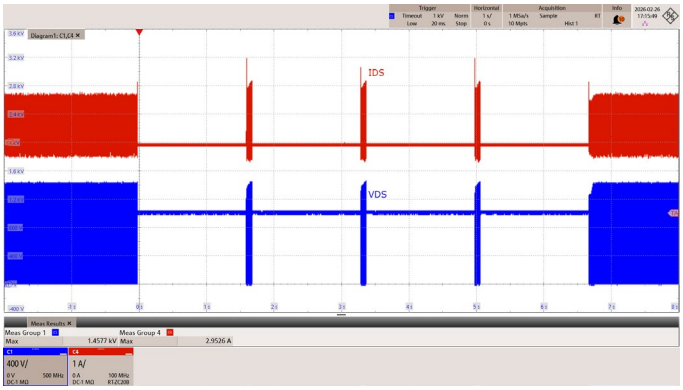


Figure 50 – Primary Drain Voltage and Current
1000 VDC, 24 V = Max – Short – Max while = Max. Output.
CH1: V_{DRAIN}, 400 V / div.
CH4: I_{DRAIN}, 1 A / div.
Time Scale: 1 s / div.
V_{DSMAX}: 1.46 kV; I_{DSMAX}: 2.95 A

9.2.2 Flyback SR FET Voltage Waveforms

9.2.2.1 SR FET Voltage Waveform at Full Load Start-up

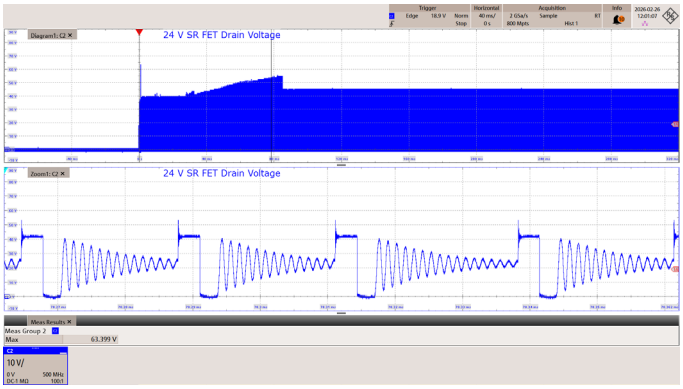


Figure 51 – 24 V SR FET Drain Voltage
200 VDC, Full-Load, Start-up.
CH2: V_{SRFET_24V}, 10 V / div.
Time Scale: 40 ms/div. (10 µs / div Zoom)
$V_{SRFET\_24V\ (MAX)}$: 63.4 V

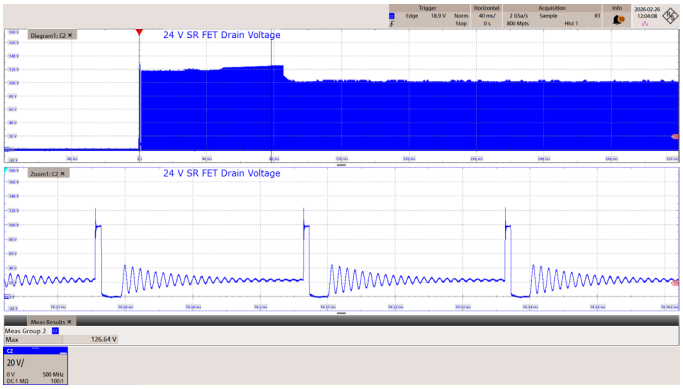


Figure 52 – 24 V SR FET Drain Voltage
800 VDC, Full-Load, Start-up.
CH2: V_{SRFET_24V}, 20 V / div.
Time Scale: 40 ms/div. (10 µs / div Zoom)
$V_{SRFET\_24V\ (MAX)}$: 127 V

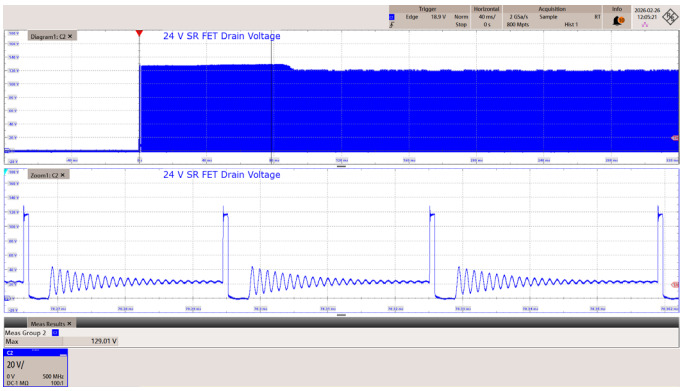


Figure 53 – 24 V SR FET Drain Voltage
1000 VDC, Full-Load, Start-up.
CH2: V_{SRFET_24V}, 20 V / div.
Time Scale: 40 ms/div. (10 µs / div Zoom)
$V_{SRFET\_24V\ (MAX)}$: 129 V

9.2.2.2 SR FET Voltage Waveform at Full Load Steady-State

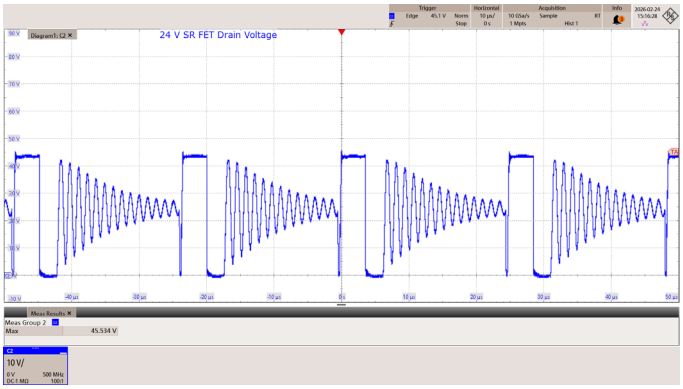


Figure 54 – 24 V SR FET Drain Voltage
200 VDC, Full-Load, Steady-State.
CH2: V_{SRFET_24V}, 10 V / div.
Time Scale: 10 µs / div.
$V_{SRFET\_24V\ (MAX)}$: 45.5 V

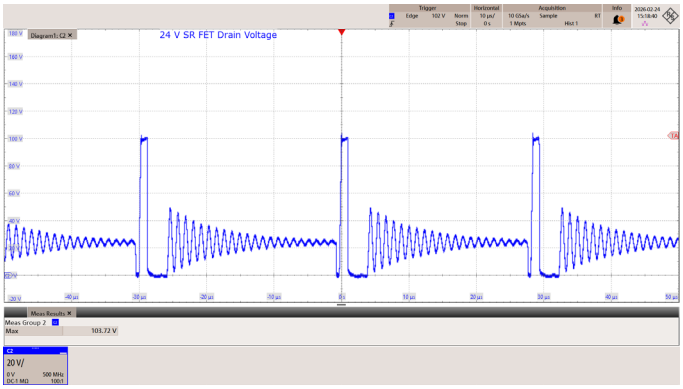


Figure 55 – 24 V SR FET Drain Voltage
800 VDC, Full-Load, Steady-State.
CH2: V_{SRFET_24V}, 20 V / div.
Time Scale: 10 µs / div.
$V_{SRFET\_24V\ (MAX)}$: 104 V

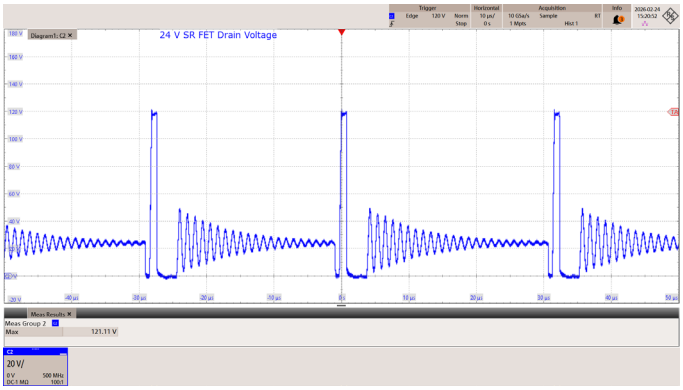


Figure 56 – 24 V SR FET Drain Voltage
1000 VDC, Full-Load, Steady-State.
CH2: V_{SRFET_24V}, 20 V / div.
Time Scale: 10 µs / div.
$V_{SRFET\_24V\ (MAX)}$: 121 V

9.2.3 16 V Output Diode Voltage Waveforms

9.2.3.1 16 V Output Diode Voltage Waveform at Full Load Start-up

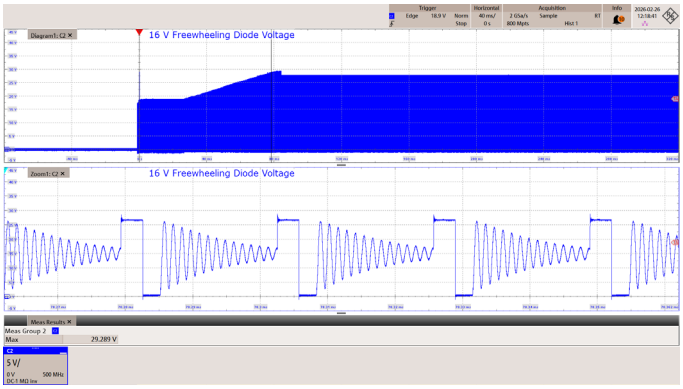


Figure 57 – 16 V Freewheeling Diode Voltage
200 VDC, Full-Load, Start-up.
CH2: $V_{FREEWHELING\_DIODE}$, 5 V / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
$V_{FREEWHELING\_DIODE(MAX)}$: 29.3 V

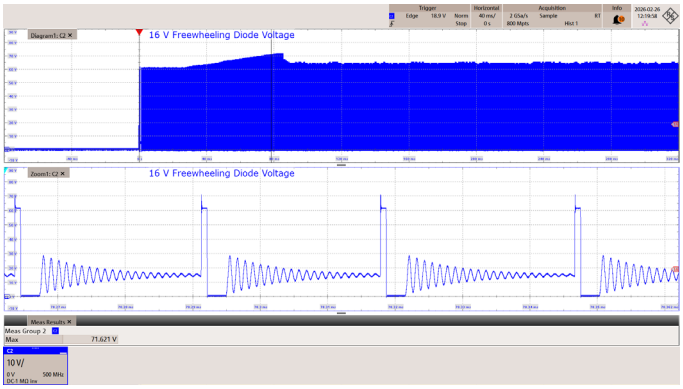


Figure 58 – 16 V Freewheeling Diode Voltage
800 VDC, Full-Load, Start-up.
CH2: $V_{FREEWHELING\_DIODE}$, 10 V / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
$V_{FREEWHELING\_DIODE(MAX)}$: 71.6 V

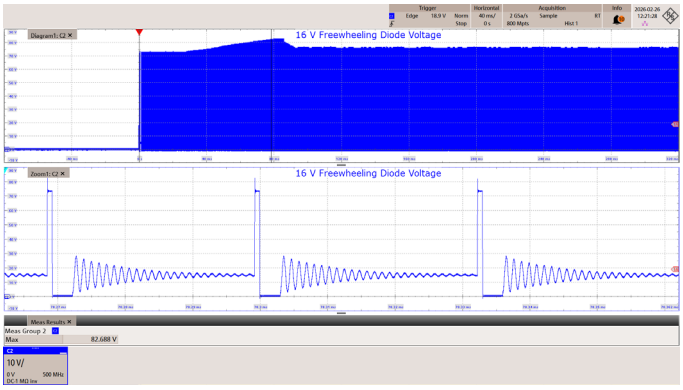


Figure 59 – 16 V Freewheeling Diode Voltage
1000 VDC, Full-Load, Start-up.
CH2: $V_{FREEWHELING\_DIODE}$, 10 V / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
$V_{FREEWHELING\_DIODE(MAX)}$: 82.7 V

9.2.3.2 16 V Output Diode Voltage Waveform at Full Load Steady-State

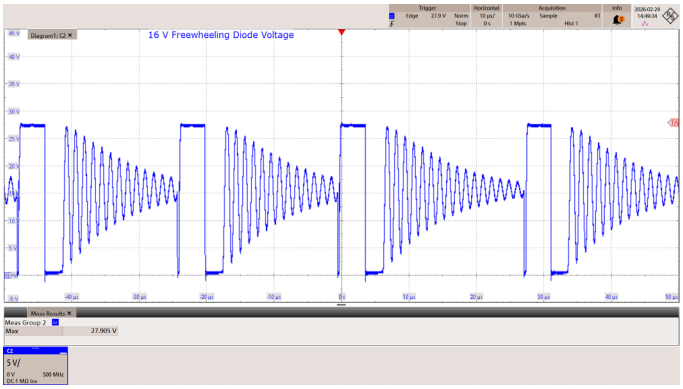


Figure 60 – 16 V Freewheeling Diode Voltage
200 VDC, Full-Load, Steady-State.
CH2: $V_{FREEWHELING\_DIODE}$, 5 V / div.
Time Scale: 10 µs / div.
$V_{FREEWHELING\_DIODE(MAX)}$: 27.9 V

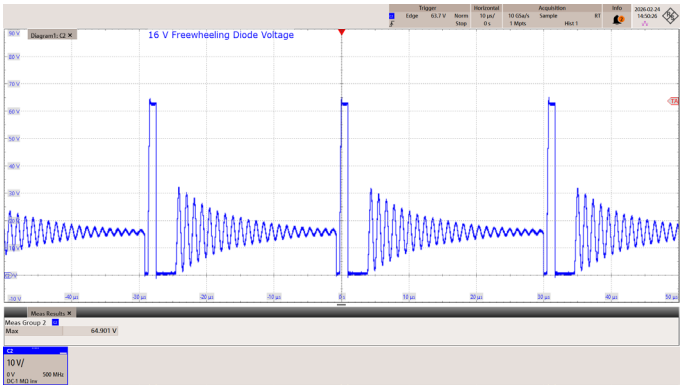


Figure 61 – 16 V Freewheeling Diode Voltage
800 VDC, Full-Load, Steady-State.
CH2: $V_{FREEWHELING\_DIODE}$, 10 V / div.
Time Scale: 10 µs / div.
$V_{FREEWHELING\_DIODE(MAX)}$: 64.9 V

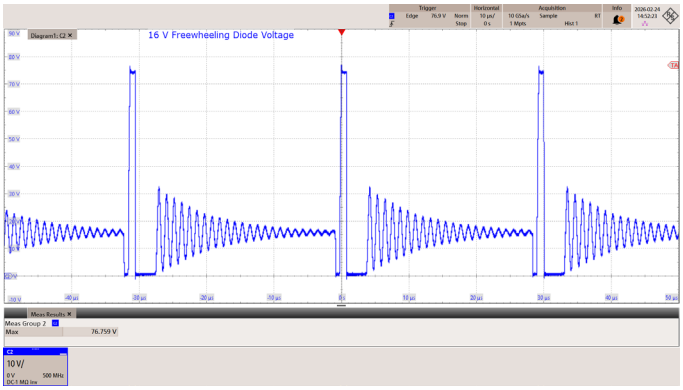


Figure 62 – 16 V Freewheeling Diode Voltage
1000 VDC, Full-Load, Steady-State.
CH2: $V_{FREEWHELING\_DIODE}$, 10 V / div.
Time Scale: 10 µs / div.
$V_{FREEWHELING\_DIODE(MAX)}$: 76.8 V

9.2.4 Maximum Voltage Stress

The voltage measured across each key component was checked at 1000 VDC input. Maximum voltage stress can occur under different combinations of input line voltages, output loads, start-up and load step. Most design specifications call for 10% ~ 20% margin between the maximum voltage stress and component rating. Table 6 lists the maximum voltage stress on key components:

Component	Part Number	Component Rating [V]	Voltage Stress	
			[V]	Derating [%]
InnoMux-2 (U1)	IMX2353F-H418	1700	1458	**85.8**
24 V_{OUT} SR FET (Q1)	AONS66520	150	129	**86**
16 V_{OUT} Freewheeling Diode (D2)	V12P10-M3/86A	100	82.7	**82.7**

Table 6 – Maximum Voltages on key components.

9.3 Dynamic Load Response

Dynamic load response was measured using an electronic load configured in dynamic constant-current mode and switched at a frequency of 10 Hz. The test showed the PSU transient response to step load changes by monitoring output voltage overshoot and undershoot. A 50% duty cycle was applied, with a load-step slew rate of 800 mA/μs. Output voltage waveforms were measured directly at the PCB. See sample waveforms in figures 63 to 68.

16 V_{OUT} Dynamic Load						
Transient 16 V 10% - 100% Load and 24 V fixed at 10% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**24 V**	**16 V**	**16 V**		**% 16 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	60 mA (10%)	35 mA (10%) - 350 mA (100%)	16	14.3	0.00	-10.6
800	60 mA (10%)	35 mA (10%) - 350 mA (100%)	16.1	14.6	0.63	-8.75
1000	60 mA (10%)	35 mA (10%) - 350 mA (100%)	16.1	14.6	0.63	-8.75
Transient 16 V 10% - 100% Load and 24 V fixed at 100% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**24 V**	**16 V**	**16 V**		**% 16 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	600 mA (100%)	35 mA (10%) - 350 mA (100%)	18.1	15.5	13.1	-3.13
800	600 mA (100%)	35 mA (10%) - 350 mA (100%)	17.8	15.5	11.3	-3.13
1000	600 mA (100%)	35 mA (10%) - 350 mA (100%)	18	15.5	12.5	-3.13

24 V_{OUT} Dynamic Load						
Transient 24 V 10% - 100% Load and 16 V_{OUT} fixed at 10% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**16 V**	**24 V**	**24 V**		**% 24 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	35 mA (10%)	60 mA (10%) - 600 mA (100%)	24.5	23.7	2.08	-1.25
800	35 mA (10%)	60 mA (10%) - 600 mA (100%)	24.5	23.7	2.08	-1.25
1000	35 mA (10%)	60 mA (10%) - 600 mA (100%)	24.5	23.7	2.08	-1.25
Transient 24 V 10% - 100% Load and 16 V fixed at 10% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**16 V**	**24 V**	**16 V**		**% 16 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	35 mA (10%)	60 mA (10%) - 600 mA (100%)	18.3	15.5	14.4	-3.13
800	35 mA (10%)	60 mA (10%) - 600 mA (100%)	18.1	15.5	13.1	-3.13
1000	35 mA (10%)	60 mA (10%) - 600 mA (100%)	18.3	15.5	14.4	-3.13

Transient 24 V 10% - 100% Load and 16 V fixed at 100% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**16 V**	**24 V**	**24 V**		**% 24 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	350 mA (100%)	60 mA (10%) - 600 mA (100%)	24.5	23.6	2.08	-1.67
800	350 mA (100%)	60 mA (10%) - 600 mA (100%)	24.5	23.7	2.08	-1.25
1000	350 mA (100%)	60 mA (10%) - 600 mA (100%)	24.5	23.7	2.08	-1.25
Transient 24 V 10% - 100% Load and 16 V fixed at 100% Load						
10 Hz, Duty cycle = 50%, Slew Rate = 0.8 A / ms, 10% - 100% Dynamic Load						
Input	**16 V**	**24 V**	**16 V**		**% 16 V**	
VDC	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$V_{O(MAX)}$ (V)**	**$V_{O(MIN)}$ (V)**	**$V_{O(MAX)}$ (%)**	**$V_{O(MIN)}$ (%)**
200	350 mA (100%)	60 mA (10%) - 600 mA (100%)	16.3	14.1	1.9	-11.9
800	350 mA (100%)	60 mA (10%) - 600 mA (100%)	16.3	14.4	1.9	-10.0
1000	350 mA (100%)	60 mA (10%) - 600 mA (100%)	16.4	14.5	2.5	-9.38

Table 7 – 16 V and 24 V Dynamic Load Response Summary, 10 – 100% Load, 10 Hz, 50% Duty Cycle, Slew Rate = 0.8 A / ms.

9.3.1 16 V Step Load Transient Response

9.3.1.1 Transient 16 V 10% - 100% Load and 24 V fixed at 10% Load

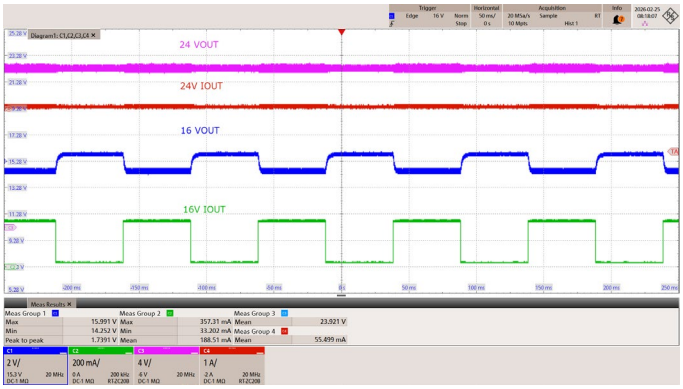


Figure 63 – 200 VDC, Dynamic Load
16 V 35 mA (10%) → 350 mA (100%)
24 V 60 mA (10%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 16 V
$V_{OUT(16V)\_MIN}$: 14.3 V

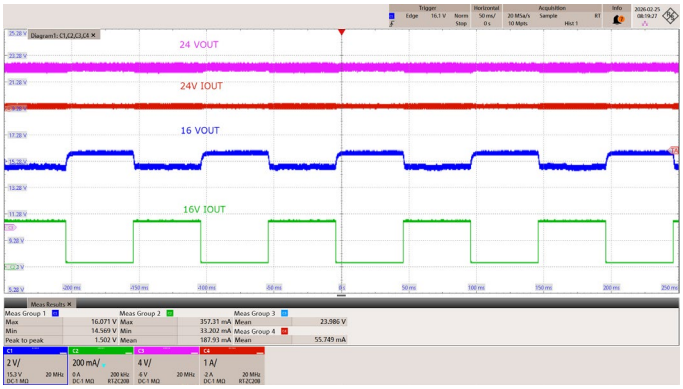


Figure 64 – 800 VDC, Dynamic Load
16V 35 mA (10%) → 350 mA (100%)
24 V 600 mA (10%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 16.1 V
$V_{OUT(16V)\_MIN}$: 14.6 V

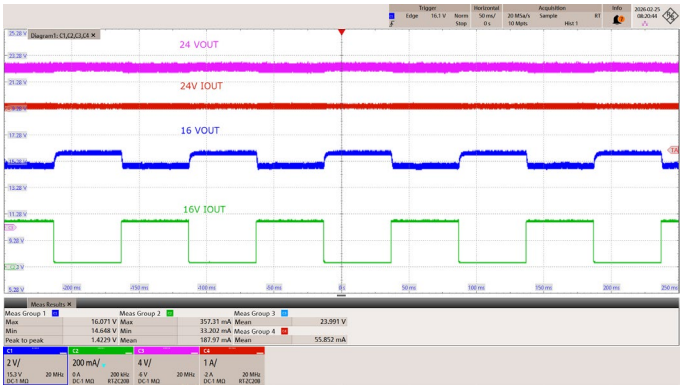


Figure 65 – 1000 VDC, Dynamic Load
16 V 35 mA (10%) → 350 mA (100%)
24 V 60 mA (10%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 16.1 V
$V_{OUT(16V)\_MIN}$: 14.6 V

9.3.1.2 Transient 16 V 10% - 100% Load and 24 V fixed at 100% Load

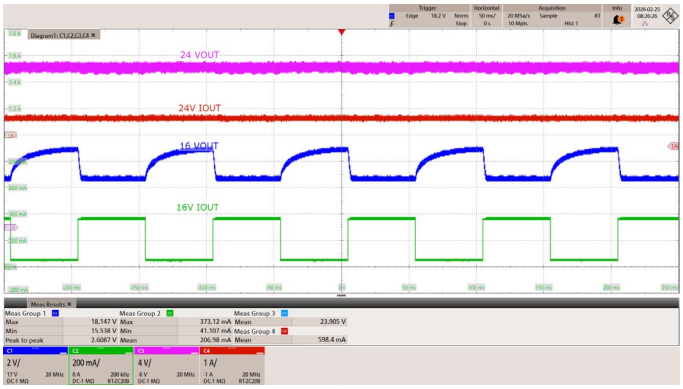


Figure 66 – 200 VDC, Dynamic Load
16 V 35 mA (10%) → 350 mA (100%)
24 V 600 mA (100%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 18.1 V
$V_{OUT(16V)\_MIN}$: 15.5 V

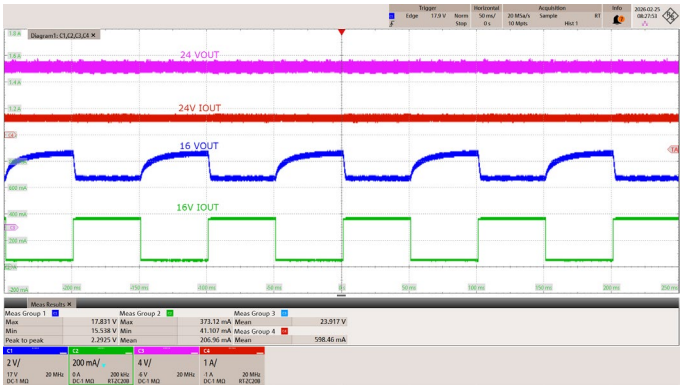


Figure 67 – 800 VDC, Dynamic Load
16 V 35 mA (10%) → 350 mA (100%)
24 V 600 mA (100%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 17.8 V
$V_{OUT(16V)\_MIN}$: 15.5 V

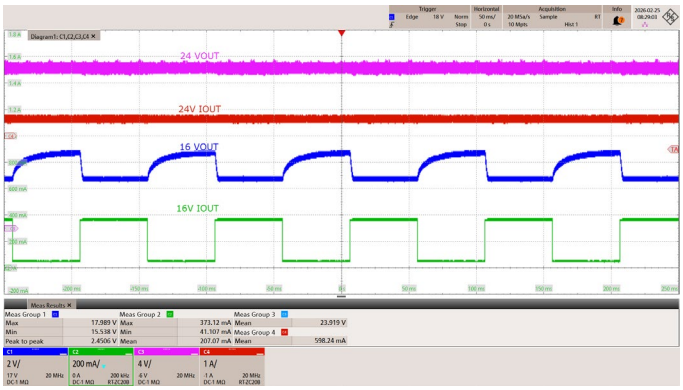


Figure 68 – 1000 VDC, Dynamic Load
16 V 35 mA (10%) → 350 mA (100%)
24 V 600 mA (100%) fixed.
CH1: $V_{OUT\_(16V)}$, 2 V / div.
CH2: $I_{OUT\_(16V)}$, 200 mA/div.
CH3: $V_{OUT\_(24V)}$, 4 V / div.
CH4: $I_{OUT\_(24V)}$, 1 A / div.
$V_{OUT(16V)\_MAX}$: 18 V
$V_{OUT(16V)\_MIN}$: 15.5 V

9.3.2 24 V Step Load Transient Response

9.3.2.1 Transient 24 V 10% - 100% Load and 16 V fixed at 10% Load

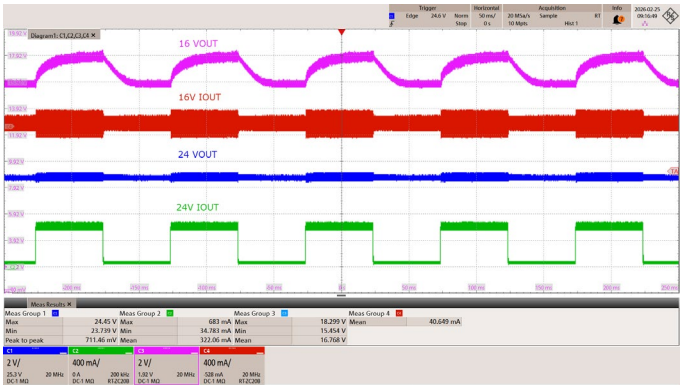


Figure 69 – 200 VDC, Dynamic Load
16 V 35 mA (10%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 400 mA / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.7 V
$V_{OUT(16V)\_MAX}$: 18.3 V
$V_{OUT(16V)\_MIN}$: 15.5 V

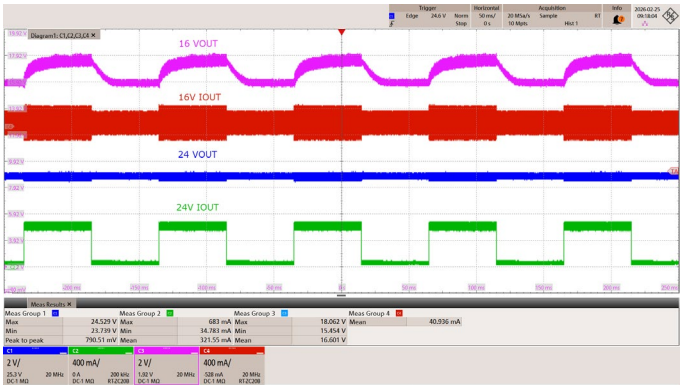


Figure 70 – 800 VDC, Dynamic Load
16 V 35 mA (10%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 400 mA / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.7 V
$V_{OUT(16V)\_MAX}$: 18.1 V
$V_{OUT(16V)\_MIN}$: 15.5 V

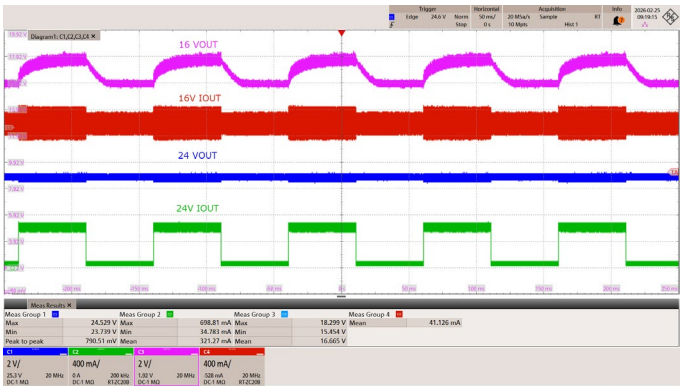


Figure 71 – 1000 VDC, Dynamic Load
16 V 35 mA (10%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 400 mA / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.7 V
$V_{OUT(16V)\_MAX}$: 18.3 V
$V_{OUT(16V)\_MIN}$: 15.5 V

9.3.2.2 Transient 24 V 10% - 100% Load and 16 V fixed at 100% Load

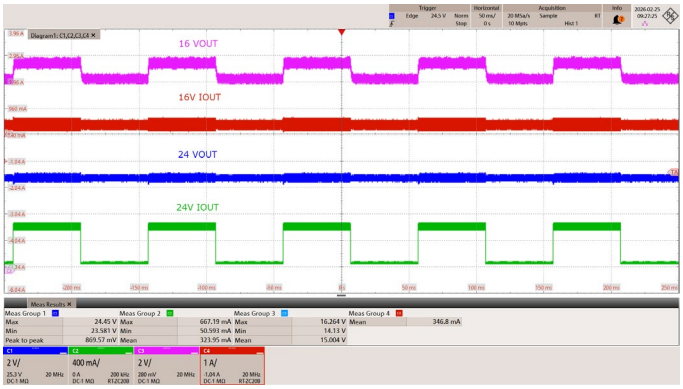


Figure 72 – 200 VDC, Dynamic Load
16 V 350 mA (100%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 1 A / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.6 V
$V_{OUT(16V)\_MAX}$: 16.3 V
$V_{OUT(16V)\_MIN}$: 14.1 V

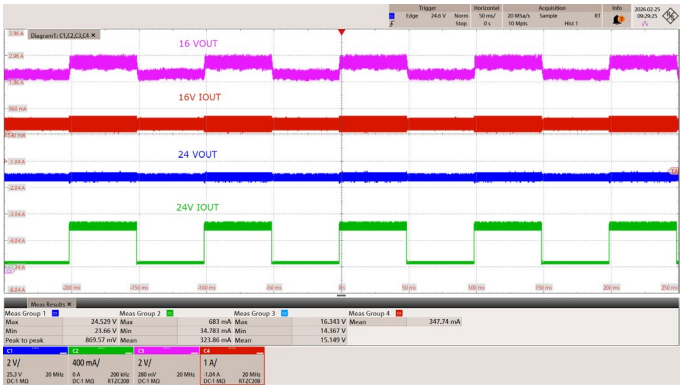


Figure 73 – 800 VDC, Dynamic Load
16 V 350 mA (100%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 1 A / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.7 V
$V_{OUT(16V)\_MAX}$: 16.3 V
$V_{OUT(16V)\_MIN}$: 14.4 V

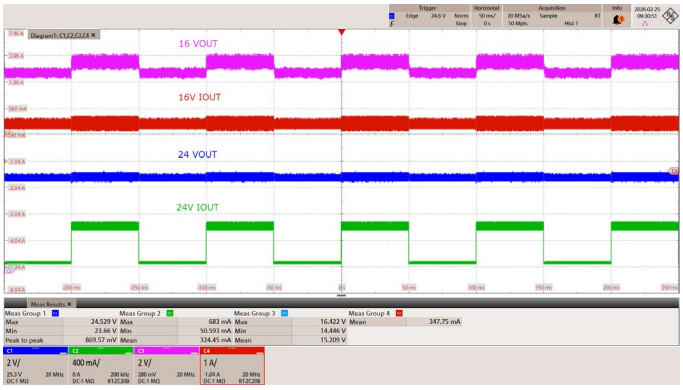
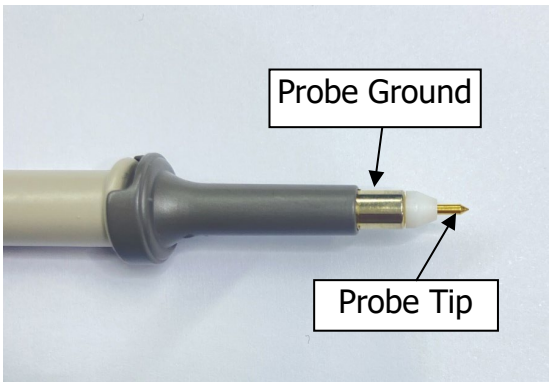


Figure 74 – 1000 VDC, Dynamic Load
16 V 350 mA (100%) fixed.
24 V 60 mA (10%) → 600 mA (100%)
CH1: $V_{OUT\_(24V)}$, 2 V / div.
CH2: $I_{OUT\_(24V)}$, 400 mA/div.
CH3: $V_{OUT\_(16V)}$, 2 V / div.
CH4: $I_{OUT\_(16V)}$, 1 A / div.
$V_{OUT(24V)\_MAX}$: 24.5 V
$V_{OUT(24V)\_MIN}$: 23.7 V
$V_{OUT(16V)\_MAX}$: 16.4 V
$V_{OUT(16V)\_MIN}$: 14.5 V

9.4 Output Ripple Measurements

9.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to minimize noise pick-up. The probe adapter configuration is shown below. It includes a coaxial cable with two parallel capacitors connected to the measurement points. The capacitors are a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.



End Cap and Ground Lead Removed.

Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement.

9.4.2 Output Voltage Ripple at constant 100% load

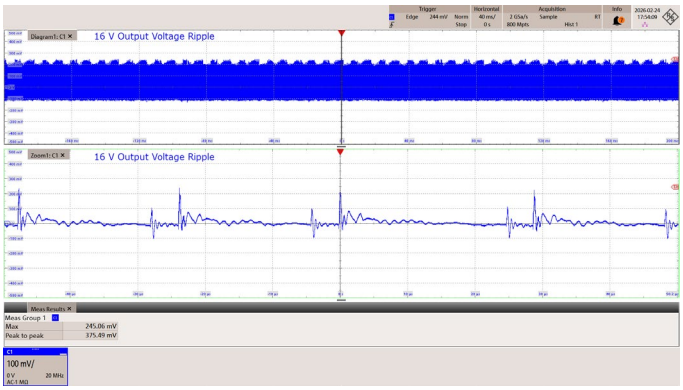


Figure 76 – 16 V Output Ripple Voltage
200 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(16V)RIPPLE}$, 100 mV / div.
Time Scale: 40 ms / div. (10 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 375 mVpp

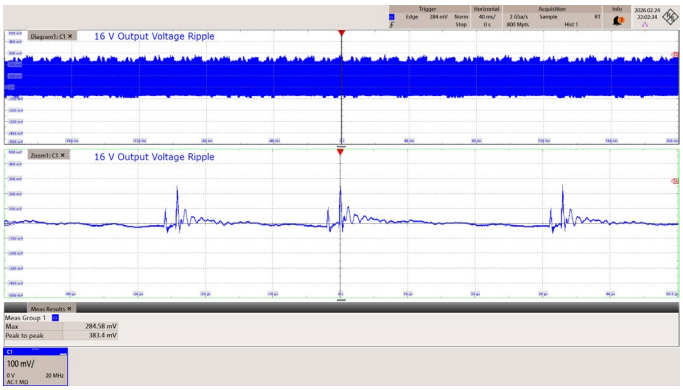


Figure 77 – 16 V Output Ripple Voltage
800 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(16V)RIPPLE}$, 100 mV / div.
Time Scale: 40 ms / div. (10 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 383 mVpp

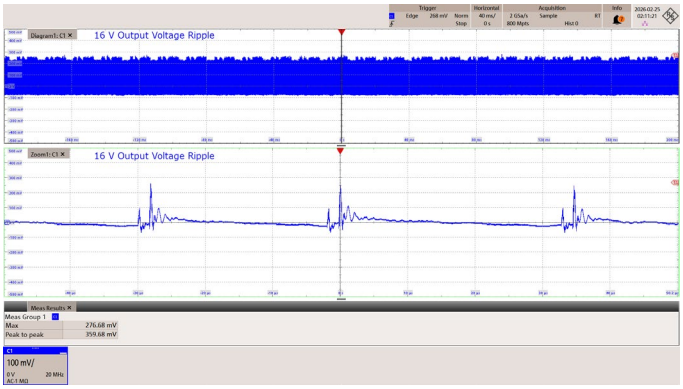


Figure 78 – 16 V Output Ripple Voltage
1000 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(16V)RIPPLE}$, 100 mV / div.
Time Scale: 40 ms / div. (10 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 360 mVpp

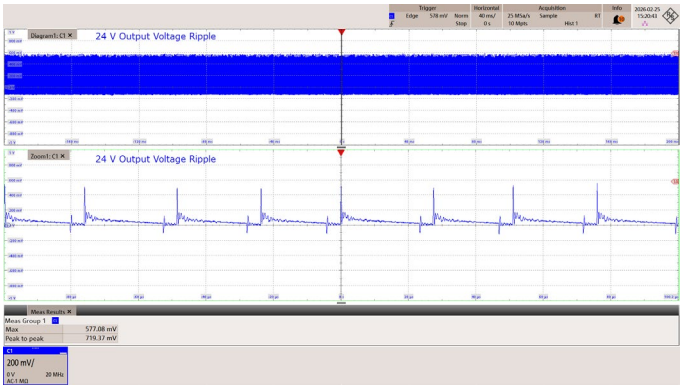


Figure 79 – 24 V Output Ripple Voltage
200 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(24V)RIPPLE}$, 200 mV / div.
Time Scale: 40 ms / div. (20 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 719 mVpp

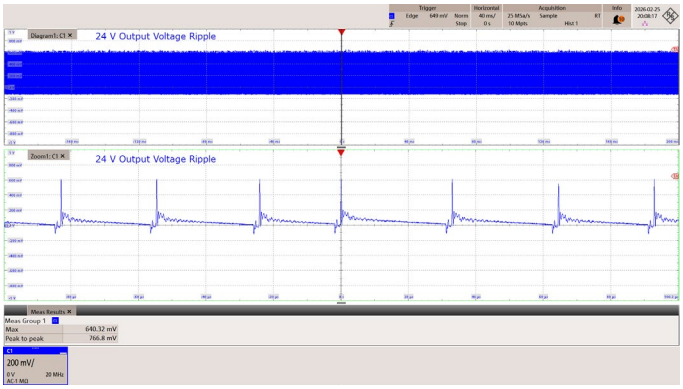


Figure 80 – 24 V Output Ripple Voltage
800 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(24V)RIPPLE}$, 200 mV / div.
Time Scale: 40 ms / div. (20 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 767 mVpp

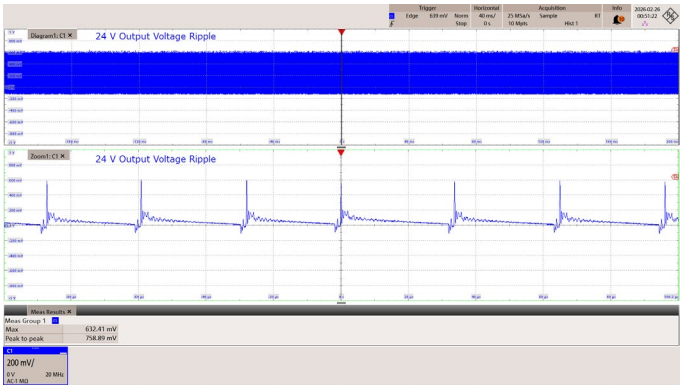


Figure 81 – 24 V Output Ripple Voltage
1000 VDC, Full-Load, Steady-State.
CH1: $V_{OUT\_(24V)RIPPLE}$, 200 mV / div.
Time Scale: 40 ms / div. (20 μs / div. Zoom)
$V_{OUT\_(16V)RIPPLE}$: 759 mVpp

9.4.3 Output Ripple vs Load

9.4.3.1 16 V Output Ripple

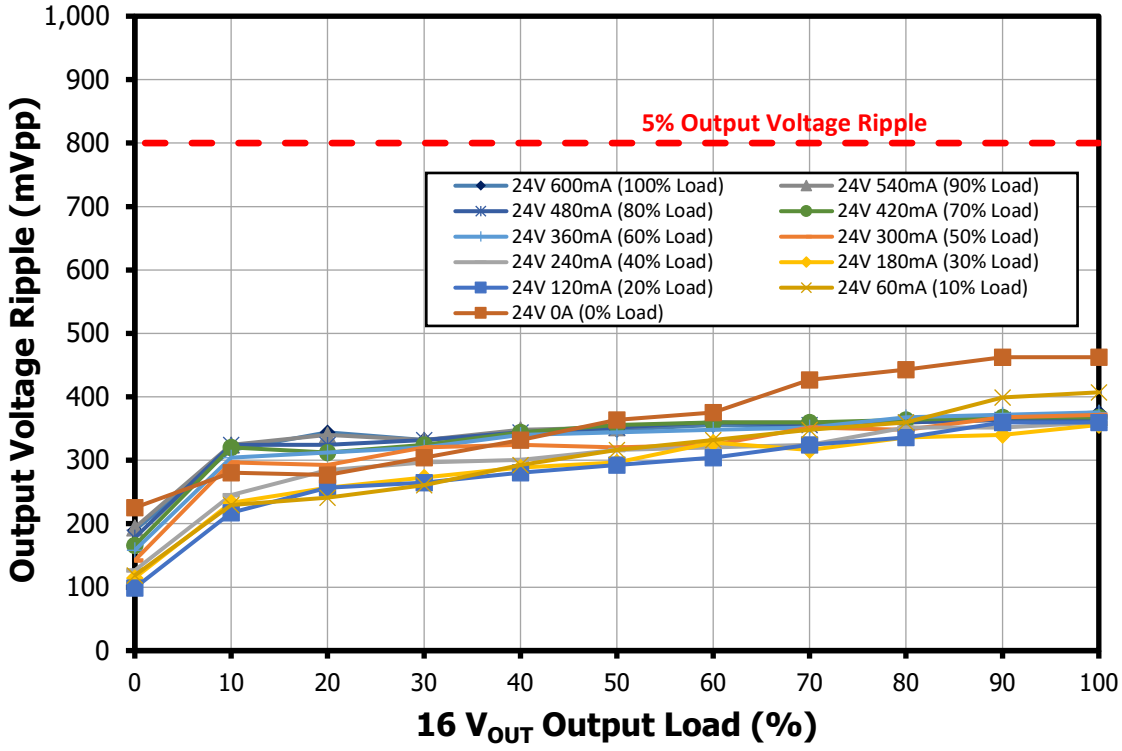


Figure 82 – 16 V Output Ripple vs. Load at 200 VDC Input Voltage, Room Temperature.

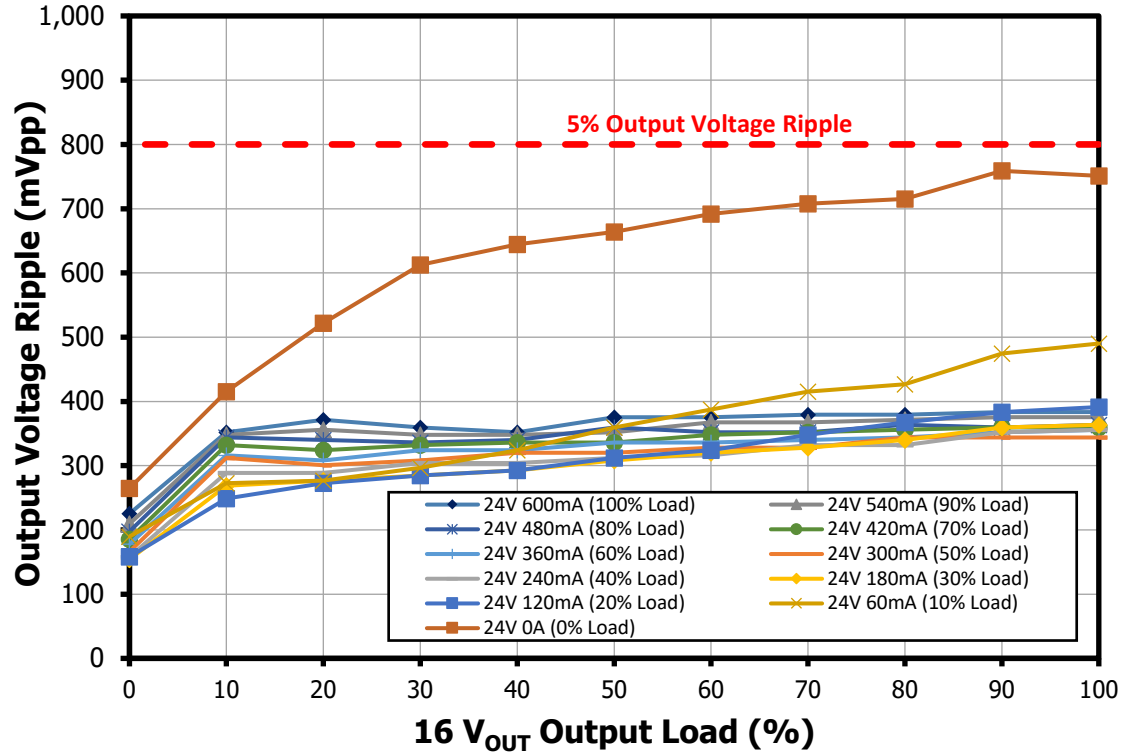


Figure 83 – 16 V Output Ripple vs. Load at 800 VDC Input Voltage, Room Temperature.

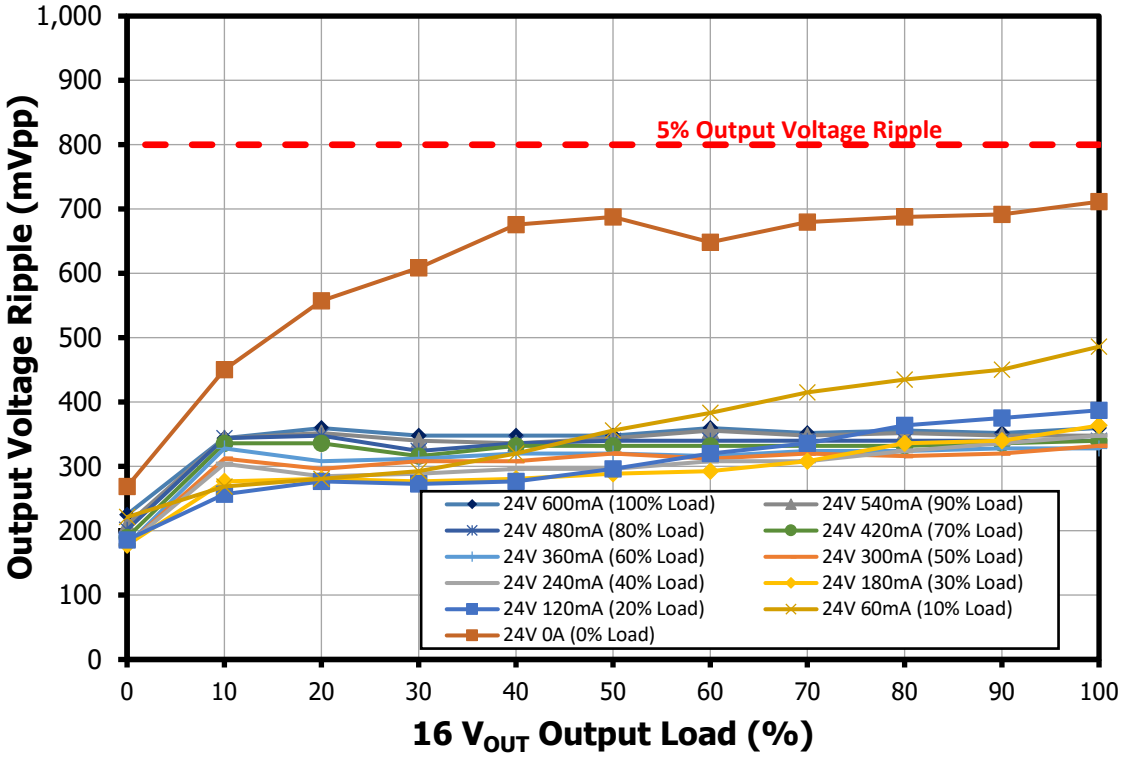


Figure 84 – 16 V Output Ripple vs. Load at 1000 VDC Input Voltage, Room Temperature.

9.4.3.2 24 V Output Ripple

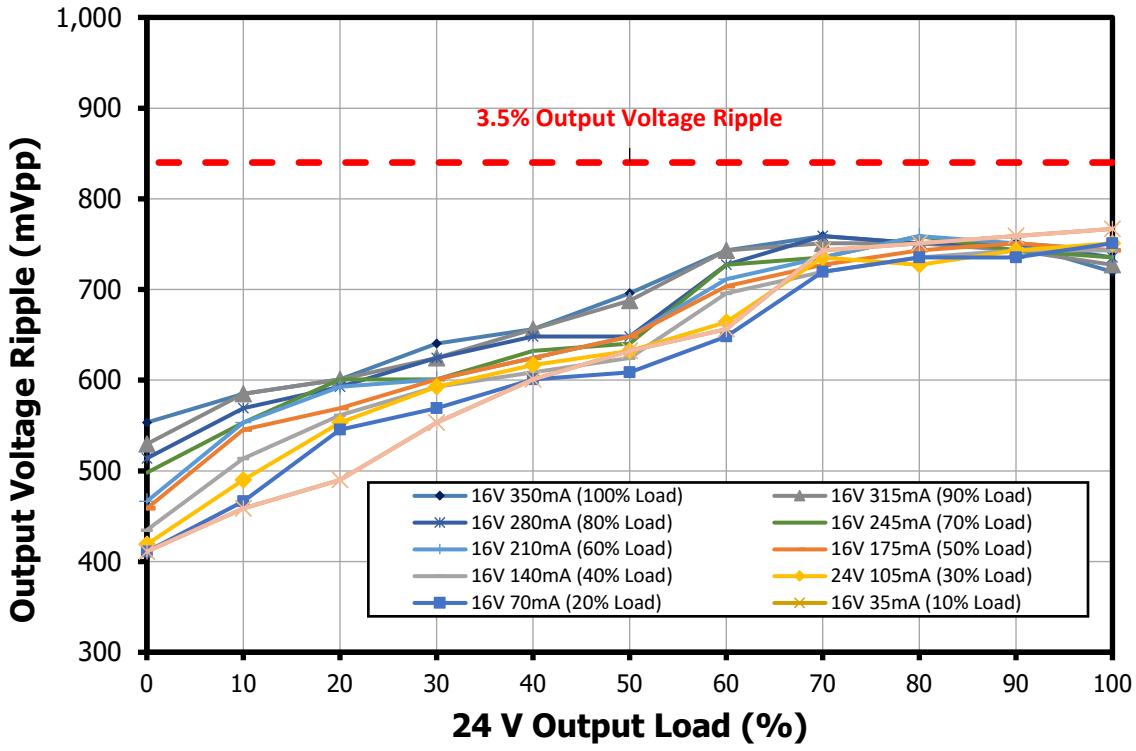


Figure 85 – 24 V Output Ripple vs. Load at 200 VDC Input Voltage, Room Temperature.

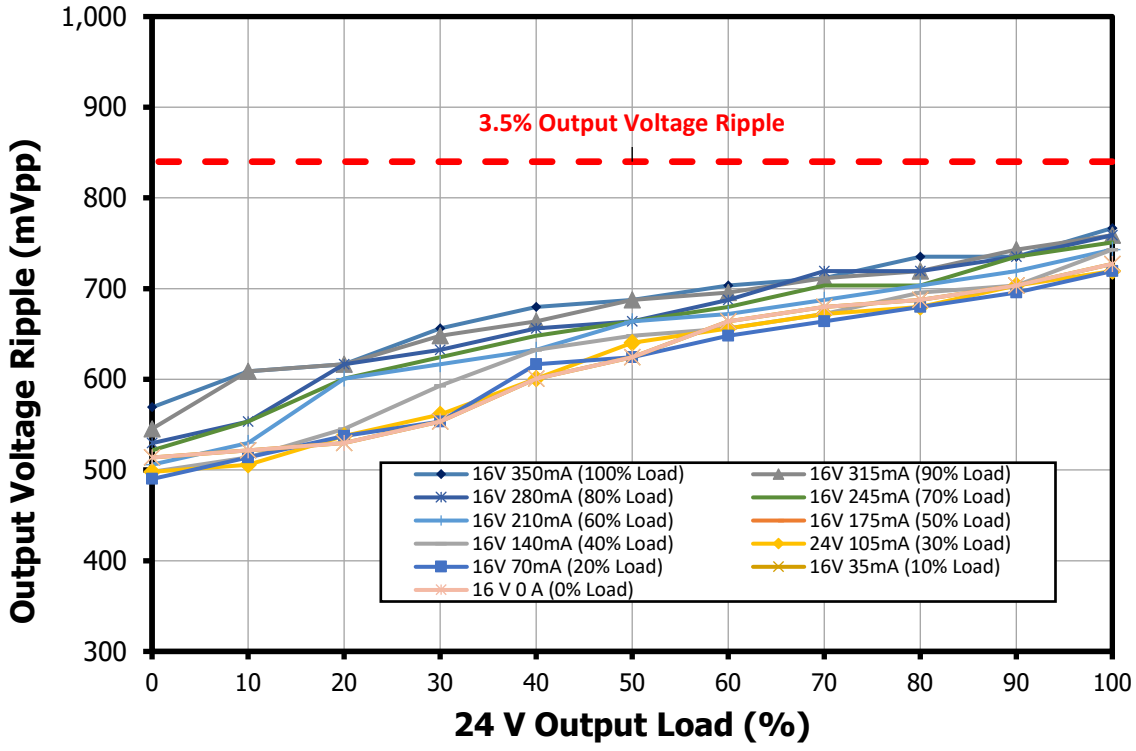


Figure 86 – 24 V Output Ripple vs. Load at 800 VDC Input Voltage, Room Temperature.

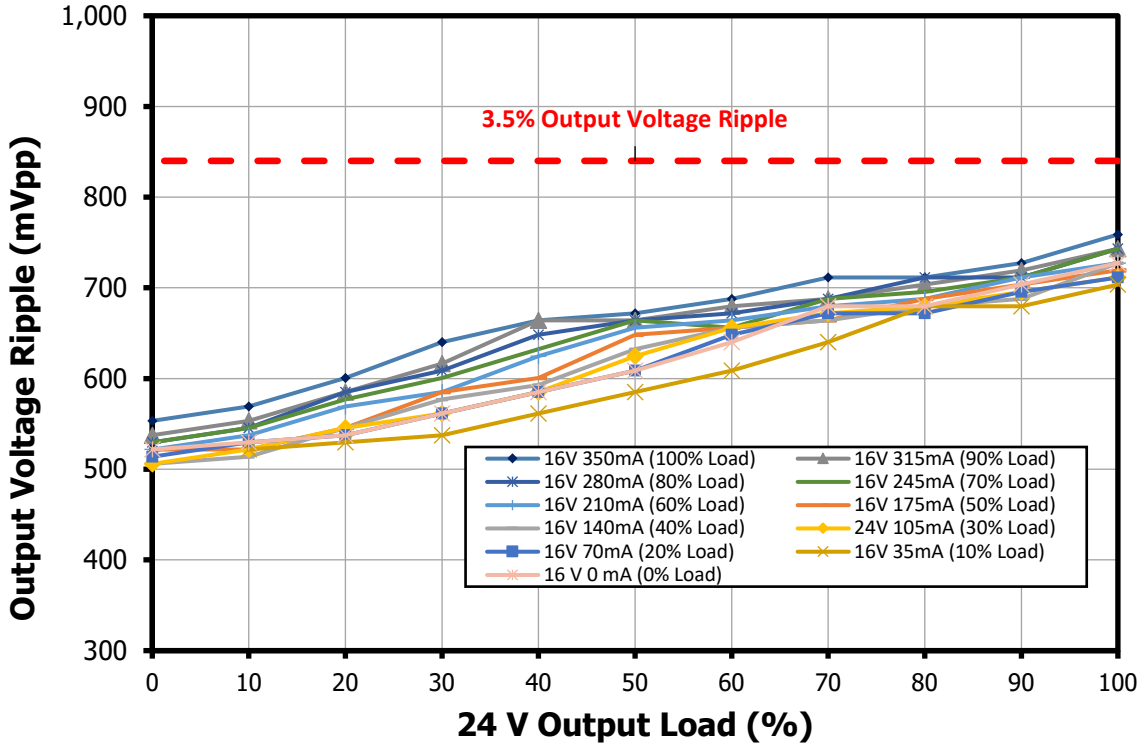


Figure 87 – 24 V Output Ripple vs. Load at 1000 VDC Input Voltage, Room Temperature.

9.5 Thermal Performance

The open frame was placed inside a large enclosure to restrict convective airflow that might affect the thermal measurements. No forced air-cooling was deployed during the test.

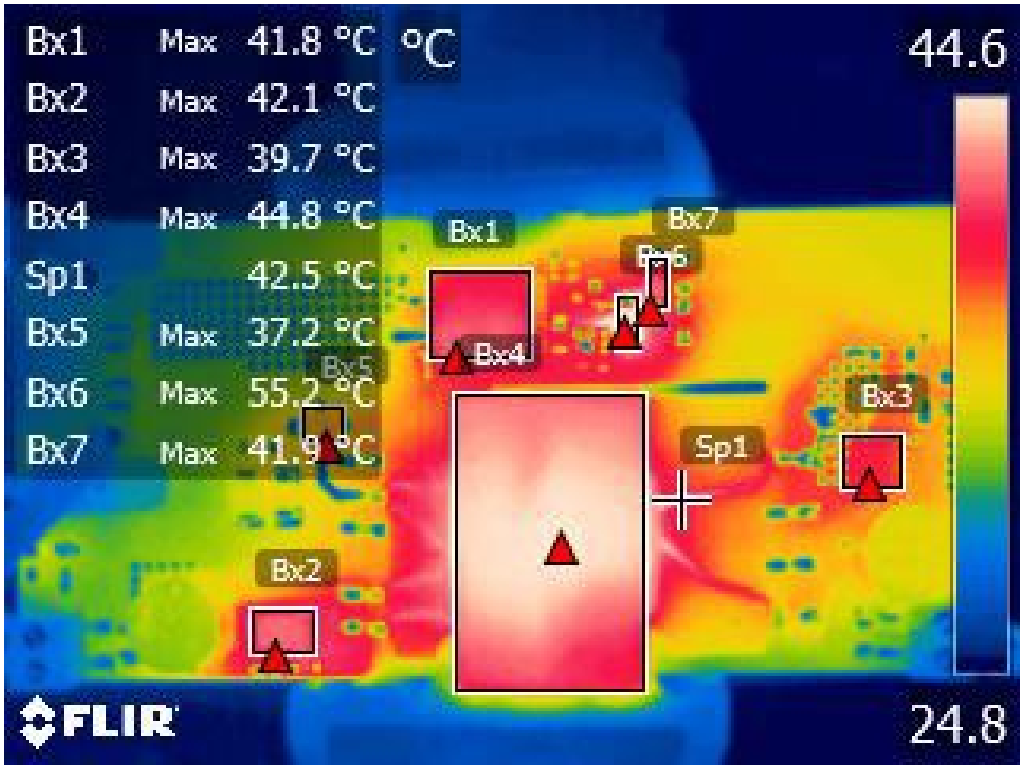
9.5.1 Thermal testing at Room Temperature

Figure 88 – Thermal Scan Test Set-up.

9.5.1.1 Thermal Test Data Summary at 25 °C Ambient Temperature

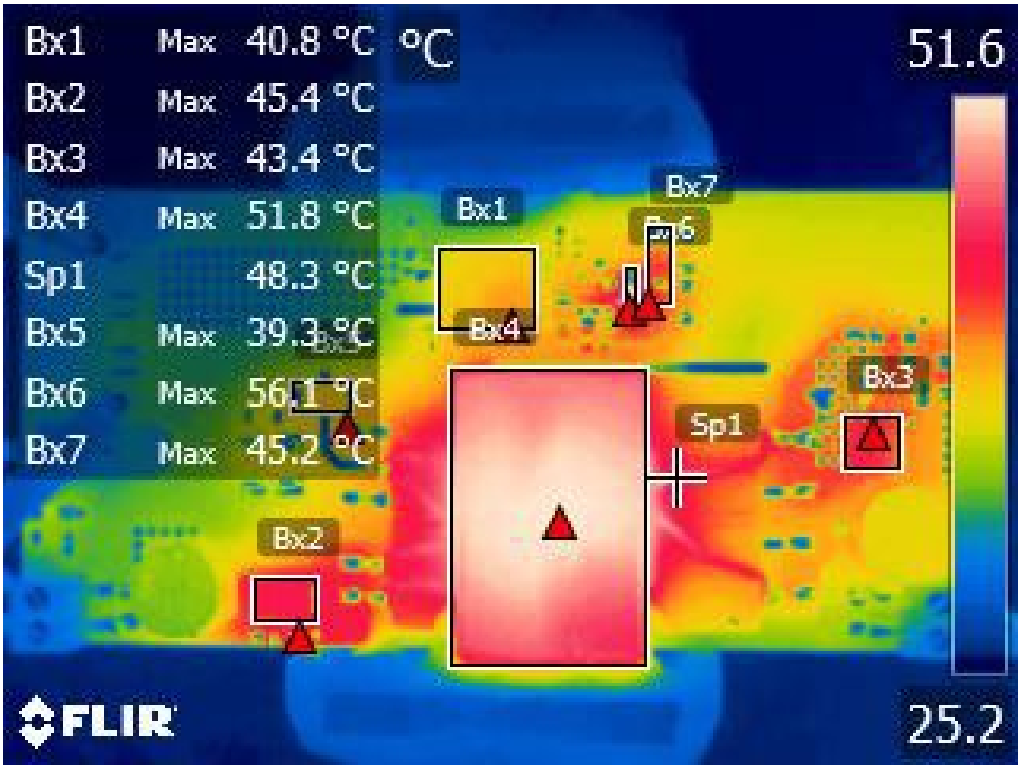
The following thermal scan data shows that the heating components remain well below their maximum temperature ratings across the entire input voltage range.

	Ref	Description	Component Temperature [°C]		
			V_{IN} = 300 VDC	V_{IN} = 800 VDC	V_{IN} = 1000 VDC
Bx1	U1	IMX2353F	41.8	40.8	41
Bx2	D2	16 V Output Diode	42.1	45.4	46.2
Bx3	Q1	AONS66520	39.7	43.4	44.3
Bx4	T1	EIQ Transformer Core	44.8	51.8	54.9
Sp1	T1	EIQ Transformer Secondary Winding	42.5	48.3	49
Bx5	D3	Primary Diode Clamp	37.2	39.3	40
Bx6	R16	24 V to BPS Resistor, 2.43 kΩ	55.2	56.1	55.5
Bx7	D4	24 V to BPS Diode	41.9	45.2	45.1
Ambient Temperature [°C]			**25.1**	**25.1**	**25.3**



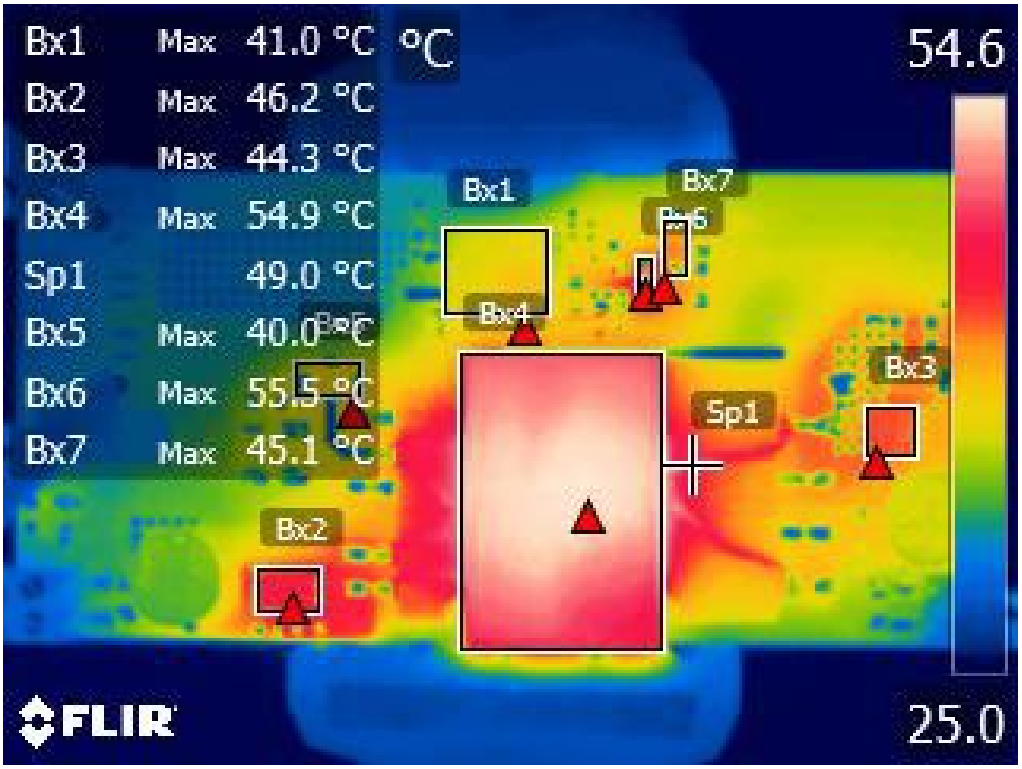
	Ref	Component	Temperature (°C)
Bx1	U1	IMX2353F	41.8
Bx2	D2	16 V Output Diode	42.1
Bx3	Q1	AONS66520	39.7
Bx4	T1	EIQ Transformer Core	44.8
Sp1	T1	EIQ Transformer Secondary Winding	42.5
Bx5	D3	Primary Diode Clamp	37.2
Bx6	R16	24 V to BPS Resistor, 2.43 kΩ	55.2
Bx7	D4	24 V to BPS Diode	41.9
Ambient Temperature [°C]			**25.1**

Figure 89 – Thermal Image, 200 VDC, Full Load.



	Ref	Component	Temperature (°C)
Bx1	U1	IMX2353F	40.8
Bx2	D2	16 V Output Diode	45.4
Bx3	Q1	AONS66520	43.4
Bx4	T1	EIQ Transformer Core	51.8
Sp1	T1	EIQ Transformer Secondary Winding	48.3
Bx5	D3	Primary Diode Clamp	39.3
Bx6	R16	24 V to BPS Resistor, 2.43 kΩ	56.1
Bx7	D4	24 V to BPS Diode	45.2
Ambient Temperature [°C]			**25.1**

Figure 90 – Thermal Image, 800 VDC, Full Load.



	Ref	Component	Temperature (°C)
Bx1	U1	IMX2353F	41.0
Bx2	D2	16 V Output Diode	46.2
Bx3	Q1	AONS66520	44.3
Bx4	T1	EIQ Transformer Core	54.9
Sp1	T1	EIQ Transformer Secondary Winding	49.0
Bx5	D3	Primary Diode Clamp	40.0
Bx6	R16	24 V to BPS Resistor, 2.43 kΩ	55.5
Bx7	D4	24 V to BPS Diode	45.1
Ambient Temperature [°C]			**25.3**

Figure 91 – Thermal Image, 1000 VDC, Full Load.

9.5.2 Thermal testing at 105 °C Ambient Temperature

The PSU was placed inside a closed box to prevent air flow affecting the thermal measurement. Ambient temperature inside the thermal chamber is 105 °C and was kept constant for 100 minutes before taking measurements. Thermal data were measured using a thermocouple and a Yokogowa data logger.

Figure 92 – Test Set-Up Picture – Unit Inside Mechanical Casing.

9.5.2.1 Thermal Test Data Summary at 105 °C Ambient Temperature

The following thermal scan data shows that the heating components remain well below their maximum temperature ratings across the entire input voltage range.

Thermal Test Data Summary				
Ref Des.	**Description**	**Component Temperature [°C]**		
		200 VDC	**800 VDC**	**1000 VDC**
U1	IMX2353F	116	114	115
R10	24 V Snubber resistor	114	116	117
Q1	24 V SR FET AONS66520	115	117	118
T1	EIQ Transformer Core	119	124	126
FD4	Transformer Secondary Winding	116	119	121
D7	EIQ Transformer Primary Winding	117	120	121
D2	16 V Output Diode	117	119	120
R16	24 V to BPS resistor	123	123	123
D2	24 V to BPS diode	116	115	115
R5	16 V Snubber Resistor	115	117	117
Amb	**Ambient**	**104**	**104**	**103**

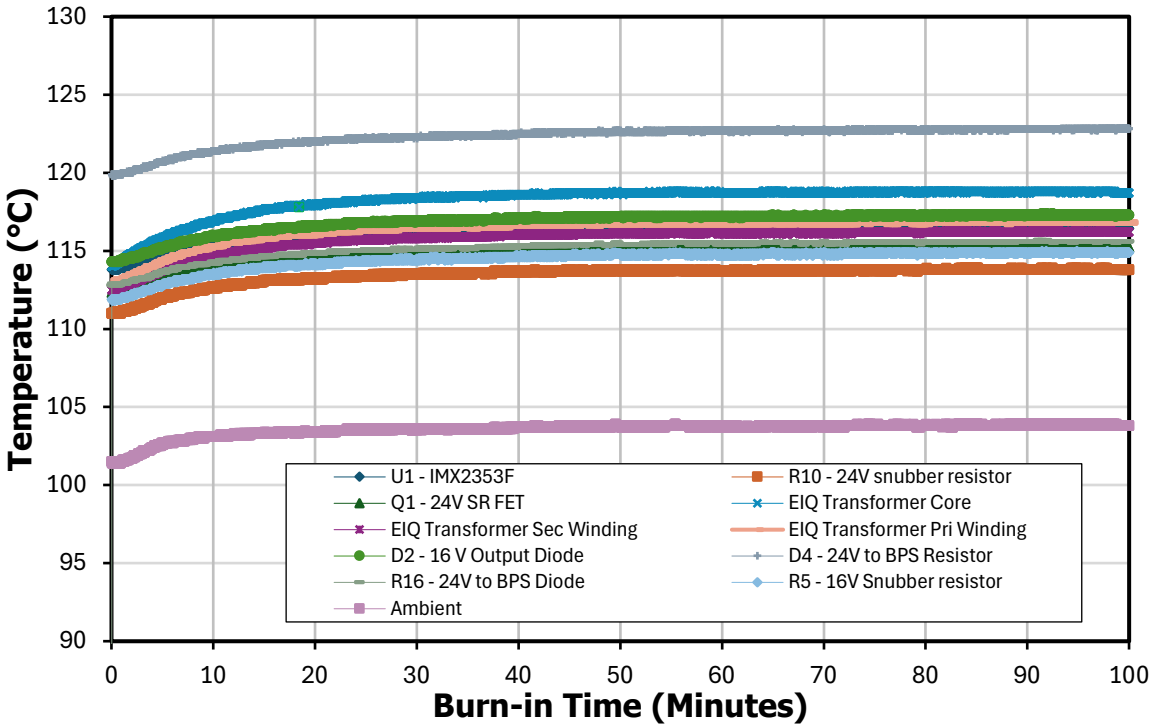


Figure 93 – 200 VDC Full Load, 105 °C Thermal Performance.

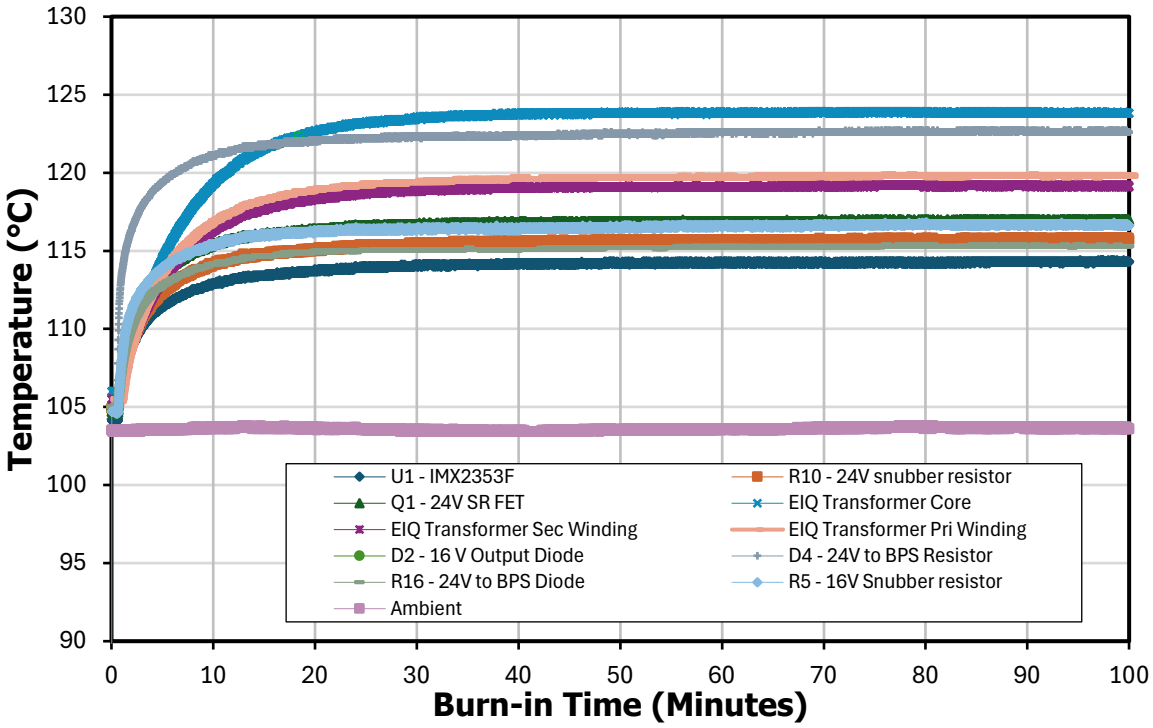


Figure 94 – 800 VDC Full Load, 105 °C Thermal Performance.

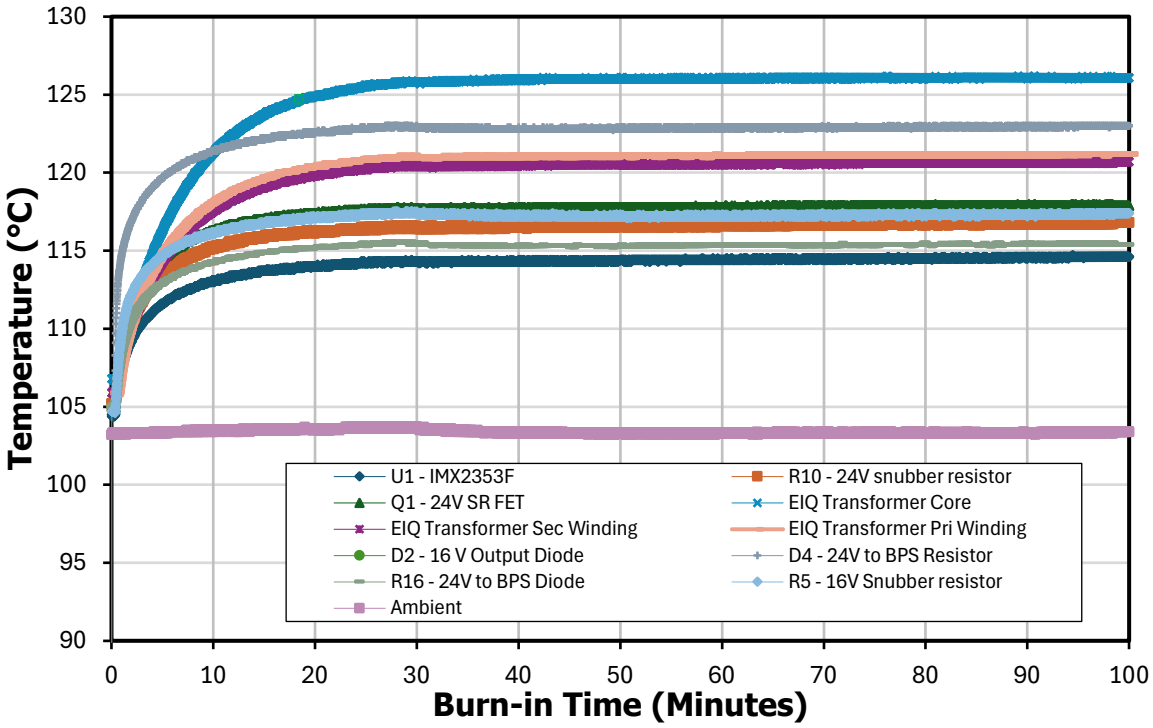


Figure 95 – 1000 VDC Full Load, 105 °C Thermal Performance.

10 Revision History

Date	Author	Revision	Description & Changes	Reviewed
29-Apr-2026	JKL	A	Initial Release.	Apps & Mktg

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