Design Example Report

Title	**100 W Isolated Flyback Power Supply Using a 1700 V InnoMux™2-EP IC IMX2353F-H418**
Specification	300 VDC – 1000 VDC Input; 24 V / 4.2 A Output
Application	Industrial and Appliance Applications
Author	Applications Engineering Department
Document Number	DER-1087
Date	November 4, 2025
Revision	A

Summary and Features

- Ultra-wide range input
- >90% full load efficiency
    - Zero Voltage switching (ZVS)
    - 1700 V PowiGaN™ primary switch
    - Synchronous Rectification (SR)
- Constant high efficiency across input voltage and load range
- Accurate regulation – better than ±1% across line and load
- Very low component count: (less than 50 parts)
- Safety features
    - Output overvoltage protection (OVP)
    - Accurate thermal protection with wide hysteresis

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes 24 V / 4.2 A power supply intended for appliance and industrial applications, utilizing IMX2353F-H418 from the InnoMux™2-EP family of ICs.

The SMPS features a Constant Voltage (CV) output and can deliver a maximum output power of 100 W, with an input voltage of up to 1000 VDC. This design demonstrates high efficiency and accurate output regulation, made possible from the adaptive ZVS switching algorithm employed in InnoMux2 ICs.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

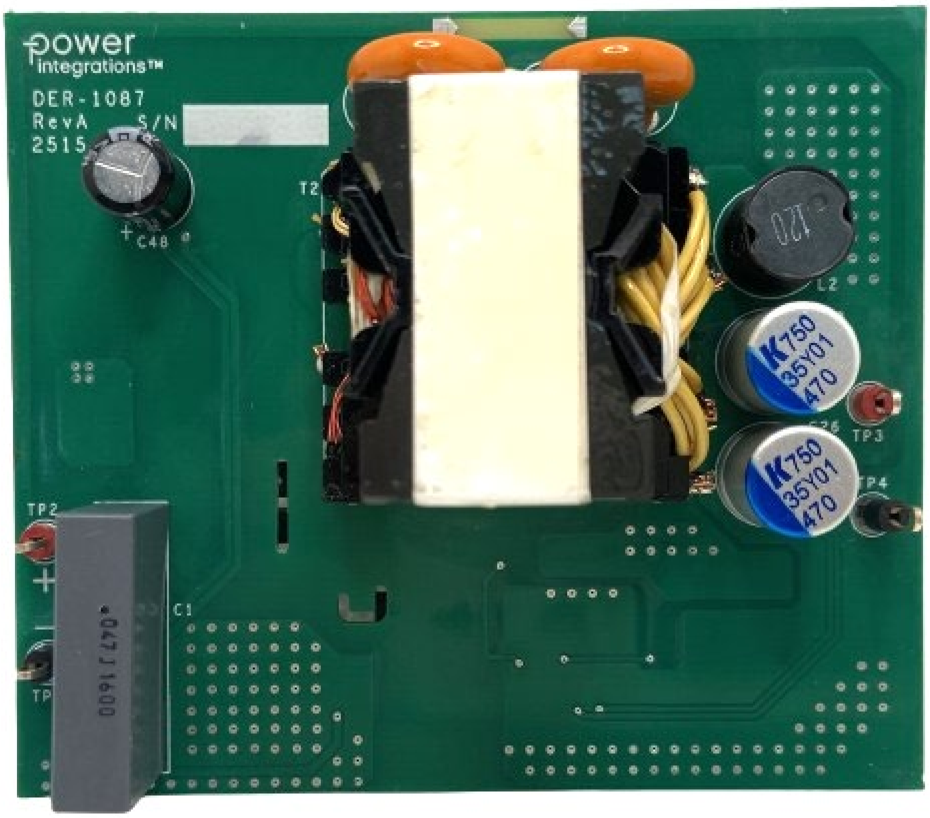


Figure 1 – Populated Circuit Board, Top View.

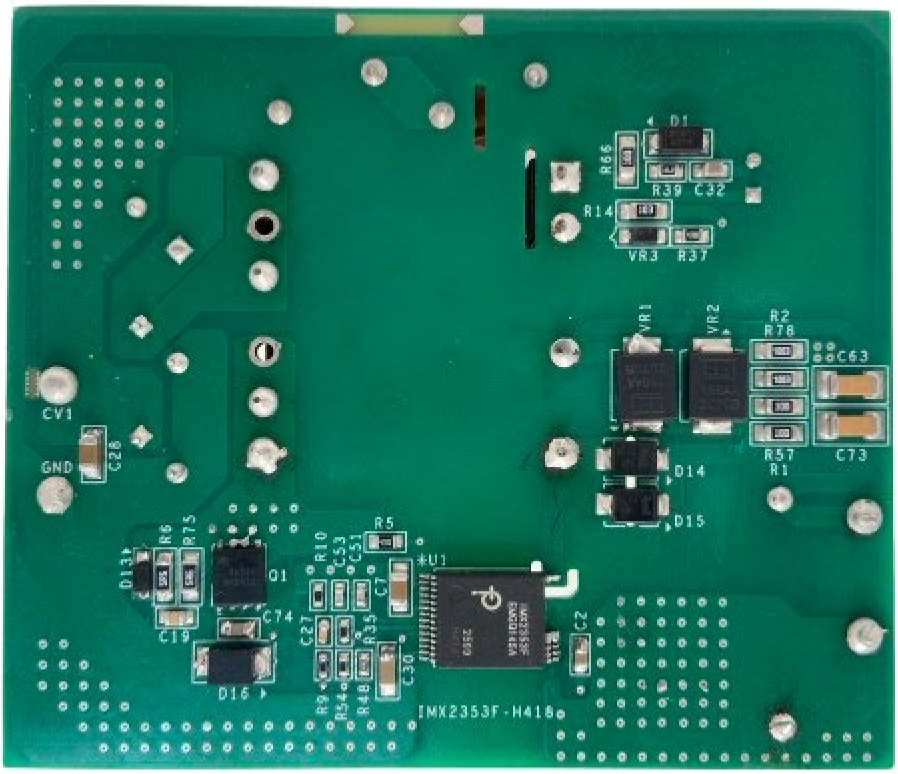


Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	300		1000	VDC	
Output						
VCV						
Rated Voltage	V_{CV1}		24.0		V	±1% initial set point tolerance
Line and Load Regulation[1]			±1%			Measured from 300 to 1000 VDC, 0% to 100% load
Dynamic Response			±5%			0-100% load step
Ripple Voltage	V_{CV1_RIPPLE}			500	mV	20 MHz Bandwidth, at 25 °C Ambient
Rated Current	I_{CV1}		4.2		A	
Total Output Power						
Output Power	P_{OUT}		100		W	300 – 1000 VDC input
Efficiency						
Full Load	η		90		%	Measured at 1000 VDC, 25 °C
			91	91.5	%	Measured at 800 VDC, 25 °C
			92	92.5	%	Measured at 500 VDC, 25 °C
			92	92.5	%	Measured at 300 VDC, 25 °C
Standby Input Power				<0.4	W	Measured at 500 VDC, 25 °C, CV1 200 mW
Environmental						
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Table 1 – Power Supply Specifications.

Note:

1. Measured across input line and load

3 Schematic

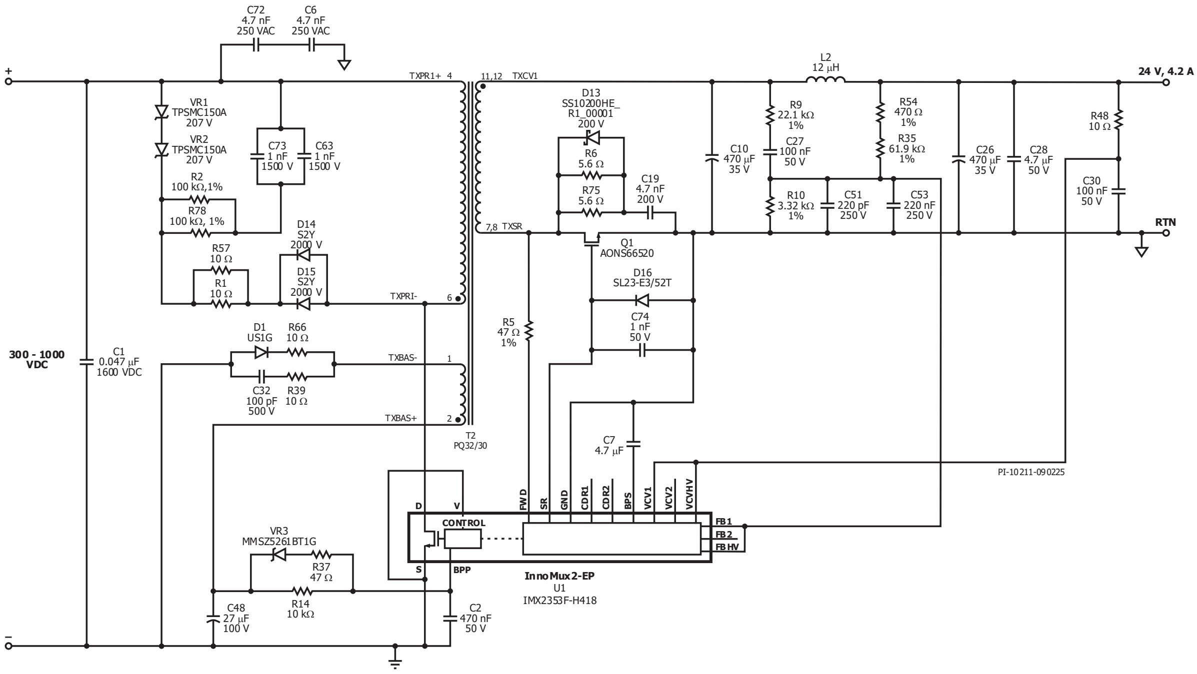


Figure 3 – Full Schematic.

4 Circuit Description

4.1 Primary-Side

4.1.1 Input Capacitor

The film capacitor C1 is connected in parallel with the DC input connector J3 and provides filtering for ripple on the DC input.

4.1.2 Primary Switching Circuit

The primary side of the transformer is connected between the input DC bus (TXPRI+) and the drain of the integrated primary switch of InnoMux2-EP IC (U1, pin 28). The primary current loop closes at the negative terminal of C2 via the S pin of U1 (pin 18/19). An RCD-type primary clamp (D14, D15, R1, R57, R2, R78, VR1, VR2, C63 and C73) is used to limit the peak drain voltage spike on the integrated primary switch, caused by the leakage inductance of the transformer when the switch turns off.

4.1.3 Primary-Side Controller Power Source

The primary-side controller is integrated into the InnoMux2-EP IC (U1). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor (C2) when AC voltage is first applied to the converter input. During normal operation (steady-state), the primary-side controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D1 and capacitor C48. Resistor R66 is inserted into the discharge circuit to limit transient current. The output of the primary-side auxiliary supply is connected to the BPP pin via a current-limiting resistor, R14.

4.1.4 Primary-Side OVP

Primary-side output overvoltage protection (OVP) is implemented by the Zener diode VR3 and series resistor R37. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding causes the Zener diode VR3 to conduct, increasing the current into the BPP pin. If this current exceeds the I_{SD} limit (7.5 mA), OVP protection is triggered, and the controller implements a latching shutdown.

4.1.5 Primary Peak Current Limit

The value of capacitor C2 is used to set the maximum primary current to either STANDARD or INCREASED level. In this case, a 470 nF capacitor sets the primary-side controller peak current limit to its STANDARD level of 1.85 A.

4.2 Secondary-Side

The secondary side of the InnoMux2-EP IC (U1) is powered from an internal regulator connected to BPS pin (U1, pin 6). At the beginning of startup, power for the BPS regulator is provided by the FORWARD pin (U1, pin 10). Capacitor C7 is a decoupling capacitor.

4.2.1 InnoMux2-EP Pin Configuration for 1CV Application

InnoMux2-EP can also be used for single output applications using the same part type used for multiple output power supplies. To do this, the pin connections shown in table 2 must be implemented.

Pin Number	Pin Name	Connection
1	FB1	Connected to FBHV
3	FB2	Floating
5	CDR1	Floating
8	FBHV	Connected to FB1
11	VCV1	Connected to VCHV
12	VCV2/AS	Floating
13	VCVHV	Connected to VCV1

Table 2 – InnoMux2-EP Pinout for 1 CV Application.

4.2.2 Primary to Secondary-Side Communication

The secondary side of the InnoMux2-EP IC (U1) sends a request to the primary-side controller to initiate a switching cycle via the internal safety-isolated FluxLink™ communication channel.

4.2.3 InnoMux2-EP Power Supply

During startup, the InnoMux2-EP secondary-side controller is also powered from VCV1 output via resistor R48. A local decoupling capacitor, C30, is connected close to the VCVHV/VCV1 pin of U1. An internal regulator lowers the VCV1 voltage to 5 V and supplies it to the BPS rail. Resistor R48 and capacitor C30 provide local decoupling and ESD protection.

4.2.4 Synchronous Rectifier (SR) MOSFET Drive

The SR pin drives the synchronous rectifier (SR) MOSFET (Q1) when the transformer is delivering energy to the secondary circuit. Before the end of secondary discharge, the gate voltage of the SR MOSFET is reduced to maintain a fixed source-to-drain voltage across the SR MOSFET. This functionality prevents the premature turn-off of the SR MOSFET.

In DCM operation, the SR MOSFET (Q1) is turned on for a short period just before the primary switch turns on. This action generates a reverse current in the CV1 secondary winding, which then commutates to cause a reverse current flow in the transformer on the primary. This reverse current discharges the voltage across the primary switch, allowing it to turn on at zero (or near zero) voltage. This mechanism, termed SR-ZVS, substantially minimizes switching loss, significantly reducing the turn-on loss for the primary switch, especially with high input voltage. The timing and duration of the ZVS conduction pulse applied to via the secondary side SR FET is automatically adjusted by the secondary controller on the InnoMux-2 IC.

Capacitor C74 and diode D16 clamp the negative transient gate-to-source voltage and protect the SR MOSFET driver pin.

4.2.5 Output Control

Output rectification for the CV1 output is provided by the SR MOSFET (Q1). To ensure low output ripple voltage, a Π filter consisting of capacitors C10, C26 and inductor L2 is employed. A low ESR capacitor, C10, is used in the first stage to attenuate ripple current, while capacitor C26, an aluminum polymer type, minimizes switching noise. Additionally, a multilayer ceramic capacitor (MLCC), C28, is connected across the CV1 output terminals to provide a low-impedance bypass for any high-frequency noise.

The RC snubber network consisting of R6, R75 and C19 serves to dampen high-frequency ringing across the SR MOSFET (Q1). This ringing results from the oscillation of transformer leakage inductance and secondary trace inductance with the MOSFET body capacitance.

The output voltage on CV1 is controlled by R35, R54, R10 and C51, which provide an analog current signal to FB1/FB2 (U1, pin 1 and pin 8). Loop compensation is necessary due to the use of L2 and is provided by R9 and C27.

5 PCB Layout

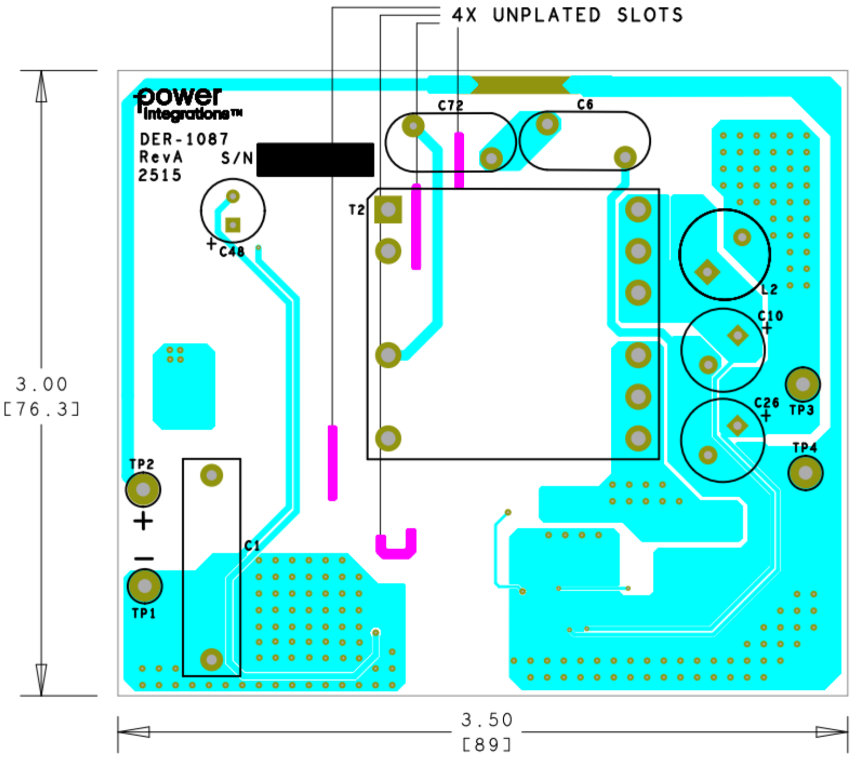


Figure 4 – Printed Circuit Board Layout, Top.

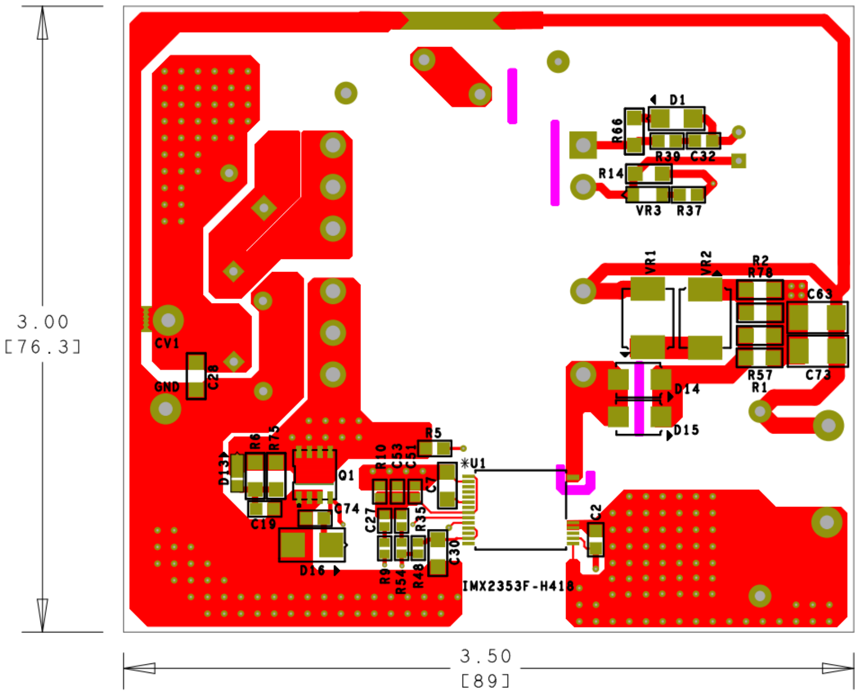


Figure 5 – Printed Circuit Board Layout, Bottom.

6 Bill of Materials

6.1 Bill of Materials: Electrical Components

Item	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	C1	0.047 μF, ±5%, Film Capacitor, Automotive, AEC-Q200, 650 VAC, 1600 VDC (1.6k VDC), Polypropylene (PP), Metallized Radial	R76TN24704040J	KEMET
2	C2	470 nF, ±10%, 50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung Electro-Mechanics
3	C6	4.7 nF, Ceramic, Y1	440LD47-R	Vishay
4	C7	4.7 μF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
5	C10	470 μF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
6	C19	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX Corp
7	C26	470 μF, 35 V, Electrolytic, Low ESR, 23 mOhm, (10 x 20)	UHD35470MPD	Nichicon
8	C27	0.1 μF (100 nF) ±10% 50 V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
9	C28	4.7 μF, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
10	C30	100 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB104	Yageo
11	C32	100 pF, 500 V, Ceramic, NP0, 0805	501R15N101KV4T	Johanson Dielectrics Inc.
12	C48	27 μF, ±20%, 100 V, Al Electrolytic, Gen. Purpose, Can, (8mm x 13mm)	EEU-FS2A270B	Panasonic Electronic Components
13	C51	220 pF, 250 V, Ceramic, COG, 0603	C1608C0G2E221J	TDK Corp
14	C53	220 pF, 250 V, Ceramic, COG, 0603	C1608C0G2E221J	TDK Corp
15	C63	1 nF, 1500 V, Ceramic, X7R, 1808	1808SC102KAT1A	AVX
16	C72	4.7 nF, Ceramic, Y1	440LD47-R	Vishay
17	C73	1 nF, 1500 V, Ceramic, X7R, 1808	1808SC102KAT1A	AVX
18	C74	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX Corp
19	D1	DIODE ULTRA FAST, GPP, 400 V, 1 A SMA	US1G-13-F	Diodes, Inc
20	D13	Diode, Schottky, 200 V, 1 A, Surface Mount SOD-123HE	SS10200HE_R1_00001	Panjit International Inc.
21	D14	Diode, 2000 V, 2 A, Surface Mount DO-214AA (SMB)	S2Y	Diotec Semiconductor
22	D15	Diode, 2000 V, 2 A, Surface Mount DO-214AA (SMB)	S2Y	Diotec Semiconductor
23	D16	30 V, 2 A, Schottky, SMD, DO-214AA Low Drop	SL23-E3/52T	Vishay
24	L2	Fixed Inductor, 12 μH, ±10%, 5.1 A, 0.035 ohm, TH	RFB1010-120L	Coilcraft
25	Q1	N-Channel 150 V 17 A (Ta), 100 A (Tc) 6.2 W (Ta), 215 W (Tc) Surface Mount 8-DFN (5 x 6)	AONS66520	Alpha & Omega Semiconductor
26	R1	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
27	R2	RES, 100 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
28	R5	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
29	R6	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
30	R9	RES, 22.1 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2212V	Panasonic
31	R10	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3321V	Panasonic
32	R14	RES, 10 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J103V	Panasonic
33	R35	RES, 61.9 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF6192V	Panasonic
34	R37	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
35	R39	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
36	R48	RES, 10 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
37	R54	RES, 470 R, 1%, 1/10 W, Thick Film, 0603 (1608 Metric)	ERJ-3EKF4700V	Panasonic
38	R57	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
39	R66	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
40	R75	RES, 5.6 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J5R6V	Panasonic
41	R78	RES, 100 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1003V	Panasonic
42	T2	Bobbin, PQ32/30, Vertical, 12 pins	BQ32/30-1112CPFR	TDK
43	U1	InnoMux2-EP WG, InSOP-T28G	10-01592-00	Power Integrations
44	VR1	TVS, 207 V Clamp, 7.3 A Ipp, Unidirectional, SMC, DO-214AB	TPSMC150A	Littelfuse Inc
45	VR2	TVS, 207 V Clamp, 7.3 A Ipp, Unidirectional, SMC, DO-214AB	TPSMC150A	Littelfuse Inc
46	VR3	DIODE ZENER 47 V 500 MW SOD123	MMSZ5261BT1G	ON Semi

Table 3 – Electrical Bill of Materials.

6.2 Bill of Materials: Mechanical Components

Item	Ref Des.	Description	Mfr. Part Number	Manufacturer
1	TP1	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
2	TP2	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
3	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
4	TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

Table 4 – Mechanical Bill of Materials.

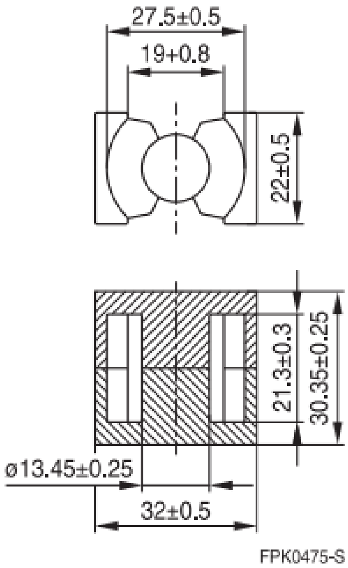
7 Transformer (T1) Specification

7.1 Core Information

PQ 32/30

Core **B65879B**

- To IEC 63093-13
- Delivery mode: sets



Magnetic characteristics (per set)

$\Sigma l/A$ = 0.441 mm^{-1}
l_e = 67.80 mm
A_e = 153.8 mm^2
A_{min} = 127.5 mm^2
V_e = 10440 mm^3

Approx. weight 57.4 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
N49	3450 +30/–20%	1210	< 3.65 (50 mT, 500 kHz, 100 °C)	B65879B0000R049
N87	4800 +30/–20%	1700	< 7.00 (200 mT, 100 kHz, 100 °C)	B65879B0000R087
N97	5000 +30/–20%	1760	< 5.80 (200 mT, 100 kHz, 100 °C)	B65879B0000R097
N95	6100 +30/–20%	2140	< 6.30 (200 mT, 100 kHz, 25 °C – 100 °C) < 7.56 (200 mT, 100 kHz, 120 °C)	B65879B0000R095

Other A_L values/air gaps and materials available on request – see Processing remarks on page 4.
Combination with I core available on request.

Figure 6 – PQ32/30 Core Information.

7.2 Bobbin Information

PQ 32/30

Accessories **B65880E**

Coil former

Material: GFR thermosetting plastic (UL 94 V-0, insulation class to IEC 60085:
F ≙ max. operating temperature 155 °C), color code black
Sumikon PM 9820® [E41429 (M)], SUMITOMO BAKELITE CO LTD

Solderability: to IEC 60068-2-20, test Ta, method 1 (aging 3): 235 °C, 2 s

Resistance to soldering heat: to IEC 60068-2-20, test Tb, method 1B: 350 °C, 3.5 s

Sections	A_N mm^2	l_N mm	A_R value µΩ	Terminals	Ordering code
1	104	62	21	12	B65880E2012D001

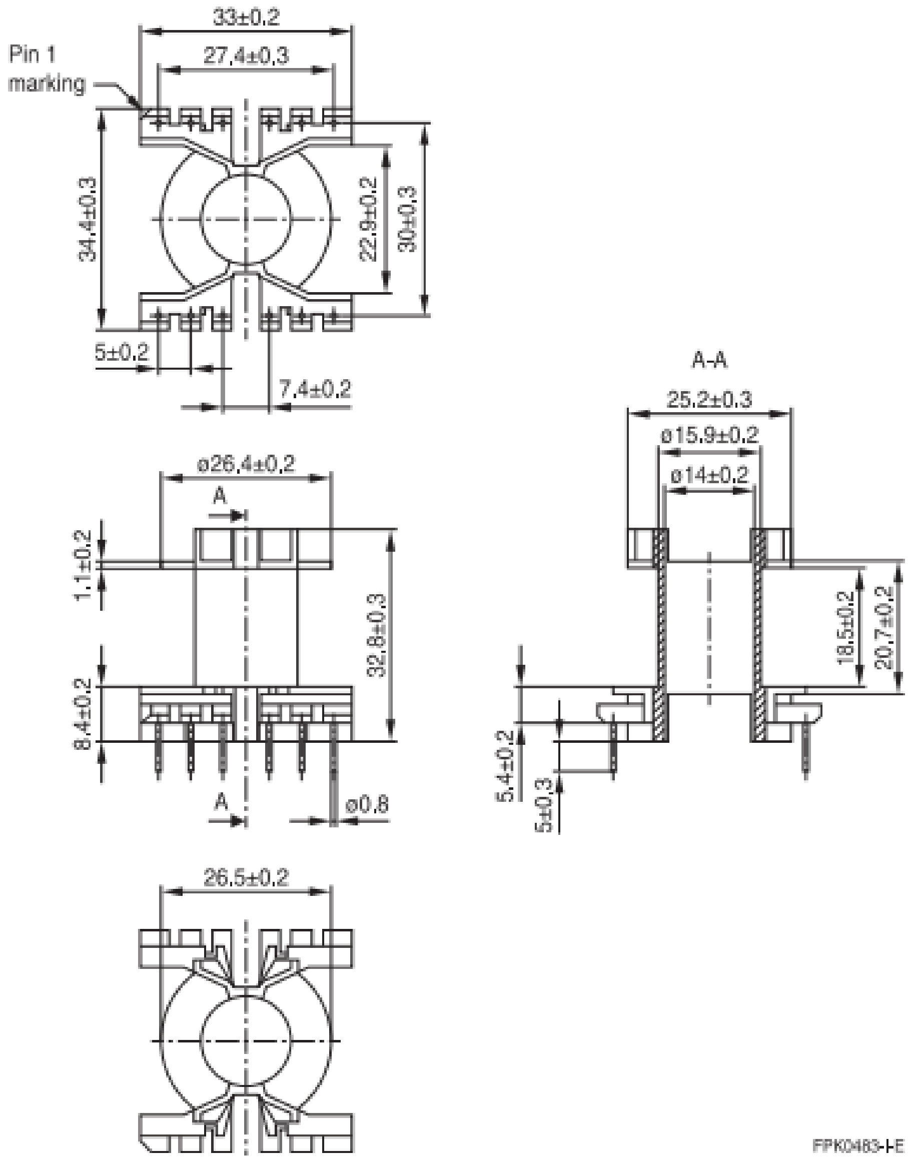


Figure 7 – PQ32/30 Bobbin Information.

7.3 Transformer Electrical Diagram

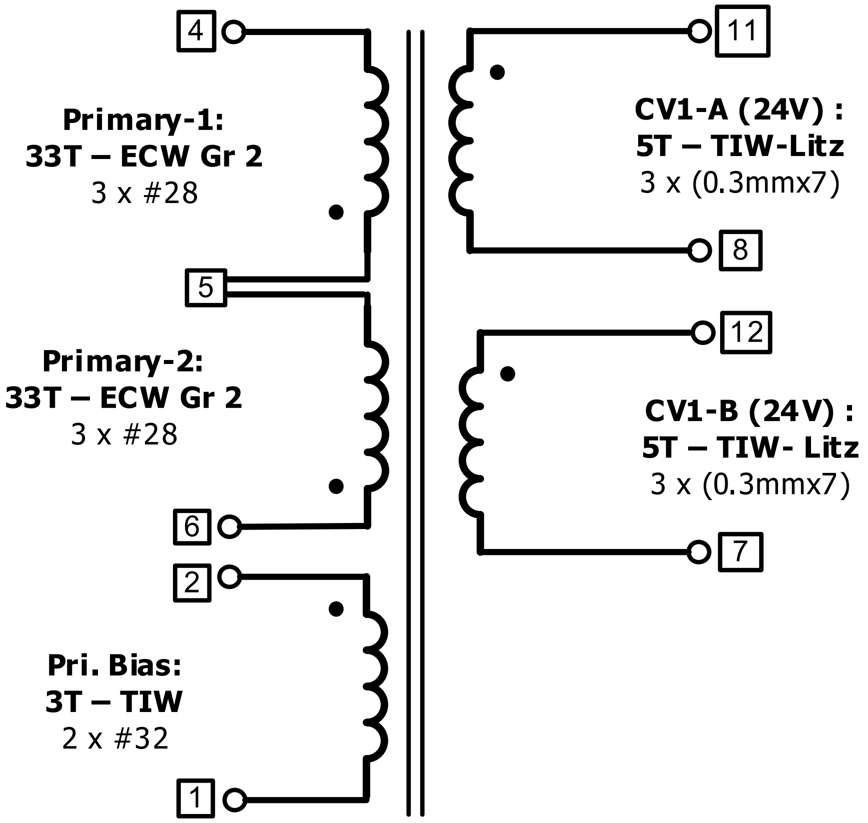


Figure 8 – Transformer Electrical Diagram.

7.4 Transformer Electrical Specification

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1, 2, 4, 5, 6 to 7, 8, 11, 12	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 6, with all other windings open.	**1100 μH ±5%**
Resonant Frequency	Between pin 4 and 6, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and 6, with all secondary windings shorted (pins 7, 8, 9, 10, 11, 12), and primary bias winding opened (pins 1, 2).	< 21 μH

Table 5 – Transformer Electrical Specifications.

7.5 Winding Stack Diagram

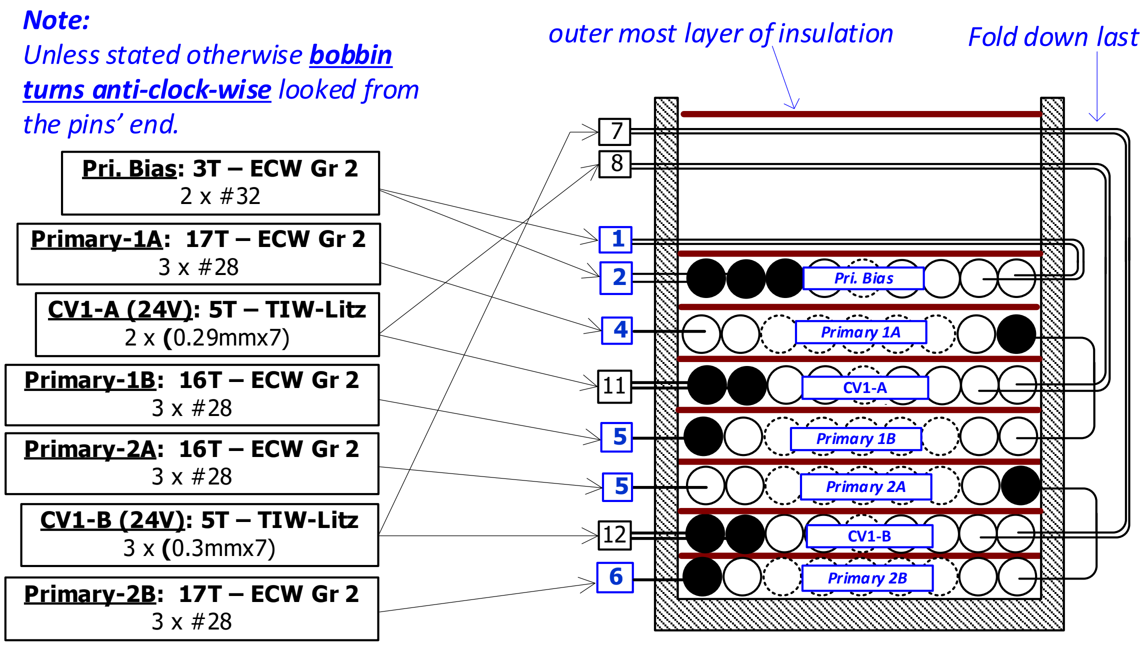


Figure 9 – Transformer Build Diagram.

7.6 List of Materials

Item	Description
[1]	Core: PQ32/30.
[2]	Bobbin: PQ32/30, 12 pins (6/6).
[3]	Magnet Wire: #28, 0.38 mm, Grade 2 ECW.
[4]	TEX: #32, 0.203 mm, Triple Insulated Wire.
[5]	TEX-ELZ Wire: 0.3 mm x 7, Triple Insulated Wire – Litz Type.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 18 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 19 mm Wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 13 mm Wide.
[9]	Varnish: Recommended, E962-A (alternative: Dolph BC-359).

Table 6 – Transformer Materials List.

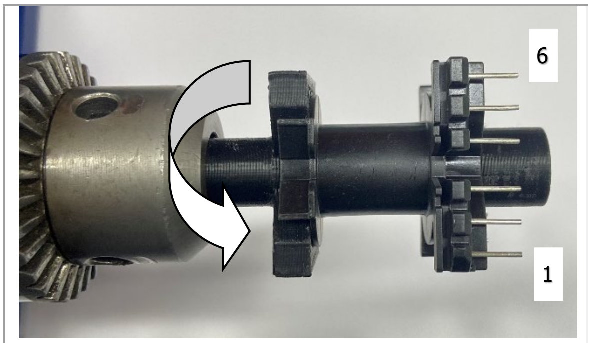
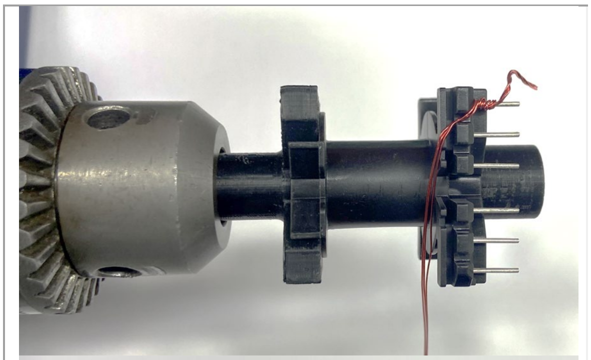
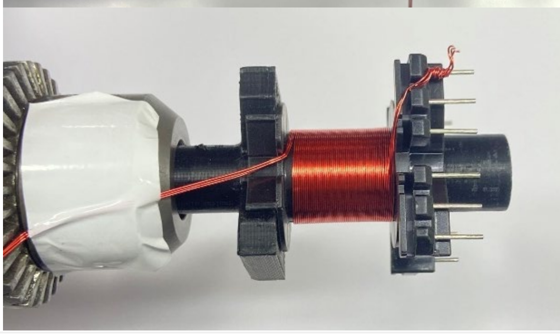
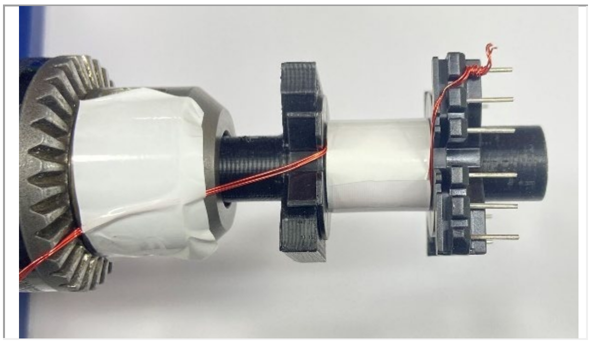
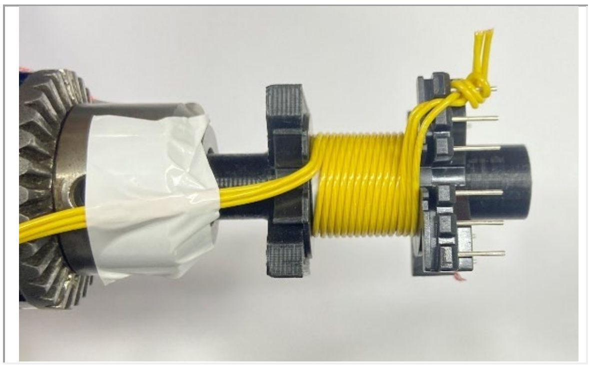
7.7 Transformer Test

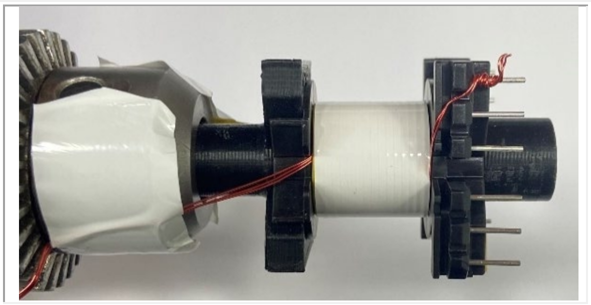
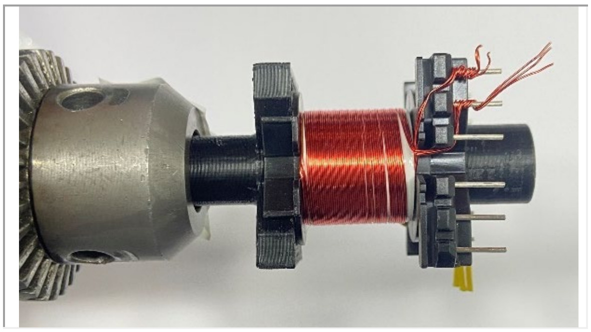
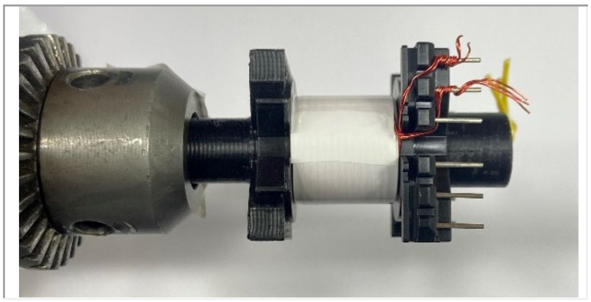
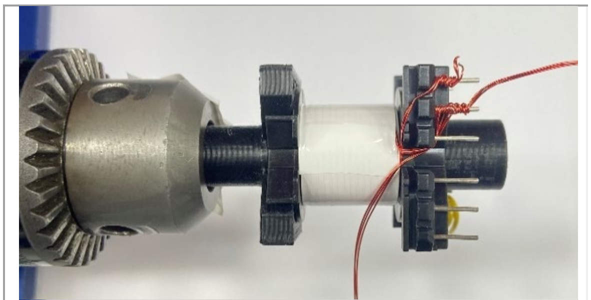
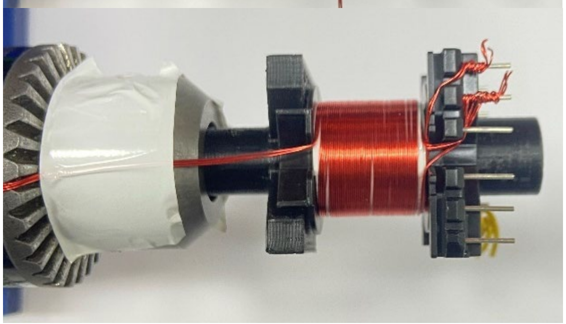
The measured inductances of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

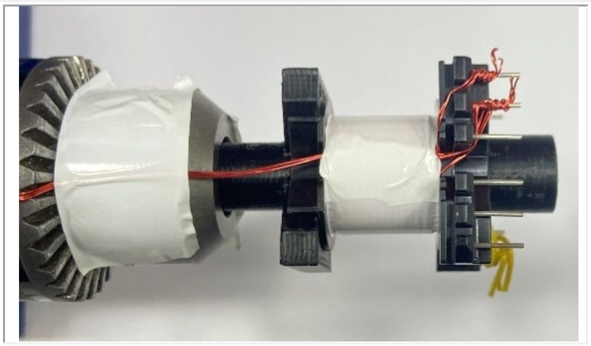
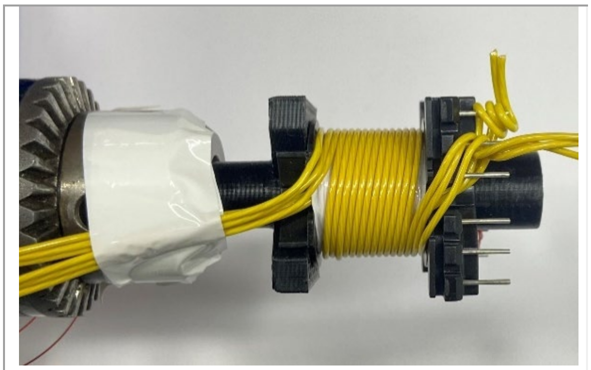
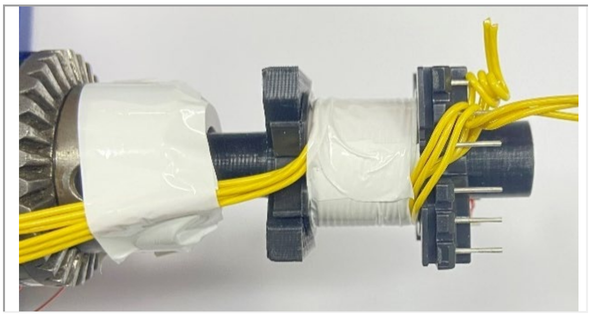
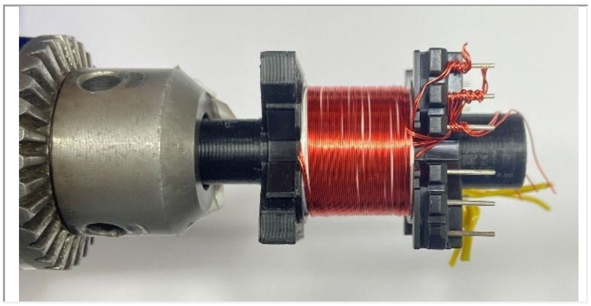
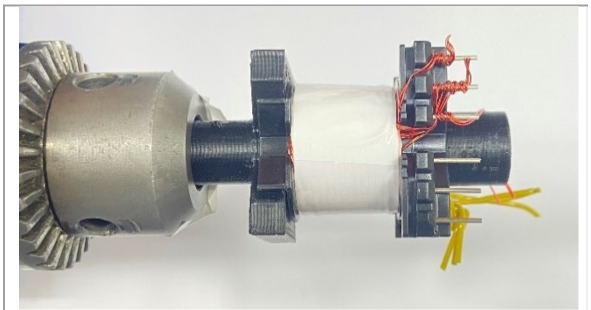
Inductance [μH]		Between Pins	Pins Shorted
L_{pri} [μH]	1102	4 - 6	
$L_{CV1\text{-}A}$ [μH]	6.91	7 - 12	
$L_{CV1\text{-}B}$ [μH]	6.62	8 - 11	
$L_{pribias}$ [μH]	2.60	1 - 2	
L_{lkgpri} [μH]	12.3	4 - 6	7, 8, 11, 12

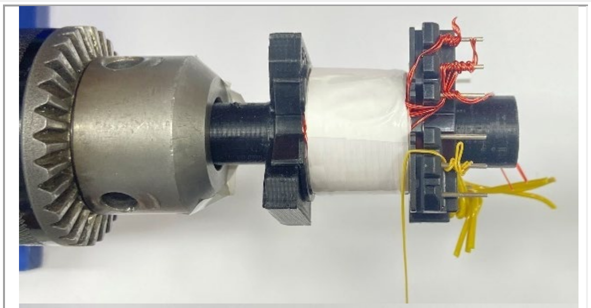
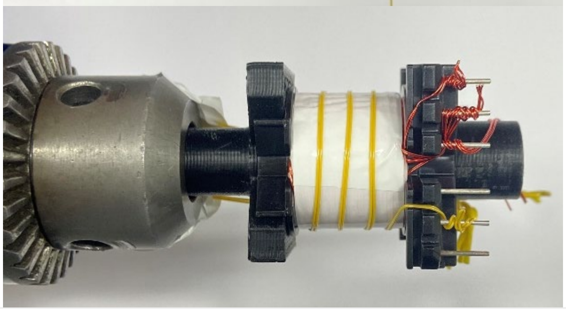
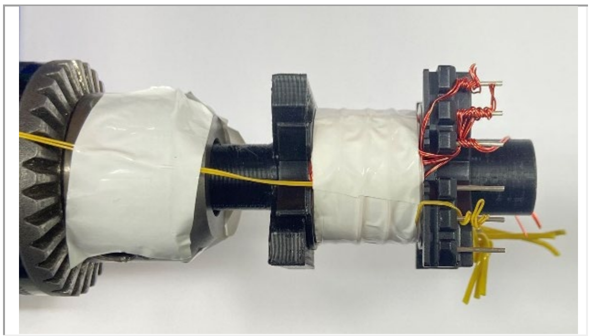
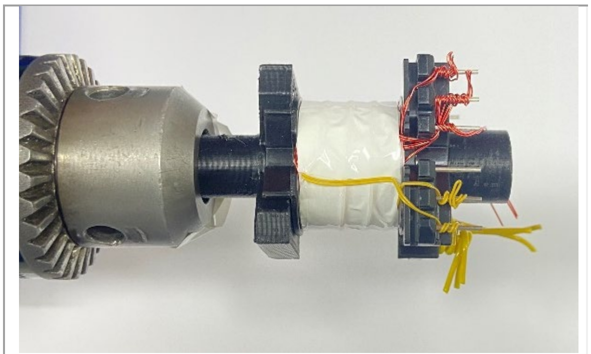
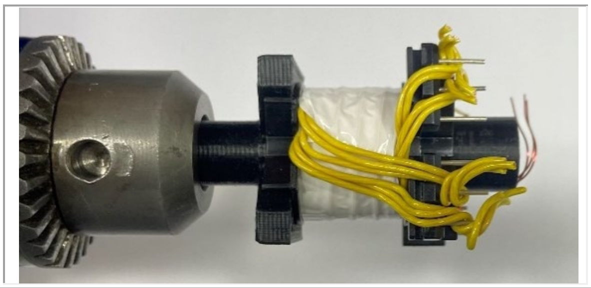
Table 7 – Winding Inductance. All measurement done in 100 kHz at 1 V_{RMS}.

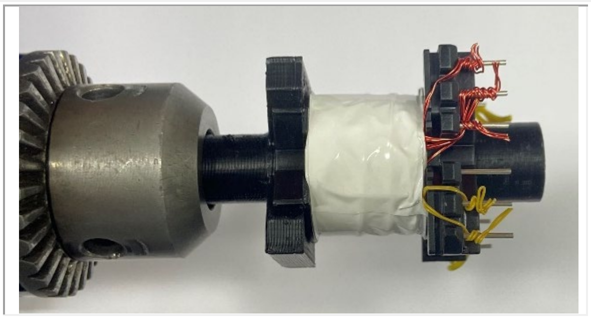
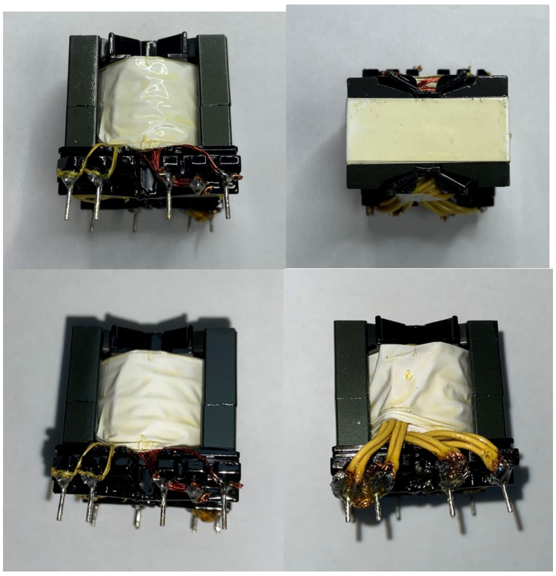
7.8 Winding Illustration

Winding Preparation		Place the bobbin on the mandrel with the pins' side facing to the right. Bobbin winding direction is anti-clockwise when looked from pins' end.
Primary-2B		Start at pin 6. Wind 3 strands and 17 turns of wire Item [3] in 1 layer, with normal tension from right to left. Terminate the winding temporarily on the mandrel using a piece of tape with an excess of around 2 meters. Do not cut off.
Insulation layer		Add 1 layer of tape Item [6].
CV1-B		Start at pin 12. Prepare 3 strands of Item [5] and wind 5 turns from right to left. Terminate the winding temporarily on the mandrel using a piece of tape with an excess of around 10 cm. Do not cut off.

Insulation layer		Add 1 layer of tape, Item [6].
Primary-2A		Remove the taped end of Primary-2B and wind 16 turns of primary-2A from left to right. Terminate at pin 5.
Insulation layer		Add 1 layer of tape, Item [6].
Primary-1B	 	Start at pin 5. Prepare 3 strands of Item [3] and wind 16 turns in 1 layer, with normal tension from right to left. Terminate the winding temporarily on the mandrel using a piece of tape with an excess of around 2 meters. Do not cut off.

Insulation Layer		Add 1 layer of tape, Item [6].
CV1-A		Start at pin 11. Prepare 3 strands of Item [5] and wind 5 turns from right to left. Terminate the winding again temporarily on the mandrel using a piece of tape with an excess of around 10 cm. Do not cut off.
Insulation Layer		Add 1 layer of tape, Item [7].
Primary-1A		Remove the taped end of Primary-1B and wind 17 turns of primary-1A from left to right. Terminate at pin 4.
Insulation Layer		Add 1 layer of tape, Item [7].

Primary Bias		Start at pin 2. Prepare 2 strands Item [4] and wind 3 turns from right to left and terminate temporarily on the mandrel using a tape.
Insulation Layer		Add 1 layer of tape, Item [7].
Primary Bias termination		Remove the taped end of the Primary Bias winding. Press down across the bobbin window before terminating at pin 1.
CV1-A and CV1-B termination		Remove the taped ends of the CV1-A and CV1-B windings. Press down across the bobbin window before terminating at pin 7 and 8.

Insulation Layer		Add 1 layer of tape, Item [7].
Finish Assembly		Gap core to achieve a nominal inductance of 474 μH across the primary winding pins, 4 and 6. Secure core halves into the bobbin using Item [9]. Then reinforce the enclosure using around 13 cm of tape, Item [8]. Vacuum impregnate varnish for 30 minutes to make sure varnish is well infiltrated. Recommended varnish, Item [9]. Dry in oven for 30 minutes at 100 °C temp. Label "DER1087 XXX.X μH" (XXX.X = measured primary inductance value in μH)

8 Performance

8.1 Full Load Efficiency vs. Line

The full load efficiency vs. line measurement is shown below. Results were obtained across line voltage (300 VDC, 500 VDC, 800 VDC, 1000 VDC) measured at full load.

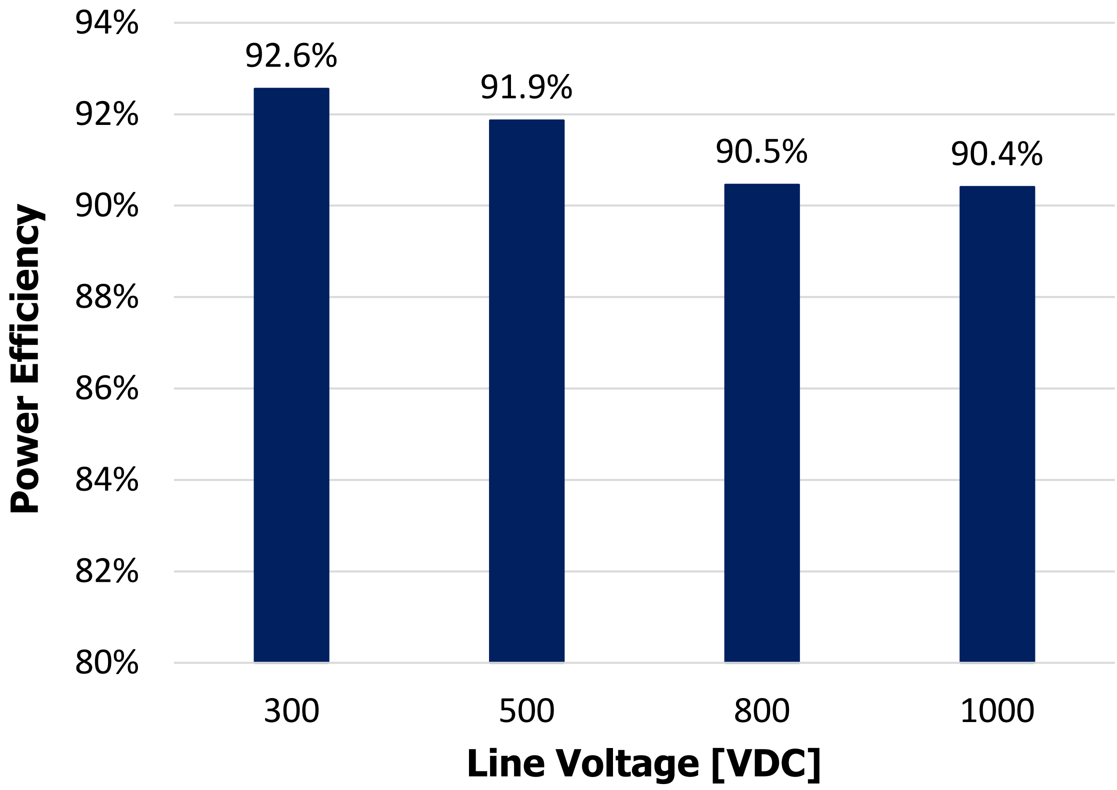


Figure 10 – Full Load Efficiency vs. Line Voltage at Room Temperature.

8.2 Efficiency vs. Load

The efficiency vs. load measurement is shown below and was obtained for combinations of:

1. Input line voltages (300 VDC, 500 VDC, 800 VDC, 1000 VDC)
2. CV1 = 24 V @ 4.2 A (5% to 100% with 5% load increments)

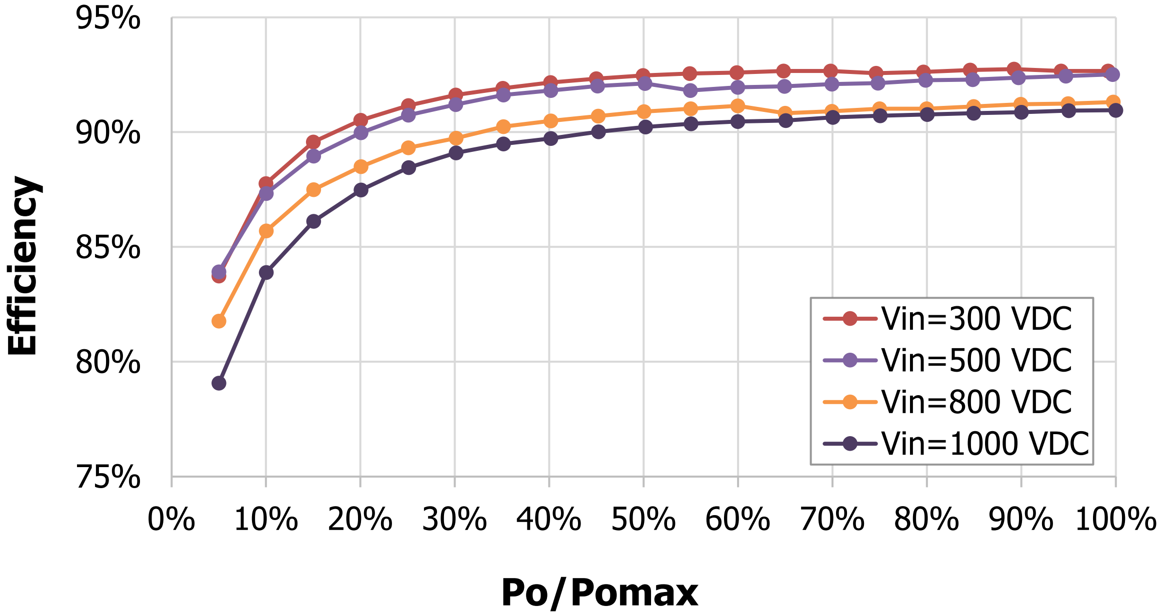


Figure 11 – Efficiency vs. Load Across Line, Room Temperature.

8.3 Output Load Regulation

The output voltage regulation error vs. load measurement is shown below. Results were obtained for all combinations of:

1. Input line voltages = 300 VDC, 500 VDC, 800 VDC, 1000 VDC
2. CV1 = 24 V @ 4.2 A (0% to 100% with 5% load increments)

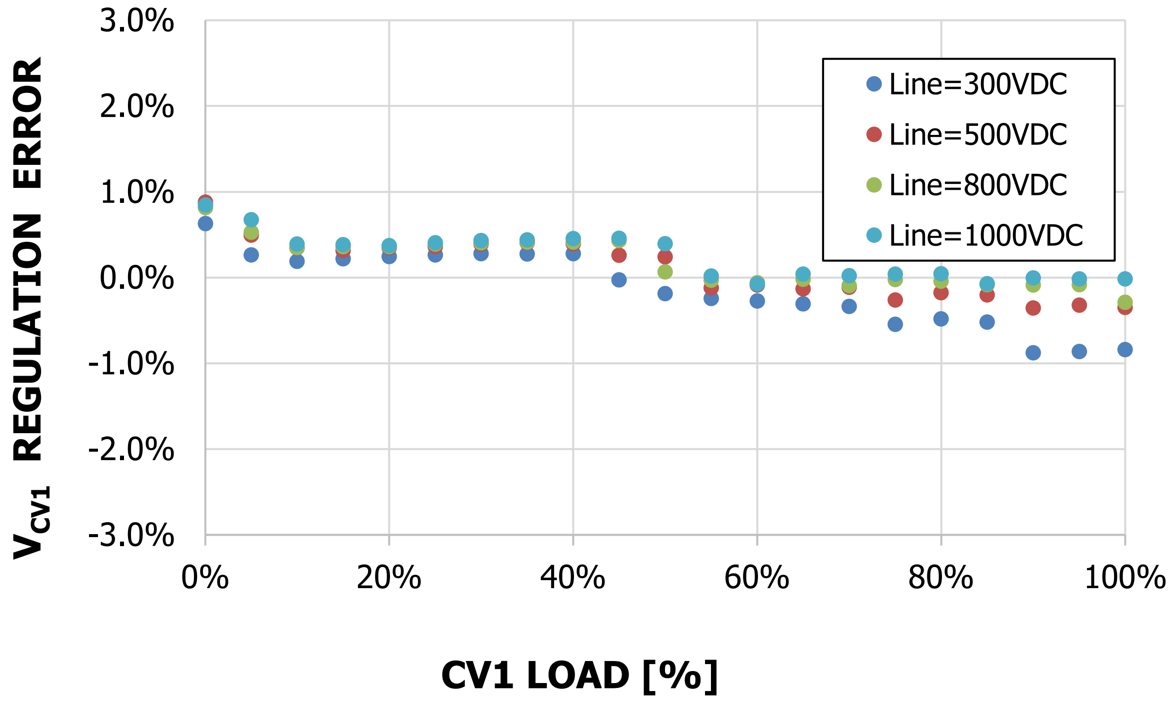


Figure 12 – CV1 Output Voltage Error vs. Output Load, Room Temperature.

8.4 Full Load Line Regulation

The output voltage regulation error vs. input voltage measurement is shown below. Results were obtained for all combinations of:

1. Input line voltages = 300 to 1000 VDC with 30 V increment
2. CV1 = 24 V @ 4.2 A

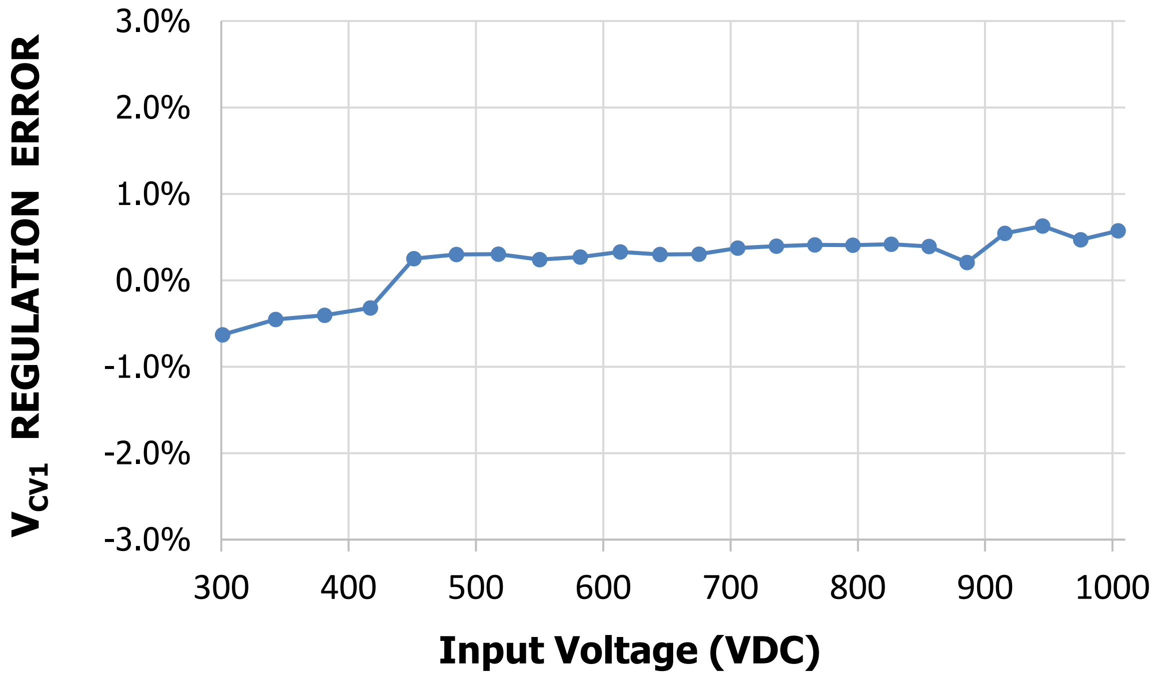


Figure 13 – CV1 Output Voltage Error vs. Line, Room Temperature.

8.5 No-Load and Standby Input Power

Output power vs. input power in standby are shown below. Results were obtained under the following test conditions:

1. Input line voltages = 300 VDC, 500 VDC, 800 VDC, 1000 VDC
2. CV1 output = 0 mW to 250 mW; 0 mW to 1000 mW

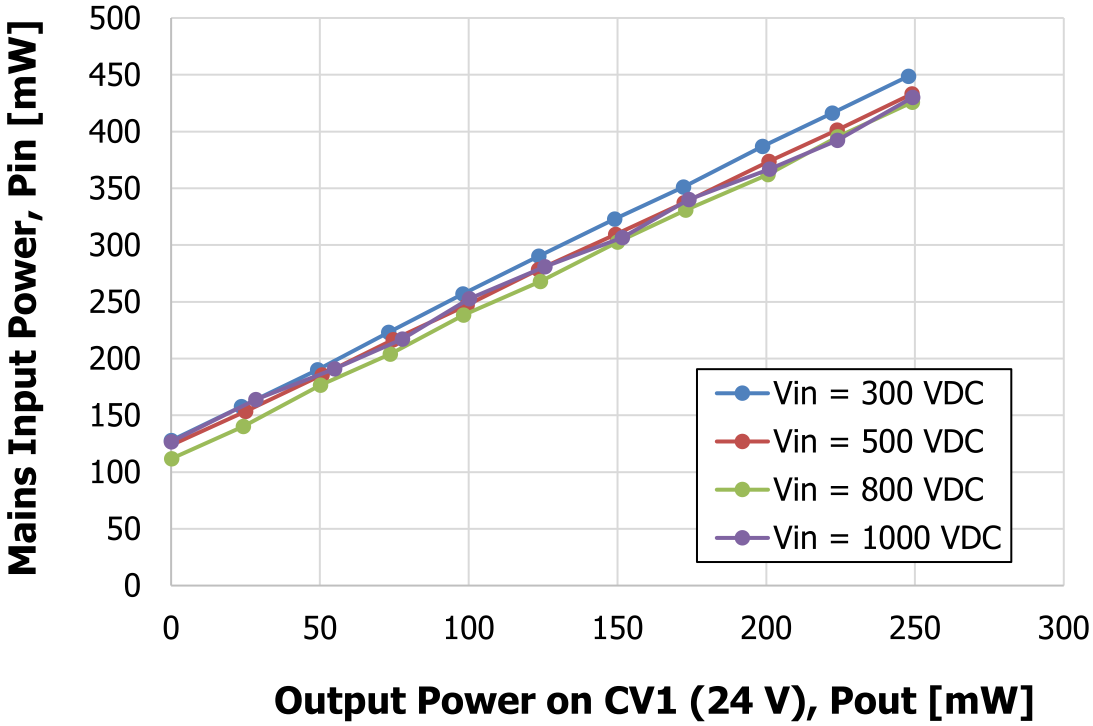


Figure 14 – Available Standby Power Measured against Input Power (0 – 450 mW). Across Input Voltage. Test Performed at Room Temperature.

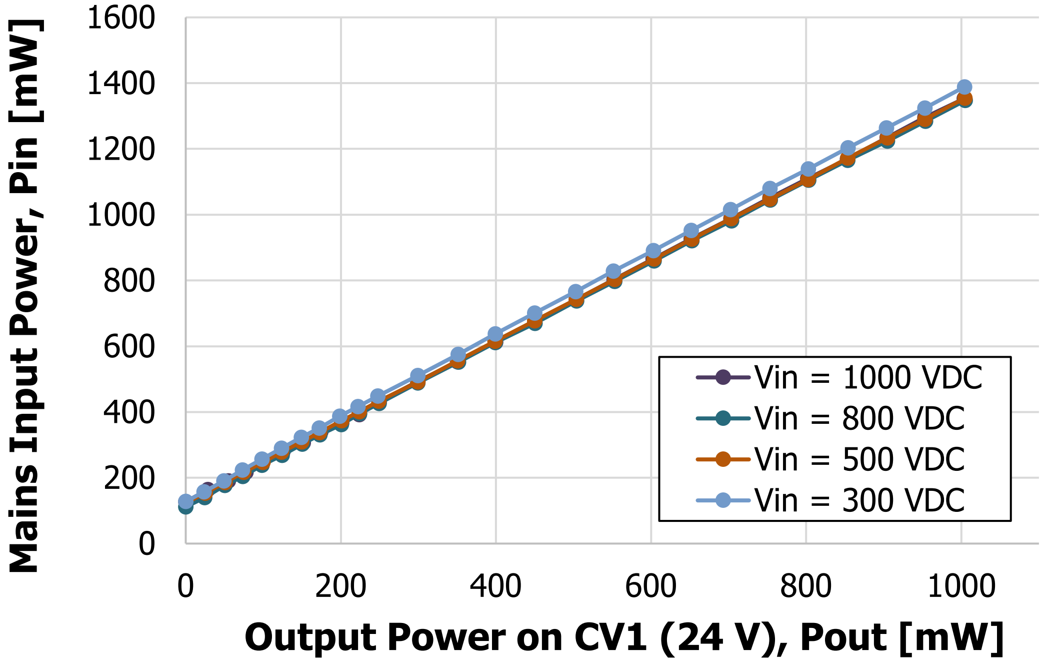


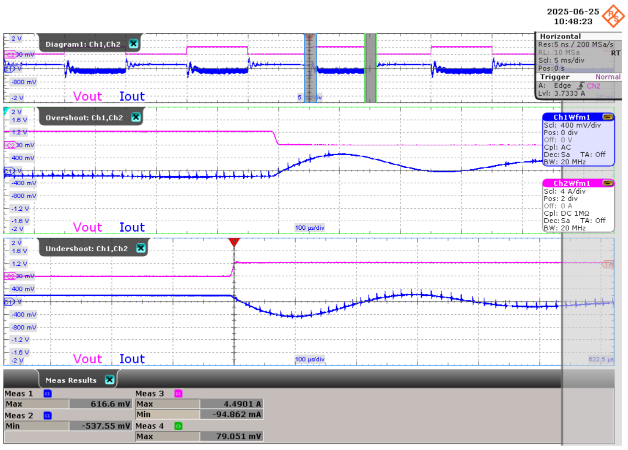
Figure 15 – Available Standby Power Measured against Input Power (0 – 1400 mW input). Across Input Voltage. Test Performed at Room Temperature.

8.6 Load Transient Response

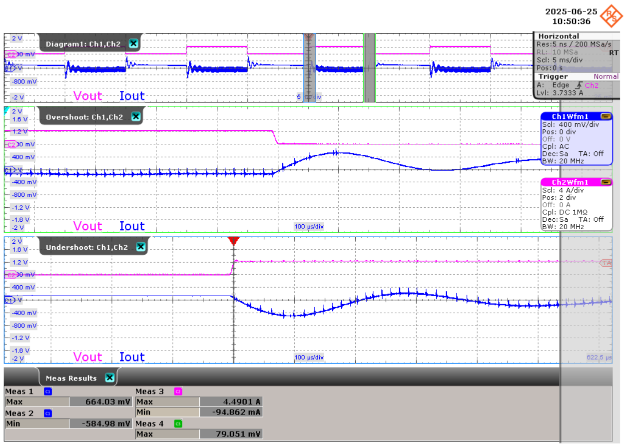
8.6.1 CV1 Step Load Transient Response

The load transient test was performed under the following test conditions:

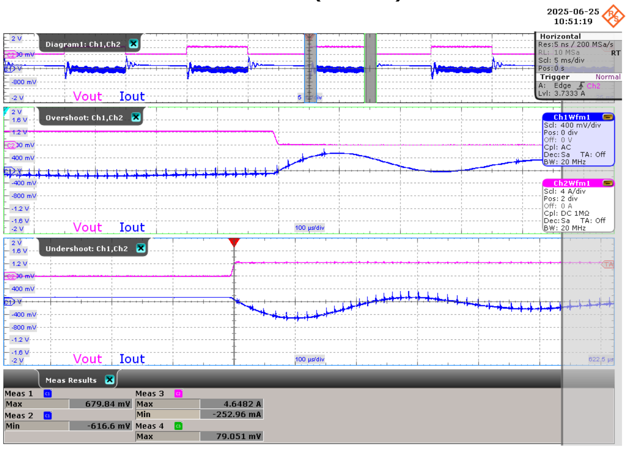
- Input line voltage = 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- CV1 load step between 0 A and 4.2 A (0% and 100% load) and back to 0 A
- CV1 is at 0% load for 5 ms and at 100% load for 5 ms
- Slew rate: 800 mA/µs



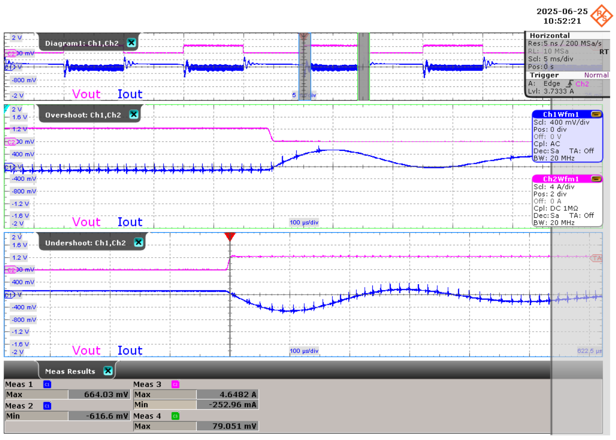
(a) 300 VDC, ICV1 = 0 A → 4.2 A (100%) → 0 A.
Overshoot: 0.617 V (2.5%).
Undershoot: -0.538 V (-2.2%).



(b) 500 VDC, ICV1 = 0 A → 4.2 A (100%) → 0 A.
Overshoot: 0.664 V (2.8%).
Undershoot: -0.585 V (-2.4%).



(c) 800 VDC, ICV1 = 0 A → 4.2 A (100%) → 0 A.
Overshoot: 0.680 V (2.8%).
Undershoot: -0.617 V (-2.5%).



(d) 1000 VDC, ICV1 = 0 A → 4.2 A (100%) → 0 A.
Overshoot: 0.664 V (2.7%).
Undershoot: -0.617 V (-2.5%).

Figure 16 – CV (24 V) Output - Load Transient at Full Load.

8.7 Switching Waveforms

8.7.1 Primary Switch Maximum Voltage

The primary switch (U1) maximum voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Load transient with full load on the output:
    - CV1 = 24 V @ 4.2 A
- 200 MHz bandwidth selected on the oscilloscope

Figure 17 – Primary Switch Worst Case Peak Voltage, V_{PRI_PK} = 1.45 kV.

8.7.2 SR FET Voltage Waveform

The SR FET (Q1) maximum voltage test was performed under the following conditions:

- Line input voltage 1000 VDC
- Start-up with full load
- 20 MHz bandwidth selected on the oscilloscope

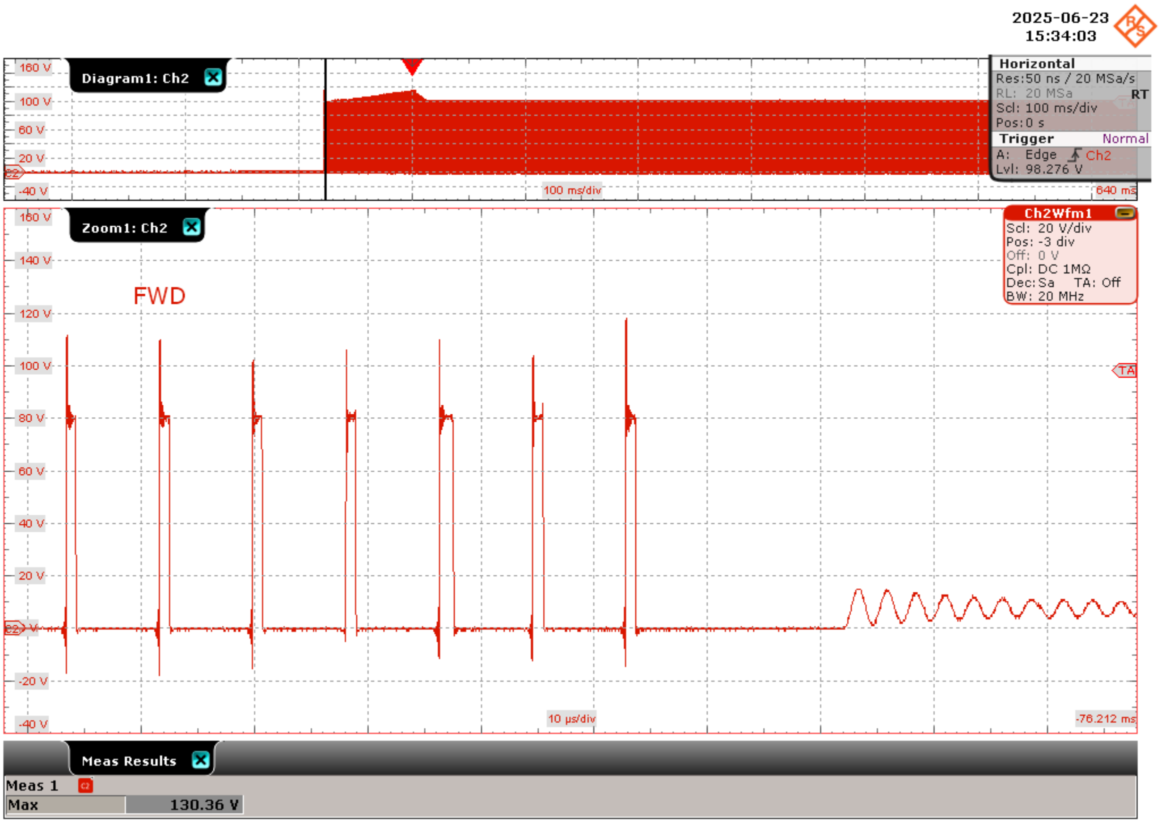


Figure 18 – SR FET Worst Case Peak Voltage, V_{SR_PK} = 130 V.

8.7.3 BPP Rectifier Diode Reverse Voltage Waveform

The BPP rectifier diode (D1) maximum reverse voltage test was performed under the following test conditions:

- Line input voltage 1000 VDC
- Start-up with full load
- 20 MHz bandwidth selected on the oscilloscope

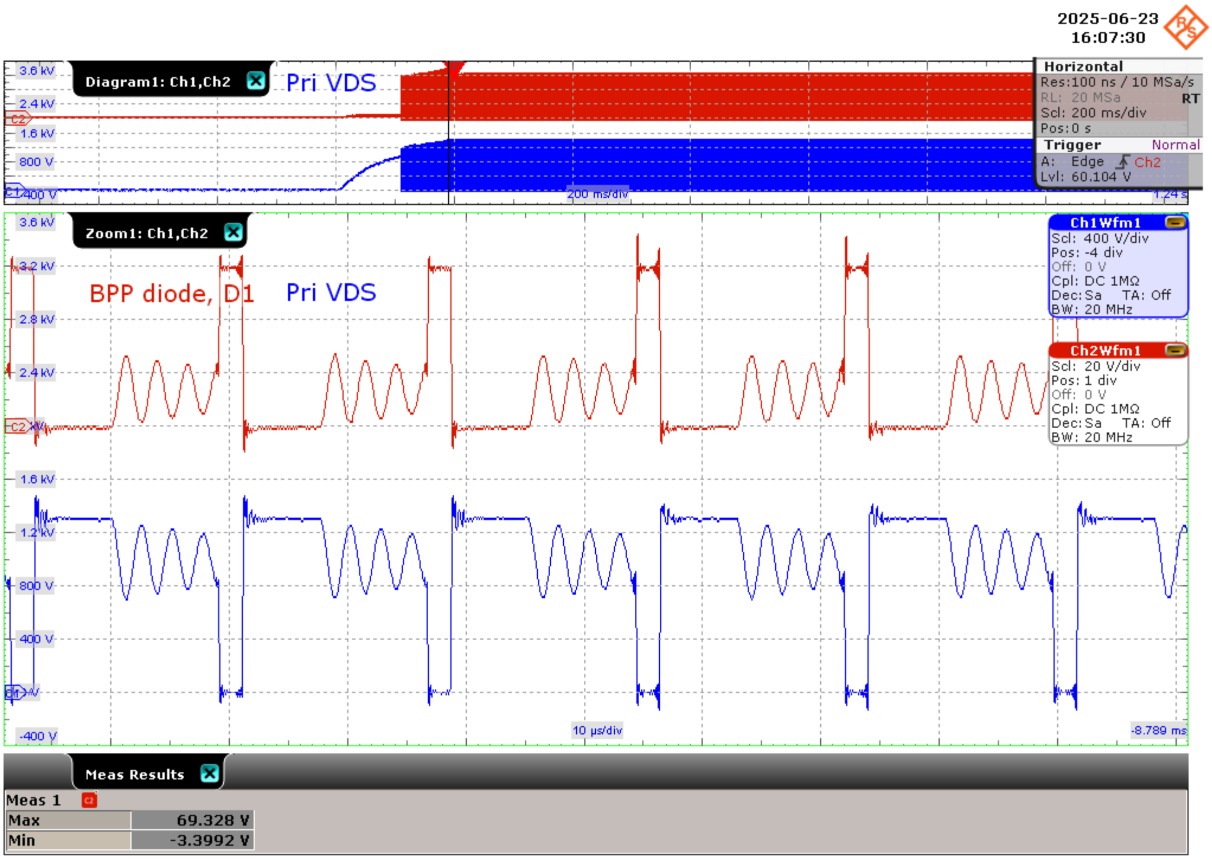


Figure 19 – BPP Rectifier Diode Worst Case Reverse Voltage, V_{D1_PK} = 69.3 V.

8.7.4 Maximum Voltage Stress

The voltage waveforms on each key component, i.e., MOSFETs & diodes, were checked to confirm that maximum voltages were below the component voltage ratings at 1000 VDC input voltage. Maximum voltage stress can occur under different combinations of input line voltages, output loads, start-up and load step. Most design specifications call for 10% ~ 20% margin between the maximum voltage stress and component rating. The table below lists the maximum voltage stress on key components:

Component	Part Number	Component Rating [V]	Voltage Stress	
			[V]	Derating [%]
InnoMux2 (U1)	IMX2353F-H418	1700	1448	**85%**
SR FET (Q1)	AONS66520	150	130	**87%**
BPP Diode (D1)	US1G	400	69.3	**17%**

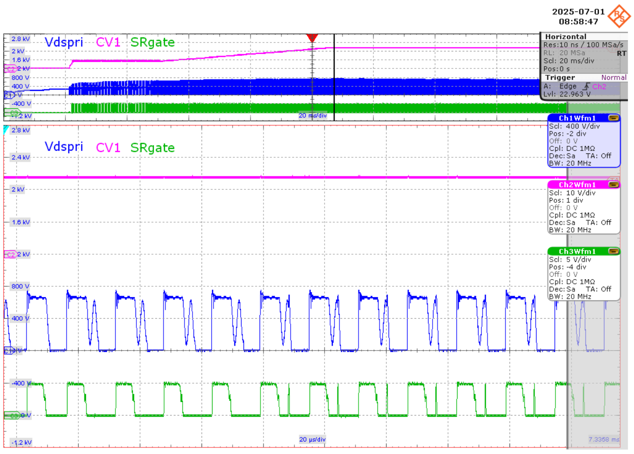
Table 8 – Maximum Voltages on key components.

8.8 Start-Up

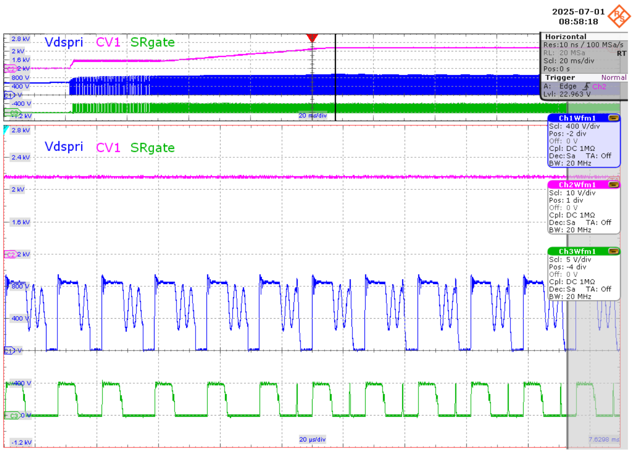
8.8.1 Start-up under Full Load

The start-up test was performed using the following test conditions:

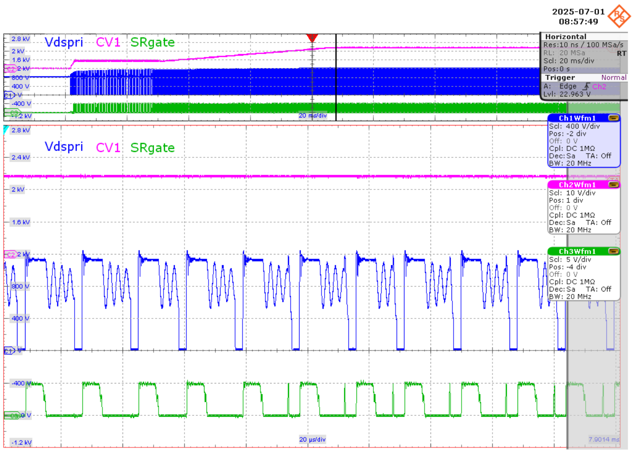
- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC
  - CV1 = 24 V @ 100 W (Full Load)



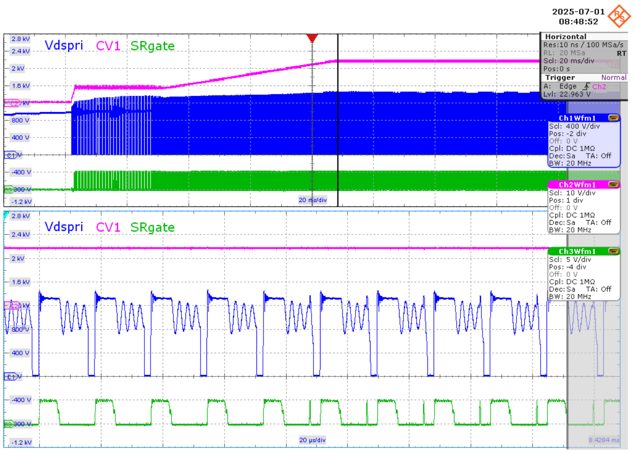
(a) 300 VDC Input Line Voltage.
CV1 = 5 V @ 4.2 A



(b) 500 VDC Input Line Voltage.
CV1 = 5 V @ 4.2 A



(c) 800 VDC Input Line Voltage.
CV1 = 5 V @ 4.2 A



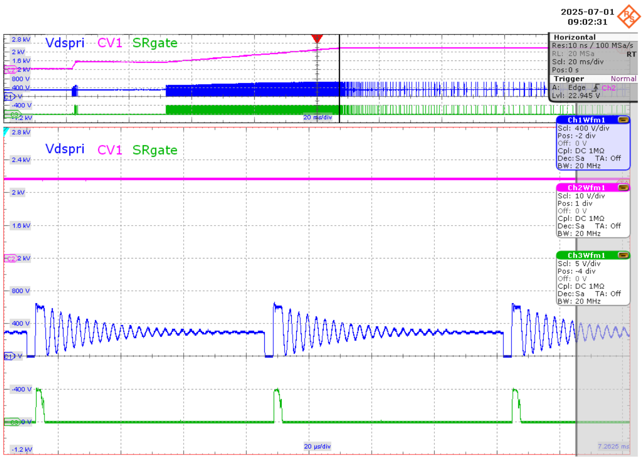
(d) 1000 VDC Input Line Voltage.
CV1 = 5 V @ 4.2 A

Figure 20 – Start-up with Output Loads.

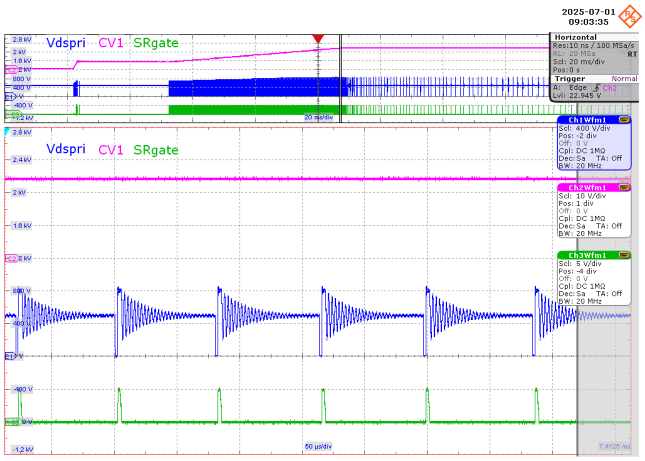
8.8.2 No-Load Start-up

The no load start-up test was performed using the following test conditions:

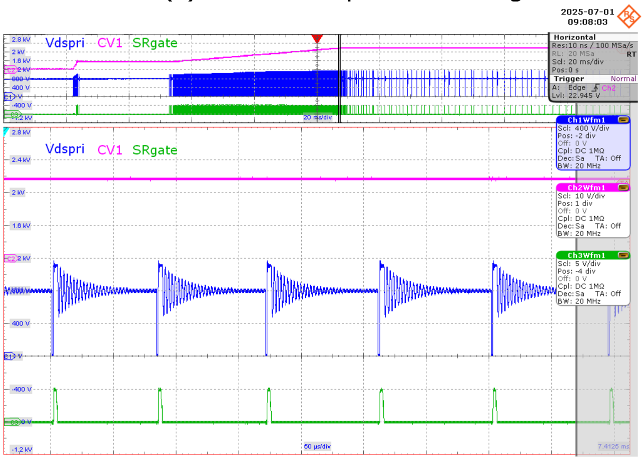
- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC



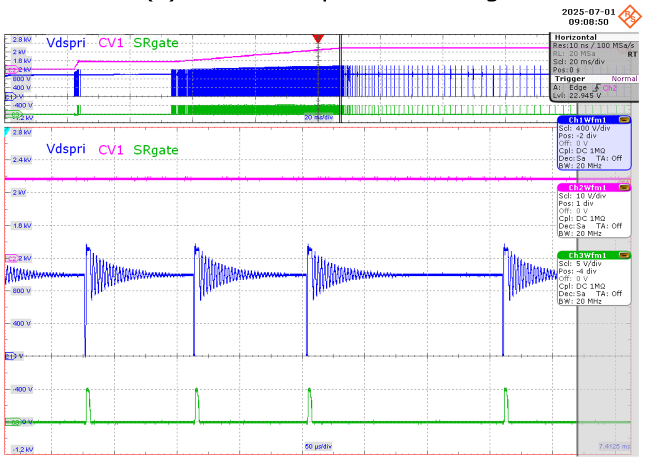
(a) 300 VDC Input Line Voltage.



(b) 500 VDC Input Line Voltage.



(c) 800 VDC Input Line Voltage.



(d) 1000 VDC Input Line Voltage.

Figure 21 – No-load Start-up.

8.9 Output Ripple Measurements

8.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was utilized to minimize noise pick-up. The probe adapter configuration is shown below. It includes a coaxial cable with two parallel capacitors connected to the measurement points. The capacitors are a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.

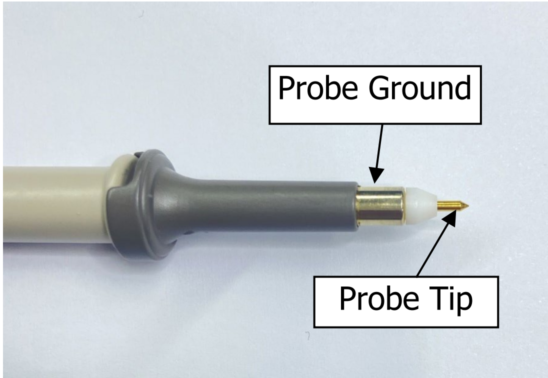
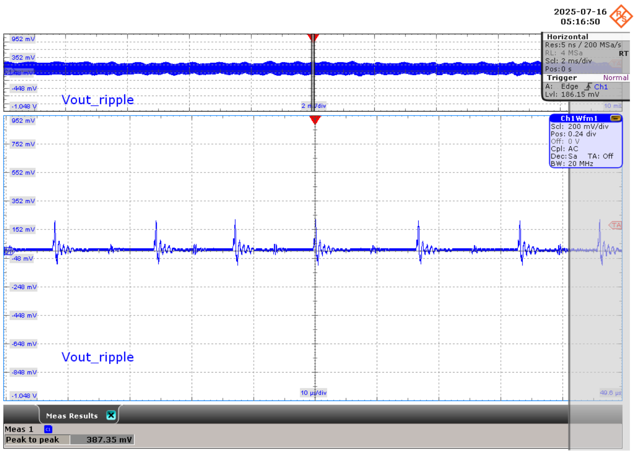
 End Cap and Ground Lead Removed.	 Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

Figure 22 – Oscilloscope Probe Prepared for Ripple Measurement.

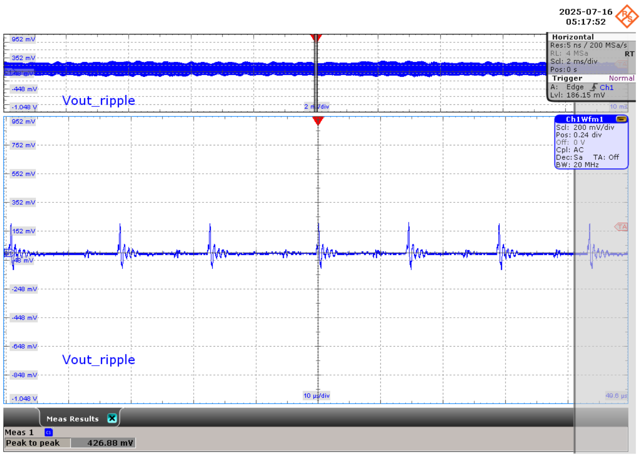
8.9.2 CV1 Output Ripple

The CV1 and CVHV output ripple were tested under the following conditions:

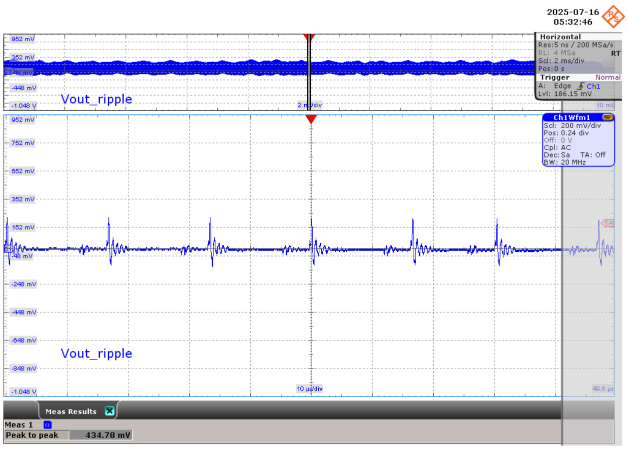
- Input line voltage 300 VDC, 500 VDC, 800 VDC, 1000 VDC
- CV1 = 24 V @ 4.2 A
- 20 MHz bandwidth selected on the oscilloscope



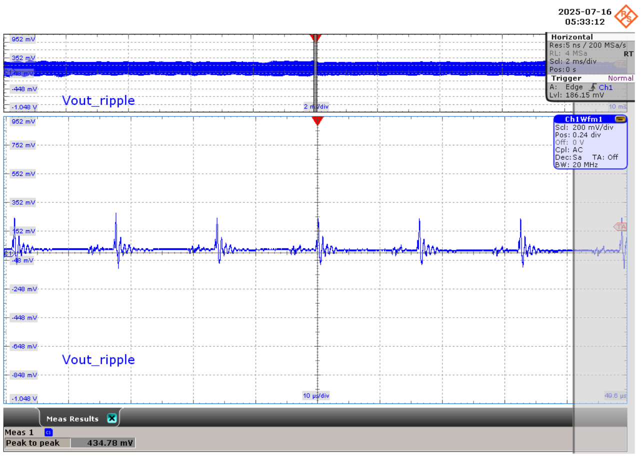
(a) 300 VDC Input Line Voltage
V_{RIPPLE_CV1} = 0.378 V



(b) 500 VDC Input Line Voltage
V_{RIPPLE_CV1} = 0.427 V



(c) 800 VDC Input Line Voltage
V_{RIPPLE_CV1} = 0.435 V

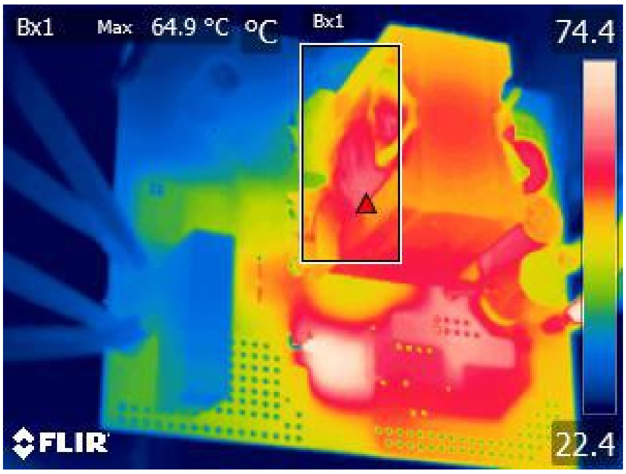


(d) 1000 VDC Input Line Voltage
V_{RIPPLE_CV1} = 0.435 V

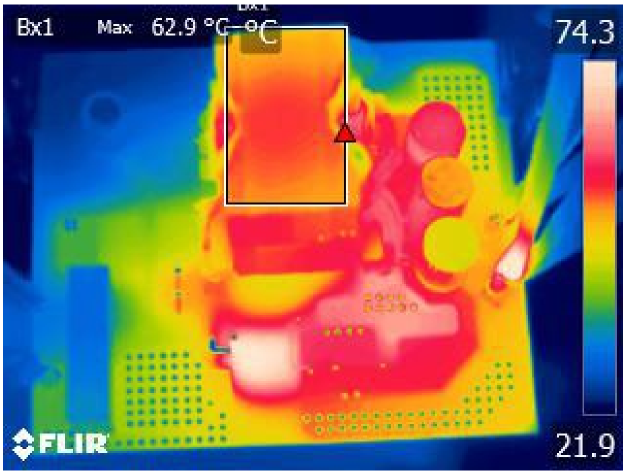
Figure 23 – VCV1 Output Ripple and Noise.

8.10 Thermal Performance

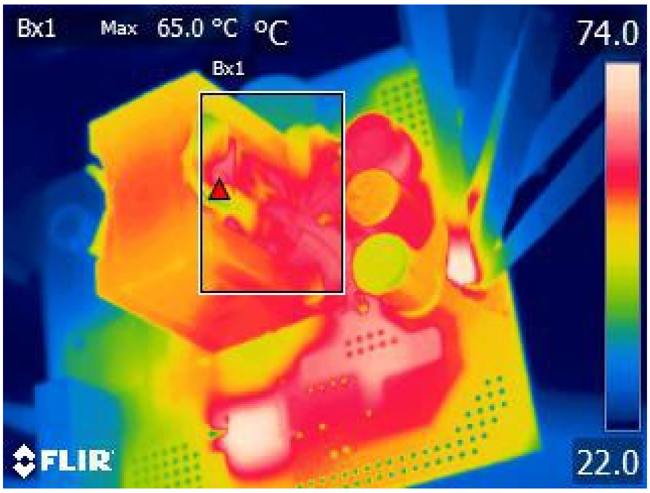
Heatsinks are not required for the design. Instead, copper pour area on the PCB was used for cooling the InnoMux2-EP IC. No forced air-cooling was required during any test. The temperatures of the hottest components in the assembly are shown below.



(a) Primary winding side



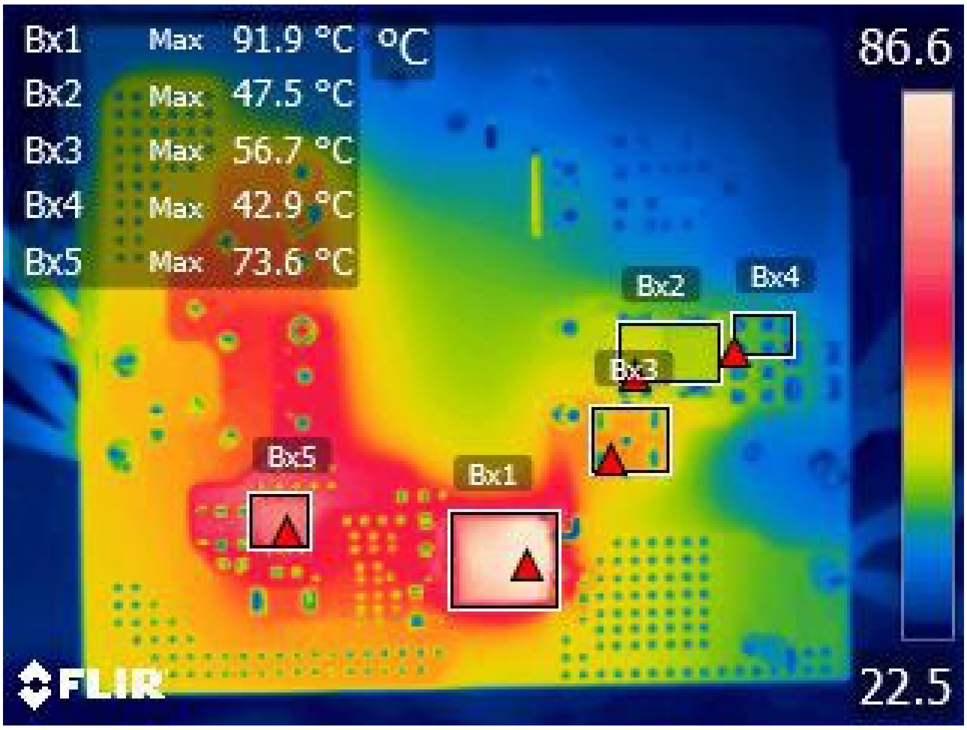
(b) Core



(c) Secondary winding side

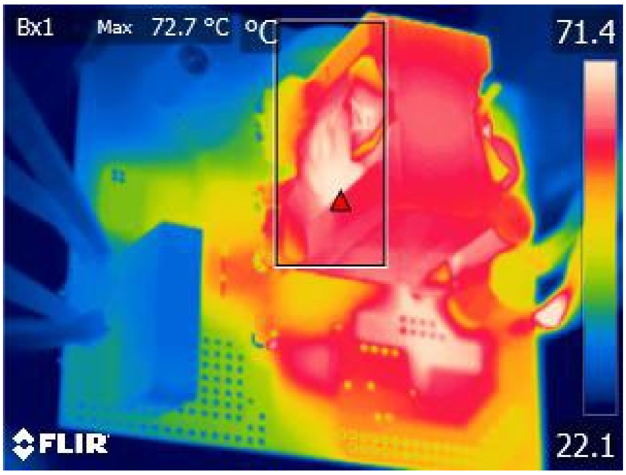
Component Ref. Des.	Component Description	Component Temperature, T [°C]
Transformer T1	Primary Winding	64.9
	Core	62.9
	Secondary Winding	65.0
	Ambient	22.0

Figure 24 – Thermal Image Top View. 300 VDC, Full Power.

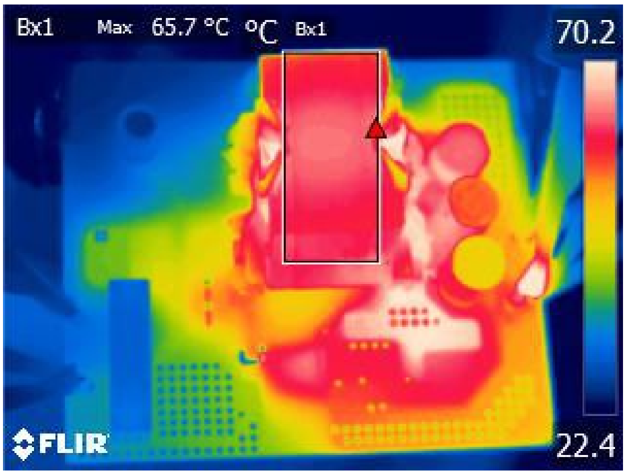


Legend	Component Ref. Des.	Component Description	Component Temperature, T [°C]
Bx1	U1	InnoMux2-EP	91.9
Bx2	VR1/VR2	Snubber Zener	47.5
Bx3	D14/D15	Snubber Diode	56.7
Bx4	R2/R78	Snubber Resistors	42.9
Bx5	Q1	SR FET	73.6
		Ambient	22.5

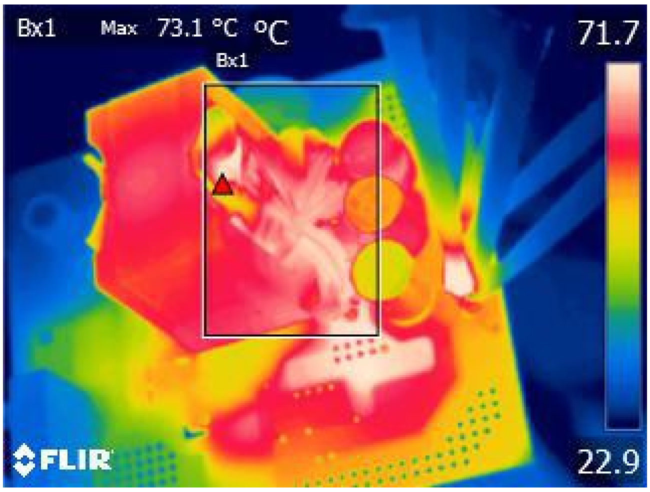
Figure 25 – Thermal Image Bottom View. 300 VDC, Full Power.



(a) Top View, Primary winding side

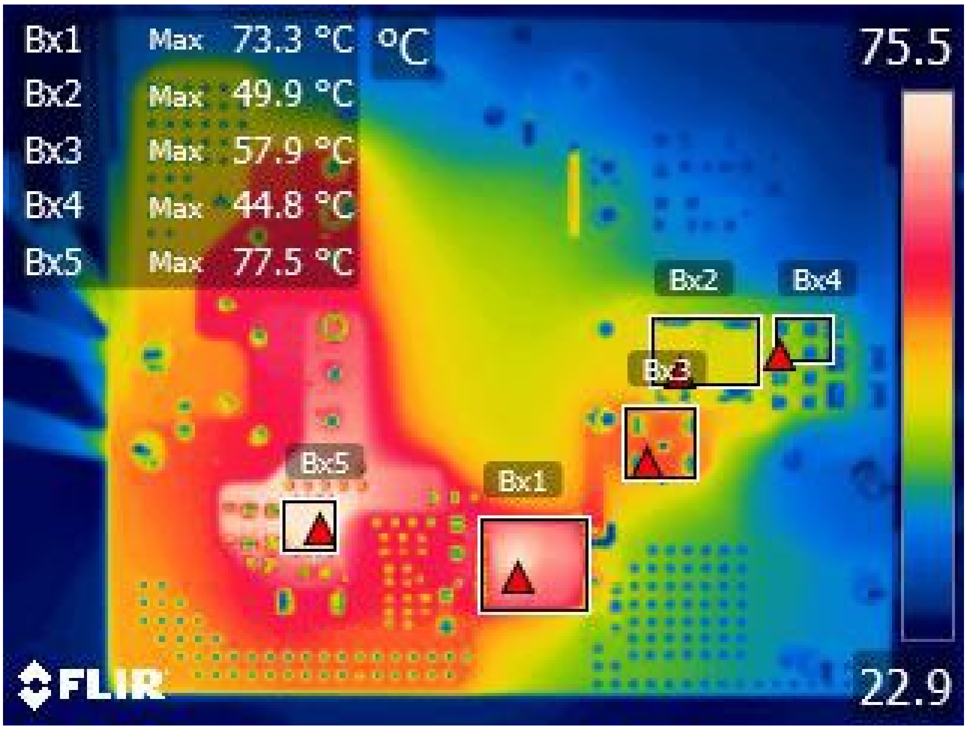


(b) Top View, Core



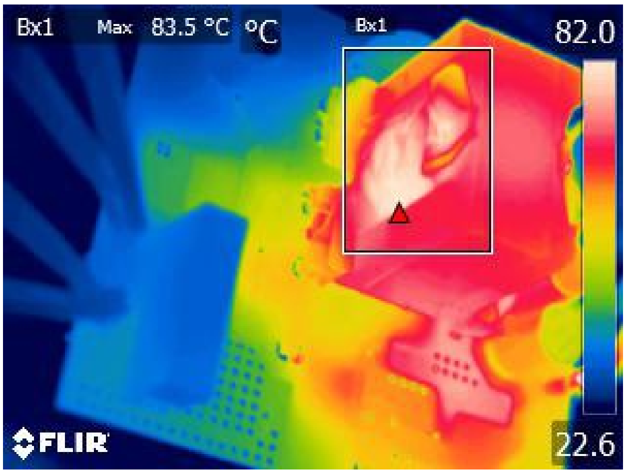
Component Ref. Des.	Component Description	Component Temperature, T [°C]
Transformer T1	Primary Winding	72.7
	Core	65.7
	Secondary Winding	73.1
	Ambient	22.1

Figure 26 – Thermal Image Top View. 500 VDC, Full Power.

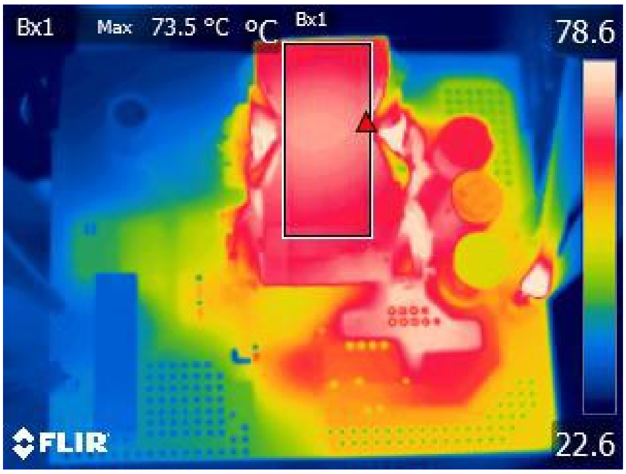


Legend	Component Ref. Des.	Component Description	Component Temperature, T [°C]
Bx1	U1	InnoMux2-EP	73.3
Bx2	VR1/VR2	Snubber Zener	49.9
Bx3	D14/D15	Snubber Diode	57.9
Bx4	R2/R78	Snubber Resistors	44.8
Bx5	Q1	SR FET	77.5
		Ambient	22.9

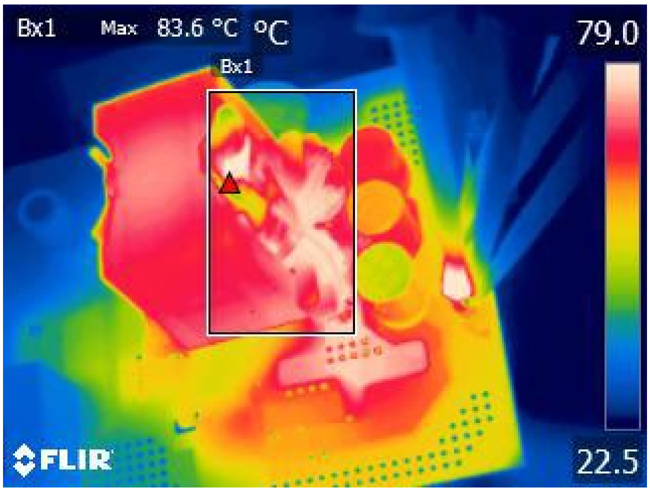
Figure 27 – Thermal Image Bottom View. 500 VDC, Full Power.



(a) Primary winding side



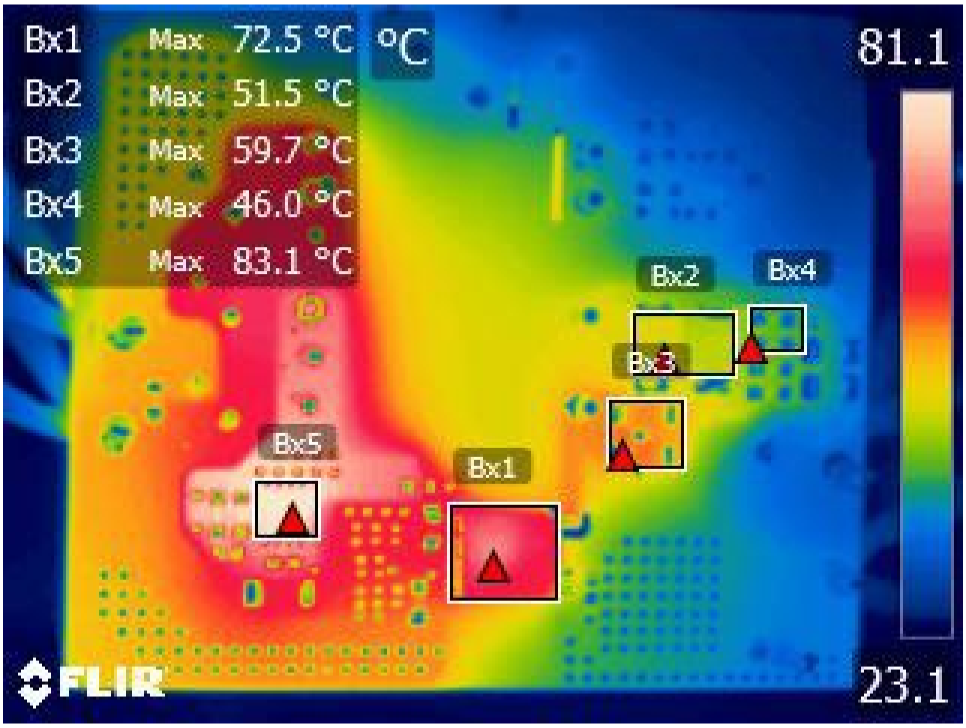
(b) Core



(b) Secondary winding side

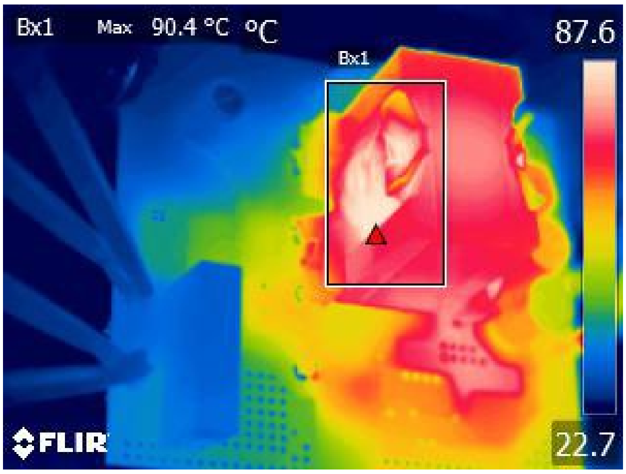
Component Ref. Des.	Component Description	Component Temperature, T [°C]
Transformer T1	Primary Winding	83.5
	Core	73.5
	Secondary Winding	83.6
	Ambient	22.5

Figure 28 – Thermal Image Top View. 800 VDC, Full Power.

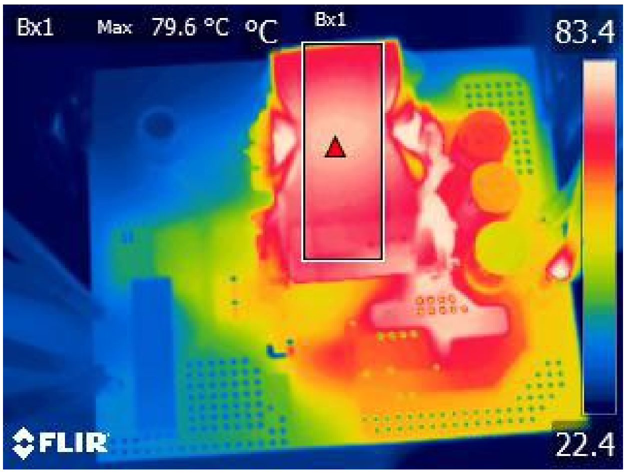


Legend	Component Ref. Des.	Component Description	Component Temperature, T [°C]
Bx1	U1	InnoMux2-EP	72.5
Bx2	VR1/VR2	Snubber Zener	51.5
Bx3	D14/D15	Snubber Diode	59.7
Bx4	R2/R78	Snubber Resistors	46.0
Bx5	Q1	SR FET	83.1
		Ambient	22.9

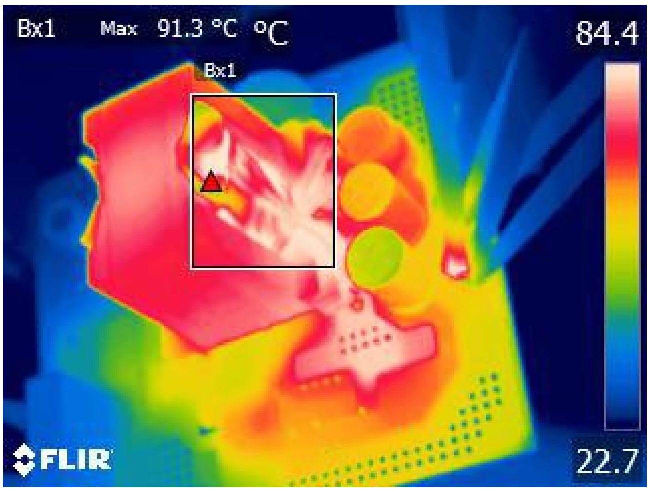
Figure 29 – Thermal Image Bottom View. 800 VDC, Full Power.



(a) Primary winding side



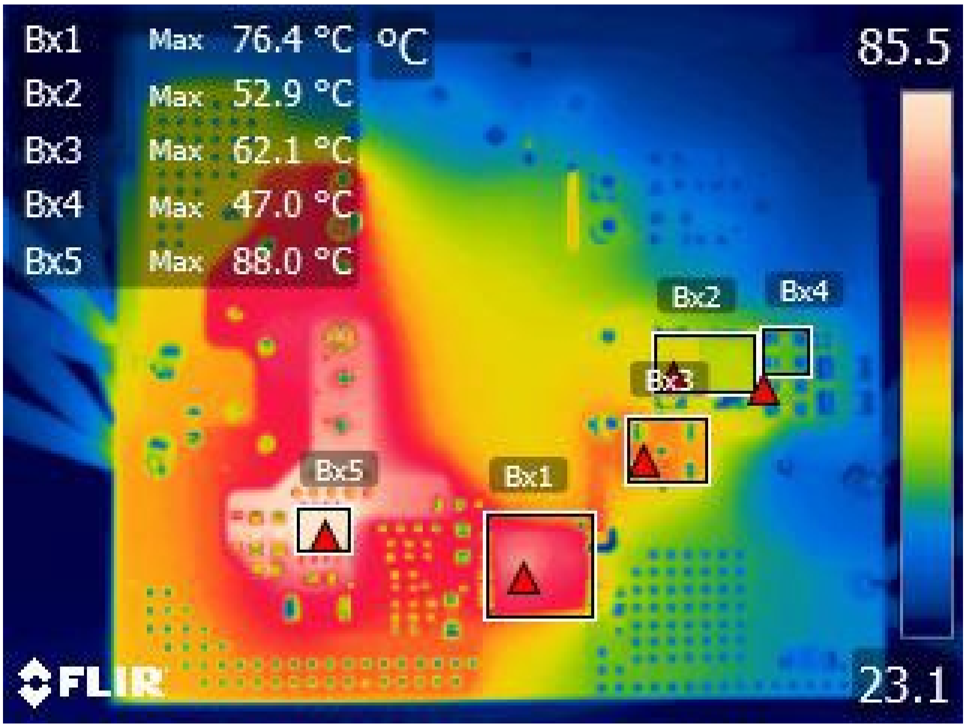
(b) Core



(c) Secondary winding side

Component Ref. Des.	Component Description	Component Temperature, T [°C]
Transformer T1	Primary Winding	90.4
	Core	79.6
	Secondary Winding	91.3
	Ambient	22.7

Figure 30 – Thermal Image Top View. 1000 VDC, Full Power.



Legend	Component Ref. Des.	Component Description	Component Temperature, T [°C]
Bx1	U1	InnoMux2-EP	76.4
Bx2	VR1/VR2	Snubber Zener	52.9
Bx3	D14/D15	Snubber Diode	62.1
Bx4	R2/R78	Snubber Resistors	47.0
Bx5	Q1	SR FET	88.0
		Ambient	23.1

Figure 31 – Thermal Image Bottom View. 1000 VDC, Full Power.

Component	Description	Bottom Side Component Temperature [°C]			
		V_{IN} = 300 VDC	V_{IN} = 500 VDC	V_{IN} = 800 VDC	V_{IN} = 1000 VDC
U1	InnoMux2-EP	91.9	73.3	72.5	76.4
VR1/VR2	Snubber Zener	47.5	49.9	51.5	52.9
D14/D15	Snubber Diode	56.7	57.9	59.7	62.1
R2/R78	Snubber Resistors	42.9	44.8	46.0	47.0
Q1	SR FET	73.6	77.5	83.1	88.0
	Ambient	22.5	22.9	22.9	23.1

Table 9 – Bottom Side Component Temperatures, 300 VDC, 500 VDC, 800 VDC and 1000 VDC, Full Load (100 W).

Component	Description	Top Side Component Temperature [°C]			
		V_{IN} = 300 VDC	V_{IN} = 500 VDC	V_{IN} = 800 VDC	V_{IN} = 1000 VDC
Transformer T1	Pri Winding	64.9	72.7	83.5	90.4
	Core	62.9	65.7	73.5	79.6
	Sec Winding	65.0	73.1	83.6	91.3
	Ambient	22.0	22.1	22.5	22.7

Table 10 – Top Side Component Temperatures, 300 VDC, 500 VDC, 800 VDC and 1000 VDC, Full Load (100 W).

9 Revision History

Date	Author	Revision	Description & Changes	Reviewed
4-Nov-25	JT/AM/CQ	A	Initial Release.	Apps & Mktg

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