Design Example Report

Title	**60 W Isolated Flyback Power Supply using TOPSwitchGaN (TOP7074K)**
Specification	85 – 265 VAC Input; 24 V / 2.5 A Output
Application	Appliances
Author	Applications Engineering Department
Document Number	DER-1079
Date	June 29, 2026
Revision	B

Summary and Features

- >90% full load efficiency at 115 VAC and 92% full load efficiency at 230 VAC
- ≥90% efficient at 10% load across line
- >90% average efficiency at 115 VAC and 230 VAC
- >55% efficient at 230 VAC and 300 mW input power
- <100 mW no-load input power at 230 VAC
- Extensive protection features including:
  - Line overvoltage and undervoltage protection
  - Over Temperature Protection (OTP)
  - Short circuit protection
- Class B conducted EMI with > 6 dB margin

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
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www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a flyback converter that provides an isolated output voltage of 24 V at 2.5 A from a wide input voltage range of 85 VAC to 265 VAC. This power supply utilizes the TOP7074K from the TOPSwitchGaN™ family of ICs.

This document contains the complete power supply specification, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

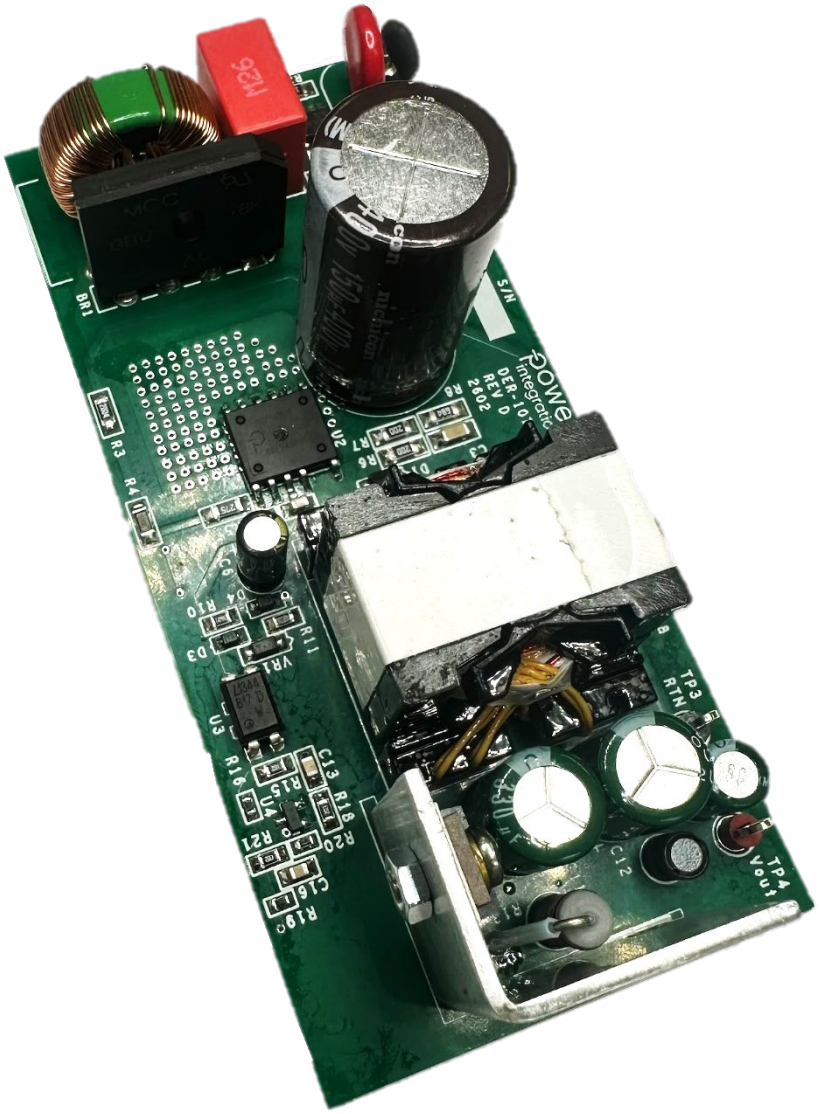


Figure 1 – Oblique View.

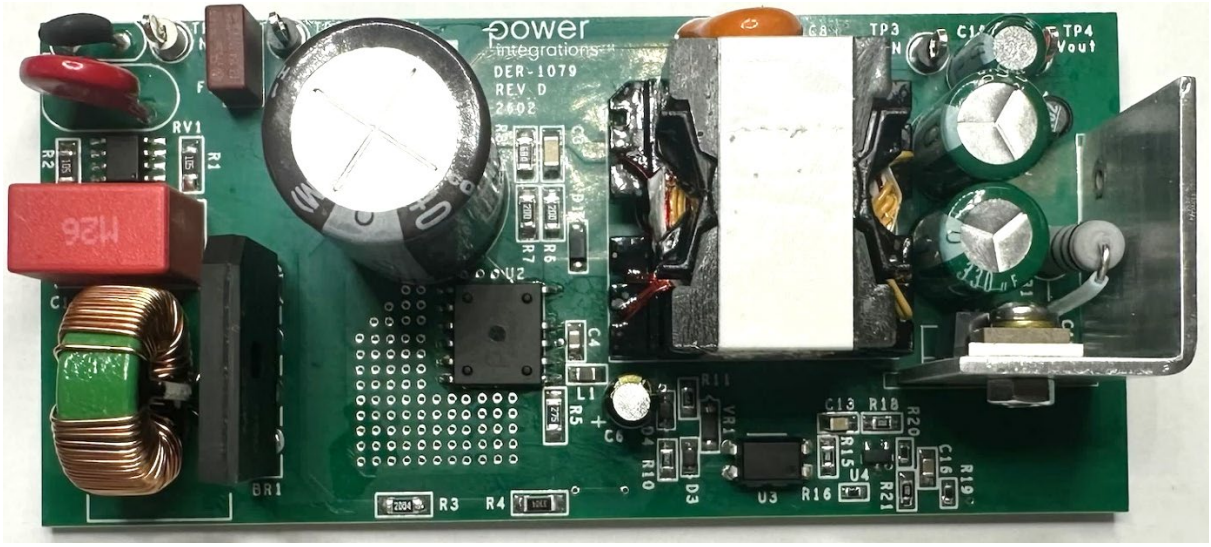


Figure 2 – Top View.

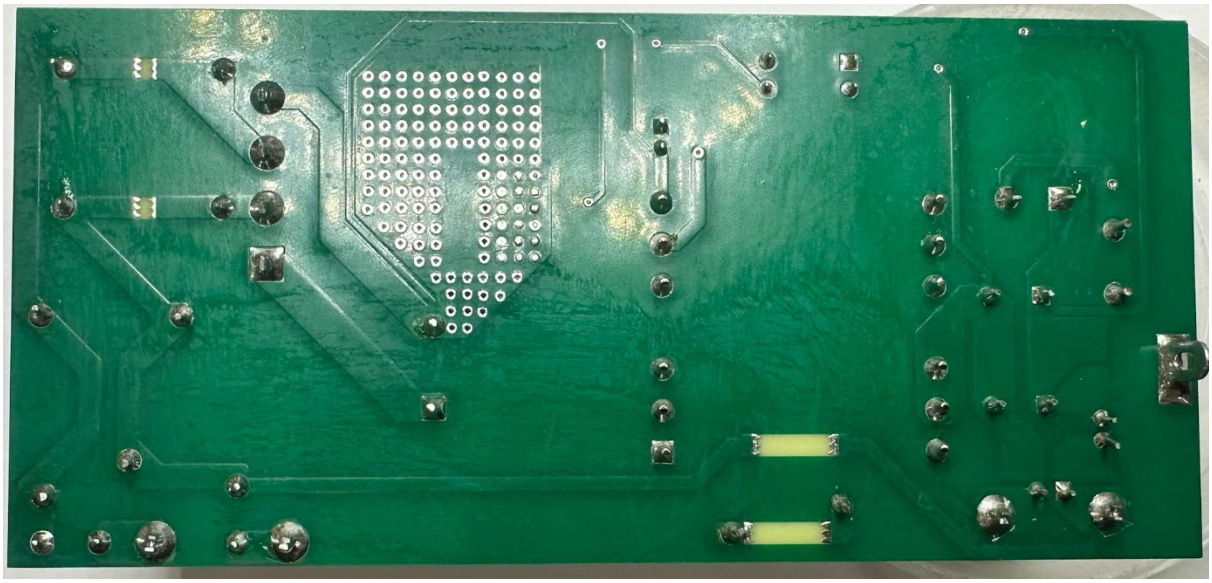


Figure 3 – Bottom View.

2 Power Supply Specification

The table represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50 / 60	64	Hz	
No-load Input Power (230 VAC)				100	mW	
Output1						
Output Voltage	V_{OUT1}	22.8	24	25.2	V	± 5%
Output Ripple Voltage	$V_{RIPPLE1}$			240	mV	20 MHz Bandwidth.
Output Current	I_{OUT1}	0		2.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		60		W	
Efficiency						
Full Load 115 VAC	$\eta_{115\ VAC}$		90		%	Measured at P_{OUT} 25 °C.
Full Load 230 VAC	$\eta_{230\ VAC}$		91		%	
Average efficiency at 25, 50, 75 and 100% of P_{OUT}	η_{DOE}		88		%	Measured at Nominal Input 115 VAC and 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge (Differential)				±2	kV	1.2/50 μs Surge, IEC 61000-4-5 Differential Mode: Series Impedance = 2 Ω
Ring Wave (Common Mode)				±6	kV	100 kHz Ring Wave Common Mode: Series Impedance = 12 Ω
Electrical Fast Transient (EFT)				±4	kV	15 ms @ 5 kHz 0.75 ms @ 100 kHz
ESD – Air Discharge				±16.5	kV	
ESD – Contact Discharge				±8.8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

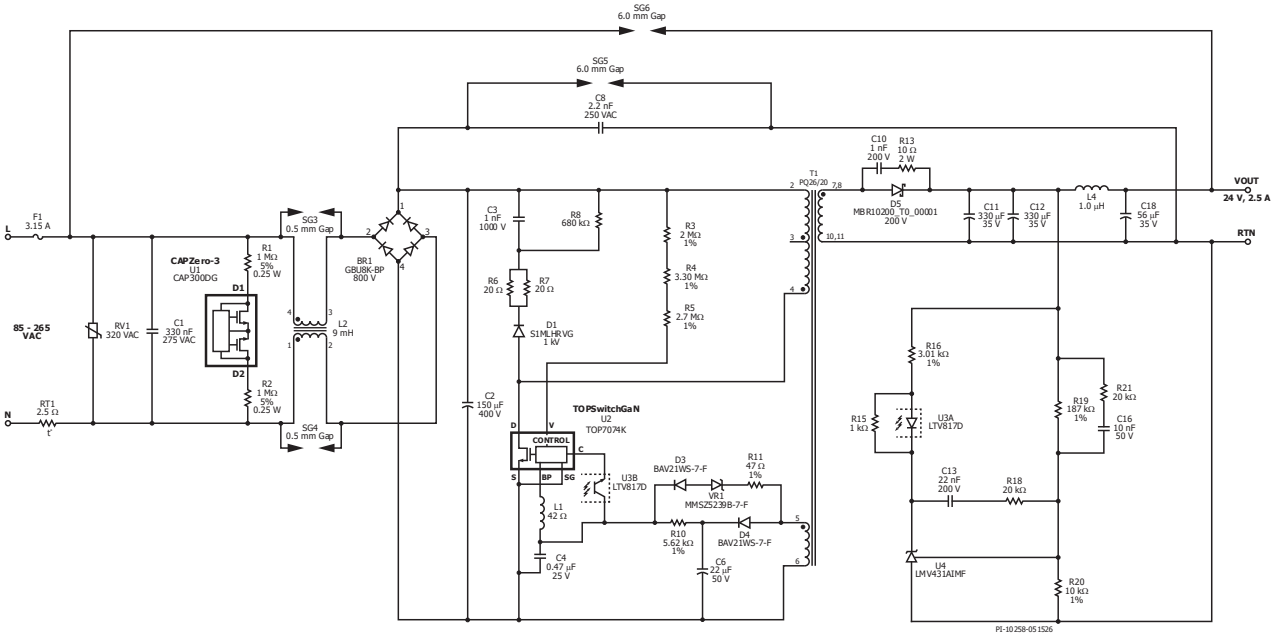


Figure 4 – Schematic.

4 Circuit Description

This power supply employs a TOP7074K off-line switcher IC, (U2), in a flyback configuration. U2 has an integrated high voltage PowiGaN switch. It regulates the output by adjusting the PowiGaN switch off time duration, which is proportional to the current fed into its CONTROL pin. ILIM is adjusted according to switching frequency.

4.1 Input EMI Filtering and Rectification

Fuse F1 isolates the circuit and provides protection from component failure. X-Capacitor C1 together with common mode choke (CMC) L2 forms an EMI filter that attenuates both common mode and differential mode conducted EMI. BR1 converts the AC line voltage into the DC voltage seen across bulk capacitor C2. The CAPZero™-3 IC (U1) along with bleed resistors, R1 and R2, discharges the stored energy in X capacitor C1 when AC is disconnected, meeting safety requirements. When AC is connected the resistors are disconnected, reducing no-load power consumption.

4.2 TOPSwitchGaN Primary

The TOP7074K device (U2) integrates an oscillator, a switch controller, start-up and protection circuitry, and PowiGaN switch, all on one monolithic IC. One side of the power transformer (T1) primary winding is connected to the positive side of the bulk capacitor C2, and the other side is connected to the DRAIN pin (D pin) of U2. When the PowiGaN switch turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The spike amplitude is limited by an RCD clamp network that consists of D1, R6, R7, C3 and R8. Resistors R6 and R7 are used together with capacitor C3 and resistor R8 to damp high frequency ringing and improve EMI. This arrangement was selected to reduce clamp losses under light and no-load conditions. Y capacitor C8, connected between the primary and secondary side helps improve EMI.

The TOP7074K regulates the output by adjusting the power PowiGaN switch off-time duration in proportion to the current into its CONTROL pin. The power supply output voltage is sensed on the secondary side by shunt regulator U4 and provides a feedback signal to the primary side through optocoupler U3.

Line undervoltage and overvoltage thresholds are determined by the current supplied from resistors R3, R4 and R5 to the V pin. R11, D3, and VR1 provide output overvoltage protection (OVP). An increase in output voltage causes an increase in the bias winding voltage, sensed by VR1. Once VR1 is activated, it will inject current to the BP pin causing the IC U2 to shut down and enter auto-restart (AR).

At start-up, bypass capacitor C4 is charged through the DRAIN (D) pin, which is placed as close as possible to U2. Once it is charged, U2 begins to switch. Capacitor C4 stores enough energy to ensure the TOPSwitchGaN IC is powered until the output reaches regulation. The value of C4 also sets the maximum ILIM for the primary switch (in this case ILIM is set to standard). After start-up, the bias winding delivers current via diode D4 and R10 to

charge capacitor C6 which in turn powers the controller. Resistor R10 is used to set the typical bias current of the IC U4. Ferrite bead L1 minimizes the noise on the BP Pin.

4.3 Output Rectification

Schottky diode D5 rectifies the secondary winding output of T1. The output voltage is filtered by C11, C12, C18 and L4. Resistor R13 and capacitor C10 snubs the voltage spike caused by the commutation of D5. Low ESR capacitors C11, C12 and LC filter L4 and C18 help in minimizing output voltage ripple.

4.4 Output Feedback

The reference IC, U4 (LMV431AIMF), is used to set the output voltage programmed via the feedback resistor divider composed of R19 and R20. The LMV431AIMF varies its cathode voltage to keep its input voltage constant (1.24 V, ±1%). As the cathode voltage changes, the current through the optocoupler LED and corresponding photo-transistor within U2 changes. R16, C13, R18, R21 and C16 ensure stable operation, while resistor R15 maintains minimum bias to U3.

5 PCB Layout

5.1 PCB Specification

- Layer: 2
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz
- Finishing: LF HASL
- Material: FR4
- Solder mask: Green
- Silkscreen: White

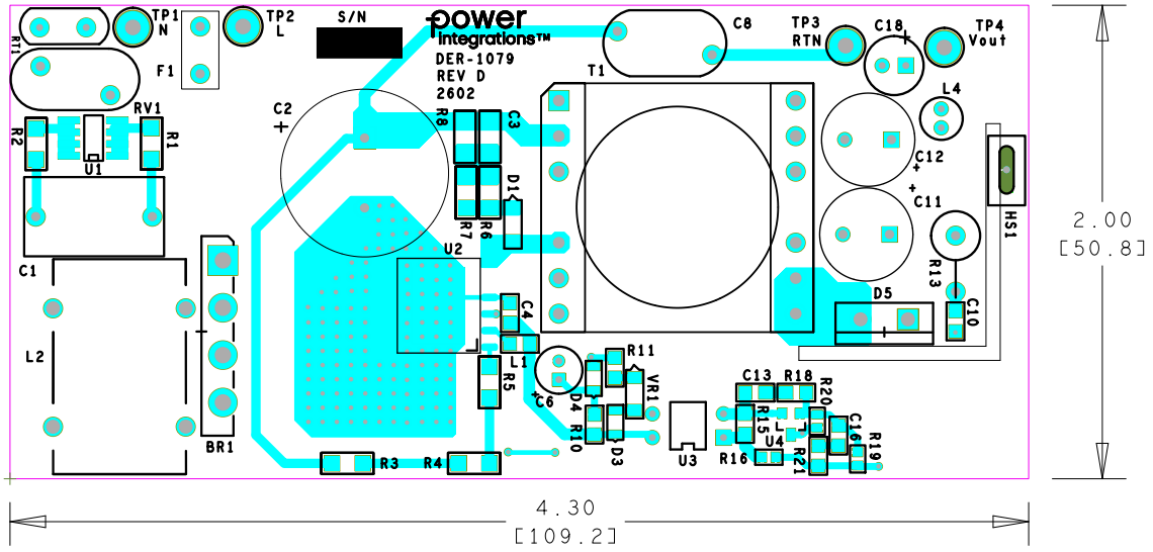


Figure 5 – Printed Circuit Board, Top View.

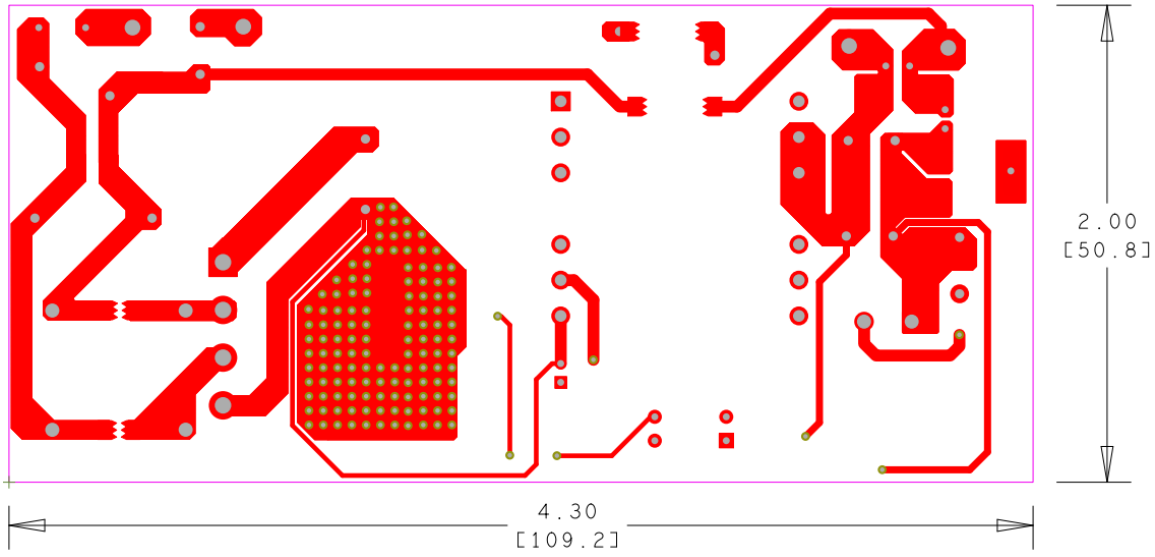


Figure 6 – Printed Circuit Board, Bottom View.

6 Bill of Materials

6.1 Electrical BOM

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial Co.
2	1	C1	330 nF, ±10%, 275 VAC, Film Capacitor, X2, 15 mm x 8.5 mm	890324024003CS	Wurth Electronics Inc.
3	1	C2	150 μF, ±20%, 400 V, Aluminum Electrolytic Capacitor, 18 mm x 33.5 mm	UCP2G151MHD6	Nichicon
4	1	C3	1 nF, ±10%, 1000 V, Ceramic Capacitor, X7R, 1206 (3216 Metric)	CC1206KKX7RCBB102	Yageo
5	1	C4	0.47 μF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	CGA4J2X7R1E474K125AA	TDK Corporation
6	1	C6	22 μF, ±20%, 50 V, Aluminum Electrolytic Capacitor, 5 mm x 11 mm	EEU-FM1H220H	Panasonic Electronic Components
7	1	C8	2200 pF, ±20%, 500 VAC (Y1), 760 VAC (X1), Ceramic Capacitor, Y5U (E), Radial	440LD22-R	Vishay
8	1	C10	1 nF, ±10%, 200 V, Ceramic, X7R, 0805 (2012 Metric)	08052C102KAT2A	AVX Corp
9	2	C11 C12	330 μF, ±20%, 35 V, Aluminum Electrolytic Capacitor, Very Low ESR, 38 mΩ, 10 mm x 16 mm	EKZE350ELL331MJ16S	Nippon Chemi-Con
10	1	C13	22 nF, ±10%, 200 V, Ceramic, X7R, 0805 (2012 Metric)	08052C223KAT2A	AVX Corp
11	1	C16	10 nF, ±10%, 50 V, Ceramic, X7R, 0805 (2012 Metric)	C0805X103K5RAC7210	Kemet
12	1	C18	56 μF, ±20%, 35 V, Aluminum Electrolytic, Very Low ESR, 130 mΩ, 6.3 mm x 11 mm	EKZE350ELL560MF11D	Nippon Chemi-Con
13	1	D1	1000 V, 1 A, Diode, Standard, Surface Mount, Sub SMA	S1MLHRVG	TAIWAN SEMICONDUCTOR
14	2	D3 D4	200 V, 200 mA, Diode, Standard, SOD-323	BAV21WS-7-F	Diode Inc.
15	1	D5	200 V, 10 A, Diode, Schottky, Through Hole TO-220AC	MBR10200_T0_00001	Panjit International Inc.
16	1	F1	3.15 A, 300 V, Fuse Board Mount, Slow Blow, Radial	36913150000	Littelfuse Inc
17	1	L1	42 ohms @ 100 MHz, Ferrite Bead, 0805 (2012 Metric)	LSMCC201208T420RG	Taiyo Yuden
18	1	L2	9 mH, 2 A, Common Mode Choke	T18107V-902S P.I. Custom	Fontaine Technologies
19	1	L4	1.0 μH, ±20%, 3 A, 20 mΩ, Fixed Inductor	11R102C	Murata Power Solutions Inc
20	2	R1 R2	1 MΩ, ±5%, 0.25 W, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	RMCF1206JT1M00	Stackpole Electronics Inc
21	1	R3	2.00 MΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-8ENF2004V	Panasonic
22	1	R4	3.30 MΩ, ±1%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	KTR18EZPF3304	Rohm Semiconductor
23	1	R5	2.7 MΩ, ±5%, 1/4 W Chip Resistor, Thick Film, 1206 (3216 Metric)	RC1206FR-072M7L	YAGEO
24	2	R6 R7	20 Ω, ±5%, 2/3 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-P08J200V	Panasonic

25	1	R8	680 kΩ, ±5%, 2/3 W Chip Resistor, Thick Film, 1206 (3216 Metric)	ERJ-P08J684V	Panasonic
26	1	R10	5.62 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF5621V	Panasonic
27	1	R11	47.0 Ω, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF47R0V	Panasonic
28	1	R13	10 Ω, ±5%, 2 W, Through Hole Resistor, Metal Oxide	RSF200JB-10R	Yageo
29	1	R15	1 kΩ, ±5%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6GEYJ102V	Panasonic
30	1	R16	3.01 kΩ, ±1%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6ENF3011V	Panasonic
31	2	R18 R21	20 kΩ, ±5%, 1/8 W Chip Resistor, Thick Film, 0805 (2012 Metric)	ERJ-6GEYJ203V	Panasonic
32	1	R19	187 kΩ, ±1%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	ERJ-3EKF1873V	Panasonic
33	1	R20	10.0 kΩ, ±1%, 1/10 W Chip Resistor, Thick Film, 0603 (1608 Metric)	ERJ-3EKF1002V	Panasonic
34	1	RT1	2.5 Ω, ±25%, 3 A, Inrush Current Limiter	SL08 2R503	Ametherm
35	1	RV1	510 V, 2.5 kA Varistor, 48 J, Through Hole Disc, 10 mm	V320LA10P	Littelfuse
36	1	T1	Bobbin, PQ26/20, Vertical, 12 pins	B65878E0012D001	EPCOS (TDK)
37	1	U1	CAPZero-3, CAP300DG, SO-8C	CAP300DG	Power Integrations
38	1	U2	TOPSwitchGaN, TOP7074K, eSOP-12B	TOP7074K	Power Integrations
39	1	U3	Optoisolator, Transistor Output, 5000 V_{RMS}, 35 V, CTR 300-600%, 1 Channel 4-DIP	LTV-817D	Liteon
40	1	U4	1.24 V Shunt Regulator IC, 1%, -40 to 85 °C, SOT23-3	LMV431AIMF/NOPB	Texas Instruments
41	1	VR1	9.1 V 500 MW, Diode, Zener, SOD-123	MMSZ5239B-7-F	Diodes, Inc

6.2 Mechanical BOM

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	2	TP2 TP3	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	TP4	Test Point, BLK, THRU-HOLE MOUNT	5010	Keystone
4	1	HS1	Heatsink, DER-1079 Rev-B	61-00386-00	Power Integrations
5	1	HS2	Terminal, Eyelet, Tin Plated Brass, Zierick	190	Keystone
6	1		Wakefield Thermal Joint Compound	120-SA	Wakefield
7	1		Flat Washer #4	5205820-2	Tyco Electronics
8	1		Washer Shoulder, #4, 0.140 Shoulder	7721-3PPSG	Aavid Thermalloy
9	1		#4-40 x 0.375 Machine Screw	PMSSS 440 0038 PH	Building Fasteners
10	1		Nut, Hex, Kep 4-40, S ZN Cr3 plating RoHS	.4CKNTZR	Olander

7 Transformer Specification

7.1 Electrical Diagram

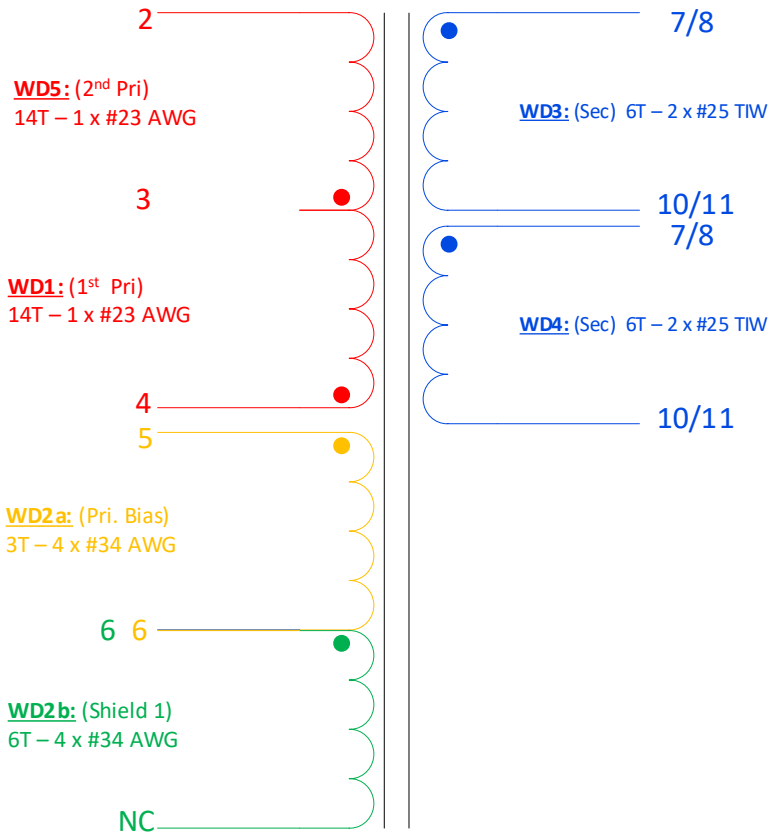


Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK} and 100 kHz frequency, between pin 2 to pin 4, with all other Windings open.	454 µH
Tolerance	Tolerance of Primary Inductance.	±5%
Leakage Inductance	Measured across primary winding with all other windings shorted.	< 4.54 µH

7.3 Material List

Item	Description
[1]	Core: PQ26/20, TDK-PC95; or equivalent.
[2]	Bobbin: PQ26/20, Vertical, 12 pins (6/6).
[3]	Magnet wire: #23 AWG, double coated.
[4]	Magnet wire: #34 AWG, double coated.
[5]	Magnet wire: #25 AWG, Triple Insulated Wire.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 9.3 mm width.
[7]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

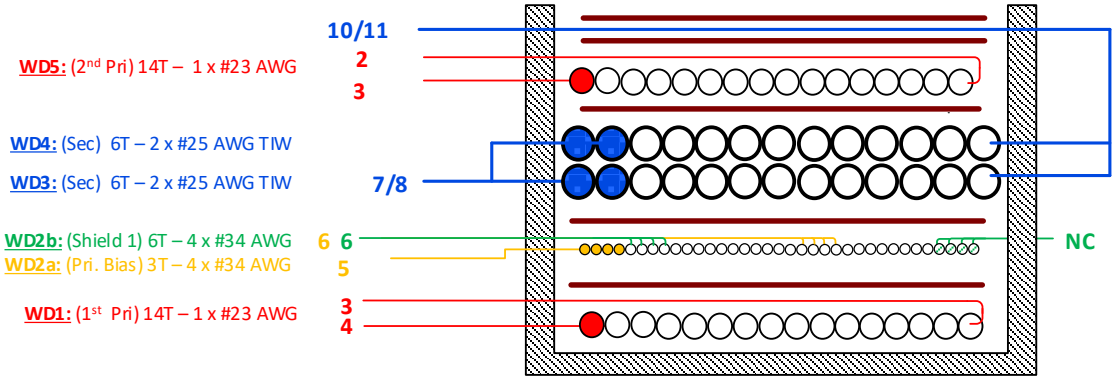
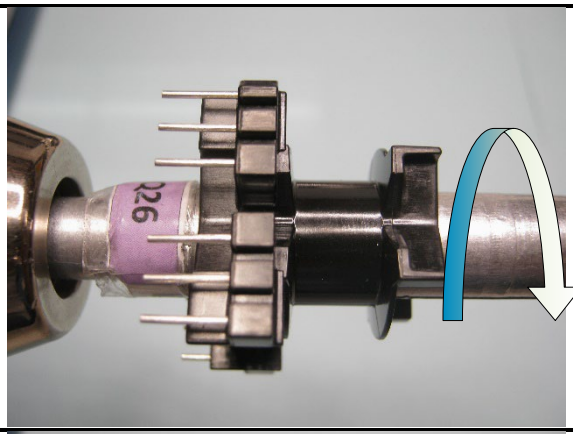
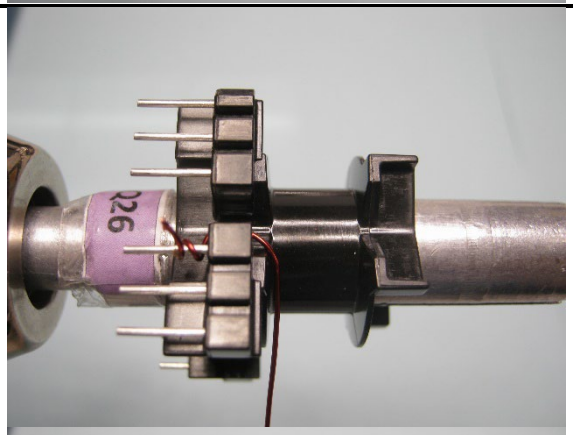
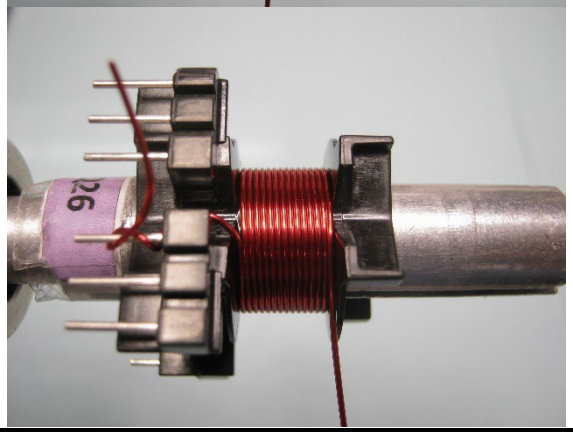


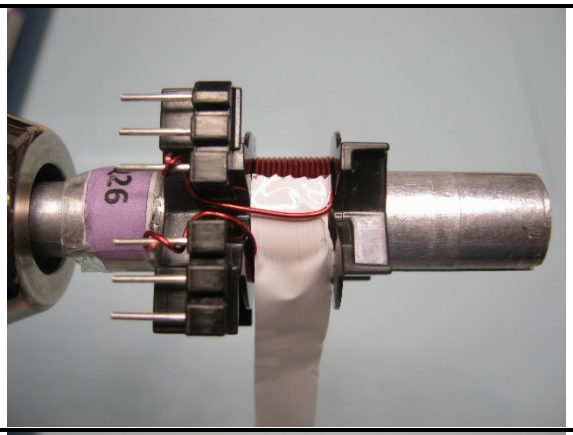
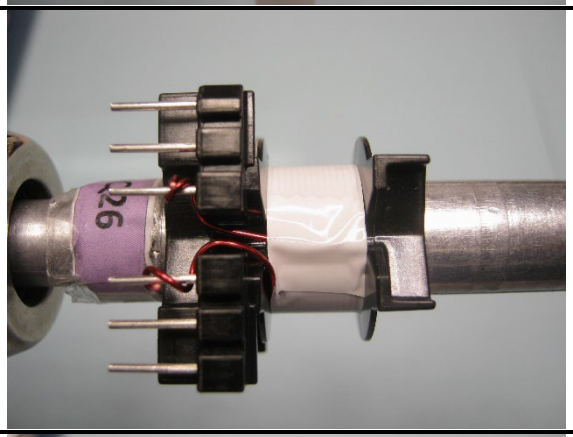
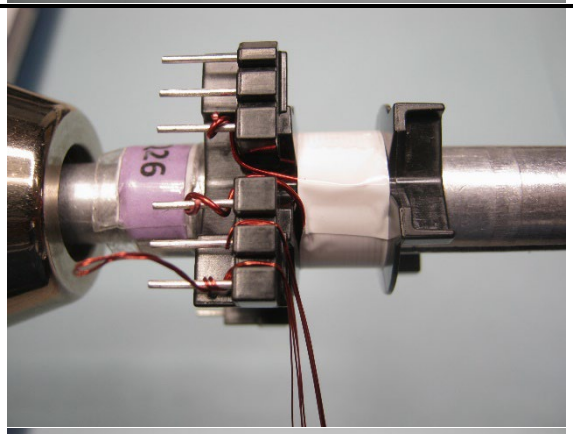
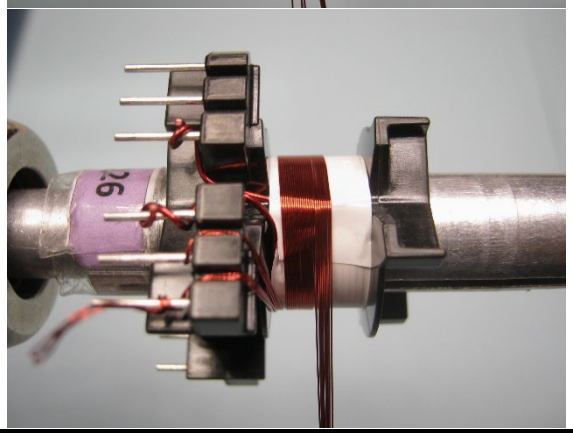
Figure 8 – Transformer Build Diagram.

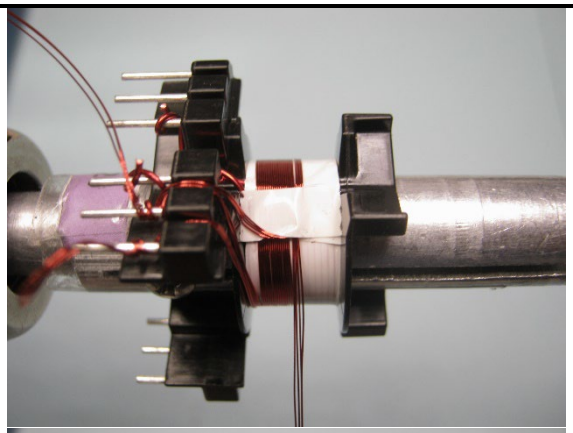
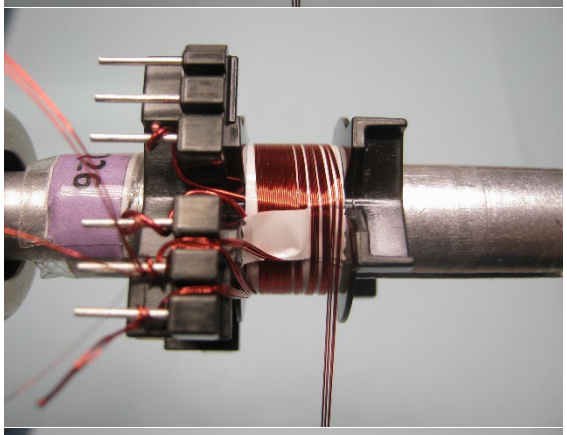
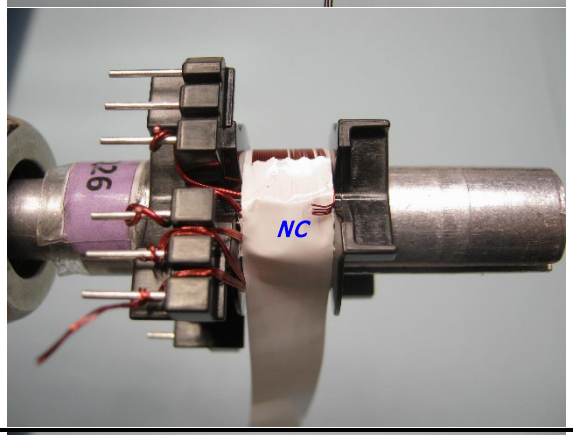
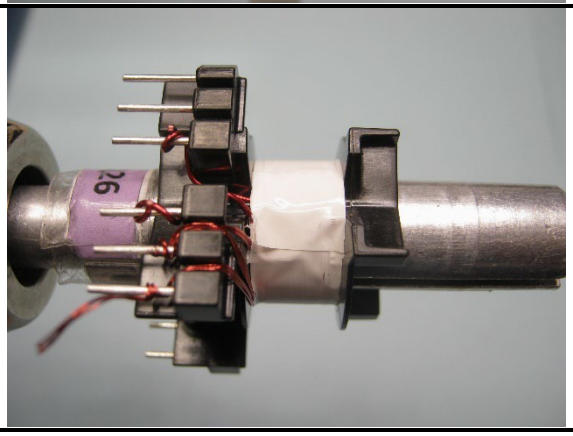
7.5 Transformer Instructions

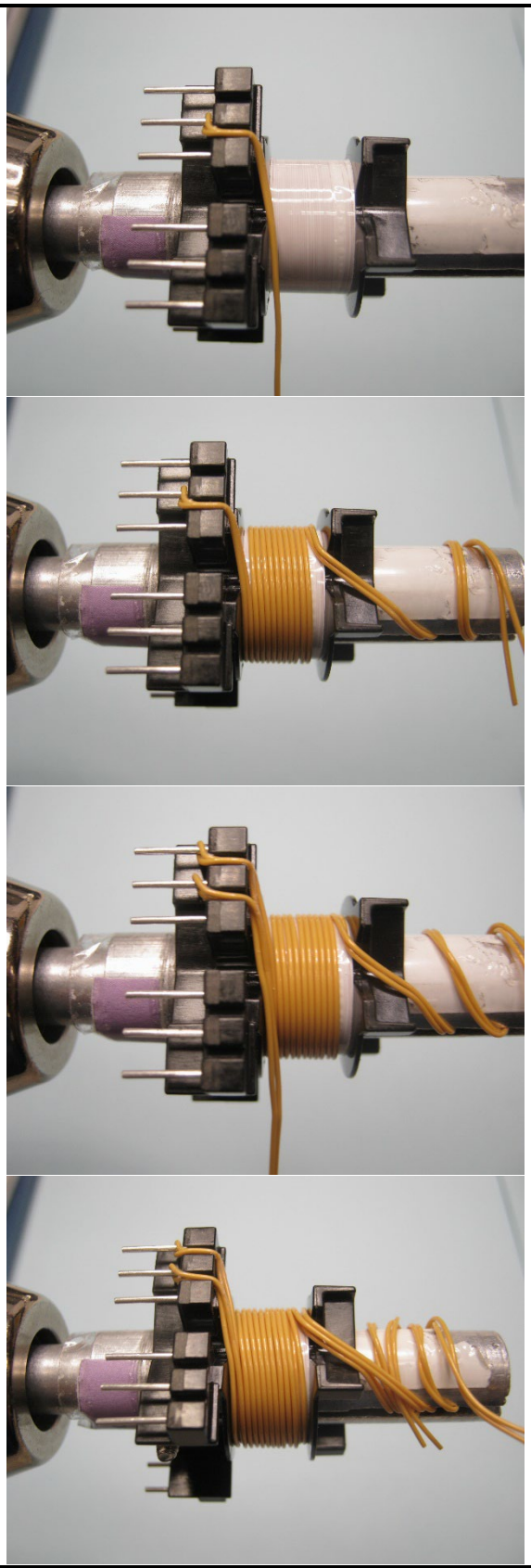
Winding preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 1st Primary	Start at pin 4, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 3.
Insulation	1 layer of tape Item [6].
WD2: Bias & WD2: Shield	Use 4 wires Item [4] start at pin 5 for Bias winding, also use 4 wires same Item [4] start at pin 6 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 small piece of tape to hold the windings, bring 4 wires of Bias winding to the left and terminate at pin 6. Continue winding 3 more turns then cut short 4 wires for Shield Winding as No-Connect.
Insulation	1 layer of tape Item [6].
WD3 & WD4 Secondary	Start at pin 7, use 2 wires of Item [5], wind 6 turns from left to right. At the last turn exit the wires and leave ~ 1" floating for later termination for WD3-Secondary. Repeat the same with start pin 8 and exit the wires as above for WD4-Secondary.
Insulation	1 layer of tape Item [6].
WD5 2nd Primary	Start at pin 3, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 2.
Insulation	1 layer of tape Item [6].
Finish	Bring 4 wires floating from secondary winding to the left to terminate at pins 10 and 11. Secure the wires with 2 layers of tape Item [6]. Gap core halves to get 443 μH and secure with tape. Varnish with Item [7].

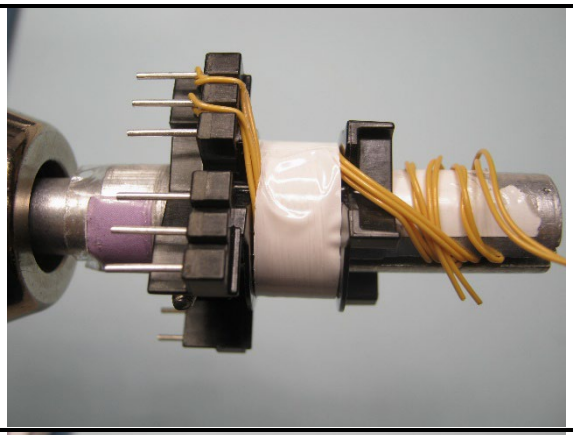
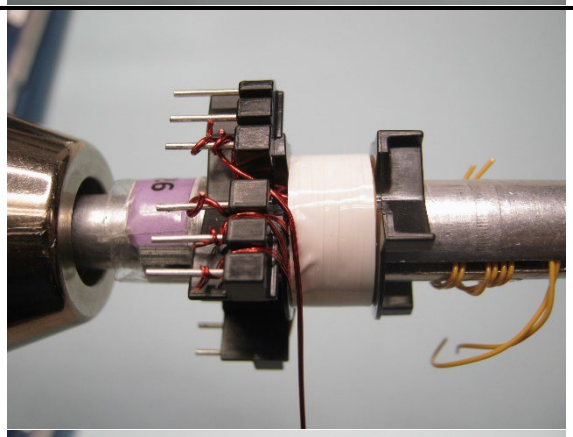
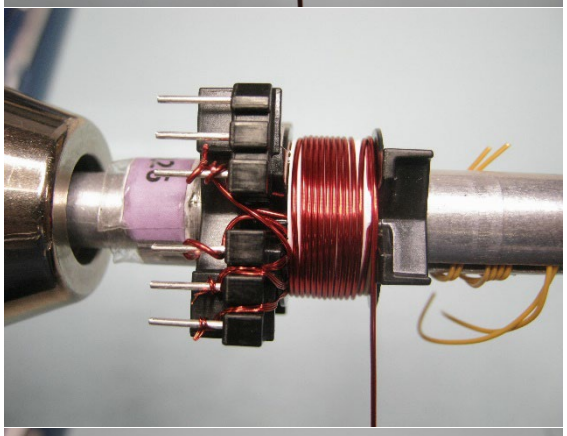
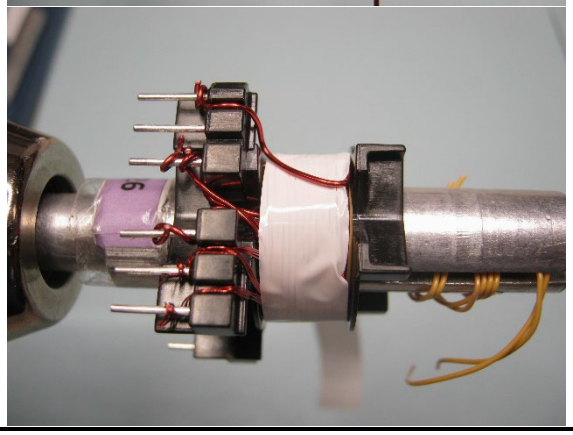
7.6 Transformer Winding Illustrations

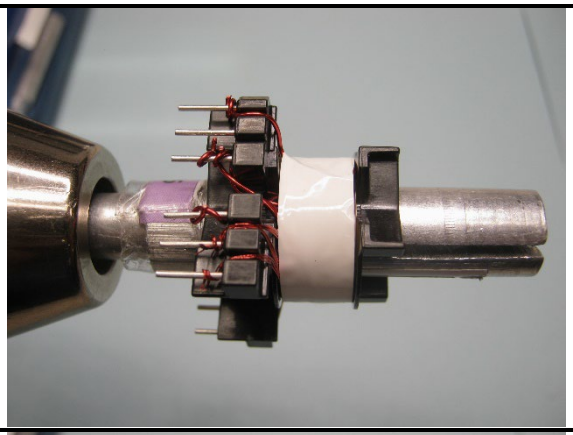
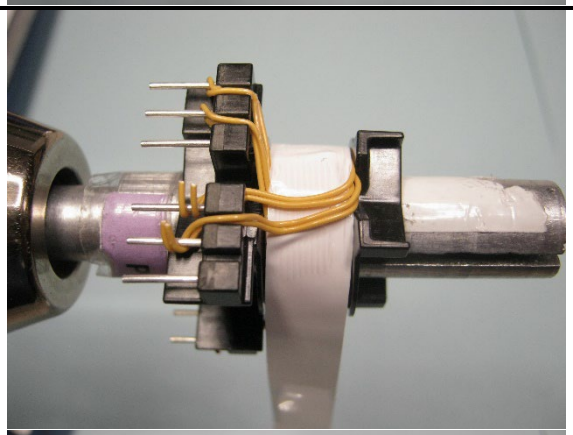
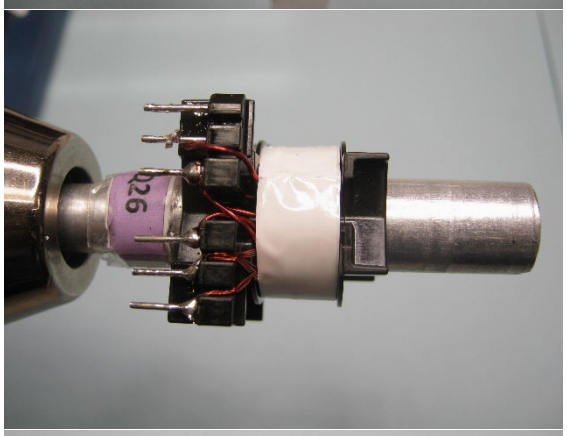
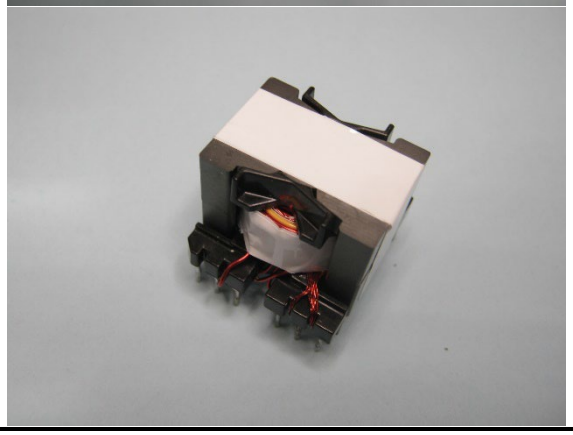
Winding preparation		Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**	 	Start at pin 4, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 3.

		
Insulation		1 layer of tape Item [6].
WD2: Bias **&** **WD2: Shield**	 	Use 4 wires Item [4] start at pin 5 for Bias winding, also use 4 wires same Item [4] start at pin 6 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 small piece of tape to hold the windings, bring 4 wires of Bias winding to the left and terminate at pin 6. Continue winding 3 more turns then cut short 4 wires for Shield Winding as No-Connect.

	  	
Insulation		1 layer of tape Item [6].

WD3 & WD4 Secondary		Start at pin 7, use 2 wires of Item [5], wind 6 turns from left to right. At the last turn exit the wires and leave ~ 1” floating for later termination for WD3-Secondary. Repeat the same with start pin 8 and exit the wires as above for WD4-Secondary.

Insulation		1 layer of tape Item [6].
WD5 **2nd Primary**	  	Start at pin 3, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 2.

Insulation		1 layer of tape Item [7].
Finish	  	Bring 4 wires floating from secondary winding to the left to terminate at pins 10 and 11 Secure the wires with 2 layers of tape Item [6]. Gap core halves to get 443 μH and secure with tape. Varnish with Item [7].

8 Design Spreadsheet

1	ACDC_TOPSwitchGaN_Flyback_060126; Rev.1.0; Copyright Power Integrations 2026	INPUT	INFO	OUTPUT	UNITS	TOPSwitchGaN Single/Multi Output Flyback Design Spreadsheet
2	APPLICATION VARIABLES					Design Title
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	85		85	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			85-265 VAC		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	150.0		150.0	μF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	IOUT	2.500		2.500	A	Output current
11	POUT			60.00	W	Output power
12	EFFICIENCY	0.86		0.86		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.60		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
15						
16						
17						
18	PRIMARY CONTROLLER SELECTION					
19	PACKAGE_DEVICE	eSOP		eSOP		Device Package
20	ILIMIT_MODE			STANDARD		Device current limit mode
21	DEVICE_GENERIC	AUTO		TOP7074		Generic device code
22	DEVICE_CODE			TOP7074K		Actual device code
23	POUT_MAX			70	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			1.02	Ω	Primary switch on time drain resistance at 100 °C
25	ILIMIT_MIN			1.760	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			1.900	A	Typical current limit of the primary switch
27	ILIMIT_MAX			2.040	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			800	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.74	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			598.4	V	Peak drain voltage on the primary switch during turn-off. A 110 V leakage spike voltage is assumed
31						
32						
33						
34	WORST CASE ELECTRICAL PARAMETERS					
35	FSWITCHING_MAX	119500		119500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage.
36	VOR	115.0		115.0	V	Secondary voltage reflected to the primary when the primary switch turns off

37	VMIN			91.90	V	Valley of the minimum input AC voltage at full load
38	KP			0.54		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.558		Primary switch duty cycle
41	TIME_ON_MAX			9.26	µs	Primary switch on-time
42	TIME_ON_AT_FSWITCHING_MAX			4.67	µs	Primary switch on-time at FSWITCHING_MAX
43	TIME_OFF			3.70	µs	Primary switch off-time at 85 VAC, 60 W, and 119500 Hz.
44	LPRIMARY_MIN			431.6	µH	Minimum primary inductance
45	LPRIMARY_TYP			454.4	µH	Typical primary inductance
46	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			477.1	µH	Maximum primary inductance
48						
49	PRIMARY CURRENT					
50	IPEAK_PRIMARY			2.002	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			0.813	A	Primary switch current pedestal
52	IAVG_PRIMARY			0.722	A	Primary switch average current
53	IRIPPLE_PRIMARY			1.413	A	Primary switch ripple current
54	IRMS_PRIMARY			1.014	A	Primary switch RMS current
55						
56	SECONDARY CURRENT					
57	IPEAK_SECONDARY			9.341	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			3.796	A	Secondary winding current pedestal
59	IRMS_SECONDARY			4.214	A	Secondary winding RMS current
60						
61						
62						
63	TRANSFORMER CONSTRUCTION PARAMETERS					
64	CORE SELECTION					
65	CORE	PQ26		PQ26		Core selection. Refer to the Magnetics Designer tab to see the detailed report
66	CORE CODE			PQ26/20-3C95		Core code
67	AE			121.00	mm^2	Core cross sectional area
68	LE			45.00	mm	Core magnetic path length
69	AL			7020	nH/turns^2	Ungapped core effective inductance
70	VE			5470.0	mm^3	Core volume
71	BOBBIN			CPV-PQ26/20-1S-12P-Z		Bobbin
72	AW			33.30	mm^2	Window area of the bobbin
73	BW			9.00	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75						
76	PRIMARY WINDING					

77	NPRIMARY			28	turns	Primary turns
78	BPEAK			2965	Gauss	Peak flux density
79	BMAX			2793	Gauss	Maximum flux density
80	BAC			970	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			580	nH/turns^ 2	Typical gapped core effective inductance
82	LG			0.241	mm	Core gap length
83						
84	PRIMARY BIAS WINDING					
85	NBIAS_PRIMARY			3	turns	Primary bias winding number of turns
86						
87	SECONDARY WINDING					
88	NSECONDARY	6		6	turns	Secondary winding number of turns
89						
90	SECONDARY BIAS WINDING					
91	NBIAS_SECONDARY			NA	turns	Secondary bias winding number of turns
92						
93						
94						
95	PRIMARY COMPONENTS SELECTION					
96	LINE UNDERVOLTAGE					
97	BROWN-IN REQURED	77.00		77.00	V	Required AC RMS/DC line voltage brown-in threshold
98	RLS			8.04	MΩ	Connect two 4.02 MOhm resistors to the V-pin for the required UV/OV threshold
99	BROWN-IN ACTUAL			64.5 V - 79.5 V	V	Actual AC RMS/DC brown-in range
100	BROWN-OUT ACTUAL			54.9 V - 68.6 V	V	Actual AC RMS/DC brown-out range
101						
102	LINE OVERVOLTAGE					
103	OVERVOLTAGE_LINE			302.5 V - 339.6 V	V	Actual AC RMS/DC line over-voltage range
104						
105	PRIMARY BIAS DIODE					
106	VBIAS_PRIMARY	10.0		10.0	V	Rectified primary bias voltage
107	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE_PRIMARY			52.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
110	CBP			0.47	µF	BP pin capacitor
111						
112						
113						
114	SECONDARY COMPONENTS					
115	VREF_REG			1.25	V	Reference voltage of the feedback
116	RFB_UPPER			182.00	kΩ	Upper feedback resistor (connected to the first output voltage)

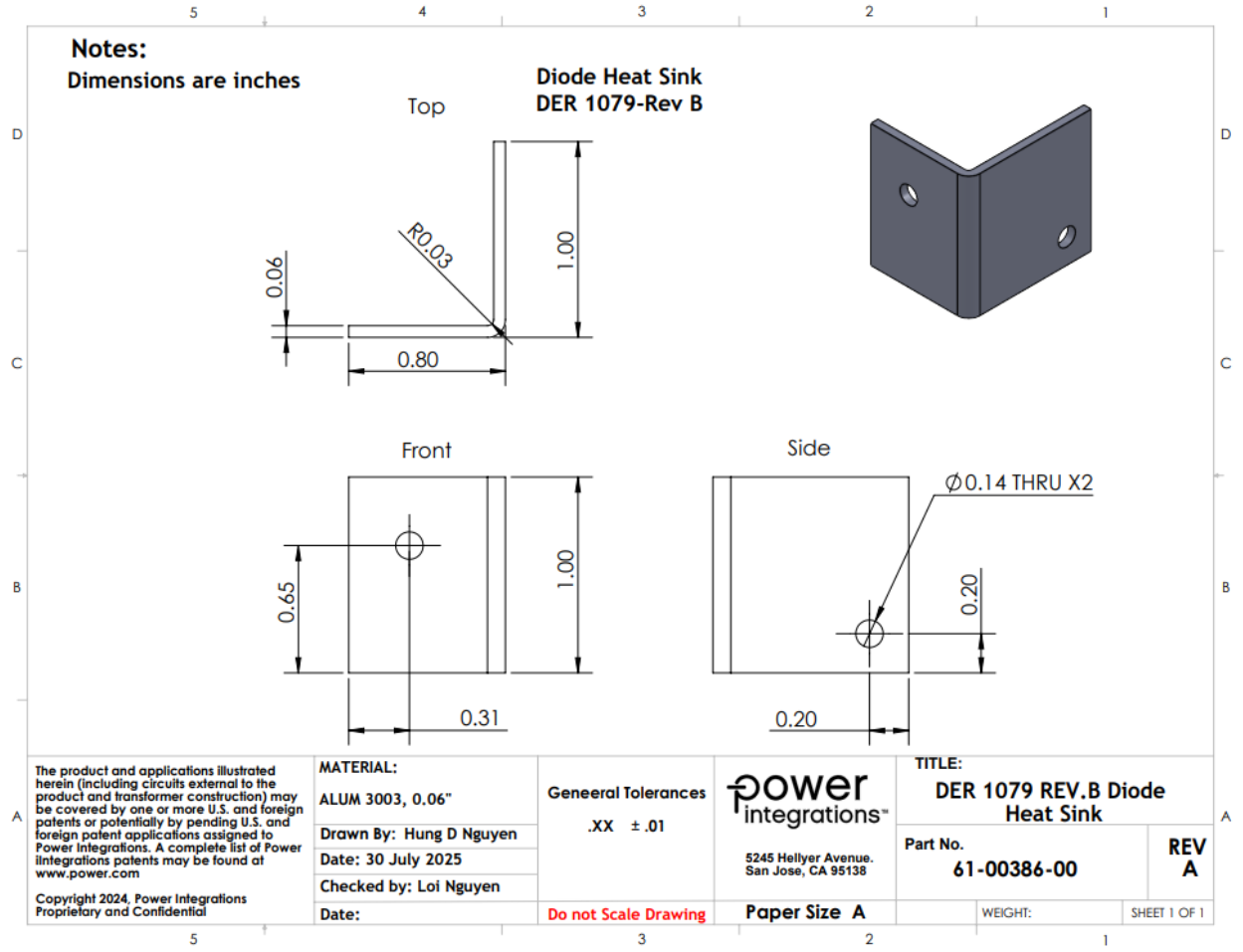
117	RFB_LOWER			10.00	kΩ	Lower feedback resistor
118						
119	SECONDARY BIAS					
120	USE_SECONDARY_BIAS	NO		NO		Use secondary bias winding for the design
121	SEC_BIAS_FORWARD	NO		NA		Secondary bias in-phase with primary. A Linear voltage regulator is connected after the secondary bias rectification capacitor. Select "YES" to enable this configuration
122	VZ_LINEAR_REGULATOR			NA	V	Zener voltage for linear regulator. Only applicable if SEC_BIAS_FORWARD is enabled.
123	VBIAS_SECONDARY_TARGET			NA	V	Target secondary bias rectified voltage (Affects Secondary Bias turns value)
124	VBIAS_SECONDARY_ACTUAL			NA	V	Secondary bias rectified voltage (Calculated using actual secondary bias winding turns).
125	OUTPUT_VBIAS_SECONDARY			NA	V	Secondary bias output voltage
126	VF_BIAS_SECONDARY			NA	V	Bias winding diode forward drop
127	VREVERSE_BIASDIODE_SECONDARY			NA	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
128	CBIAS_SECONDARY			NA	µF	Bias winding rectification capacitor
129						
130						
131	MULTIPLE OUTPUT PARAMETERS					
132	OUTPUT 1					
133	VOUT1			24.00	V	Output 1 voltage
134	IOUT1			2.50	A	Output 1 current
135	POUT1			60.00	W	Output 1 power
136	VD1			0.70	V	Forward voltage drop of diode for output 1
137	NS1			6	turns	Number of turns for output 1
138	ISPEAK1			9.34	A	Instantaneous peak value of the secondary current for output 1
139	ISRMS1			4.214	A	Root-mean-squared value of the secondary current for output 1
140	ISRIPPLE1			3.392	A	Current ripple on the secondary waveform for output 1
141	PIV1_CALCULATED			124.62	V	Computed peak inverse voltage stress on the diode for output 1
142	OUTPUT_RECTIFIER1	AUTO		MUR620		Recommended diode for output 1.
143	PIV1_RATING			200.00	V	Peak inverse voltage rating on the diode for output 1
144	TRR1			35.00	ns	Reverse recovery time of the diode for output 1
145	IFM1			6.00	A	Maximum forward continuous current of the diode for output 1
146	PLOSS_DIODE1			3.97	W	Maximum diode power loss for output 1

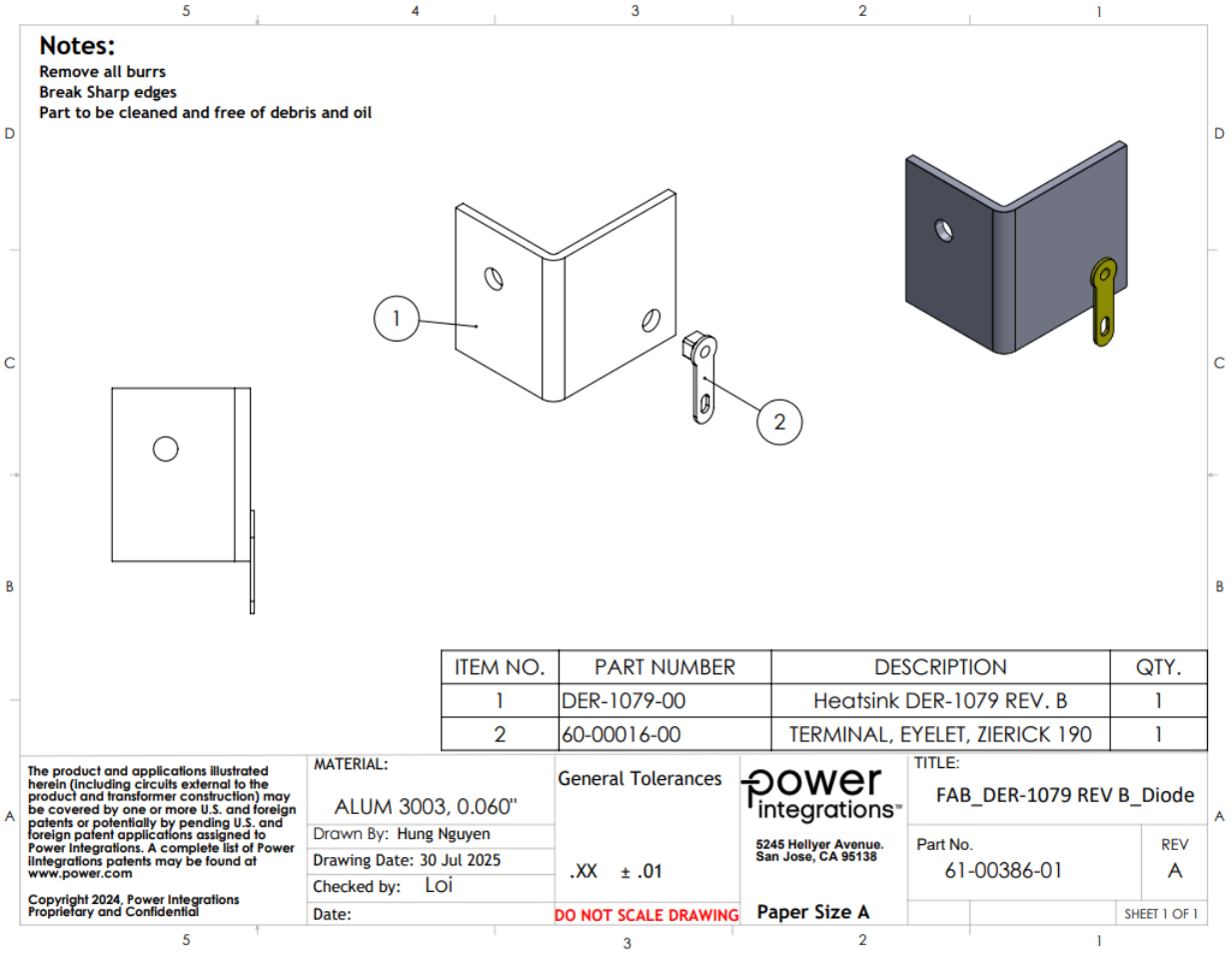
147						
148	OUTPUT 2					
149	VOUT2			0.00	V	Output 2 voltage
150	IOUT2			0.000	A	Output 2 current
151	POUT2			0.00	W	Output 2 power
152	VD2			N/A	V	Forward voltage drop of diode for output 2
153	NS2			N/A	turns	Number of turns for output 2
154	ISPEAK2			N/A	A	Instantaneous peak value of the secondary current for output 2
155	ISRMS2			N/A	A	Root mean squared value of the secondary current for output 2
156	ISRIPPLE2			N/A	A	Current ripple on the secondary waveform for output 2
157	PIV2			N/A	V	Computed peak inverse voltage stress on the diode for output 2
158	OUTPUT_RECTIFIER2	AUTO		N/A		Recommended diode for output 2.
159	PIV2_RATING			N/A	V	Peak inverse voltage rating on the diode for output 2
160	TRR2			N/A	ns	Reverse recovery time of the diode for output 2
161	IFM2			N/A	A	Maximum forward continuous current of the diode for output 2
162	PLOSS_DIODE2			N/A	W	Maximum diode power loss for output 2
163						
164	OUTPUT 3					
165	VOUT3			0.00	V	Output 3 voltage
166	IOUT3			0.000	A	Output 3 current
167	POUT3			0.00	W	Output 3 power
168	VD3			N/A	V	Forward voltage drop of diode for output 3
169	NS3			N/A	turns	Number of turns for output 3
170	ISPEAK3			N/A	A	Instantaneous peak value of the secondary current for output 3
171	ISRMS3			N/A	A	Root mean squared value of the secondary current for output 3
172	ISRIPPLE3			N/A	A	Current ripple on the secondary waveform for output 3
173	PIV3			N/A	V	Computed peak inverse voltage stress on the diode for output 3
174	OUTPUT_RECTIFIER3	AUTO		N/A		Recommended diode for output 3.
175	PIV3_RATING			N/A	V	Peak inverse voltage rating on the diode for output 3
176	TRR3			N/A	ns	Reverse recovery time of the diode for output 3
177	IFM3			N/A	A	Maximum forward continuous current of the diode for output 3
178	PLOSS_DIODE3			N/A	W	Maximum diode power loss for output 3
179						

180	PO_TOTAL			60.00	W	Total power of all outputs
181	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
182						
183						
184						
185	DESIGN EVALUATION - COMPENSATION AND STABILITY ANALYSIS					
186	COMPONENT SELECTION					
187	COUT	660.0		660.0	μF	Output capacitor
188	RESR_COUT	19.00		19.00	mΩ	ESR of output capacitor
189						
190	SHUNT REGULATOR NETWORK					
191	VREF_REG			1.25	V	Reference voltage of the feedback. To change this parameter, go to "SECONDARY COMPONENTS" section
192	IKA_MIN			0.10	mA	Minimum cathode current required on the shunt regulator. Use datasheet value
193	R_COMP	20.00		20.00	kΩ	Resistor connected from shunt regulator cathode to RFB_LOWER; in series with C_COMP
194	C_COMP	10.00		10.00	nF	Capacitor connected from shunt regulator cathode to RFB_LOWER; in series with R_COMP
197						
198	FEEDBACK NETWORK					
199	RFB_LOWER			10.00	kΩ	Lower feedback resistor
200	RFB_UPPER			182.00	kΩ	Upper feedback resistor
201	USE_RC_RFB_UPPER	YES		YES		Select "YES" to use series resistor-capacitor network across RFB_UPPER
202	RRFB_UPPER			20.00	kΩ	Resistor across RFB_UPPER; in series with CRFB_UPPER
203	CRFB_UPPER			10.00	nF	Capacitor across RFB_UPPER; in series with RRFB_UPPER
204						
205	OPTOCOUPLER NETWORK					
206	RREF_BIAS	1.00		1.00	kΩ	Resistor across optocoupler LED
207	C_OPTO	30.0		30.0	pF	Parasitic capacitance of the optocoupler primary side. Use datasheet value
208	VF_LED	1.20		1.20	V	LED maximum forward voltage. Use datasheet value
211	RLED_COMP	3010.0		3010.0	Ω	LED resistor. Resistor connected from VOUT to optocoupler
215						
216	OPERATING CONDITIONS (PIXls Charts)					
217	USER_VIN			115	V	Input voltage corner to be evaluated in the Bode plot in PIXls Charts tab
218	POUT			60.00	W	Output power to be evaluated

219	OUTPUT RIPPLE			2.00	%	Estimated output voltage percentage ripple seen by the compensation network. Decrease to add DC offset to the Bode Magnitude Plot and vice-versa
220	EFFICIENCY			0.86		ACDC efficiency estimate to be evaluated
221	Z FACTOR			0.60		Z-factor to be evaluated
222	FSWITCHING			84195	Hz	Maximum switching frequency at the output power to be evaluated
223	KP			0.89		Measure of continuous/discontinuous mode of operation
224	MODE_OPERATION			CCM		Mode of operation
225	DUTYCYCLE			0.446		Primary switch duty cycle
226	TIME_ON			5.30	µs	Primary switch on-time
227	TIME_OFF			6.58	µs	Primary switch off-time
228						
229	BODE STABILITY PARAMETERS (PIXls Charts)					
230	F_CO			2300	Hz	Crossover frequency
231	DC GAIN			38.0	dB	DC gain
232	PHASE_MARGIN			95.4	degrees	Phase margin
233	GAIN_MARGIN			17.1	dB	Gain margin
234						
235	INPUT VOLTAGE CORNER ANALYSIS - BODE PARAMETER RANGE					
236	VIN_1			115	V	Input voltage 1 to be evaluated in determining the range of Bode stability parameters (nominal voltage, by default)
237	VIN_2			230	V	Input voltage 2 to be evaluated in determining the range of Bode stability parameters (nominal voltage, by default)
238	F_CO_RANGE			2300 - 4590	Hz	Range of crossover frequency across the input voltage range defined
239	DC_GAIN_RANGE			38 - 41.5	dB	Range of DC gain across the input voltage range defined
240	PHASE_MARGIN_RANGE			95.4 - 100.9	degrees	Range of phase margin across the input voltage range defined
241	GAIN_MARGIN_RANGE			17.1 - 22.3	dB	Range of gain margin across the input voltage range defined
242						

9 Heatsink Assembly





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	DER-1079-00	Heatsink DER-1079 REV. B	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1

MATERIAL: ALUM 3003, 0.060"

Drawn By: Hung Nguyen

Drawing Date: 30 Jul 2025

Checked by: Loi

Date:

General Tolerances

.XX ± .01

DO NOT SCALE DRAWING

power integrations™

5245 Hellyer Avenue.
San Jose, CA 95138

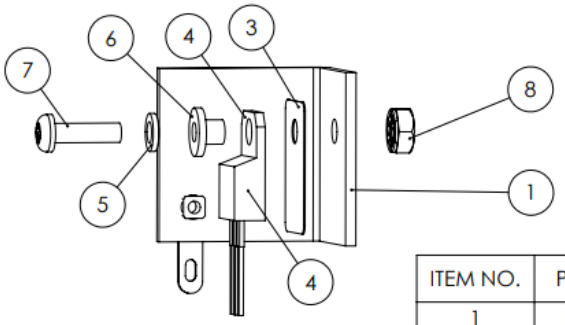
Paper Size A

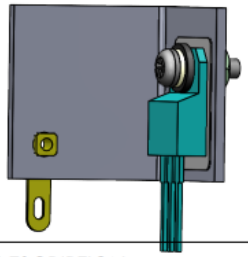
TITLE: FAB_DER-1079 REV B_Diode

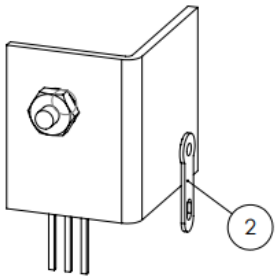
Part No. 61-00386-01

REV A

SHEET 1 OF 1







ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	DER-1079-00	Heatsink DER-1079 REV. B	1
2	60-00016-00	TERMINAL, EYELET, ZIERICK 190	1
3	66-00120-00	Wakefield_Thermal_Joint_Compound	1
4	15-01079-00	200 V, 10 A, Dual Schotkky, TO-220AB	1
5	75-00164-00	Flat Washer, #4	1
6	75-00154-00	Washer,Shoulder, #4, 0.125 Shoulder x 0.140 Dia, Polyphenylene Sulfide PPS	1
7	75-00003-00	#4-40 x .375 Machine Screw	1
8	75-00068-00	Nut, Hex, Kep 4-40, S ZN Cr3 plateing RoHS	1

MATERIAL: ALUM 3003, 0.060"

Drawn By: Hung D Nguyen

Date: 30 Jul 2025

Checked by: Loi

General Tolerances .XX ± .01

Do not Scale Drawing

power integrations

5245 Hellyer Avenue. San Jose, CA 95138

DER 1079 REV B Diode Heat Sink Assembly

PI Part NO. 61-00386-02

REV A

WEIGHT:

SHEET 1 OF 1

10 Performance Data

10.1 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line condition.

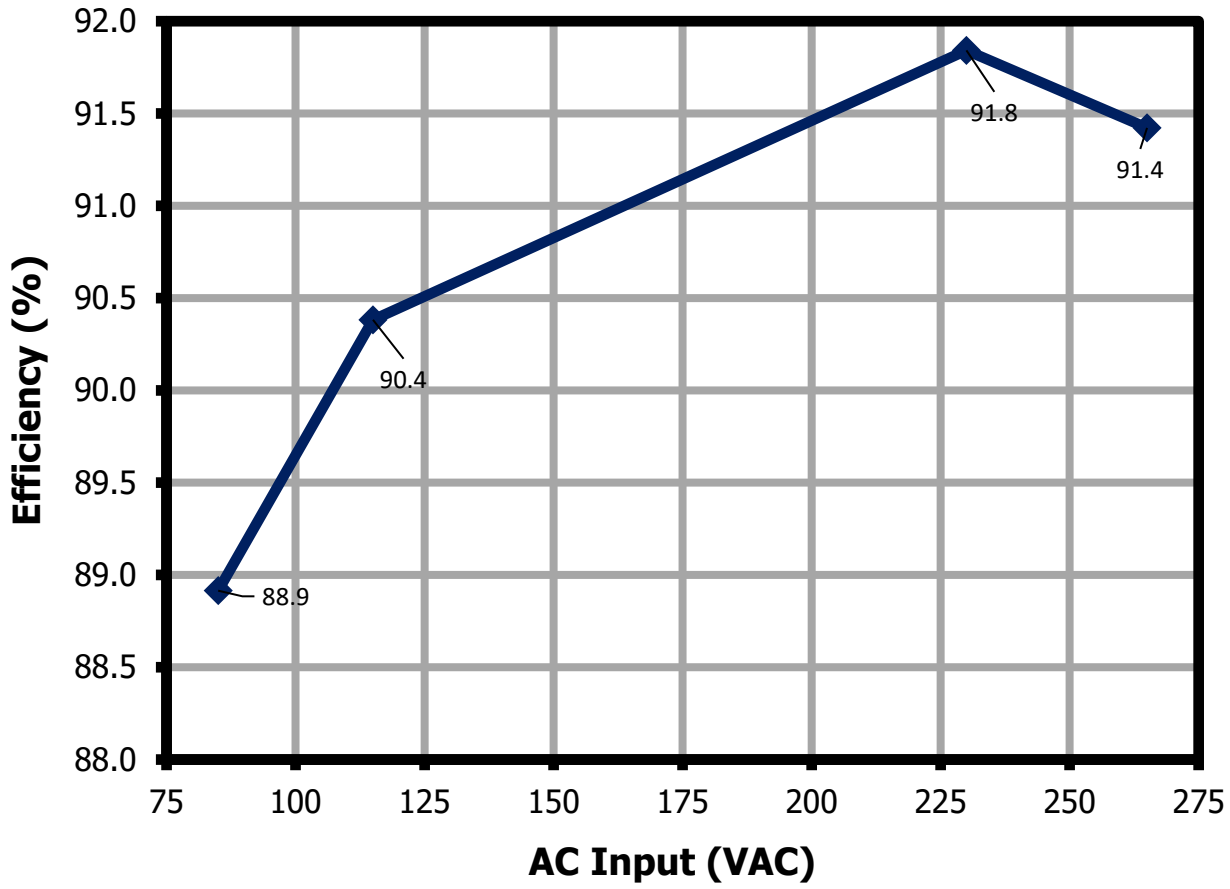


Figure 9 – Efficiency vs. Input Voltage.

VAC	Freq	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	Efficiency
(RMS)	(Hz)	(W)	(V)	(A)	(W)	(%)
85	60	66.8	23.8	2.49	59.4	88.9
115	60	65.7	23.8	2.49	59.4	90.4
230	50	64.5	23.8	2.49	59.3	91.8
265	50	64.7	23.7	2.49	59.2	91.4

10.2 Efficiency vs. Load

Test Condition: Soak for 15 minutes at full load for each line voltage, and 10 seconds for each load point.

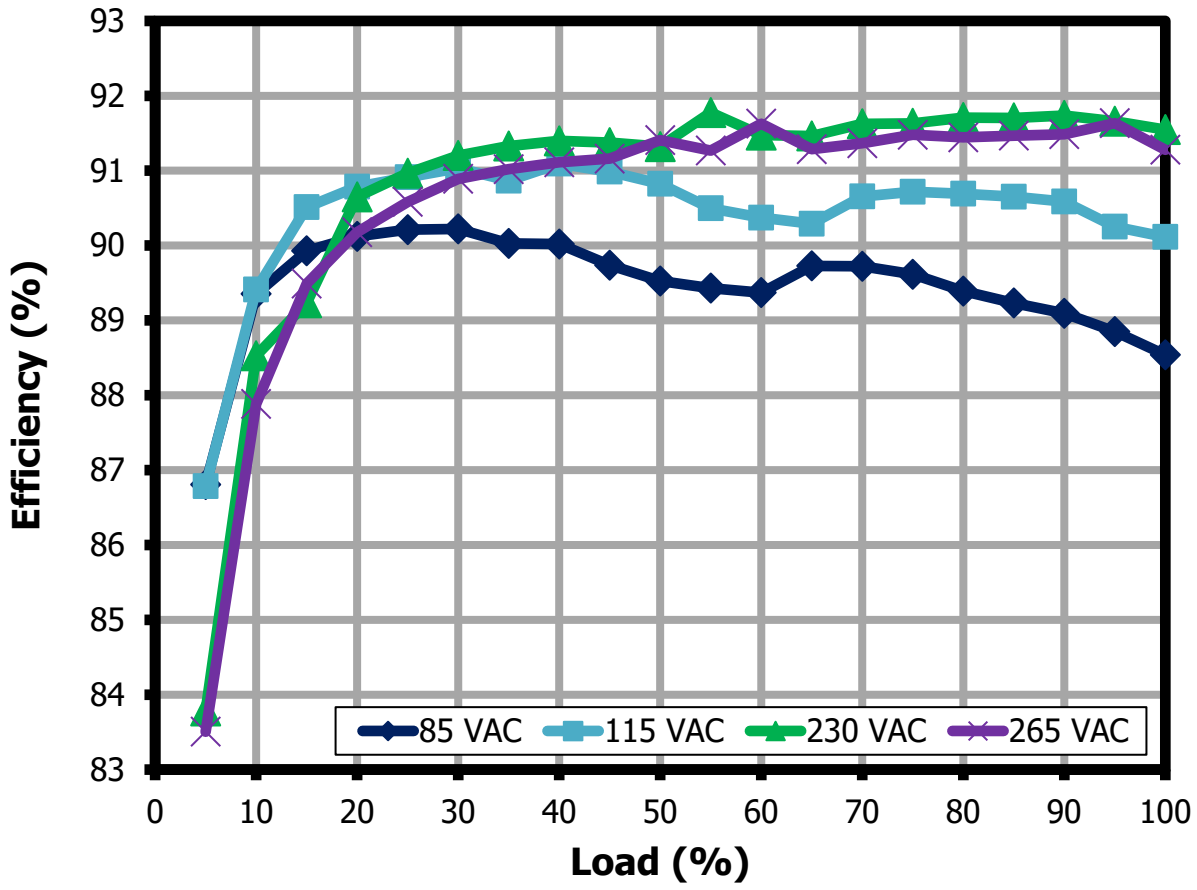


Figure 10 – Efficiency vs. Percentage Load.

10.2.1 Average and 10% Efficiency

10.2.1.1 Average Efficiency Standard

	Test	Average	Average	10% Load
Output Voltage (V)	Power (W)	DOE6 Limit (%)	CoC v5 Tier 2 (%)	CoC v5 Tier 2 (%)
24	60	88.0	89.0	79.0

10.2.1.2 Average and 10% Efficiency at 115 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	COC5T2 Limit
(A)	(W)	(V_{DC})	(A_{DC})	(W)	(%)	(%)	(%)
100%	66.2	23.9	2.49	59.7	90.2	**90.7**	89.0
75%	49.4	24.0	1.87	44.8	90.7		
50%	32.9	24.0	1.25	29.9	90.8		
25%	16.4	24.0	0.62	14.9	91.1		
10%	6.57	24.0	0.25	5.96	90.6	---	79.0

10.2.1.3 Average and 10% Efficiency at 230 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	COC5T2 Limit
(A)	(W)	(V_{DC})	(A_{DC})	(W)	(%)	(%)	(%)
100%	65.1	23.9	2.49	59.7	91.6	**91.5**	89.0
75%	48.9	23.9	1.87	44.8	91.6		
50%	32.6	24.0	1.25	29.9	91.7		
25%	16.3	24.0	0.62	14.9	91.2		
10%	6.6	24.0	0.25	5.95	89.6	---	79.0

10.2.2 No-Load Input Power

Test Condition: Soak for 15 minutes for each line voltage point with 5-minute integration time.

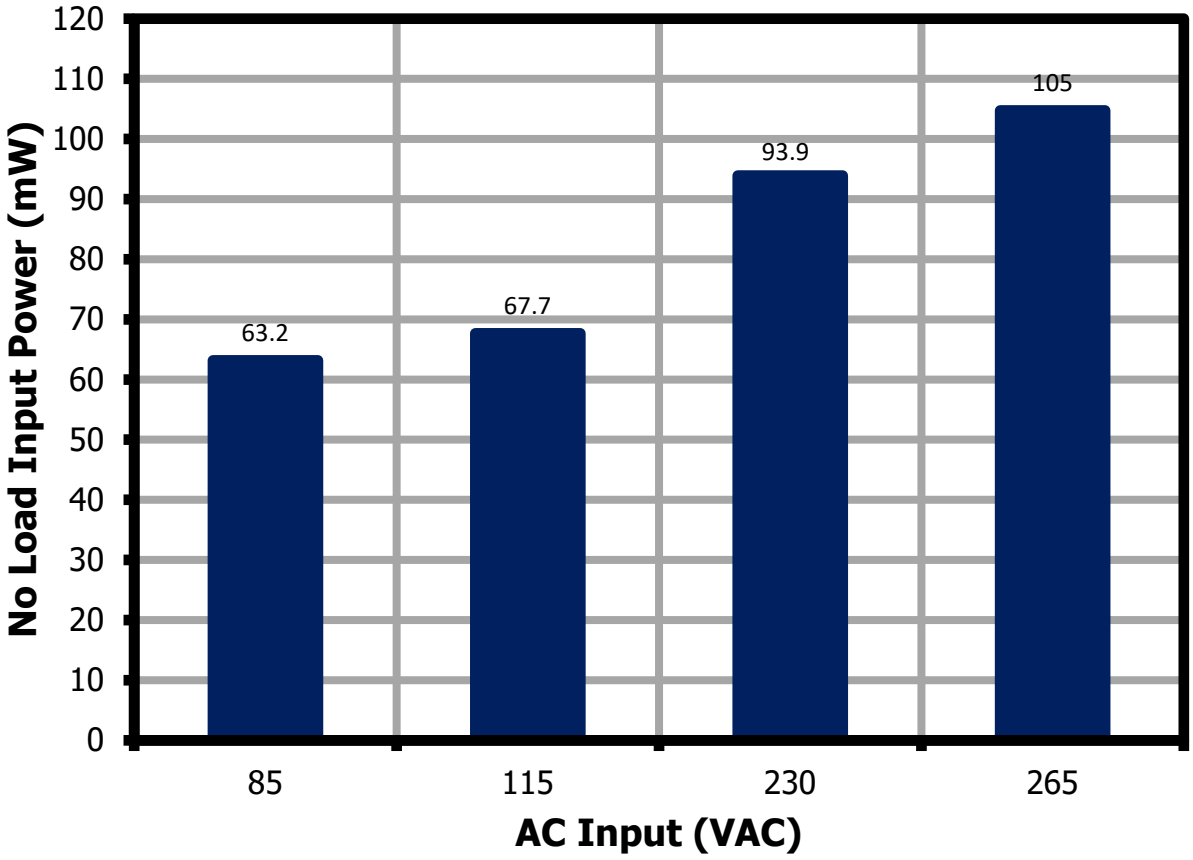


Figure 11 – No-Load Input Power vs. Line at Room Temperature.

VAC (RMS)	No Load P_{IN} (mW)
85	63.2
115	67.7
230	93.9
265	105

10.2.3 Line Regulation

Test Condition: Soak for 15 minutes for each line voltage point.

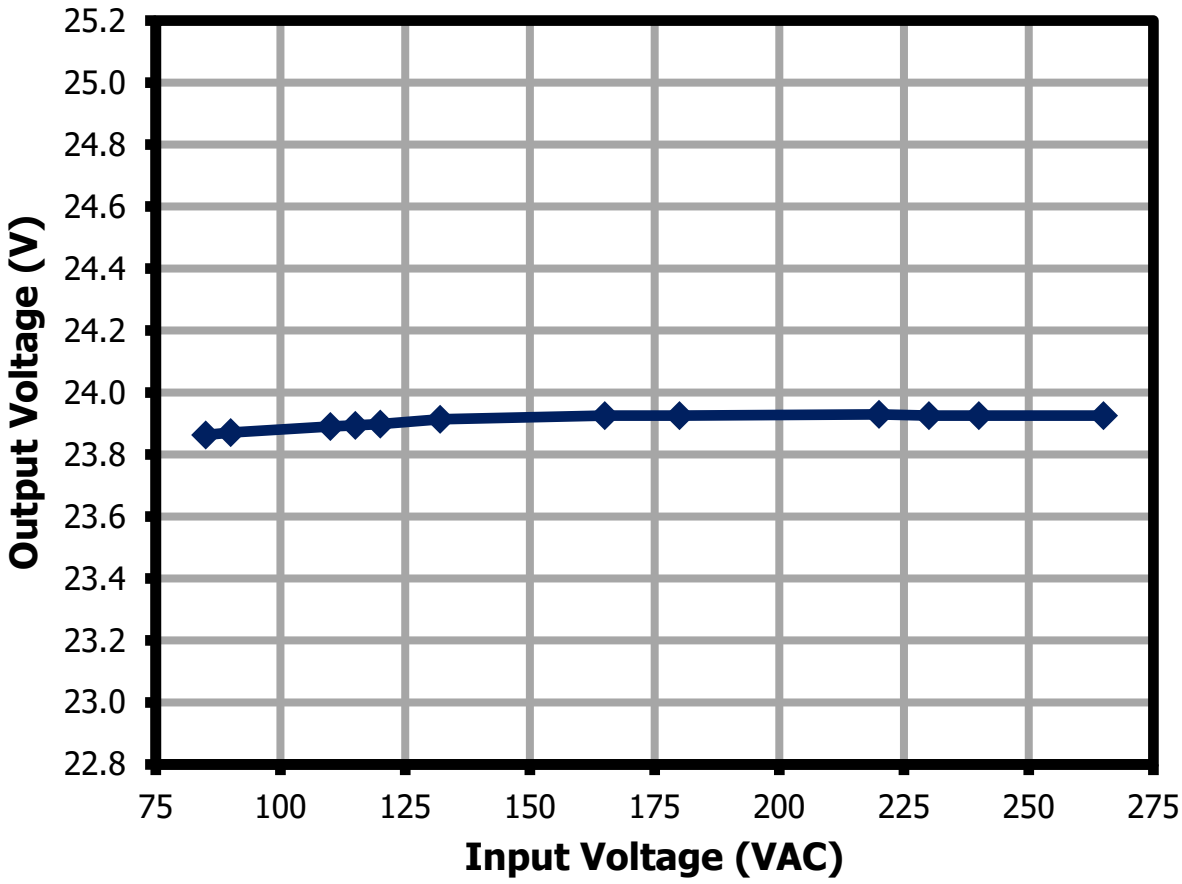


Figure 12 – Output Voltage vs. Line Voltage.

10.2.4 Load Regulation

Test Condition: Soak for 15 minutes each line voltage point at full load, and 10 seconds for each load.

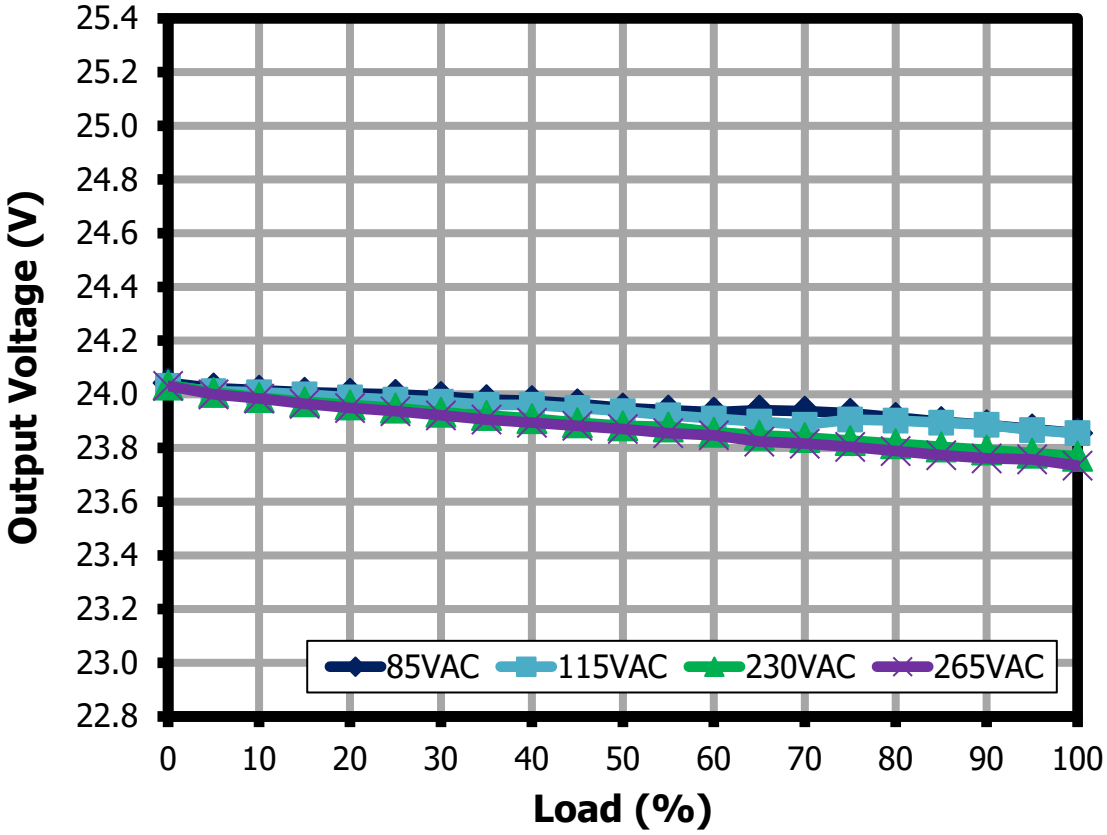


Figure 13 – Output Voltage vs. Percent Load.

10.2.5 Standby Efficiency

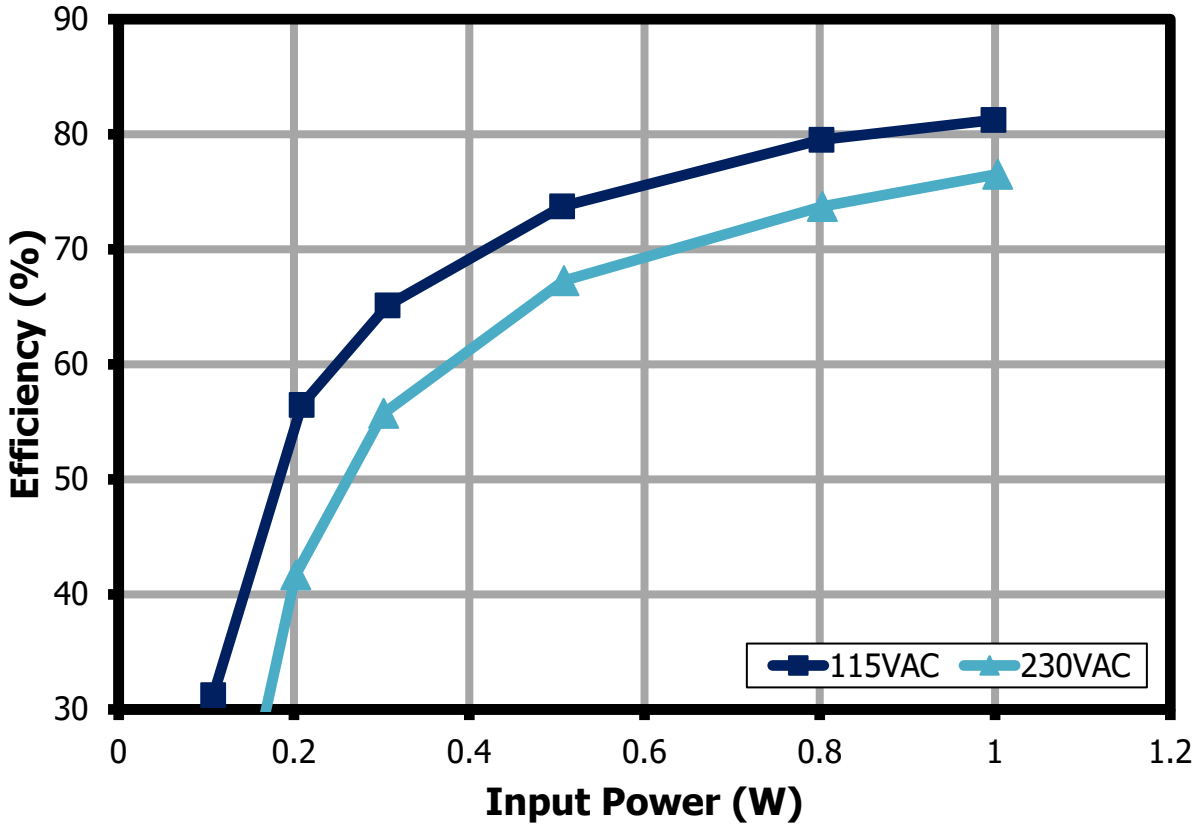


Figure 14 – Efficiency vs. Input Power.

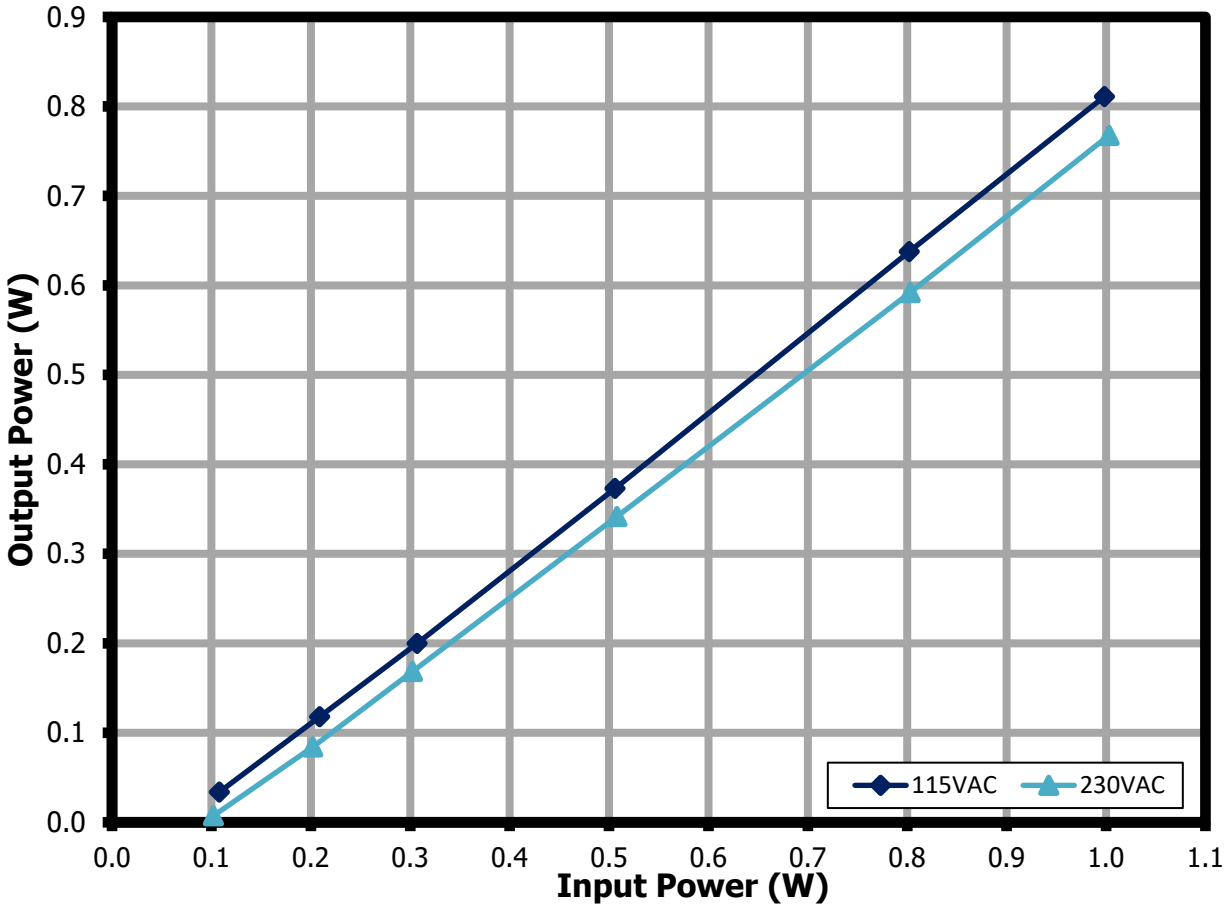


Figure 15 – Output Power vs. Input Power.

11 Waveforms

11.1 Load Transient Response

Test Condition: Dynamic load frequency = 10 Hz, Duty cycle = 50%
Slew Rate = 0.4 A / µs

11.1.1 0% to 100% Output Load Transient Condition

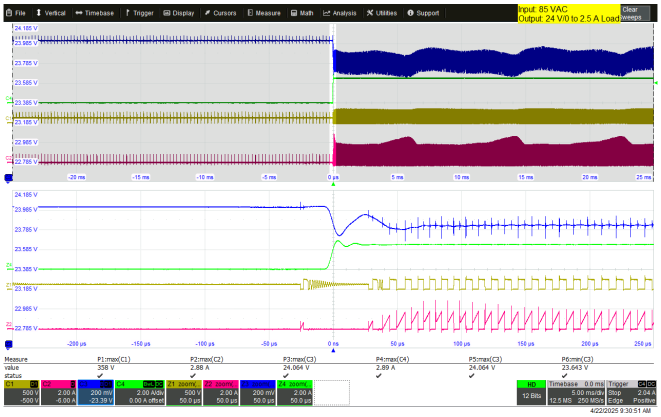


Figure 16 – 85 VAC, 60 Hz. Io = 0 – 2.5 A (0-100%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.6 V

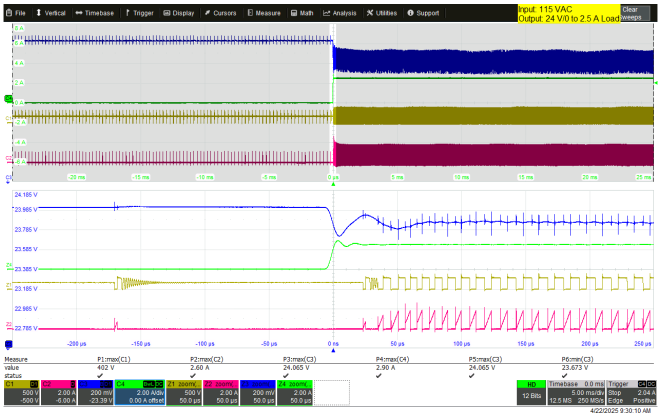


Figure 17 – 115 VAC, 60 Hz. Io = 0 – 2.5 A (0-100%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.7 V

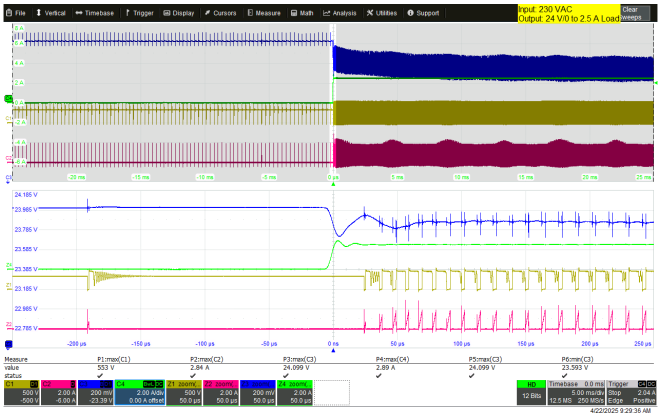


Figure 18 – 230 VAC, 50 Hz. Io = 0 – 2.5 A (0-100%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.6 V

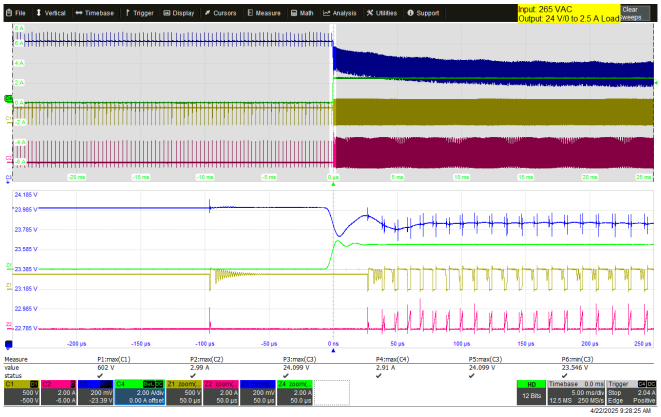


Figure 19 – 265 VAC, 50 Hz. Io = 0 – 2.5 A (0-100%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.5 V

11.1.2 100% to 0% Output Load Transient Condition

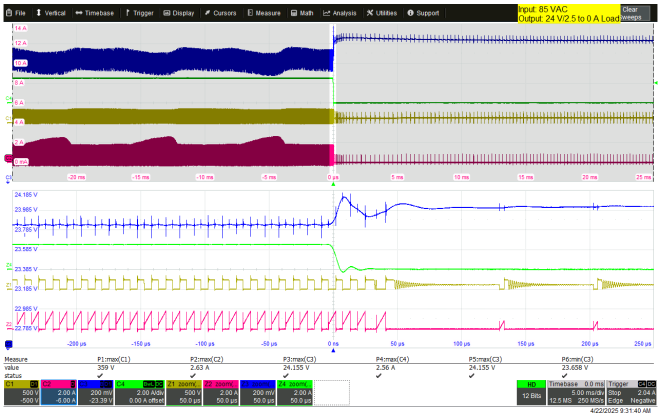


Figure 20 – 85 VAC, 60 Hz. Io = 0 – 2.5 A (100-0%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.2 V
Output Voltage, min = 23.7 V

Figure 21 – 115 VAC, 60 Hz. Io = 0 – 2.5 A (100-0%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.7 V

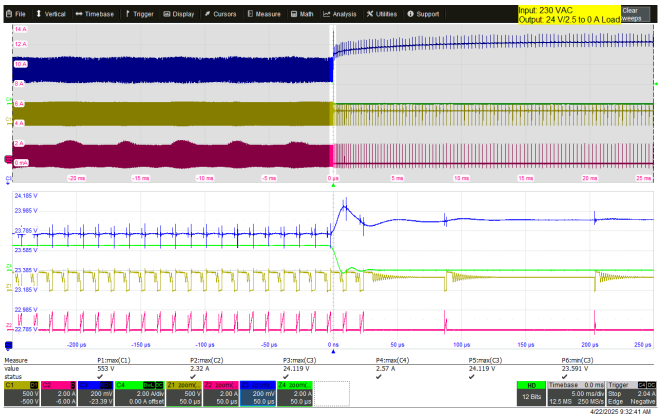


Figure 22 – 230 VAC, 50 Hz. Io = 0 – 2.5 A (100-0%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.6 V

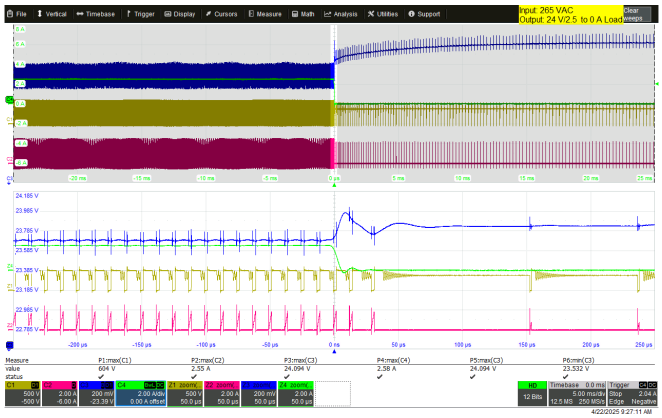


Figure 23 – 265 VAC, 50 Hz. Io = 0 – 2.5 A (100-0%) load step.
CH1: TOP7074K_V_{DS}, 500 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 2 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: I_{OUT}, 2 A / div., 5 ms / div.
Zoom: 50 µs / div.
Output Voltage, max = 24.1 V
Output Voltage, min = 23.5 V

11.2 Output Start-up

11.2.1 Full Load CC Mode

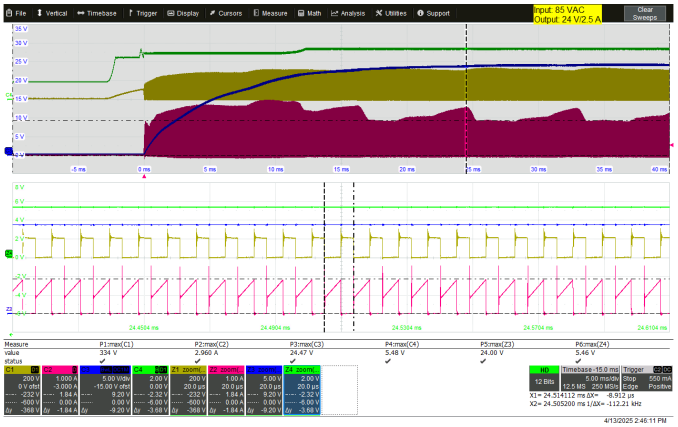


Figure 24 – 85 VAC, 60 Hz. 24 V / 2.5 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.5 V
Start-up time = 24.5 ms

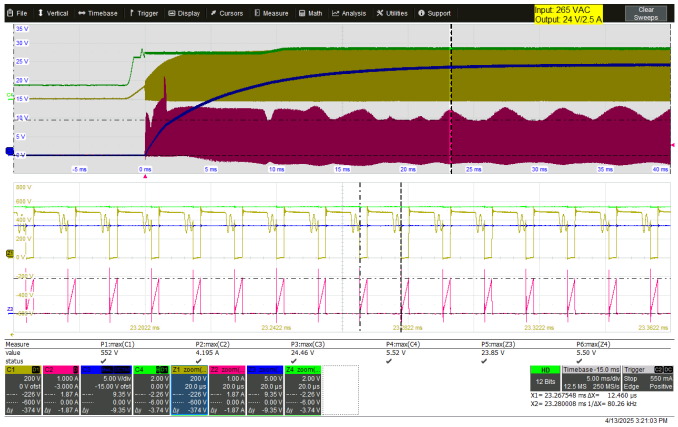


Figure 25 – 265 VAC, 50 Hz. 24 V / 2.5 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.5 V
Start-up time = 22.2 ms

11.2.2 Full Load CR Mode

Figure 26 – 85 VAC, 60 Hz. 24 V / 2.5 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 10 ms / div.
CH3: V_{OUT}, 5 V / div., 10 ms / div.
CH4: V_{BP}, 2 V / div.,10 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.3 V
Start-up time = 25 ms

Figure 27 – 265 VAC, 50 Hz. 24 V / 2.5 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 10 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 10 ms / div.
CH3: V_{OUT}, 5 V / div., 10 ms / div.
CH4: V_{BP}, 2 V / div.,10 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.1 V
Start-up time = 27 ms

11.2.3 No Load

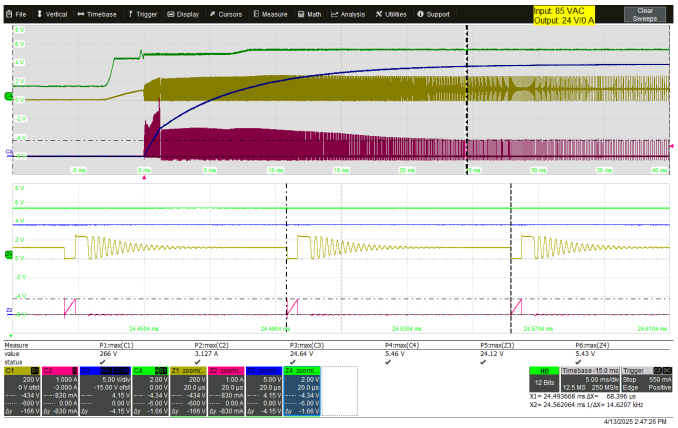


Figure 28 – 85 VAC, 60 Hz. 24 V / 0 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.6 V
Start-up time = 24.6 ms

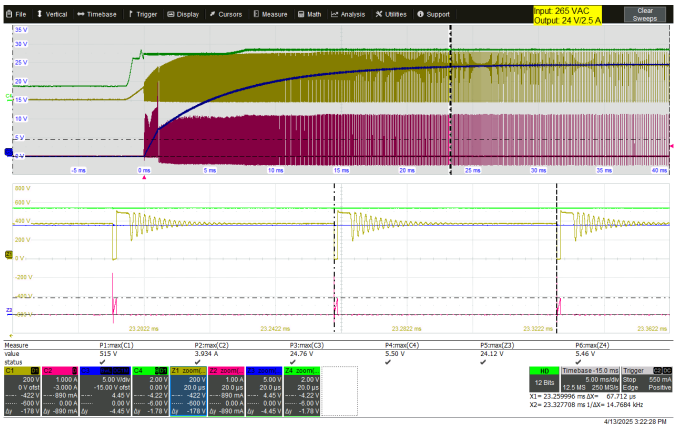


Figure 29 – 265 VAC, 50 Hz. 24 V / 0 A.
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
Output Voltage, max = 24.8 V
Start-up time = 23.3 ms

11.3 Switching Waveforms

11.3.1 Primary Drain Voltage and Current at Normal Operation

11.3.1.1 Full Load

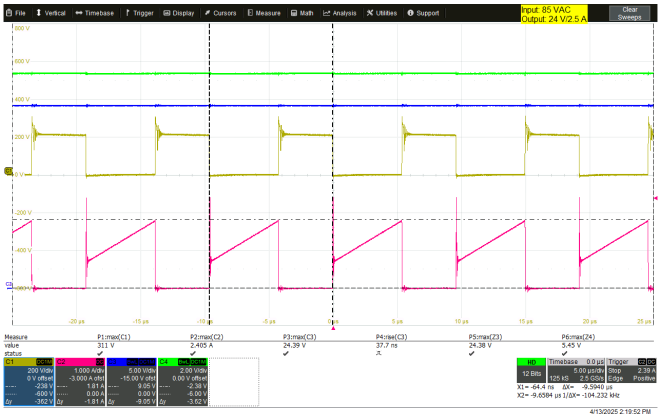


Figure 30 – 85 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 µs / div.
CH3: V_{OUT}, 5 V / div., 5 µs / div.
CH4: V_{BP}, 2 V / div., 5 µs / div.
TOP7074K Drain voltage, max = 331 V
TOP7074K Drain current, max = 2.41 A
ILIM = 1.81 A, F_{SW}= 104 kHz

Figure 31 – 265 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 µs / div.
CH3: V_{OUT}, 5 V / div., 5 µs / div.
CH4: V_{BP}, 2 V / div., 5 µs / div.
TOP7074K Drain voltage, max = 552 V
TOP7074K Drain current, max = 2.56 A
ILIM = 1.85 A, F_{SW} = 81 kHz

11.3.1.2 No Load

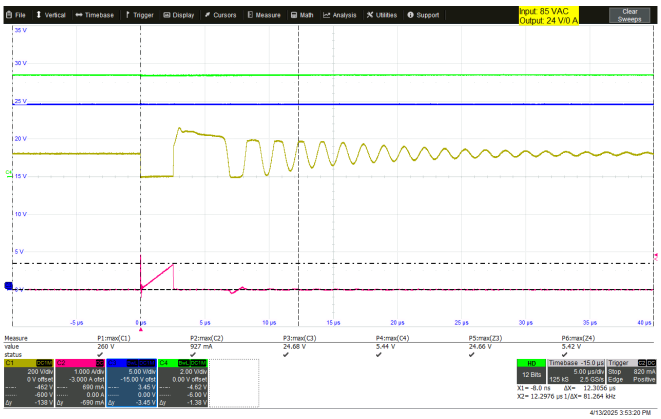


Figure 32 – 85 VAC, Io = 0 A (No-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 µs / div.
CH3: V_{OUT}, 5 V / div., 5 µs / div.
CH4: V_{BP}, 2 V / div., 5 µs / div.
TOP7074K Drain voltage, max = 260 V
TOP7074K Drain current, max = 0.93 A
ILIM = 0.69 A

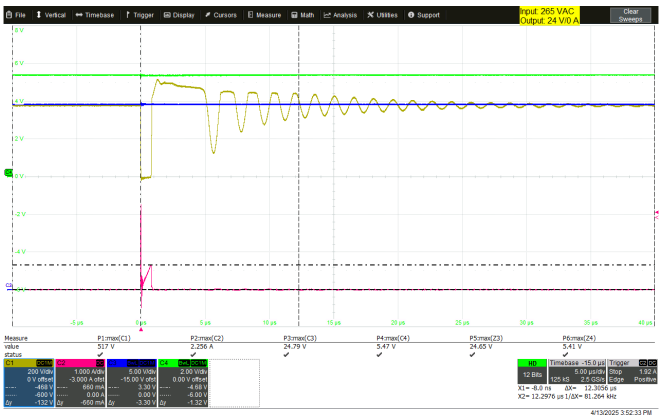


Figure 33 – 265 VAC, Io = 0 A (No-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 µs / div.
CH3: V_{OUT}, 5 V / div., 5 µs / div.
CH4: V_{BP}, 2 V / div., 5 µs / div.
TOP7074K Drain voltage, max = 517 V
TOP7074K Drain current, max = 2.26 A
ILIM = 0.66 A

11.3.2 Primary Drain Voltage and Current at Start-up Operation

11.3.2.1 Full Load

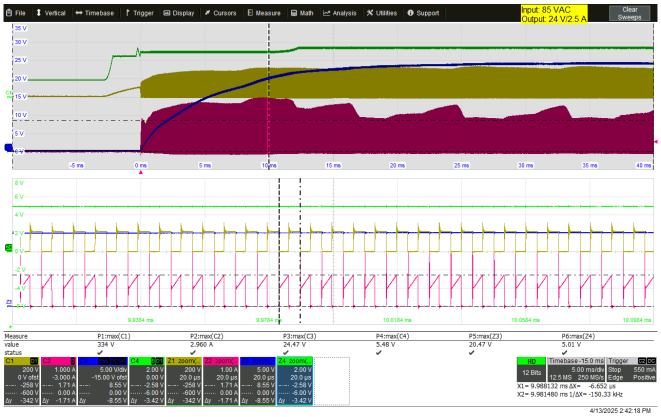


Figure 34 – 85 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
TOP7074K Drain voltage, max = 334 V
TOP7074K Drain current, max = 2.96 A

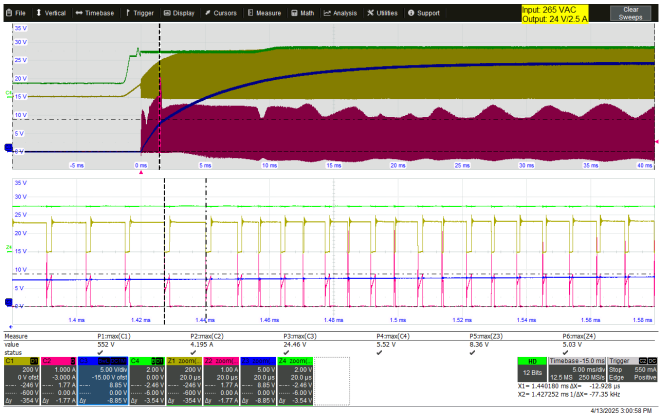


Figure 35 – 265 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
TOP7074K Drain voltage, max = 552 V
TOP7074K Drain current, max = 4.2 A

11.3.2.2 No Load

Figure 36 – 85 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
TOP7074K Drain voltage, max = 266 V
TOP7074K Drain current, max = 3.13 A

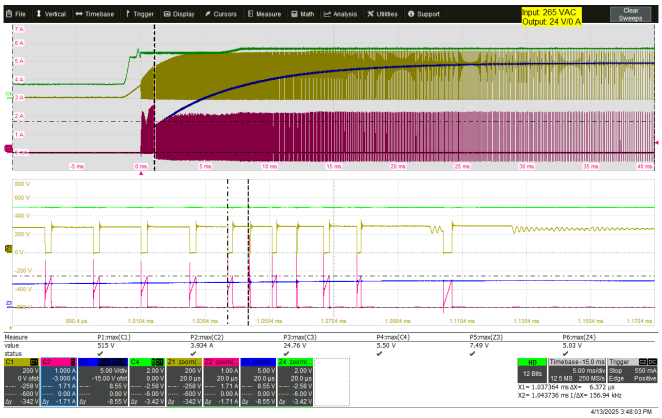


Figure 37 – 265 VAC, Io = 2.5 A (Full-Load).
CH1: TOP7074K_V_{DS}, 200 V / div., 5 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 5 ms / div.
CH3: V_{OUT}, 5 V / div., 5 ms / div.
CH4: V_{BP}, 2 V / div., 5 ms / div.
Zoom: 20 µs / div.
TOP7074K Drain voltage, max = 515 V
TOP7074K Drain current, max = 3.93 A

11.3.3 Freewheeling Diode Voltage at Normal Operation

11.3.3.1 Full Load

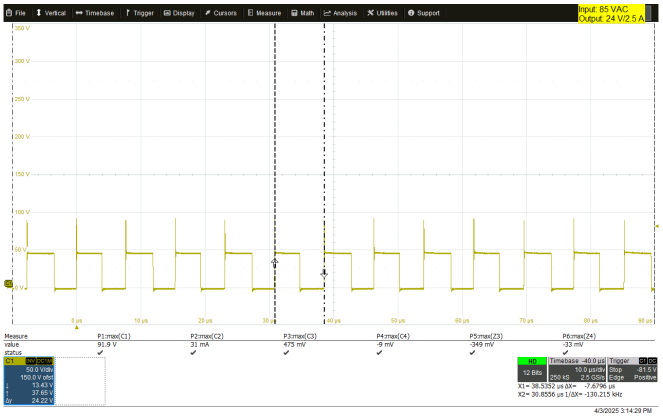


Figure 38 – 85 VAC, Io = 2.5 A (Full-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 10 µs/div.
OUTPUT DIODE voltage, max = 91.9 V

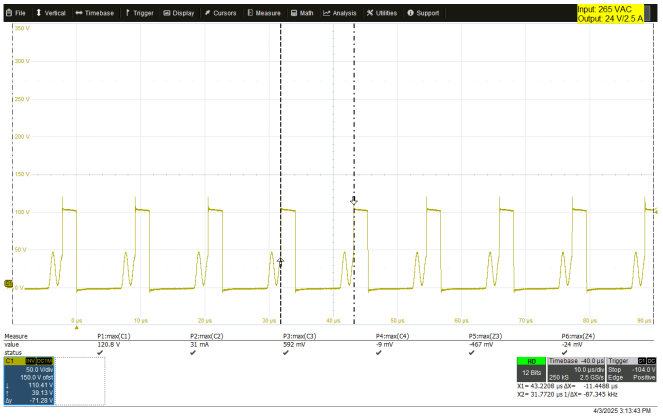


Figure 39 – 265 VAC, Io = 2.5 A (Full-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 10 µs/div.
OUTPUT DIODE voltage, max = 121 V

11.3.3.2 No Load

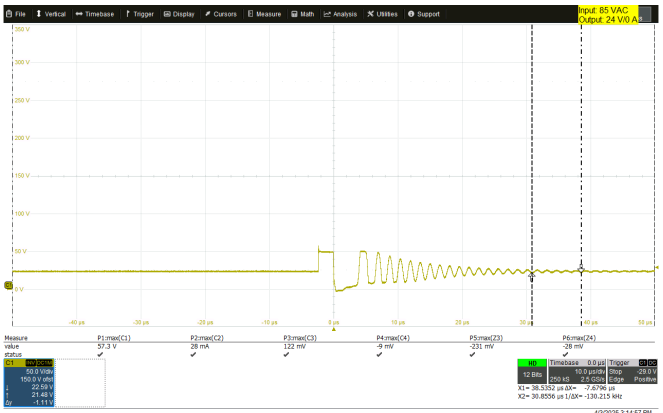


Figure 40 – 85 VAC, Io = 0 A (No-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 10 µs/div.
OUTPUT DIODE voltage, max = 91.9 V

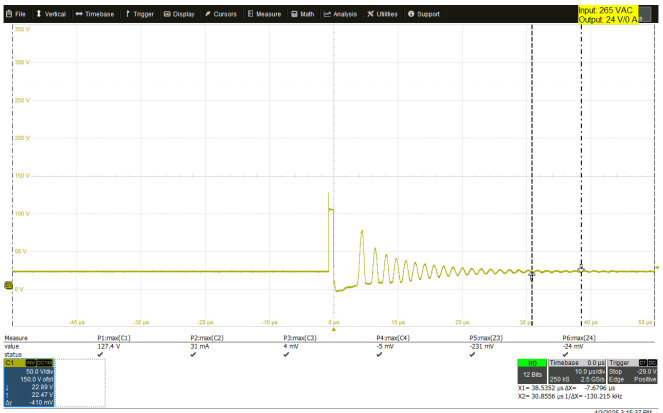


Figure 41 – 265 VAC, Io = 0 A (No-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 10 µs/div.
OUTPUT DIODE voltage, max = 127 V

11.3.4 Freewheeling Diode Voltage at Start-Up

11.3.4.1 Full Load

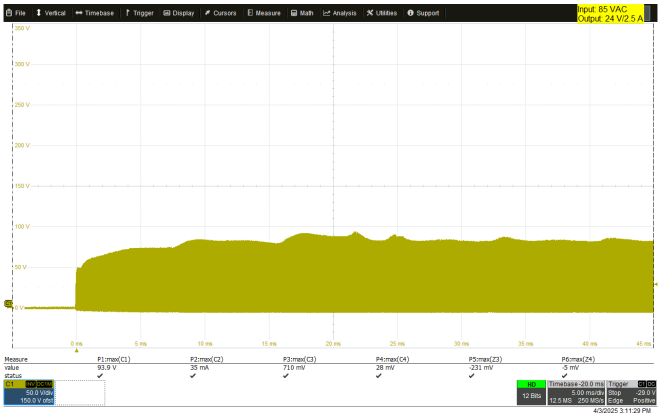


Figure 42 – 85 VAC, Io = 2.5 A (Full-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 5 ms/div.
OUTPUT DIODE voltage, max = 93.9 V

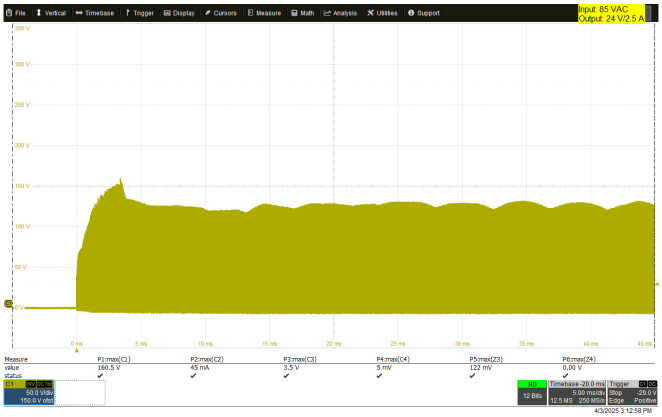


Figure 43 – 265 VAC, Io = 2.5 A (Full-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 5 ms/div.
OUTPUT DIODE voltage, max = 161 V

11.3.4.2 No Load

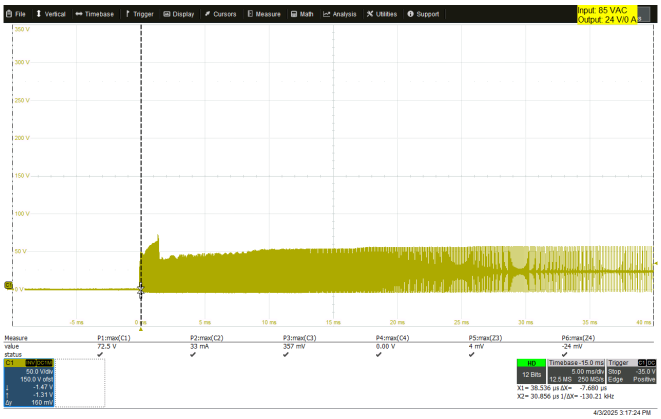


Figure 44 – 85 VAC, Io = 0 A (No-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 5 ms/div.
OUTPUT DIODE voltage, max = 72.5 V

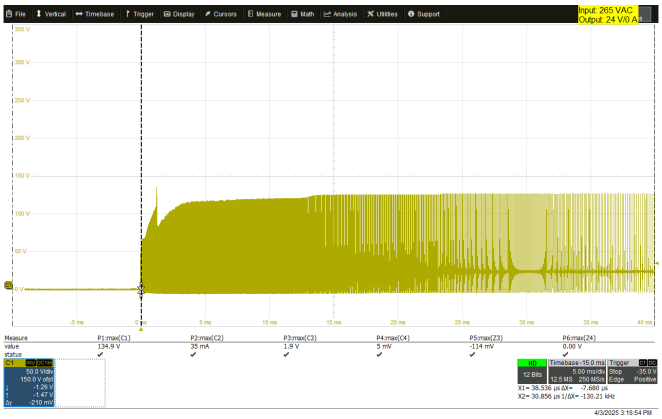


Figure 45 – 265 VAC, Io = 0 A (No-Load).
CH 1: OUTPUT RECTIFIER VOLTAGE: 50 V/div., 5 ms/div.
OUTPUT DIODE voltage, max = 135 V

11.4 Output Voltage Ripple

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in figures 46 and 47 (below).

The 4987BA probe adapter is affixed with two capacitors connected in parallel across the probe tip. The capacitors include one 0.1 μF / 50 V ceramic type and one 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic capacitor is polarized, so proper polarity across DC outputs must be maintained during measurements (see below).

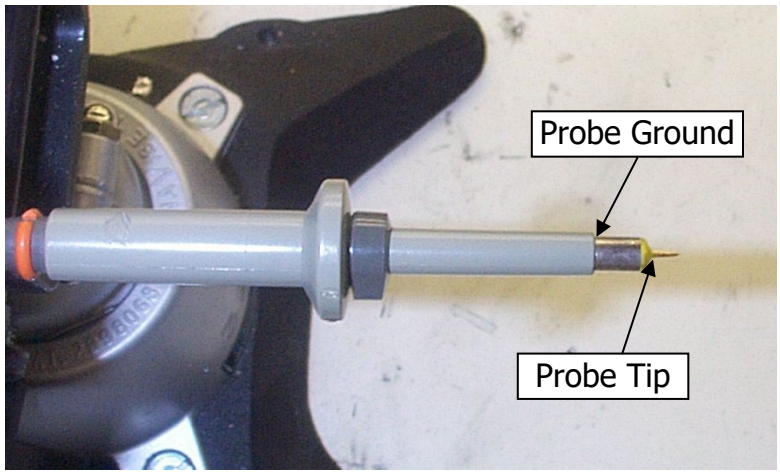


Figure 46 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

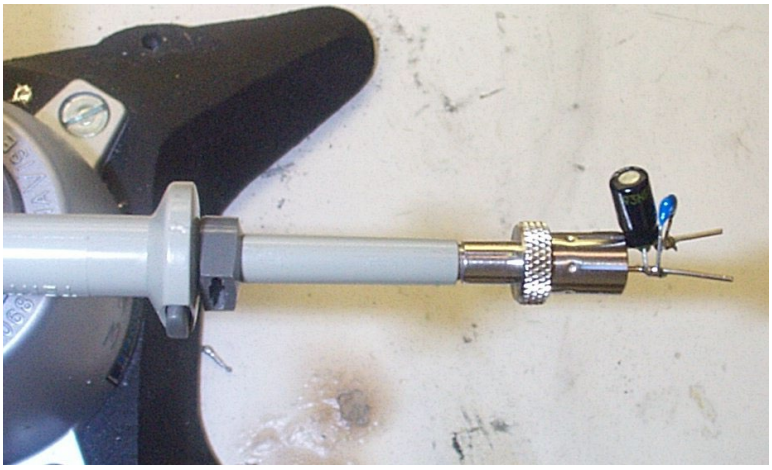


Figure 47 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.4.2 Measurement Results

Note: All ripple measurements were taken at PCB end.

11.4.2.1 100% Load Condition

85 VAC – 24 V/2.5 A

Figure 48 – 85 VAC, 60 Hz. 24 V / 2.5 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 67 mV_{PK-PK}

115 VAC – 24 V/2.5 A

Figure 49 – 115 VAC, 60 Hz. 24 V / 2.5 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 47 mV_{PK-PK}

230 VAC – 24 V/2.5 A

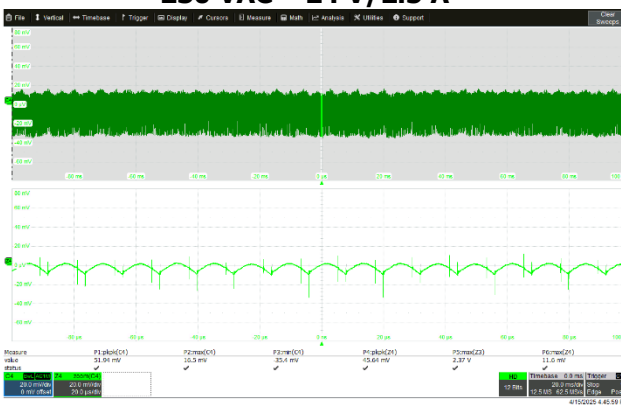


Figure 50 – 230 VAC, 50 Hz. 24 V / 2.5 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 52 mV_{PK-PK}

265 VAC – 24 V/2.5 A

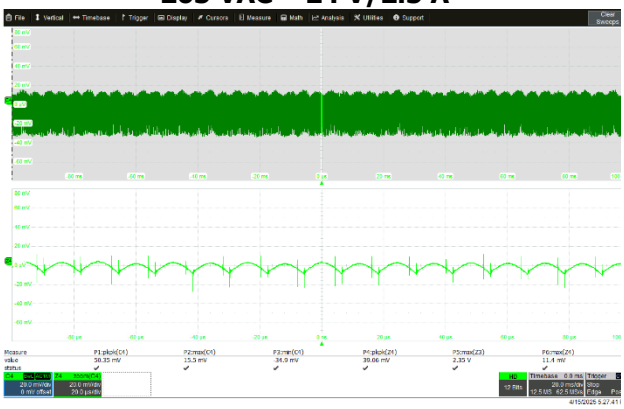


Figure 51 – 265 VAC, 50 Hz. 24 V / 2.5 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 50 mV_{PK-PK}

11.4.2.2 75% Load Condition

85 VAC – 24 V/1.88 A

Figure 52 – 85 VAC, 60 Hz. 24 V / 1.88 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 48 mV_{PK-PK}

115 VAC – 24 V/1.88 A

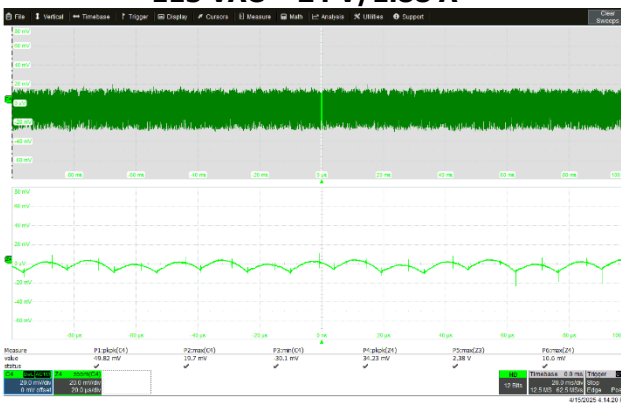


Figure 53 – 115 VAC, 60 Hz. 24 V / 1.88 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 49 mV_{PK-PK}

230 VAC – 24 V/1.88 A

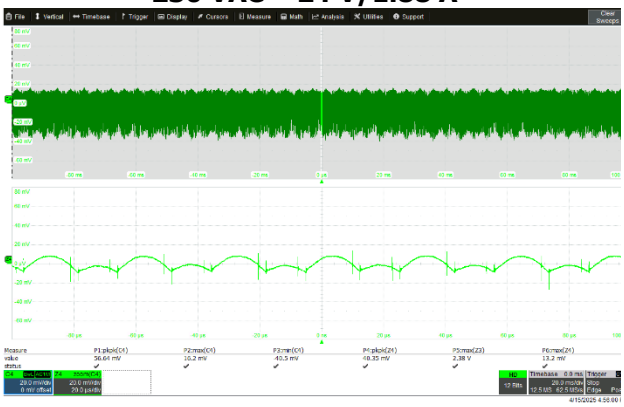


Figure 54 – 230 VAC, 50 Hz. 24 V / 1.88 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 56 mV_{PK-PK}

265 VAC – 24 V/1.88 A

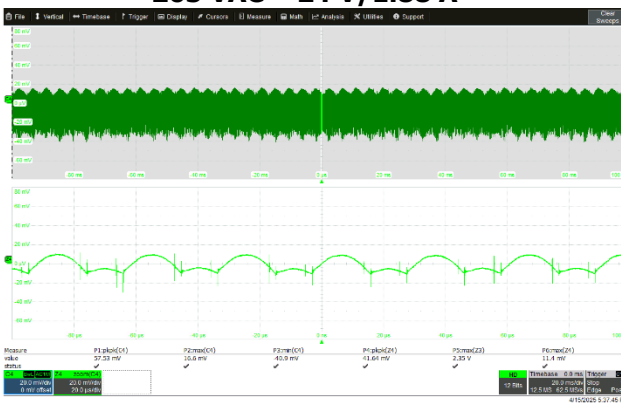


Figure 55 – 265 VAC, 50 Hz. 24 V / 1.88 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 57 mV_{PK-PK}

11.4.2.3 50% Load Condition

85 VAC – 24 V/1.25 A

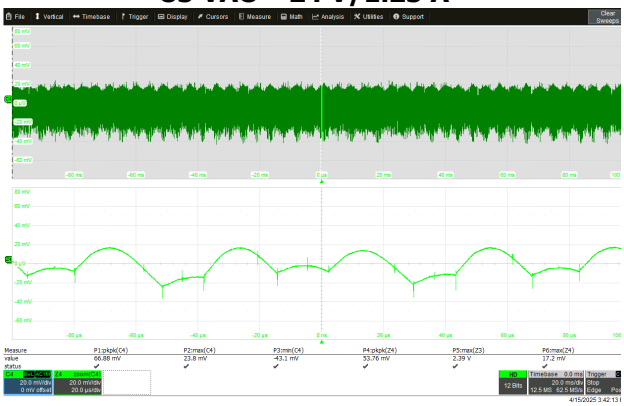


Figure 56 – 85 VAC, 60 Hz. 24 V / 1.25 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 67 mV_{PK-PK}

115 VAC – 24 V/1.25 A

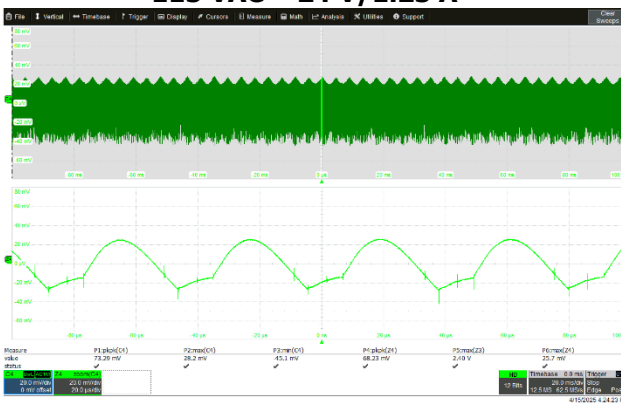


Figure 57 – 115 VAC, 60 Hz. 24 V / 1.25 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 73 mV_{PK-PK}

230 VAC – 24 V/1.25 A

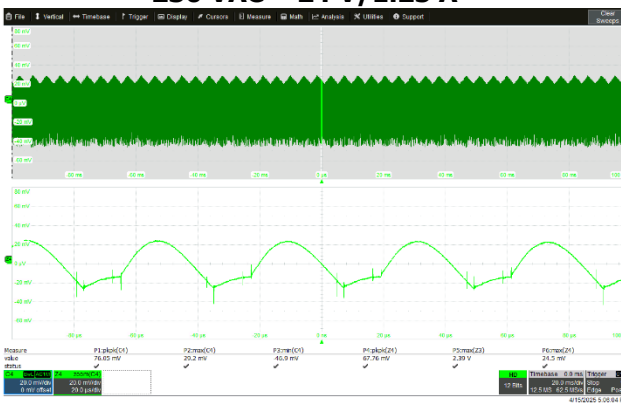


Figure 58 – 230 VAC, 50 Hz. 24 V / 1.25 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 76 mV_{PK-PK}

265 VAC – 24 V/1.25 A

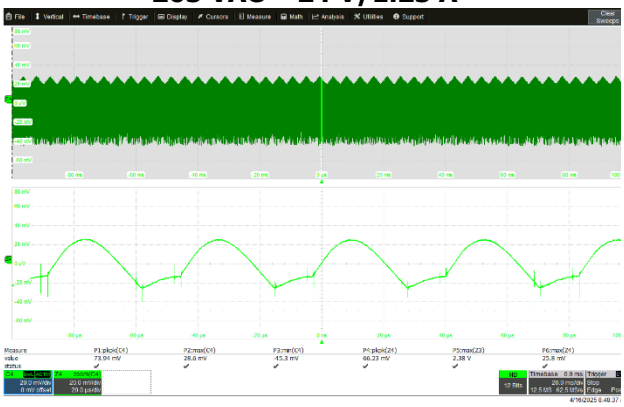


Figure 59 – 265 VAC, 50 Hz. 24 V / 1.25 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 67 mV_{PK-PK}

11.4.2.4 25% Load Condition

85 VAC – 24 V/0.63 A

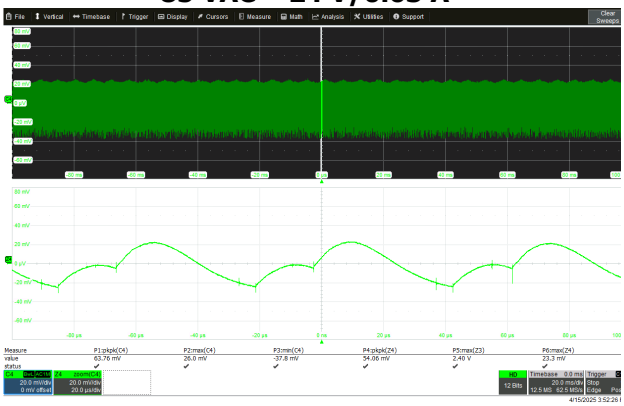


Figure 60 – 85 VAC, 60 Hz. 24 V / 0.63 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 63 mV_{PK-PK}

115 VAC – 24 V/0.63 A

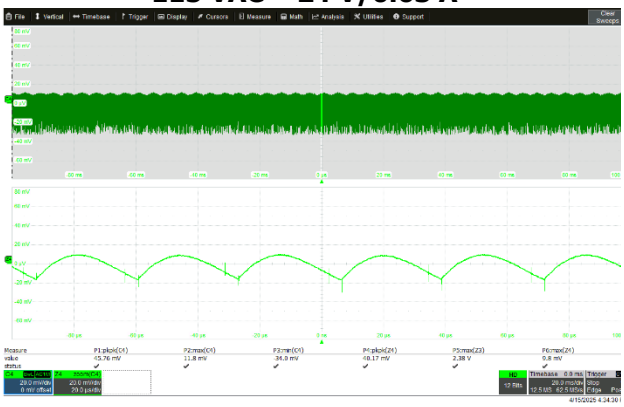


Figure 61 – 115 VAC, 60 Hz. 24 V / 0.63 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 45 mV_{PK-PK}

230 VAC – 24 V/0.63 A

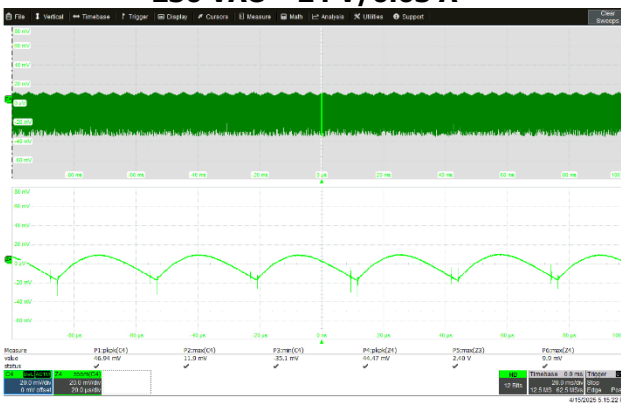


Figure 62 – 230 VAC, 50 Hz. 24 V / 0.63 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 47 mV_{PK-PK}

265 VAC – 24 V/0.63 A

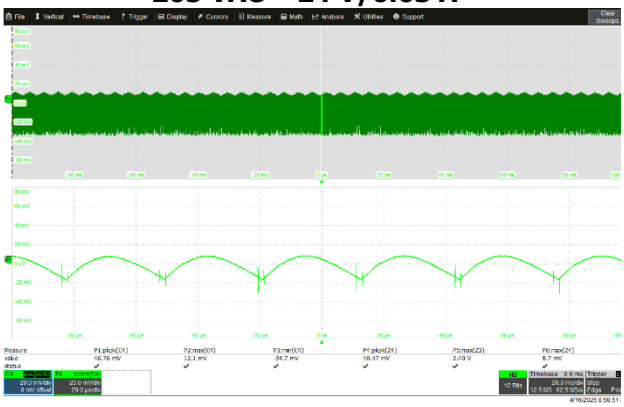


Figure 63 – 265 VAC, 50 Hz. 24 V / 0.63 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 46 mV_{PK-PK}

11.4.2.5 0% Load Condition

85 VAC – 24 V/0 A

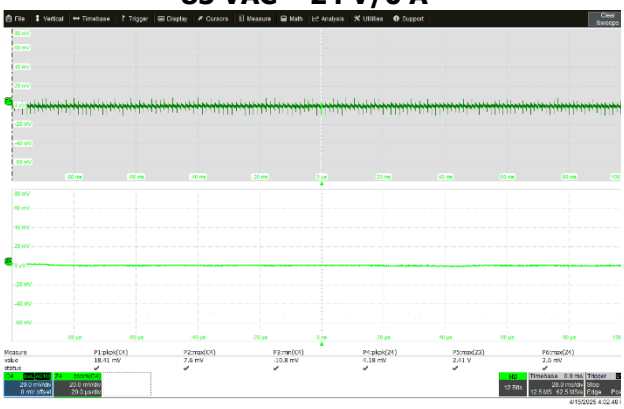


Figure 64 – 85 VAC, 60 Hz. 24 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 18 mV_{PK-PK}

115 VAC – 24 V/0 A

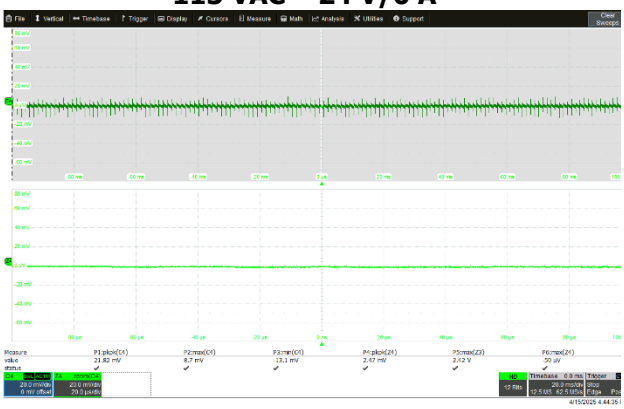


Figure 65 – 115 VAC, 60 Hz. 24 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 21 mV_{PK-PK}

230 VAC – 24 V/0 A

Figure 66 – 230 VAC, 50 Hz. 24 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 33 mV_{PK-PK}

265 VAC – 24 V/0 A

Figure 67 – 265 VAC, 50 Hz. 24 V / 0 A.
CH1: $V_{OUT(pk-pk)}$, 20 mV / div, 20 ms / div.
Zoom: 20 µs / div.
V_{OUT} Ripple = 33 mV_{PK-PK}

11.4.3 Output Ripple Voltage Graph

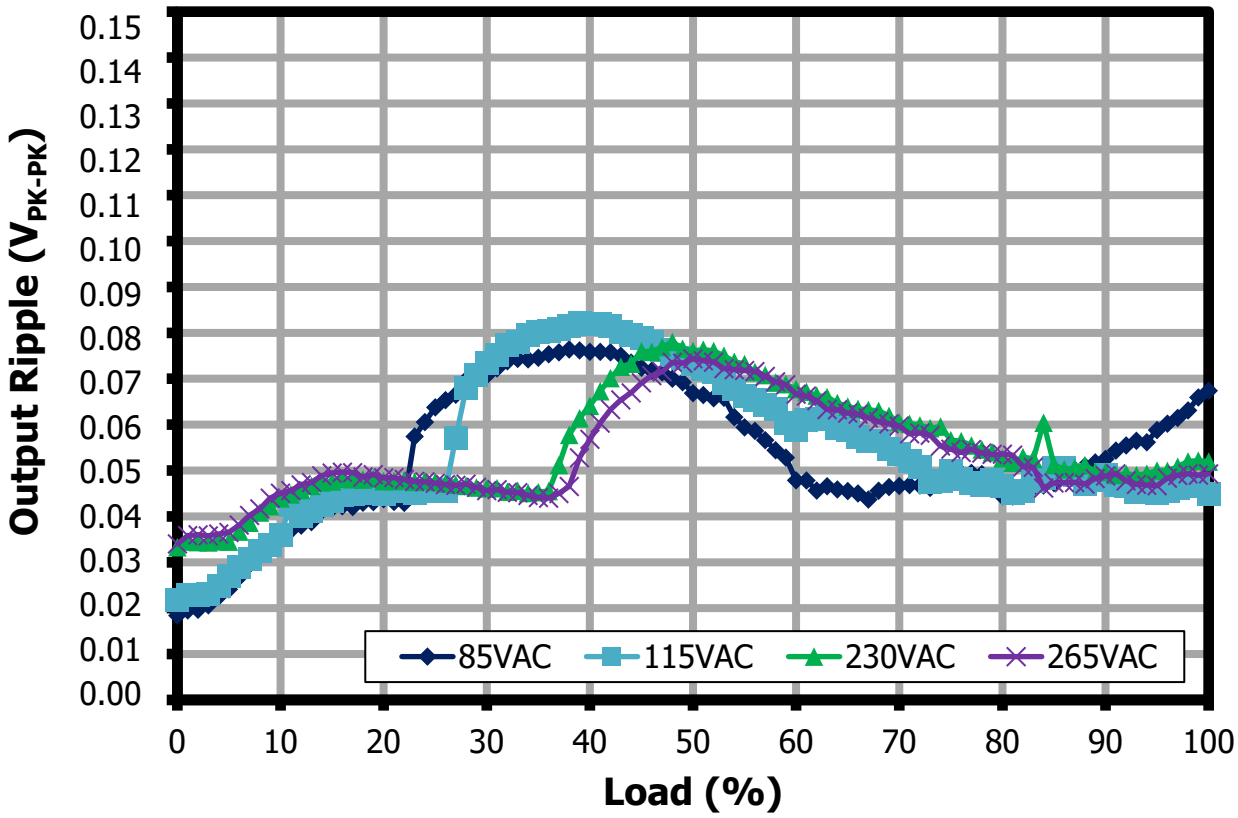


Figure 68 – Voltage Ripple (Measured at PCB End and at Room Temperature).

12 Thermal Performance

12.1 Thermal Performance at Room Temperature

12.1.1 85 VAC Full Load at Room Ambient

Test result after 2 hours running continuously inside an enclosure at 85 VAC full load using FLIR thermal camera to measure component temperatures.

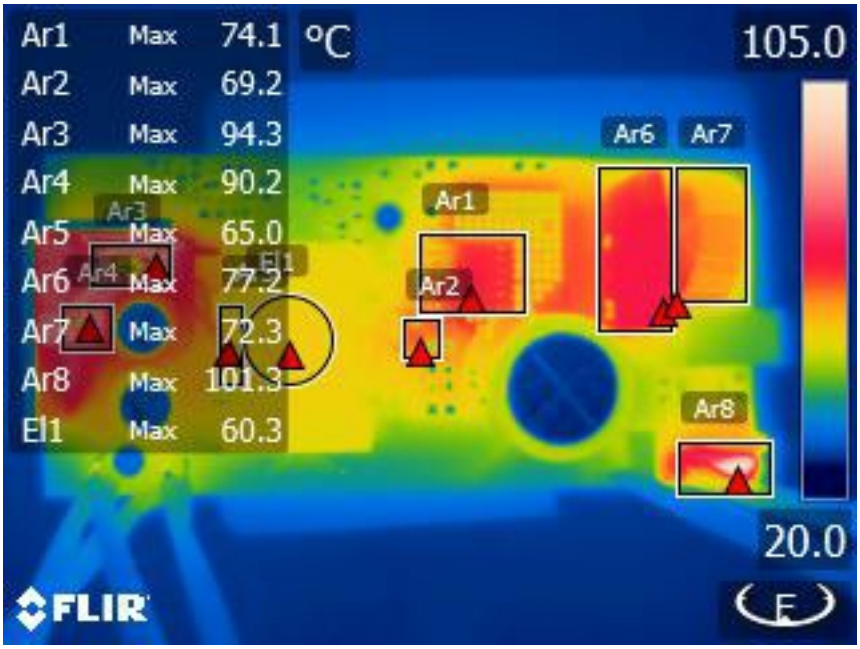


Figure 69 – 85 VAC 60 Hz. Top Side Thermals.

Component		Actual Temperature	Temperature (Normalized to 25 °C)
Ambient		31.4	25
Ar1	TOP7074K (U2)	74.1	67.7
Ar2	Primary Snubber Diode (D1)	69.2	62.8
Ar3	Output Diode Rectifier (D5)	94.3	87.9
Ar4	Secondary Snubber Resistor (R13)	90.2	83.8
Ar5	TF Winding (T1)	65.0	58.6
Ar6	Bridge Rectifier (BR1)	77.2	70.8
Ar7	CMC (L2)	72.3	65.9
Ar8	Thermistor (RT1)	101	94.9
El1	TF Core (T1)	60.3	53.9

12.1.2 265 VAC Full Load at Room Ambient

Test result after 2 hours running continuously inside an enclosure at 265 VAC full load using FLIR thermal camera to measure component temperatures.

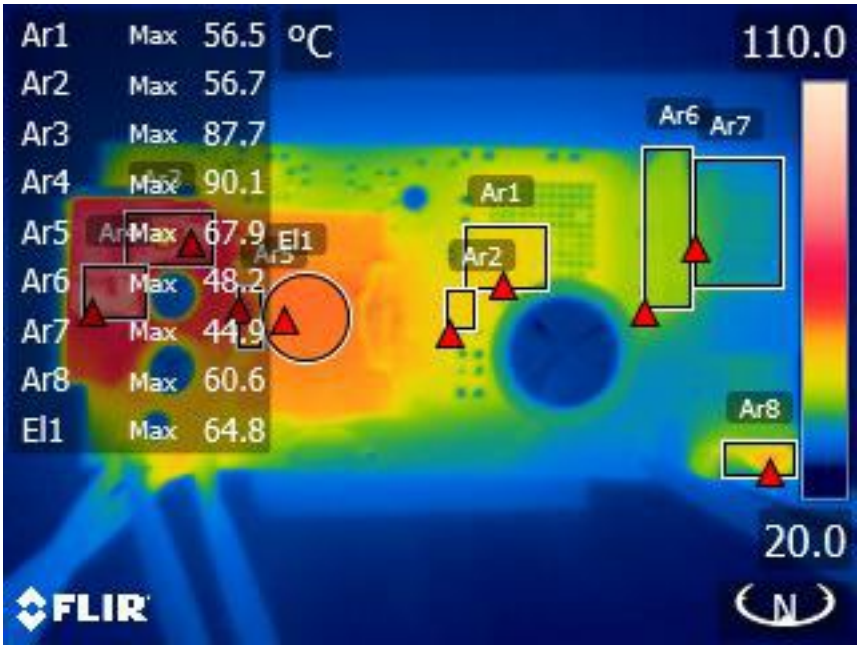


Figure 70 – 265 VAC 50 Hz. Top Side Discrete Component Thermals.

Component		Actual Temperature	Temperature (Normalized to 25 °C)
Ambient		28	25
Ar1	TOP7074K (U2)	56.5	52.5
Ar2	Primary Snubber Diode (D1)	56.7	53.7
Ar3	Output Diode Rectifier (D5)	87.7	84.7
Ar4	Secondary Snubber Resistor (R13)	90.1	87.1
Ar5	TF Winding (T1)	67.9	64.9
Ar6	Bridge Rectifier (BR1)	48.2	45.2
Ar7	CMC (L2)	44.9	41.9
Ar8	Thermistor (RT1)	60.6	57.6
El1	TF Core (T1)	64.8	61.8

12.2 Thermal Performance at 25 °C Ambient

12.2.1 85 VAC Full Load at 25 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 85 VAC full load using thermocouple to measure component temperatures.

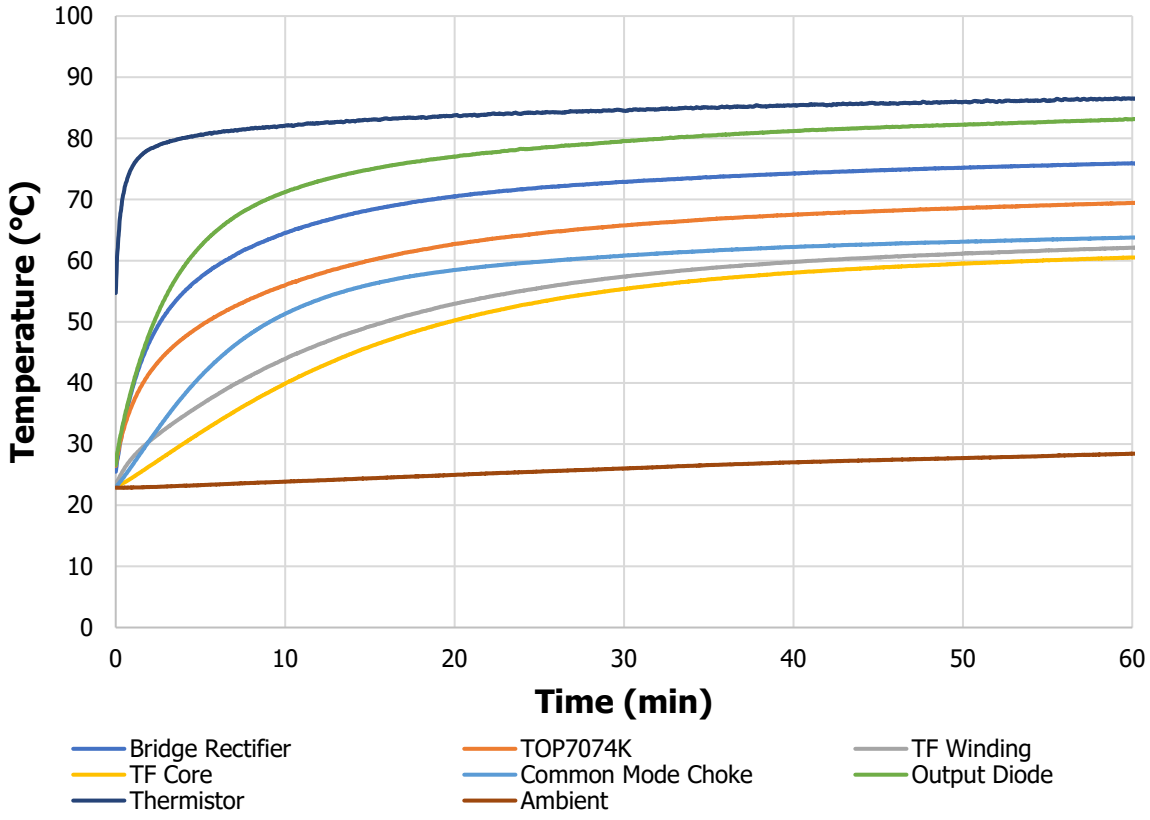


Figure 71 – 85 VAC 60 Hz Component Thermals.

Component	Temperature (°C)
TOP7074K	69.8
TF Winding	62.5
TF Core	60.9
Bridge Rectifier	76.3
Common Mode Choke	64.1
Output Diode	83.6
Thermistor	86.9
Ambient	28.8

12.2.2 265 VAC Full Load at 25 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 265 VAC full load using thermocouple to measure component temperatures.

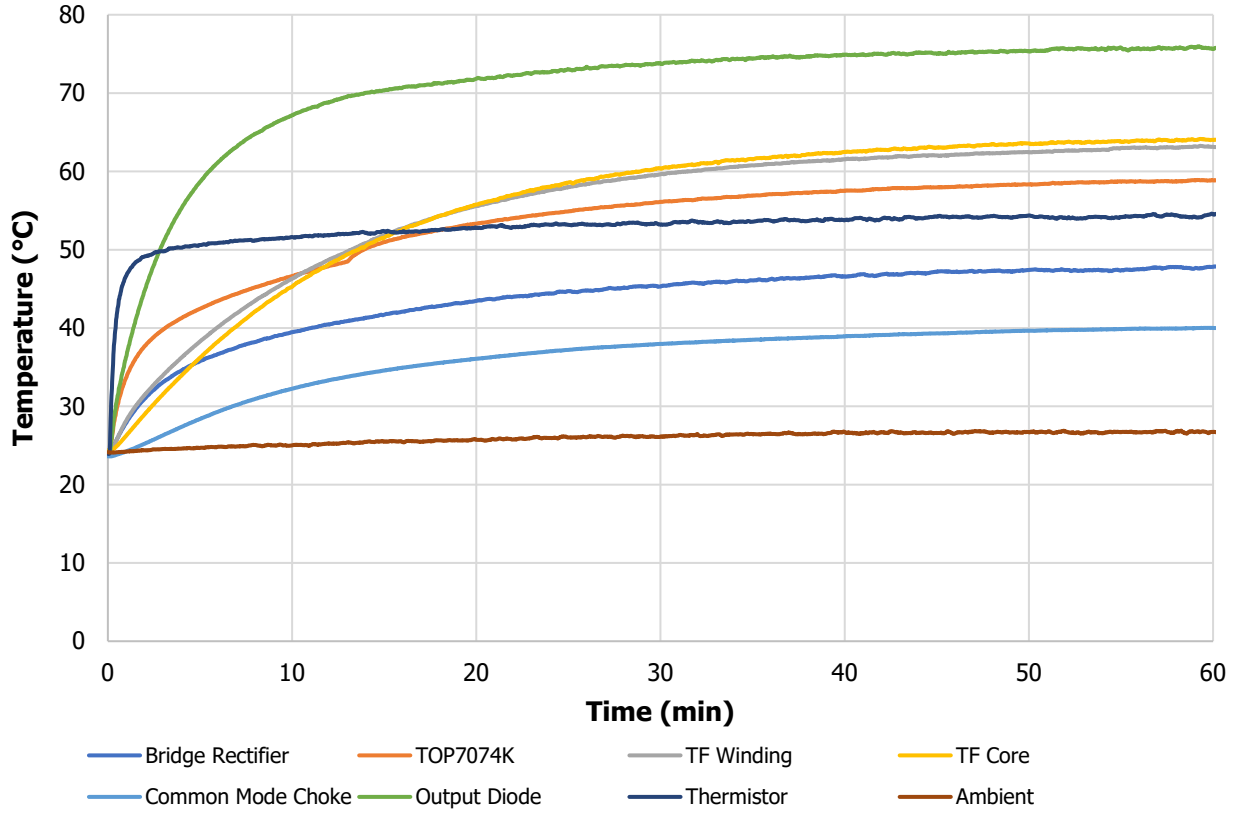


Figure 72 – 265 VAC 50 Hz Component Thermals.

Component	Temperature (°C)
TOP7074K	58.9
TF Winding	63.1
TF Core	64.1
Bridge Rectifier	47.9
Common Mode Choke	40
Output Diode	75.8
Thermistor	54.6
Ambient	26.7

12.3 Thermal Performance at 40 °C Ambient

12.3.1 85 VAC Full Load at 40 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 85 VAC full load using thermocouple to measure component temperatures.

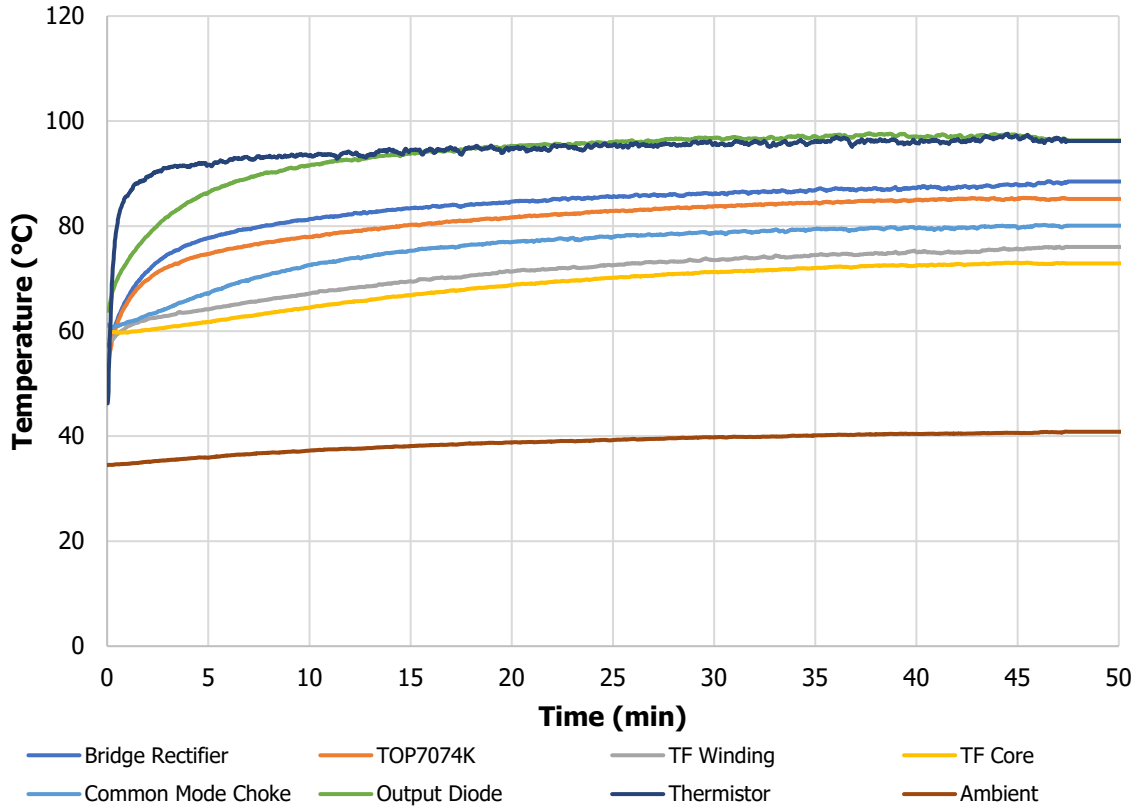


Figure 73 – 85 VAC 60 Hz Component Thermals.

Component	Temperature (°C)
TOP7074K	85.4
TF Winding	76.1
TF Core	73.1
Bridge Rectifier	88.5
Common Mode Choke	80.2
Output Diode	97.7
Thermistor	97.6
Ambient	40.9

12.3.2 265 VAC Full Load at 40 °C Ambient

Test result after 60 mins running continuously inside thermal chamber at 265 VAC full load using thermocouple to measure component temperatures.

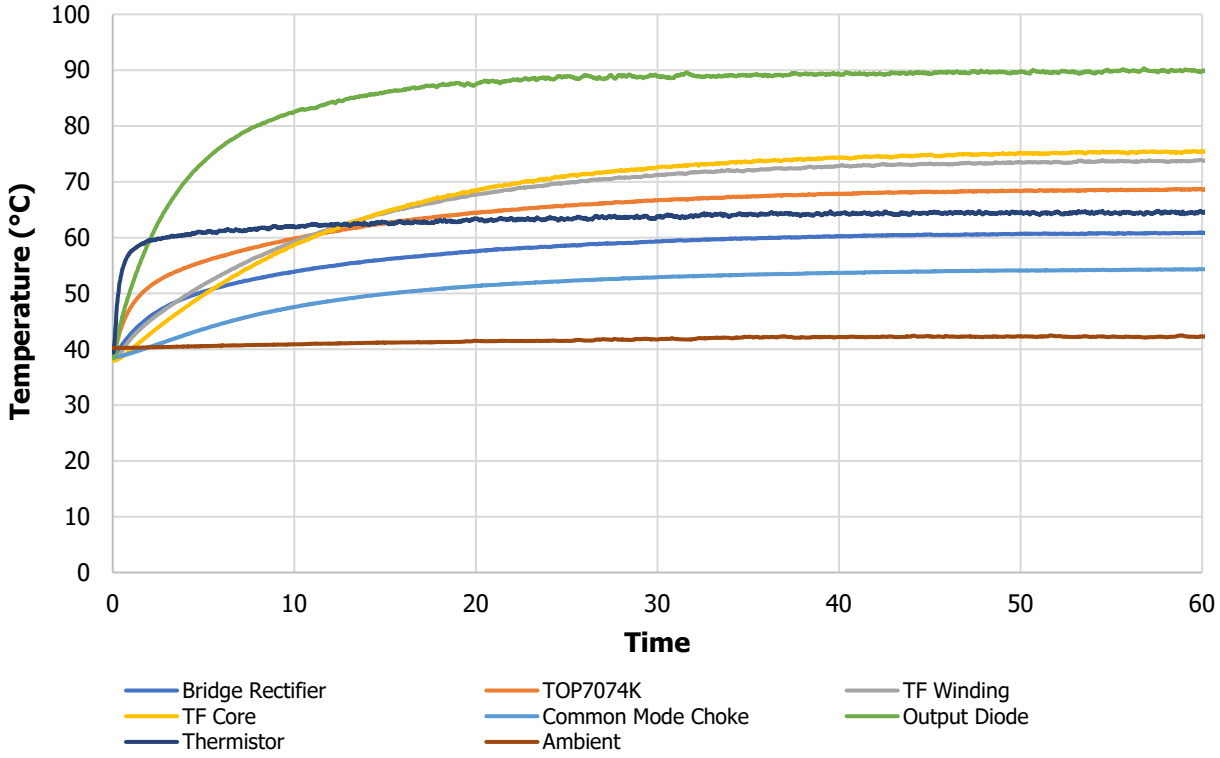


Figure 74 – 265 VAC 50 Hz Component Thermals.

Component	Temperature (°C)
TOP7074K	68.9
TF Winding	74.1
TF Core	75.8
Bridge Rectifier	61.1
Common Mode Choke	54.5
Output Diode	90.4
Thermistor	64.9
Ambient	43

13 Fault Protection

13.1 Output Short-Circuit Protection

13.1.1 Start-Up Short

Figure 75 – 85 VAC, Startup Output Short.
CH1: TOP7074K_V_{DS}, 200 V / div., 500 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 500 ms / div.
CH3: V_{OUT}, 5V / div., 500 ms / div.
CH4: V_{BP}, 2 V / div., 500 ms / div.
Zoom: 20 ms/div.
$V_{DS\ max}$ = 247 V, 34% derating
$I_{DS\ max}$ = 2.86 A
$t_{AR(ON)}$ = 74 ms
$t_{AR(OFF)}$ = 1.22 s
$t_{AR(OFF)H}$ = 371 ms

Figure 76 – 265 VAC, Startup Output Short.
CH1: TOP7074K_V_{DS}, 200 V / div., 500 ms / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 500 ms / div.
CH3: V_{OUT}, 5V / div., 500 ms / div.
CH4: V_{BP}, 2 V / div., 500 ms / div.
Zoom: 20 ms/div.
$V_{DS\ max}$ = 572 V, 78.9% derating
$I_{DS\ max}$ = 6.66 A
$t_{AR(ON)}$ = 368 ms
$t_{AR(OFF)}$ = 1.25 s
$t_{AR(OFF)H}$ = 371 ms

13.2 Overpower Protection

Figure 77 – 100 VDC, Io = 3.1 A (74.4 W).
CH1: TOP7074K_V_{DS}, 200 V / div., 500 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 500 µs / div.
CH3: V_{BP}, 1 V / div., 500 µs / div.
CH4: V_{OUT}, 5 V / div., 500 µs / div.
Zoom: 10 µs/div.
F_S = 152 kHz
I_{LIM} = 1.86 A

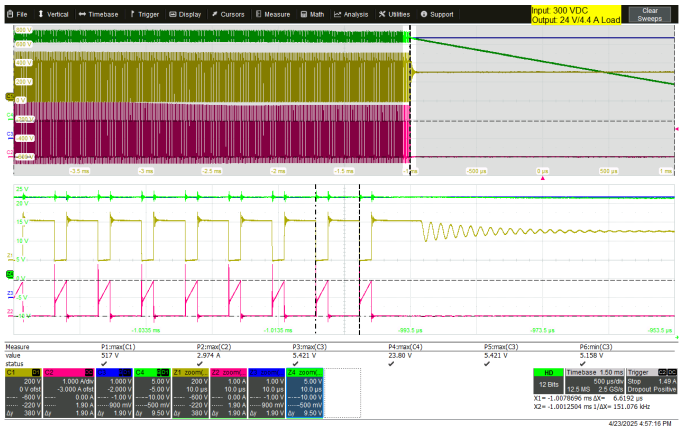


Figure 78 – 300 VDC, Io = 4.4 A (106 W).
CH1: TOP7074K_V_{DS}, 200 V / div., 500 µs / div.
CH2: TOP7074K_I_{DS}, 1 A / div., 500 µs / div.
CH3: V_{BP}, 1 V / div., 500 µs / div.
CH4: V_{OUT}, 5 V / div., 500 µs / div.
Zoom: 10 µs/div.
F_S = 151 kHz
I_{LIM} = 1.9 A

13.3 Overtemperature Protection

The unit was placed inside the thermal chamber and ambient temperature was increased to trigger over-temperature conditions and then decreased for thermal recovery. IC case temperature was measured using thermocouple.

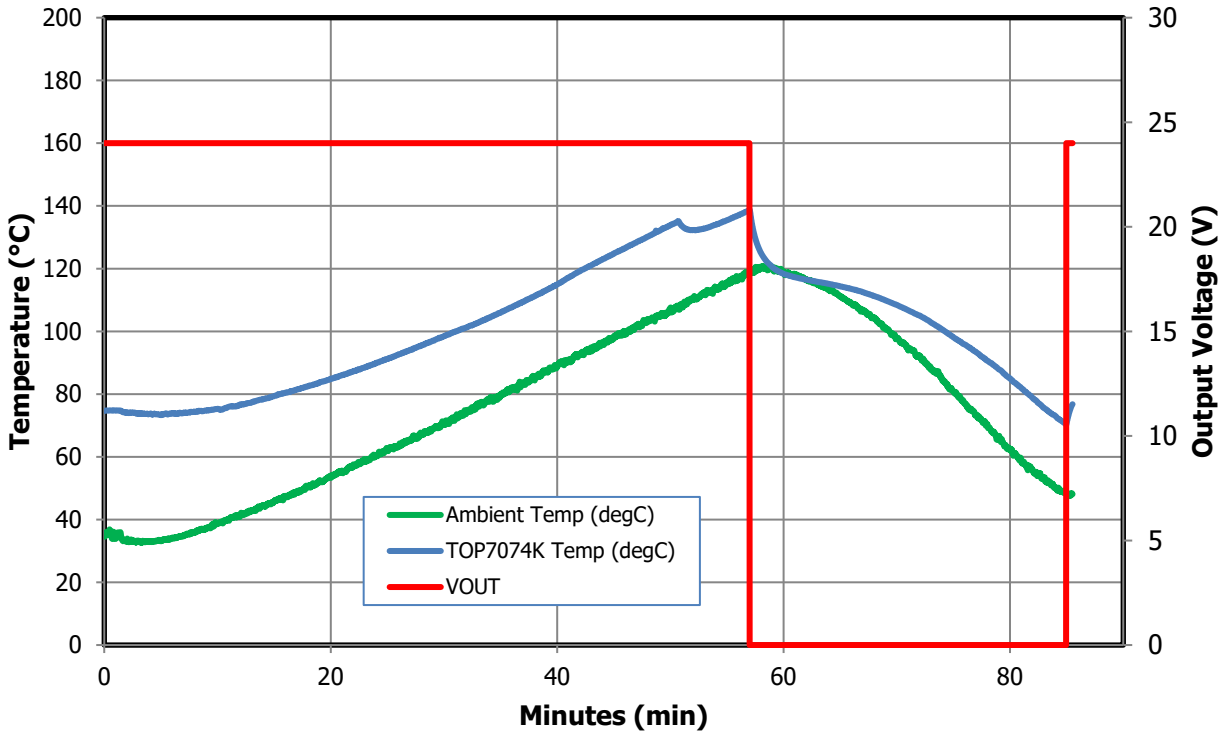


Figure 79 – 85 VAC Full Load OTP.

OTP Temperature	138 °C
Recovery Temperature	70.3 °C
Hysteresis	68.5 °C

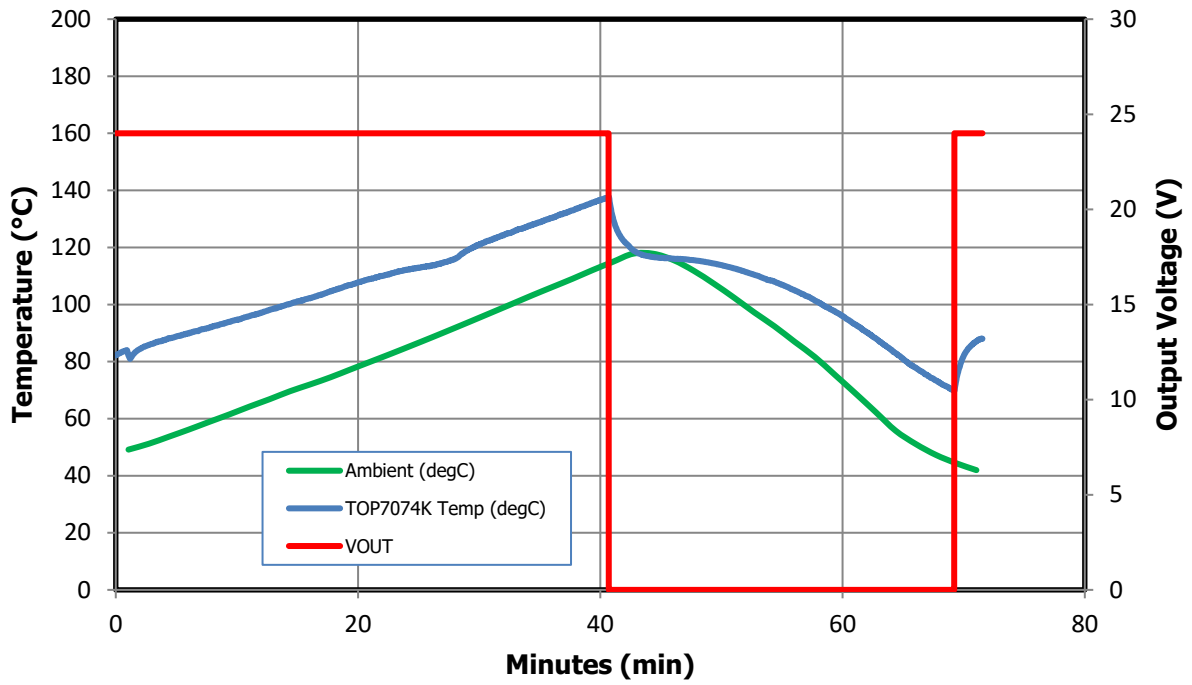


Figure 80 – 85 VAC Full Load OTP.

OTP Temperature	138 °C
Recovery Temperature	69.8 °C
Hysteresis	68.0 °C

14 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (24 V, 2.5 A). Measurements were taken with floating ground.

14.1 Test Set-up Equipment

14.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Input voltage set at 115 VAC and 230 VAC.
4. 24 V R_{LOAD} resistance is 9.6 Ohms.

14.2 Output Float

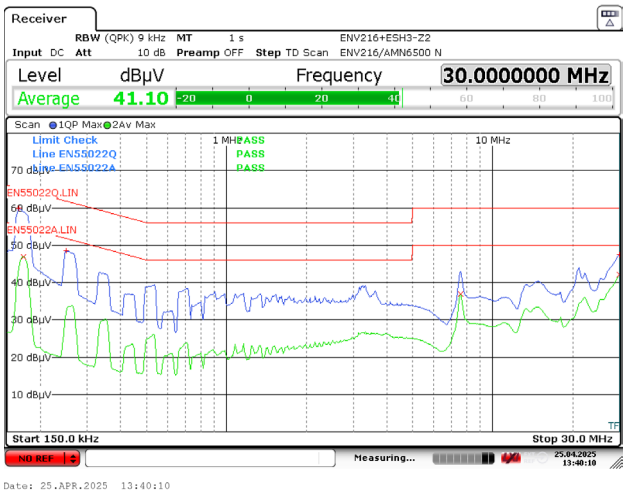


Figure 81 – 115 VAC 60 Hz.
Line / Neutral - Floating

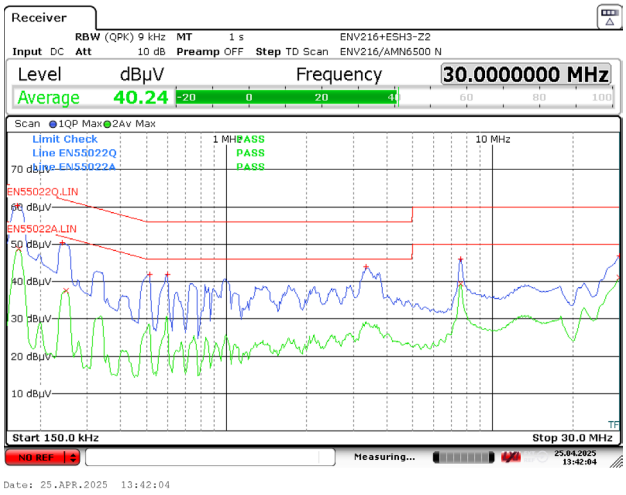


Figure 82 – 230 VAC 50 Hz.
Line / Neutral - Floating

15 ESD

All ESD strikes were applied at PCB end with 115 and 230 VAC input voltage and full load.

Input: 115 VAC, Output: 24 V/9.6 Ω Full Load

Passed ±8.8 kV contact discharge

Contact Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+8.8	24 V	10	PASS
-8.8	24 V	10	PASS
+8.8	GND	10	PASS
-8.8	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Passed ±16.5 kV air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+16.5	24 V	10	PASS
-16.5	24 V	10	PASS
+16.5	GND	10	PASS
-16.5	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Input: 230 VAC, Output: 24 V/9.6 Ω Full Load

Passed ±8.8 kV contact discharge

Contact Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+8.8	24 V	10	PASS
-8.8	24 V	10	PASS
+8.8	GND	10	PASS
-8.8	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

Passed ±16.5 kV air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+16.5	24 V	10	PASS
-16.5	24 V	10	PASS
+16.5	GND	10	PASS
-16.5	GND	10	PASS

Note: In all PASS results, power supply was still functional after the test.

16 Combination Wave (Differential Mode)

Tested at 115 and 230 VAC input voltage and full load

Input: 115 VAC, Output: 24 V/9.6 Ω Full Load

Passed 2 kV Differential Mode Combination Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+2000 V	0°	L, N	2 Ω	10	PASS
–2000 V	0°	L, N	2 Ω	10	PASS
+2000 V	90°	L, N	2 Ω	10	PASS
–2000 V	90°	L, N	2 Ω	10	PASS
+2000 V	180°	L, N	2 Ω	10	PASS
–2000 V	180°	L, N	2 Ω	10	PASS
+2000 V	270°	L, N	2 Ω	10	PASS
–2000 V	270°	L, N	2 Ω	10	PASS

Input: 230 VAC, Output: 24 V/9.6 Ω Full Load

Passed 2 kV Differential Mode Combination Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+2000 V	0°	L, N	2 Ω	10	PASS
–2000 V	0°	L, N	2 Ω	10	PASS
+2000 V	90°	L, N	2 Ω	10	PASS
–2000 V	90°	L, N	2 Ω	10	PASS
+2000 V	180°	L, N	2 Ω	10	PASS
–2000 V	180°	L, N	2 Ω	10	PASS
+2000 V	270°	L, N	2 Ω	10	PASS
–2000 V	270°	L, N	2 Ω	10	PASS

17 Ring Wave (Common Mode)

Tested at 115 VAC and 230 VAC input voltage and full load

Input: 115 VAC, Output: 24 V/9.6 Ω Full Load

Passed 6 kV Common Mode Ring Wave Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+6000 V	0°	L/N - PE	12	10	PASS
–6000 V	0°	L/N - PE	12	10	PASS
+6000 V	90°	L/N - PE	12	10	PASS
–6000 V	90°	L/N - PE	12	10	PASS
+6000 V	180°	L/N - PE	12	10	PASS
–6000 V	180°	L/N - PE	12	10	PASS
+6000 V	270°	L/N - PE	12	10	PASS
–6000 V	270°	L/N - PE	12	10	PASS

Input: 230 VAC, Output: 24 V/9.6 Ω Full Load

Passed 6 kV Common Mode Ring Wave Surge Event

Surge Voltage	Phase Angle	IEC Coupling	Generator Impedance	Number of Strikes	Results
+6000 V	0°	L/N - PE	12	10	PASS
–6000 V	0°	L/N - PE	12	10	PASS
+6000 V	90°	L/N - PE	12	10	PASS
–6000 V	90°	L/N - PE	12	10	PASS
+6000 V	180°	L/N - PE	12	10	PASS
–6000 V	180°	L/N - PE	12	10	PASS
+6000 V	270°	L/N - PE	12	10	PASS
–6000 V	270°	L/N - PE	12	10	PASS

18 EFT

Tested at 115 VAC & VAC Input Voltage and Full Load
Input: 115 VAC, Output: 24 V/9.6 Ω Full Load

Passed 4 kV EFT Event

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass

Input: 230 VAC, Output: 24 V/9.6 Ω Full Load

Passed 4 kV EFT Event

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2	Pass

Surge Voltage	Injection Phase	Frequency	T-Burst	T-Rep	Test Duration	Injection Location	Remarks
+4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	0°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	90°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	180°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	5 kHz	15 ms	300 ms	120 s	L1/L2 - PE	Pass
+4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass
–4000 V	270°	100 kHz	750 μs	300 ms	120 s	L1/L2 - PE	Pass

19 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Oct-25	MA	A	Initial Release	Apps & Mktg.
29-Jun-26	MA	B	Updated Schematic	Apps & Mktg.

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