Design Example Report

Title	**75 W 24 V Low Profile LED Driver Using CAPZero™-2, HiperPFS™-4 Qspeed™ diode and PowiGaN-Based InnoSwitch4™-QR ICs**
Specification	Input: 198 VAC – 305 VAC Nominal Output: 24 V / 3.13 A
Application	LED Driver, Smart Lighting
Author	Applications Engineering Department
Document Number	DER-1061
Date	November 3, 2025
Revision	A

Summary and Features

- > 92% full load efficiency @ 230 VAC
- Low profile board < 16 mm high
- Low component count (80 parts)
- > 0.93 full load power factor from 230 - 277 VAC
- Full load THD, < 10% @ 230 VAC
- Protection Features
  - Fast input UV/OV protection
  - Output over-current, overvoltage and undervoltage protection
  - Over-temperature protection (OTP)
- Meets 2 kV combination wave differential mode surge
- Meets 2.5 kV ring-wave common mode and differential surge

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a two-stage 75 W isolated flyback power supply that utilizes the HiperPFS™-4 Boost PFC IC and the InnoSwitch4™-QR flyback IC. The power supply can deliver a continuous output of 24 V / 3.13 A across an input range of 198 VAC to 305 VAC. The power supply is designed for LED strip light applications and utilizes low-profile components to meet typical form factor requirements. The low-profile packages employed by the HiperPFS-4 and InnoSwitch4-QR ICs make them ideal for this type of application.

The HiperPFS-4 devices incorporate a continuous conduction mode (CCM) boost PFC controller and 600 V power MOSFET in a single IC.

The InnoSwitch4-QR IC combines a high-voltage PowiGaN switch with both primary-side and secondary-side controllers in a single IC.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

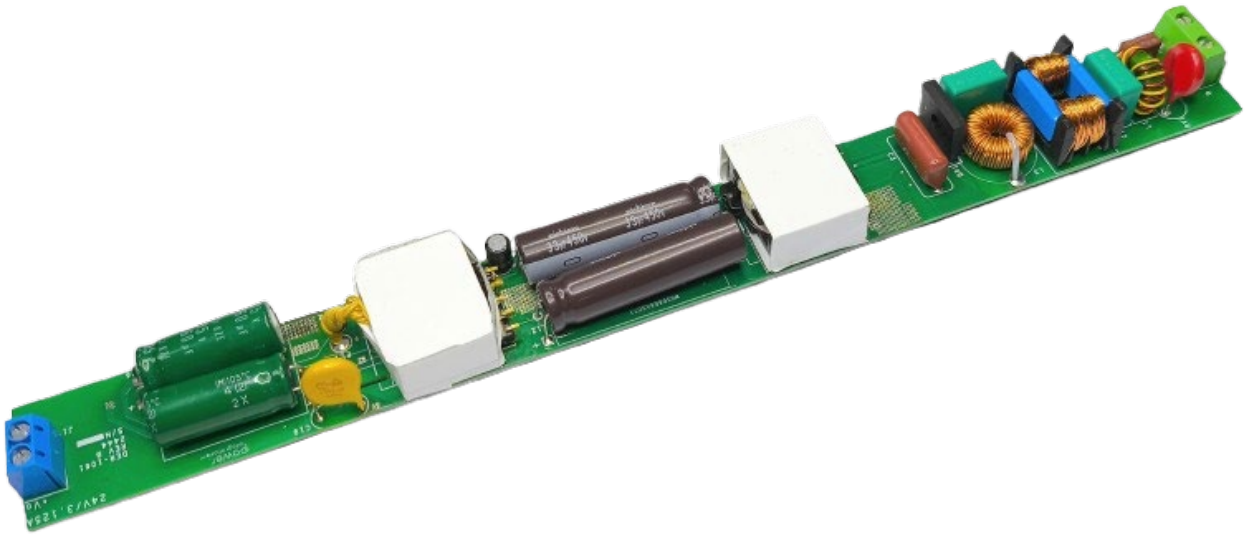


Figure 1 – Populated Circuit Board, Oblique View of Top Side.

Figure 2 – Populated Circuit Board, Top Side.

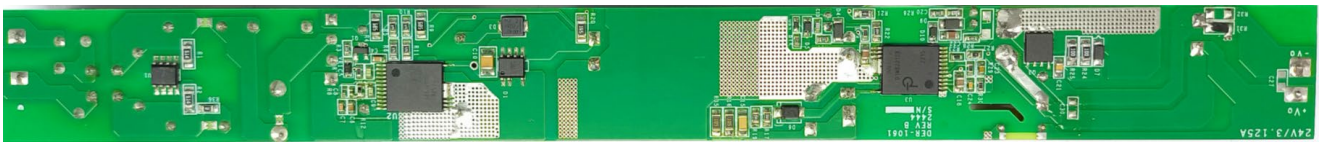


Figure 3 – Populated Circuit Board, Bottom Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	198		305	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				100	mW	277 VAC.
Output						
Output Voltage	V_{OUT}	22.8	24	25.2	V	±5%
Output Current	I_{OUT}			3.13	A	
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz Bandwidth.
Output Power	P_{OUT}		75		W	
Efficiency						
Full Load	$\eta_{Full-Load}$	92			%	At 230 VAC and 277 VAC, Measured at Output Terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Load floating			Resistive Load
Line Surge						
Combination (L/N)				±2	kV	Differential: 2 Ω
Ring Wave (L/N & L,N/PE)				±2.5	kV	Differential and Common Mode: 12 Ω
ESD				±16.5		Air Discharge
				±8.8		Contact Discharge
Ambient Temperature	T_{AMB}	0		55	°C	Free Convection, Sea Level in Sealed Enclosure.

Figure 4 – Power Supply Specification.

3 Schematic

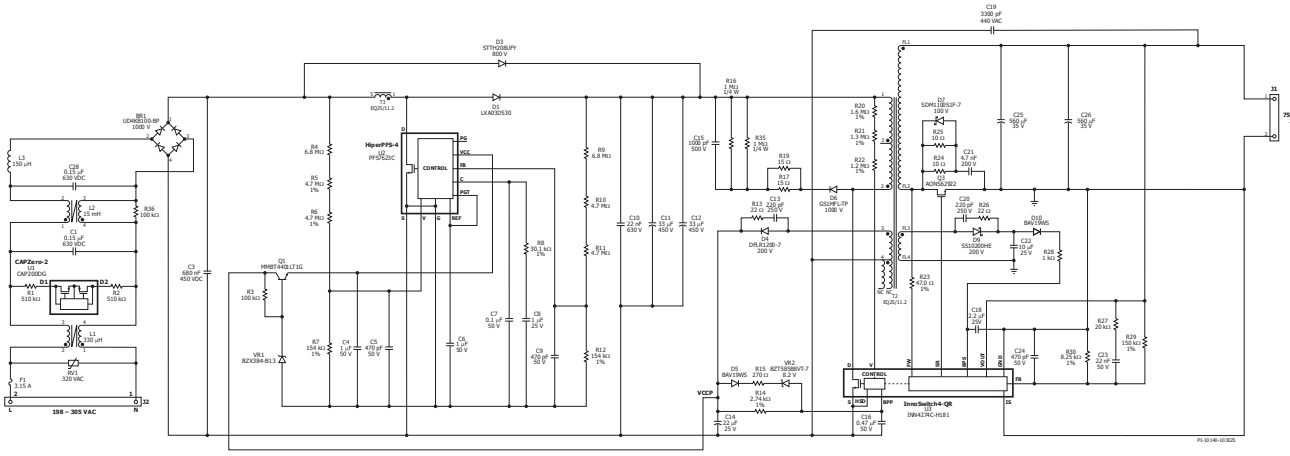


Figure 5 – Schematic Showing PFC and DC-DC isolated flyback Conversion Stages.

4 Circuit Description

4.1 Input Rectification and EMI Filtering

Fuse F1 isolates the PSU circuitry and provides protection from component failure. RV1 protects the circuit from high voltage differential surge. The common-mode chokes L1 and L2, along with the differential choke L3 and X-capacitors C1 and C28, attenuate common-mode and differential-mode noise. C3 provides differential mode EMI filtering. The HiperPFS-4 IC provides compensation for the input filter capacitance that is inserted in front of the PFC stage. The value of C3 was optimized to support this correction characteristic.

4.2 Zero Loss Automatic X-Capacitor Discharge CAPZero-2 IC

To satisfy safety requirements when the AC supply is disconnected, the CAP200DG IC (U1) automatically quickly discharges the X capacitors C1 and C28 to a safe (SELV) level by connecting discharge resistors R1 and R2 when the AC rail is disconnected. When AC voltage is applied, the CAP200DG IC blocks current flow, reducing no-load power loss of this stage to less than 5 mW.

4.3 Boost PFC using HiperPFS-4

The PFC circuit shown in Figure 5 uses a PFS7623C device from the HiperPFS-4 family. This design provides a nominal regulated output voltage of 400 V to the flyback converter and maintains a high input power factor and high efficiency across load and line. Boost inductor T3 and boost diode D1, in conjunction with the HiperPFS-4 IC U2 form the boost converter stage, controlling the input current to the power supply while simultaneously regulating the DC output voltage.

Diode D3 is used to bypass the PFC inductor T3 and charge the bulk capacitors C11 and C12 during start-up when the rectified AC voltage is greater than the output of the PFC. Capacitor C10 is used to reduce EMI and prevent voltage overshoot across the MOSFET inside U2. The PFS7623C IC requires a regulated supply of 12 V for normal operation (15 V maximum) which is provided by the flyback stage. Resistor R3, Zener diode VR1, and transistor Q1 form a series pass regulator that provides a 12 V regulated supply to the PFS7623C IC. Capacitor C4 filters the IC supply voltage and provides decoupling to ensure reliable operation.

The power-good signal is not used in this design, so the POWER GOOD THRESHOLD pin is tied to the REFERENCE pin. IC U2 is configured to full-power mode by capacitor C6, which is connected to the REFERENCE pin. The rectified AC input voltage to the power supply is sensed by U1 via resistors R4 - R7. These resistor values are large to minimize power consumption. Capacitor C5, connected in parallel with the bottom resistor R7, prevents noise being introduced into the VOLTAGE MONITOR pin. The output voltage divider network comprising resistors R9 - R12 is used to scale the output voltage and provide feedback to the IC. Capacitor C9, in parallel with resistor R12, attenuates high-frequency noise. Components R8, C8, and C7 are required for shaping the loop response of the feedback network.

4.4 InnoSwitch4-QR Primary

This DC-DC stage is an isolated flyback converter. One end of the primary winding of transformer (T2) is connected to the rectified DC bus, while the other end is connected to the DRAIN pin of the power switch inside the InnoSwitch4-QR IC (U3).

Rectifier diode D6, resistors R16, R17, R19, and R35 along with capacitor C15, form a primary clamp circuit that reduces the voltage spike across the primary switch during turn-off which is caused by the leakage inductance of the transformer.

The InnoSwitch4-QR IC (U3) is self-starting, using an internal high-voltage current source to charge the capacitor C16 connected to the BPP pin when high voltage DC is first applied. During normal operation, the primary side of U3 is powered from the auxiliary bias-winding of transformer T2. The auxiliary supply voltage is rectified by diode D4 and filtered by electrolytic capacitor C14. Bias supply-current limiting resistor R14 is optimized to efficiently deliver bias current to U3 at full load. The slow reverse recovery of the bias diode and the RC snubber formed by R13 and C13 reduce radiated EMI.

Output regulation is achieved by cycle-by-cycle frequency and ILIM adjustment based on output load. At high load, the switching frequency and ILIM are high. Both are reduced as load decreases. The value of the PRIMARY BYPASS pin capacitor (C16) sets the maximum ILIM for the IC (in this case to standard). A switching cycle is initiated by the secondary-side controller which sends a switching request to the primary controller across the isolation barrier via a safety-rated magneto-inductive communication link (FluxLink™) located inside the InnoSwitch4-QR IC. When a switching request is received by the controller on the primary side of the IC, the primary switch is turned on, and will remain on until the primary current ramps to the device current limit. The current limit itself is set by the rate at which switching requests are received by the primary-side controller.

4.5 InnoSwitch4-QR Secondary

The secondary side block of the InnoSwitch4-QR controller IC is powered by a 4.5 V (V_{BPS}) internal regulator, which is supplied from either the VOUT or FWD Pins. The SECONDARY BYPASS pin is connected to an external decoupling capacitor C18 and is internally fed from the internal voltage regulator. To minimize power dissipated by the internal linear regulator, an auxiliary bias supply for the BPS was added. This is formed by D9, C22, D10, and R28. Additionally, an RC snubber (C20 and R26) was connected across D9 to reduce radiated EMI.

The secondary side controller in the InnoSwitch4-QR IC regulates output voltage, provides output current sensing, and delivers the gate-drive for the Synchronous Rectification MOSFET (SR FET). The secondary output of the transformer is rectified by SR FET Q3 and filtered by capacitors C25 and C26.

To reduce high-frequency voltage ringing during the SR FET turn-off (which would create radiated EMI and/or exceed the peak inverse voltage (PIV) rating of Q3), RC snubber components C21, R24, and R25 were added. The use of a Schottky type rectifier diode, D7, increases the efficiency of the output rectifier.

The FORWARD pin provides input for negative edge detection, which is used to determine timing for the turn-on of the SR FET Q3. The voltage sensed by resistor R23 on the FORWARD pin is used to determine when to turn the SR FET off in discontinuous mode (DCM) operation. This occurs when the voltage across the SR FET drops below zero. In continuous conduction mode (CCM), the SR FET is turned off before a switching cycle request is sent to the primary. This process provides accurate timing for the synchronous MOSFET turn-off and ensures optimum synchronization between primary and secondary switching.

Output voltage is regulated via a reference voltage of 1.265 V on the IC FB pin. Voltage divider resistors R29 and R30 are used to set the nominal output voltage to 24 V. Additionally, the RC phase boost (C23 and R27) helps to speed up voltage sensing, thereby reducing output ripple voltage and preventing pulse grouping. C24 minimizes noise on the FB pin of U3.

Over-current protection is triggered by the detection of continuous secondary switching requests at above the overload detection frequency f_{OVL} (140 kHz typical). When requests above this frequency are received continuously for longer than 82 ms (t_{AR}) U3 will enter auto-restart.

5 PCB Layout

The PCB uses FR4 material with a thickness of 1.2 mm and a double-sided copper layer with a thickness of 2.0 oz.

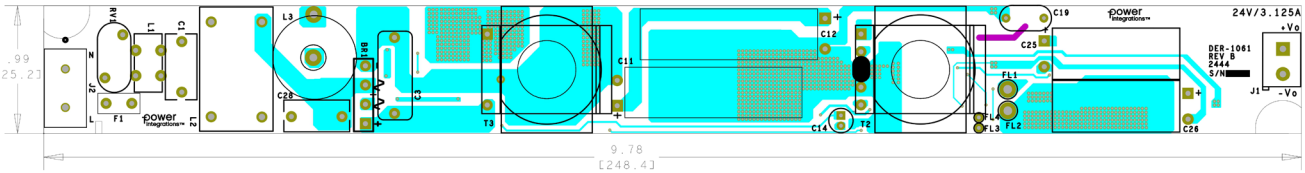


Figure 6 – Printed Circuit Layout, Top.

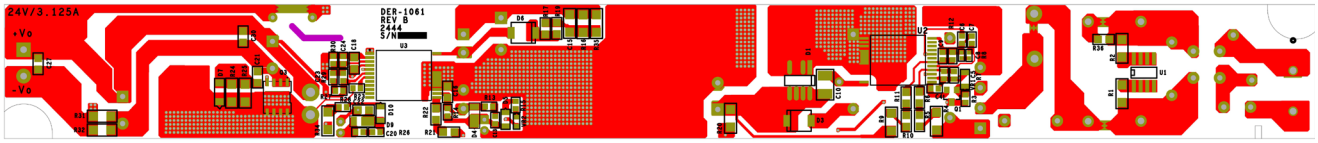


Figure 7 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item Number	Part Reference	Qty.	Description	Mfr. Part Number	Manufacturer
1	BR1	1	Bridge Rectifier, 1000 V, 4 A, 4-ESIP, D3K, -55 °C ~ 150 °C (TJ), Vf=1 V @ 7.5 A	UD4KB100-BP	Micro Commercial Co
2	C1 C28	2	CAP, 0.15 µF, ±20%, 630 VDC, 310 VAC, FILM, POLYPROP, RAD, X2, 13mmL, 6mmW, 12mmH, 10mm LS	F861AP154M310L	KEMET
3	C3	1	CAP, FILM, 0.68 µF, 10%, 450 VDC, RADIAL	ECW-FD2W684K	Panasonic Electronic Components
4	C4 C6	2	1 µF, ±10%, 50 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	06035C105KAT2A	AVX Corporation
5	C5 C9	2	470 pF 50 V, Ceramic, C0G/NP0, 0603	VJ0603A471JXAAC	Vishay Vitramon
6	C7	1	CAP, 0.1 µF ±10% 50 V Ceramic Capacitor X7R 0603 (1608 Metric)	CGA3E2X7R1H104K080AA	TDK Corporation
7	C8	1	1 µF 25 V, Ceramic, X5R, 0402 REPLACEMENT FOR 20-09142-00 a replacement for 20-00844-00	TMK105BJ105MV-F	Taiyo Yuden
8	C10	1	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
9	C11 C12	2	33 µF, 450 V, Aluminum Electrolytic Capacitors, Radial, Can 10000 Hrs @ 105 °C, (10 x 40)	UCS2W330MND9	Nichicon
10	C13 C20	2	220 pF, 250 V, Ceramic, COG, 0603	C1608C0G2E221J	TDK Corp
11	C14	1	22 µF, 25V, Electrolytic, 20%, Gen. Purpose, (5 x 7 mm)	EEA-GA1E220	Panasonic
12	C15	1	1000 pF, 1 nF, ±10%, 500 V, Ceramic Capacitor X7R, 1206 (3216 Metric)	CC1206KKX7RBBB102	Yageo
13	C16	1	0.47 µF, ±10%, 50 V, Ceramic, X7R, 0805 (2012 Metric), -55 °C ~ 125 °C	CGA4J3X7R1H474K125AB	TDK Corp
14	C18	1	2.2 µF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	C2012X7R1E225K125AB	TDK Corporation
15	C19	1	3300 pF, ±20%, 440 VAC, Ceramic Capacitor Y5U (E), Safety X1, Y2, Radial, Disc	VY2332M41Y5US63V7	Vishay Beyschlag/Draloric/ BC Components
16	C21	1	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX Corp
17	C22	1	10 µF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	GRT21BC71E106KE13L	Murata Electronics
18	C23	1	0.022 µF, ±10%, 50 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	06035C223KAT2A	AVX Corp
19	C24	1	470 pF, ±10%, 50 V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B471KB8NFNC	Samsung
20	C25 C26	2	560 µF, 35 V, Electrolytic, Very Low ESR, 22 mOhm, (10 x 25)	EKZE350ELL561MJ25S	Nippon Chemi-Con
21	D1	1	530 V, 3 A, D PACKAGE (SO-8C)	LXA03D530	Power Integrations
22	D3	1	Diode, GP, 800 V, 2 A, Surface Mount SMBflat DO-221AA, SMB Flat Leads	STTH208UFY	STMicroelectronics
23	D4	1	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes Inc
24	D5 D10	2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
25	D6	1	Diode, GP, 1000 V, 1 A, Surface Mount DO-221AC (SMA-FL) (SlimSMA)	GS1MFL-TP	Micro Commercial Co
26	D7	1	DIODE, SCHOTTKY, 100 V, 1 A, SOD123F	SDM1100S1F-7	Diodes Incorporated
27	D9	1	Diode, Schottky, 200 V, 1 A, Surface Mount SOD-123HE	SS10200HE_R1_00001	Panjit International Inc.
28	F1	1	3.15 A, 300 V, Slow, Long Time Lag, RST	36913150000	Littelfuse Inc

29	L1	1	CMC, 330 µH @ 100KHz, ±20%, Toroidal, wound on 32-00315-00 toroidal core	32-00466-00	Power Integrations
30	L2	1	15 mH @ 10 kHz, 2 Line Common Mode Choke, Through Hole, 1.3 A, DCR 430 mOhm (Typ), 24.5 x 14.5 mm x 13.5 mm height	B82732F2132B001	Epcos
31	L3	1	150 µH, 20%, 2.5 A, Rdc=0.01, INDUCTOR, TOROID, HI AMP, VERT, 16.5 mmDiam, 8.5 mm Thick, 8.5 mm LS	7447018	Wurth Elect Inc
32	Q1	1	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300 mW, SOT-23, SOT-23-3 (TO-236)	MMBT4401LT1G	On Semiconductor
33	Q3	1	MOSFET, N-CH, 120 V, 85 A (at VGS = 10 V), Trench Power AlphaSGT 120V TM technology, DFN5X6	AONS62922	Alpha & Omega Semiconductor Inc.
34	R1 R2	2	RES, 510 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J514V	Panasonic
35	R3	1	RES, 100 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
36	R4 R9	2	RES, 6.8 M, 5%, 1/4 W, Thick Film, 1206	RC1206JR-076M8L	YAGEO
37	R5 R6 R10 R11	4	RES, 4.7 M, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ475V	Panasonic
38	R7 R12	2	RES, 154 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1543V	Panasonic
39	R8	1	RES, 30.1 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
40	R13 R26	2	RES, 22 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
41	R14	1	RES, 2.74 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2741V	Panasonic
42	R15	1	RES, 270 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ271V	Panasonic
43	R16 R35	2	RES, 1 Mohms, ±5%, 0.25 W, 1/4 W Chip Resistor, 1206 (3216 Metric), High Voltage Thick Film	KTR18EZPJ105	Rohm Semiconductor
44	R17 R19	2	RES, 15 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ150V	Panasonic
45	R20	1	RES, 1.6 M, 5%, 1/4 W, Thick Film, 1206	RC1206JR-071M6L	YAGEO
46	R21	1	RES, 1.3 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1304V	Panasonic
47	R22	1	RES, 1.2 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1204V	Panasonic
48	R23	1	RES, 47.0 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF47R0V	Panasonic
49	R24 R25	2	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
50	R27	1	RES, 20 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
51	R28	1	RES, 1 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
52	R29	1	RES, 150 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1503V	Panasonic
53	R30	1	RES, 8.25 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8251V	Panasonic
54	R31	1	RES, 0 Ohms Jumper, Chip Resistor 1206 (3216 Metric), Metal Element	JR1206X40E	Ohmite
55	R36	1	100 kOhms, ±5%, 0.5 W, 1/2 W, Chip Resistor 0805 (2012 Metric), Automotive AEC-Q200, Pulse Withstanding Thick Film	ERJ-P06J104V	Panasonic
56	RV1	1	320 VAC, 48 J, 10 mm, RADIAL	V320LA10P	Littlefuse
57	T2 T3	2	Bobbin, EQ25, 6 pins, 5 pri, 1 sec	EQ25-11.2-6P-THL-A5-11	TBI
58	U1	1	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
59	U2	1	HiperPFS-4, InSOP24B	PFS7623C	Power Integrations
60	U3	1	InnoSwitch4-QR, INN4274C-H181, 230 VDC, 80 W, insop-24D	INN4274C-H181	Power Integrations
61	VR1	1	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP Semiconductors
62	VR2	1	Zener Diode 8.2 V 350 mW ±2% Surface Mount EMD2, SC-79, SOD-523	BZT585B8V2T-7	Diodes Incorporated

Table 1 – Electrical Parts.

Item Number	Part Reference	Qty.	Description	Mfr. Part Number	Manufacturer
1	J1	1	CONN TERM BLOCK, 2 POS, 5 mm, PCB	ED500/2DS	On Shore Technology Inc
2	J2	1	2 Position Wire to Board Terminal Block Horizontal with Board 0.300" (7.62 mm) Through Hole	1707027	Phoenix Contact
3	INS1	1	INN4 Gap pad 32 mm x 25 mm	COH-1706-200-20	Taica
4	INS2	1	Flyback TRF Gap pad 45 mm x 25 mm	COH-1706-200-20	Taica
5	Case	1	Case (Please refer to Section 12)	Custom	Custom

Table 2 – Miscellaneous Parts.

7 Boost Inductor Design Spreadsheet

1	**Hiper_PFS-4_Boost_031722; Rev.1.4; Copyright Power Integrations 2022**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**Continuous Mode Boost Converter Design Spreadsheet**
2	Enter Application Variables					Design Title
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN	180		180	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other voltages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	277		277	VAC	Maximum AC input voltage
6	VBROWNIN		Info	82	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
7	VBROWNOUT		Info	71	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
8	VO	400	Info	400	VDC	Brown IN/OUT voltage has changed due to modifications in the V-pin ratio from 100:1. Recommend Vpin ratio= FB pin ratio for optimized operation. Check the PF, input current distortion, brown in/out and power delivery
9	PO	81		81	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max	55	Info	55	°C	Verify thermal performance
12	Efficiency Estimate	0.95		0.95		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core auto pick core size
19						
20	**KP and INDUCTANCE**					
21	KP_TARGET	0.78		0.78		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
22	LPFC_TARGET (0 bias)			1102	µH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
23	LPFC_DESIRED (0 bias)		Info	1102	µH	Inductance too high: Core size will be too big
24	KP_ACTUAL			0.782		Actual KP calculated from LPFC_DESIRED
25	LPFC_PEAK			1102	µH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26						
27	Basic current parameters					

28	IAC_RMS			0.47	A	AC input RMS current at VACMIN and Full Power load
29	IO_DC			0.20	A	Output average current/Average diode current
30						
31						
32	PFS Parameters					
33	PFS Package	C		C		HiperPFS package selection
34	PFS Part Number	PFS7623C	Info	PFS7623C		Load power exceeds the max power rating of this family! Consider changing the input voltage range or selecting a larger device. Thermal issues possible. Verify thermal performance on the bench
35	Operating Mode	Full Power		Full Power		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
36	IOCP min			2.60	A	Minimum Current limit
37	IOCP typ			2.80	A	Typical current limit
38	IOCP max			3.00	A	Maximum current limit
39	IP			1.10	A	MOSFET peak current
40	IRMS			0.37	A	PFS MOSFET RMS current
41	RDSON			0.87	Ohms	Typical RDSon at 100 °C
42	FS_PK			107.2	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
43	FS_AVG			97.0	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
44	PCOND_LOSS_PFS			0.119	W	Estimated PFS Switch conduction losses
45	PSW_LOSS_PFS			1.322	W	Estimated PFS Switch switching losses
46	PFS_TOTAL			1.441	W	Total Estimated PFS Switch losses
47	TJ Max			100	deg C	Maximum steady-state junction temperature
48	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
49	HEATSINK Theta-CA			38.84	°C/W	Maximum thermal resistance of heatsink
50						
51						
52	INDUCTOR DESIGN					
53	Basic Inductor Parameters					
54	LPFC (0 Bias)			1102	μH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
55	LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
56	IL_RMS			0.53	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
57	Material and Dimensions					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60 u, 75 u, 90 u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	EQ		EQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	EQ25		EQ25		Core part number

62	Ae	89.70		89.70	mm^2	Core cross sectional area
63	Le			41.40	mm	Core mean path length
64	AL			4400.00	nH/t^2	Core AL value
65	Ve			4.15	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			4.95	mm	Core height/Height of window; ID if toroid
67	MLT			57.0	mm	Mean length per turn
68	BW			4.25	mm	Bobbin width
69	LG			0.91	mm	Gap length (Ferrite cores only)
70	Flux and MMF calculations					
71	BP_TARGET (ferrite only)			3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3871	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			1347	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance, minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCP_typ divided by µ at zero current
77	I_TEST			2.8	A	Current at which B_TEST and H_TEST is calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3613	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCP_typ
80	Wire					
81	TURNS			100		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			0.53	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	38		38	AWG	Inductor wire gauge
85	Filar	10		10		Filar >4 not supported, please reduce Filar
86	OD (per strand)			0.102	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.45	mm	Will be different than OD if Litz
88	DCR			1.568	ohm	ChokeDCResistance
89	P AC Resistance Ratio			0.42		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J		Warning	6.54	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
92	Layers			11.16		Estimated layers in winding
93	Loss calculations					
94	BAC-p-p			1053	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave

95	LPFC_CORE_LOSS			0.053	W	Estimated Inductor core Loss
96	LPFC_COPPER_LOSS			0.517	W	Estimated Inductor copper losses
97	LPFC_TOTAL_LOSS			0.569	W	Total estimated Inductor Losses
98						
99						
100	PFC Diode					
101	PFC Diode Part Number	LXA03D530		LXA03D530		PFS Diode Part Number
102	Type / Part Number			Qspeed		PFC Diode Type / Part Number
103	Manufacturer			PI		Diode Manufacturer
104	VRRM			530.0	V	Diode rated reverse voltage
105	IF			3.00	A	Diode rated forward current
106	Qrr			75.0	nC	Qrr at High Temperature
107	VF			1.33	V	Diode rated forward voltage drop
108	PCOND_DIODE			0.286	W	Estimated Diode conduction losses
109	PSW_DIODE			0.225	W	Estimated Diode switching losses
110	P_DIODE			0.511	W	Total estimated Diode losses
111	TJ Max			100.0	deg C	Maximum steady-state operating temperature
112	Rth-JS		Info	27.00	degC/W	Rth too high. Will result in high diode loss
113	HEATSINK Theta-CA			89.98	degC/W	Maximum thermal resistance of heatsink
114	IFSM			25.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
115						
116						
117	Output Capacitor					
118	COUT	68		68	µF	Minimum value of Output capacitance
119	VO_RIPPLE_EXPECTED			10.0	V	Expected ripple voltage on Output with selected Output capacitor
120	T_HOLDUP_EXPECTED			24.2	ms	Expected holdup time with selected Output capacitor
121	ESR_LF	0.22		0.22	ohms	Low Frequency Capacitor ESR
122	ESR_HF	0.02		0.02	ohms	High frequency ESR must be between 0.01 and 1 ohms
123	IC_RMS_LF			0.15	A	Low Frequency Capacitor RMS current
124	IC_RMS_HF			0.28	A	High Frequency Capacitor RMS current
125	CO_LF_LOSS			0.005	W	Estimated Low Frequency ESR loss in Output capacitor
126	CO_HF_LOSS			0.002	W	Estimated High frequency ESR loss in Output capacitor
127	Total CO LOSS			0.006	W	Total estimated losses in Output Capacitor
128						
129						
130	Input Bridge (BR1) and Fuse (F1)					
131	I^2t Rating			5.22	A^2*s	Minimum I^2t rating for fuse
132	Fuse Current rating			1.45	A	Minimum Current rating of fuse
133	VF			0.90	V	Input bridge Diode forward Diode drop
134	IAVG			0.90	A	Input average current at VBROWNOUT.
135	PIV_INPUT BRIDGE			392	V	Peak inverse voltage of input bridge

136	PCOND_LOSS_BRIDGE			0.768	W	Estimated Bridge Diode conduction loss
137	CIN			0.68	µF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
138	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
139	CIN_PLOSS			0.005	W	Input Capacitor Loss
140	RT1			9.79	ohms	Input Thermistor value
141	D_Precharge			1N5407		Recommended precharge Diode
142						
143						
144	PFS4 small signal components					
145	C_REF			1.0	µF	REF pin capacitor value
146	RV1			4.0	MOhms	Line sense resistor 1
147	RV2			6.0	MOhms	Line sense resistor 2
148	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
149	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
150	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80 µs) Pick the closest available capacitance.
151	C_VCC			1.0	µF	Supply decoupling capacitor
152	C_C			100	nF	Feedback C pin decoupling capacitor
153	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
154	PGT set resistor			320.5	kohm	Power good threshold setting resistor
155						
156						
157	Feedback Components					
158	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
159	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
160	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
161	RFB_4			155.5	kohms	Feedback network, lower divider resistor
162	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80 µs) Pick the closest available capacitance.
163	RFB_5			34.8	kohms	Feedback network: zero setting resistor
164	CFB_2			1000	nF	Feedback component- noise suppression capacitor
165						
166						
167	Loss Budget (Estimated at VACMIN)					
168	PFS Losses			1.441	W	Total estimated losses in PFS
169	Boost diode Losses			0.511	W	Total estimated losses in Output Diode
170	Input Bridge losses			0.768	W	Total estimated losses in input bridge module
171	Input Capacitor Losses			0.005	W	Total estimated losses in input capacitor
172	Inductor losses			0.569	W	Total estimated losses in PFC Choke

173	Output Capacitor Loss			0.154	W	Total estimated losses in Output capacitor
174	EMI choke copper loss			0.022	W	Total estimated losses in EMI choke copper
175	Total losses			3.470	W	Overall loss estimate
176	Efficiency			0.96		Estimated efficiency at VACMIN, full load
177						
178						
179	CAPZero component selection recommendation					
180	CAPZero Device			CAP200DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
181	Total Series Resistance (Rcapzero1+Rcapzero2)			1.046	MOhms	Maximum Total Series resistor value to discharge X-Capacitors
182						
183						
184	EMI filter components recommendation					
185	CX2			330	nF	X capacitor after differential mode choke and before bridge, ratio with Po
186	LDM_calc			461	µH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
187	CX1			330	nF	X capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	typical common mode choke value
189	LCM_leakage			30	µH	estimated leakage inductance of CM choke, typical from 30~60 µH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			431	µH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
193	DCR_LDM			0.030	Ohms	Total DCR of DM choke (or CM #2) for estimating copper loss
184	EMI filter components recommendation					
185	CX2			330	nF	X capacitor after differential mode choke and before bridge, ratio with Po
186	LDM_calc			461	µH	Estimated minimum differential inductance to avoid <10 kHz resonance in input current
187	CX1			330	nF	X capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	typical common mode choke value
189	LCM_leakage			30	µH	estimated leakage inductance of CM choke, typical from 30 ~ 60 µH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			431	µH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss

193	DCR_LDM			0.030	Ohms	Total DCR of DM choke (or CM #2) for estimating copper loss
184	EMI filter components recommendation					
185	CX2			330	nF	X capacitor after differential mode choke and before bridge, ratio with Po
186	LDM_calc			461	μH	Estimated minimum differential inductance to avoid <10 kHz resonance in input current
187	CX1			330	nF	X capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	typical common mode choke value
189	LCM_leakage			30	μH	estimated leakage inductance of CM choke, typical from 30 ~ 60 μH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			431	μH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
193	DCR_LDM			0.030	Ohms	Total DCR of DM choke (or CM #2) for estimating copper loss
194						
195	Note: CX2 can be placed between CM chock and DM choke depending on EMI design requirement.					
196						

Table 3 – Boost Inductor Design Spreadsheet.

Note:

Row 90 warning (high current density) – verified passing efficiency and thermal performance.

8 Flyback Transformer Design Spreadsheet

1	**ACDC_InnoSwitch4-QR_Flyback_050624; Rev.1.0; Copyright Power Integrations 2024**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet**
2	APPLICATION VARIABLES					Design Title
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	390		390	V	Minimum DC input voltage
5	VIN_MAX	410		410	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Range of AC input voltage
7	LINEFREQ				Hz	AC Input voltage frequency
8	CAP_INPUT	66.0			μF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	3.125		3.125	A	Output current
12	POUT			75.00	W	Output power
13	EFFICIENCY	0.93		0.93		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
16						
17						
18						
19	**ILIMIT_MODE**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	INN4274		INN4274		Generic device code
22	DEVICE_CODE			INN4274C		Actual device code
23	POUT_MAX			80	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.62	Ω	Primary switch on time drain resistance at 100 °C
25	ILIMIT_MIN			1.953	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			2.100	A	Typical current limit of the primary switch

27	ILIMIT_MAX			2.247	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.12	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			600.0	V	Peak drain voltage on the primary switch during turn-off. A 30V leakage spike voltage is assumed
31						
32						
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	94000		94000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	160.0		160.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			390.00	V	Valley of the minimum input AC voltage at full load
38	KP			1.55		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			DCM		Mode of operation
40	DUTYCYCLE			0.209		Primary switch duty cycle
41	TIME_ON			2.70	µs	Primary switch on-time
42	TIME_OFF			8.44	µs	Primary switch off-time
43	LPRIMARY_MIN			442.4	µH	Minimum primary inductance
44	LPRIMARY_TYP			465.6	µH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			488.9	µH	Maximum primary inductance
47						
48	PRIMARY CURRENT					
49	IPEAK_PRIMARY			2.176	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.201	A	Primary switch average current
52	IRIPPLE_PRIMARY			2.176	A	Primary switch ripple current
53	IRMS_PRIMARY			0.540	A	Primary switch RMS current
54						
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			14.794	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal

58	IRMS_SECONDARY			5.732	A	Secondary winding RMS current
59						
60						
61						
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	CORE SELECTION					
64	CORE	EQ25		EQ25		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE			EQ25-3C96		Core code
66	AE	89.70		89.70	mm^2	Core cross sectional area
67	LE	34.40		34.40	mm	Core magnetic path length
68	AL			4400	nH/turns^2	Ungapped core effective inductance
69	VE	2872.0		2872.0	mm^3	Core volume
70	BOBBIN			EQ25 - 1 (P4-S0)		Bobbin name
71	AW	18.07		18.07	mm^2	Window area of the bobbin
72	BW	4.25		4.25	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
74						
75	PRIMARY WINDING					
76	NPRIMARY			34		Primary turns
77	BPEAK			3757	Gauss	Peak flux density
78	BMAX			3450	Gauss	Maximum flux density
79	BAC			1725	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			403	nH/turns^2	Typical gapped core effective inductance
81	LG			0.254	mm	Core gap length
82						
83	PRIMARY BIAS WINDING					
84	NBIAS_PRIMARY			4		Primary bias winding number of turns
85						
86	SECONDARY WINDING					
87	NSECONDARY	5		5		Secondary winding number of turns
88						
89	SECONDARY BIAS WINDING					
90	NBIAS_SECONDARY			2		Secondary bias winding number of turns
91						

92						
93						
94	**PRIMARY COMPONENTS SELECTION**					
95	LINE UNDERVOLTAGE					
96	BROWN-IN REQURED	112		112	V	Required AC RMS/DC line voltage brown-in threshold
97	RLS			4.1	MΩ	Connect two 4.32 MOhm resistors to the V-pin for the required UV/OV threshold
98	BROWN-IN ACTUAL			94.4V – 114.5V	V	Actual AC RMS/DC brown-in range
99	BROWN-OUT ACTUAL			83.9V – 104.2V	V	Actual AC RMS/DC brown-out range
100						
101	LINE OVERVOLTAGE					
102	OVERVOLTAGE_LINE			430.9V – 489.3V	V	Actual AC RMS/DC line over-voltage range
103						
104	PRIMARY BIAS DIODE					
105	VBIAS_PRIMARY	15.0		15.0	V	Rectified primary bias voltage
106	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
107	VREVERSE_BIASDIODE_PRIMARY			67.44	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
108	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
109	CBPP			0.47	µF	BPP pin capacitor
110						
111						
112						
113	**SECONDARY COMPONENTS**					
114	RFB_UPPER	150.00		150.00	kΩ	Upper feedback resistor (connected to the first output voltage)
115	RFB_LOWER			8.25	kΩ	Lower feedback resistor
116	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
117						
118	SECONDARY BIAS DIODE					
119	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
120	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
121	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
122	VREVERSE_BIASDIODE_SECONDARY			29.12	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
123	CBIAS_SECONDARY			10	µF	Bias winding rectification capacitor
124	CBPS			2.20	µF	BPP pin capacitor
125						
126						
127	MULTIPLE OUTPUT PARAMETERS					

128	OUTPUT 1					
129	VOUT1			24.00	V	Output 1 voltage
130	IOUT1			3.13	A	Output 1 current
131	POUT1			75.00	W	Output 1 power
132	IRMS_SECONDARY1			5.732	A	Root mean squared value of the secondary current for output 1
133	IRIPPLE_CAP_OUTPUT1			4.805	A	Current ripple on the secondary waveform for output 1
134	NSECONDARY1			5		Number of turns for output 1
135	VREVERSE_RECTIFIER1			84.29	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
136	SRFET1	Auto		AONS62922		Secondary rectifier (Logic MOSFET) for output 1
137	VF_SRFET1			0.022	V	SRFET on-time drain voltage for output 1
138	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
139	RDSON_SRFET1			7.0	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1
140						

Table 4 – Flyback Transformer Design Spreadsheet.

9 Flyback Transformer Specification

9.1 Electrical Diagram

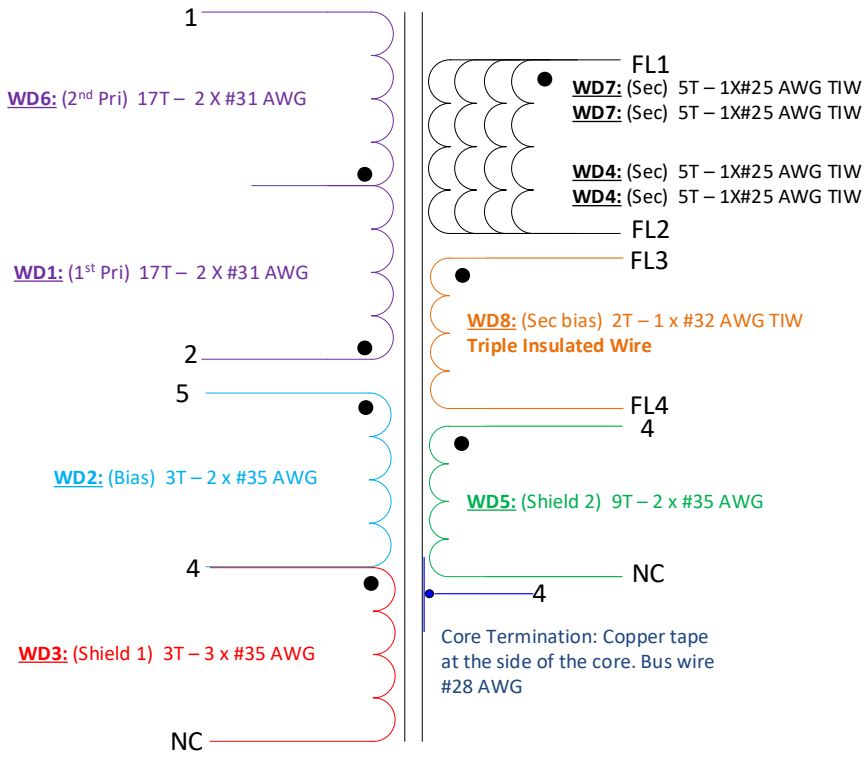


Figure 8 – Transformer Schematic.

9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	465 µH ±5%
Primary Leakage Inductance	Measure inductance across Pin 1-2 with all other windings shorted	10 µH ±5%

Table 5 – Transformer Electrical Specification.

9.3 Materials

Item	Description
[1]	Core: PI P/N: 99-00122-00 (EQ25/LP-3C95)
[2]	Bobbin: PI P/N: 25-01249-00 (Bobbin, EQ25, 6 pins, 5pri, 1sec) Manufacturer PN: EQ25-11.2-6P-THL-A5-11 Manufacturer: TBI
[3]	Magnet wire: #31 AWG, double coated.
[4]	Magnet wire: #35 AWG, double coated.
[5]	Bus wire: #28 AWG
[6]	TIW Wire: #25 AWG Tripple Insulated
[7]	TIW Wire: #32 AWG Tripple Insulated
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 4.5 mm width
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 9 mm width
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 20 mm Width
[11]	Copper Foil Tape
[12]	Varnish: Dolph BC-359

Table 6 – Transformer Materials.

9.4 Transformer Build Diagram

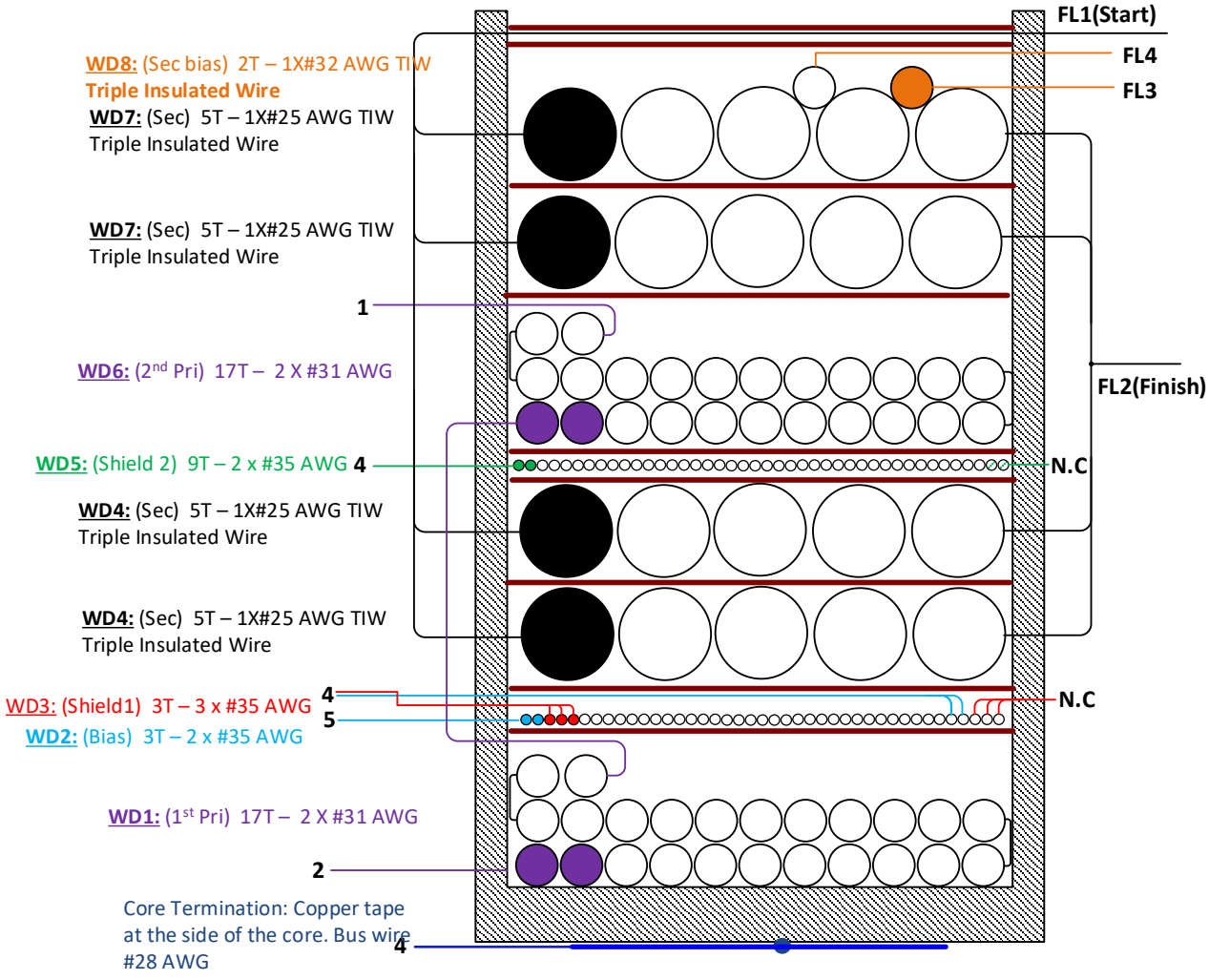
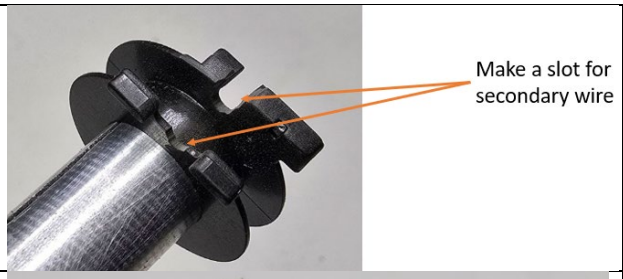
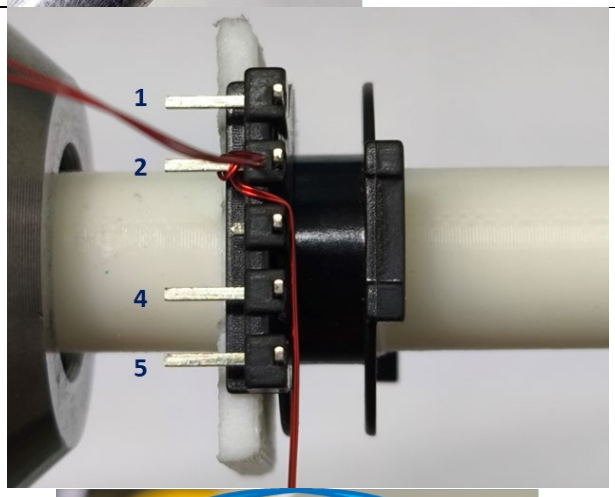
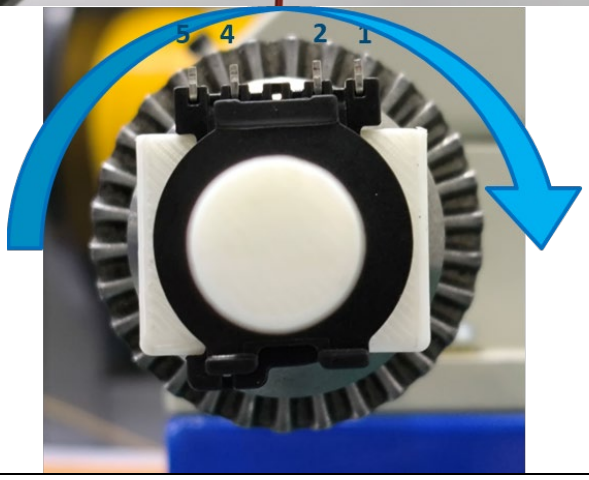
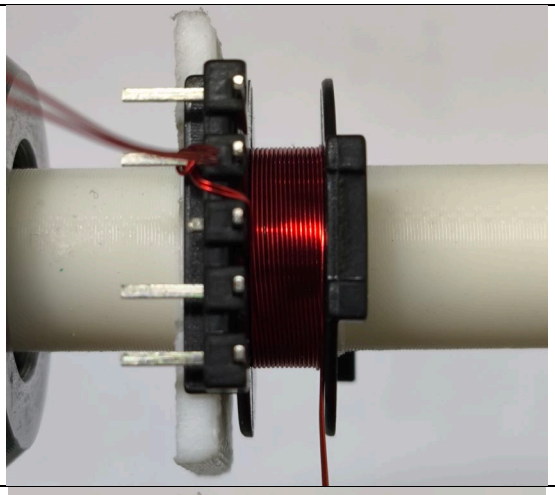
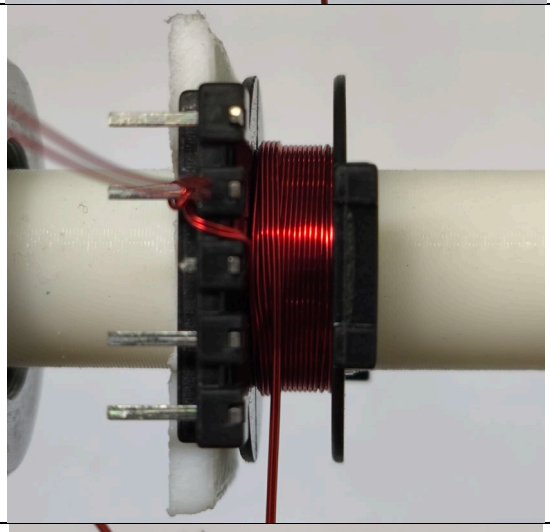
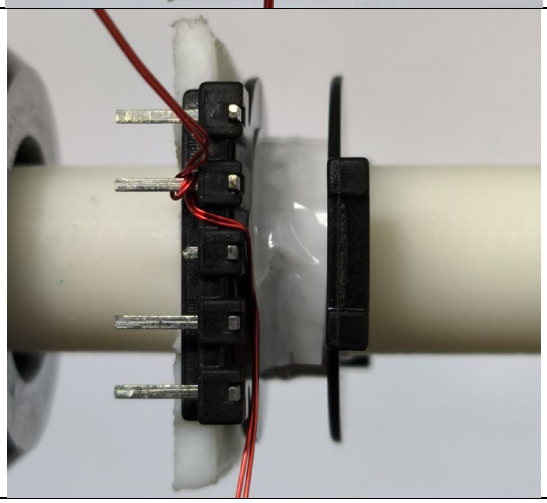
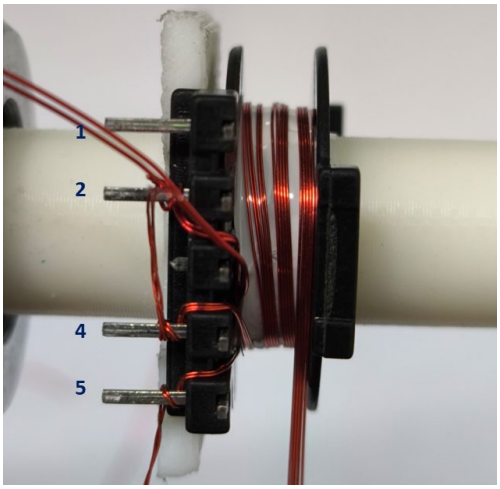
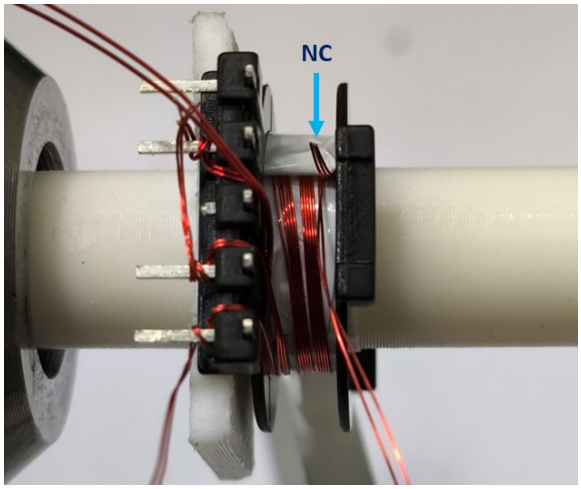
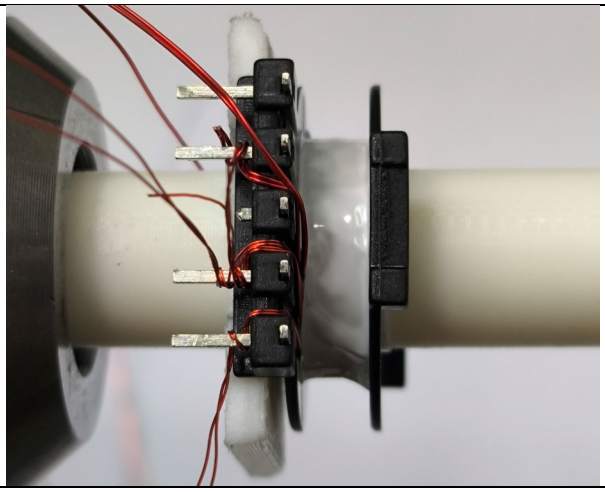


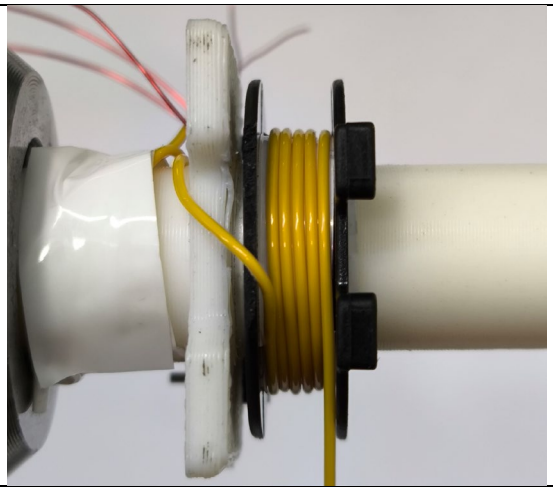
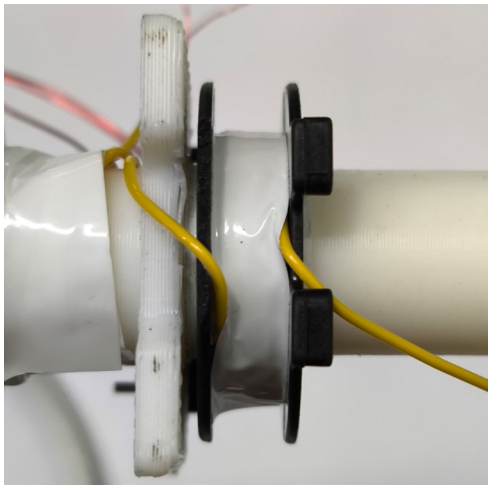
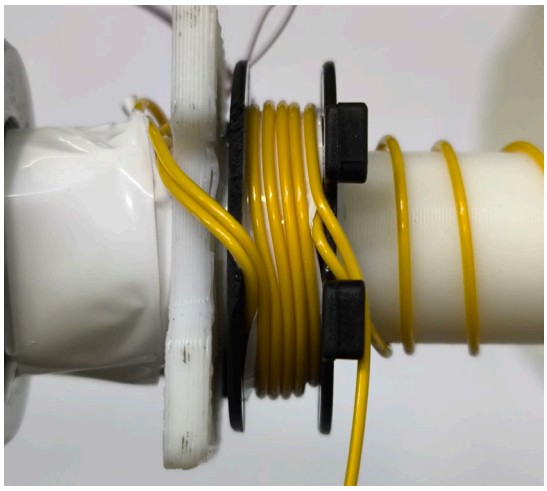
Figure 9 – Transformer Build Diagram.

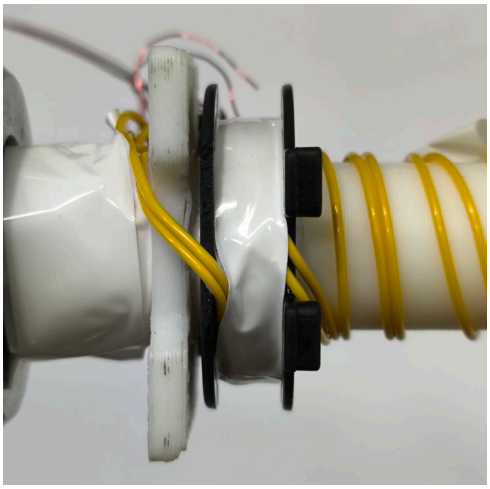
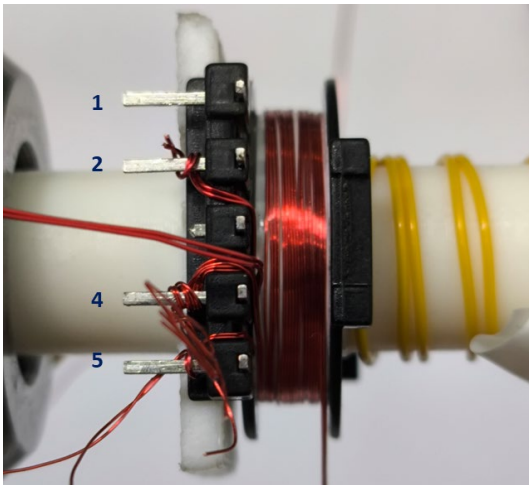
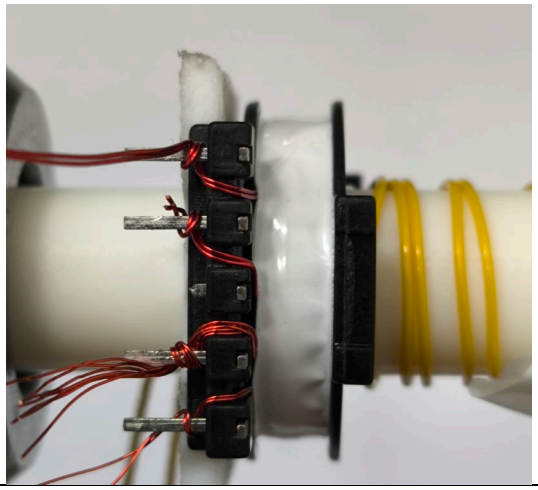
9.5 Winding Illustrations

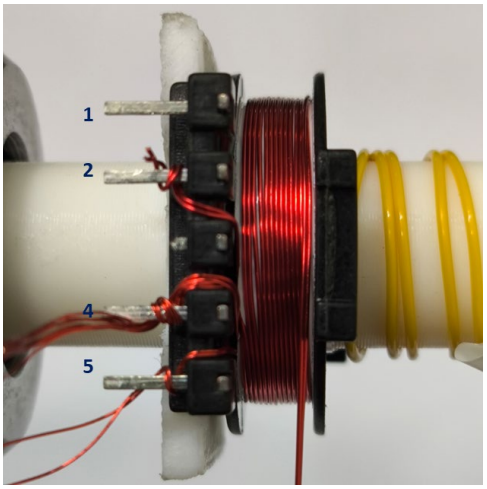
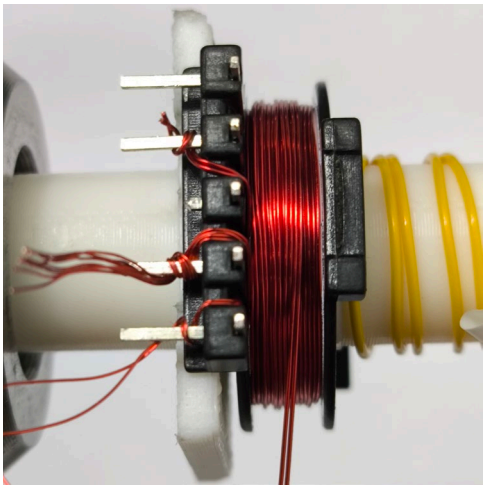
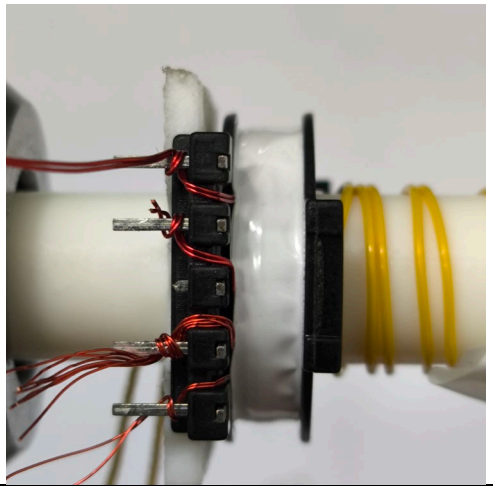
Bobbin Preparation		Remove pin 6 and make a slot for secondary wires as shown.
WD1 **1st Primary**	 	Remove pin 3. Bobbin is oriented on winder jig such that pins 1-5 is on the left side. The winding direction of jig is clockwise.

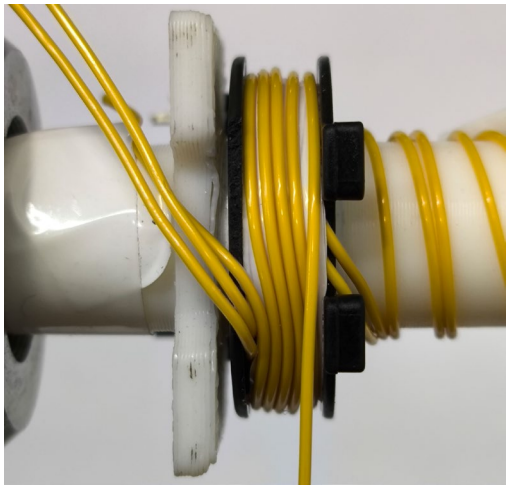
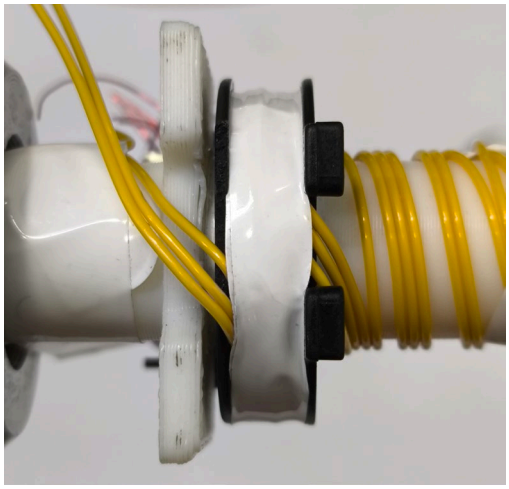
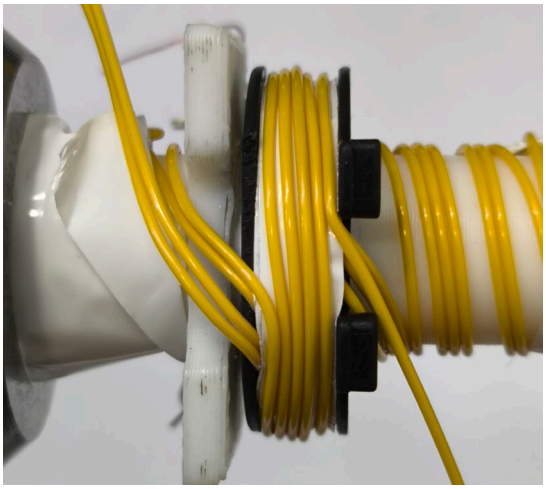
		Start at pin 2 and wind 7 bifilar turns of wire Item [3] from left to right.
		Continue winding 7 bifilar turns of wire Item [3] from right to left. Then wind 3 turns from left to right. Bring bifilar wire Item [3] to the left and keep it floating.
Insulation		1 layer of tape Item [8].

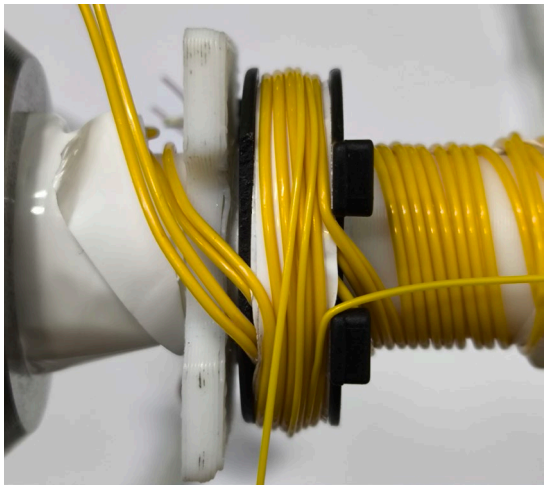
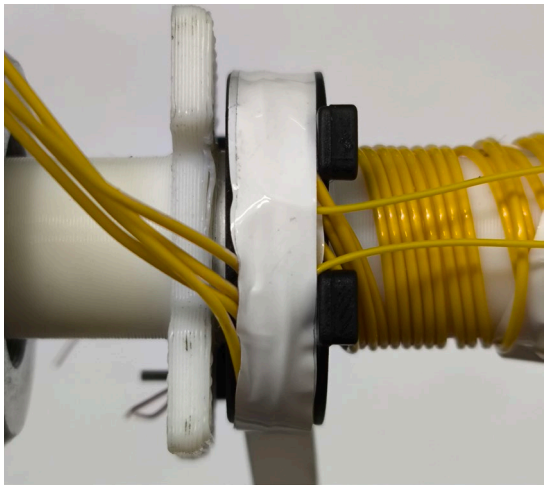
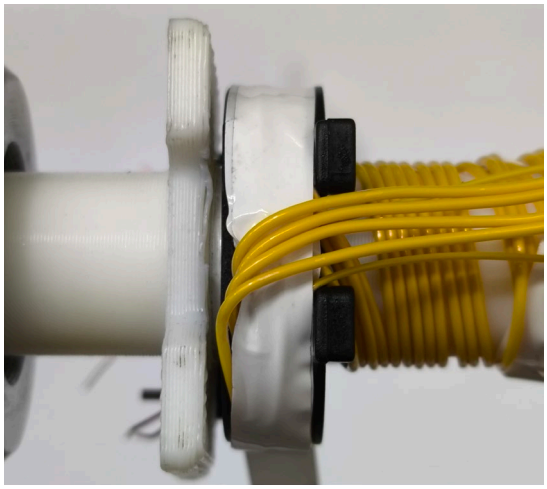
WD2: Bias & WD3: Shield1		Use 2 wires Item [4] start at pin 5 for Bias winding, also use 3 wires same Item [4] start at pin 4 for Shield1 winding. Wind all 3 wires in parallel.
		At the 3rd turn: - bring 2 wires for Bias winding to the left and terminate at pin 4 - For Shield1 winding, cut short 3 wires as no connect
Insulation		1 layer of tape Item [8].

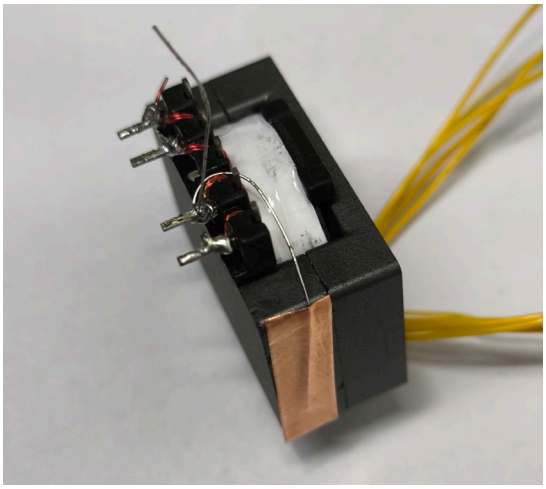
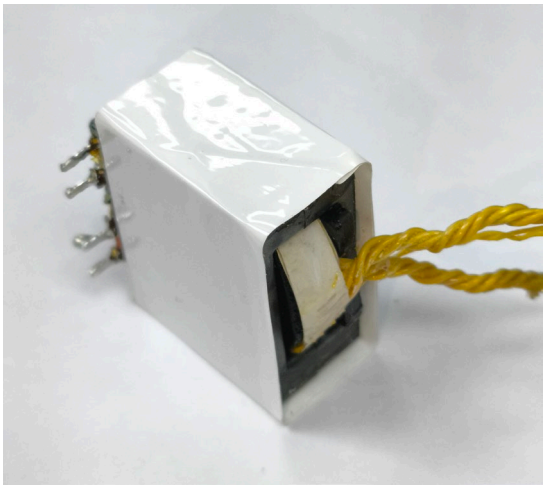
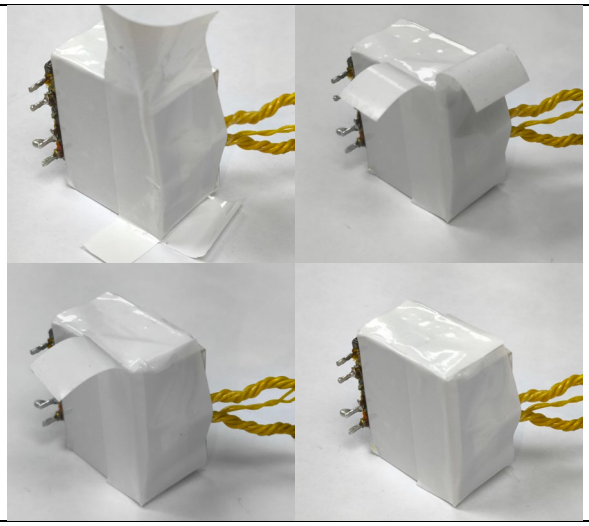
WD4 **Secondary**		Use wire Item [6]. Start at the left slot of the secondary side, leaving at least 32 mm floating and mark it as FL1. Wind 5 turns in 1 layer from left to right and leave at least 22 mm floating at the right slot of the secondary side and mark it as FL2.
Insulation		1 layer of tape Item [8].
WD4 **Secondary**		Wind another layer identical to the previous one using 5 turns of wire Item [6].

Insulation		1 layer of tape Item [8].
WD5 **Shield2**		Start at pin 4, wind 9 bifilar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation		1 layer of tape Item [8].

WD6 **2nd Primary**		Use wire from the 1st Primary that was kept floating and wind 7 bifilar turns of wire Item [3].
		Continue winding 6 bifilar turns of wire Item [3] from right to left. Then wind 4 turns from left to right. Bring bifilar wire Item [3] to the left and finish winding at pin 1.
Insulation		1 layer of tape Item [8].

WD7 **Secondary 2**		Use wire Item [6]. Start at the left slot of the secondary side, leaving at least 32 mm floating and mark it as FL1. Wind 5 turns in 1 layer from left to right and leave at least 22 mm floating at the right slot of the secondary side and mark it as FL2.
Insulation		1 layer of tape Item [8].
WD7 **Secondary 2**		Wind another layer identical to the previous one using 5 turns of wire Item [6].

WD8 **Secondary Bias**		Use wire Item [7]. Start at the right slot of the secondary side, leaving at least 22 mm floating, and mark it as FL3. Wind 2 turns from right to left, then bring the wire back to the right slot, leaving at least 22 mm floating, and mark it as FL4.
Insulation		1 layer of tape Item [8].
Secondary Wire Terminals		Take all the wires Item [6] from the left and bring it to the right. Add 2 layers of tape Item [8].

Core Gap and Grounding		Gap one of the core halves to achieve 465 µH of primary inductance, measured across pin 1 and pin 2. Apply a small strip of Item [11] on the side of the transformer and connect to pin 4 using wire Item [5] for ground termination.
Finish		Apply 2 layers of tape Item [10] firmly around the two cores. Tape Item [10] is slightly wider than the core. There should be 1 mm excess tape on both sides.
		Use tape Item [10] to cover the secondary side with excess tape at the bottom of the transformer.

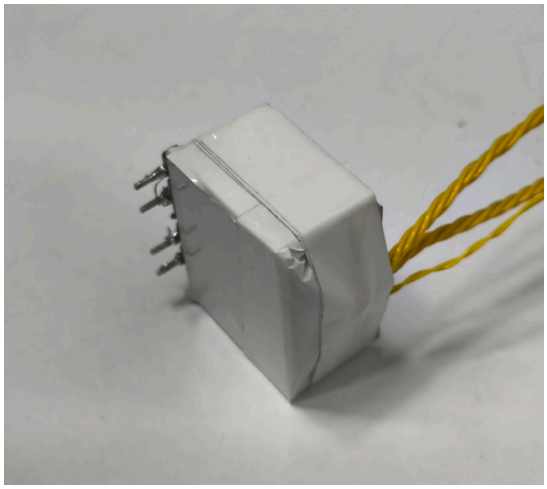
		Apply 2 layers of tape Item [9] around the transformer. Twist together the 4 strands of FL1 and do the same with the 4 strands of FL2. Twist together FL3 and FL4. Cut the floating wires to 20 mm. Varnish the transformer with Item [12], then cure the varnish in an oven at 100 °C for 1 hour.

Table 7 – Transformer Winding Illustrations.

10 Boost Inductor Specification

10.1 Electrical Diagram

Figure 10 – Boost Inductor Electrical Diagram.

10.2 Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 4	1100 µH ±5%

Table 8 – Boost Inductor Electrical Specification.

10.3 Materials

Item	Description
[1]	Core: PI P/N: 99-00122-00 (EQ25/LP-3C95)
[2]	Bobbin: PI P/N: 25-01249-00 (Bobbin, EQ25, 6 pins, 5 pri, 1 sec) Manufacturer PN: EQ25-11.2-6P-THL-A5-11 Manufacturer: TBI
[3]	Magnet wire: 10/#38 or 10/0.1 mm Unserved Litz Wire
[4]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 4.5 mm width.
[5]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 20 mm width.
[6]	Varnish: Dolph BC-359.

Table 9 – Boost Inductor Materials.

10.4 Build Diagram

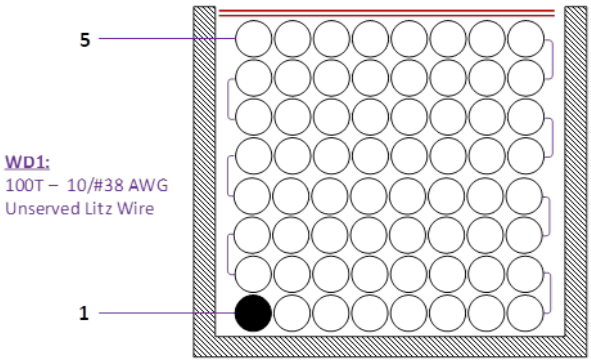
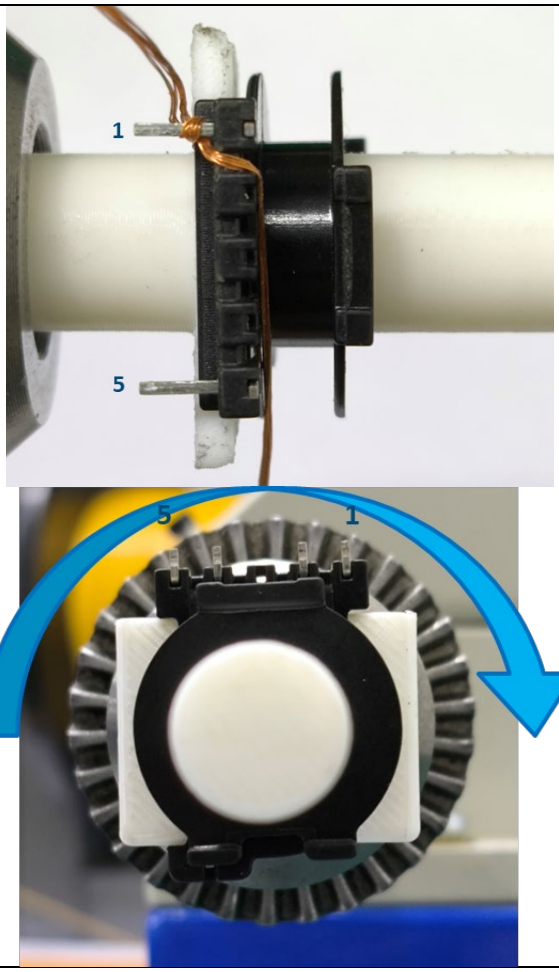


Figure 11 – Boost Inductor Build Diagram.

10.5 Winding Illustrations

WD1		Remove pins 2-4 and pin 6. Bobbin is oriented on winder jig such that pins 1-5 is on the left side. The winding direction of jig is clockwise.

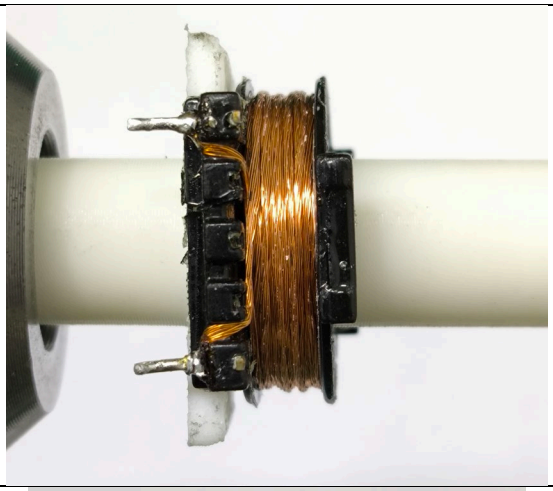
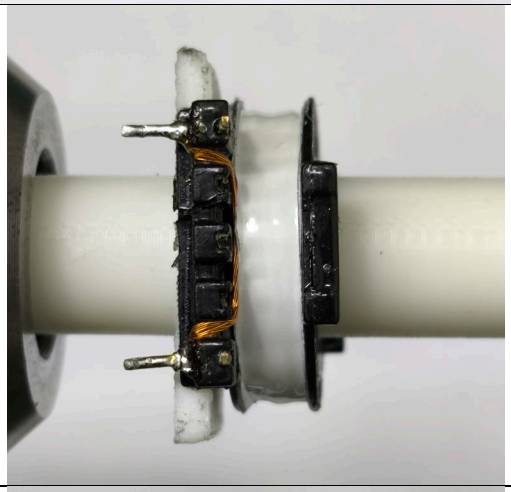
		Start at pin 1 and wind 100 turns of wire Item [3] from left to right, then right to left, and so on.
Insulation		2 layers of tape Item [4].
Finish		Gap one of the core halves to achieve 1100 µH inductance, measured across pin 1 and pin 5. Apply 2 layers of tape Item [5] around the transformer. Tape Item [5] is slightly wider than the core. There should be 1 mm excess tape on both sides. Varnish the transformer with Item [6], then cure the varnish in an oven at 100 °C for 1 hour.

Table 10 – Boost Inductor Winding Illustrations.

11 L1 (32-00466-00): Custom HF Input CMC

11.1 Electrical Diagram

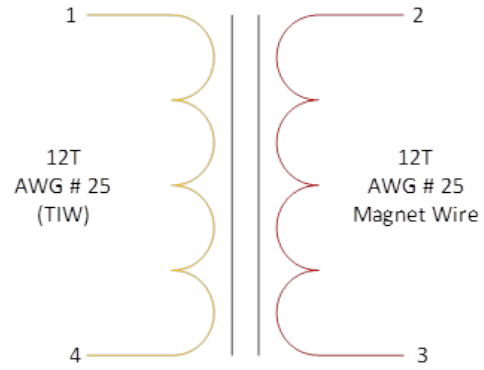


Figure 12 – **Input CMC** Electrical Diagram.

11.2 Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and pin 4 or pin 2 and pin 3 with all other windings open.	330 µH
Tolerance	Tolerance of Primary Inductance.	±20%

Table 11 – **Input CMC Electrical Specification**.

11.3 Materials

Item	Description
[1]	Toroid Core: 12.0 mm O.D. 6.0 mm Th 4.0 mm ID (Manufacturer PN: GL50 T 12X6X4-C; Manufacturer: Bipolar Electronics TW)
[2]	Magnet Wire (Double Coated): #25 AWG.
[3]	TIW (Tripple Insulated wire) Wire: #25 AWG.

Table 12 – **Input CMC Materials**.

11.4 Inductor Build Diagram

Figure 13 – Input CMC Build Diagram.

11.5 Inductor Construction

1. Winding 1 – Wind 12 turns of Item [2] and [3] in bifilar wound as shown in figure 13.

12 Case and Gap Pad

12.1 Case Dimensions

Dimensions are in mm and inches. Case material: Polycarbon / PC+ (can withstand at least 120 °C without deformation).

12.1.1 Enclosure Top Half

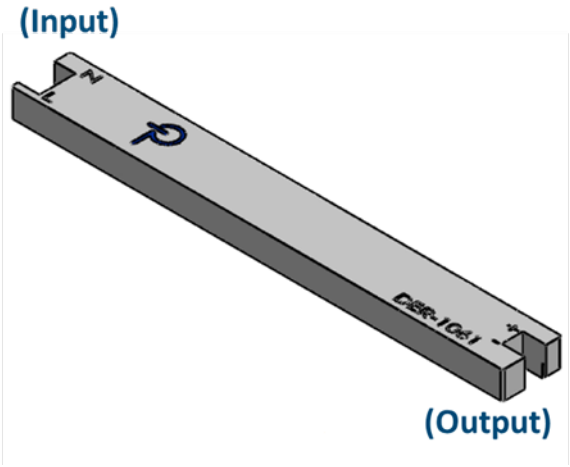


Figure 14 – Enclosure Top Half Dimensions (Isometric View).

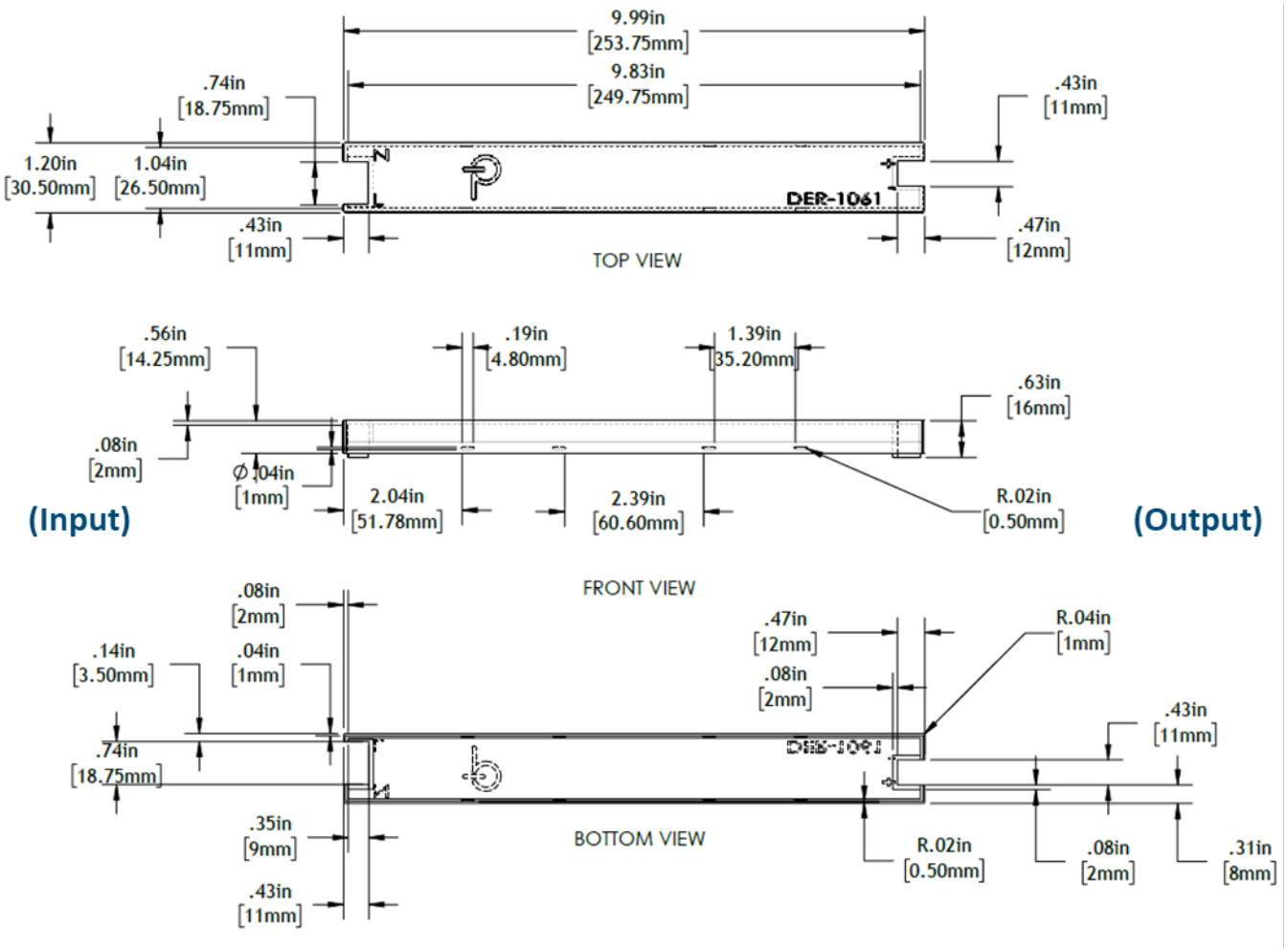


Figure 15 – Enclosure Top Half Dimensions (Top, Front, and Bottom View).

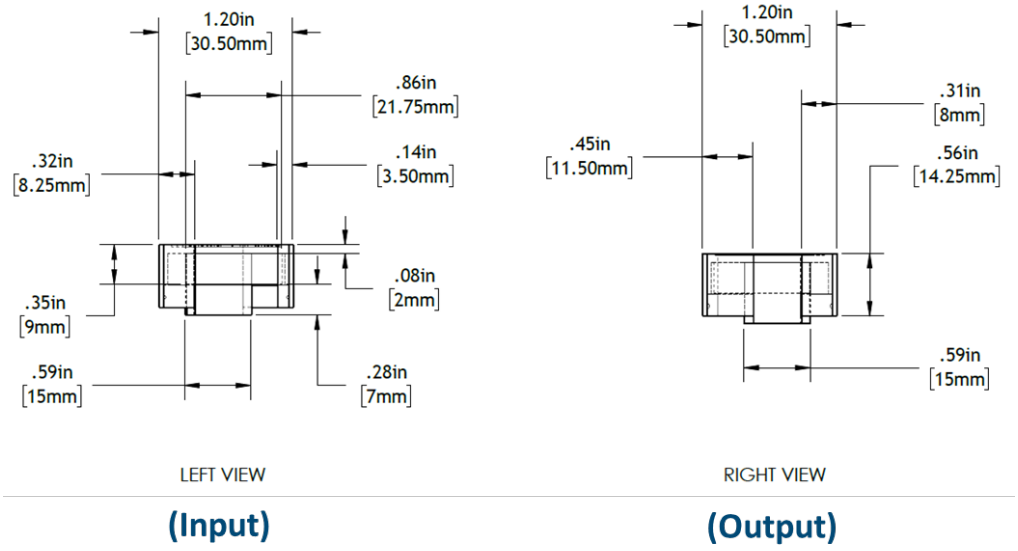


Figure 16 – Enclosure Top Half Dimensions (Side View).

12.1.2 Enclosure Bottom Half

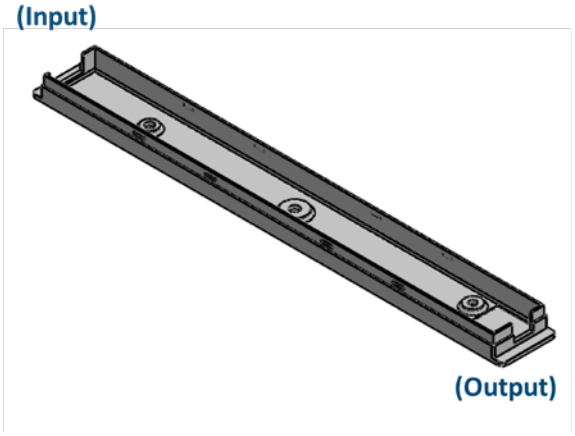


Figure 17 – Enclosure Bottom Half Dimensions (Isometric View).

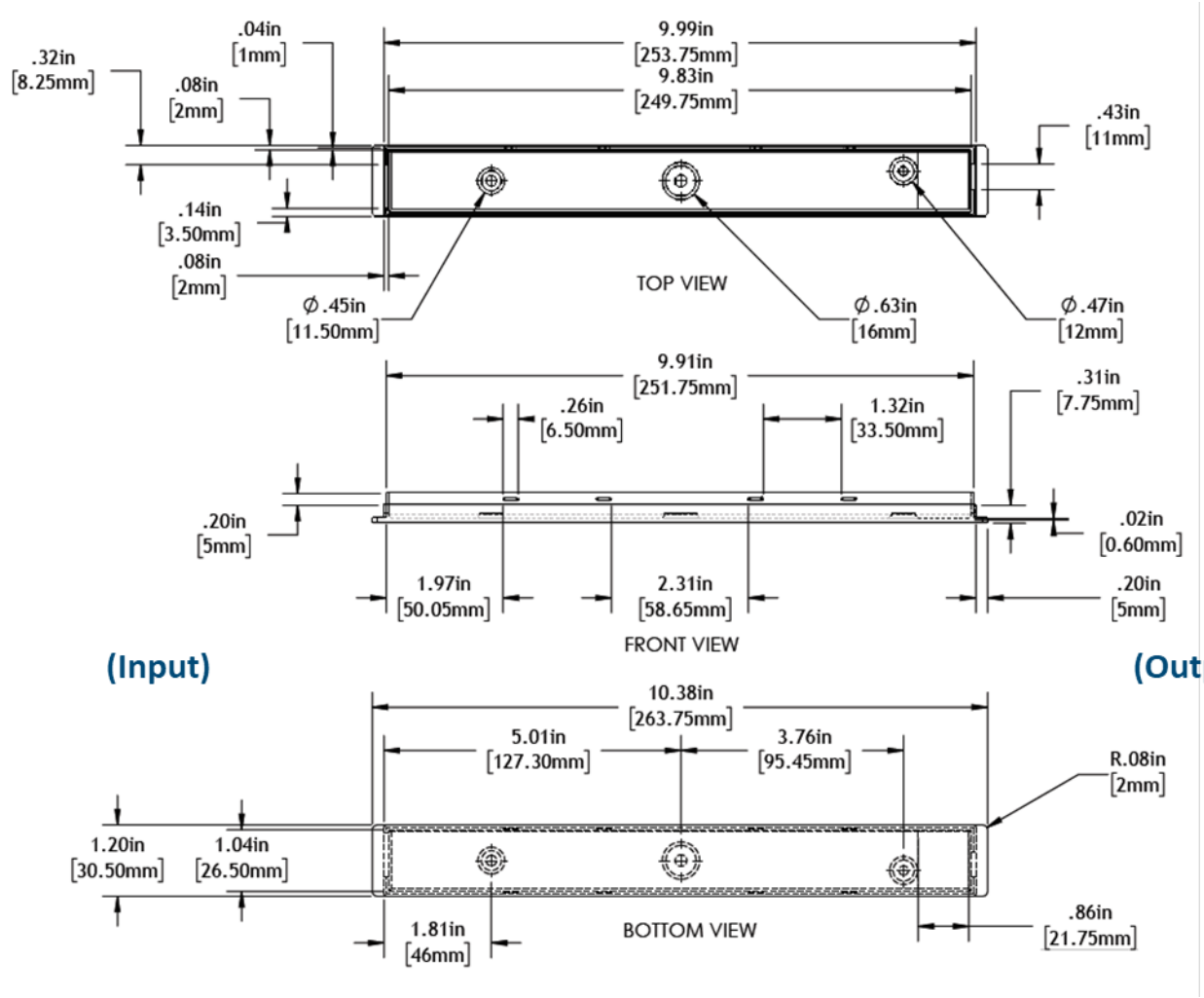


Figure 18 – Enclosure Bottom Half Dimensions (Top, Front, and Bottom View).

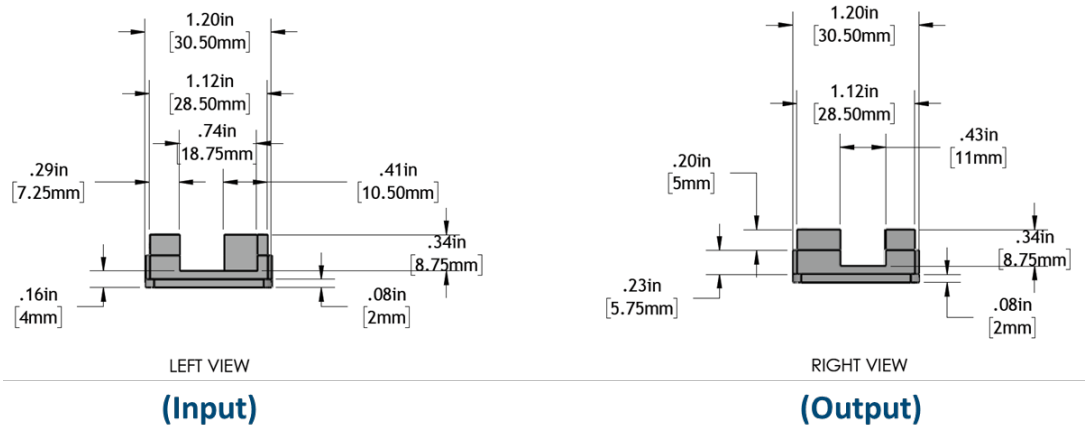


Figure 19 – Enclosure Bottom Half Dimensions (Side View).

12.2 Gap Pad

2 mm thick gap pad (Manufacturer PN: COH-1706-200-20) was placed on top of U3-Innoswitch (32 mm x 25 mm) and on top of T2 the flyback transformer (45 mm x 25 mm).

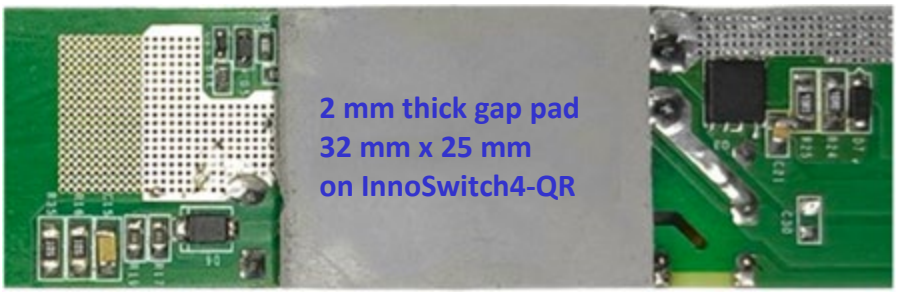
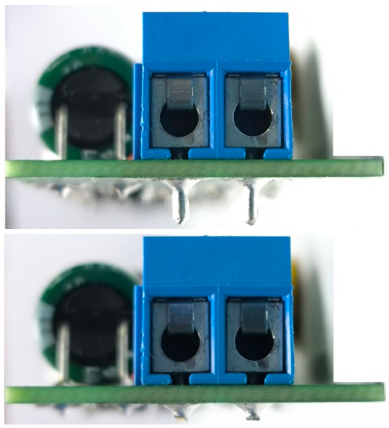
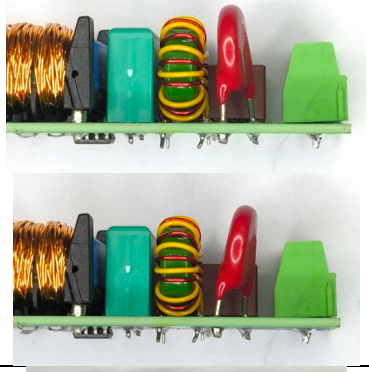
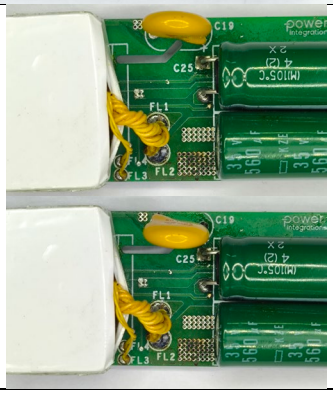


Figure 20 – INS1: InnoSwitch4-QR IC Gap Pad Setup on DER-1061 (Bottom View).

Figure 21 – INS2: Flyback TRF Gap Pad Setup on DER-1061 (Top View).

12.3 Assembly Illustrations

	Trim excess leads of J1 (output)
	Bend RV1 slightly toward J2 (input)
	Bend C19 slightly toward FL1 and FL2

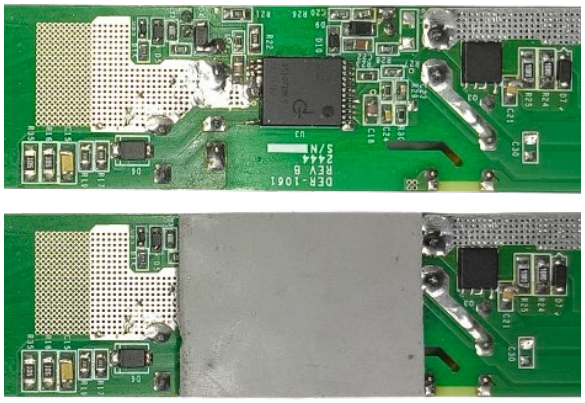
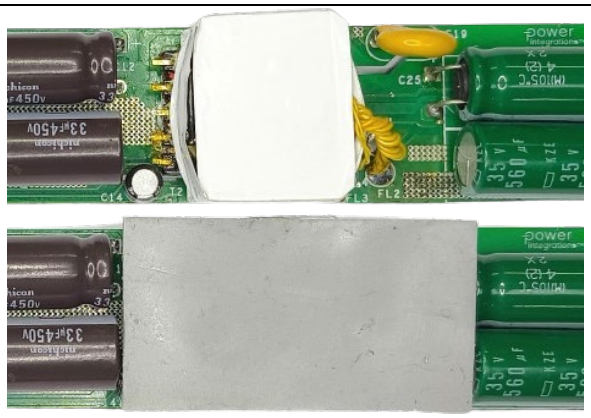
	Place INS1 on top of InnoSwitch4-QR IC. Place board with gap pad on bottom half of the case.
	Place INS2 on top of Flyback TRF Snap top half together with bottom half of the case.

Table 13 – Case and Gap Pad Assembly Instructions.

13 Performance Data

Performance data collected at room temperature, with voltages taken on the input and output terminals of the PCB unless noted otherwise.

13.1 Efficiency

13.1.1 Full Load Efficiency vs Input Voltage

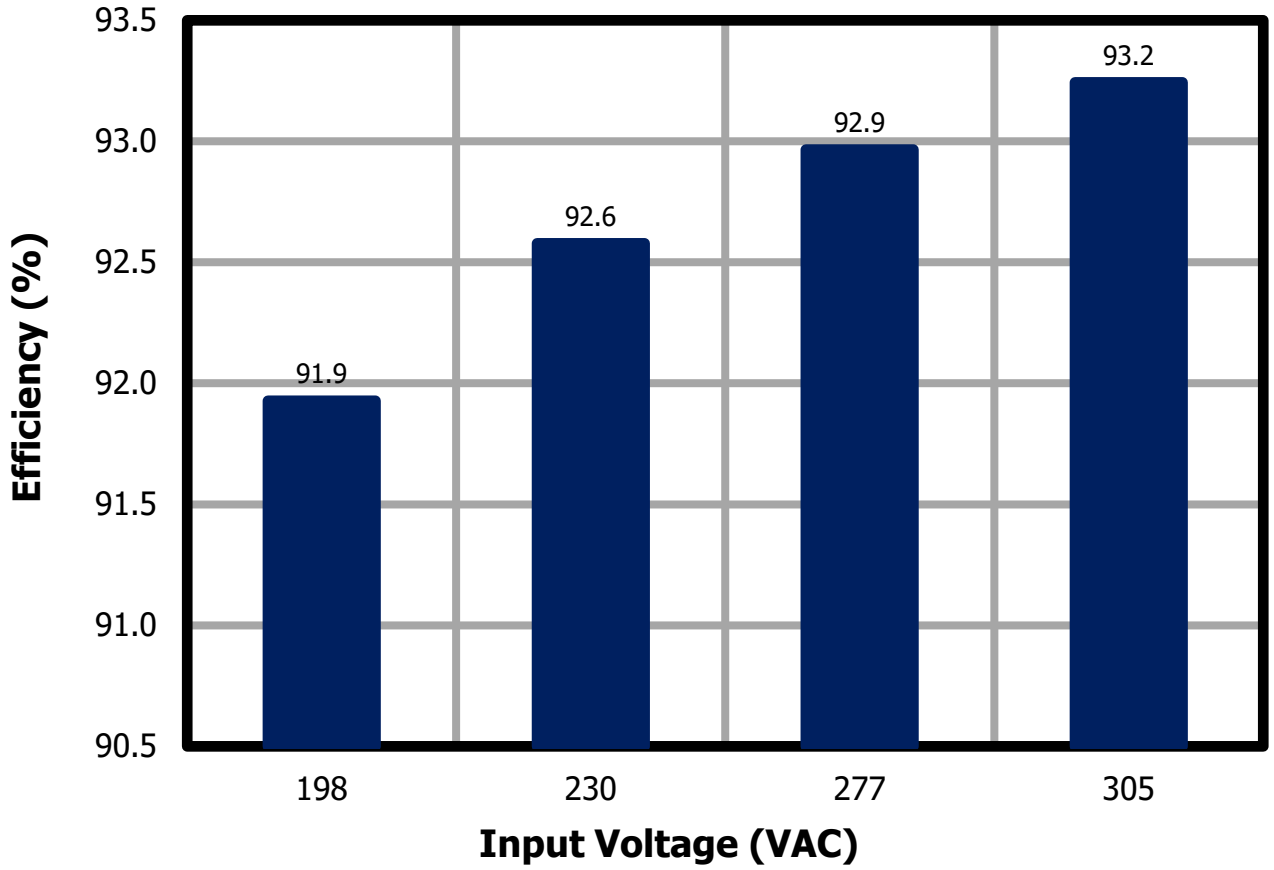


Figure 22 – Full Load Efficiency vs. Input Line Voltage.

13.1.2 Efficiency vs Output Load

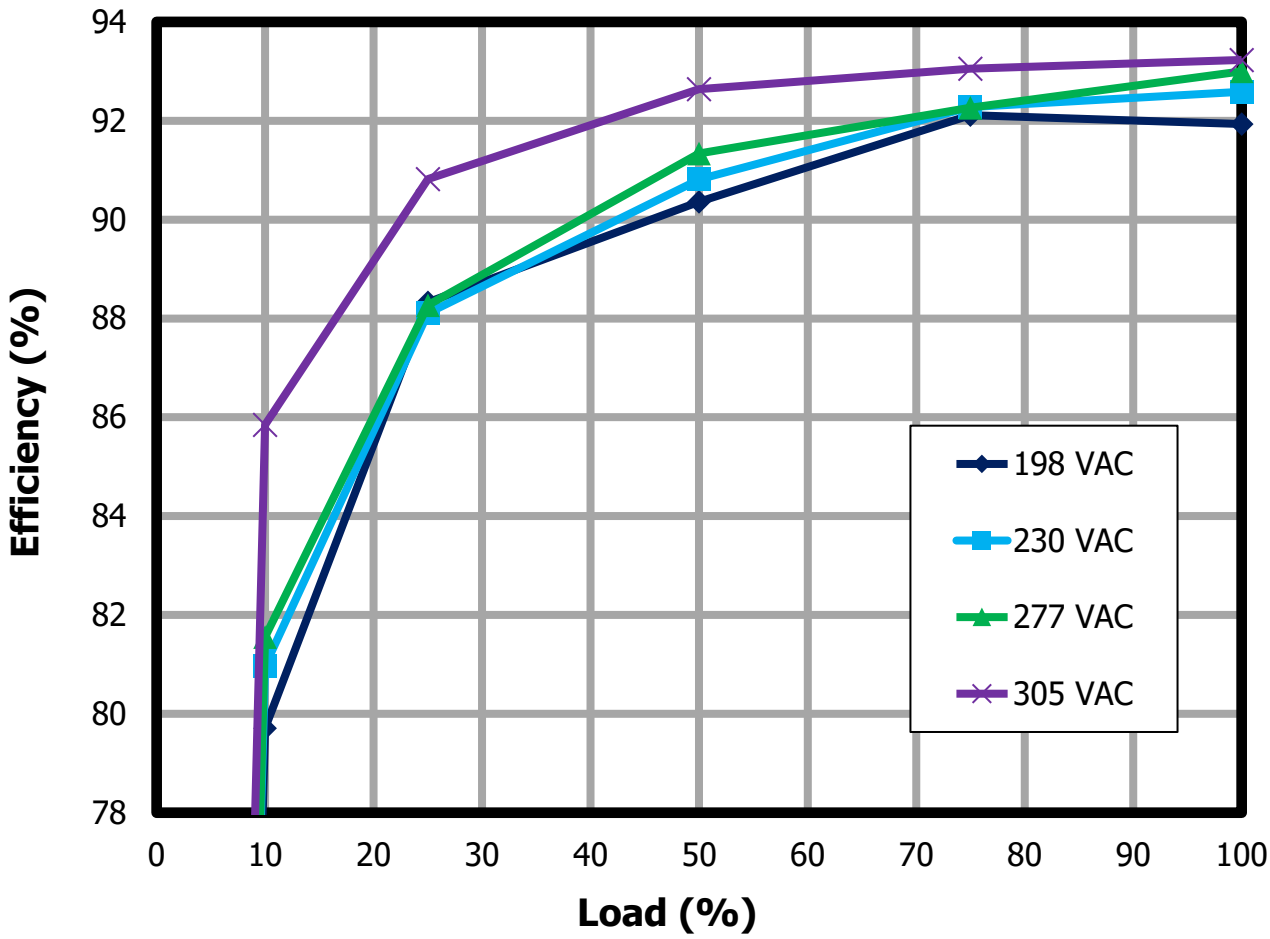


Figure 23 – Efficiency vs Load.

13.2 Power Factor

13.2.1 Power Factor vs Input Line Voltage at Full Load

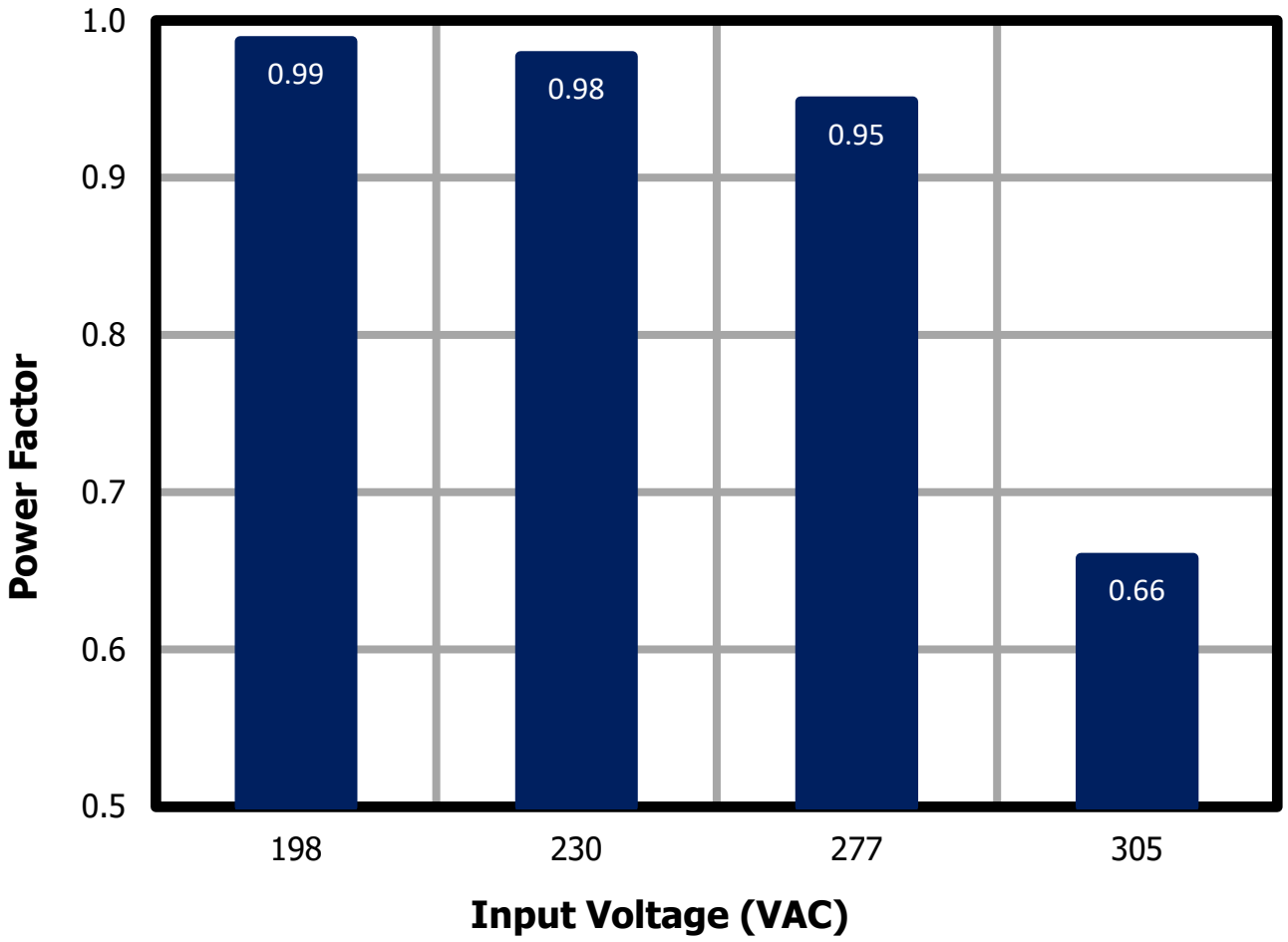


Figure 24 – Power Factor vs Input Line, 24 V Full Load.

13.2.2 Power Factor vs Output Load

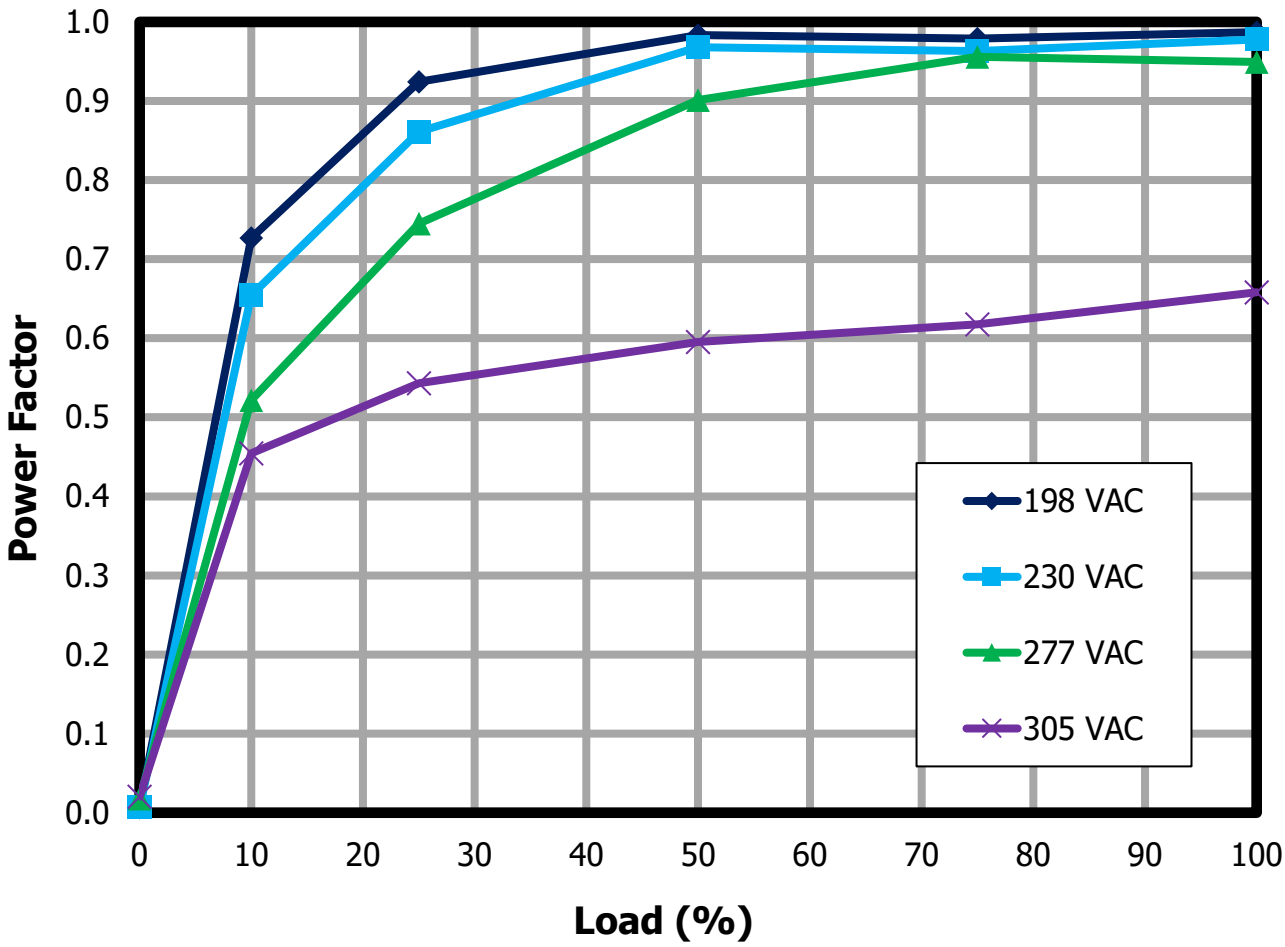


Figure 25 – Power Factor vs Load.

13.3 Total Harmonic Distortion (THD)

13.3.1 Total Harmonic Distortion (THD) vs Input Line at Full Load

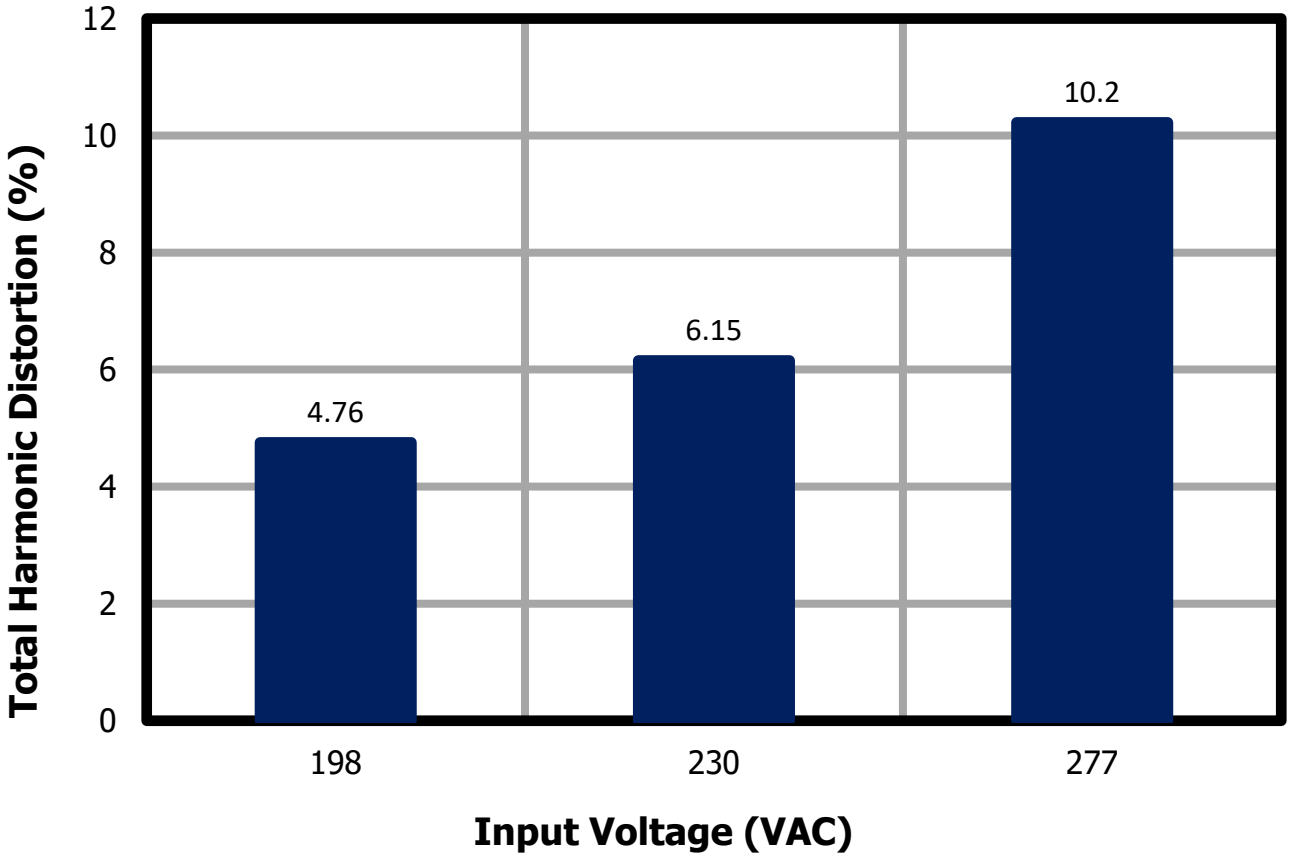


Figure 26 – THD vs Input Line, 24 V Full Load.

13.3.2 Total Harmonic Distortion (THD) vs Output Load

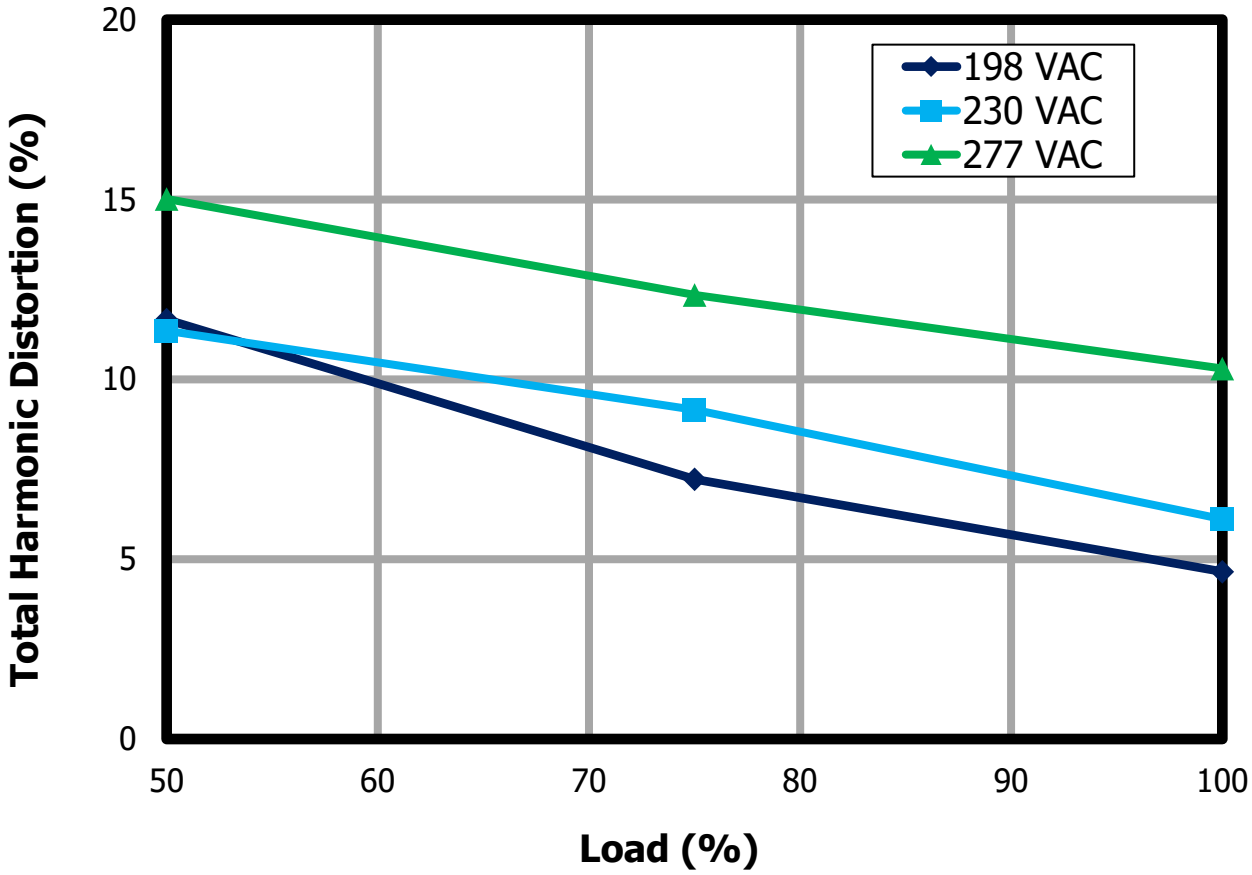


Figure 27 – THD vs Load.

13.4 Individual Harmonics Content at Full-Load

Individual current harmonics were shown to be below the Class C limit.

Set-up: Open frame unit.
Load: 24 V 3.13 A CC.
V_{IN}: 230 V 50 Hz.
Ambient Temperature: 25 °C.
Soak Time: 10 minutes.

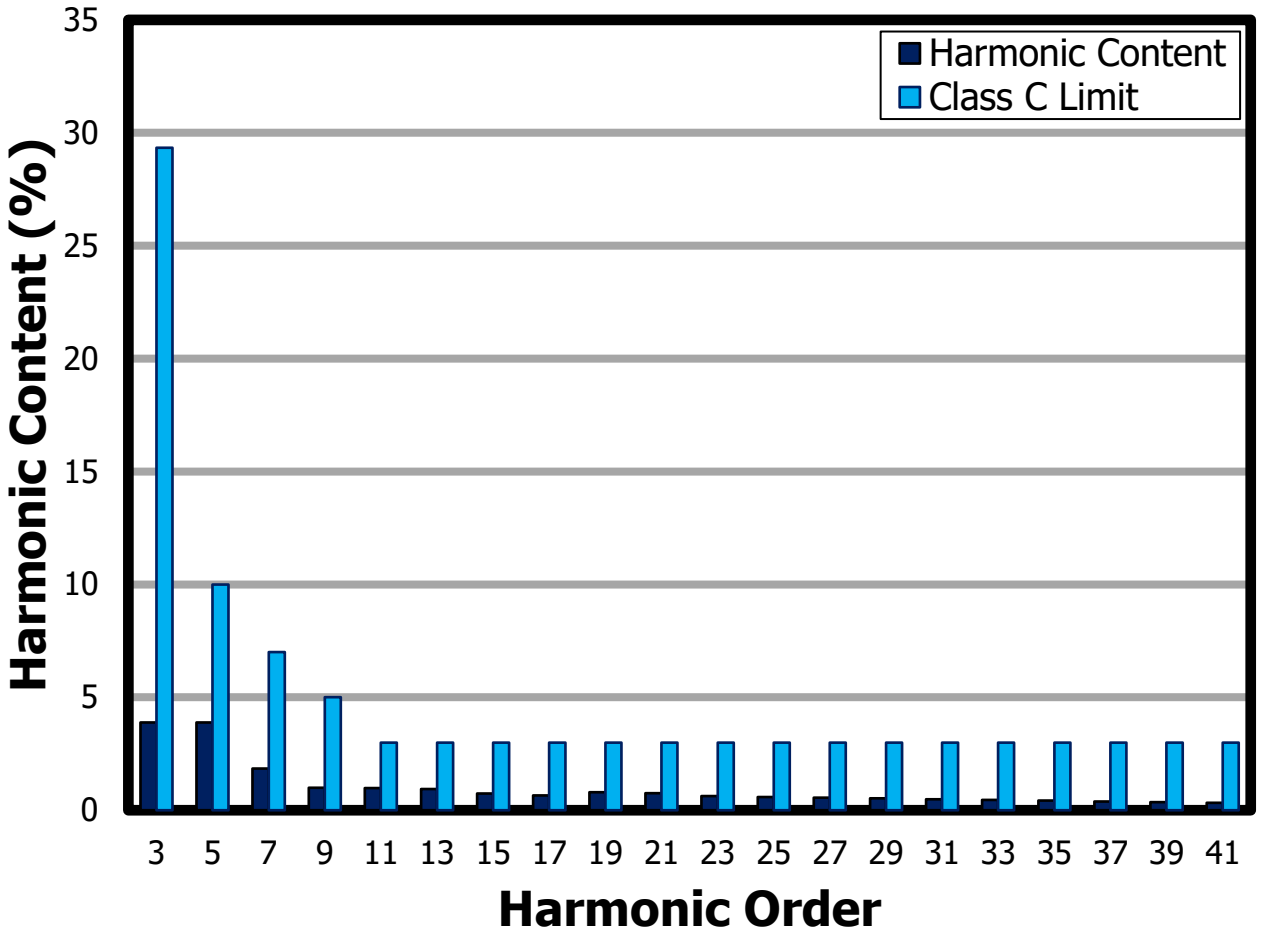


Figure 28 – Full Load Input Current Harmonics at 230 VAC 50 Hz.

Set-up: Open frame unit.
Load: 24 V 3.13 A CC.
V_{IN}: 277 V 50 Hz.
Ambient Temperature: 25 °C.
Soak Time: 10 minutes.

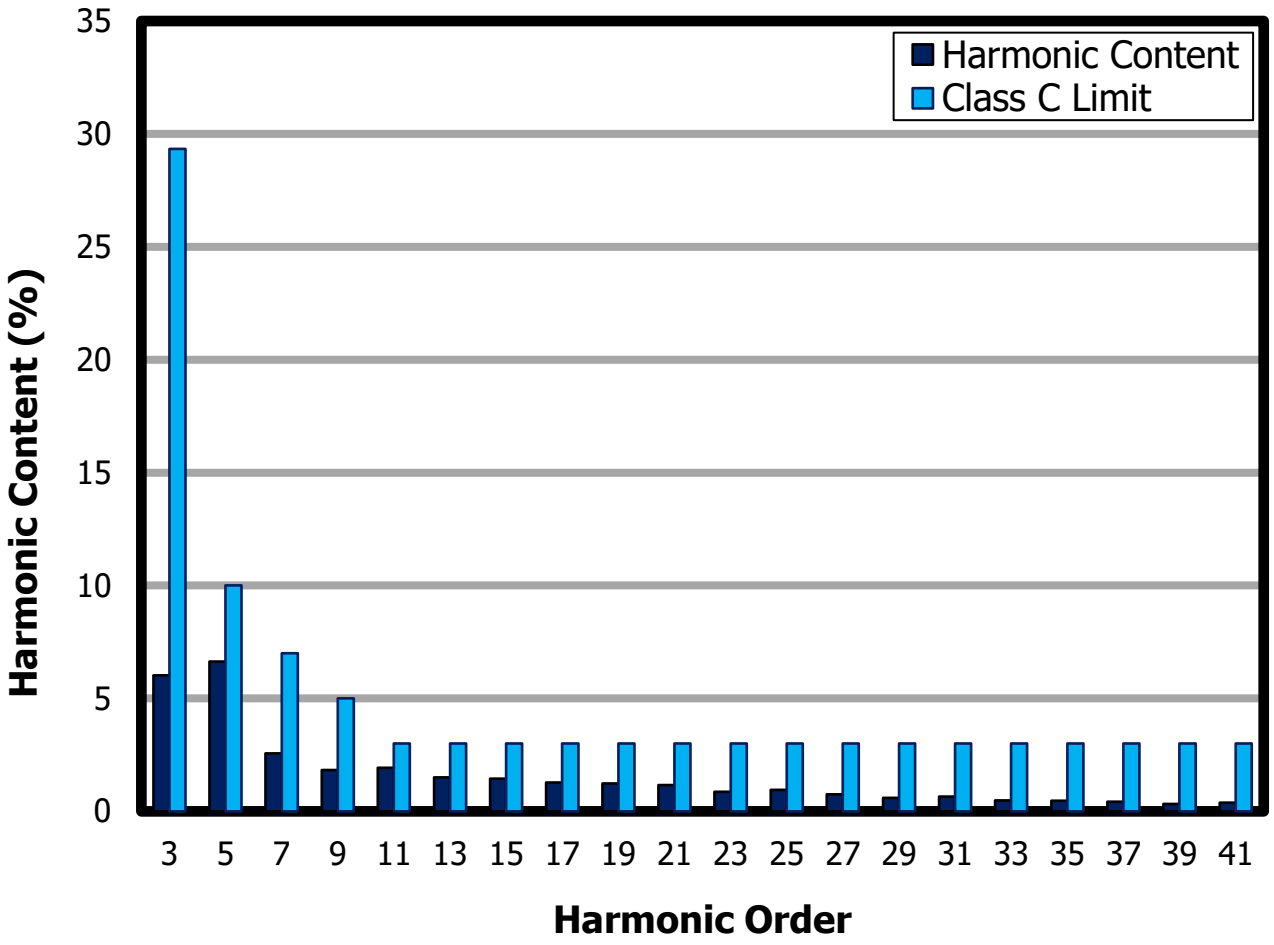


Figure 29 – Full Load Input Current Harmonics at 277 VAC 50 Hz.

13.5 Individual Harmonics Content at 25% Load

Individual current harmonics were shown to be below the Class C limit.

Set-up: Open frame unit.
Load: 24 V 781 mA CC.
V_{IN}: 230 V 50 Hz.
Ambient Temperature: 25 °C.
Soak Time: 10 minutes.

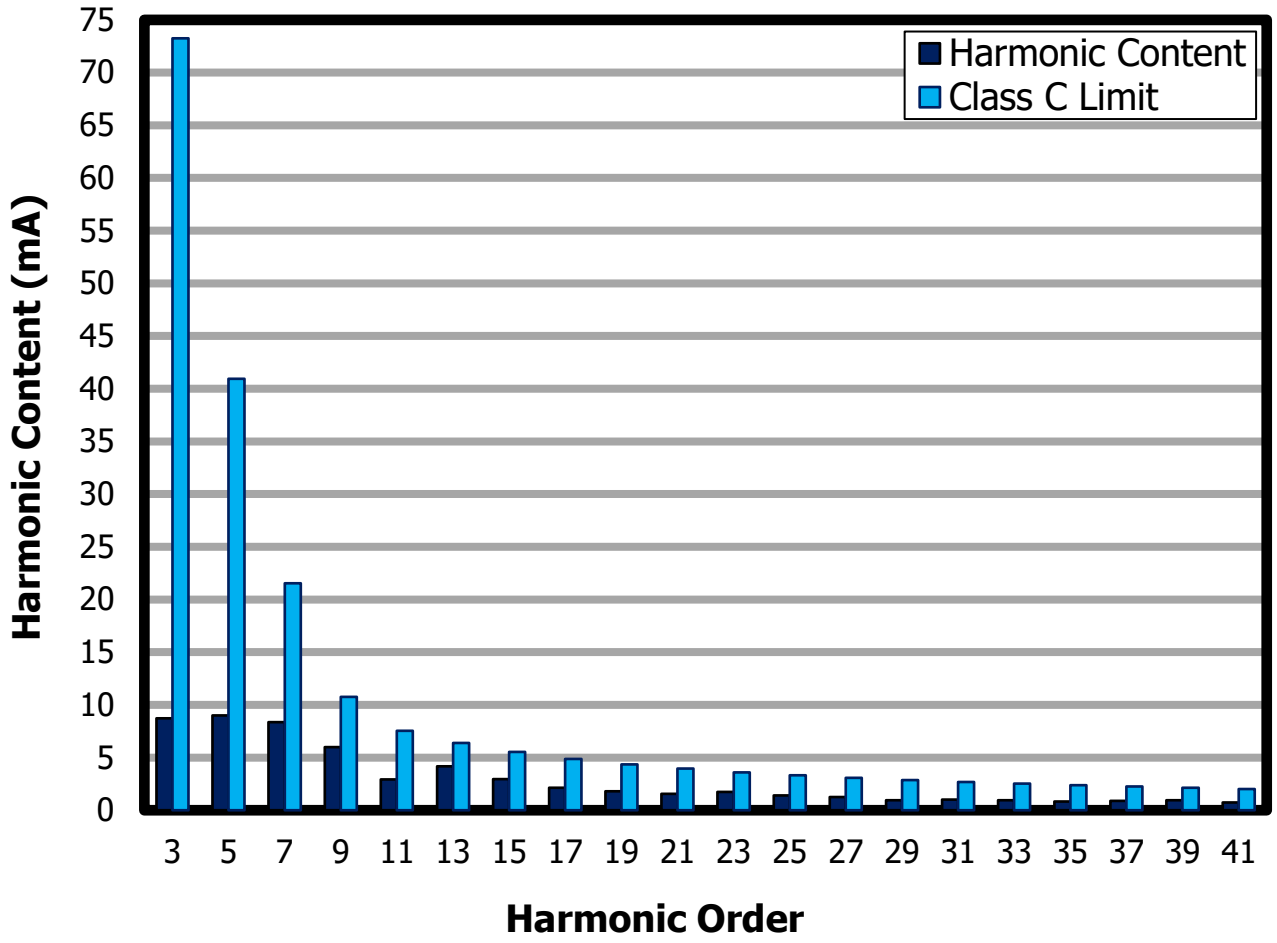


Figure 30 – Full Load Input Current Harmonics at 230 VAC 50 Hz.

Set-up: Open frame unit.
Load: 24 V 781 mA CC.
V_{IN}: 277 V 50 Hz.
Ambient Temperature: 25 °C.
Soak Time: 10 minutes.

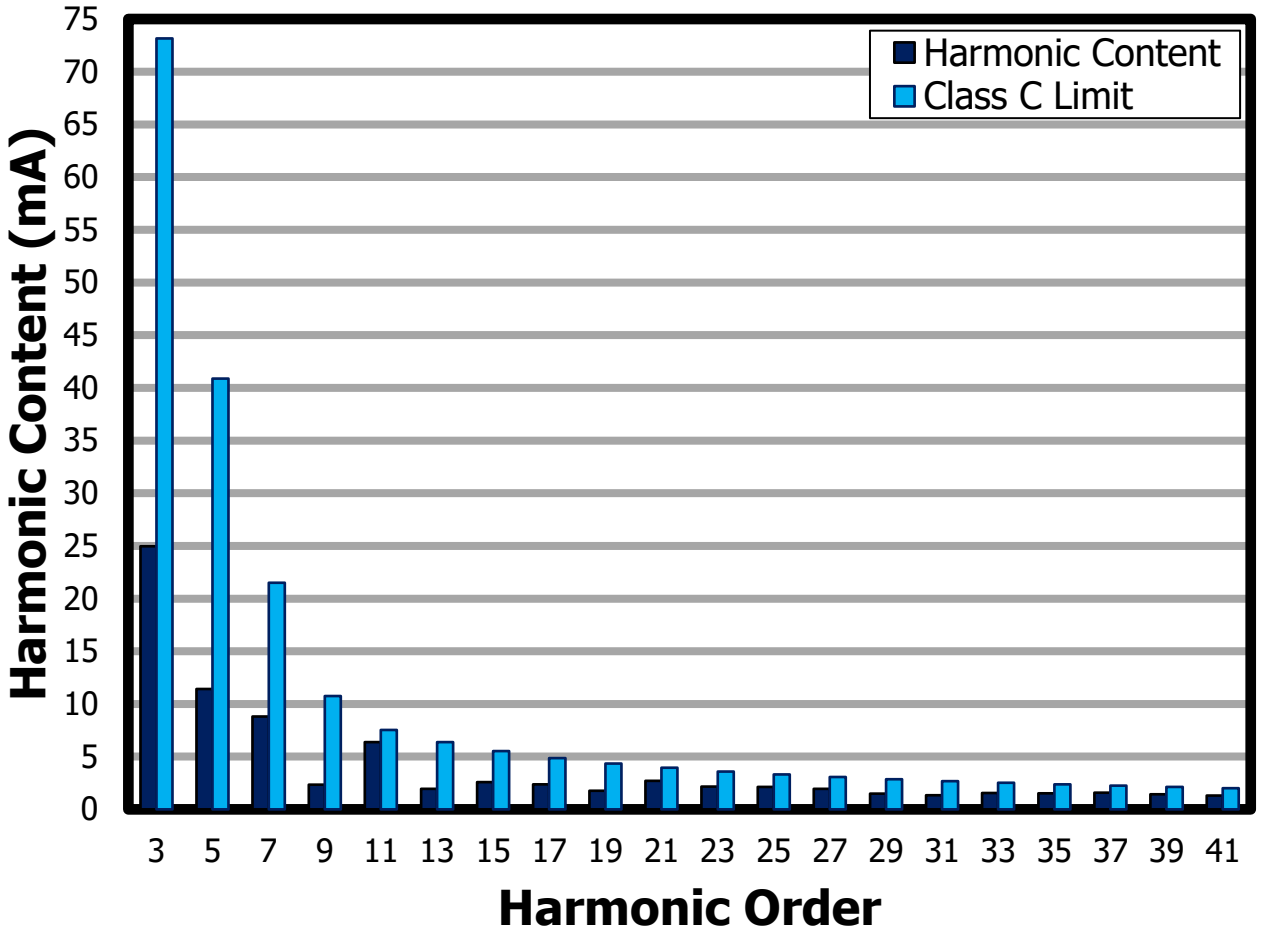


Figure 31 – Full Load Input Current Harmonics at 277 VAC 50 Hz.

13.6 Output Voltage Regulation

Output voltage was measured on the board.

13.6.1 Output Voltage Regulation vs Input Line at Full Load

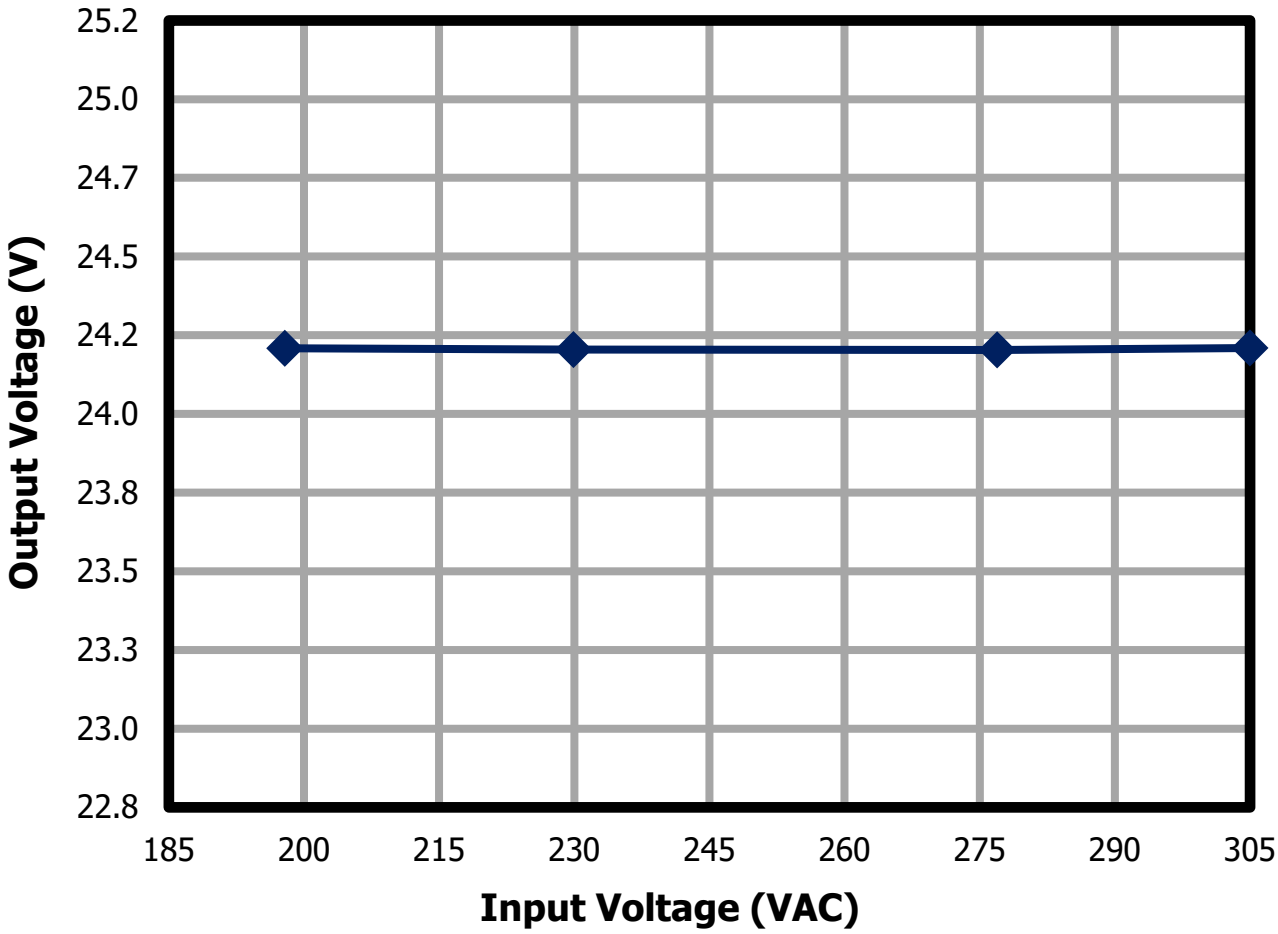


Figure 32 – Voltage Regulation vs Input Line, 24 V Full Load.

13.6.2 Output Voltage Regulation vs Output Load

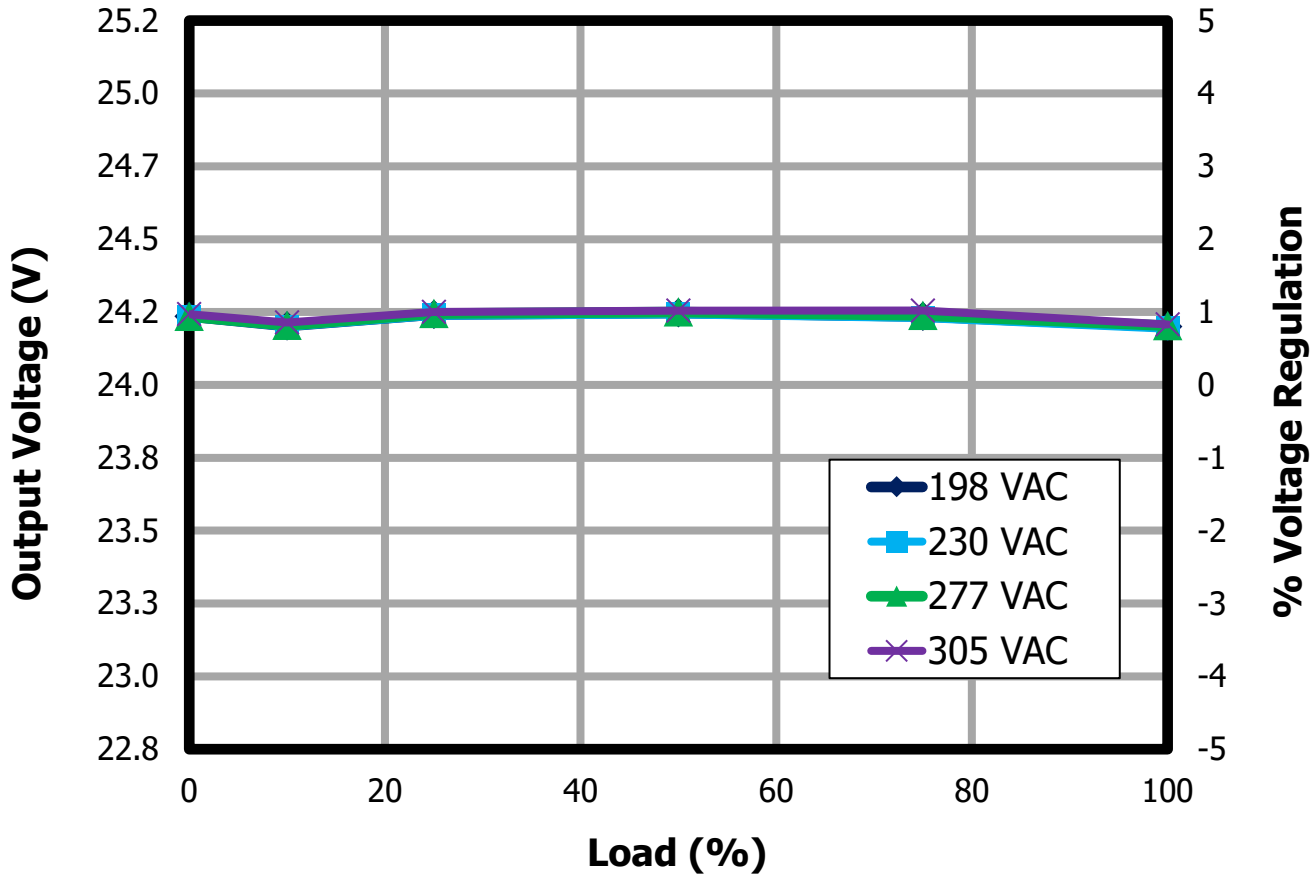


Figure 33 – Voltage Regulation vs Load.

13.7 No-Load Input Power

No load input power was measured using a Yokogawa WT310E power meter.

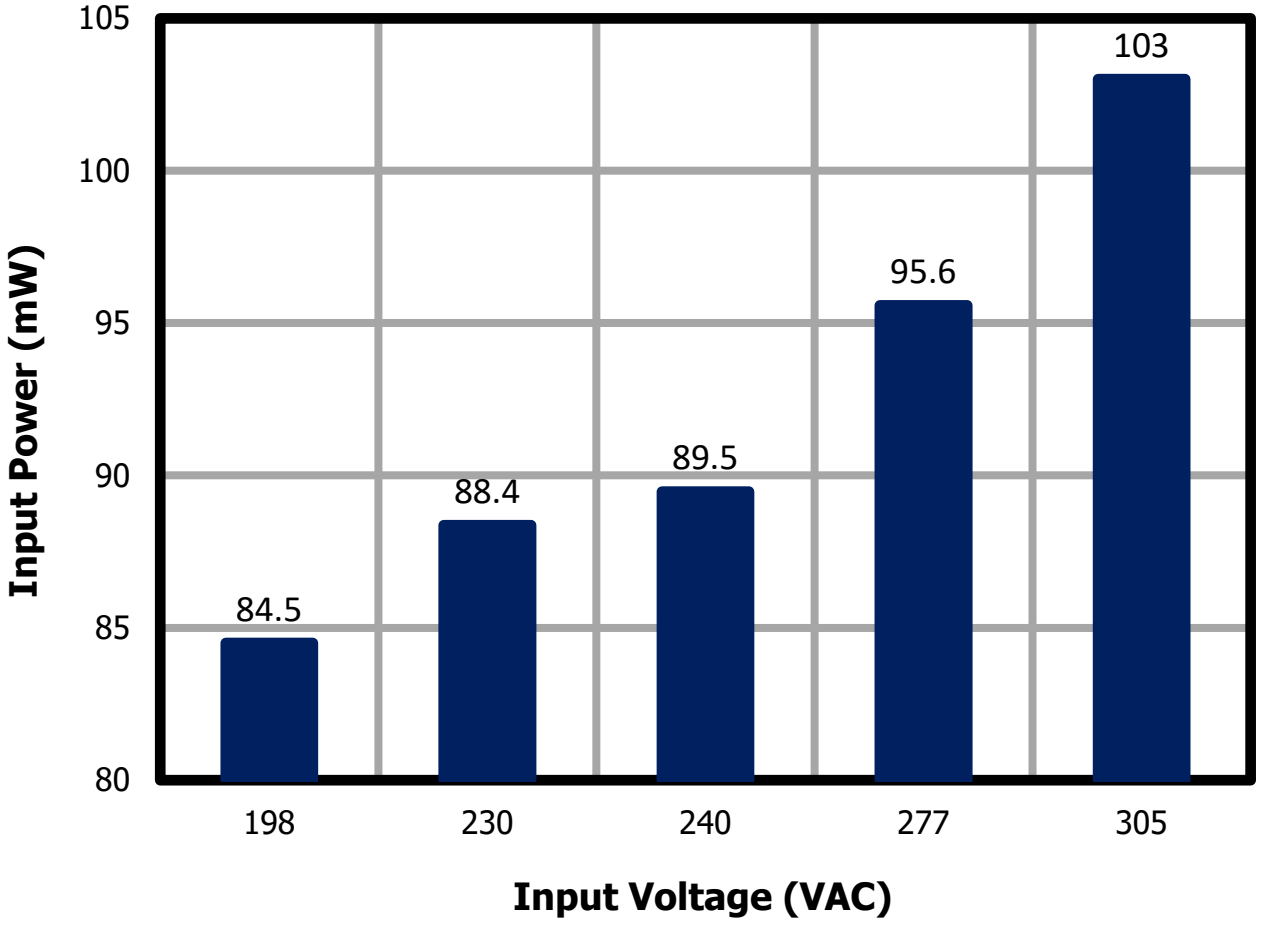


Figure 34 – No-Load Input Power.

13.8 Output Ripple Voltage at 24 V

Output ripple voltage was measured at the end of 100 mΩ output cable.

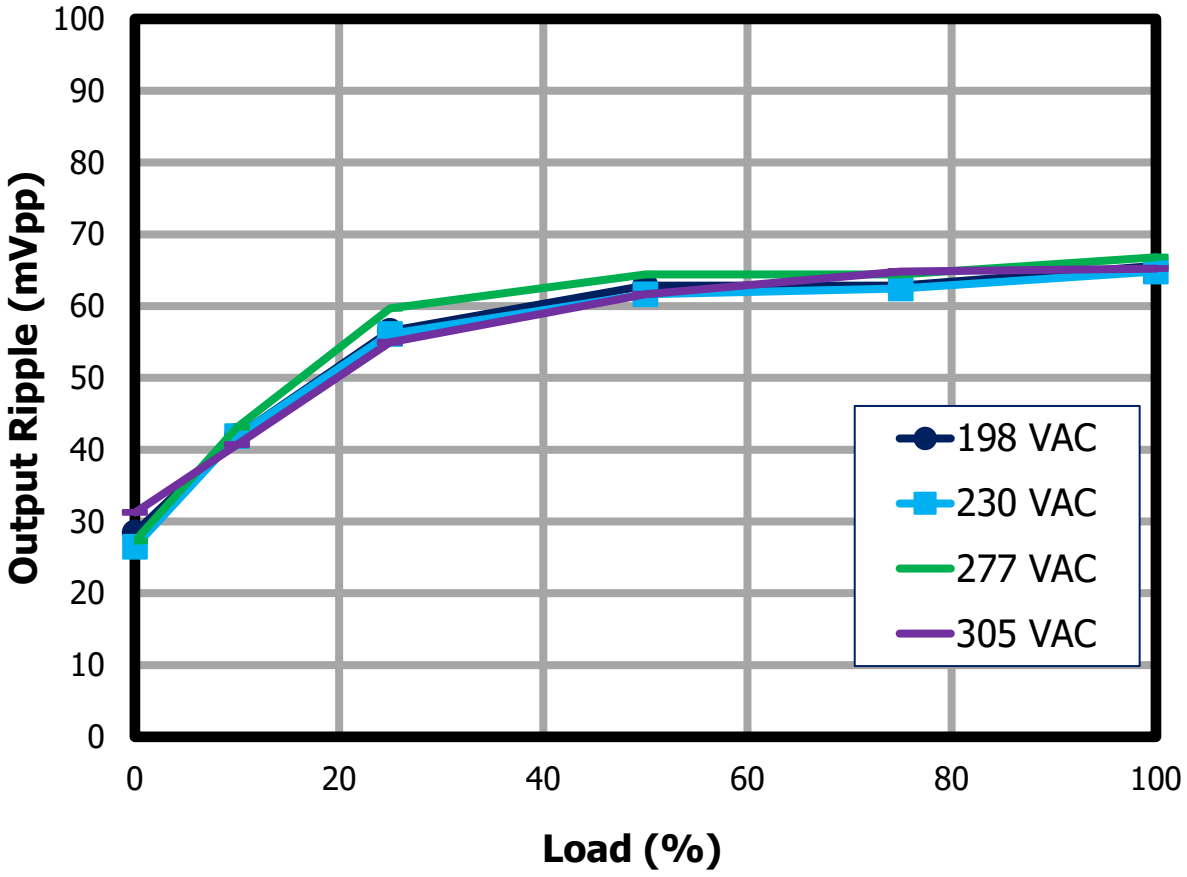


Figure 35 – Ripple voltage vs. Load.

13.9 Average and 10% Load Efficiency

13.9.1 Average and 10% Efficiency at 230 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	DOE6 Limit
(A)	(W)	(VDC)	(mA_{DC})	(W)	(%)	(%)	(%)
100%	81.6	24.2	3124	75.6	92.6	91.0	83.3
75%	61.5	24.2	2343	56.8	92.3		
50%	41.7	24.2	1562	37.9	90.8		
25%	21.5	24.2	781	18.9	88.1		
10%	9.3	24.2	312	7.56	81.0	---	73.3

Table 14 – Average and 10% Efficiency at 230 VAC.

13.9.2 Average and 10% Efficiency at 277 VAC

Load	P_{IN}	V_{OUT} at PCB	I_{OUT}	P_{OUT}	Efficiency at PCB	Average Efficiency	DOE6 Limit
(A)	(W)	(VDC)	(mA_{DC})	(W)	(%)	(%)	(%)
100%	81.3	24.2	3124	75.6	93.0	91.2	83.3
75%	61.5	24.2	2343	56.7	92.3		
50%	41.5	24.2	1562	37.9	91.3		
25%	21.5	24.2	781	18.9	88.3		
10%	9.28	24.2	312	7.57	81.6	---	73.3

Table 15 – Average and 10% Efficiency at 277 VAC.

13.10 Thermal Test

13.10.1 Board Thermal testing - Room Temperature

The open frame PSU was placed in a horizontal position inside an acrylic plastic housing. Thermal data were measured using a FLIR camera.

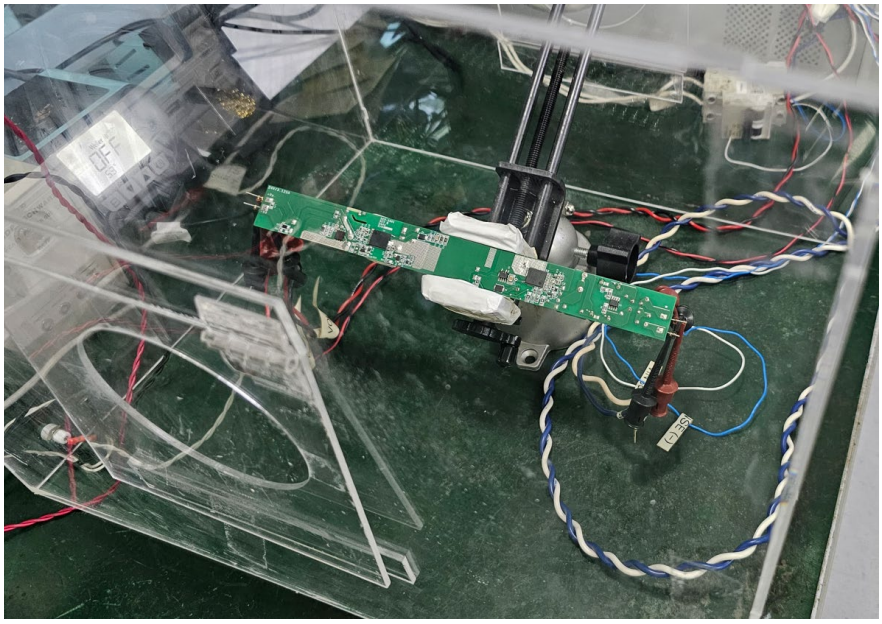


Figure 36 – Room Temperature Thermal Scan Test Set-up.

13.10.1.1 Thermal Scan Test Data (Summary)

Circuit Location	Ambient Temperature to 25 °C			
	198 VAC	230 VAC	277 VAC	305 VAC
	50 Hz	50 Hz	50 Hz	50 Hz
BR1-(Rectifier)	60.3	54.1	49.8	45.1
T3-(PFC Inductor)	53.3	48.2	44.4	41.2
U2-(PFS7623C)	74.4	55.6	53.1	46.2
D1-(Boost Diode)	65.3	56.5	54.1	51.6
T2-(Flyback Transformer)	83.9	82.8	83.9	82.7
U3-(INN4274C)	77	75.6	75.7	75.4
Q3-(SR FET)	72.5	71.8	71.9	72.0

Table 16 – Room Temperature Thermal Scan Test Data.

Component temperatures were well within their thermal limits. See the following thermal images for more details.

13.10.1.2Thermal Scan at 198 VAC 24 V / 3.13 A

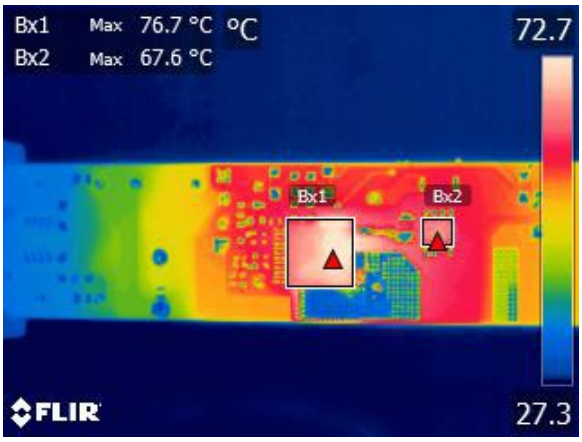


Figure 37 – Thermal Scan 198 V 24 V / 3.13 A
Bx1: U2-(PFS7623C): 76.7 °C
Bx2: D1-(Boost Diode): 67.6 °C
Ambient: 27.3 °C

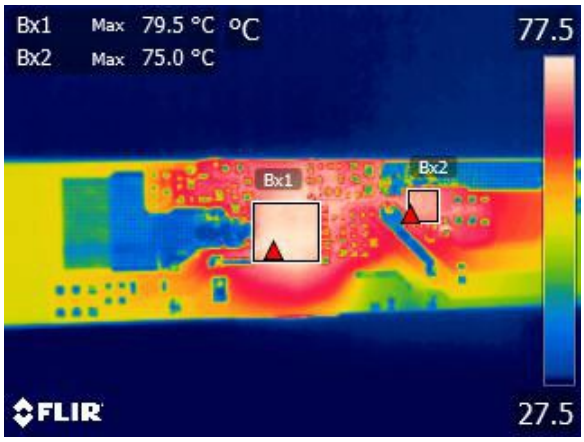


Figure 38 – Thermal Scan 198 V 24 V / 3.13 A
Bx1: U3-Pri (INN4274C): 79.5 °C
Bx2: Q3-Sec (SR FET): 75.0 °C
Ambient: 27.5 °C

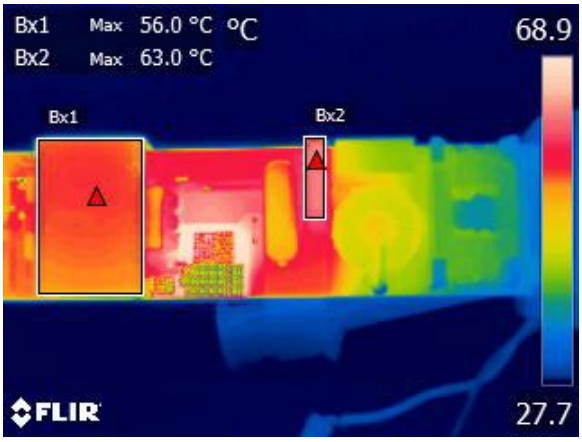


Figure 39 – Thermal Scan 198 V 24 V / 3.13 A
Bx1: T3-(PFC Inductor): 56.0 °C
Bx2: BR1-(Rectifier): 63.0 °C
Ambient: 27.7 °C

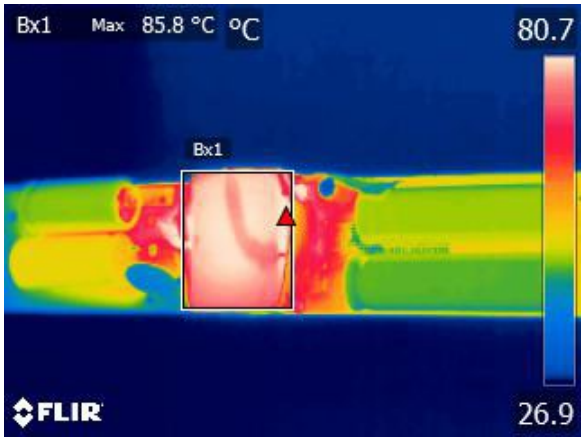


Figure 40 – Thermal Scan 198 V 24 V / 3.13 A
Bx1: T2-(Flyback TRF): 85.8 °C
Ambient: 26.9 °C

13.10.1.3Thermal Scan at 230 VAC 24 V / 3.13 A

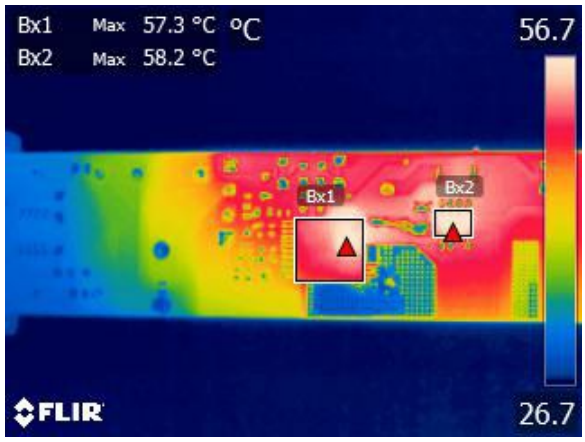


Figure 41 – Thermal Scan 230 V 24 V / 3.13 A
Bx1: U2-(PFS7623C): 57.3 °C
Bx2: D1-(Boost Diode): 58.2 °C
Ambient: 26.7 °C

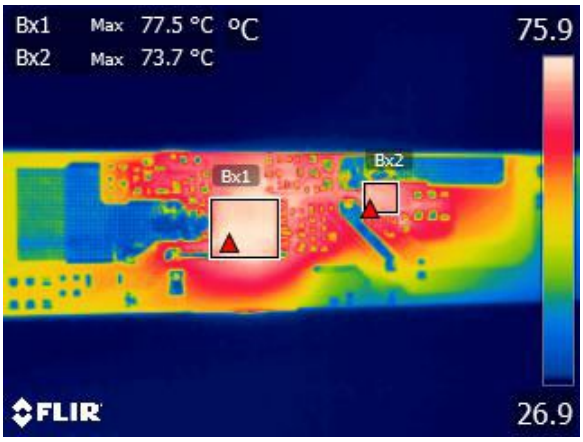


Figure 42 – Thermal Scan 230 V 24 V / 3.13 A
Bx1: U3-Pri (INN4274C): 77.5 °C
Bx2: Q3-Sec (SR FET): 73.7 °C
Ambient: 26.9 °C

Figure 43 – Thermal Scan 230 V 24 V / 3.13 A
Bx1: T3-(PFC Inductor): 50.3 °C
Bx2: BR1-(Rectifier): 56.2 °C
Ambient: 27.1 °C

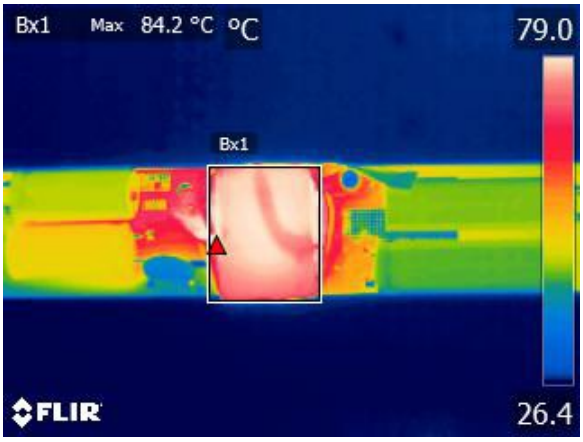


Figure 44 – Thermal Scan 230 V 24 V / 3.13 A
Bx1: T2-(Flyback TRF): 84.2 °C
Ambient: 26.4 °C

13.10.1.4Thermal Scan at 277 VAC 24 V / 3.13 A

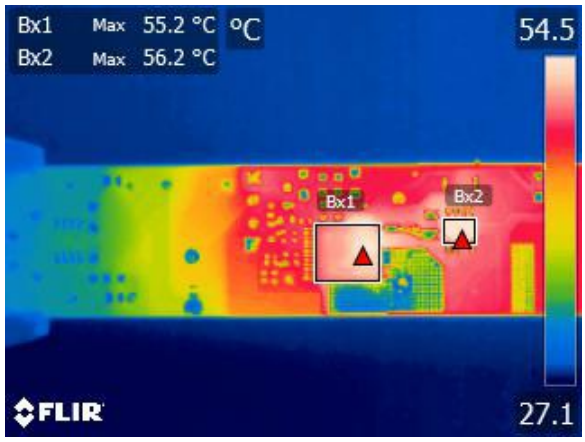


Figure 45 – Thermal Scan 277 V 24 V / 3.13 A
Bx1: U2-(PFS7623C): 55.2 °C
Bx2: D1-(Boost Diode): 56.2 °C
Ambient: 27.1 °C

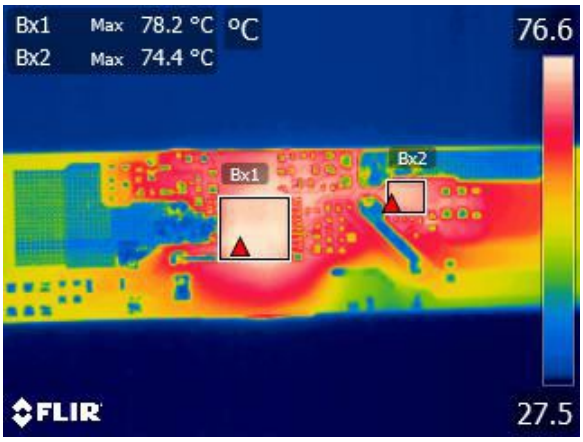


Figure 46 – Thermal Scan 277 V 24 V / 3.13 A
Bx1: U3-Pri (INN4274C): 78.2 °C
Bx2: Q3-Sec (SR FET): 74.4 °C
Ambient: 27.5 °C

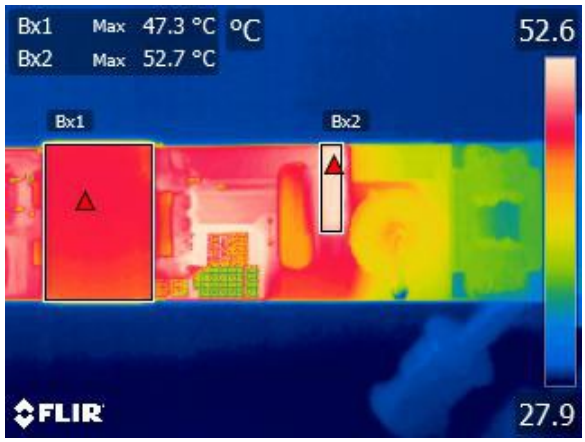


Figure 47 – Thermal Scan 277 V 24 V / 3.13 A
Bx1: T3-(PFC Inductor): 47.3 °C
Bx2: BR1-(Rectifier): 52.7 °C
Ambient: 27.9 °C

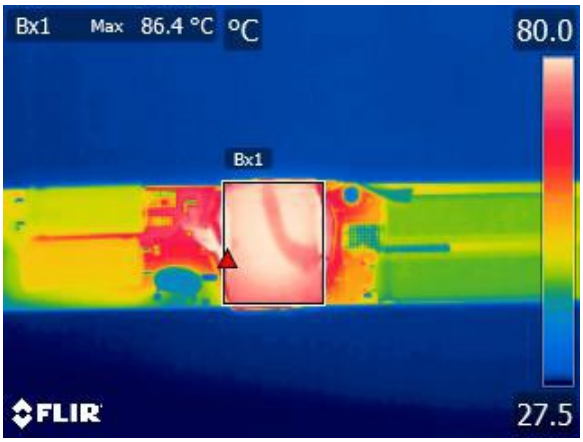


Figure 48 – Thermal Scan 277 V 24 V / 3.13 A
Bx1: T2-(Flyback TRF): 86.4 °C
Ambient: 27.5 °C

13.10.1.5Thermal Scan at 305 VAC 24 V / 3.13 A

Figure 49 – Thermal Scan 305 V 24 V / 3.13 A
Bx1: U2-(PFS7623C): 48.2 °C
Bx2: D1-(Boost Diode): 53.6 °C
Ambient: 27.0 °C

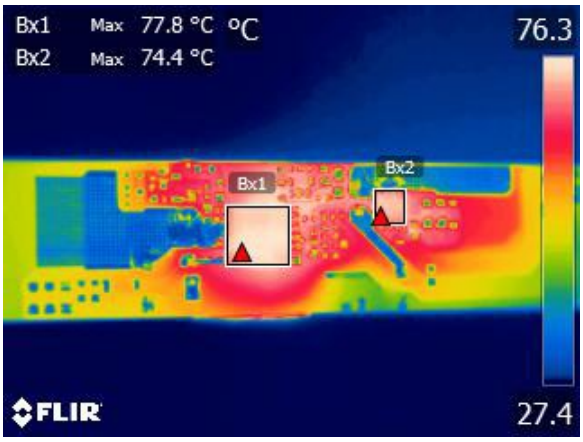


Figure 50 – Thermal Scan 305 V 24 V / 3.13 A
Bx1: U3-Pri (INN4274C): 77.8 °C
Bx2: Q3-Sec (SR FET): 74.4 °C
Ambient: 27.4 °C

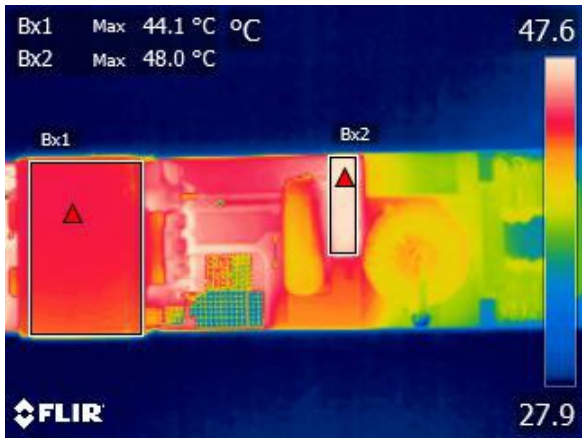


Figure 51 – Thermal Scan 305 V 24 V / 3.13 A
Bx1: T3-(PFC Inductor): 44.1 °C
Bx2: BR1-(Rectifier): 48 °C
Ambient: 27.9 °C

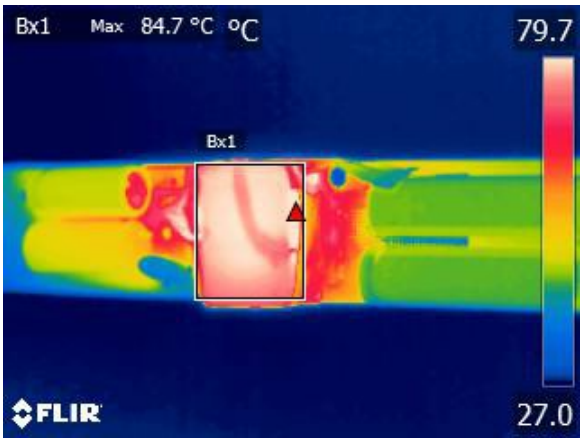


Figure 52 – Thermal Scan 305 V 24 V / 3.13 A
Bx1: T2-(Flyback TRF): 84.7 °C
Ambient: 27.0 °C

13.10.2 Thermal Test at 55 °C Ambient

The PSU was placed inside a plastic enclosure and then placed in a closed box to prevent air flow from affecting the thermal measurement. Thermal data was taken using a thermocouple and a Graphtec data logger.

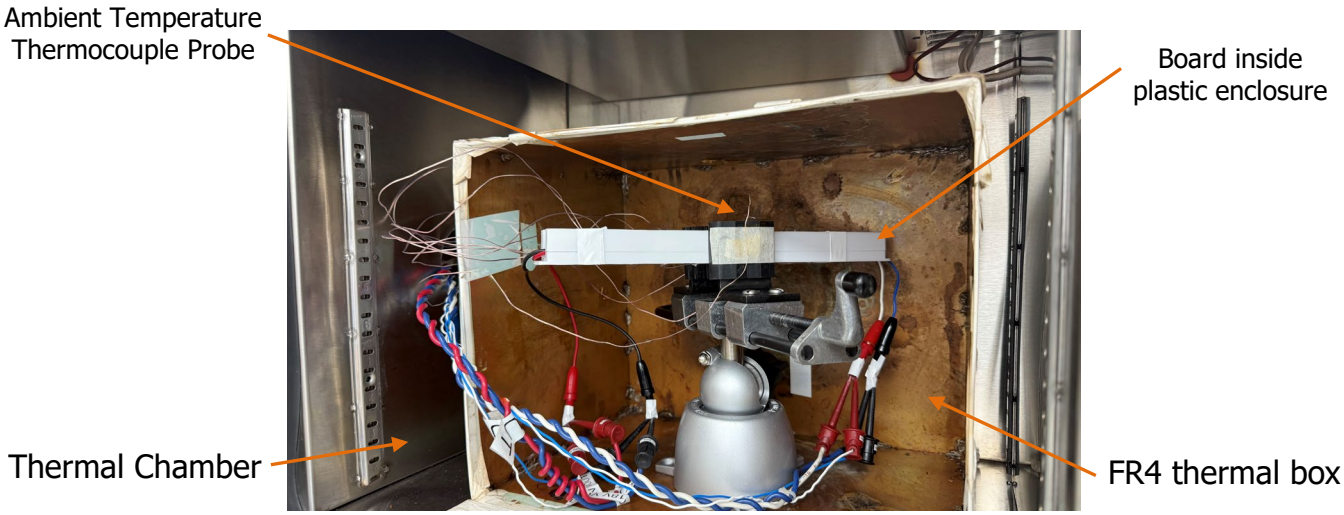


Figure 53 – Thermal Chamber Test Set-up with Case at 55 °C Ambient.

Circuit Location	Temperature °C	
	198 VAC	305 VAC
	50 Hz	50 Hz
Ambient	55.5	55.3
BR1-(Rectifier)	91.0	75
T3-(PFC Inductor)	91.3	75.1
U2-(PFS7623C)	102	75.4
D1-(Boost Diode)	92.4	77.5
T2-(Flyback Transformer)	110	108
U3-(INN4274C)	102	98.9
Q3-(SR FET)	111	110

Table 17 – Thermal Chamber Test Data at Normal Ambient 55°C.

All component temperatures were well within their thermal limits.

14 Waveforms

14.1 Start-up Profile

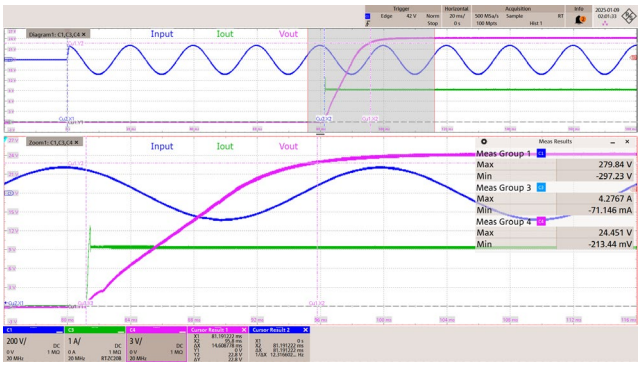


Figure 54 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{IN}, 200 V / div., 20 ms / div.
CH2: I_{OUT}, 1 A / div., 20 ms / div.
CH3: V_{OUT}, 3 V / div., 20 ms / div.
Zoom: 4 ms/div.
$t_{ON\ Delay}$: 81.2 ms
t_{Rise} = 14.6 ms
V_{MAX} = 24.5 V

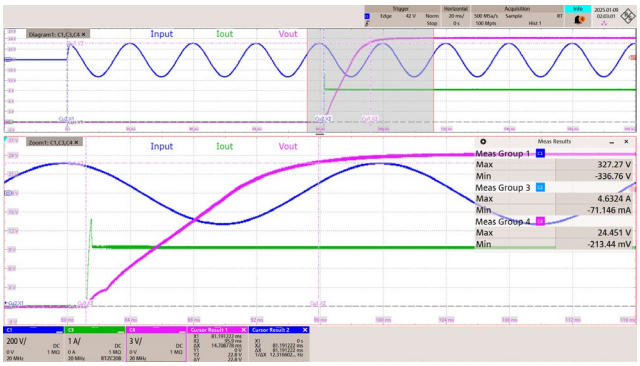


Figure 55 – 230 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{IN}, 200 V / div., 20 ms / div.
CH2: I_{OUT}, 1 A / div., 20 ms / div.
CH3: V_{OUT}, 3 V / div., 20 ms / div.
Zoom: 4 ms/div.
$t_{ON\ Delay}$: 81.2 ms
t_{Rise} = 14.7 ms
V_{MAX} = 24.5 V

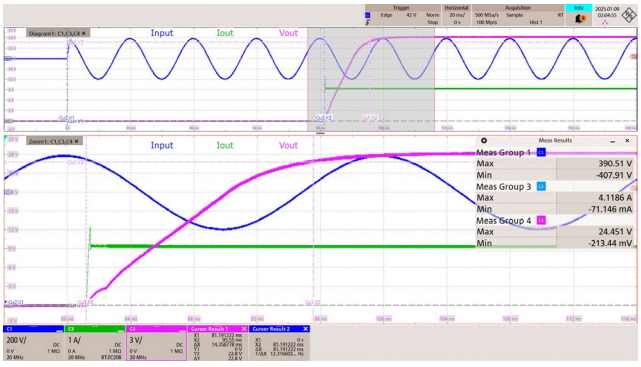


Figure 56 – 277 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{IN}, 200 V / div., 20 ms / div.
CH2: I_{OUT}, 1 A / div., 20 ms / div.
CH3: V_{OUT}, 3 V / div., 20 ms / div.
Zoom: 4 ms/div.
$t_{ON\ Delay}$: 81.2 ms
t_{Rise} = 14.4 ms
V_{MAX} = 24.5 V

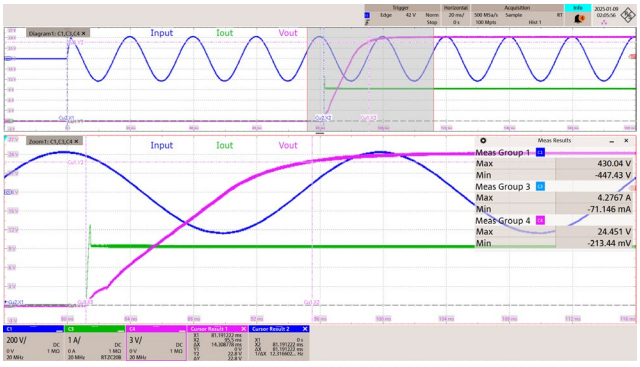


Figure 57 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{IN}, 200 V / div., 20 ms / div.
CH2: I_{OUT}, 1 A / div., 20 ms / div.
CH3: V_{OUT}, 3 V / div., 20 ms / div.
Zoom: 4 ms/div.
$t_{ON\ Delay}$: 81.2 ms
t_{Rise} = 14.3 ms
V_{MAX} = 24.5 V

14.2 PFC Drain Voltage and Current

14.2.1 PFC Drain Voltage and Current During Start Up into Full Load

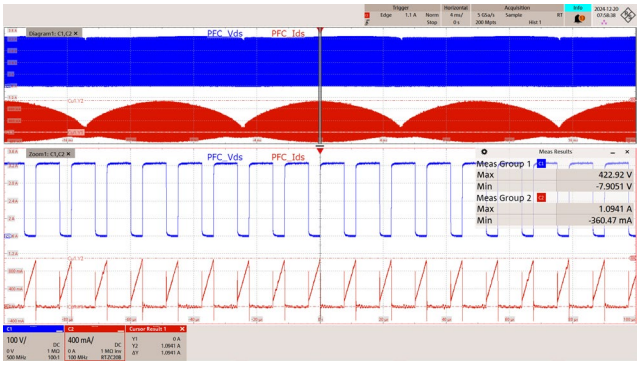


Figure 58 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 4 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 423 V
$I_{DS\ MAX}$ = 1.09 A

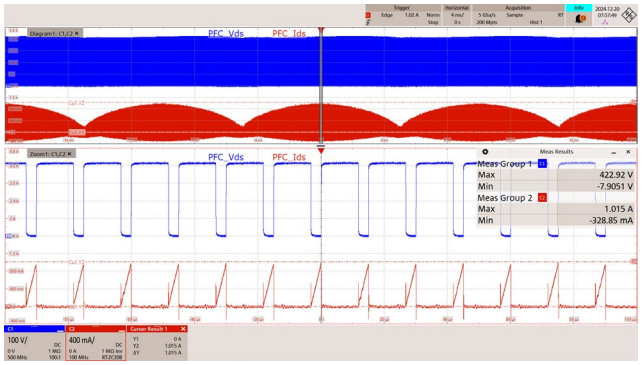


Figure 59 – 230 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 4 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 4 ms / div.
Zoom: 20 µs /div.
$V_{DS\ MAX}$ = 423 V
$I_{DS\ MAX}$ = 1.02 A

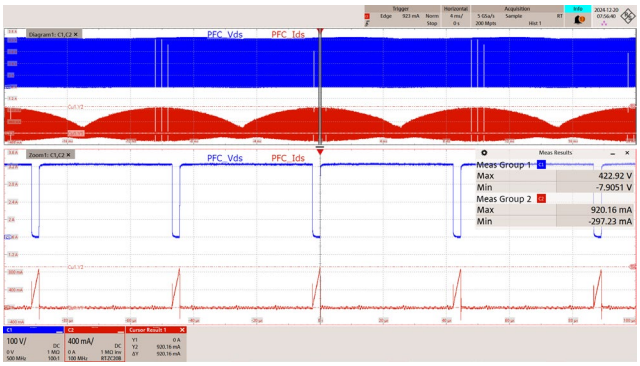


Figure 60 – 277 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 4 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 423 V
$I_{DS\ MAX}$ = 920 mA

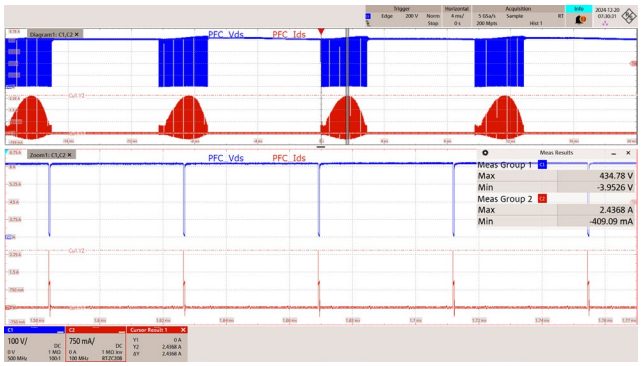


Figure 61 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 4 ms / div.
CH2: PFC_I_{DS}, 750 mA / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 435 V
$I_{DS\ MAX}$ = 2.44 A

14.2.2 PFC Drain Voltage and Current During Start Up into Full Load

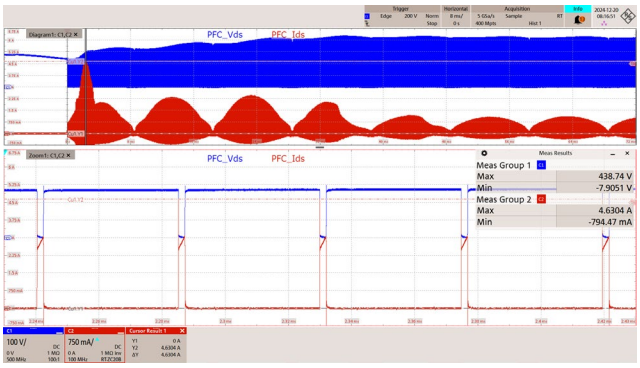


Figure 62 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 8 ms / div.
CH2: PFC_I_{DS}, 750 mA / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 439 V
$I_{DS\ MAX}$ = 4.63 A

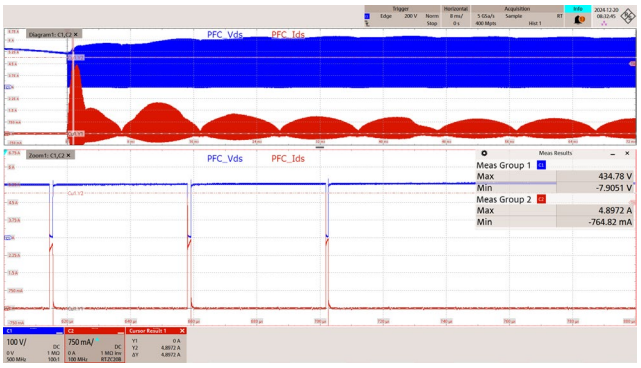


Figure 63 – 230 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 8 ms / div.
CH2: PFC_I_{DS}, 750 mA / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 435 V
$I_{DS\ MAX}$ = 4.90 A

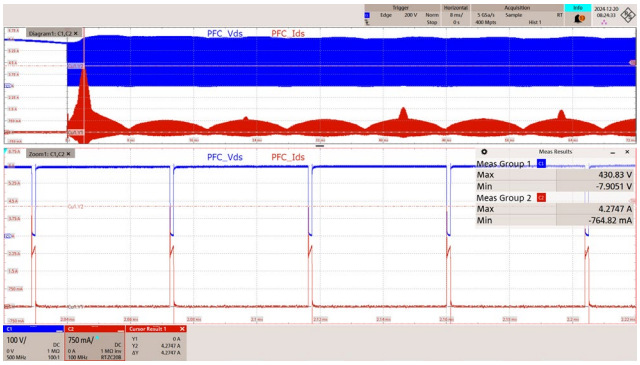


Figure 64 – 277 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 8 ms / div.
CH2: PFC_I_{DS}, 750 mA / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 431 V
$I_{DS\ MAX}$ = 4.27 A

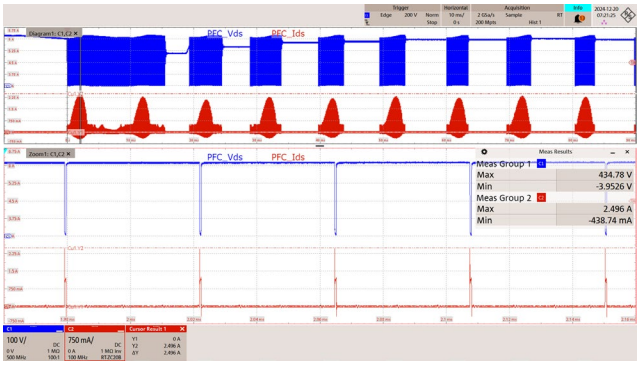


Figure 65 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC_V_{DS}, 100 V / div., 10 ms / div.
CH2: PFC_I_{DS}, 750 mA / div., 10 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 435 V
$I_{DS\ MAX}$ = 2.50 A

14.2.3 PFC Drain Voltage and Current During Transient Loading

Set-up: 1 kHz dynamic load using Chroma 63113A E-load. 0 A – 3.13 A with 50% duty cycle and load current slew rate of 800 mA/µs.

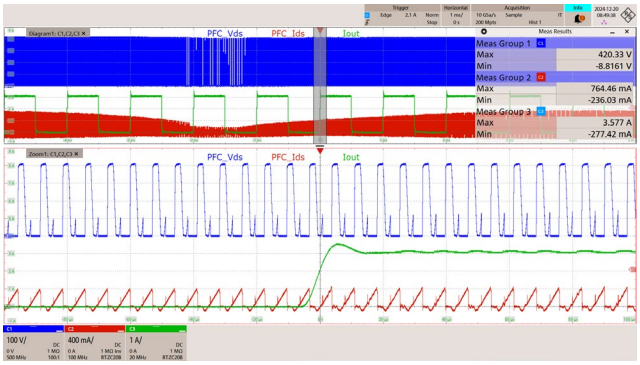


Figure 66 – 198 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC_V_{DS}, 100 V / div., 1 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 420 V
$I_{DS\ MAX}$ = 764 mA

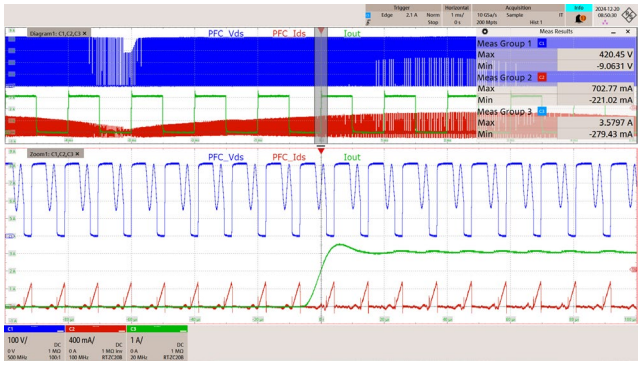


Figure 67 – 230 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC_V_{DS}, 100 V / div., 1 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 420 V
$I_{DS\ MAX}$ = 703 mA

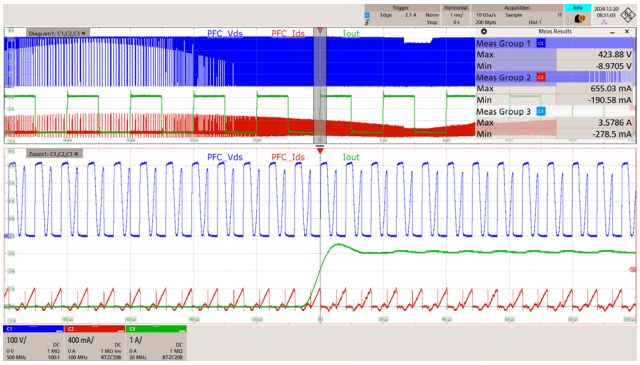


Figure 68 – 277 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC_V_{DS}, 100 V / div., 1 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 424 V
$I_{DS\ MAX}$ = 655 mA

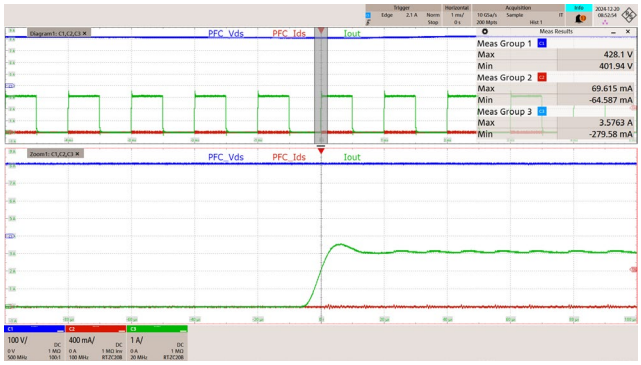


Figure 69 – 305 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC_V_{DS}, 100 V / div., 1 ms / div.
CH2: PFC_I_{DS}, 400 mA / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 428 V
$I_{DS\ MAX}$ = 69.6 mA

14.3 PFC Boost Diode Reverse Voltage Waveforms

14.3.1 PFC Boost Diode Reverse Voltage at Full Load (Steady State)

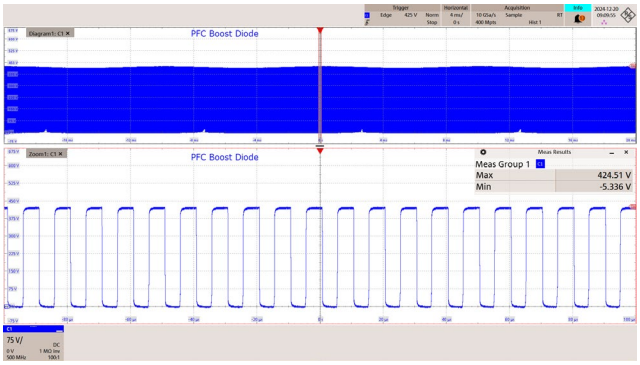


Figure 70 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{D\ MAX}$ = 425 V

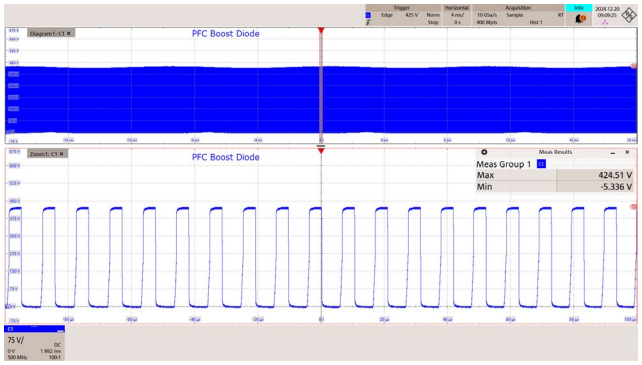


Figure 71 – 230 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 425 V

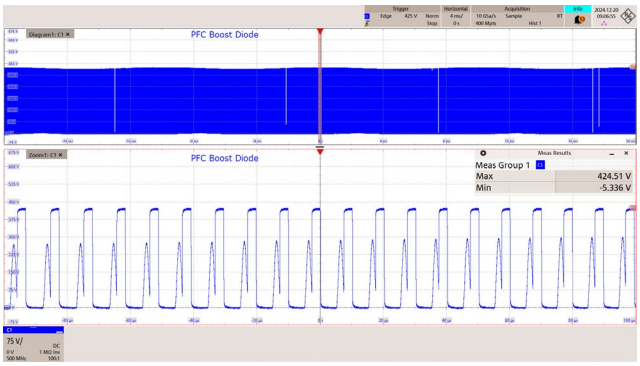


Figure 72 – 277 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 425 V

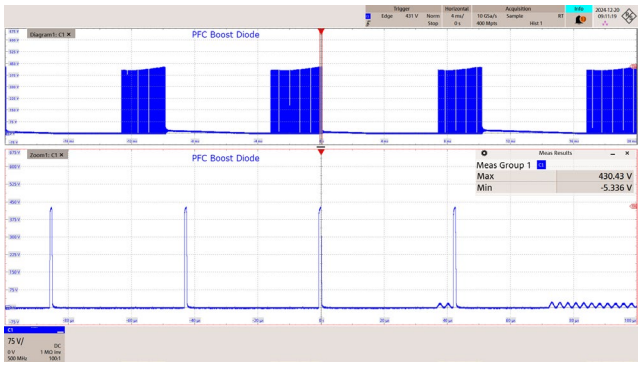


Figure 73 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 4 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 430 V

14.3.2 PFC Boost Diode Reverse Voltage During Start Up into Full Load

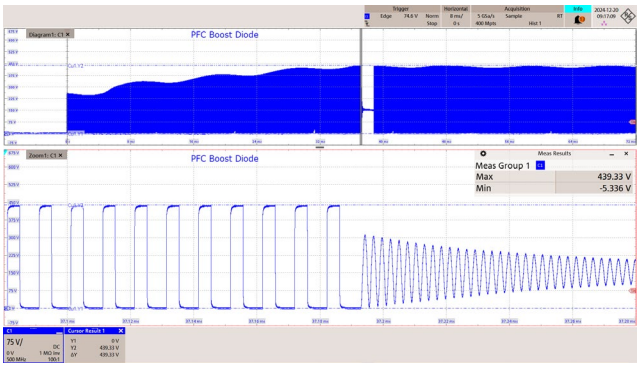


Figure 74 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{D\ MAX}$ = 439 V

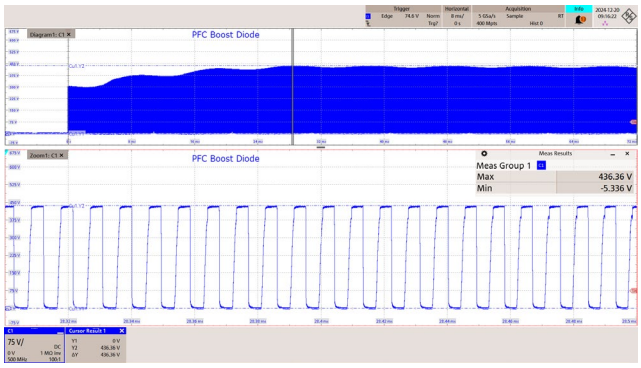


Figure 75 – 230 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 436 V

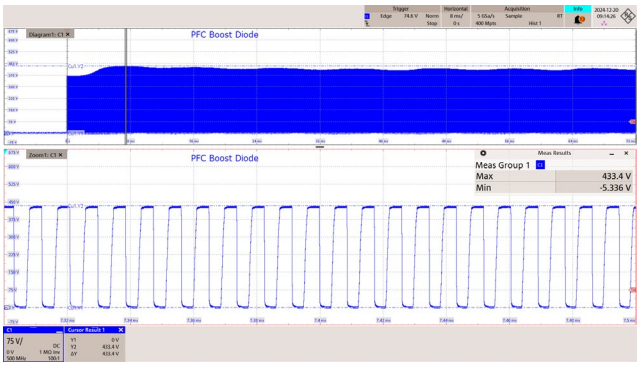


Figure 76 – 277 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 433 V

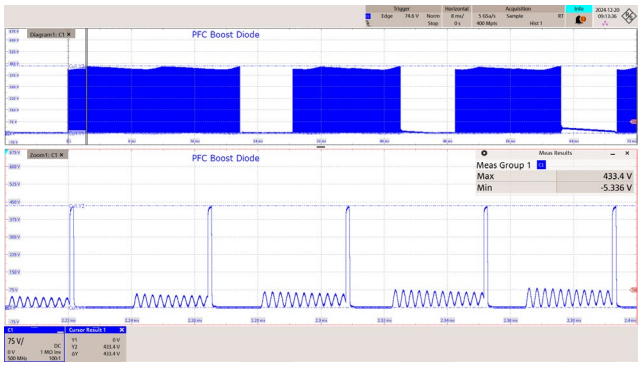


Figure 77 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: PFC Boost Diode Reverse Voltage,
75 V / div., 8 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 433 V

14.3.3 PFC Boost Diode Reverse Voltage When Transient Load Applied

Set-up: 1 kHz dynamic load using Chroma 63113A E-load. 0 A – 3.13 A with 50% duty cycle and load current slew rate of 800 mA/µs.

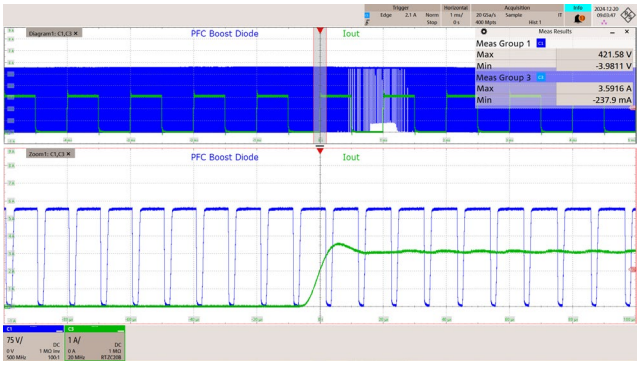


Figure 78 – 198 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC Boost Diode Reverse Voltage, 75 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{D\ MAX}$ = 422 V

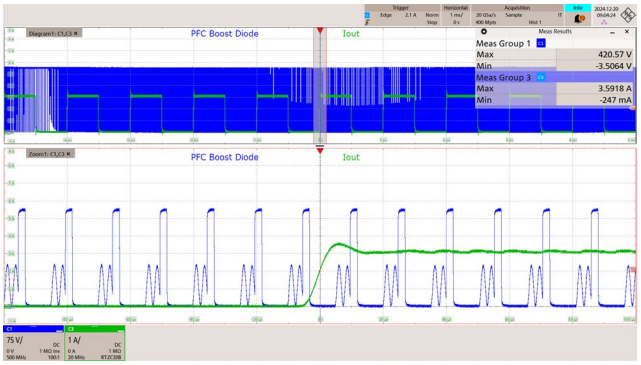


Figure 79 – 230 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC Boost Diode Reverse Voltage, 75 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 421 V

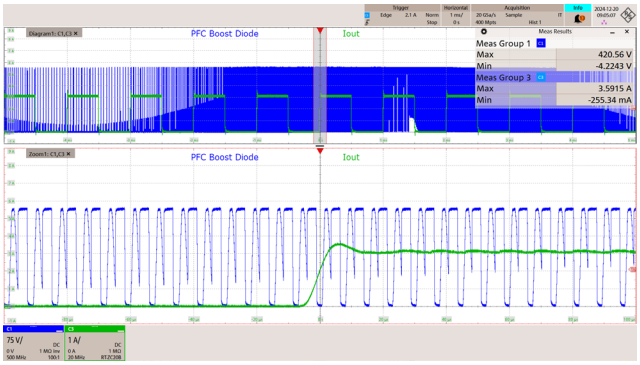


Figure 80 – 277 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: PFC Boost Diode Reverse Voltage, 75 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 421 V

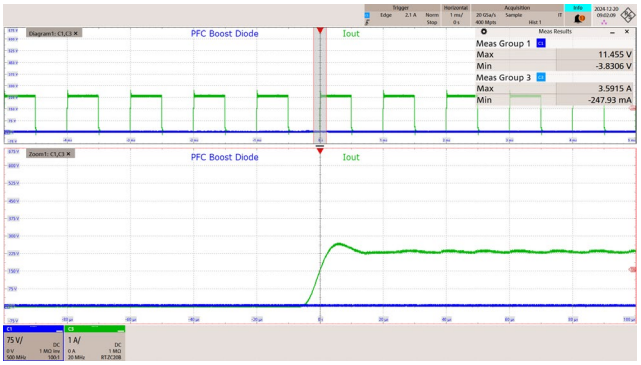


Figure 81 – 305 VAC, 50 Hz. 24V / 0A - 3.13 A Transient
CH1: PFC Boost Diode Reverse Voltage, 75 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 11.5 V

14.4 Flyback Primary Drain Voltage and Current

14.4.1 Flyback Primary Drain Voltage and Current at Full Load (Steady State)

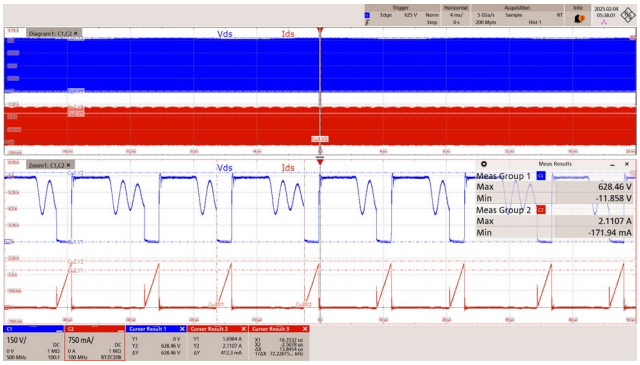


Figure 82 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{DS}, 150 V / div., 4 ms / div.
CH2: I_{DS}, 750 mA / div., 4 ms / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 628 V
$I_{DS\ MAX}$ = 2.11 A

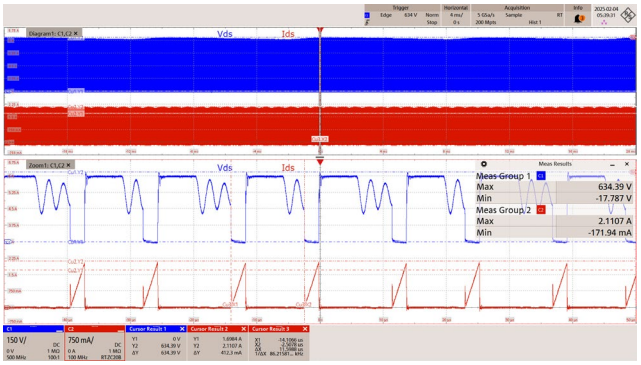


Figure 83 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{DS}, 150 V / div., 4 ms / div.
CH2: I_{DS}, 750 mA / div., 4 ms / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 634 V
$I_{DS\ MAX}$ = 2.11 A

14.4.2 Flyback Primary Drain Voltage and Current During Start Up at Full Load

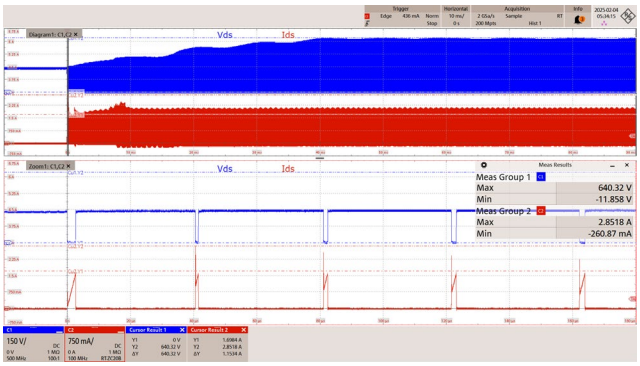


Figure 84 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 750 mA / div., 10 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 640 V
$I_{DS\ MAX}$ = 2.85 A

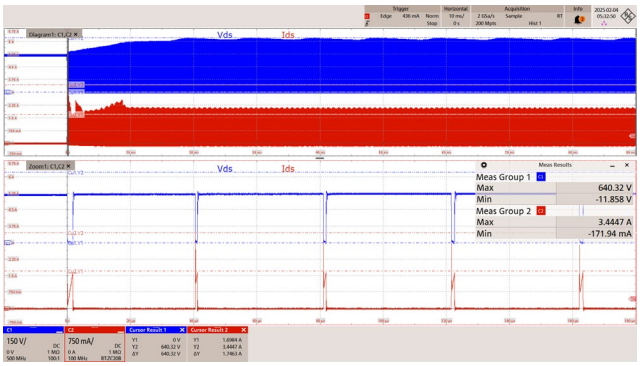


Figure 85 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: V_{DS}, 150 V / div., 10 ms / div.
CH2: I_{DS}, 750 mA / div., 10 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 640 V
$I_{DS\ MAX}$ = 3.44 A

14.4.3 Flyback Primary Drain Voltage and Current During Transient Loading

Set-up: 1 kHz dynamic load using Chroma 63113A E-load. 0 A – 3.13 A with 50% duty cycle and load current slew rate of 800 mA/µs.

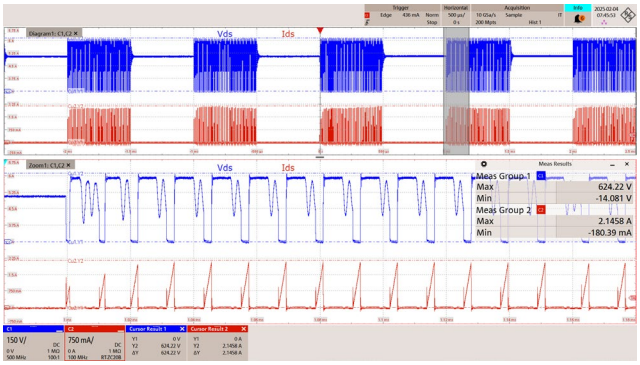


Figure 86 – 198 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{DS}, 150 V / div., 500 µs / div.
CH2: I_{DS}, 750 mA / div., 500 µs / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 624 V
$I_{DS\ MAX}$ = 2.15 A

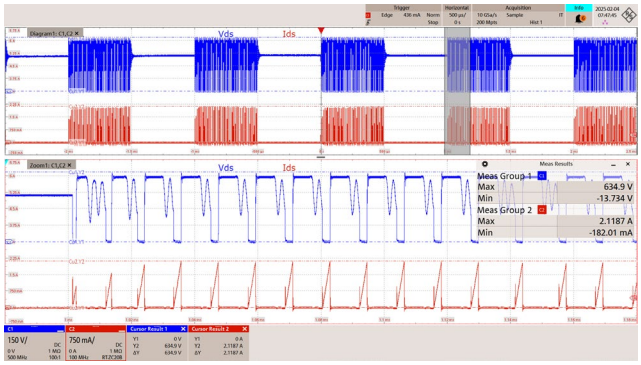


Figure 87 – 305 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{DS}, 150 V / div., 500 µs / div.
CH2: I_{DS}, 750 mA / div., 500 µs / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 635 V
$I_{DS\ MAX}$ = 2.12 A

14.4.4 Flyback Primary Drain Voltage and Current During Output Short Circuit (Measured at the Edge of the PCB)

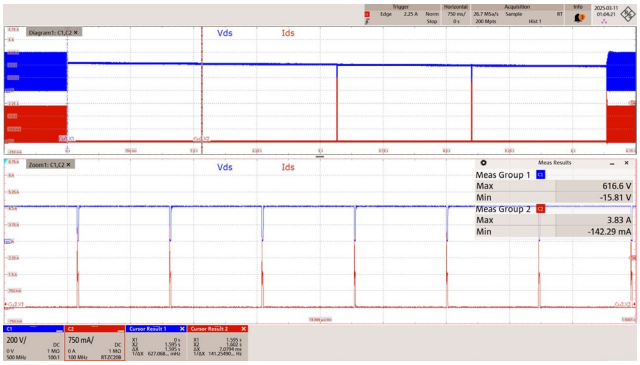


Figure 88 – 198 VAC, 50 Hz. Output Short.
CH1: V_{DS}, 200 V / div., 750 ms / div.
CH2: I_{DS}, 750 mA / div., 750 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 617 V
$I_{DS\ MAX}$ = 3.83 A
$t_{AR\ ON}$ = 7.08 ms
$t_{AR\ OFF}$ = 1.6 s

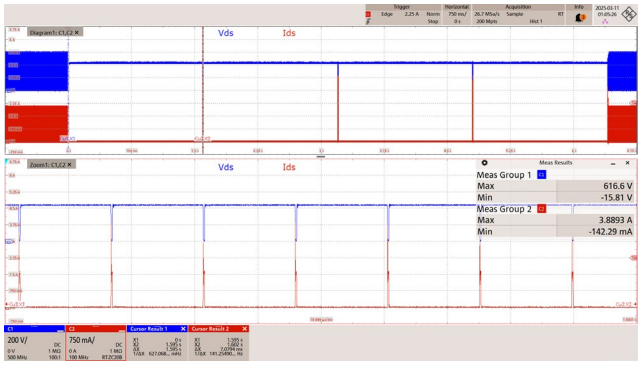


Figure 89 – 305 VAC, 50 Hz. Output Short.
CH1: V_{DS}, 200 V / div., 750 ms / div.
CH2: I_{DS}, 750 mA / div., 750 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 617 V
$I_{DS\ MAX}$ = 3.89 A
$t_{AR\ ON}$ = 7.08 ms
$t_{AR\ OFF}$ = 1.6 s

14.5 Flyback SR FET (Q3) Voltage Waveforms

14.5.1 Flyback SR FET (Q3) Voltage under Full Load (Steady State)

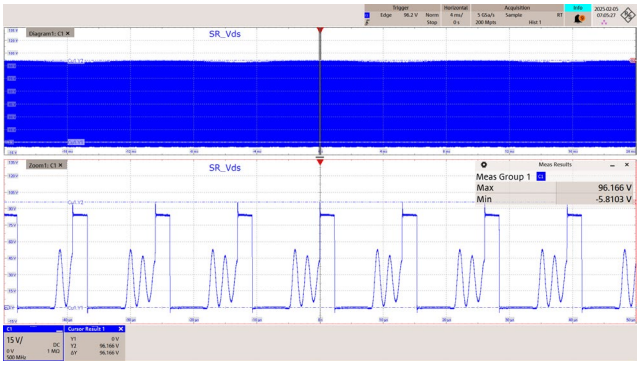


Figure 90 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: SR_V_{DS}, 15 V / div., 4 ms / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 96.2 V

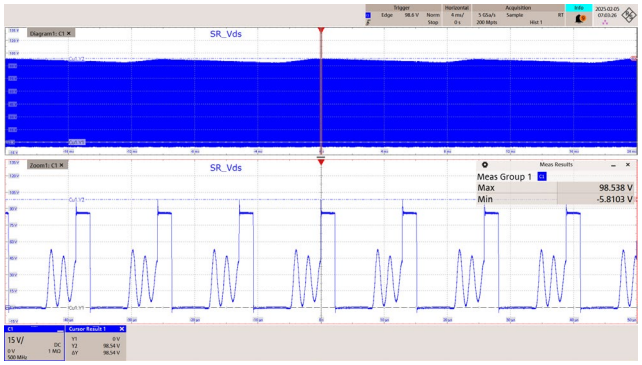


Figure 91 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: SR_V_{DS}, 15 V / div., 4 ms / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 98.5 V

14.5.2 Flyback SR FET (Q3) Voltage at Full Load During Start-up (CC Load)

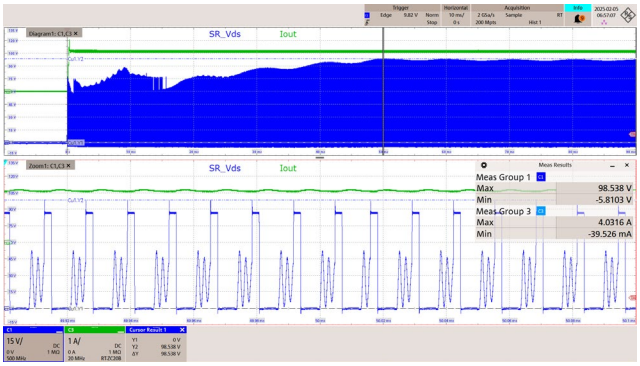


Figure 92 – 198 VAC, 50 Hz. 24 V / 3.13 A.
CH1: SR_V_{DS}, 15 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 98.5 V

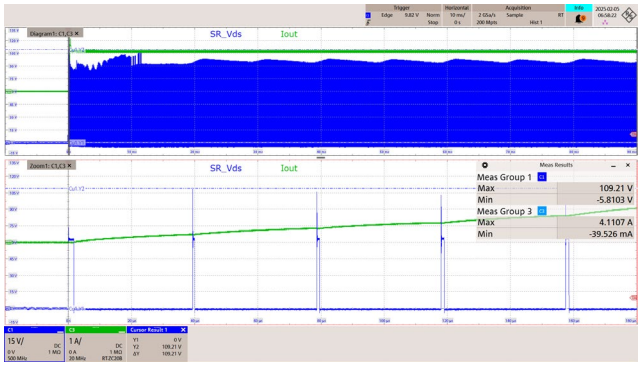


Figure 93 – 305 VAC, 50 Hz. 24 V / 3.13 A.
CH1: SR_V_{DS}, 15 V / div., 10 ms / div.
CH3: I_{OUT}, 1 A / div., 10 ms / div.
Zoom: 20 µs/div.
$V_{DS\ MAX}$ = 109 V

14.5.3 Flyback SR FET (Q3) Drain Voltage During Transient Loading

Set-up: 1 kHz dynamic load using Chroma 63113A E-load. 0 A – 3.13 A with 50% duty cycle and load current slew rate of 800 mA/µs.

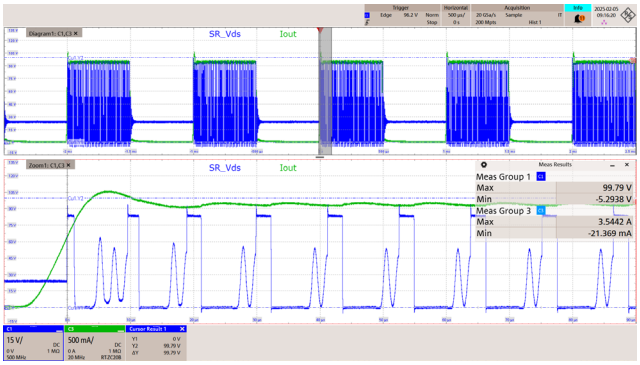


Figure 94 – 198 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: SR_V_{DS}, 15 V / div., 500 µs / div.
CH3: I_{OUT}, 500 mA / div., 500 µs / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 99.8 V

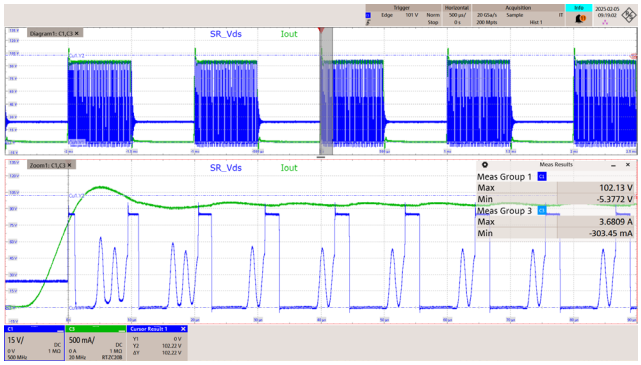


Figure 95 – 305 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: SR_V_{DS}, 15 V / div., 500 µs / div.
CH3: I_{OUT}, 500 mA / div., 500 µs / div.
Zoom: 10 µs/div.
$V_{DS\ MAX}$ = 102 V

14.6 Load Transient Response

Voltage was measured at the output terminals.

14.6.1 0% - 100% Load Transient

Set-up: 1 kHz dynamic load using Chroma 63113A E-load. 0 A – 3.13 A with 50% duty cycle and load current slew rate of 800 mA/µs.

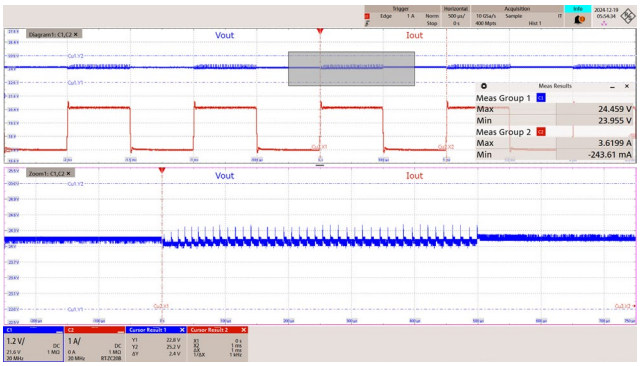


Figure 96 – 198 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_{OUT}, 1 A / div., 500 µs / div.
Zoom: 100 µs/div.
$V_{OUT\ MAX}$ = 24.5 V
$V_{OUT\ MIN}$ = 24 V

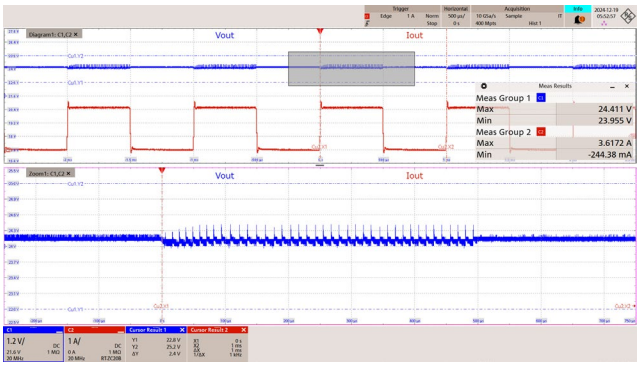


Figure 97 – 230 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_{OUT}, 1 A / div., 500 µs / div.
Zoom: 100 µs/div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24.0 V

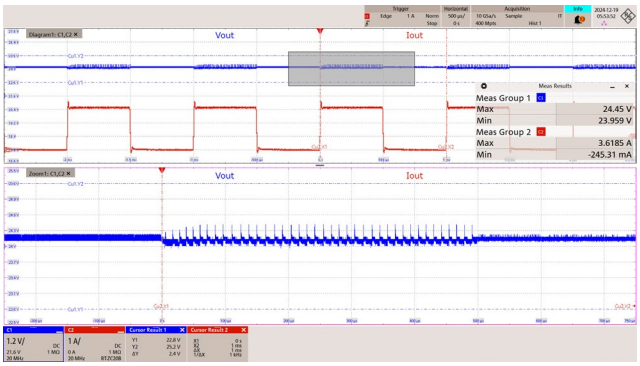


Figure 98 – 277 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_{OUT}, 1 A / div., 500 µs / div.
Zoom: 100 µs/div.
$V_{OUT\ MAX}$ = 24.5 V
$V_{OUT\ MIN}$ = 24 V

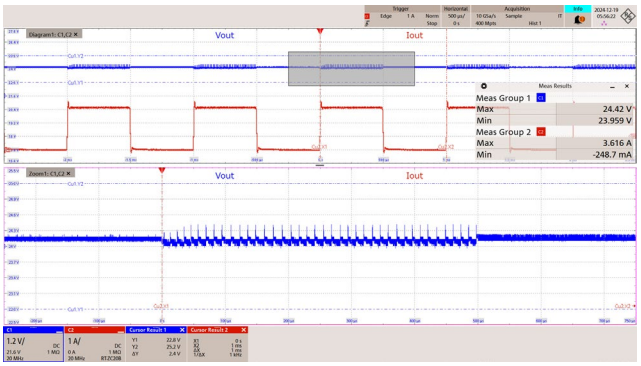


Figure 99 – 305 VAC, 50 Hz. 24 V / 0 A - 3.13 A Transient
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_{OUT}, 1 A / div., 500 µs / div.
Zoom: 100 µs/div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V

14.7 Input Line On/Off Cycling Test

Set up: 1 s AC on, 1 s AC off

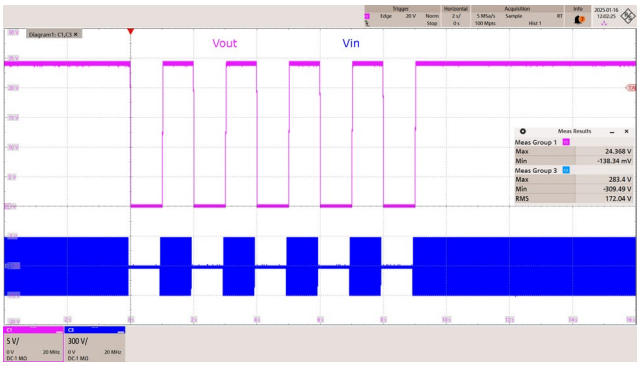


Figure 100 – 198 VAC, 50 Hz. 24 V / 3.13 A
CH1: V_{OUT}, 5 V / div., 2 s / div.
CH3: V_{IN}, 300 V / div., 2 s / div.
Remarks: Output recovers upon re-application of AC

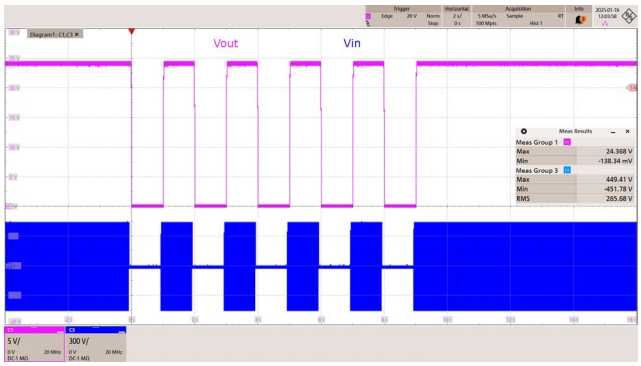


Figure 101 – 305 VAC, 50 Hz. 24 V / 3.13 A
CH1: V_{OUT}, 5 V / div., 2 s / div.
CH3: V_{IN}, 300 V / div., 2 s / div.
Remarks: Output recovers upon re-application of AC

14.8 Output Ripple Voltage Waveforms

14.8.1 Ripple Measurement Technique

To conduct output ripple measurements, a modified oscilloscope test probe must be used to reduce spurious signals caused by noise pickup.

A 4987BA probe adapter was equipped with two capacitors connected in parallel across the probe tip. These capacitors are one 0.1 μF/50 V ceramic type and one 47 μF/50 V aluminum-electrolytic type. Since the aluminum electrolytic capacitor is polarized, proper polarity must be maintained across DC outputs (refer to figure 102 below).

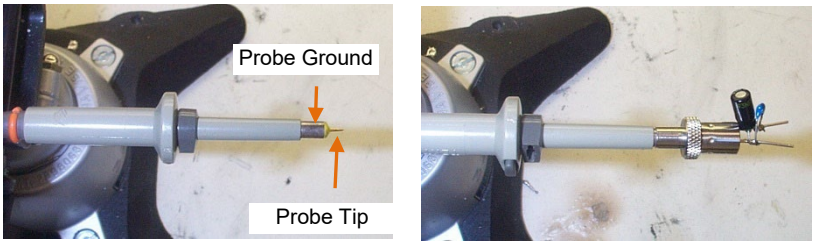


Figure 102 – Ripple voltage probe using Probe Master 4987A BNC Adapter.

14.8.2 Output Ripple Voltage at 100% Load

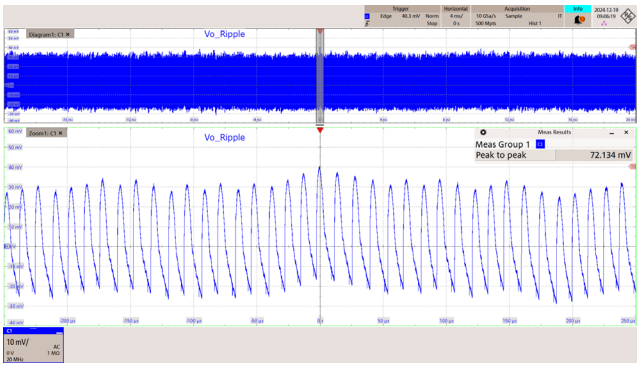


Figure 103 – 198 VAC, 50 Hz. 24 V / 100% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 72.1 mVp-p

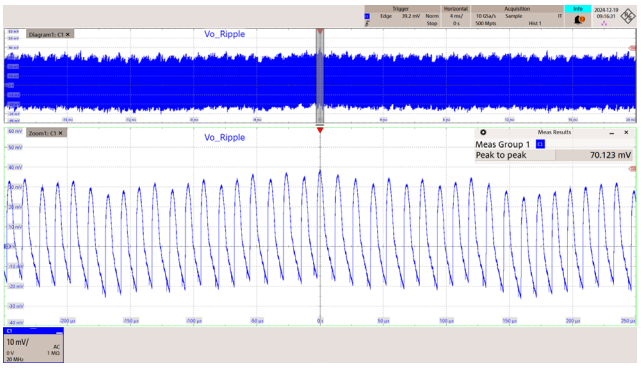


Figure 104 – 230 VAC, 50 Hz. 24 V / 100% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 70.1 mVp-p

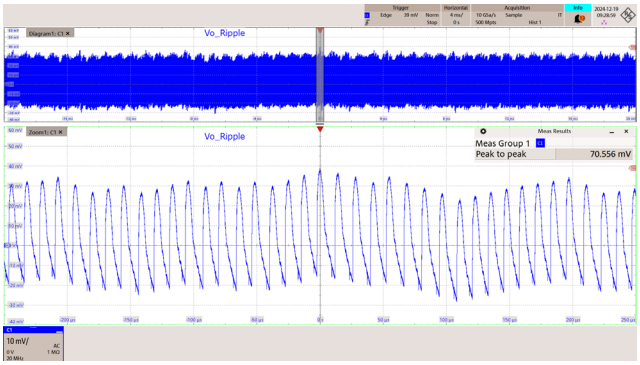


Figure 105 – 277 VAC, 50 Hz. 24 V / 100% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 70.6 mVp-p

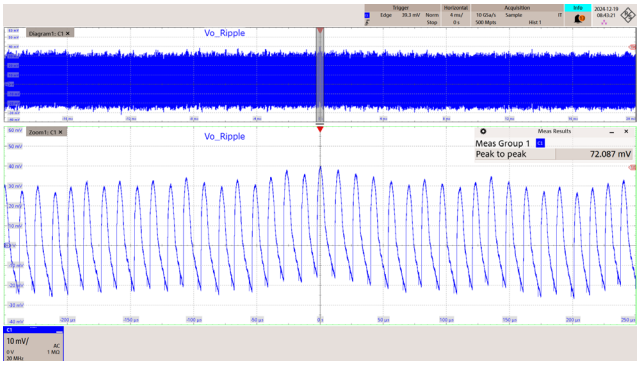


Figure 106 – 305 VAC, 50 Hz. 24 V / 100% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 72.1 mVp-p

14.8.3 Output Ripple Voltage at 80% Load

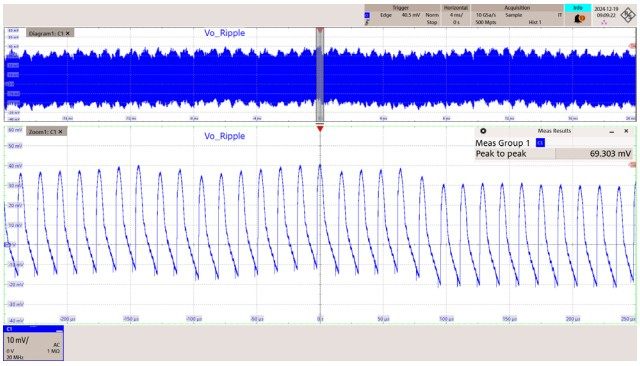


Figure 107 – 198 VAC, 50 Hz. 24 V / 80% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 69.3 mVp-p

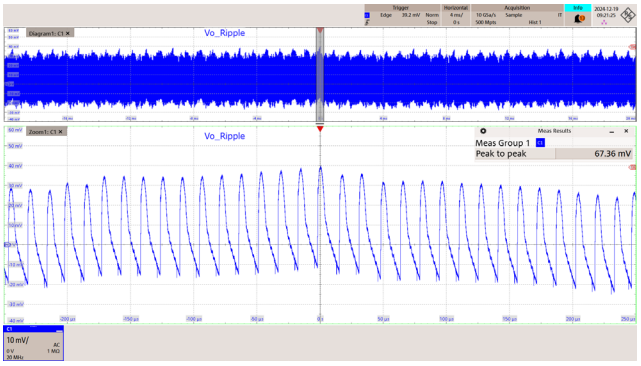


Figure 108 – 230 VAC, 50 Hz. 24 V / 80% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 67.4 mVp-p

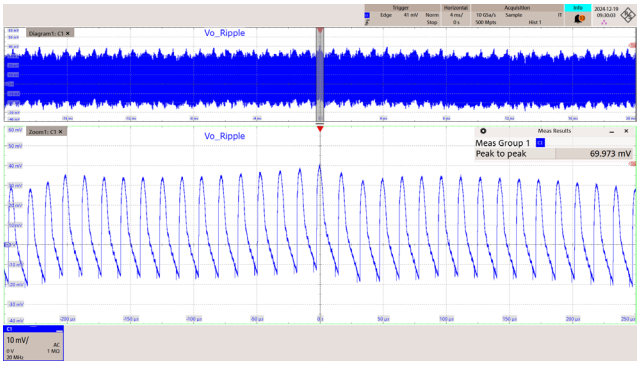


Figure 109 – 277 VAC, 50 Hz. 24 V / 80% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 70 mVp-p

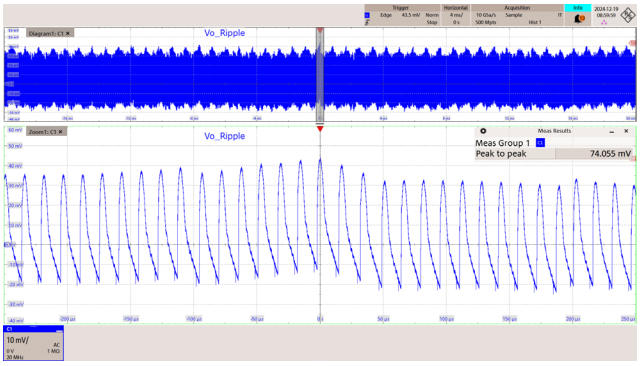


Figure 110 – 305 VAC, 50 Hz. 24 V / 80% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 74 mVp-p

14.8.4 Output Ripple Voltage at 60% Load

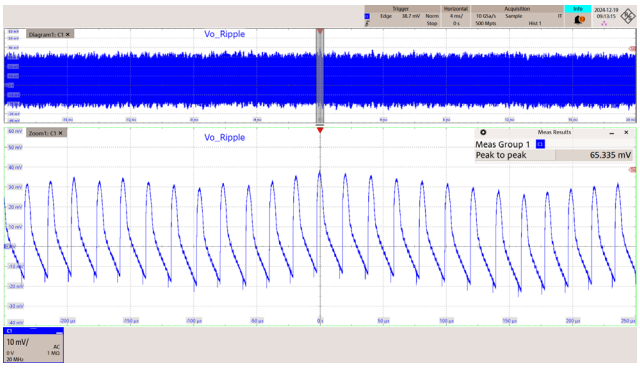


Figure 111 – 198 VAC, 50 Hz. 24 V / 60% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 65.3 mVp-p

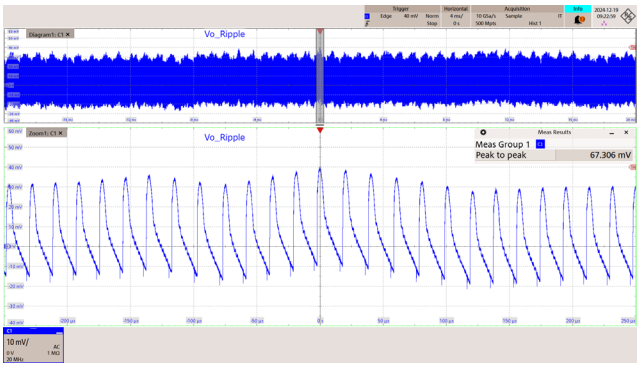


Figure 112 – 230 VAC, 50 Hz. 24 V / 60% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 67.3 mVp-p

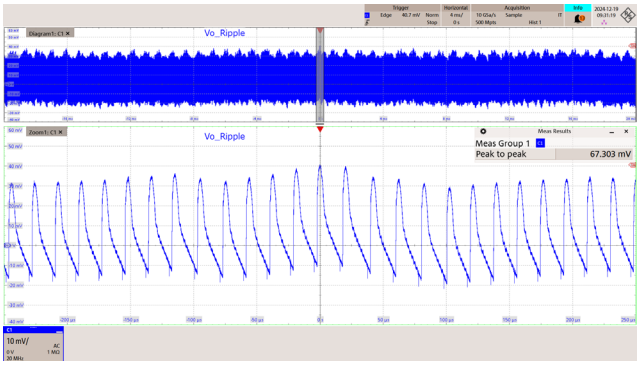


Figure 113 – 277 VAC, 50 Hz. 24 V / 60% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 67.3 mVp-p

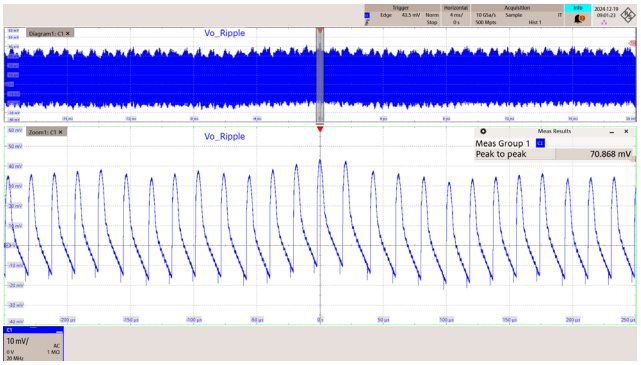


Figure 114 – 305 VAC, 50 Hz. 24 V / 60% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 µs/div.
V_{RIPPLE} = 70.9 mVp-p

14.8.5 Output Ripple Voltage at 40% Load

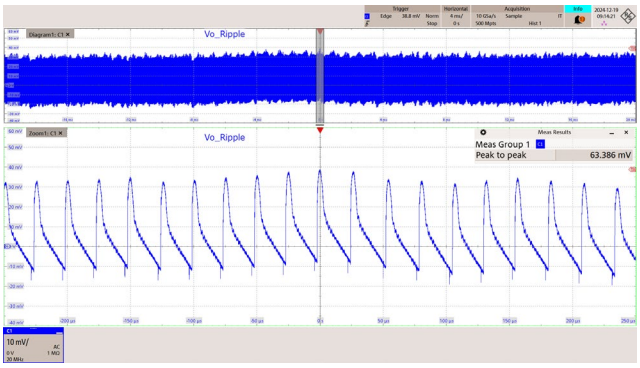


Figure 115 – 198 VAC, 50 Hz. 24 V / 40% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 63.4 mVp-p

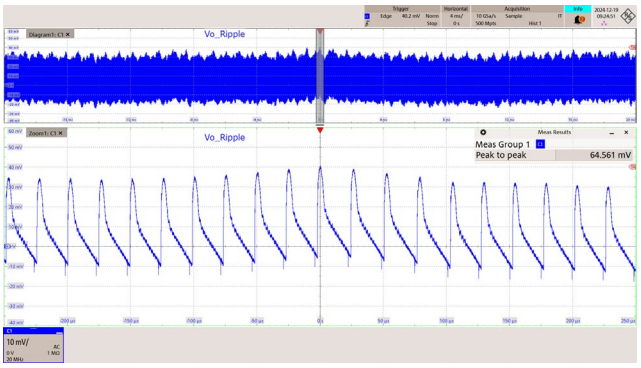


Figure 116 – 230 VAC, 50 Hz. 24 V / 40% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 64.6 mVp-p

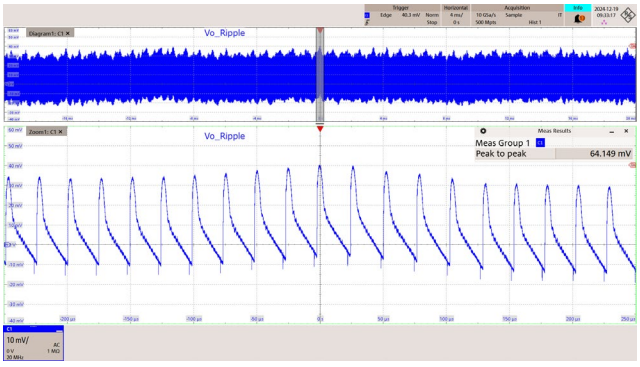


Figure 117 – 277 VAC, 50 Hz. 24 V / 40% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 64.2 mVp-p

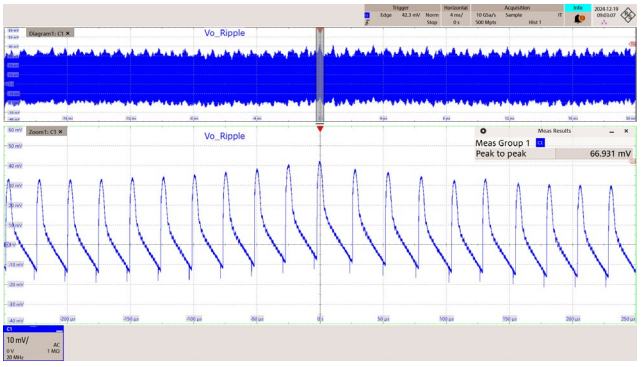


Figure 118 – 305 VAC, 50 Hz. 24 V / 40% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 66.9 mVp-p

14.8.6 Output Ripple Voltage at 20% Load

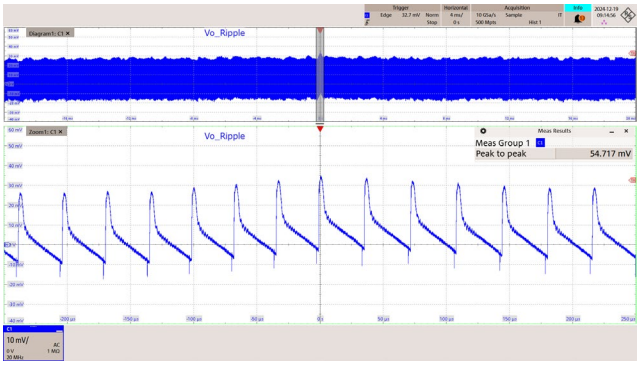


Figure 119 – 198 VAC, 50 Hz. 24 V / 20% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 54.7 mVp-p

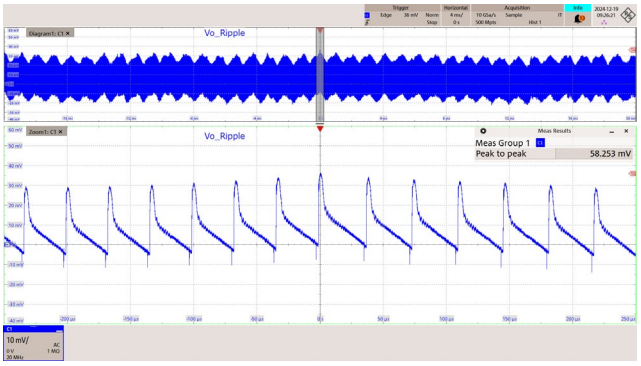


Figure 120 – 230 VAC, 50 Hz. 24 V / 20% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 58.3 mVp-p

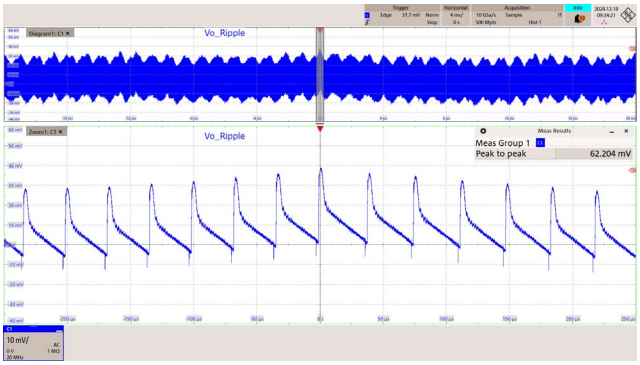


Figure 121 – 277 VAC, 50 Hz. 24 V / 20% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 62.2 mVp-p

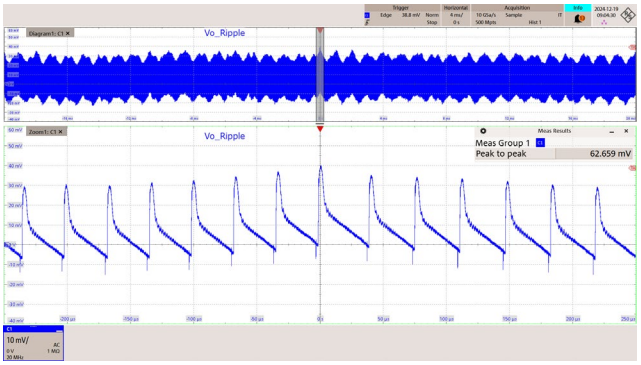


Figure 122 – 305 VAC, 50 Hz. 24 V / 20% Load
CH1: Ripple, 10 mV / div., 4 ms / div.
Zoom: 50 μs/div.
V_{RIPPLE} = 62.7 mVp-p

14.9 Output Overvoltage Protection

Using a mechanical switch, a 15.4 KΩ resistor was connected between the FB pin and GND to trigger an OVP event.

14.9.1 Output OVP Waveforms

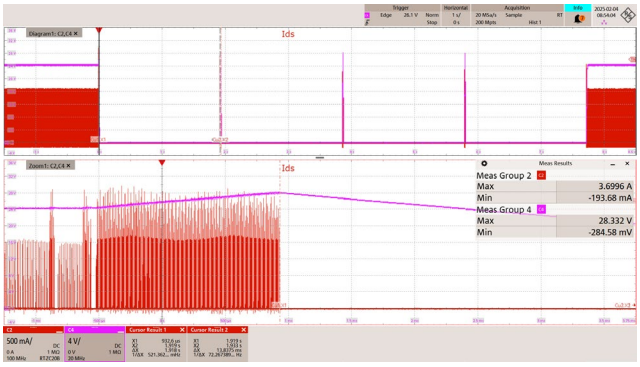


Figure 123 – 198 VAC, 50 Hz. 3.13 A Output OVP
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 500 µs / div.
$V_{OUT\ MAX}$ = 28.3 V
$I_{DS\ MAX}$ = 3.70 A

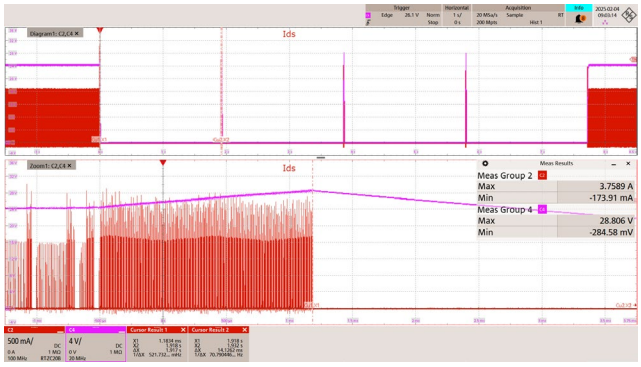


Figure 124 – 305 VAC, 50 Hz. 3.13 A Output OVP
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 500 µs / div.
$V_{OUT\ MAX}$ = 28.8 V
$I_{DS\ MAX}$ = 3.76 A

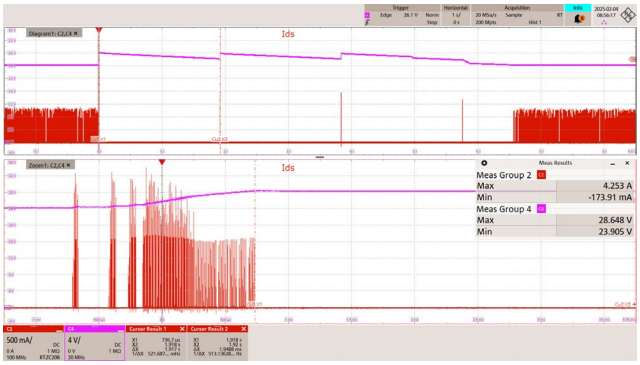


Figure 125 – 198 VAC, 50 Hz. No Load Output OVP
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 500 µs / div.
$V_{OUT\ MAX}$ = 28.7 V
$I_{DS\ MAX}$ = 4.25 A

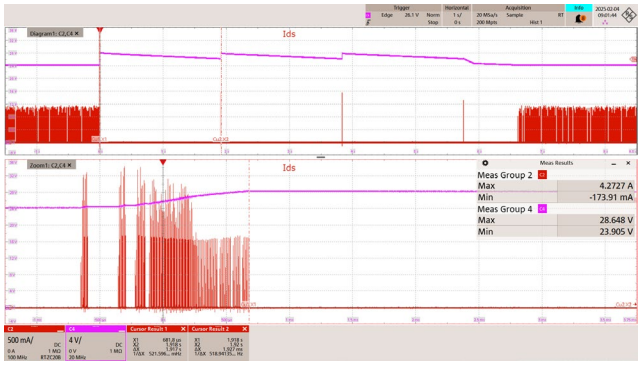


Figure 126 – 305 VAC, 50 Hz. No Load Output OVP
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 500 µs / div.
$V_{OUT\ MAX}$ = 28.7V
$I_{DS\ MAX}$ = 4.27 A

14.10 Over-Current Protection

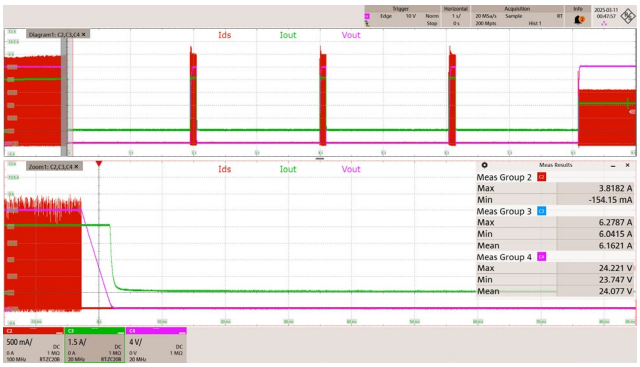


Figure 127 – 198 VAC, 50 Hz. 24 V / 6 A
Over-current
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: I_{OUT}, 1.5 A / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 10 ms / div.
$V_{OUT\ MAX}$ = 24.1 V
$I_{OUT\ MAX}$ = 6.16 A
$I_{DS\ MAX}$ = 3.82 A

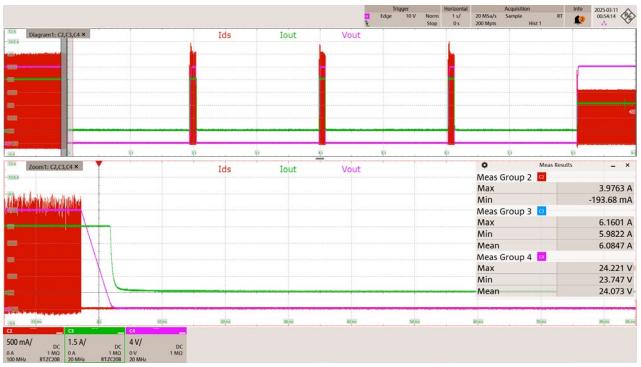


Figure 128 – 305 VAC, 50 Hz. 24 V / 6 A
Over-current
CH2: I_{DS}, 500 mA / div., 1 s / div.
CH4: I_{OUT}, 1.5 A / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 10 ms / div.
$V_{OUT\ MAX}$ = 24.1 V
$I_{OUT\ MAX}$ = 6.08 A
$I_{DS\ MAX}$ = 3.98 A

15 Constant Voltage PWM Dimming

Dimming is achieved by varying the duty cycle of the output current. The dimming performance was demonstrated using a constant voltage DALI dimmer, ranging from 0.1% to 100% PWM duty cycle.

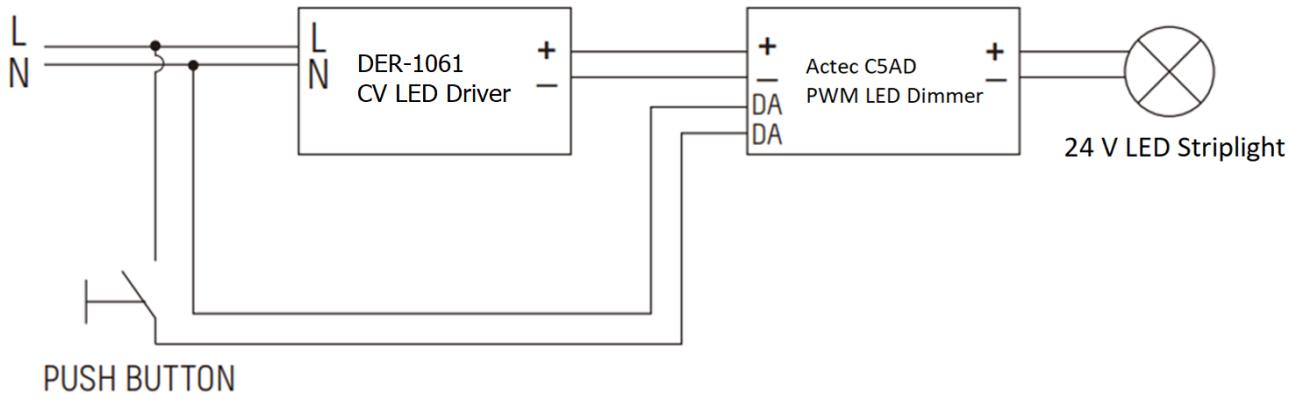


Figure 129 – PWM LED Dimming Test Set-up.

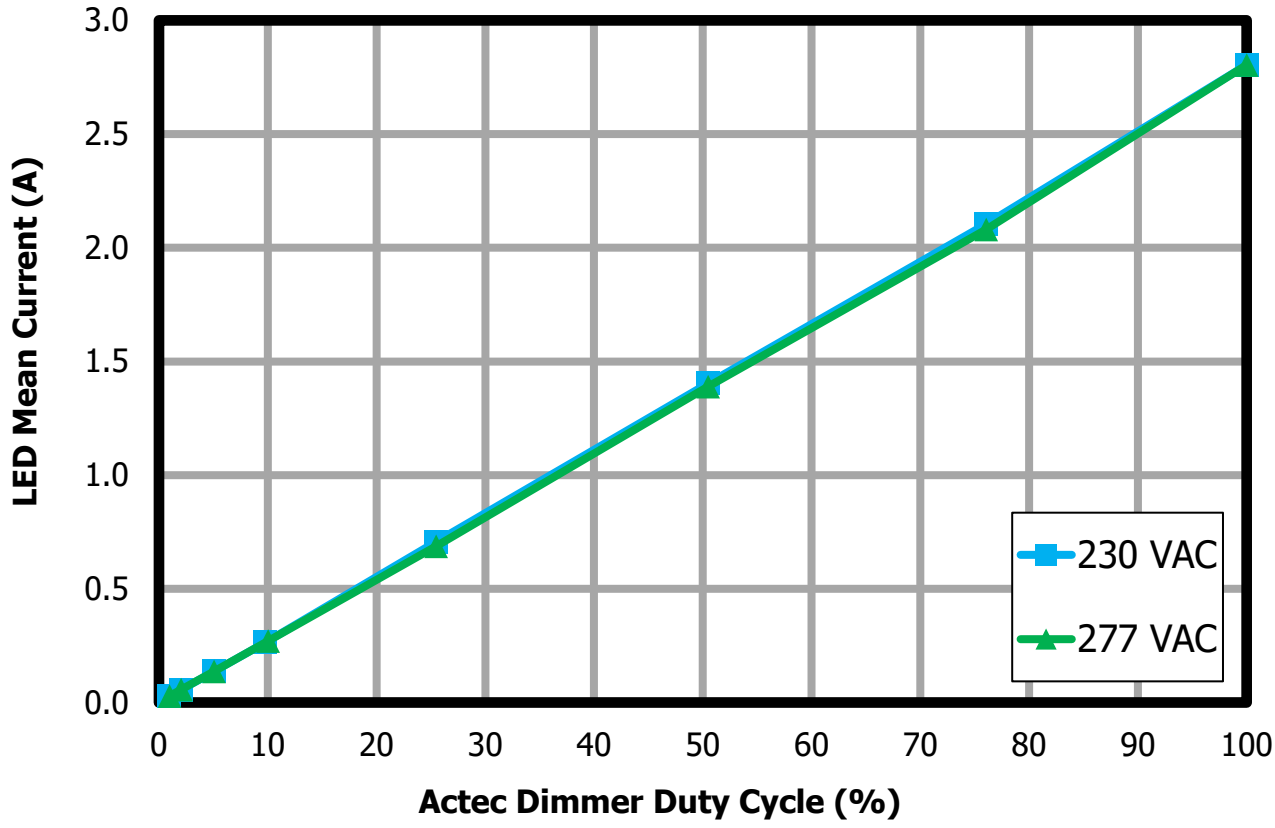


Figure 130 – Dimming Performance.

15.1 PWM Dimming Waveforms at 230 VAC

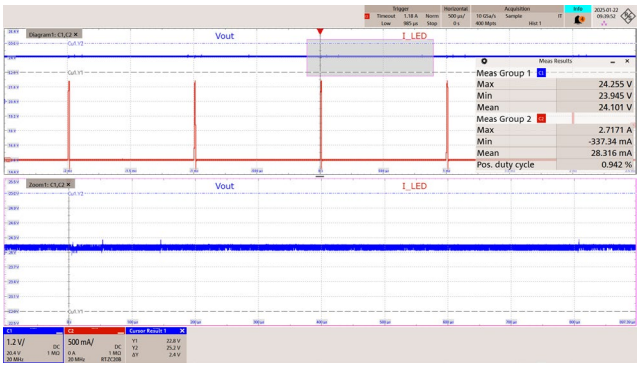


Figure 131 – 230 VAC, 50 Hz. 24 V LED
1% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.72 A
$I_{LED\ MEAN}$ = 28.3 mA

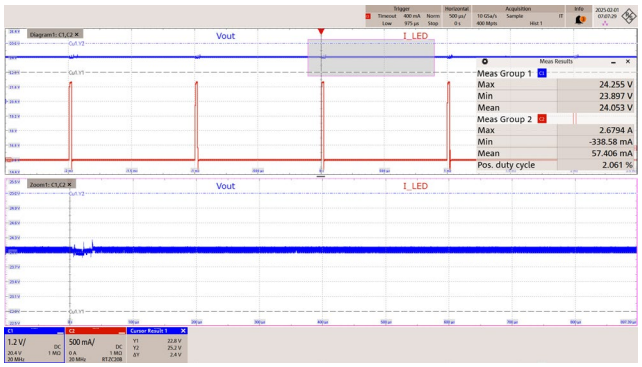


Figure 132 – 230 VAC, 50 Hz. 24 V LED
2% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 23.9 V
$I_{LED\ MAX}$ = 2.68 A
$I_{LED\ MEAN}$ = 57.4 mA

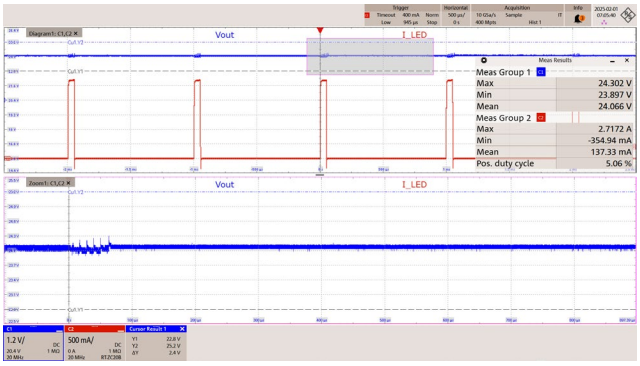


Figure 133 – 230 VAC, 50 Hz. 24 V LED
5% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 23.9 V
$I_{LED\ MAX}$ = 2.72 A
$I_{LED\ MEAN}$ = 137 mA

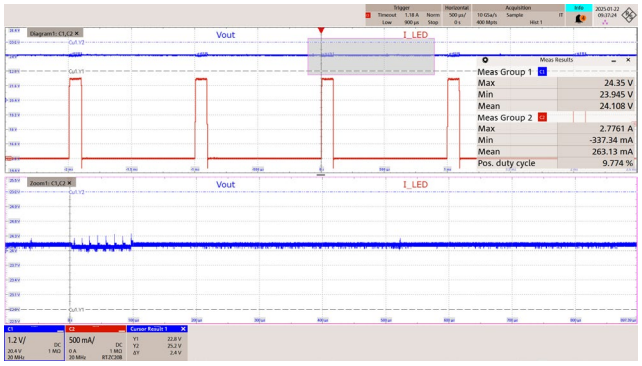


Figure 134 – 230 VAC, 50 Hz. 24 V LED
10% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.78 A
$I_{LED\ MEAN}$ = 263 mA

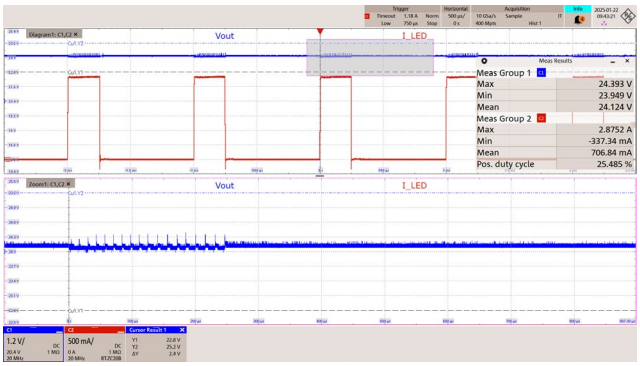


Figure 135 – 230 VAC, 50 Hz. 24 V LED 25% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.88 A
$I_{LED\ MEAN}$ = 707 mA

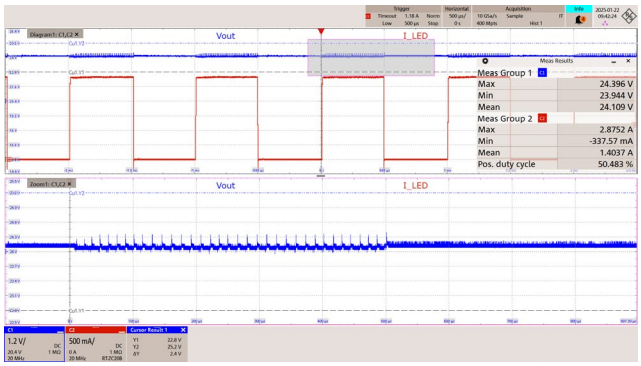


Figure 136 – 230 VAC, 50 Hz. 24 V LED 50% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 23.9 V
$I_{LED\ MAX}$ = 2.88 A
$I_{LED\ MEAN}$ = 1.40 A

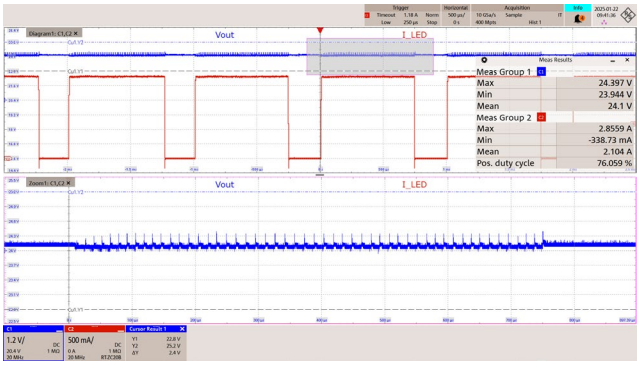


Figure 137 – 230 VAC, 50 Hz. 24 V LED 75% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.86 A
$I_{LED\ MEAN}$ = 2.10 A

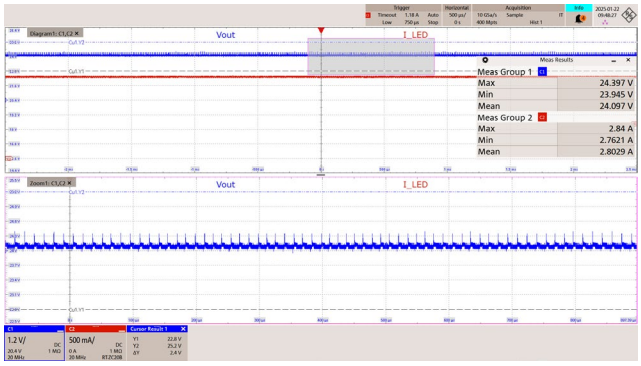


Figure 138 – 230 VAC, 50 Hz. 24 V LED 100% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.84 A
$I_{LED\ MEAN}$ = 2.80 A

15.2 PWM Dimming Waveforms at 277 VAC

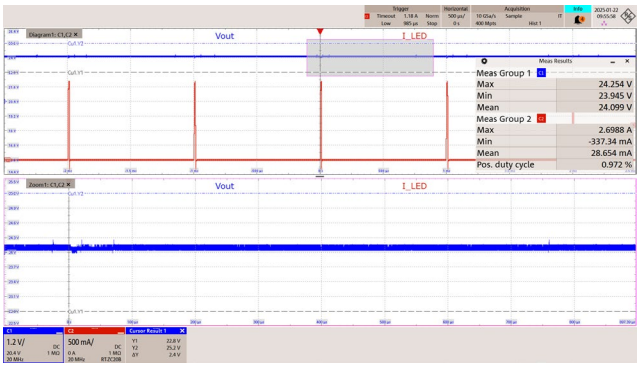


Figure 139 – 277 VAC, 50 Hz. 24 V LED
1% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.70 A
$I_{LED\ MEAN}$ = 28.7 mA

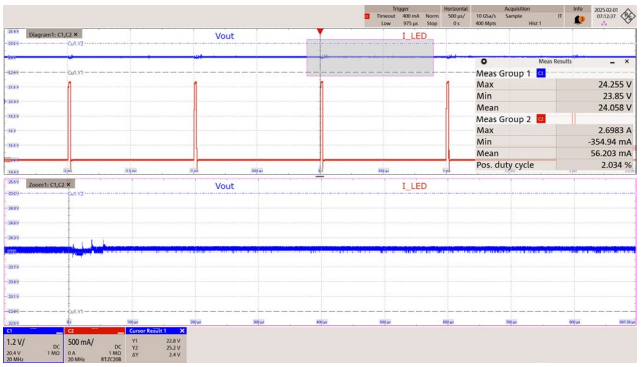


Figure 140 – 277 VAC, 50 Hz. 24 V LED
2% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 23.9 V
$I_{LED\ MAX}$ = 2.70 A
$I_{LED\ MEAN}$ = 56.2 mA

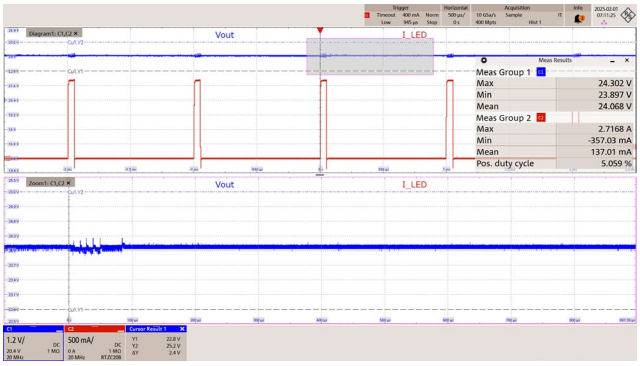


Figure 141 – 277 VAC, 50 Hz. 24 V LED
5% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.3 V
$V_{OUT\ MIN}$ = 23.9 V
$I_{LED\ MAX}$ = 2.72 A
$I_{LED\ MEAN}$ = 137 mA

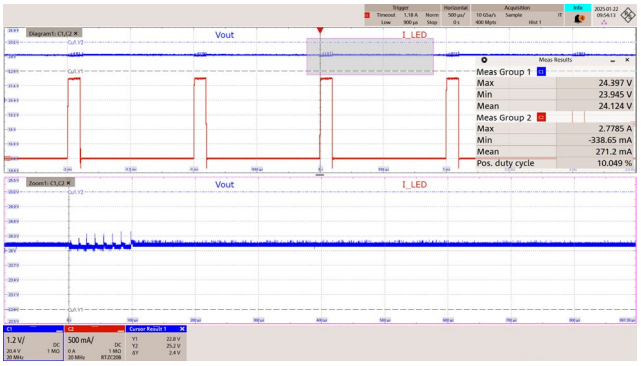


Figure 142 – 277 VAC, 50 Hz. 24 V LED
10% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.78 A
$I_{LED\ MEAN}$ = 271 mA

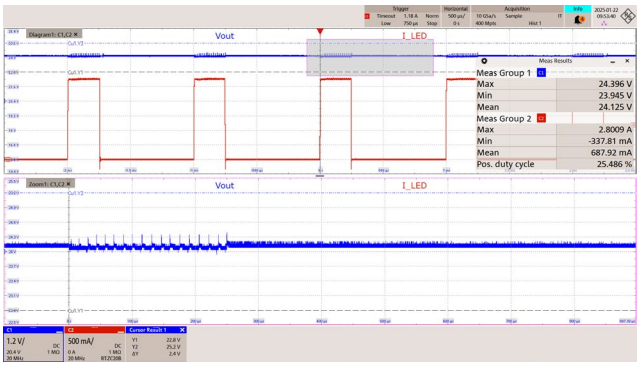


Figure 143 – 277 VAC, 50 Hz. 24 V LED
25% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.80 A
$I_{LED\ MEAN}$ = 688 mA

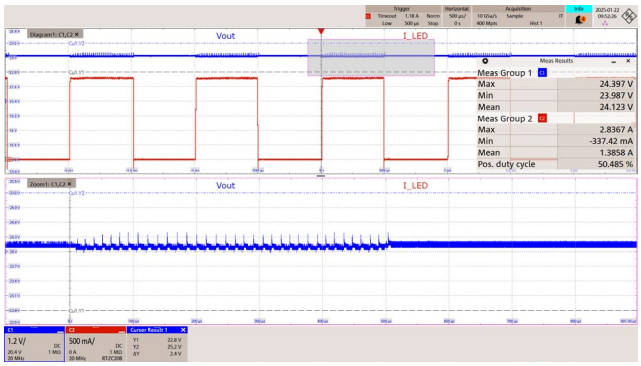


Figure 144 – 277 VAC, 50 Hz. 24 V LED
50% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.84 A
$I_{LED\ MEAN}$ = 1.39 A

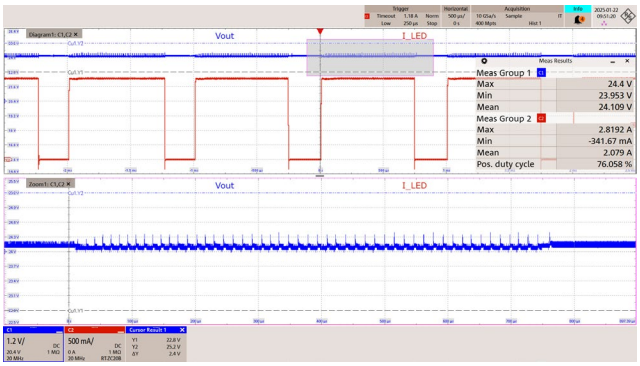


Figure 145 – 277 VAC, 50 Hz. 24 V LED
75% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.82 A
$I_{LED\ MEAN}$ = 2.08 A

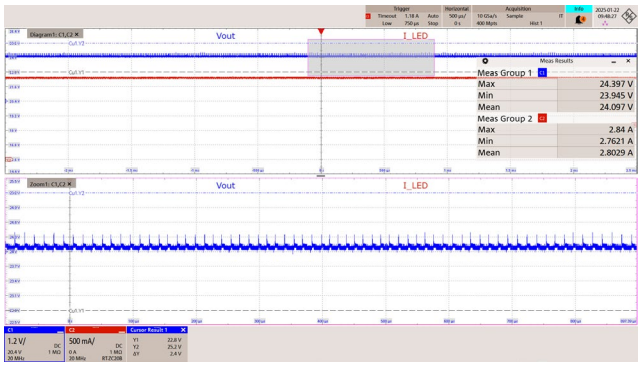


Figure 146 – 277 VAC, 50 Hz. 24 V LED
100% Duty Cycle
CH1: V_{OUT}, 1.2 V / div., 500 µs / div.
CH2: I_LED, 500 mA / div., 500 µs / div.
Zoom: 100 µs / div.
$V_{OUT\ MAX}$ = 24.4 V
$V_{OUT\ MIN}$ = 24 V
$I_{LED\ MAX}$ = 2.84 A
$I_{LED\ MEAN}$ = 2.80 A

16 Audible Noise

A microphone was placed 10 cm away from the top of the cased PSU, above the flyback transformer.

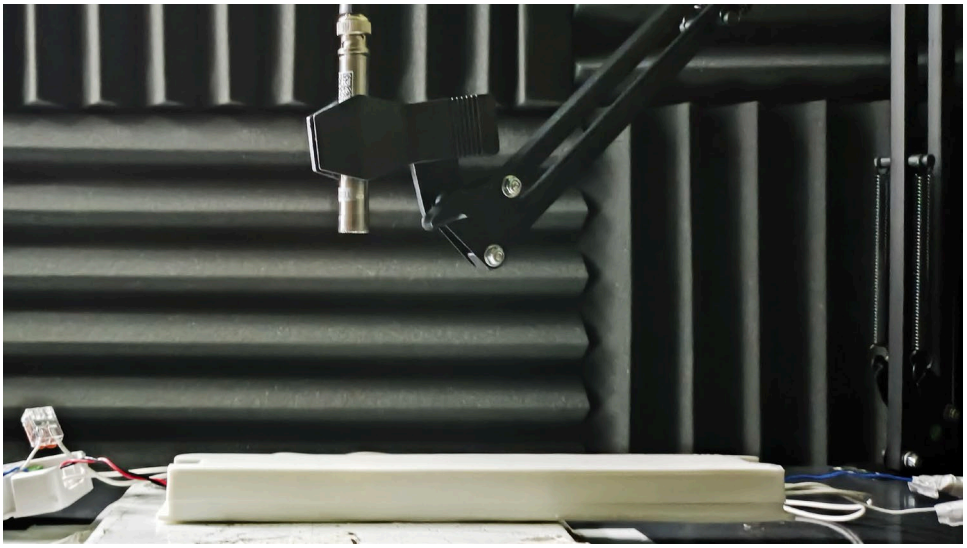


Figure 147 – Audible Noise Test Set-up.

16.1 Audible Noise Scan

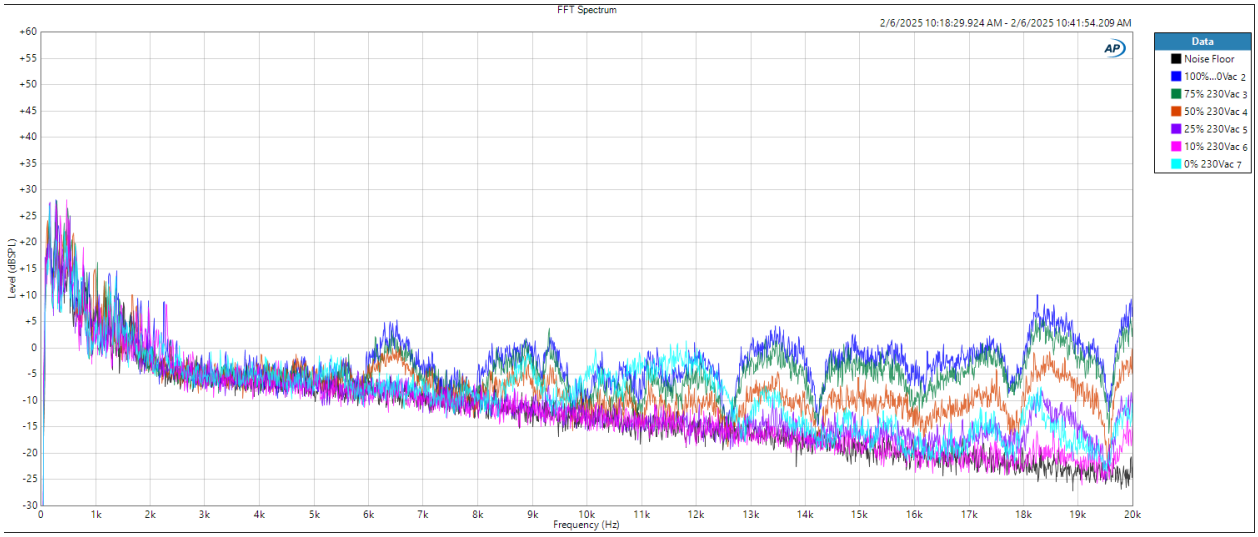


Figure 148 – 230 VAC Input, 24 V / 0-100% Load Sweep.

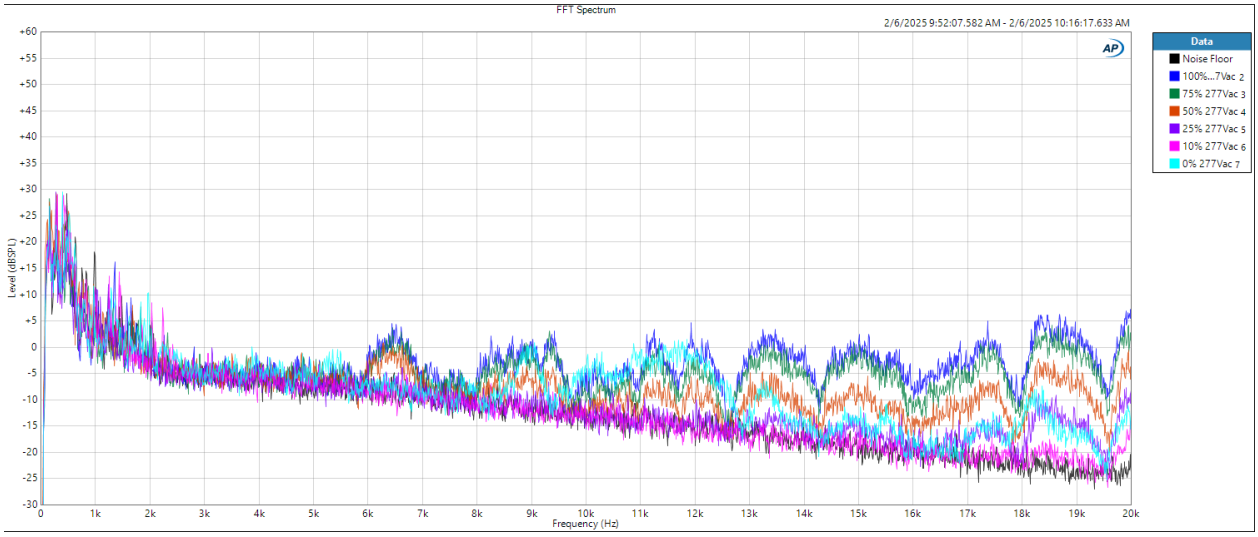


Figure 149 – 277 VAC Input, 24 V / 0-100% Load Sweep.

17 Conducted EMI

EMI scans were performed using 7.68 Ω fixed (resistive) load.

17.1 Test Set-up

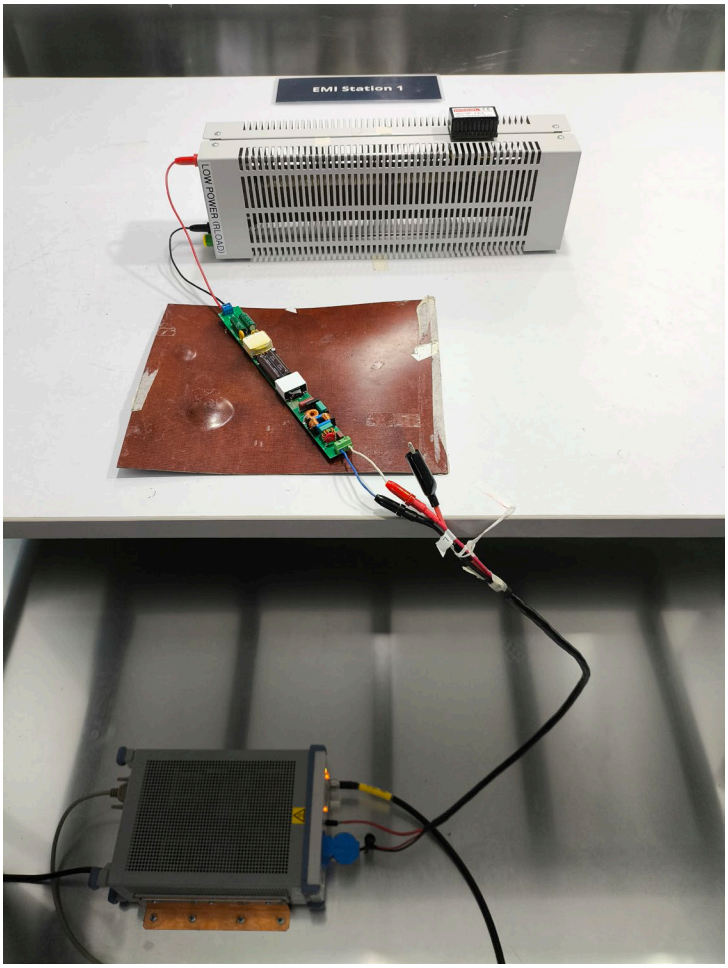
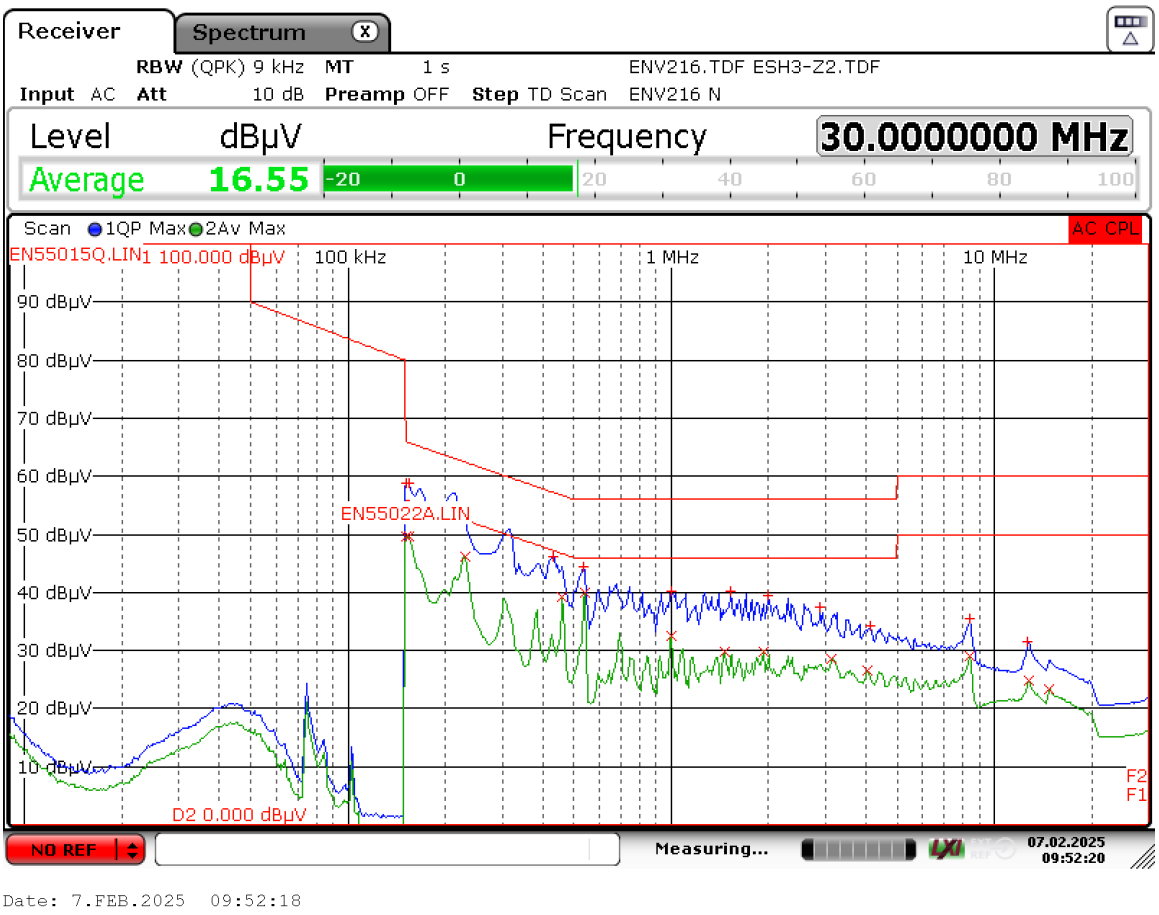


Figure 150 – Conducted EMI Test Set-up.

17.2 Floating Output



Date: 7.FEB.2025 09:52:18

Figure 151 – Conducted EMI at 24 V 3.13 A (7.68 Ω, Floating), 230 VAC.

18 Line Surge

The unit was subjected to ±2500 V ring wave and ±2000 V combination wave surges with 10 strikes for each condition. The unit would be considered to have failed if the result of the test was a non-recoverable interruption of output that require either repair or AC cycling.

18.1 Combination Wave Differential Mode Surge

AC Input Voltage (VAC)	Surge Voltage (kV)	Injection Location	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2000	L to N	0	2	10	PASS – No AR
230	-2000	L to N	0	2	10	PASS – No AR
230	+2000	L to N	90	2	10	PASS – with AR
230	-2000	L to N	90	2	10	PASS – with AR
230	+2000	L to N	180	2	10	PASS – No AR
230	-2000	L to N	180	2	10	PASS – No AR
230	+2000	L to N	270	2	10	PASS – with AR
230	-2000	L to N	270	2	10	PASS – with AR

Note: output recovered after AR

Table 18 – Combination Wave Differential Mode Surge.

18.2 Ring Wave Surge

18.2.1 Ring Wave Differential Mode Surge

AC Input Voltage (VAC)	Surge Voltage (kV)	Injection Location	Phase Angle (º)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2500	L to N	0	12	10	PASS – No AR
230	-2500	L to N	0	12	10	PASS – No AR
230	+2500	L to N	90	12	10	PASS – No AR
230	-2500	L to N	90	12	10	PASS – No AR
230	+2500	L to N	180	12	10	PASS – No AR
230	-2500	L to N	180	12	10	PASS – No AR
230	+2500	L to N	270	12	10	PASS – No AR
230	-2500	L to N	270	12	10	PASS – No AR

Table 19 – Ring Wave Differential Mode Surge.

18.2.2 Ring Wave Common Mode Surge

AC Input Voltage (VAC)	Surge Voltage (kV)	Injection Location	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2500	L,N to P.E.	0	12	10	PASS – No AR
230	-2500	L,N to P.E.	0	12	10	PASS – No AR
230	+2500	L,N to P.E.	90	12	10	PASS – No AR
230	-2500	L,N to P.E.	90	12	10	PASS – No AR
230	+2500	L,N to P.E.	180	12	10	PASS – No AR
230	-2500	L,N to P.E.	180	12	10	PASS – No AR
230	+2500	L,N to P.E.	270	12	10	PASS – No AR
230	-2500	L,N to P.E.	270	12	10	PASS – No AR

Table 20 – Ring Wave Common Mode Surge.

19 Electrostatic Discharge Test (ESD)

ESD testing was conducted at 24 V output. Pass criterion: no permanent interruption of output.

19.1 Contact Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+8.8	Output +	10	PASS – with AR
230	-8.8	Output +	10	PASS – with AR
230	+8.8	Output -	10	PASS – No AR
230	-8.8	Output -	10	PASS – No AR

Note: output always recovers after AR

Table 21 – Contact Discharge.

19.2 Air Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+16.5	Output +	10	PASS – No AR
230	-16.5	Output +	10	PASS – No AR
230	+16.5	Output -	10	PASS – with AR
230	-16.5	Output -	10	PASS – No AR

Note: output always recovers after AR

Table 22 – Air Discharge.

20 Appendix

20.1 Schematic – Showing Provisional Component Positions

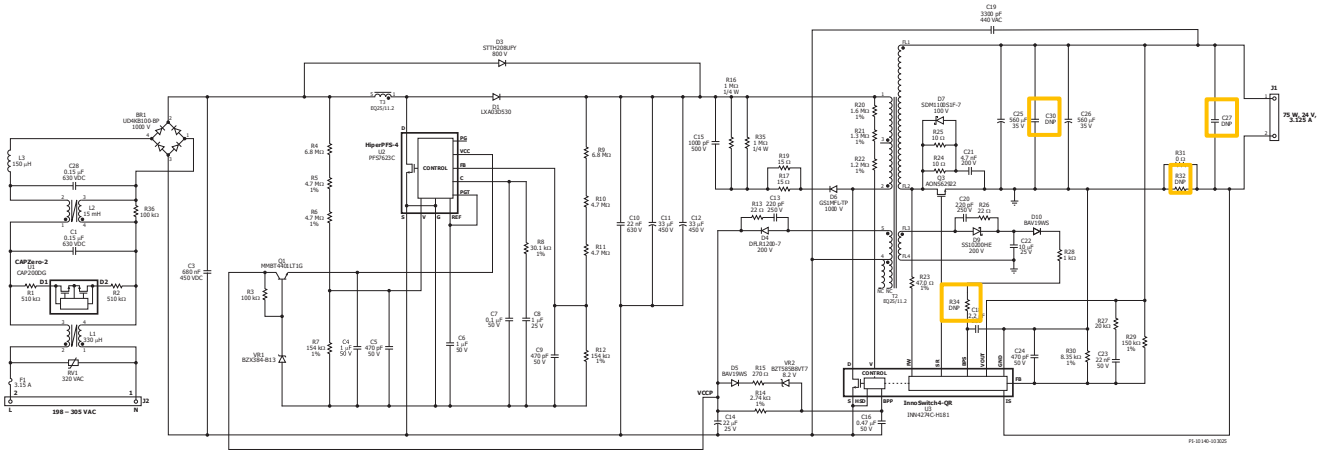


Figure 152 – DER1061 Complete Schematic.

DNP are optional components. These optional components allow modifications to be made to the power supply.

- C27 and C30 – Location for additional capacitor to reduce output ripple
- R32 – R_{SENSE} together with R31 for optional OCP function
- R34 – Supply BPS from the output if secondary bias is not used

20.2 Optional OCP using R_{SENSE}

20.2.1 Circuit Description

Current sense resistors R31 (40 mΩ) and R32 (11 mΩ), which would be connected to the IS pin of the InnoSwitch4 IC, and would set the OCP threshold close to 4 A. The InnoSwitch4-QR IC enters auto-restart if the voltage across the sense resistor reaches $I_{SV(TH)}$ (36 mV).

A Schottky diode D11 (B340A-13-F) – in parallel to current sense resistors, protects the IS pin during output short by keeping the voltage below 500 mV. Lowpass filter R37 (10 Ω) and C29 (4.7 μF) also protects IS pin by reducing the transient voltage seen during the high current surge experienced during an output short.

20.2.2 DER-1061 OCP Modification to Accommodate Optional Components

20.2.2.1 Top Side Re-work

Trace from R31 to IS pin needs to be cut to accommodate R37.

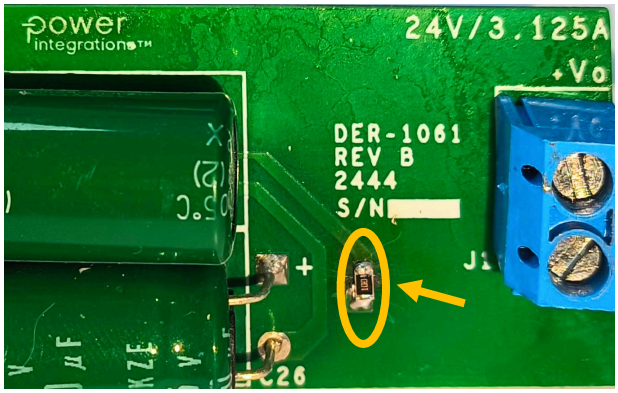


Figure 153 – Re-worked DER1061, Top.

20.2.2.2 Bottom Side Re-work

R31 and R32 are mounted on top of each other.
D11 soldered in R32 location.
C29 soldered between IS pin and C18 GND.

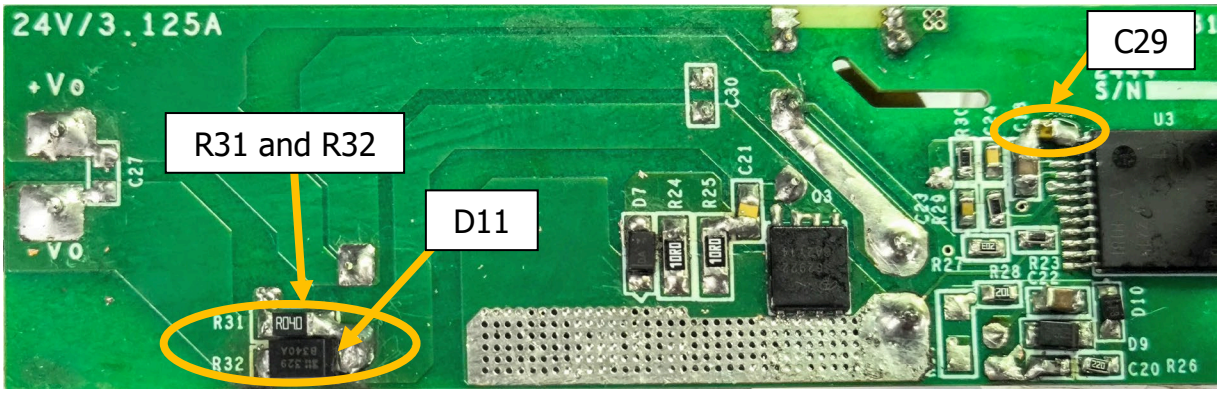


Figure 154 – Re-worked part of DER1061, Bottom.

20.2.3 OCP using R_{SENSE}

Figure 155 – 198 VAC, 50 Hz. 24 V / 4 A Over-current
CH2: I_{DS}, 750 mA / div., 1 s / div.
CH4: I_{OUT}, 1 A / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 10 ms / div.
$V_{OUT\ MAX}$ = 24.4 V
$I_{OUT\ MAX}$ = 4.02 A
$I_{DS\ MAX}$ = 4.1 A

Figure 156 – 305 VAC, 50 Hz. 24 V / 4 A Over-current
CH2: I_{DS}, 750 mA / div., 1 s / div.
CH4: I_{OUT}, 1 A / div., 1 s / div.
CH4: V_{OUT}, 4 V / div., 1 s / div.
Zoom: 10 ms / div.
$V_{OUT\ MAX}$ = 24.4 V
$I_{OUT\ MAX}$ = 4.04 A
$I_{DS\ MAX}$ = 4.54 A

21 Revision History

Date	Author	Revision	Description & Changes	Reviewed
3-Nov-25	MM/JKB	A	Initial Release.	RPA & Mktg

For the latest updates, visit our website: www.power.com

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