Design Example Report

Title	**100 W 24 V Low Profile LED Driver Using CAPZero-2, HiperPFS-4 and PowiGaN-Based InnoSwitch4-QR ICs**
Specification	Input: 198 VAC – 305 VAC Nominal Output: 24 V / 4.17 A
Application	LED Driver, Smart Lighting
Author	Applications Engineering Department
Document Number	DER-1038
Date	April 28, 2026
Revision	B

Summary and Features

- 100 W Constant Voltage LED Driver
- > 92% full load efficiency @ 230 VAC
  - Easily meets DOE6 and CoC Tier 2 efficiency requirements
- Low profile < 16 mm high
- Low components count (62 parts)
- Power factor correction stage
  - High power factor, > 0.93 from 230 - 277 VAC
  - Low THD, < 10 % from 230 - 277 VAC
- DC-DC conversion stage
  - High efficiency eliminates heatsinks
- Protection Features
    - Fast input line UV/OV protection
    - Output over-current, overvoltage and undervoltage protection
    - Over-temperature protection (OTP)
- Meets 2.5 kV combination and 4 kV ring-wave differential surge

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a two-stage, 100 W isolated flyback power supply that utilizes the HiperPFS™-4 Boost Power Factor Correction (PFC) IC and the InnoSwitch4™-QR flyback IC. The power supply can deliver a continuous output of 24 V / 4.17 A within an input range of 198 VAC to 305 VAC.

The HiperPFS-4 devices incorporate a continuous conduction mode (CCM) boost PFC controller and 600 V power MOSFET in a single, low-profile power package.

The InnoSwitch4™-QR IC combines a high-voltage PowiGaN™ switch with both primary-side and secondary-side controllers in a single, low-profile IC package.

The power supply is designed for LED strip-light applications and utilizes low-profile components to meet typical form factor requirements.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

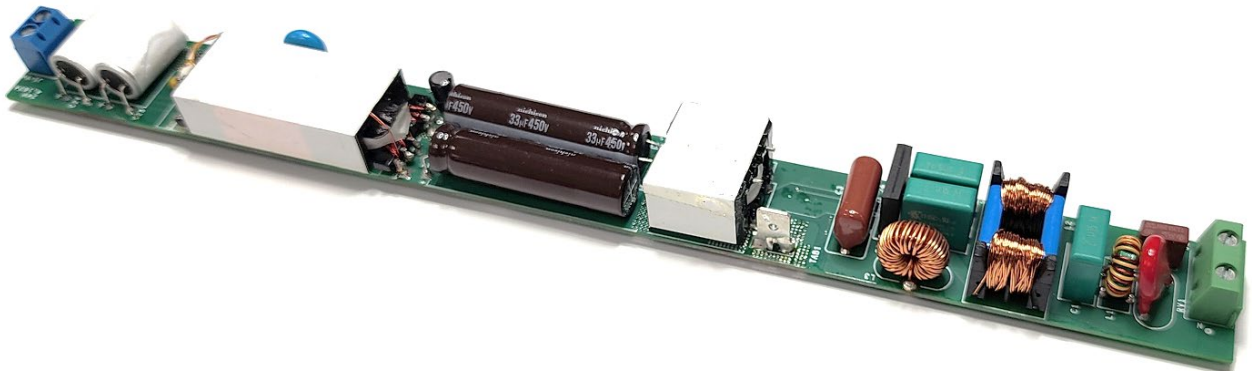


Figure 1 – Populated Circuit Board Photograph

Figure 2 – Populated Circuit Board Photograph, Top Side

Figure 3 – Populated Circuit Board Photograph, Bottom Side

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						2 Wire – no P.E.
Voltage	V_{IN}	198		305	VAC	198 V – 305 V Continuous
Low Voltage Withstand	V_{IN}	140				5 mins at full load
Frequency	f_{LINE}		50/60		Hz	see the configuration in the appendix
Output Voltage	V_{OUT}		24		V	±3%
Output Voltage Ripple	V_{RIPPLE}			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	I_{OUT}			4.17	A	±3%
Full Load Efficiency	η		92		%	230 VAC, V_{OUT} is measured on the Board.
Continuous Output Power	$P_{OUT(28\ V)}$			130	W	
Conducted EMI		Meets CISPR22B / EN55022B				Floating or Grounded Load
Operating Ambient Temperature	T_{AMB}	0		55	°C	Free Convection, Sea Level.
Immunity	**Combination Wave**			2.5	kV	Differential Mode
	Ring Wave			4	kV	Differential Mode
	ESD			15	kV	No damage Component

Table 1 – Power Supply Specification

3 Schematic

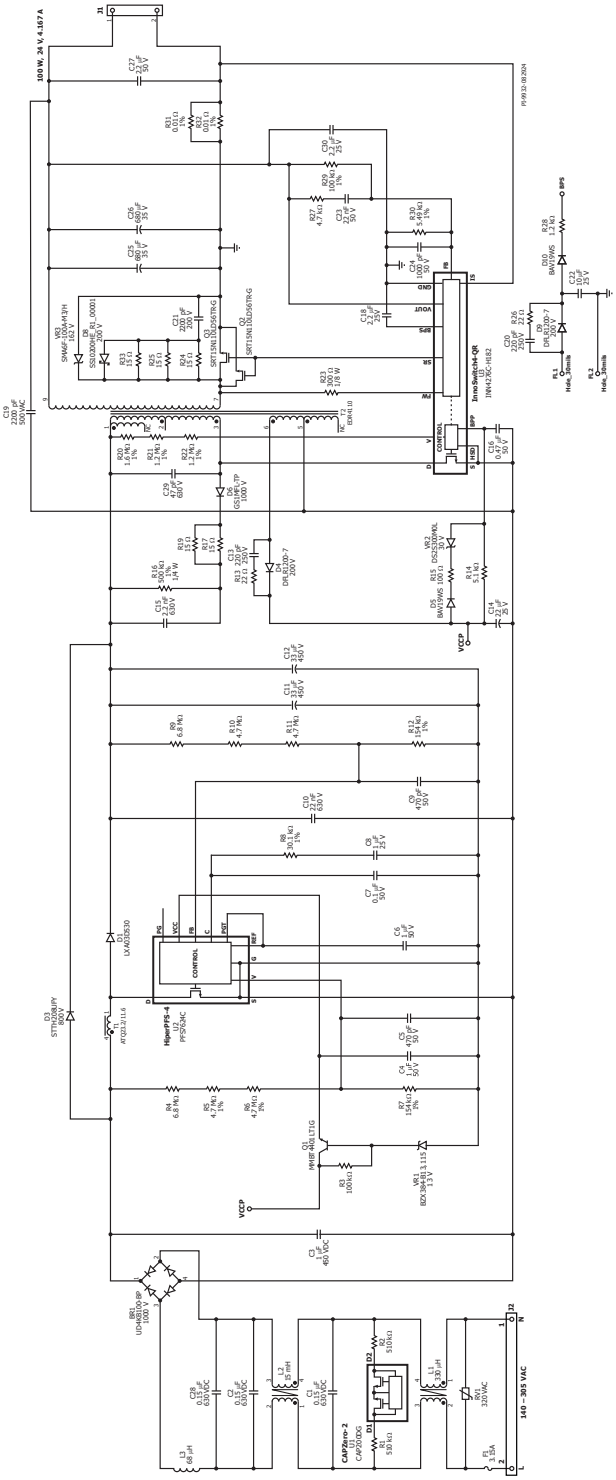


Figure 4 – Schematic Showing PFC and DC-DC isolated flyback Conversion Stages

4 Circuit Description

4.1 Input Rectification and EMI Filtering

Fuse F1 isolates the Power Supply Unit (PSU) circuitry and provides protection from component failure. RV1 protects the circuit from high voltage differential surges. The common-mode chokes L1 and L2, along with the differential choke L3 and X-capacitors C1, C2, and C28, attenuate common-mode and differential-mode noise. C3 provides differential mode Electromagnetic Interference (EMI) filtering. The value of C3 was optimized to balance conducted EMI with power factor.

4.2 Zero Loss Automatic X-Capacitor Discharge CAPZero™-2

To satisfy the safety Separated Extra Low Voltage (SELV) when the AC supply is disconnected, the CAP200DG (U1) automatically discharges the X capacitors C1 and C2 to a safe (SELV) level by connecting discharge resistors R1 and R2. When AC voltage is applied, the CAP200DG (U9) blocks current flow in the X capacitor safety discharge resistors, reducing power loss to less than 5 mW.

4.3 Boost PFC using HiperPFS-4 device

The PFC circuit shown in schematic Figure 4 was designed using a PFS7624C device from the HiperPFS-4 family of integrated PFC controllers. This design is rated for a continuous output power of 108 W and provides a nominal regulated output voltage of 400 V, maintaining a high input power factor and high efficiency across load and input line. Boost inductor T1 and boost diode D1, in conjunction with the HiperPFS-4 IC U2, form the boost converter stage, controlling the input current of the power supply while simultaneously regulating the output DC voltage.

Diode D2 limits the imposition of a resonance-induced-voltage on BR1 during start-up by bypassing inductor T1 and charging output capacitors C11 and C12. Capacitor C10 is used to reduce EMI and prevent voltage overshoot between the drain and source of the MOSFET inside U2. The PFS7624C IC requires a regulated supply of 12 V for normal operation (15 V max) which is provided by the flyback stage. Resistor R3, Zener diode VR1, and transistor Q1 form a series pass regulator that provides a 12 V regulated supply to the PFS7624C IC. Capacitor C4 filters the supply voltage and provides bypassing and decoupling to ensure reliable operation.

The power good function is not used in this design, so the POWER GOOD THRESHOLD pin is tied to the REFERENCE pin. IC U2 is configured in full-power mode by capacitor C6, which is connected to the REFERENCE pin. The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R4 - R7. These resistor values are large to minimize power consumption. Capacitor C5, connected in parallel with the bottom resistor R7, prevents noise being introduced into the VOLTAGE MONITOR pin. The output voltage divider network comprising resistors R9 - R12 is used to scale the output voltage and

provide feedback to the IC. Capacitor C9, in parallel with resistor R12, attenuates high-frequency noise. Components R8, C8, and C7 are required for shaping the loop response of the feedback network.

4.4 InnoSwitch4-QR Primary

This DC-DC stage is an isolated flyback converter. One end of the primary winding of transformer (T2) is connected to the rectified DC bus, while the other end is connected to the DRAIN pin of the power switch in InnoSwitch4-QR IC (U3).

Rectifier diode D6, resistors R16, R17, and R19, along with capacitor C15, form a primary clamp circuit that reduces the voltage spike across the primary switch during turn-off caused by leakage inductance.

C29 is added to reduce conducted EMI at full load switching frequency. RC snubber R13 and C13 help reduce radiated EMI.

The flyback controller/switch IC U3 is self-starting, using an internal high-voltage current source to charge the capacitor C16 connected to the BPP pin when high voltage DC is first applied. During normal operation, the primary-side block is powered from the primary auxiliary winding (Bias) of transformer T2. The auxiliary supply voltage is rectified by diode D4 and filtered by electrolytic capacitor C14. Bias supply current limiting resistor R14 is optimized to efficiently deliver bias current to U3 at full load.

Output regulation is achieved through cycle-by-cycle frequency and ILIM adjustment based on the output load. At high output load, the switching cycles and ILIM are higher, reducing at low output load or no-load. The value of the PRIMARY BYPASS pin capacitor (C16) sets ILIM for the IC (standard or increased). Once a cycle is enabled, the switch will remain on until the primary current ramps to the device current limit for the specific operating state.

4.5 InnoSwitch4-QR Secondary

The secondary side block of the InnoSwitch4-QR controller IC is powered by a 4.5 V (VBPS) internal regulator, which is supplied from either the VOUT or FWD Pins. The SECONDARY BYPASS pin is connected to an external decoupling capacitor C18 and is internally fed from the internal voltage regulator. To minimize the power dissipation of the internal linear regulator, an auxiliary bias supply for the BPS is added. This is formed by D9, C22, D10, and R28. Additionally, an RC snubber (C20 and R26) is connected across D9 to reduce radiated EMI.

The secondary side of the InnoSwitch4-QR IC controls output voltage, provides output current sensing, and delivers the gate-drive for the synchronous rectification MOSFET.

The transformer secondary output is rectified by Synchronous Rectifier Field-Effect Transistors (SR FETs) Q2 and Q3 and filtered by capacitors C25 and C26.

To reduce high-frequency voltage ringing during the SR FET turn-off, which would create radiated EMI and/or exceed the peak inverse voltage (PIV) rating of Q13 and Q14, RC snubber components C21, R24, R25, and R33 are employed. A Schottky rectifier diode, D8, is added to increase the efficiency of the output rectifier, improving component thermal performance, and eliminating the need for a metal heatsink. At fast transient loads, the converter initially operates in CCM, generating high leakage-inductance induced voltage spikes across the SR FET. The Transient Voltage Suppresser (TVS) diode VR3 is added to reduce voltage stress across the SR FET during fast load steps (transients).

The FORWARD pin provides input for negative-edge-detection, which is used to determine timing for the turn-on of the SR FETs Q13 and Q14. The voltage sensed by resistor R23 on the FORWARD pin is used to determine when to turn off the SR FET in discontinuous mode (DCM) operation. This occurs when the voltage across the SR FET drops below zero. In continuous conduction mode (CCM), the SR FET is turned off before a switching cycle request is sent to the primary. This provides timing for the synchronous MOSFET turn-off and ensures optimum synchronization between primary and secondary switching.

Output voltage is regulated via a reference voltage of 1.265 V on the IC FB pin. Voltage divider resistors R29 and R30 are used to set the nominal output voltage to 24 V. Additionally, the RC phase boost (C23 and R27) helps to speed up the feedback voltage sensing, thereby reducing output ripple voltage and preventing pulse grouping. C24 is added to minimize noise in the FB pin of U3.

Current sense resistors R31 and R32, which are connected to the IS pin of the InnoSwitch IC, set the Overcurrent Protection (OCP) threshold to ≤ 7 A. The InnoSwitch IC enters auto-restart if the voltage across the sense resistor reaches $I_{SV(TH)}$ (36 mV).

5 PCB Layout

The PCB uses FR4 material with a thickness of 1.6 mm and a double-sided copper layer with a thickness of 2.0 oz.

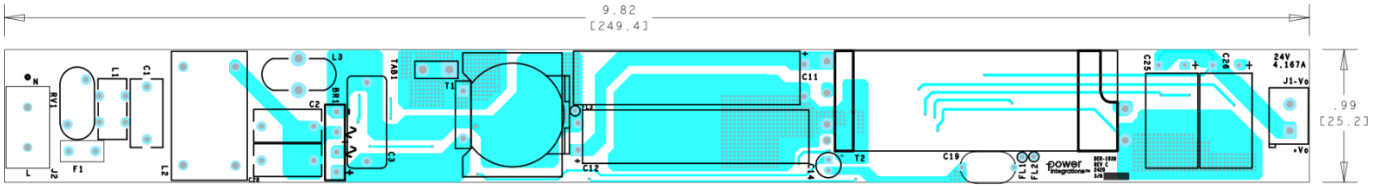


Figure 5 – Printed Circuit Layout, Top.

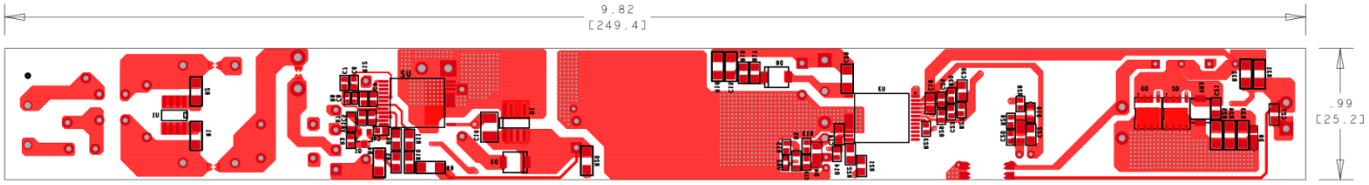


Figure 6 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item Number	Part Reference	Qty.	Description	Manufacturer Part Number	Manufacturer
1	BR1	1	Bridge Rectifier, 1000 V, 4 A, 4-ESIP, D3K, -55 °C ~ 150 °C (TJ), Vf=1 V @ 7.5 A	UD4KB100-BP	Micro Commercial Co
2	C1 C2 C28	3	CAP, 0.15 µF, ±20%, 630 VDC, 310 VAC, FILM, POLYPROP, RAD, X2, 13 mmL, 6 mmW, 12 mmH, 10mm LS	F861AP154M310L	KEMET
3	C3	1	CAP, 1 µF, Film Capacitor, 84AC, 450 VDC, Polypropylene (PP), Metallized, Radial, LS0.591" (15.00mm)	ECW-FD2W105K	Panasonic Electronic Components
4	C4 C6	2	1 µF, ±10%, 50 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	06035C105KAT2A	AVX Corporation
5	C5	1	470 pF 50 V, Ceramic, C0G/NP0, 0603	VJ0603A471JXAAC	Vishay Vitramon
6	C7	1	CAP, 0.1 µF ±10% 50 V Ceramic Capacitor X7R 0603 (1608 Metric)	CGA3E2X7R1H104K080AA	TDK Corporation
7	C8	1	1 µF 25 V, Ceramic, X5R, 0402 REPLACEMENT FOR 20-09142-00 a replacement for 20-00844-00	TMK105BJ105MV-F	Taiyo Yuden
8	C9	1	470 pF, ±10%, 50 V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B471KB8NFNC	Samsung
9	C10	1	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
10	C11 C12	2	33 µF, 450 V, Electrolytic, (10 x 37)	EKXL451ELL330MJ35S	Chemi-Con
11	C13 C20	2	220 pF, 250 V, Ceramic, COG, 0603	C1608C0G2E221J	TDK Corp
12	C14	1	22 µF, 25 V, Electrolytic, 20 %, Gen. Purpose, (5 x 7mm)	EEA-GA1E220	Panasonic
13	C15	1	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK Corp
14	C16	1	0.47 µF, ±10% ,50 V, Ceramic, X7R, 0805 (2012 Metric),-55 °C ~ 125 °C	CGA4J3X7R1H474K125AB	TDK Corp
15	C18 C30	2	2.2 µF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	CL21B225KAFNFNE	Samsung
16	C19	1	2200 pF, 500 VAC, Film, X1Y1	DE1E3RA222MA4BQ01F	Murata
17	C21	1	2200 pF, ±10%, 200 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	08052C222K4T2A	AVX Corp
18	C22	1	10 µF, ±10%, 25 V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	GRT21BC71E106KE13L	Murata Electronics
19	C23	1	0.022 µF, ±10%, 50 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	06035C223KAT2A	AVX Corp
20	C24	1	1000 pF, ±10%, 50 V, Ceramic Capacitor, X7R, 0603 (1608 Metric)	CL10B102KB8WPNC	Samsung Electro-Mechanic
21	C25 C26	2	680 µF,±20%, 35 V, Aluminum - Polymer Capacitors, Radial, Can, 18mOhm, 2000 Hrs @ 105°C (10 x 18)	A750MW687M1VAAE018	KEMET
22	C27	1	2.2 µF, ±10%, 50V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	CGA4J3X7R1H225K125AE	TDK
23	C29	1	47pF ±5% 630V Ceramic Capacitor U2J 1206 (3216 Metric)	GCM31A7U2J470JX01D	Murata Electronics
24	D1	1	530 V, 3 A, D PACKAGE (SO-8C)	LXA03D530	Power Integrations
25	D3	1	Diode, GP, 800 V ,2 A, Surface Mount SMBflat DO-221AA, SMB Flat Leads	STTH208µFY	STMicroelectronics
26	D4 D9	2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes Inc
27	D5 D10	2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
28	D6	1	Diode, GP, 1000 V, 1 A, Surface Mount DO-221AC (SMA-FL) (SlimSMA)	GS1MFL-TP	Micro Commercial Co
29	D8	1	Diode, Schottky, 200 V, 1A, Surface Mount SOD-123HE	SS10200HE_R1_00001	Panjit International Inc.
30	F1	1	3.15 A, 300 V, Slow, Long Time Lag, RST	36913150000	Littelfuse Inc
31	L1	1	CMC, 330 µH @ 100 KHz, ±10%, Toroidal, wound on 32-00330-00 toroidal core	32-00466-00	Power Integrations

32	L2	1	15 mH @ 10 kHz, 2 Line Common Mode Choke, Through Hole ,1.3 A, DCR 430 mOhm (Typ), 24.5 x 14.5 mm x 13.5 mm height	B82732F2132B001	Epcos
33	L3	1	68 µH, Unshielded Toroidal Inductor, 2A, 55 mOhm Max, Radial, Vertical (Open)	7447033	Wurth Elect Inc
34	Q1	1	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300 mW, SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semiconductor
35	Q2 Q3	2	MOSFET, N-Channel 150 V, 80 A (Ta), 157 W (Ta), Surface Mount 8-PDFN (5x6)	SRT15N110LD56TR-G	Shenzhen Sanrise Technology Co., LTD.
36	R1 R2	2	RES, 510 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J514V	Panasonic
37	R3	1	RES, 100 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
38	R4 R9	2	RES, 6.8 M, 5%, 1/4 W, Thick Film, 1206	RC1206JR-076M8L	YAGEO
39	R5 R6 R10 R11	4	RES, 4.7 M, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ475V	Panasonic
40	R7	1	RES, 154 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1543V	Panasonic
41	R8	1	RES, 30.1 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
42	R12	1	RES, 154 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1543V	Panasonic
43	R13 R26	2	RES, 22 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
44	R14	1	RES, 5.1 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ512V	Panasonic
45	R15	1	RES, 100 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
46	R16	1	RES, 500 k ±1% 0.3 W, Chip Resistor 1206 (3216 Metric) Thick Film	CRMA1206AF500KFKEF	Vishay / Techno
47	R17 R19	2	RES, 15 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ150V	Panasonic
48	R20	1	RES, 1.6 M, 5%, 1/4 W, Thick Film, 1206	RC1206JR-071M6L	YAGEO
49	R21 R22	2	RES, 1.2 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1204V	Panasonic
50	R23	1	RES, 300 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ301V	Panasonic
51	R24 R25 R33	3	RES, 15 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J150V	Panasonic
52	R27	1	RES, 4.7 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
53	R28	1	RES, 1.2 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ122V	Panasonic
54	R29	1	RES, 100 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603FR-07100KL	Yageo
55	R30	1	RES, 5.49 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5491V	Panasonic
56	R31 R32	2	RES, 0.01 R, 1%, 1/4 W, Metal Foil, Current Sense, Moisture Resistant,1206 (3216 Metric), ±100ppm/°C, -55°C ~ 155 °C	PF1206FRF070R01L	Yageo
57	RV1	1	320 VAC, 48 J, 10 mm, RADIAL	V320LA10P	Littlefuse
58	T1	1	Bobbin, ATQ23.2/11.6, Horizontal, 4 pins. (Mates with core 99-00090-00)	TBI-238-10501.11x6	TBI -Transformer Bobbin Industrial Co
59	T2	1	Bobbin, Vertical, EDR4110, 9 pins, 6pri, 3 sec	FP9-EDR41/11	Changshu Xinli Magnetic Industrial CO LTD
60	U1	1	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
61	U2	1	HiperPFS-4, InSOP24B	PFS7624C	Power Integrations
62	U3	1	InnoSwitch4-QR, INN4276C-H182, 230 VDC,125 W, insop-24D	INN4276C-H182	Power Integrations
63	VR1	1	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP Semiconductors
64	VR2	1	DIODE ZENER 30V 150MW EMD2	EDZVT2R30B	Rohm Semiconductor
65	VR3	1	TVS Diode, TRANSZORB®, 162V Clamp 3.7A Ipp Tvs Diode Surface Mount DO-221AC (SlimSMA)	SMA6F100A-M3/H	Vishay General Semiconductor - Diodes Division

Table 2 – Bill of Materials, Electrical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	TAB1	1	0.250" (6.35mm) Quick Connect Male - Solder Connector Non-Insulated	1287-ST	KeyStone Electronics
2	J1	1	CONN TERM BLOCK, 2 POS, 5 mm, PCB	ED500/2DS	On Shore Technology Inc
3	J2	1	2 Position Wire to Board Terminal Block Horizontal with Board 0.300" (7.62mm) Through Hole	1707027	Phoenix Contact

Table 3 – Bill of Materials, Miscellaneous Parts

7 Boost Inductor Design Spreadsheet

1	Hiper_PFS-4_Boost_031722; Rev.1.4; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	Continuous Mode Boost Converter Design Spreadsheet
2	Enter Application Variables					Design Title
3	Input Voltage Range	High Line	Warning	High Line		Select the appropriate device based on the input voltage range (C-Package parts are not available for high-line only designs)
4	VACMIN	198		198	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other voltages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	305		305	VAC	Maximum AC input voltage
6	VBROWNIN		Info	173	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
7	VBROWNOUT		Info	162	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
8	VO	400	Warning	400	VDC	Output Voltage could be exceeded at VACMAX
9	PO	108		108	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.96		0.96		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP		Warning	20	ms	Expected holdup time is smaller than specified value. Please use larger Output capacitance
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	KP_TARGET	0.78		0.78		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
22	LPFC_TARGET (0 bias)			906	µH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
23	LPFC_DESIRED (0 bias)	900		900	µH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
24	KP_ACTUAL			0.785		Actual KP calculated from LPFC_DESIRED
25	LPFC_PEAK			900	µH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
27	**Basic current parameters**					

28	IAC_RMS			0.57	A	AC input RMS current at VACMIN and Full Power load
29	IO_DC			0.27	A	Output average current/Average diode current
32	**PFS Parameters**					
33	PFS Package	C	Warning	C		C Package Does Not Support High-Line Only Designs
34	PFS Part Number	PFS7624C	Warning	PFS7624C		Peak power rating for the device has been exceeded. Output might drop. Change the input voltage range or select a larger device.
35	Operating Mode	Full Power		Full Power		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
36	IOCP min			3.00	A	Minimum Current limit
37	IOCP typ			3.30	A	Typical current limit
38	IOCP max			3.50	A	Maximum current limit
39	IP			1.32	A	MOSFET peak current
40	IRMS			0.42	A	PFS MOSFET RMS current
41	RDSON			0.74	Ohms	Typical RDSon at 100 'C
42	FS_PK			109.2	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
43	FS_AVG			97.6	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
44	PCOND_LOSS_PFS			0.129	W	Estimated PFS Switch conduction losses
45	PSW_LOSS_PFS			1.431	W	Estimated PFS Switch switching losses
46	PFS_TOTAL			1.561	W	Total Estimated PFS Switch losses
47	TJ Max			100	deg C	Maximum steady-state junction temperature
48	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
49	HEATSINK Theta-CA			35.65	°C/W	Maximum thermal resistance of heatsink
52	**INDUCTOR DESIGN**					
53	**Basic Inductor Parameters**					
54	LPFC (0 Bias)			900	µH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
55	LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
56	IL_RMS			0.64	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	ATQ		ATQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	ATQ23.7/14.6		ATQ23.7/14.6		Core part number
62	Ae	89.00		89.00	mm^2	Core cross sectional area
63	Le			38.20	mm	Core mean path length
64	AL			7200.00	nH/t^2	Core AL value
65	Ve			3.94	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			3.35	mm	Core height/Height of window; ID if toroid

67	MLT			49.6	mm	Mean length per turn
68	BW			6.60	mm	Bobbin width
69	LG			1.08	mm	Gap length (Ferrite cores only)
70	**Flux and MMF calculations**					
71	BP_TARGET (ferrite only)	3800		3800	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_OCP (or BP)			3792	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			1360	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance, minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCP typ divided by µ at zero current
77	I_TEST			3.3	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP typ is used.
78	B_TEST			3575	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCP typ
80	**Wire**					
81	TURNS			98		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			0.64	A	Inductor RMS current
83	Wire type	Magnet		Magnet		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	30		30	AWG	Inductor wire gauge
85	Filar	2		2		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.254	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.50	mm	Will be different than OD if Litz
88	DCR			1.070	ohm	Choke DC Resistance
89	P AC Resistance Ratio			1.04		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J		Warning	6.28	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
92	Layers			9.23		Estimated layers in winding
93	**Loss calculations**					
94	BAC-p-p			1067	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
95	LPFC_CORE_LOSS			0.051	W	Estimated Inductor core Loss
96	LPFC_COPPER_LOSS			0.727	W	Estimated Inductor copper losses
97	LPFC_TOTAL_LOSS			0.779	W	Total estimated Inductor Losses
100	**PFC Diode**					
101	PFC Diode Part Number	LXA03D530		LXA03D530		PFS Diode Part Number
102	Type / Part Number			Qspeed		PFC Diode Type / Part Number
103	Manufacturer			PI		Diode Manufacturer

104	VRRM			530.0	V	Diode rated reverse voltage
105	IF			3.00	A	Diode rated forward current
106	Qrr			75.0	nC	Qrr at High Temperature
107	VF			1.33	V	Diode rated forward voltage drop
108	PCOND_DIODE			0.377	W	Estimated Diode conduction losses
109	PSW_DIODE			0.219	W	Estimated Diode switching losses
110	P_DIODE			0.596	W	Total estimated Diode losses
111	TJ Max			100.0	°C	Maximum steady-state operating temperature
112	Rth-JS		Info	27.00	°C/W	Rth too high. Will result in high diode loss
113	HEATSINK Theta-CA			73.16	°C /W	Maximum thermal resistance of heatsink
114	IFSM			25.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
117	**Output Capacitor**					
118	COUT	68		68	µF	Minimum value of Output capacitance
119	VO_RIPPLE_EXPECTED			13.2	V	Expected ripple voltage on Output with selected Output capacitor
120	T_HOLDUP_EXPECTED			18.1	ms	Expected holdup time with selected Output capacitor
121	ESR_LF			2.02	ohms	Low Frequency Capacitor ESR
122	ESR_HF			0.81	ohms	High Frequency Capacitor ESR
123	IC_RMS_LF			0.19	A	Low Frequency Capacitor RMS current
124	IC_RMS_HF			0.33	A	High Frequency Capacitor RMS current
125	CO_LF_LOSS			0.076	W	Estimated Low Frequency ESR loss in Output capacitor
126	CO_HF_LOSS			0.091	W	Estimated High frequency ESR loss in Output capacitor
127	Total CO LOSS			0.167	W	Total estimated losses in Output Capacitor
130	**Input Bridge (BR1) and Fuse (F1)**					
131	I^2t Rating			6.33	A^2*s	Minimum I^2t rating for fuse
132	Fuse Current rating			0.85	A	Minimum Current rating of fuse
133	VF			0.90	V	Input bridge Diode forward Diode drop
134	IAVG			0.53	A	Input average current at VBROWNOUT.
135	PIV_INPUT BRIDGE			431	V	Peak inverse voltage of input bridge
136	PCOND_LOSS_BRIDGE			0.921	W	Estimated Bridge Diode conduction loss
137	CIN			0.22	µF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
138	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
139	CIN_PLOSS			0.006	W	Input Capacitor Loss
140	RT1			10.78	ohms	Input Thermistor value
141	D_Precharge			1N5407		Recommended precharge Diode
144	**PFS4 small signal components**					
145	C_REF			1.0	µF	REF pin capacitor value
146	RV1			4.0	MOhms	Line sense resistor 1
147	RV2			6.0	MOhms	Line sense resistor 2
148	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
149	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4

150	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
151	C_VCC			1.0	µF	Supply decoupling capacitor
152	C_C			100	nF	Feedback C pin decoupling capacitor
153	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
154	PGT set resistor			320.5	kohm	Power good threshold setting resistor
157	**Feedback Components**					
158	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
159	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
160	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
161	RFB_4			155.5	kohms	Feedback network, lower divider resistor
162	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
163	RFB_5			26.1	kohms	Feedback network: zero setting resistor
164	CFB_2			1000	nF	Feedback component- noise suppression capacitor
167	**Loss Budget (Estimated at VACMIN)**					
168	PFS Losses			1.561	W	Total estimated losses in PFS
169	Boost diode Losses			0.596	W	Total estimated losses in Output Diode
170	Input Bridge losses			0.921	W	Total estimated losses in input bridge module
171	Input Capacitor Losses			0.006	W	Total estimated losses in input capacitor
172	Inductor losses			0.779	W	Total estimated losses in PFC Choke
173	Output Capacitor Loss			0.167	W	Total estimated losses in Output capacitor
174	EMI choke copper loss			0.032	W	Total estimated losses in EMI choke copper
175	Total losses			4.061	W	Overall loss estimate
176	Efficiency			0.96		Estimated efficiency at VACMIN, full load
179	**CAPZero component selection recommendation**					
180	CAPZero Device			CAP200DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
181	Total Series Resistance (Rcapzero1+Rcapzero2)			1.046	MOhms	Maximum Total Series resistor value to discharge X-Capacitors
184	**EMI filter components recommendation**					
185	CX2			330	nF	X capacitor after differential mode choke and before bridge, ratio with Po
186	LDM_calc			461	µH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
187	CX1			330	nF	X capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	typical common mode choke value
189	LCM_leakage			30	µH	estimated leakage inductance of CM choke, typical from 30~60µH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			431	µH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.

192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
193	DCR_LDM			0.030	Ohms	Total DCR of DM choke (or CM #2) for estimating copper loss

Table 4 – Boost Inductor Design Spreadsheet

8 Flyback Transformer Design Spreadsheet

1	**ACDC_InnoSwitch4-QR_Flyback_050624; Rev.1.0; Copyright Power Integrations 2024**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet**
2	APPLICATION VARIABLES					Design Title
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	390		390	V	Minimum DC input voltage
5	VIN_MAX	410		410	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Range of AC input voltage
7	LINEFREQ				Hz	AC Input voltage frequency
8	CAP_INPUT				µF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	CDC			0	mV	Cable drop compensation desired at full load
11	IOUT	4.167		4.167	A	Output current
12	POUT			100.01	W	Output power
13	EFFICIENCY	0.92		0.92		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	INN4276		INN4276		Generic device code
22	DEVICE_CODE			INN4276C		Actual device code
23	POUT_MAX			105	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.37	Ω	Primary switch on time drain resistance at 100 °C
25	ILIMIT_MIN			2.697	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			2.900	A	Typical current limit of the primary switch
27	ILIMIT_MAX			3.103	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.10	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			580.0	V	Peak drain voltage on the primary switch during turn-off. A 30V leakage spike voltage is assumed
34	**WORST CASE ELECTRICAL PARAMETERS**					

35	FSWITCHING_MAX	72000		72000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
36	VOR	140.0		140.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			390.00	V	Valley of the minimum input AC voltage at full load
38	KP			1.35		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			DCM		Mode of operation
40	DUTYCYCLE			0.210		Primary switch duty cycle
41	TIME_ON			3.50	µs	Primary switch on-time
42	TIME_OFF			11.00	µs	Primary switch off-time
43	LPRIMARY_MIN			433.2	µH	Minimum primary inductance
44	LPRIMARY_TYP			456.0	µH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			478.8	µH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			2.890	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.270	A	Primary switch average current
52	IRIPPLE_PRIMARY			2.890	A	Primary switch ripple current
53	IRMS_PRIMARY			0.721	A	Primary switch RMS current
54						
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			17.342	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
58	IRMS_SECONDARY			7.221	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	CORE SELECTION					
64	CORE	Custom		Custom		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE	EDR4110		EDR4110		Core code
66	AE	170.00		170.00	mm^2	Core cross sectional area
67	LE	28.42		28.42	mm	Core magnetic path length
68	AL	8850		8850	nH/turns^2	Ungapped core effective inductance
69	VE	4832.0		4832.0	mm^3	Core volume
70	BOBBIN	EDR4110		EDR4110		Bobbin name
71	AW	31.80		31.80	mm^2	Window area of the bobbin
72	BW	3.80		3.80	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			24		Primary turns
77	BPEAK			3798	Gauss	Peak flux density
78	BMAX			3347	Gauss	Maximum flux density
79	BAC			1673	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			792	nH/turns^2	Typical gapped core effective inductance

81	LG			0.246	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			3		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY	4		4		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			1		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	LINE UNDERVOLTAGE					
96	BROWN-IN REQURED			234.00	V	Required AC RMS/DC line voltage brown-in threshold
97	RLS			8.64	MΩ	Connect two 4.32 MOhm resistors to the V-pin for the required UV/OV threshold
98	BROWN-IN ACTUAL			198.2V - 240.6V	V	Actual AC RMS/DC brown-in range
99	BROWN-OUT ACTUAL			176V - 218.8V	V	Actual AC RMS/DC brown-out range
101	LINE OVERVOLTAGE					
102	OVERVOLTAGE_LINE		Warning	907.3V - 1030.4V	V	The device voltage stress will be higher than 750V when overvoltage is triggered
104	PRIMARY BIAS DIODE					
105	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
106	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
107	VREVERSE_BIASDIODE_PRIMARY			69.25	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
108	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
109	CBPP			0.47	µF	BPP pin capacitor
113	**SECONDARY COMPONENTS**					
114	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
115	RFB_LOWER			5.62	kΩ	Lower feedback resistor
116	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
118	SECONDARY BIAS DIODE					
119	USE_SECONDARY_BIAS	AUTO		YES		Use secondary bias winding for the design
120	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
121	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
122	VREVERSE_BIASDIODE_SECONDARY			22.08	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
123	CBIAS_SECONDARY			10	µF	Bias winding rectification capacitor
124	CBPS			2.20	µF	BPP pin capacitor
127	**MULTIPLE OUTPUT PARAMETERS**					
128	OUTPUT 1					
129	VOUT1			24.00	V	Output 1 voltage
130	IOUT1			4.17	A	Output 1 current
131	POUT1			100.01	W	Output 1 power
132	IRMS_SECONDARY1			7.221	A	Root mean squared value of the secondary current for output 1
133	IRIPPLE_CAP_OUTPUT1			5.897	A	Current ripple on the secondary waveform for output 1

134	NSECONDARY1			4		Number of turns for output 1
135	VREVERSE_RECTIFIER1			92.33	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
136	SRFET1	Auto		AONS62922		Secondary rectifier (Logic MOSFET) for output 1
137	VF_SRFET1			0.029	V	SRFET on-time drain voltage for output 1
138	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
139	RDSON_SRFET1			7.0	mΩ	SRFET on-time drain resistance at 25 °C and VGS = 4.4 V for output 1

Table 5 – Flyback Transformer Design Spreadsheet

9 Flyback Transformer Specification

9.1 Electrical Diagram

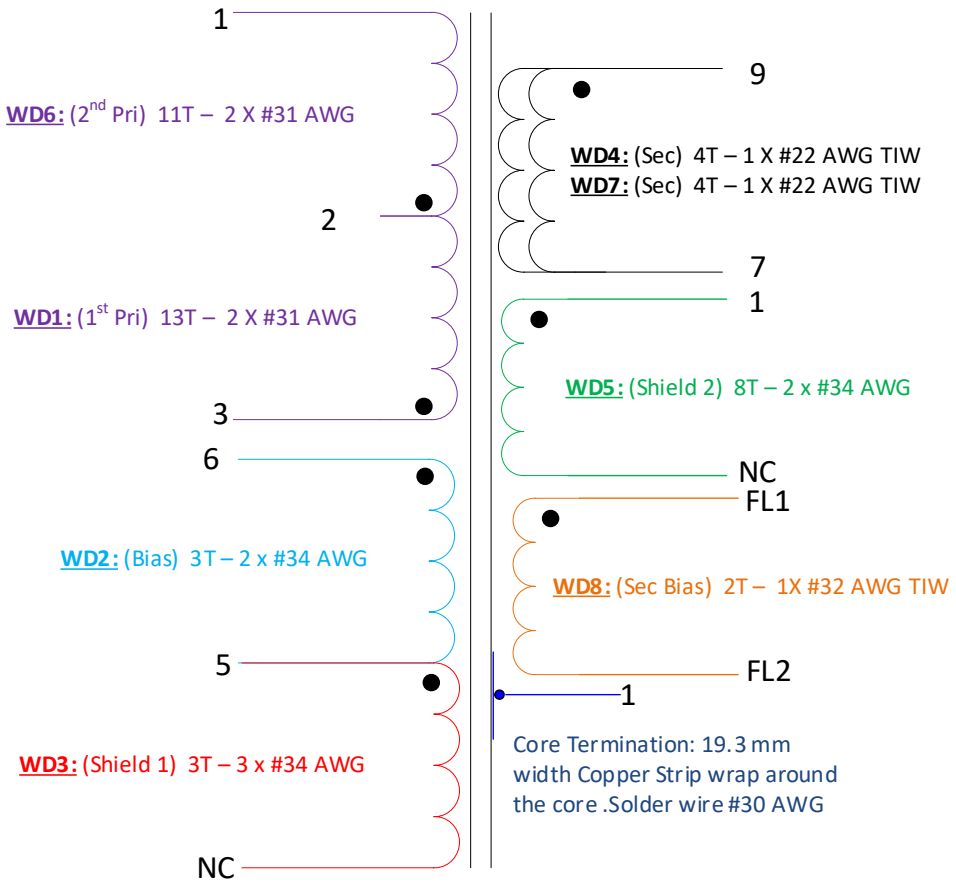


Figure 7 – Transformer Schematic

9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 3, with all other windings open.	**456 µH ± 5%**
Resonant Frequency	Between pin 1 and 3, other windings open	100 KHz (min)
Primary Leakage Inductance	Measure inductance across Pin 1-3 with Pin 9 and Pin 7 shorted	10 µH +/- 5%

Table 6 – Flyback Transformer Electrical Specifications

9.3 Materials

Item	Description
[1]	Core: EDR4110
[2]	Bobbin: Vertical, EDR4110, 9 pins, 6pri, 3sec, PI#: 25-01139-00
[3]	Magnet wire: #31 AWG, double coated.
[4]	Magnet wire: #34 AWG, double coated.
[5]	TIW: #22 AWG
[6]	TIW: 32# AWG
[7]	Tape: 3M 13450-F, Polyester Film
[8]	3 M Copper Tape (19.3 mm)
[9]	Varnish: Dolph BC-359.
[10]	Aremco-Bond 526N-B base resin
[11]	Aremco-Bond 526N-A activator resin

Table 7 – Flyback Transformer Materials

9.4 Transformer Build Diagrams

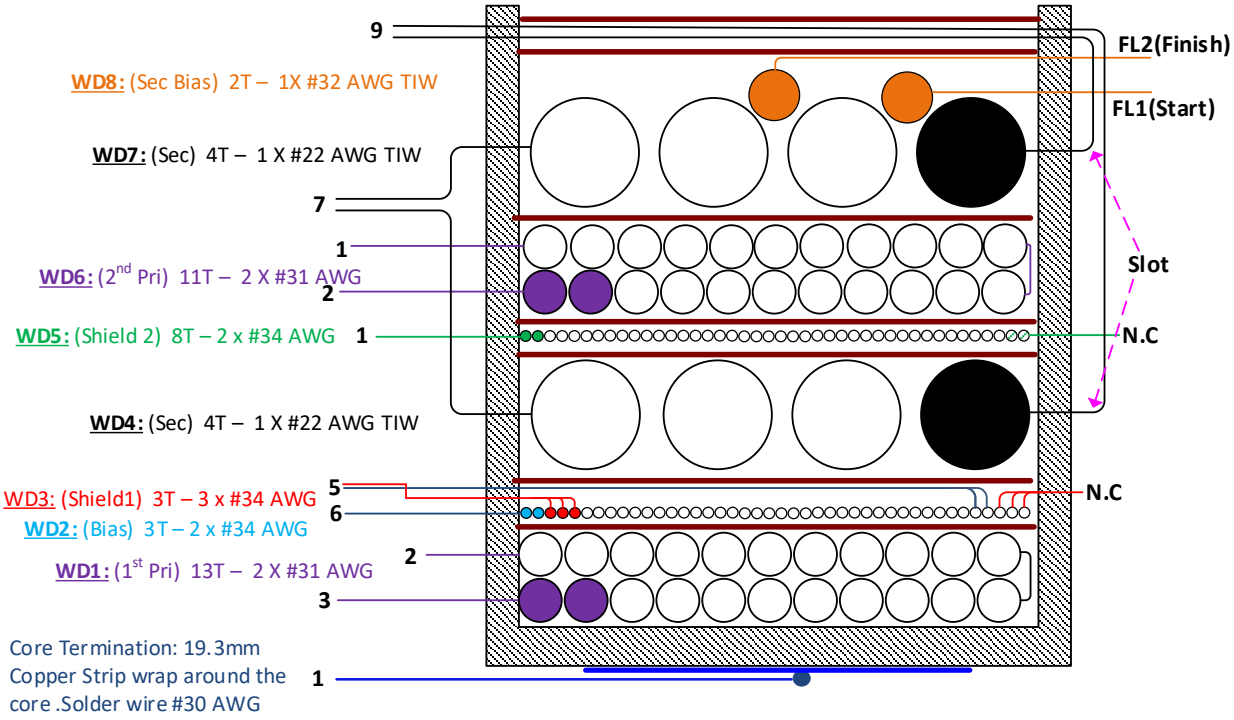
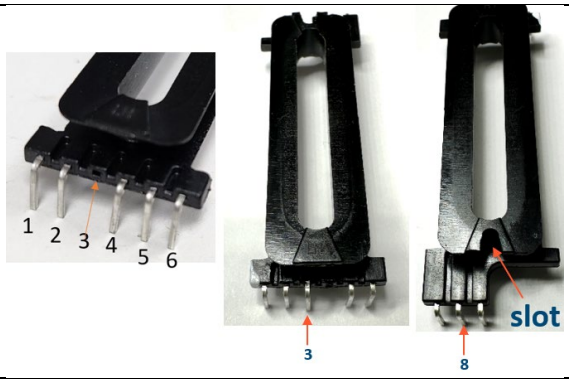
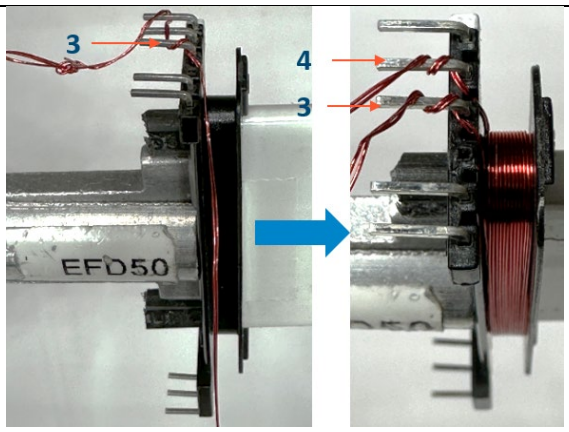
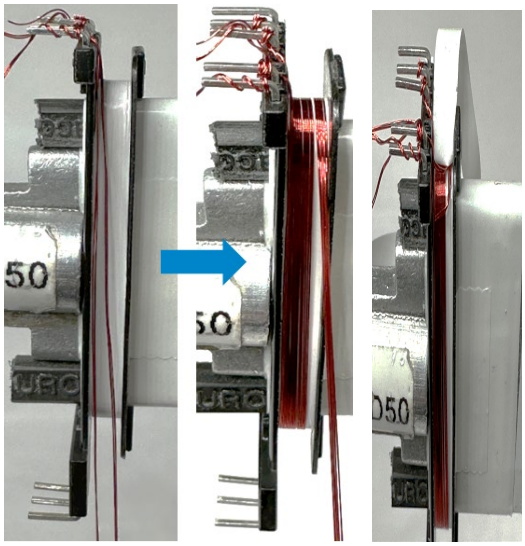
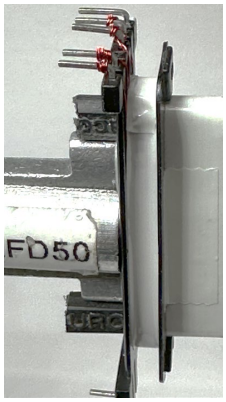
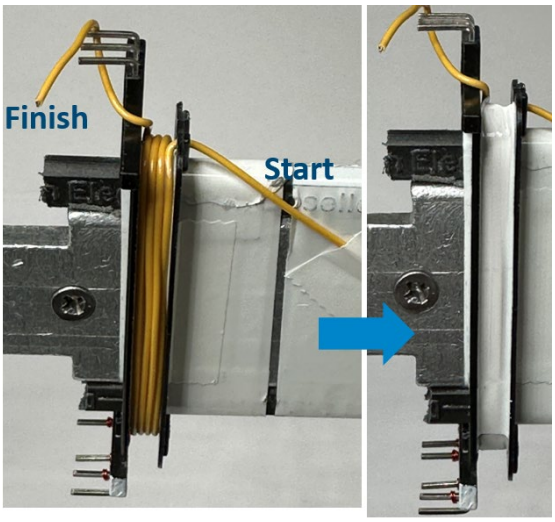


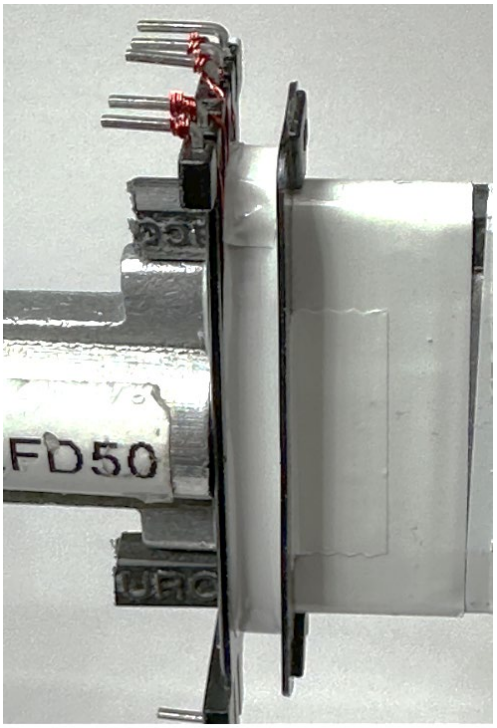
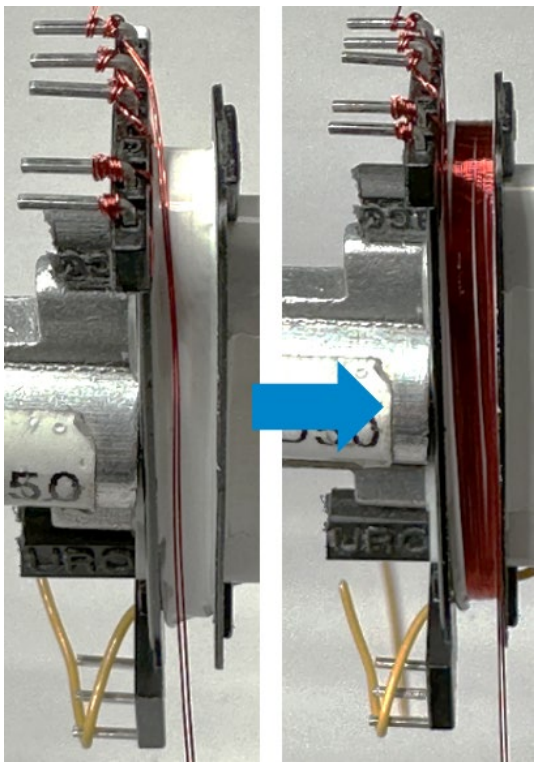
Figure 8 – Transformer Build Diagram

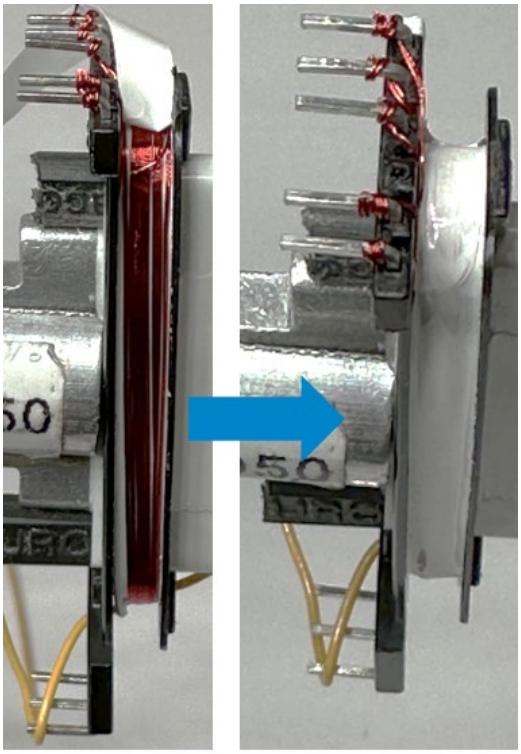
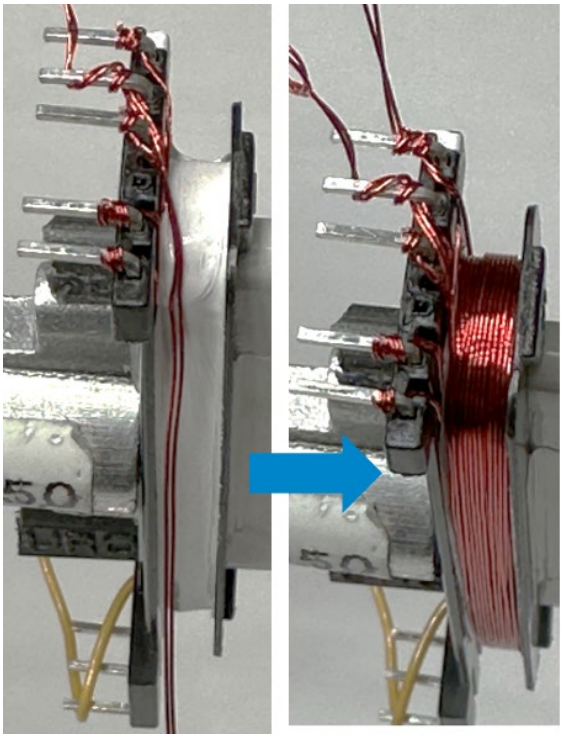
9.5 Winding Illustrations

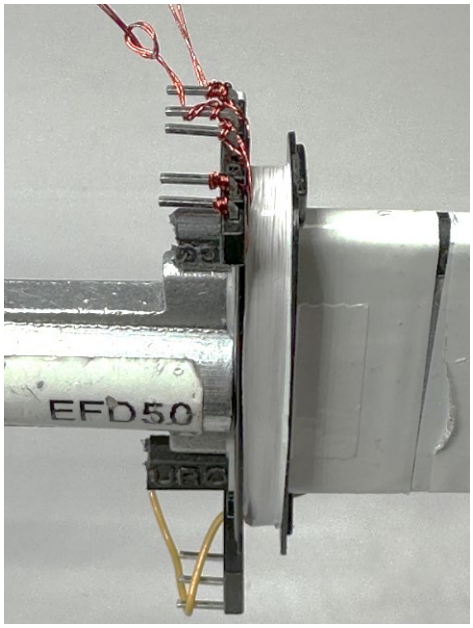
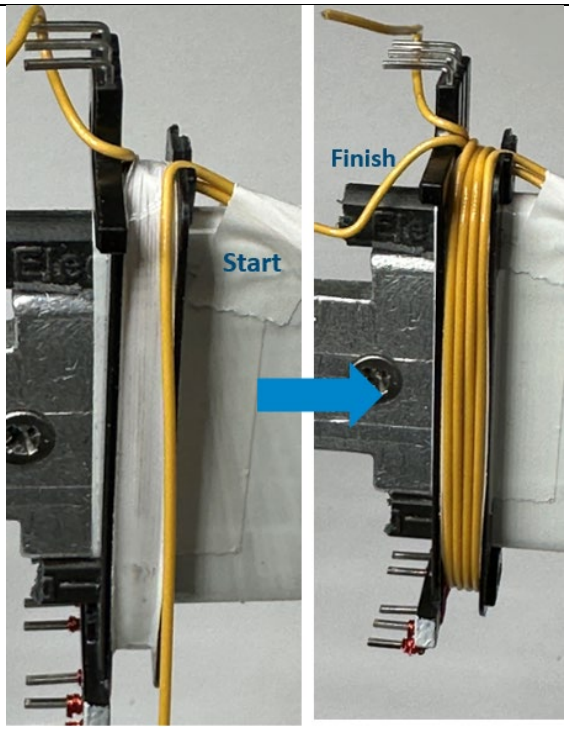
Bobbin Preparation		1. Remove terminal pin no.4 and insert it into pin 3. 2. Drill a slot for secondary wire. 3. Remove terminal pin 8.

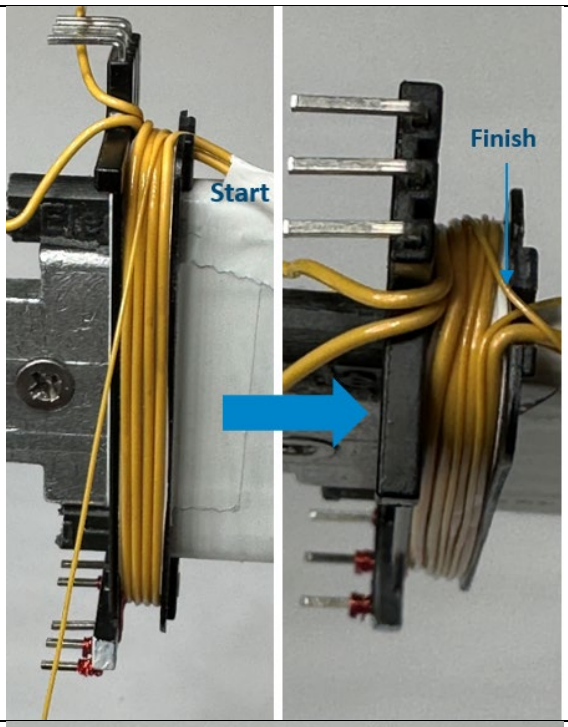
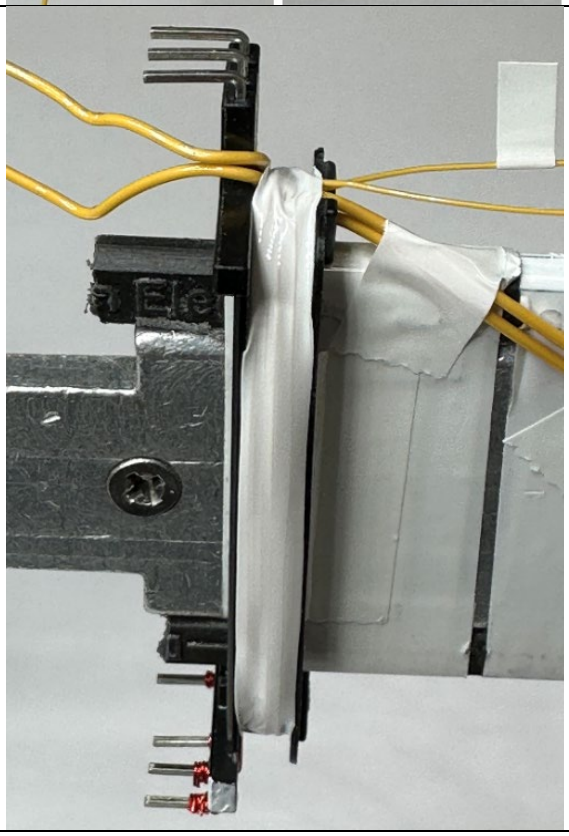
WD1 **1st Primary**		Start at pin 3 and wind 13 bifilar turns of wire item [3] in 2 layers with tight tension, from left to right and then from right to left. Finish the winding at pin 2.
Insulation		1 layer of tape item [7].

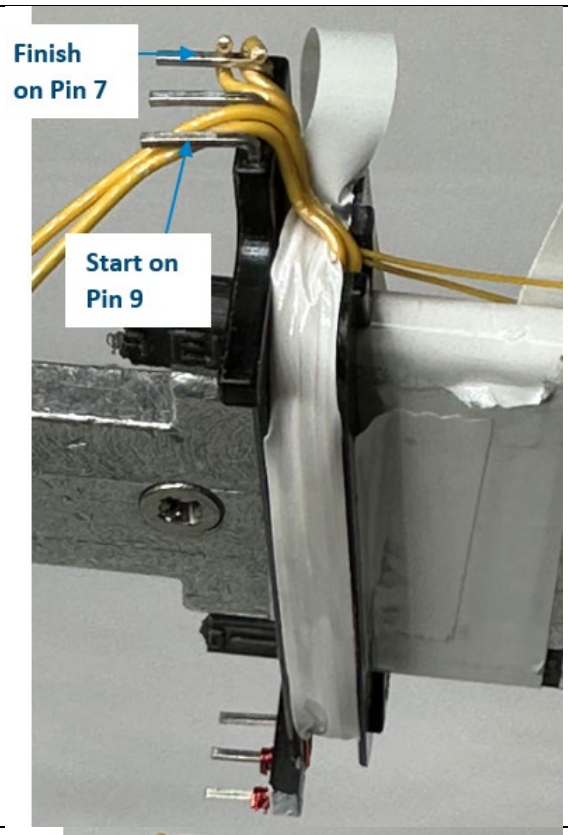
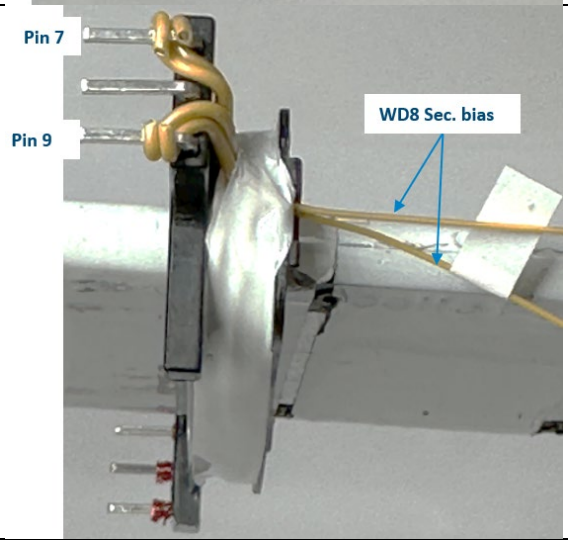
WD2: Bias & WD3: Shield1		Use 2 wires item [4] start at pin 6 for Bias winding, also use 3 wires same item [4] start at pin 5 for Shield1 winding. Wind all 5 wires in parallel, at the 3rd turn: - bring 2 wires for Bias winding to the left and terminate at pin 5, - For Shield1 winding, cut short 3 wires as no connect.
Insulation		1 layer of tape item [7].
WD4 Secondary 1		Use wire item [5]. Start at the right slot of the secondary side, leaving approximately 20mm floating. Wind 4 turns in 1 layer from right to left and terminate at Pin 7.

Insulation		1 layer of tape item [7].
WD5 **Shield2**		Start at pin 1, wind 8 bifilar turns of wire item [4], from left to right. At the last turn, cut short to leave as No-Connect.

Insulation		1 layer of tape item [7].
WD6 **2nd Primary**		Start at pin 2 and wind 11 bifilar turns of wire item [3] in 2 layers with tight tension, from left to right and then from right to left. Finish the winding at pin 1.

Insulation		1 layer of tape item [7].
WD7 **Secondary 2**		Use wire item [5]. Start at the right slot of the secondary side, leaving approximately 20mm floating. Wind 4 turns in 1 layer from right to left and terminate at Pin 7.

WD8 **Secondary Bias**		Use wire item [6]. Start at the right slot of the secondary side, leaving approximately 40mm floating, and mark it as FL1. Wind 2 turns from right to left, then bring the wire back to the right slot, leaving approximately 40mm floating, and mark it as FL2.
Insulation		1 layer of tape item [7].

Secondary Wire Terminals		Terminate the 2 secondary floating wires (Start) to pin 9
Insulation		Fixed the secondary wires using 1 layer polyester tape item 8

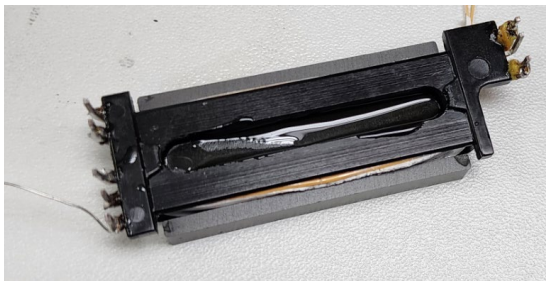
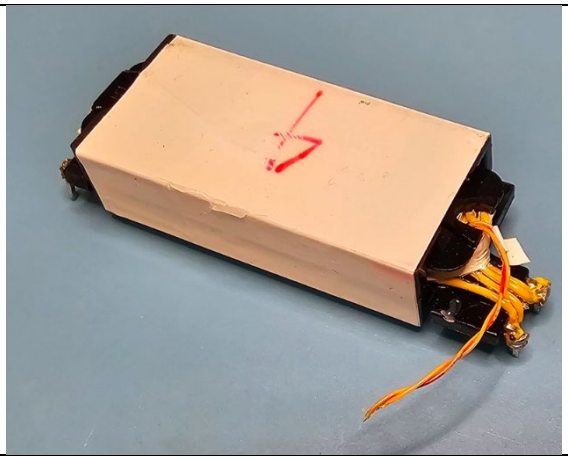
Core Gap		Gap the core halves evenly to achieve 456 µH of primary inductance, measured across pin 1 and pin 3.
Adhesive application to the center leg of the core **Note:** Adhesive is applied to the center leg of the core to mitigate audible noise caused by magnetostriction during PWM dimming.	 	Combine Aremco-Bond 526N-B base and activator resin in a 1:1 ratio. Apply the adhesive mixture to the core center leg as shown in the figure. Wrap around transformer 1 layer of 19.3 mm width 3M copper tape Item [8], solder at joint to make a closed loop, and Then solder it to terminal pin 1 via AWG#30 magnet wire. Secure the 2 cores with polyester tape item [7]. Cure the adhesive at 100°C in an oven for 1 hour.
Finish		Varnish the transformer with item [9], then cure the varnish in an oven at 100°C for 1 hour.

Table 8 – Flyback Transformer Winding Illustrations

10 Boost Inductor Specification

10.1 Electrical Diagram

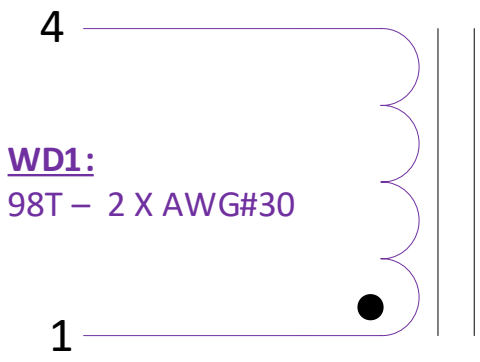


Figure 9 – Electrical Diagram

10.2 Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 4	900 µH± 5%

Table 9 – Boost Inductor Transformer Electrical Specifications

10.3 Materials

Item	Description
[1]	Core: ATQ23-11, P/N: 25-01183-00
[2]	Bobbin: ATQ23-11, P/N:25-01183-00
[3]	Magnet wire: #30 AWG, double coated.
[4]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 3.25 mm width.
[5]	Varnish: Dolph BC-359.

Table 10 – Boost Inductor Transformer Materials

10.4 Winding Diagram

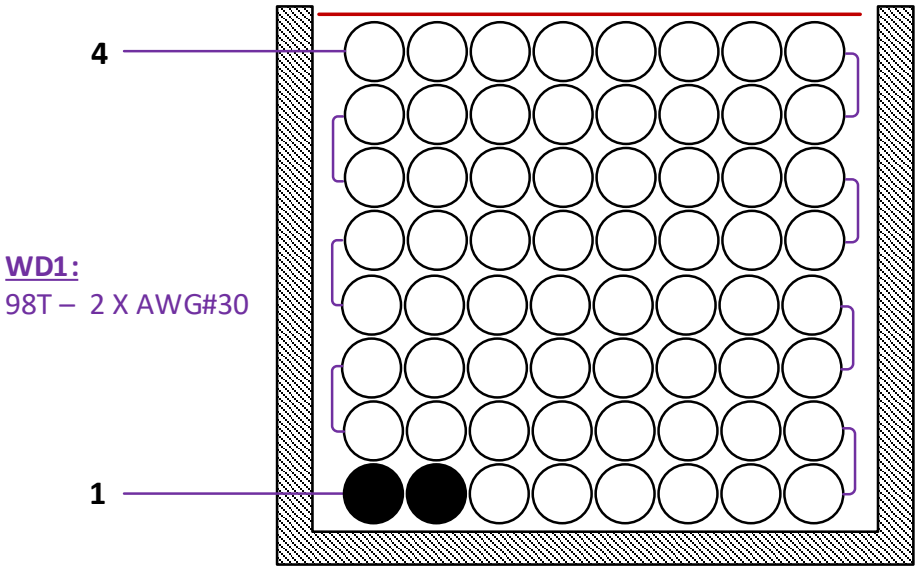


Figure 10 – Transformer Build Diagram

11 Performance Data

Performance data were measured at room temperature, with voltages taken on the input and output terminals of the PCB unless noted otherwise.

Note: Extremely low line voltage (140-180 VAC) testing was included to demonstrate low voltage thermal withstand capability for up to 5 minutes of operation.

11.1 Efficiency

11.1.1 Full Load Efficiency vs Input Voltage

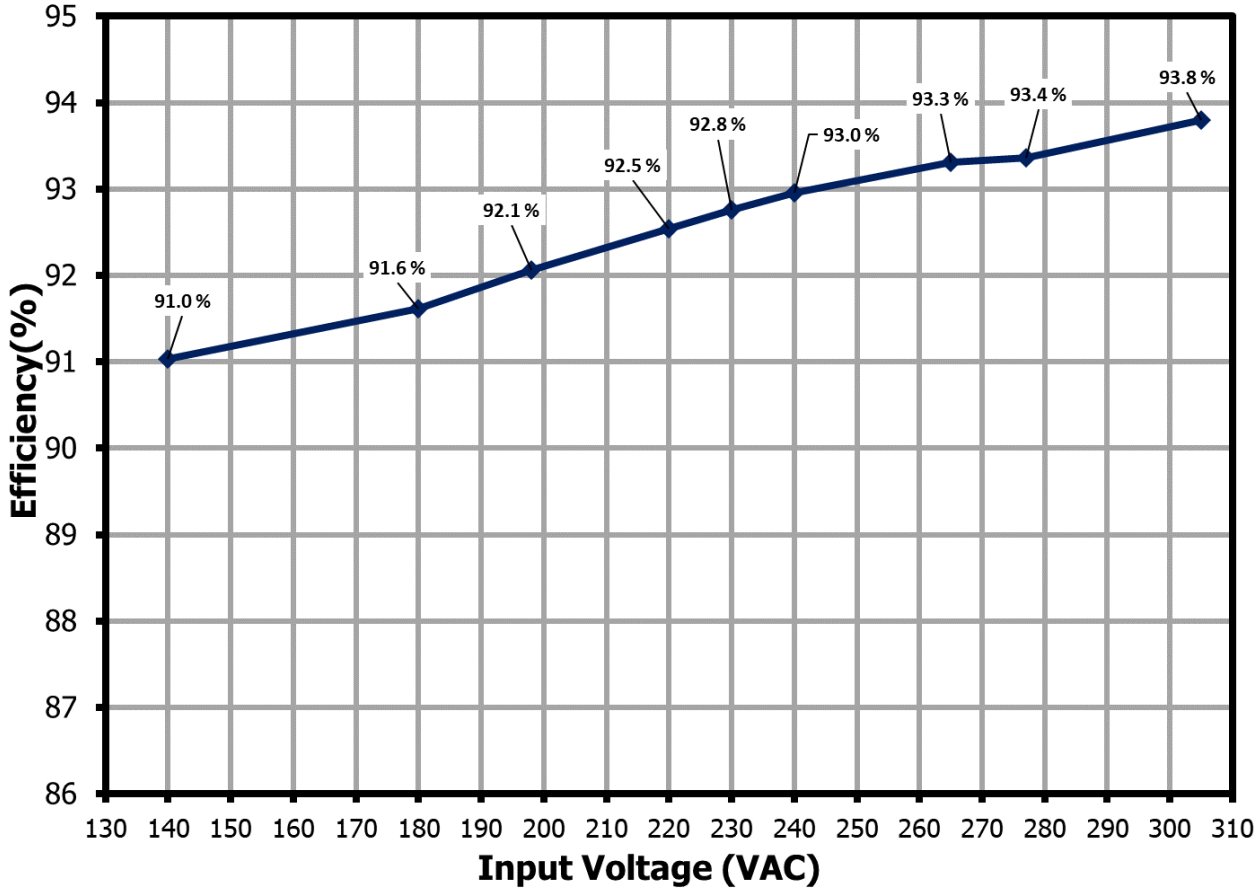


Figure 11 – Full Load Efficiency vs. Input Line Voltage

11.1.2 Efficiency vs Output Load

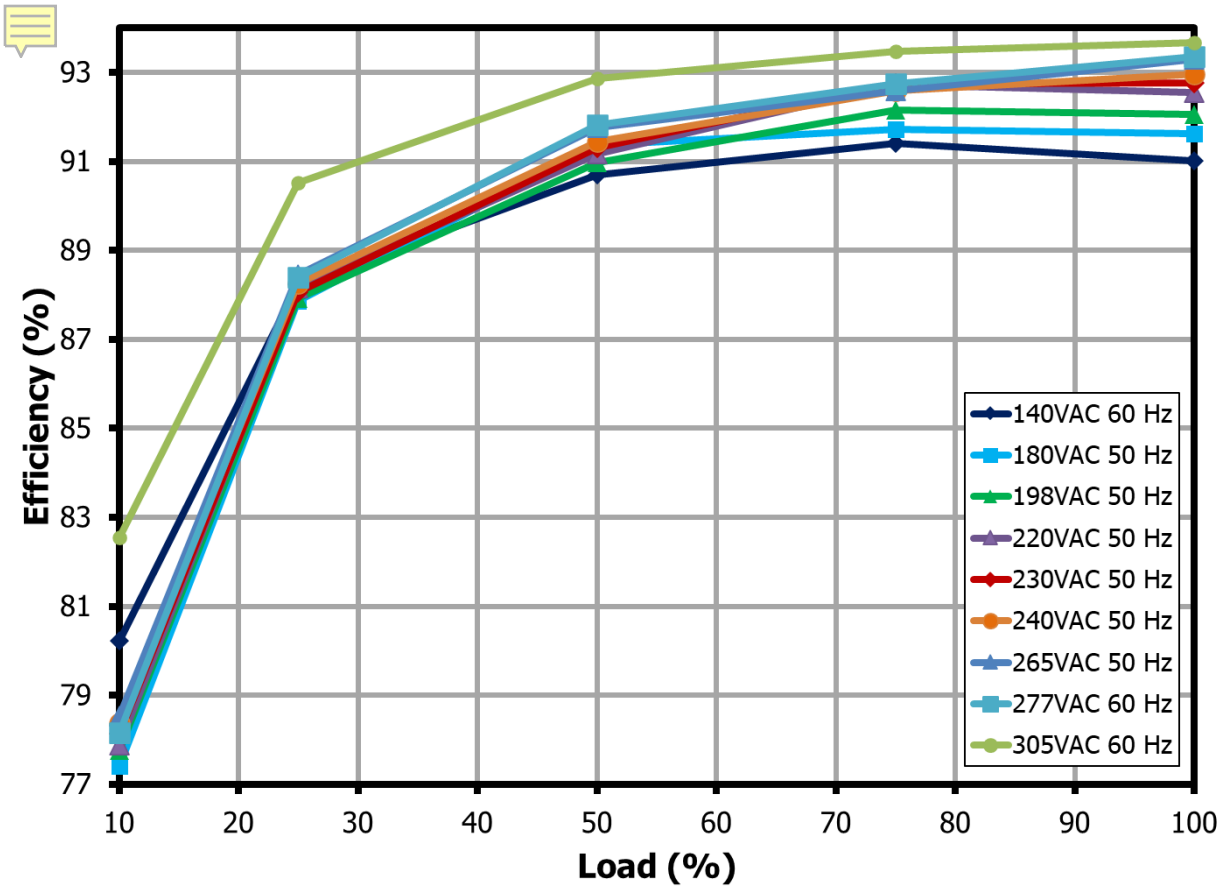


Figure 12 – Efficiency vs Load

11.2 Power Factor

11.2.1 Power Factor vs Input Line Voltage at Full Load

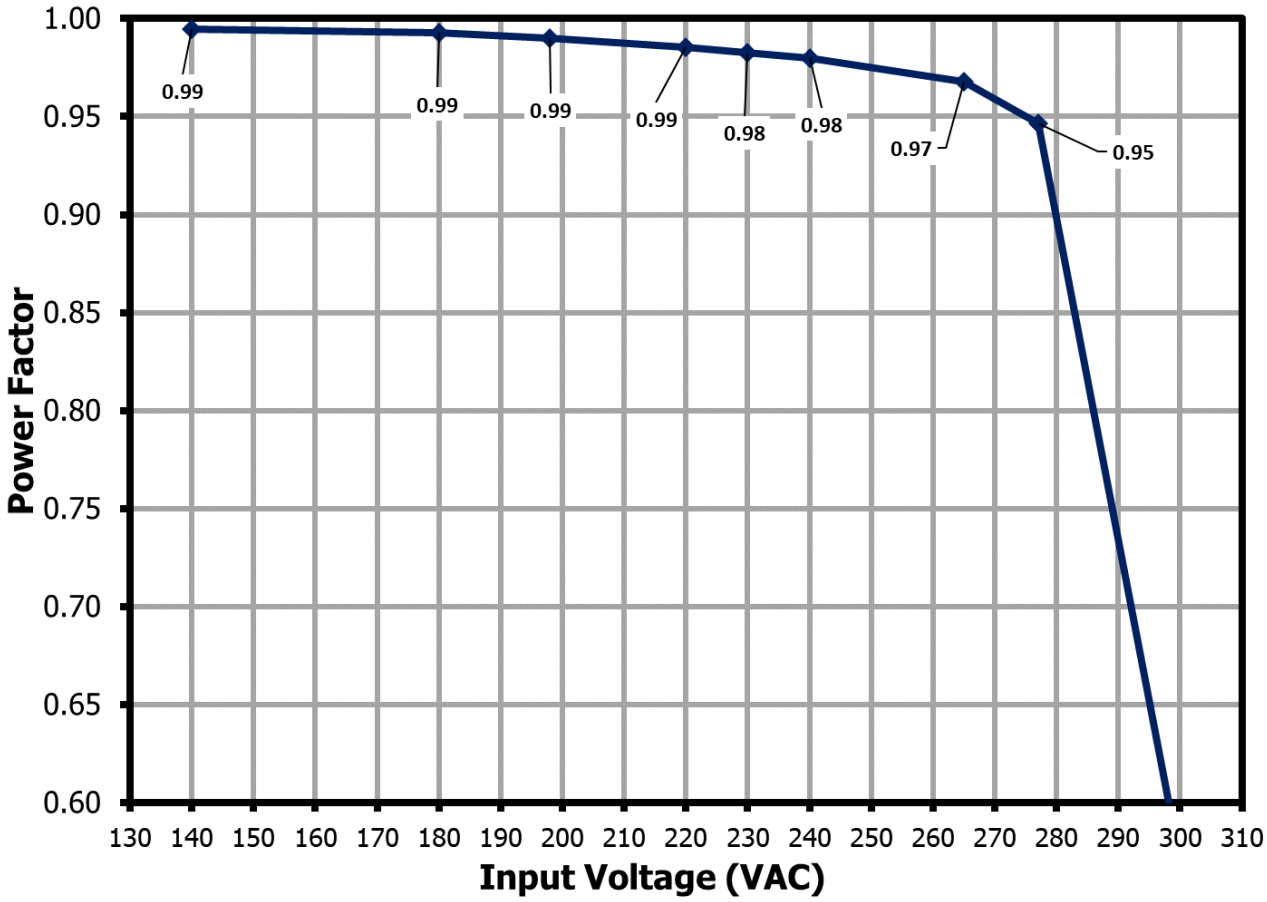


Figure 13 – Power Factor vs Input Line, 24 V Full Load

11.2.2 Power Factor vs Output Load

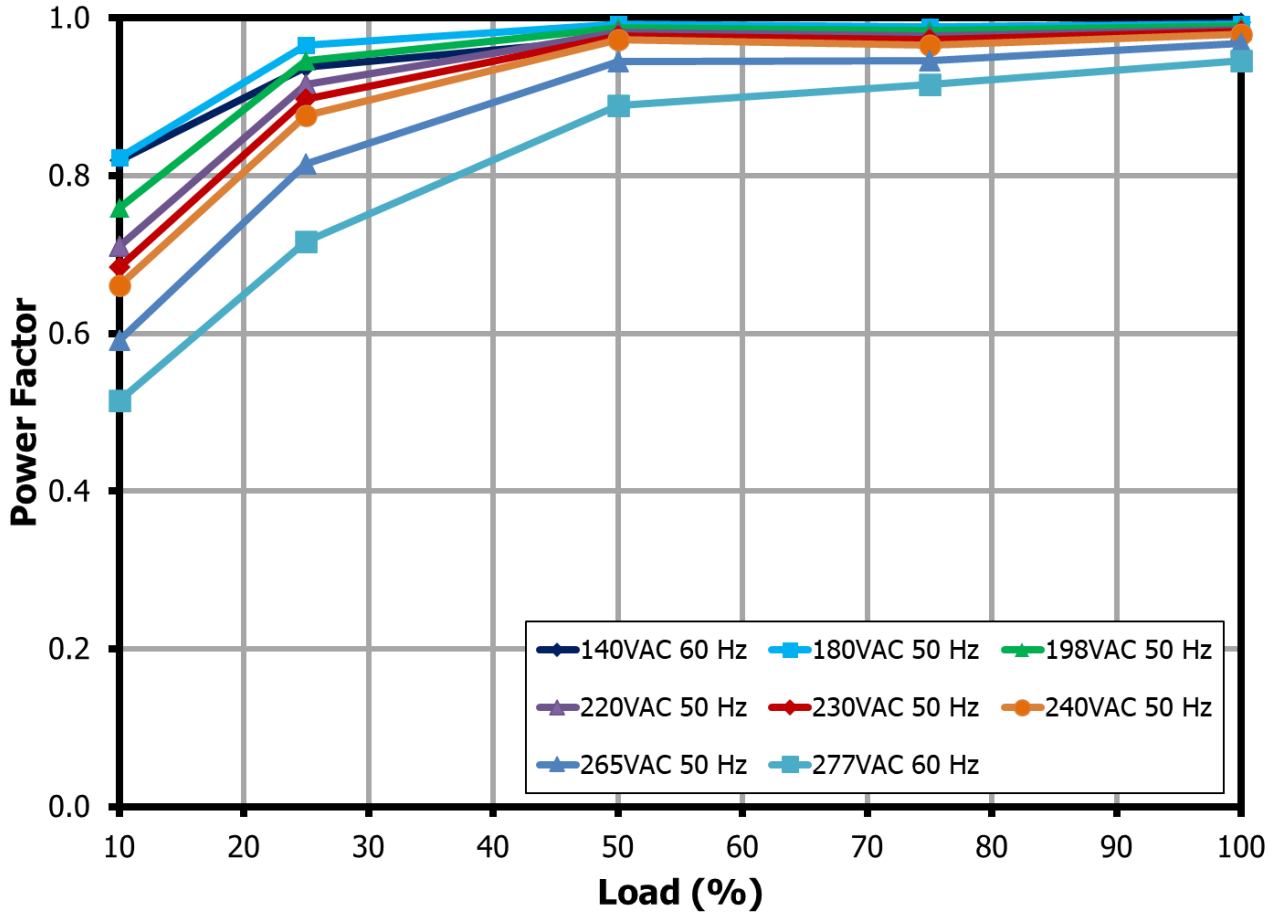


Figure 14 – Power Factor vs Load

11.3 Total Harmonic Distortion (THD)

11.3.1 Total Harmonic Distortion (THD) vs Input Line at Full Load

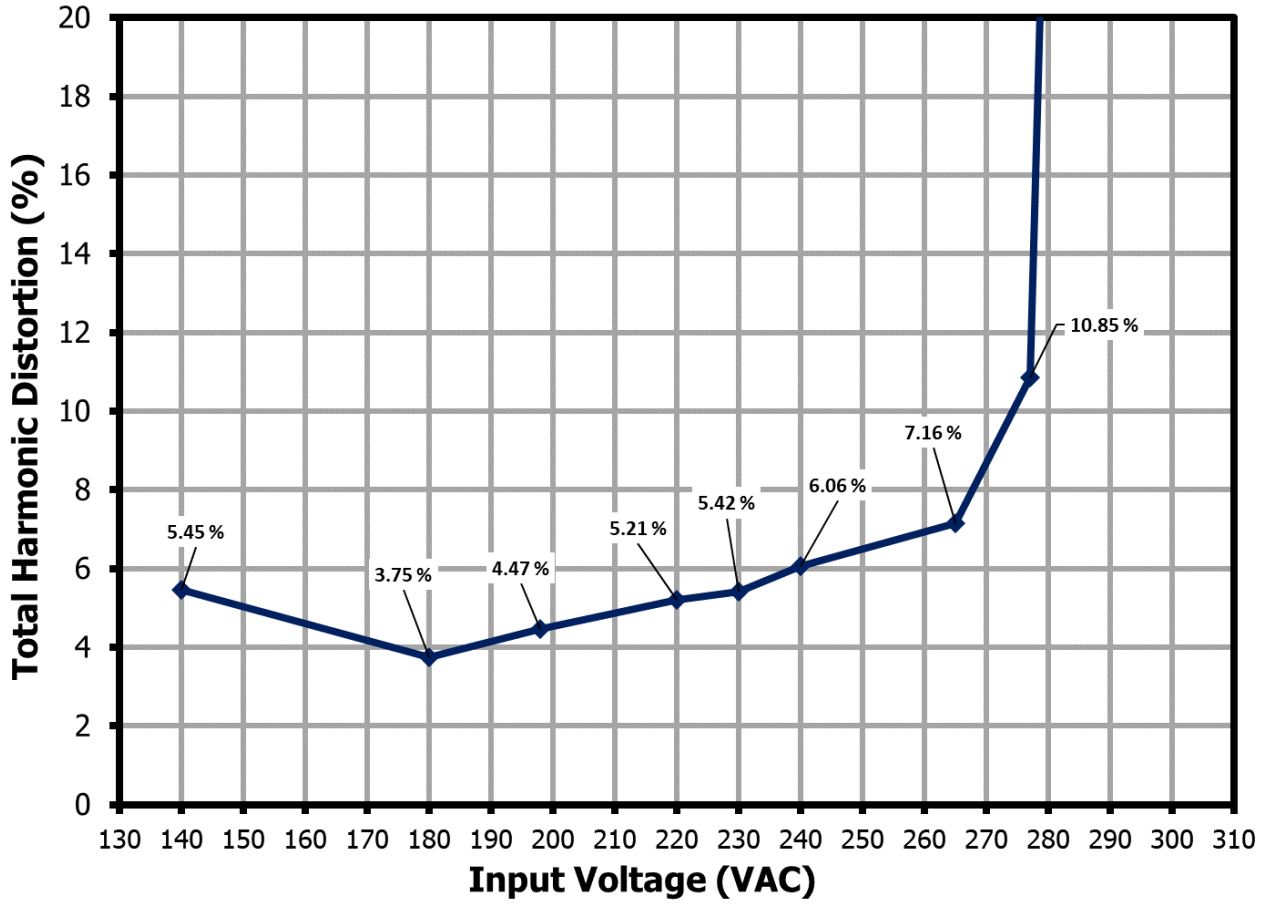


Figure 15 – THD vs Input Line, 24 V Full Load

11.3.2 Total Harmonic Distortion (THD) vs Output Load

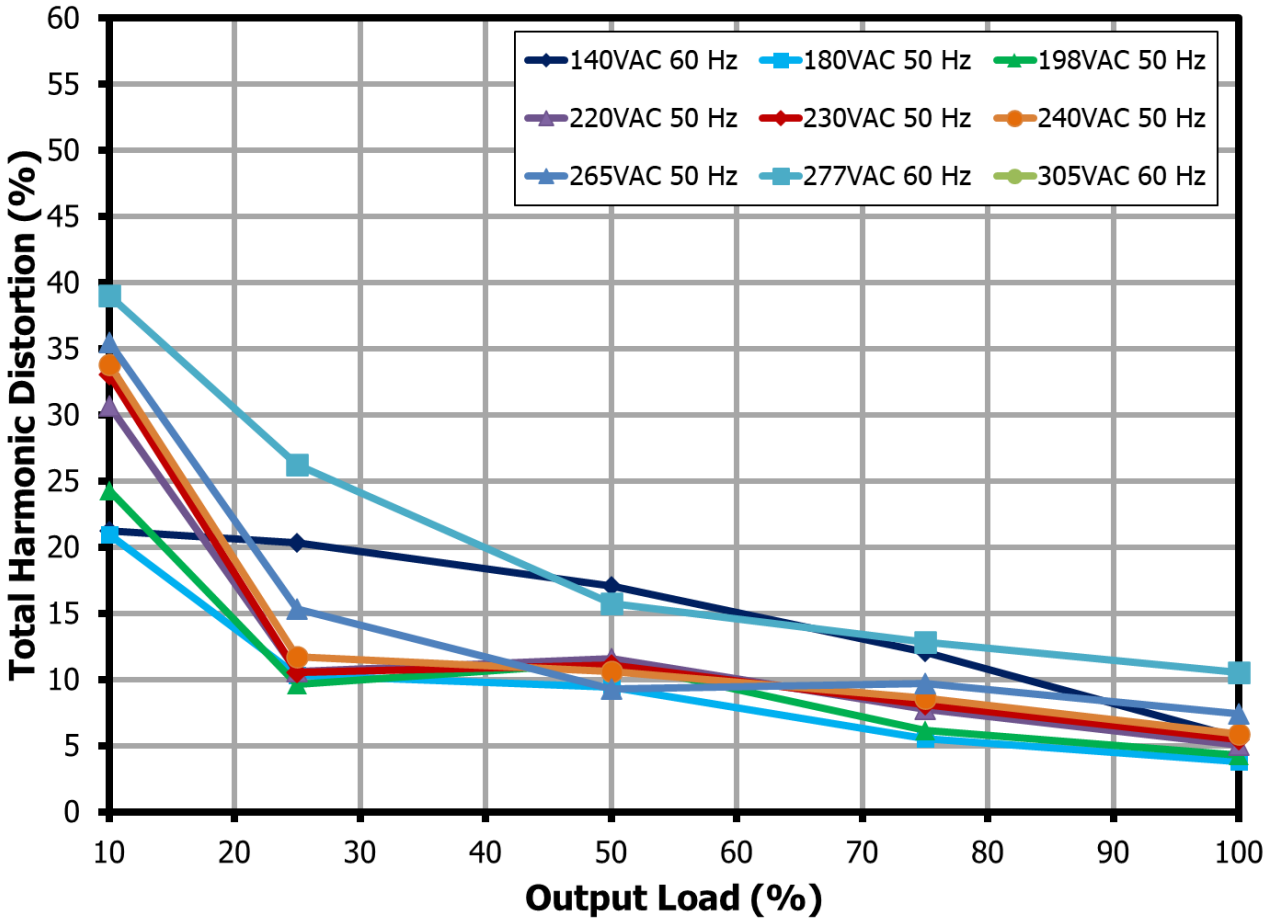


Figure 16 – THD vs Load

11.4 Output Voltage Regulation

Output voltage is measured on the board.

11.4.1 Output Voltage Regulation vs Input Line at Full Load

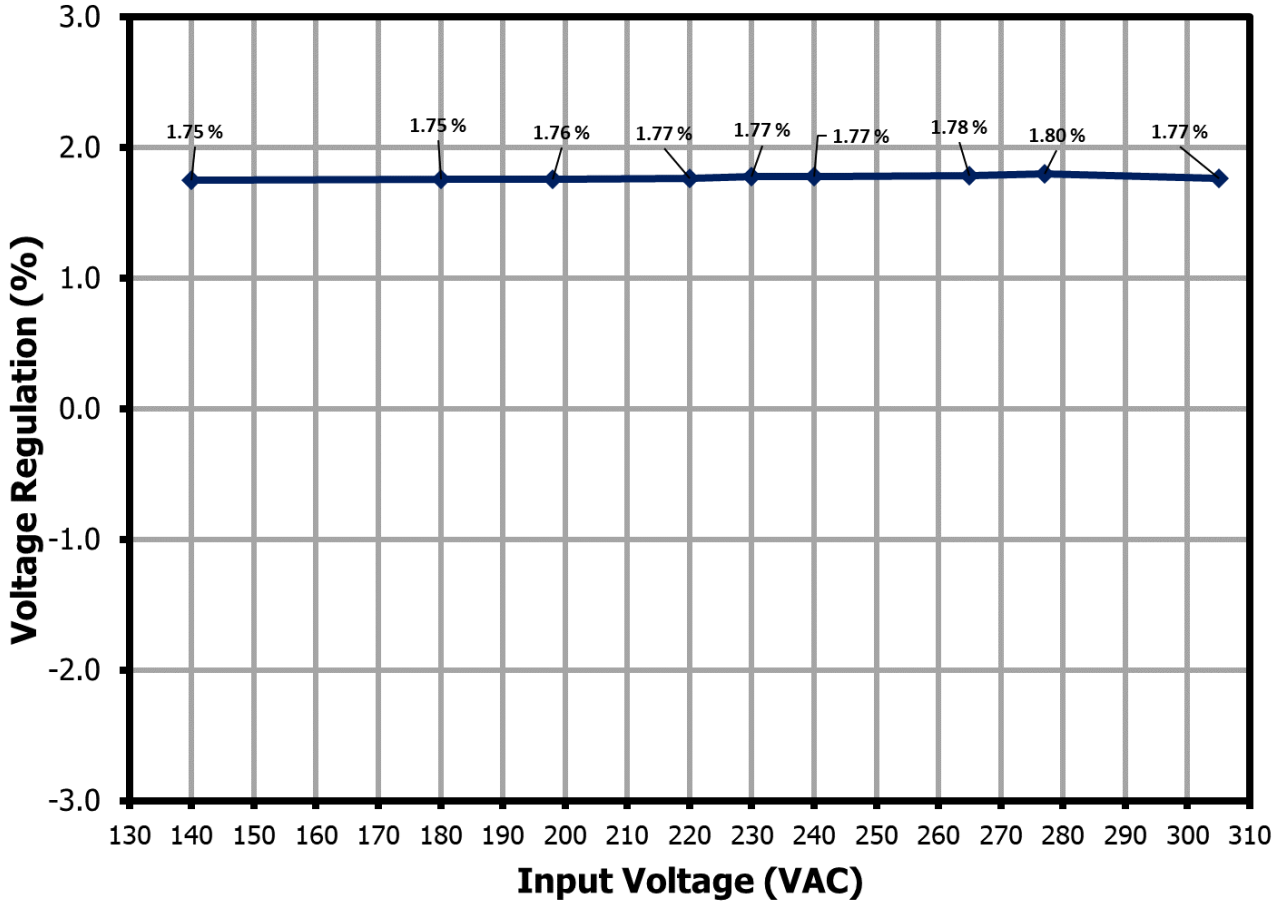


Figure 17 – Voltage Regulation vs Input Line, 24 V Full Load

11.4.2 Output Voltage Regulation vs Output Load

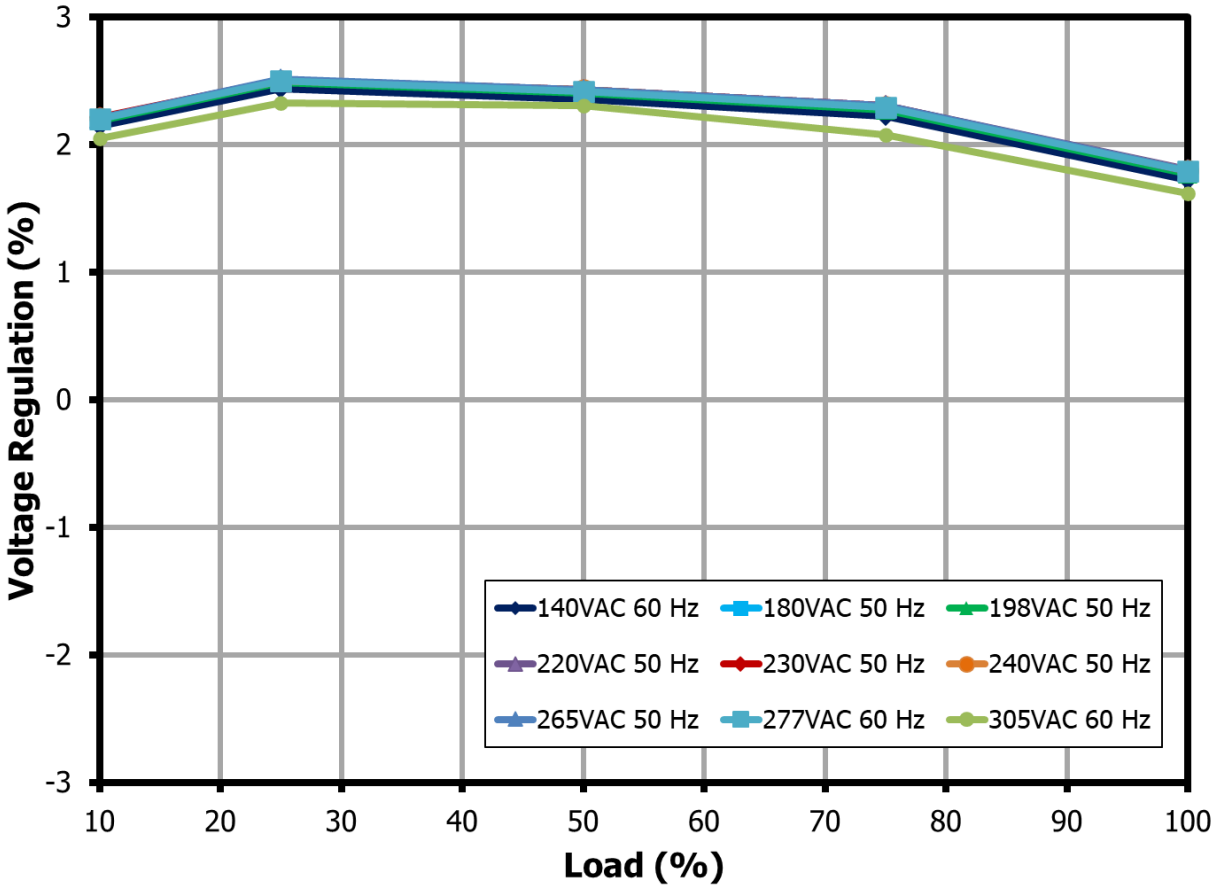


Figure 18 – Voltage Regulation vs Load

11.5 No-Load Input Power

No load input power was measured using a Yokogawa WT310E power meter. The power meter is set at its no load measurement setting to gather the data shown in Figure 19.

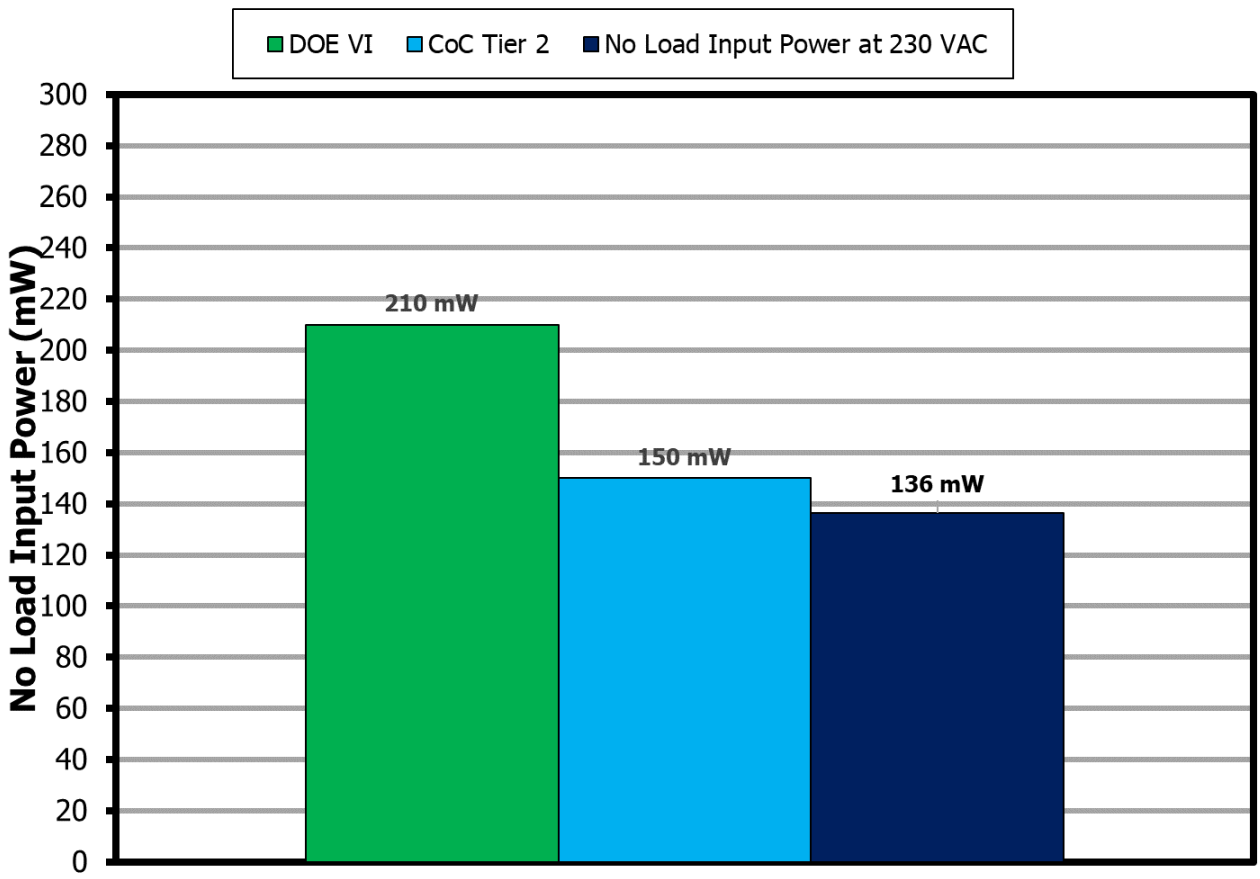


Figure 19 – No-Load Input Power at 230 VAC

11.6 Output Ripple Voltage at 24 V

Output ripple voltage was measured at the end of 100 mΩ output cable.

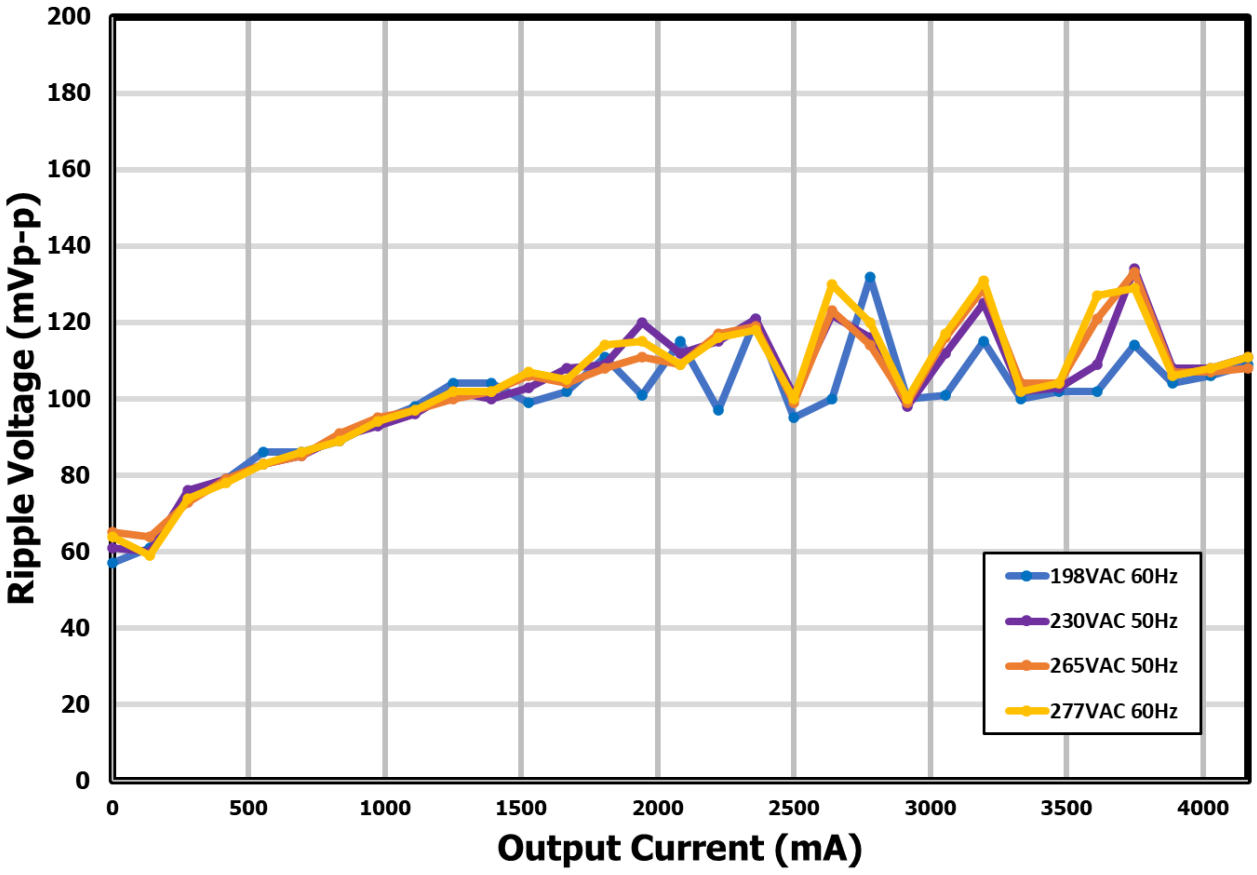


Figure 20 – Ripple voltage vs. Load

11.7 Thermal Test

11.7.1 Thermal testing - Room Temperature

The open frame PSU was placed in a horizontal position inside an acrylic plastic housing. Thermal data were measured using a FLIR IR camera.

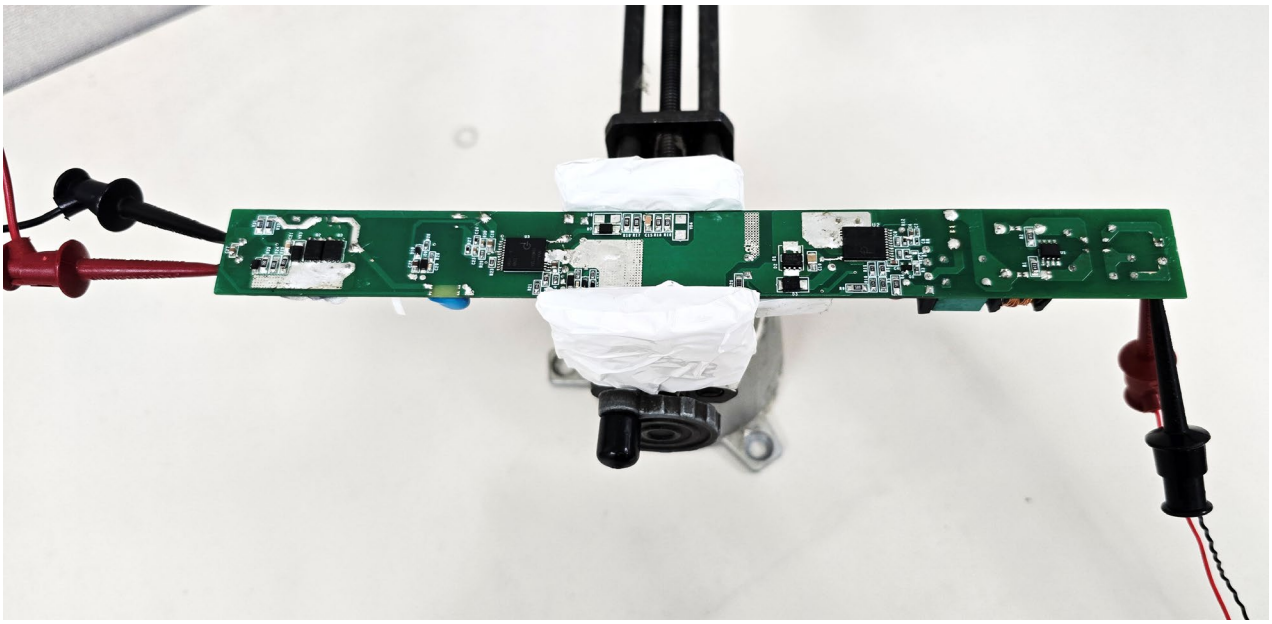


Figure 21 – Thermal Scan Test Set-up

11.7.1.1 Thermal Scan Test Data (Summary)

Circuit Location	Temperature (°C)			
	198 VAC	230 VAC	265 VAC	277 VAC
	50 Hz	50 Hz	50 Hz	60 Hz
U2-(PFS7624C)	91.8	73.9	62.9	65
D1-(Boost Diode)	79.3	69.9	64	63.7
U3-Pri (INN4276C)	77.5	75.7	76	75
U3-Sec (INN4276C)	75.8	74.5	74.6	73.8
Q2/Q3 (SRFET)	75.1	74.3	75.6	75.1
R25 (Sec. Snubber)	72.8	71.5	73.9	73.1
BR1 (Bridge Diode)	74	65.4	60.7	59.3
T1 (Boost Inductor)	70.3	61.1	55.1	54.9
T2 (Flyback TRF)	88.5	87.5	87.8	87

Table 11 – Thermal Scan Test Data

Component temperatures are well within their thermal limits. See the following thermal images for more details.

11.7.1.2 Thermal Scan at 198 VAC 24 V / 4.17 A

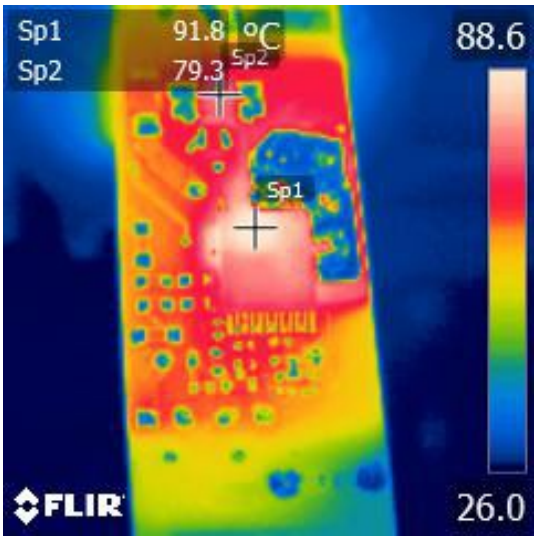


Figure 22 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: U2-(PFS7624C): 91.8 °C
Sp2: D1-(Boost Diode): 79.3 °C

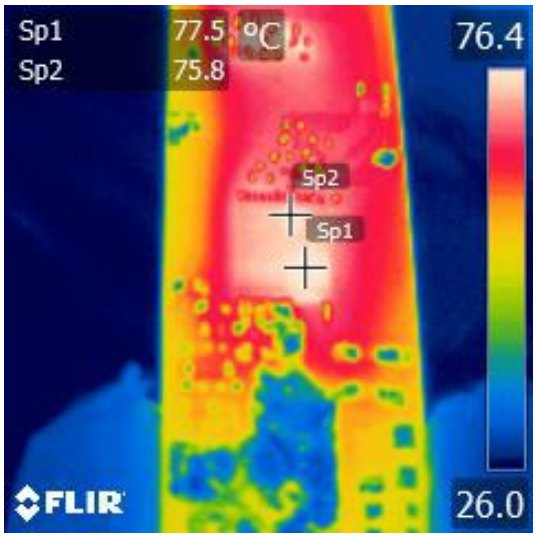


Figure 23 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: U3-Pri (INN4276C): 77.5 °C
Sp1: U3-Sec (INN4276C): 75.8 °C

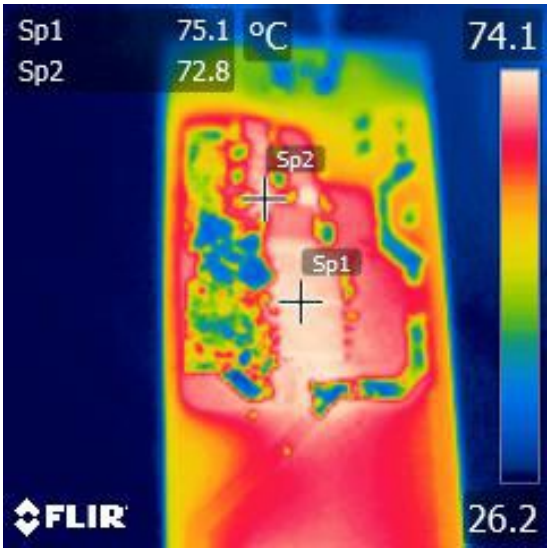


Figure 24 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: Q2/Q3 (SRFET): 75.1 °C
Sp2: R25 (Sec. Snubber): 72.8 °C

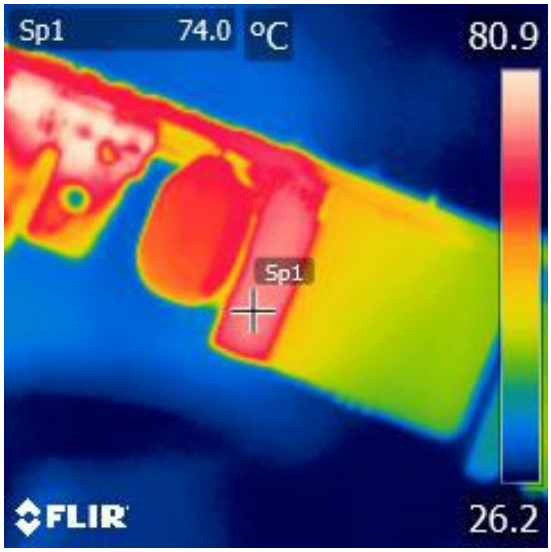


Figure 25 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: BR1 (Bridge Diode): 74 °C

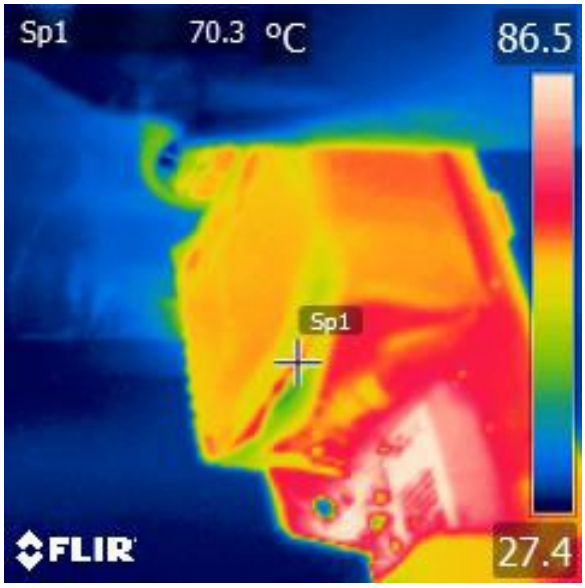


Figure 26 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: T1 (Boost Inductor): 70.3 °C

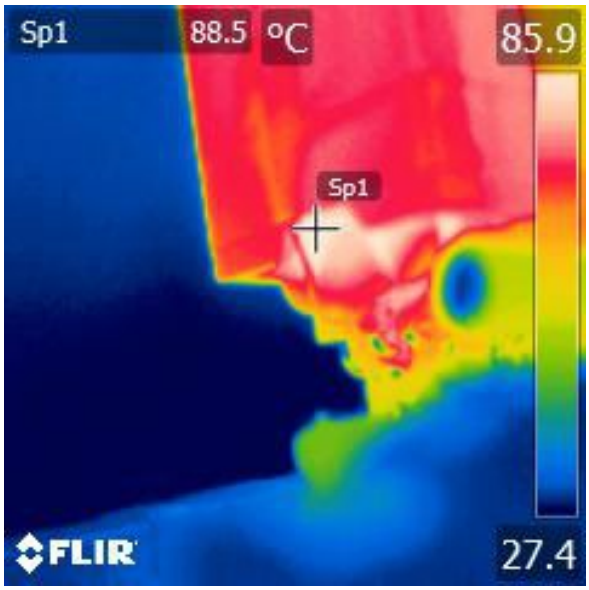


Figure 27 – Thermal Scan 198 V 24 V / 4.17 A
Sp1: T2 (Flyback TRF): 88.5 °C

11.7.1.3 Thermal Scan at 230 VAC 24 V / 4.17 A

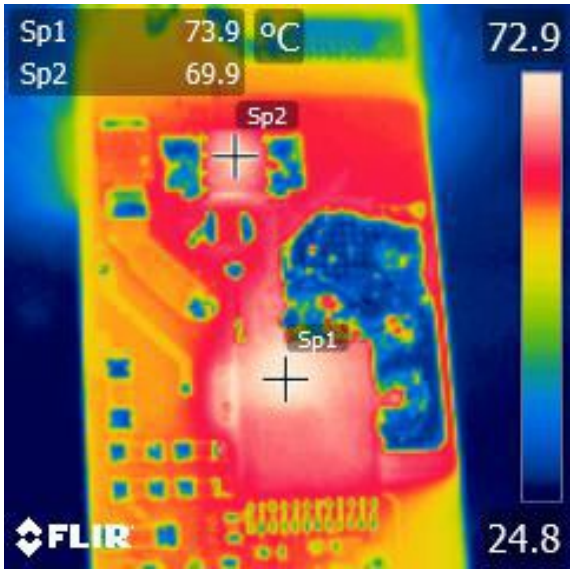


Figure 28 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: U2-(PFS7624C): 73.9 °C
Sp2: D1-(Boost Diode): 69.9 °C

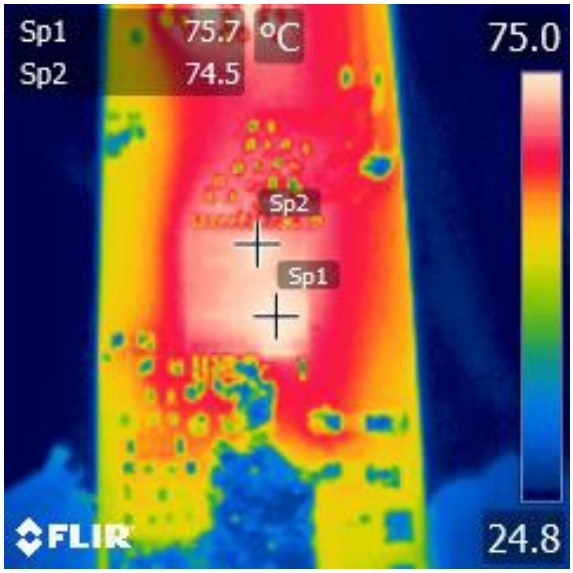


Figure 29 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: U3-Pri (INN4276C): 75.7 °C
Sp1: U3-Sec (INN4276C): 74.5 °C

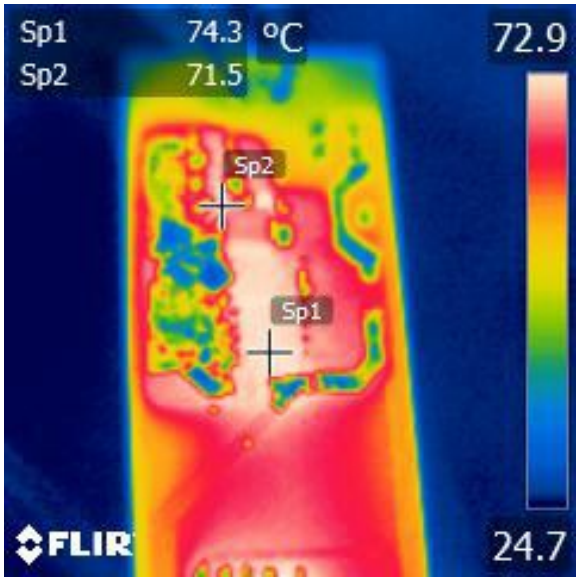


Figure 30 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: Q2/Q3 (SRFET): 74.3 °C
Sp2: R25 (Sec. Snubber): 71.5 °C

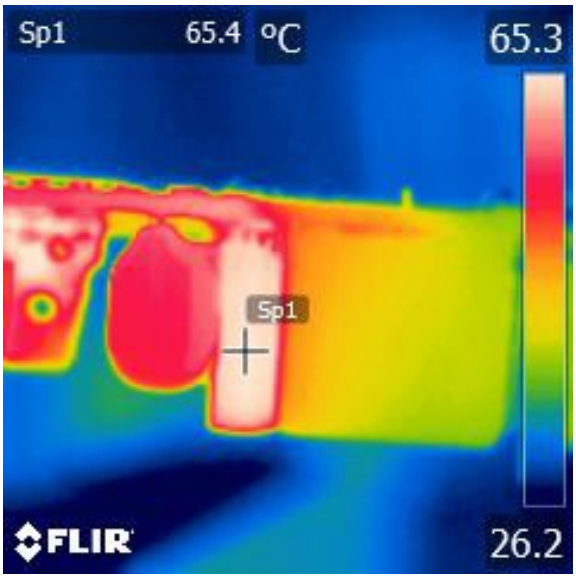


Figure 31 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: BR1 (Bridge Diode): 65.4 °C

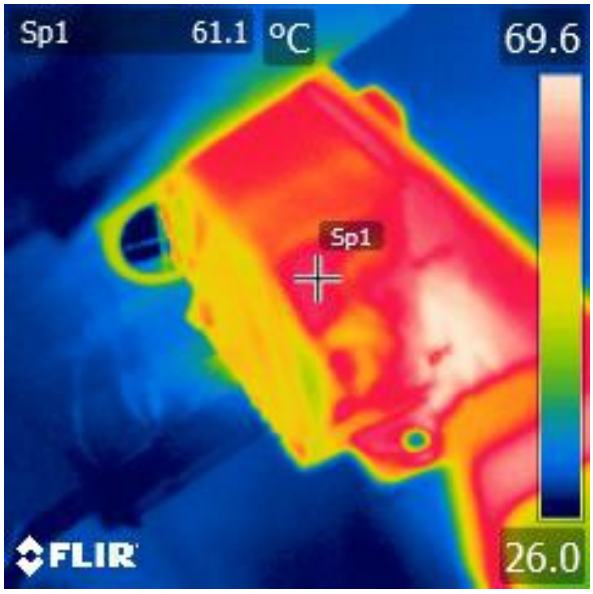


Figure 32 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: T1 (Boost Inductor): 61.1 °C

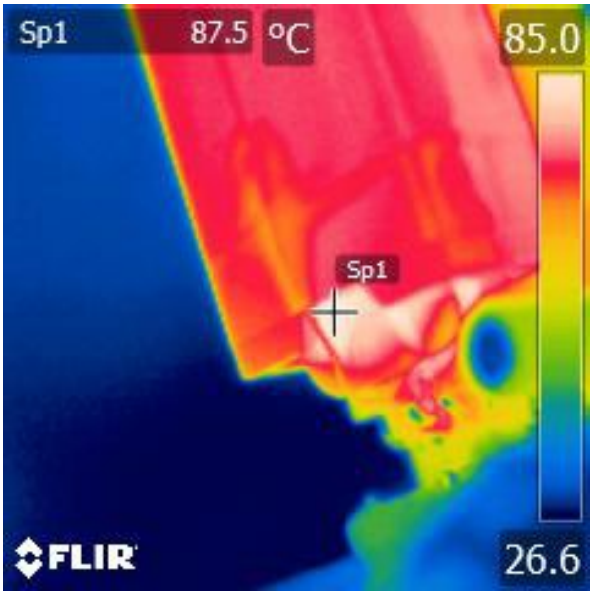


Figure 33 – Thermal Scan 230 V 24 V / 4.17 A
Sp1: T2 (Flyback TRF): 87.5 °C

11.7.1.4 Thermal Scan at 265 VAC 24 V / 4.17 A

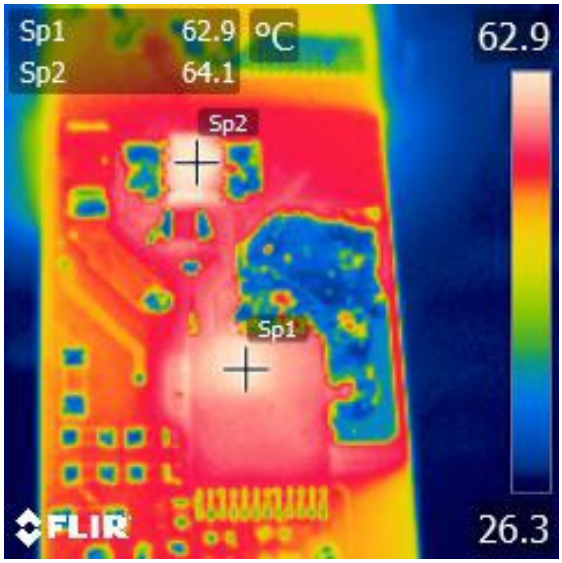


Figure 34 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: U2-(PFS7624C): 62.9 °C
Sp2: D1-(Boost Diode): 64 °C

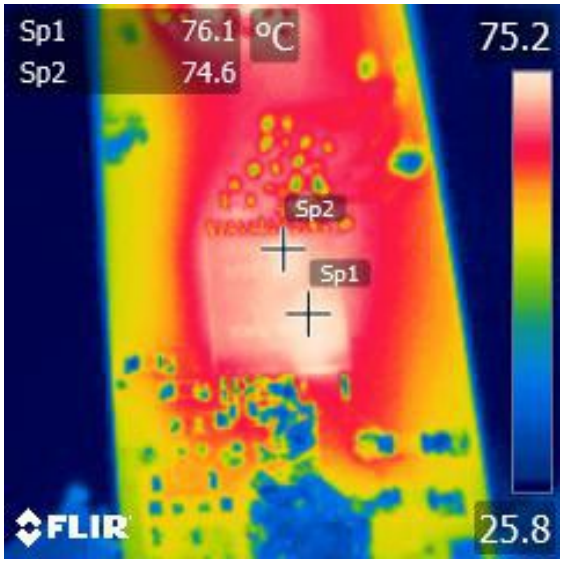


Figure 35 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: U3-Pri (INN4276C): 76 °C
Sp1: U3-Sec (INN4276C): 74.6 °C

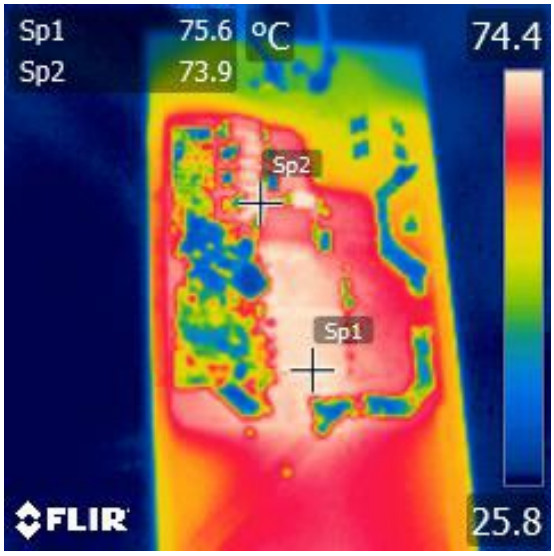


Figure 36 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: Q2/Q3 (SRFET): 75.6 °C
Sp2: R25 (Sec. Snubber): 73.9 °C

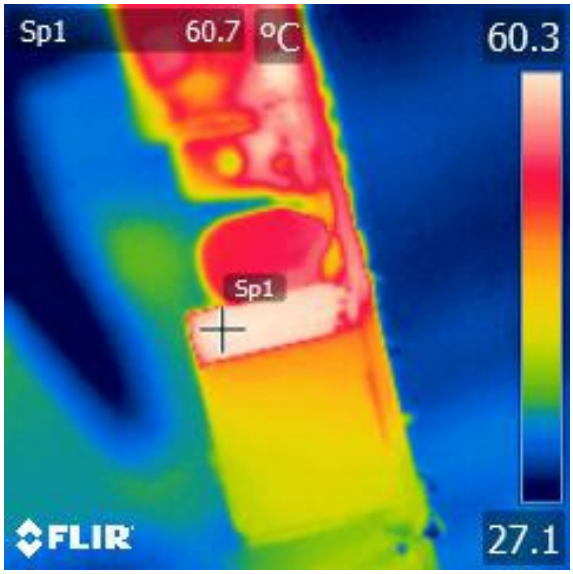


Figure 37 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: BR1 (Bridge Diode): 60.7 °C

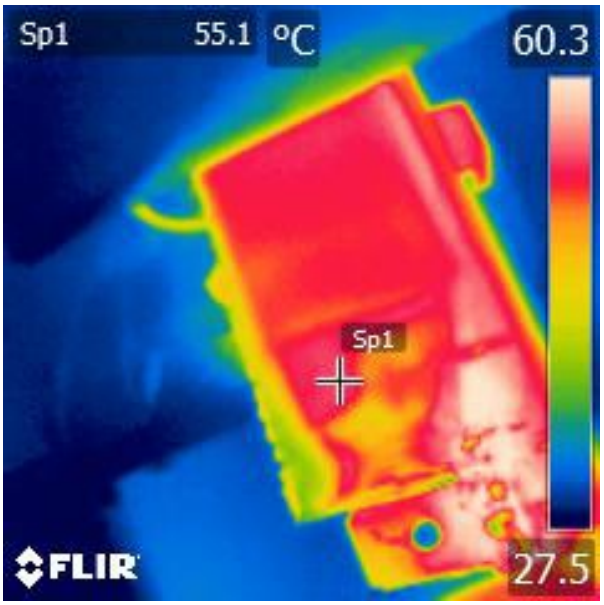


Figure 38 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: T1 (Boost Inductor): 55.1 °C

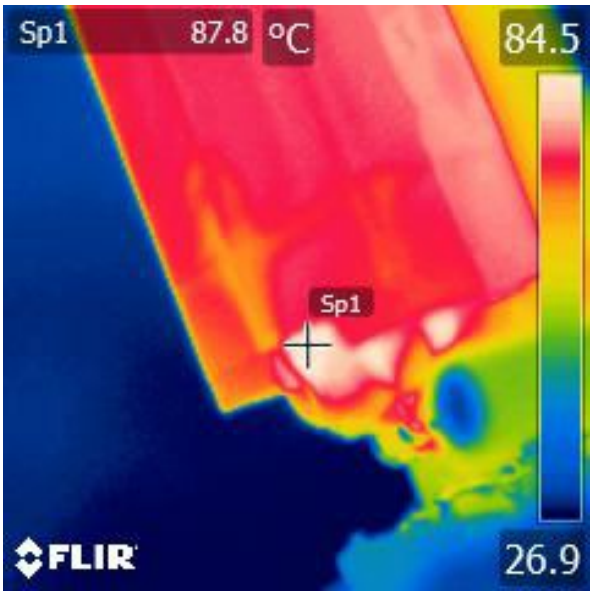


Figure 39 – Thermal Scan 265 V 24 V / 4.17 A
Sp1: T2 (Flyback TRF): 87.8 °C

11.7.1.5 Thermal Scan at 277 VAC 24 V / 4.17 A

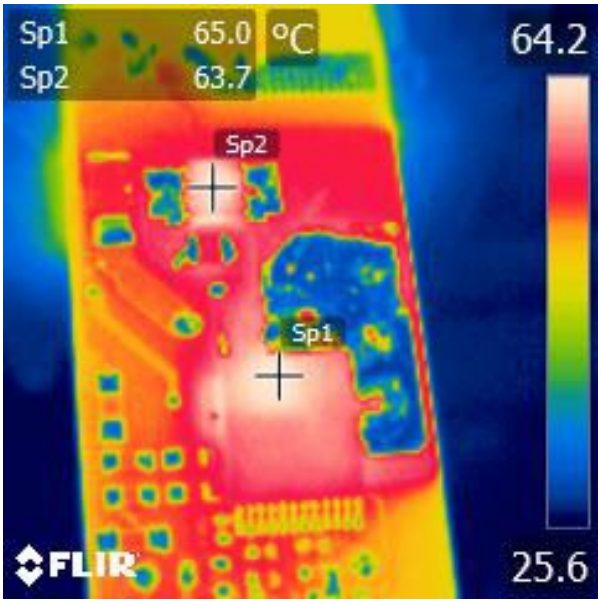


Figure 40 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: U2-(PFS7624C): 65 °C
Sp2: D1-(Boost Diode): 63.7 °C

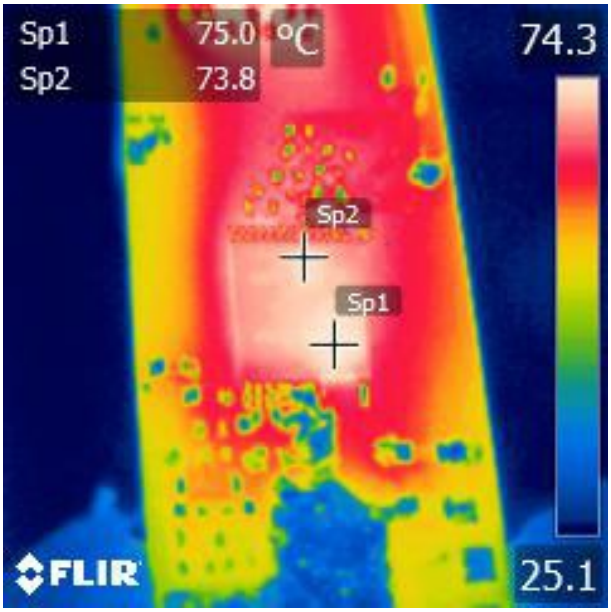


Figure 41 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: U3-Pri (INN4276C): 75 °C
Sp1: U3-Sec (INN4276C): 73.8 °C

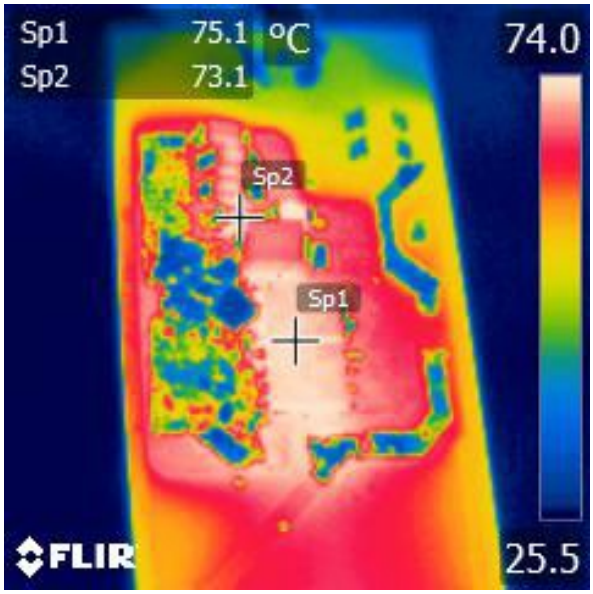


Figure 42 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: Q2/Q3 (SRFET): 75.1 °C
Sp2: R25 (Sec. Snubber): 73.1 °C

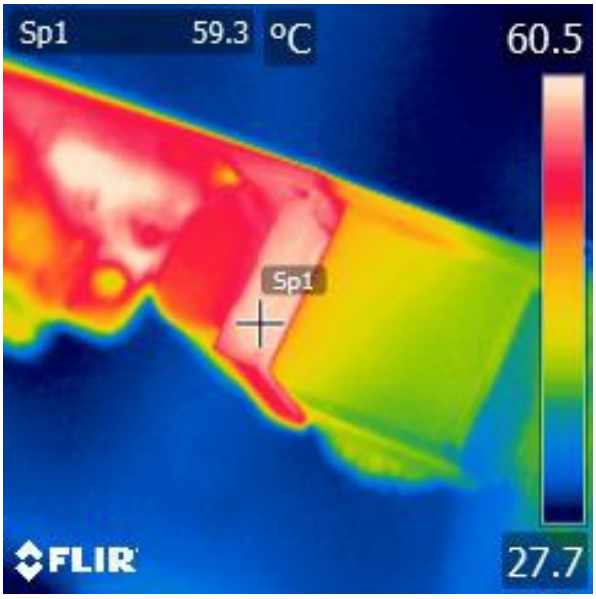


Figure 43 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: BR1 (Bridge Diode): 59.3 °C

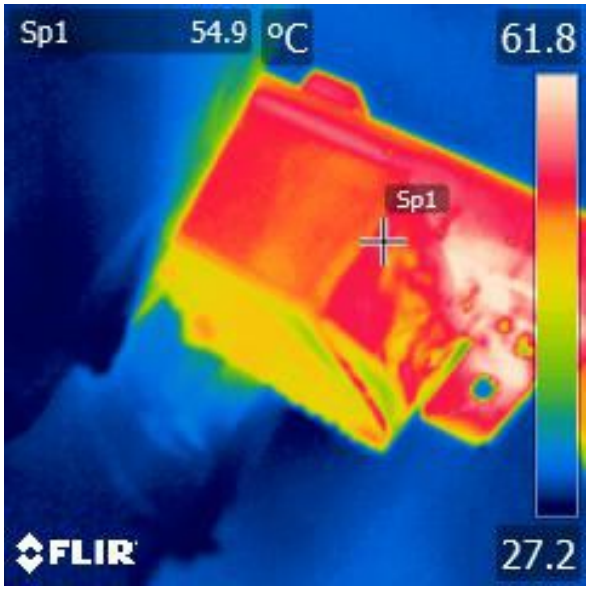


Figure 44 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: T1 (Boost Inductor): 54.9 °C

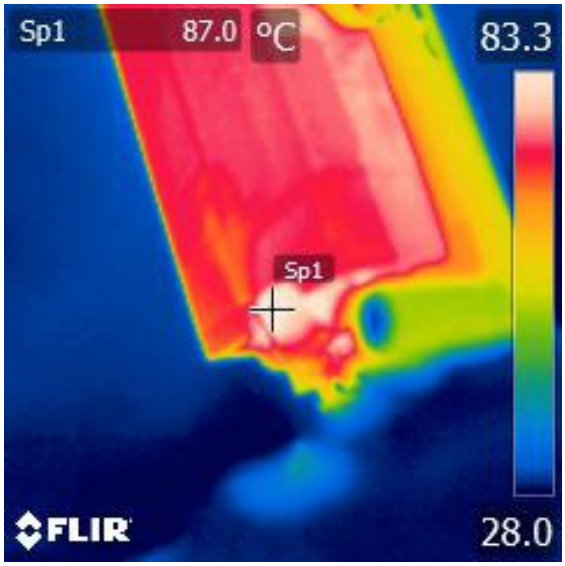


Figure 45 – Thermal Scan 277 V 24 V / 4.17 A
Sp1: T2 (Flyback TRF): 87 °C

11.7.2 Thermal Test at 55 °C Ambient

The PSU was placed inside a closed box to prevent air flow from affecting the thermal measurement. Thermal data were measured using a thermocouple and a Yokogawa data logger.

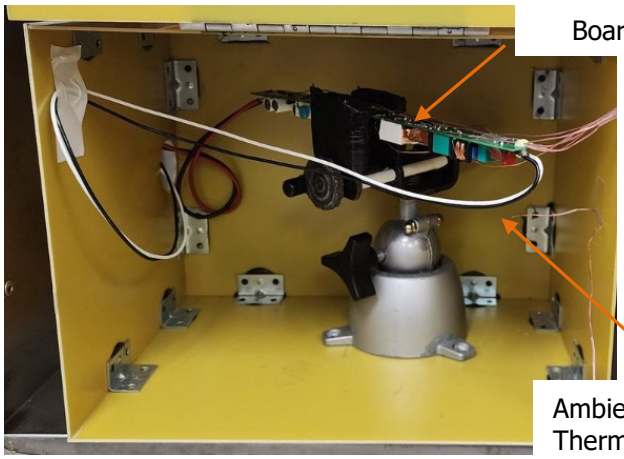


Figure 46 – Upside-Down Orientation Set-up

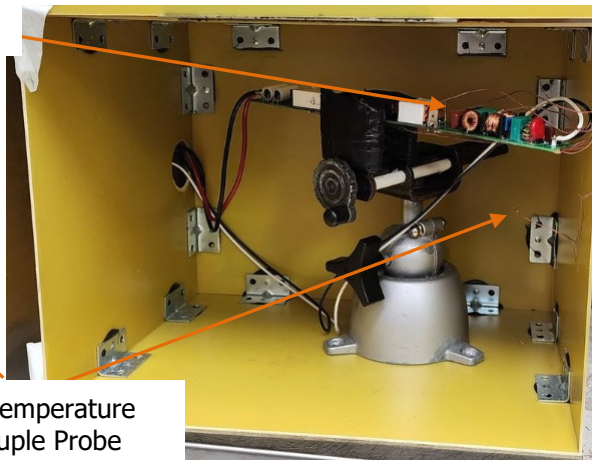


Figure 47 – Upright Position Orientation Set-up

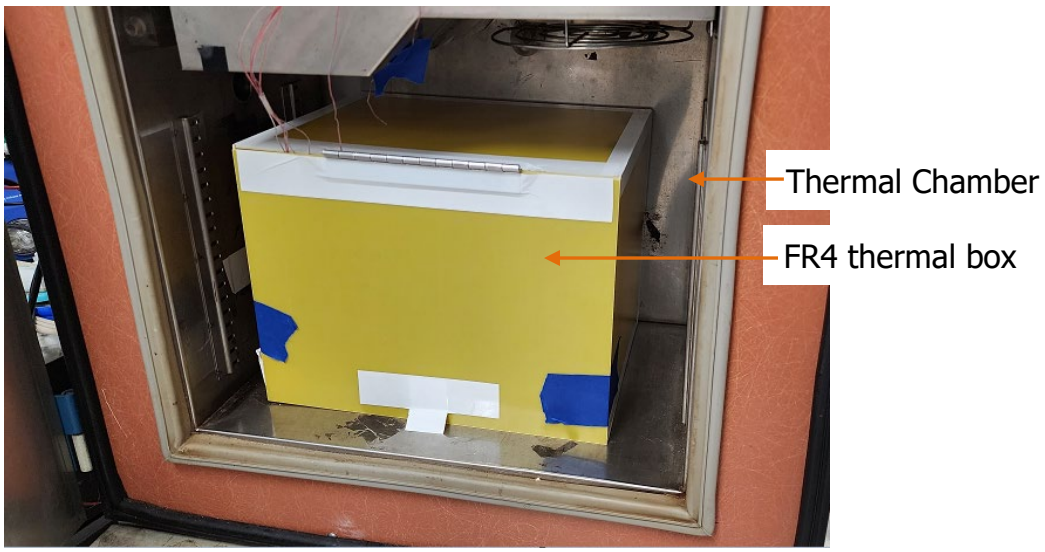


Figure 48 – Thermal Test Set-up at 55 °C Ambient

Thermal Test Data: Upside Down Orientation						
Ref. Des.	Description	Temperature °C				
		198 VAC	230 VAC	265 VAC	277 VAC	300 VAC
T2	Flyback Transformer	112	111	112	112	109
T1	PFC Inductor	93.1	88	82.3	81.9	72.6
U2	PFS4	114	97.5	86.7	89.8	73.2
U3	InnoSwitch4-QR	106	105	104	104	104
Q2/Q3	SRFET	100	102	102	102	103
D1	Boost Diode	106	95.6	89	90.2	78.4
BR1	Bridge Diode	98.2	90.9	85.7	85.3	83.5
Amb	Ambient Temperature	57.1	57.1	57.5	57.8	57.6

Table 12 – Thermal Scan Test Data: Upside Down Orientation

Thermal Test Data: Upright Orientation						
Ref. Des.	Description	Temperature °C				
		198 VAC	230 VAC	265 VAC	277 VAC	300 VAC
T2	Flyback Transformer	109	110	110	111	110
T1	PFC Inductor	99.1	92.5	85.4	90	69.9
U2	PFS4	112	97.8	87.6	89	71.6
U3	InnoSwitch4-QR	102	101	100	101	100
Q2/Q3	SRFET	99.1	99	99.1	100	100
D1	Boost Diode	105	105	90.1	91	75.2
BR1	Bridge Diode	99.7	92.5	86.5	86.5	84.4
Amb	Ambient Temperature	57.3	57.4	57.8	58	57.9

Table 13 – Thermal Scan Test Data: Upright Orientation

All component temperatures are well within their thermal limits.

12 Waveforms

12.1 Start-up Profile

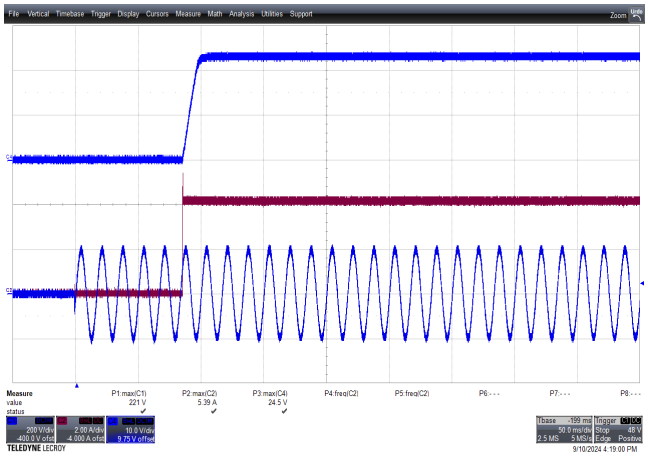


Figure 49 – Start-up Profile
140 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 200 V / div., 50 ms / div.
$t_{ON\ Delay}$: 95 ms

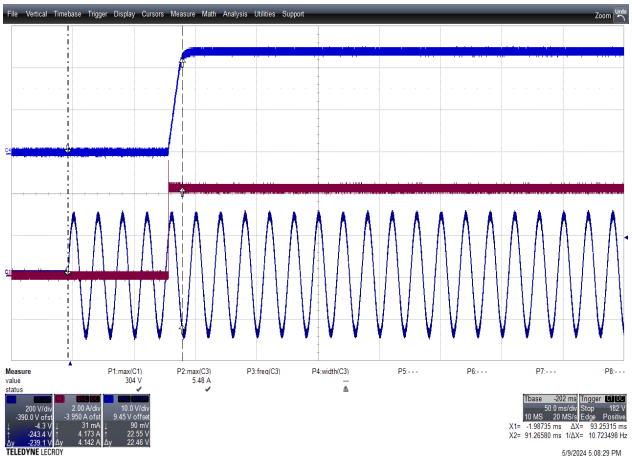


Figure 50 – Start-up Profile
198 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 200 V / div., 50 ms / div.
$t_{ON\ Delay}$: 93 ms

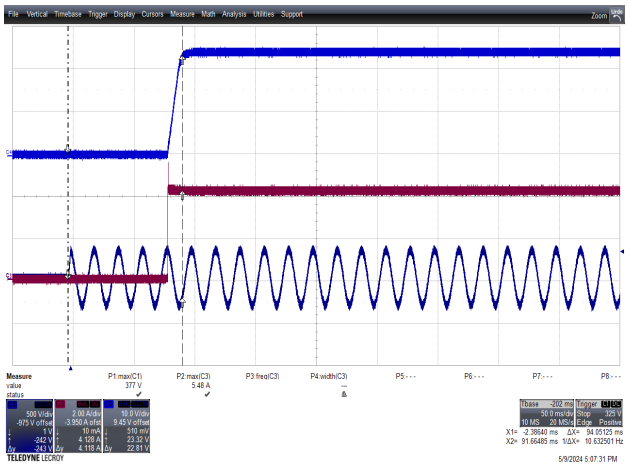


Figure 51 – Start-up Profile
230 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 500 V / div., 50 ms / div.
$t_{ON\ Delay}$: 94 ms

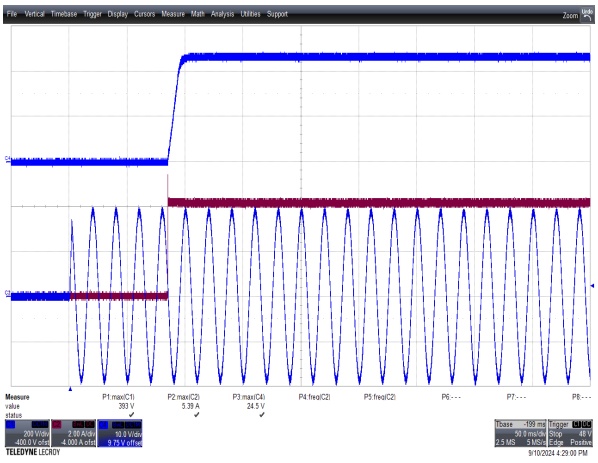


Figure 52 – Start-up Profile
265 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 200 V / div., 50 ms / div.
$t_{ON\ Delay}$: 95 ms

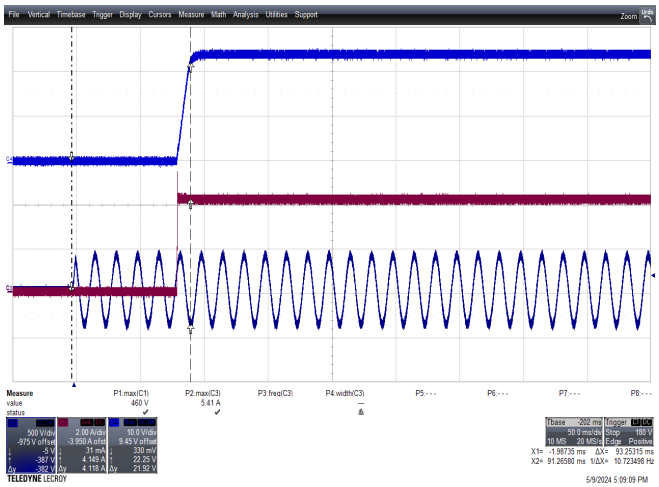


Figure 53 – Start-up Profile
277 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 500 V / div., 20 ms / div.
$t_{ON\ Delay}$: 93 ms

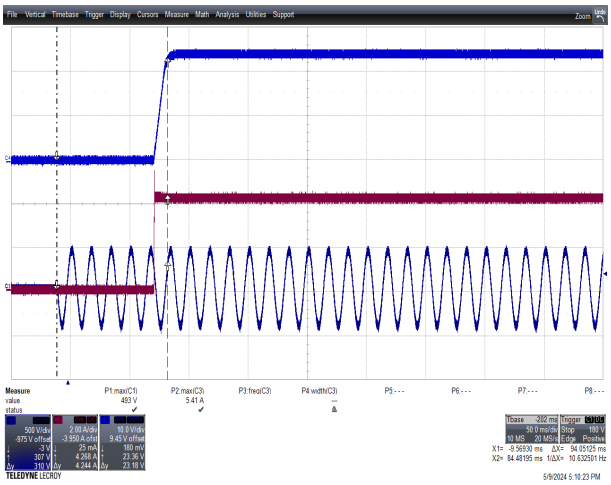


Figure 54 – Start-up Profile
305 VAC, 24 V 4.17 A Start-up
Upper 1: V_{OUT}, 10 V / div.
Uppe 2: I_{LOAD}, 2 A / div.
Lower: V_{IN}, 500 V / div., 20 ms / div.
$t_{ON\ Delay}$: 94 ms

12.2 PFC Drain Voltage and Current

12.2.1 PFC Drain Voltage and Current at Full Load Steady State

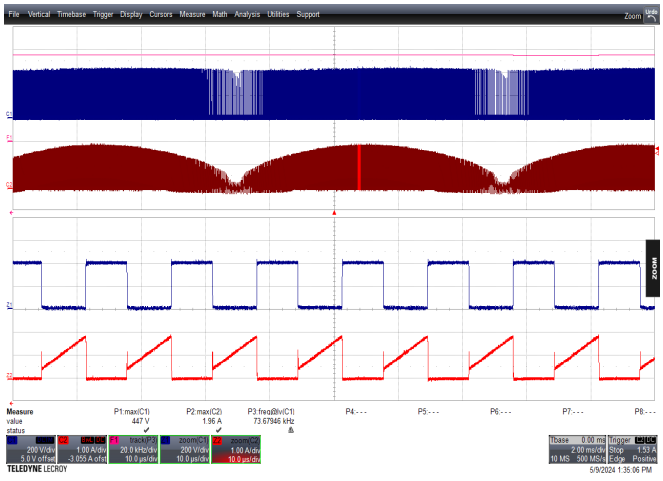


Figure 55 – PFC Primary Voltage and Current
140 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 447 V; I_{DSMAX}: 1.96 A

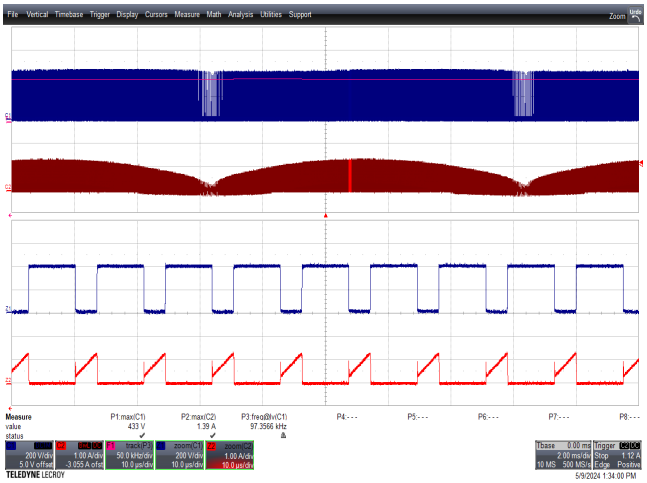


Figure 56 – PFC Drain Voltage and Current
198 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 433 V; I_{DSMAX}: 1.39 A

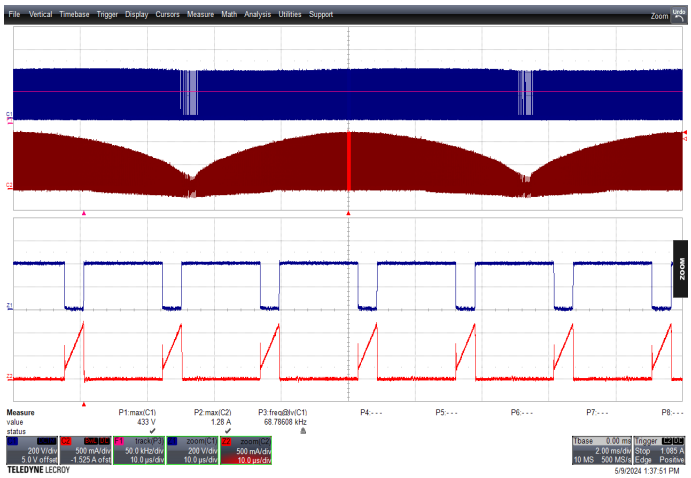


Figure 57 – PFC Drain Voltage and Current
230 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 433 V; I_{DSMAX}: 1.28 A

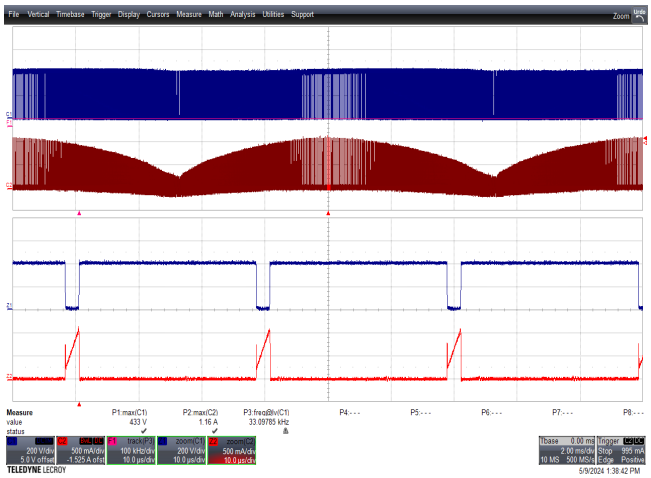


Figure 58 – PFC Primary Voltage and Current
265 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 433 V; I_{DSMAX}: 1.16 A

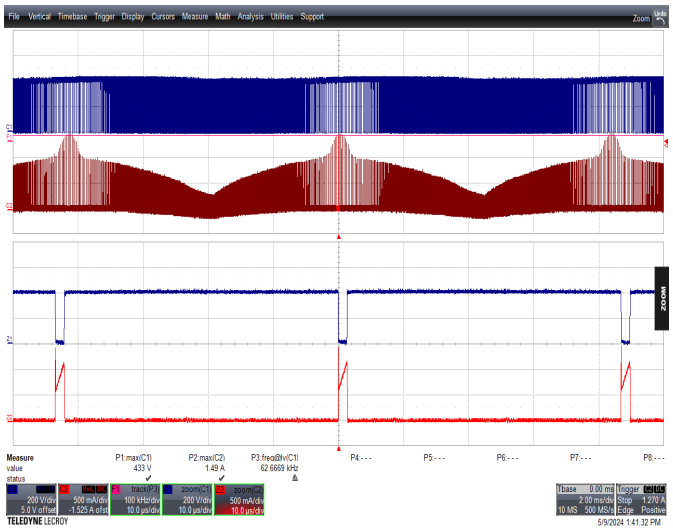


Figure 59 – PFC Drain Voltage and Current
277 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 0.5 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 433 V; I_{DSMAX}: 1.49 A

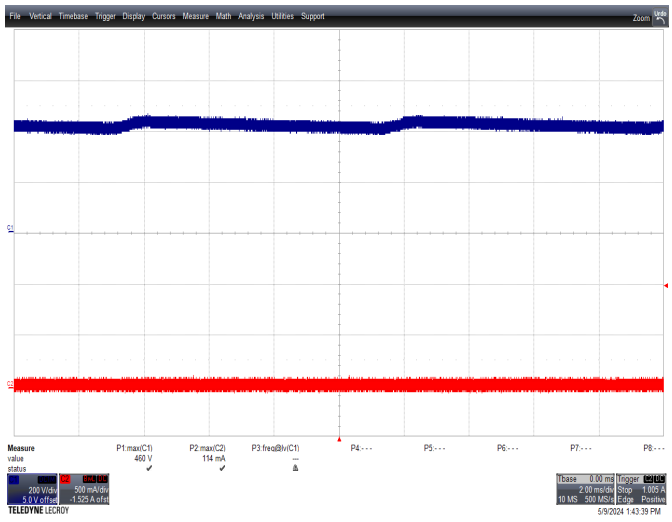


Figure 60 – PFC Drain Voltage and Current
305 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 0.5 A / div., 10 µs / div.(Zoom)
V_{DSMAX}: 460 V; I_{DSMAX}: 114 mA

12.2.2 PFC Drain Voltage and Current at Start-up Full Load

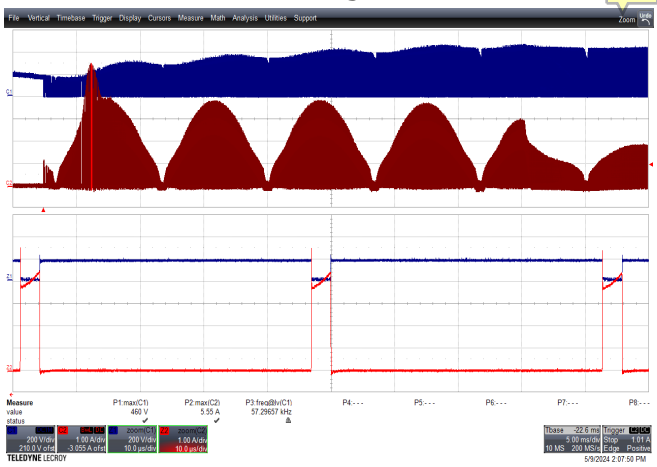


Figure 61 – PFC Drain Voltage and Current
140 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div. (Zoom)
V_{DSMAX}: 460 V; I_{DSMAX}: 5.55 A

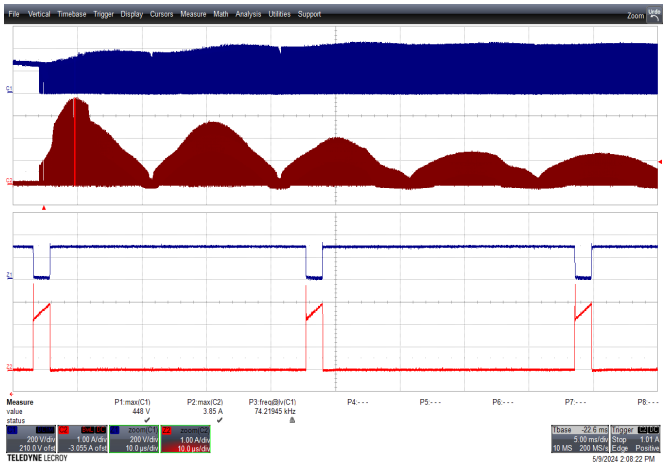


Figure 62 – PFC Drain Voltage and Current
198 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div.,10 µs / div. (Zoom)
V_{DSMAX}: 448 V; I_{DSMAX}: 3.85 A

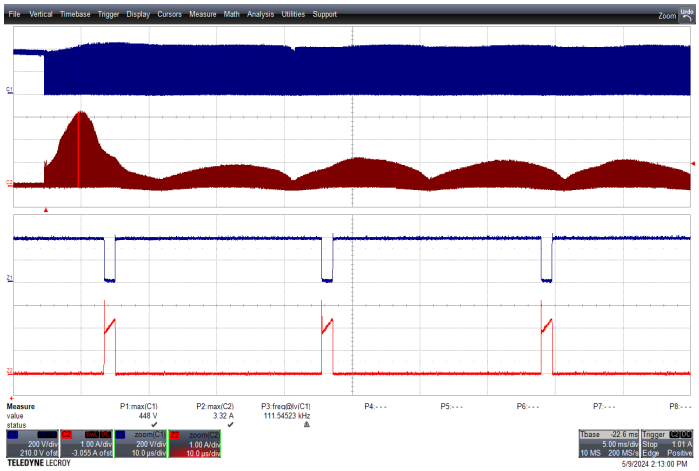


Figure 63 – PFC Drain Voltage and Current
265 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div. (Zoom)
V_{DSMAX}: 448 V; I_{DSMAX}: 3.32 A

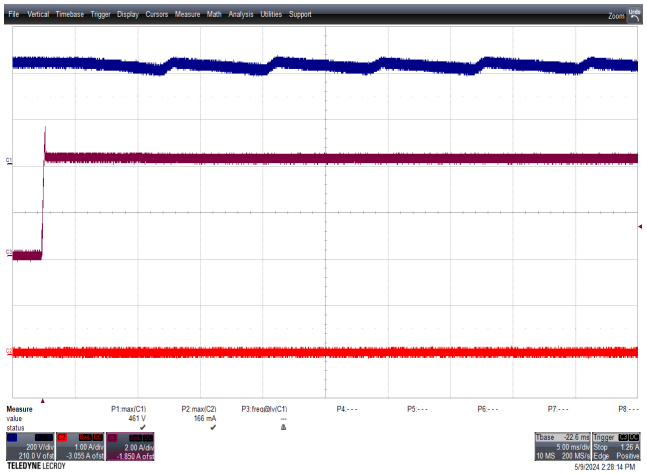


Figure 64 – PFC Drain Voltage and Current
305 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div.,10 µs / div. (Zoom)
V_{DSMAX}: 461 V; I_{DSMAX}: 166 mA

12.2.3 PFC Drain Voltage and Current at Transient Load

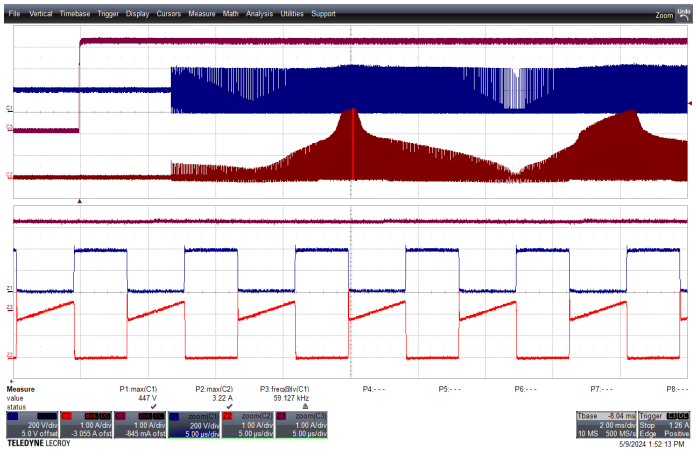


Figure 65 – PFC Drain Voltage and Current
140 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 5 µs / div.(Zoom)
V_{DSMAX}: 447 V; I_{DSMAX}: 3.22 A

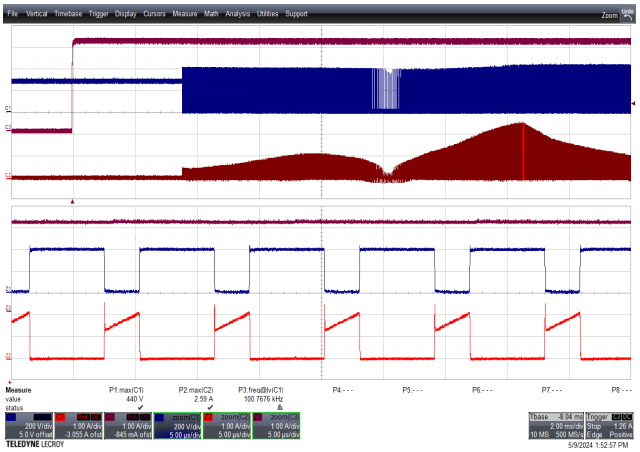


Figure 66 – PFC Drain Voltage and Current
198 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 5 µs / div.(Zoom)
V_{DSMAX}: 440 V; I_{DSMAX}: 2.59 A

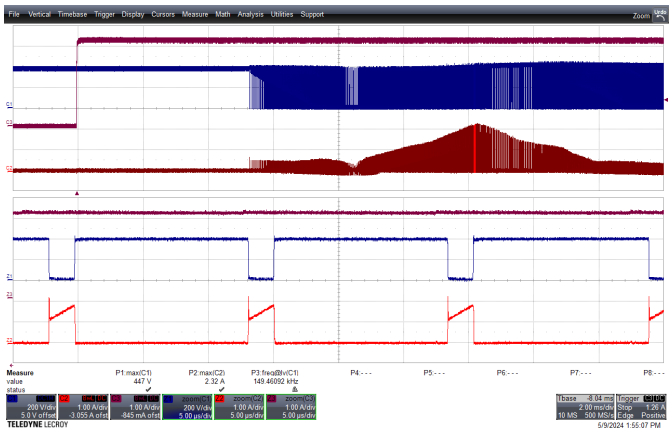


Figure 67 – PFC Drain Voltage and Current
265 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 5 µs / div.(Zoom)
V_{DSMAX}: 447 V; I_{DSMAX}: 2.32 A

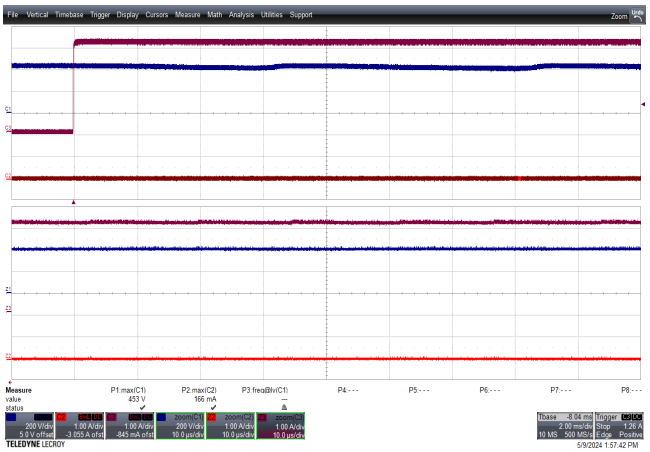


Figure 68 – PFC Drain Voltage and Current
305 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 5 µs / div.(Zoom)
V_{DSMAX}: 453 V; I_{DSMAX}: 166 mA

12.3 PFC Boost Diode Reverse Voltage Waveforms

12.3.1 PFC Boost Diode Reverse Voltage at Full Load Steady State

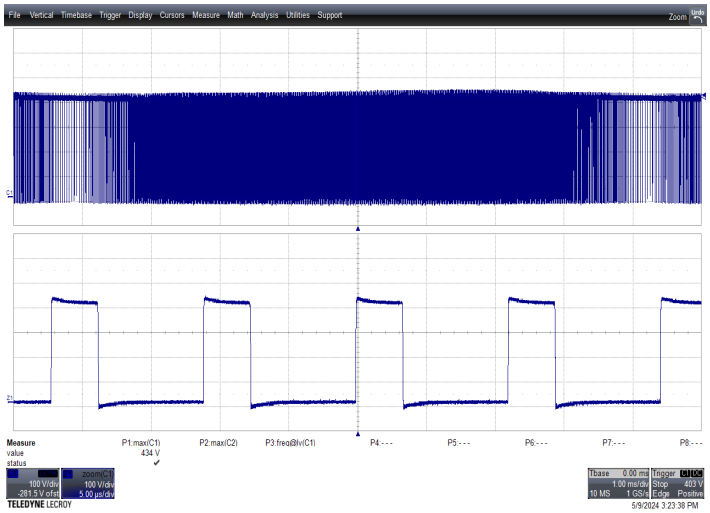


Figure 69 – PFC Boost Diode Reverse Voltage
198 VAC, 24 V 4.17 A Steady-State
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 434 V

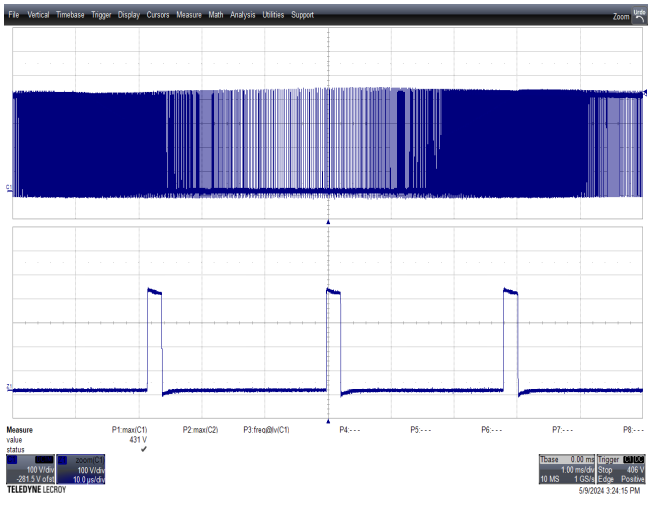


Figure 70 – PFC Boost Diode Reverse Voltage
265 VAC, 24 V 4.17 A Steady-State
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 431 V

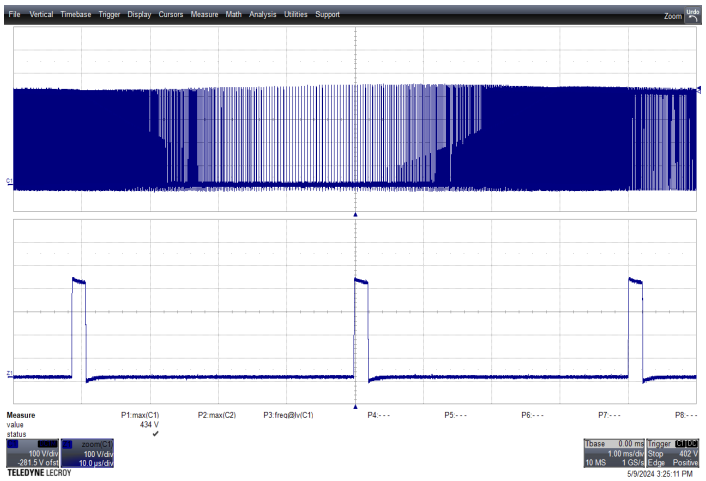


Figure 71 – PFC Boost Diode Reverse Voltage
277 VAC, 24 V 4.17 A Steady-State
V_{DS}, 100 V / div., 10 µs / div.(Zoom)
V_{DMAX}: 434 V

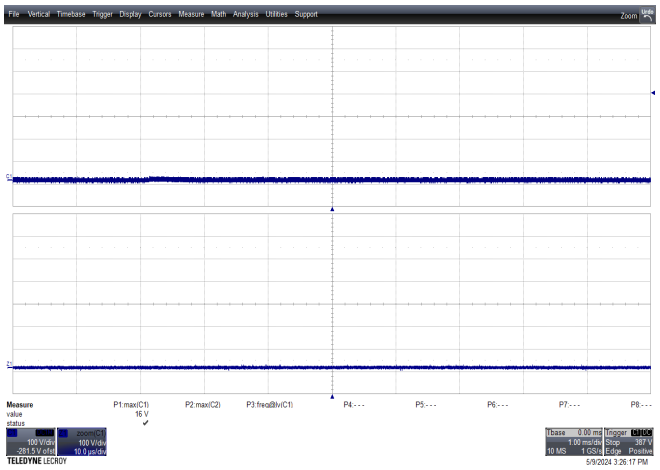


Figure 72 – PFC Boost Diode Reverse Voltage
305 VAC, 24 V 4.17 A Steady-State
V_{DS}, 100 V / div., 10 µs / div.(Zoom)
V_{DMAX}: 16 V

12.3.2 PFC Boost Diode Reverse Voltage at Start-up Full Load

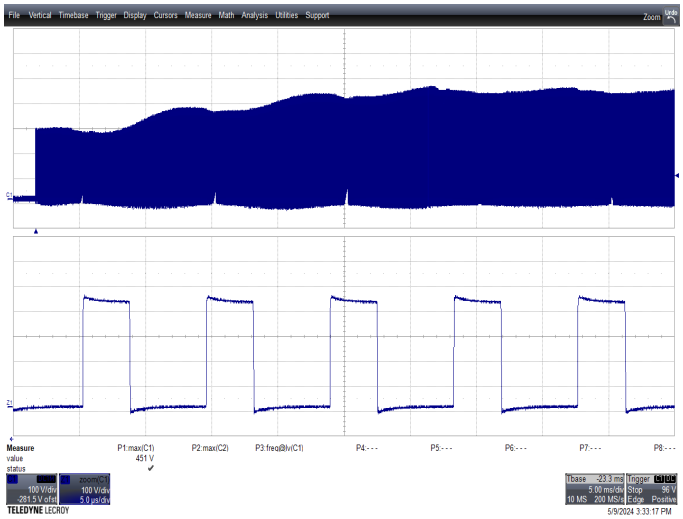


Figure 73 – PFC Boost Diode Reverse Voltage
198 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 451 V

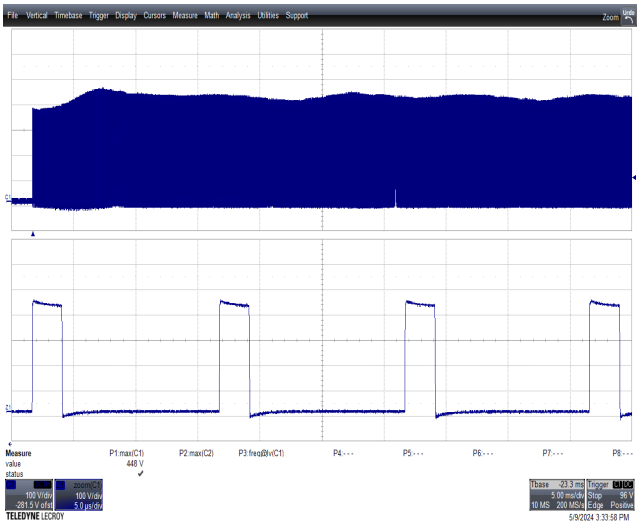


Figure 74 – PFC Boost Diode Reverse Voltage
265 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 448 V

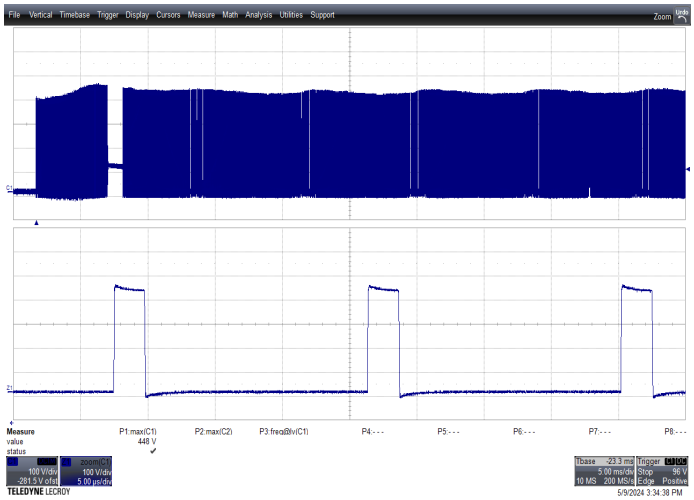


Figure 75 – PFC Boost Diode Reverse Voltage
277 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 448 V

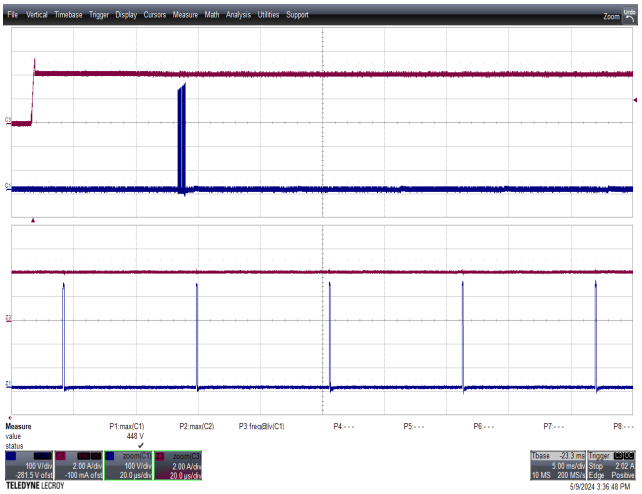


Figure 76 – PFC Boost Diode Reverse Voltage
305 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 448 V

12.3.3 PFC Boost Diode Reverse Voltage at Transient Load

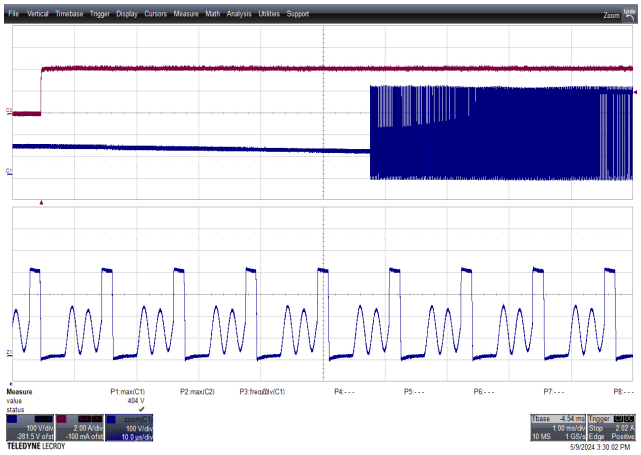


Figure 77 – PFC Boost Diode Reverse Voltage
198 VAC, 24 V 4.17 A Transient
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 404 V

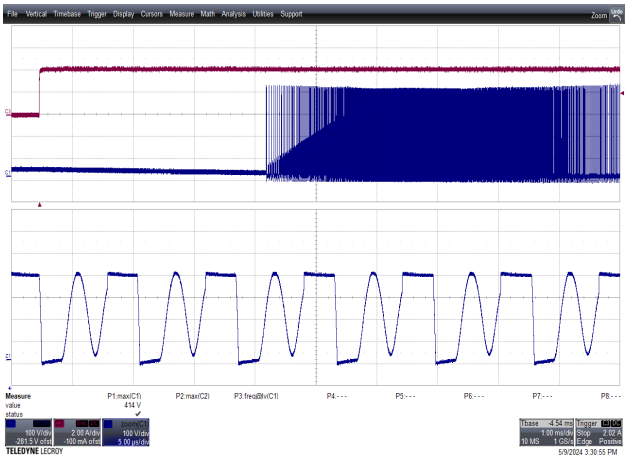


Figure 78 – PFC Boost Diode Reverse Voltage
265 VAC, 24 V 4.17 A Transient
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMX}: 414 V

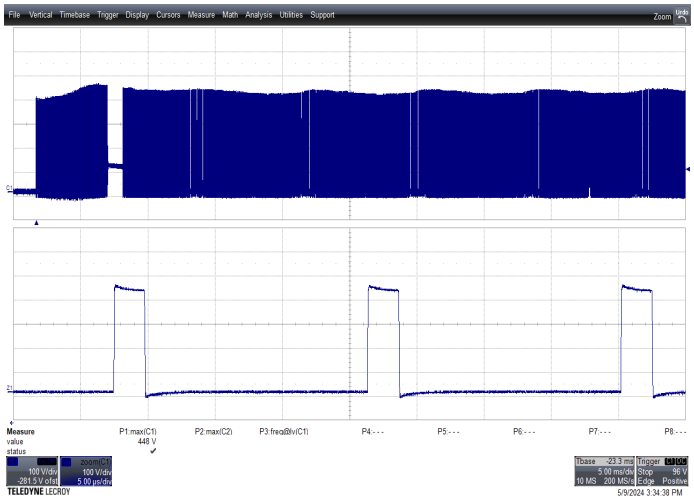


Figure 79 – PFC Boost Diode Reverse Voltage
277 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 448 V

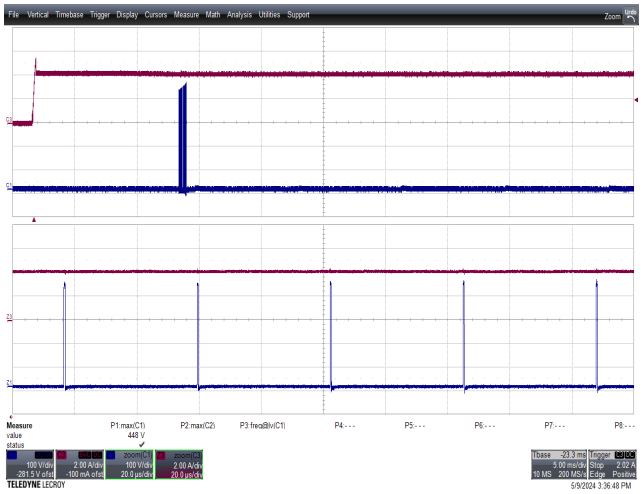


Figure 80 – PFC Boost Diode Reverse Voltage
305 VAC, 24 V 4.17 A Start-up
V_{DS}, 100 V / div., 5 µs / div.(Zoom)
V_{DMAX}: 448 V

12.4 Flyback Primary Drain Voltage and Current

12.4.1 Flyback Primary Drain Voltage and Current at Full Load Steady State

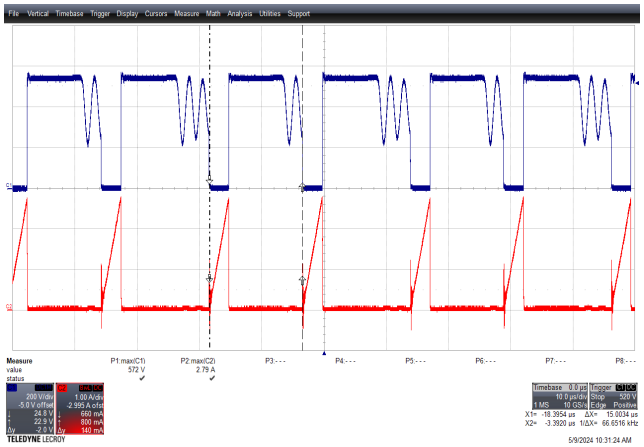


Figure 81 – Primary Drain Voltage and Current
140 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 572 V; I_{DSMAX}: 2.79 A

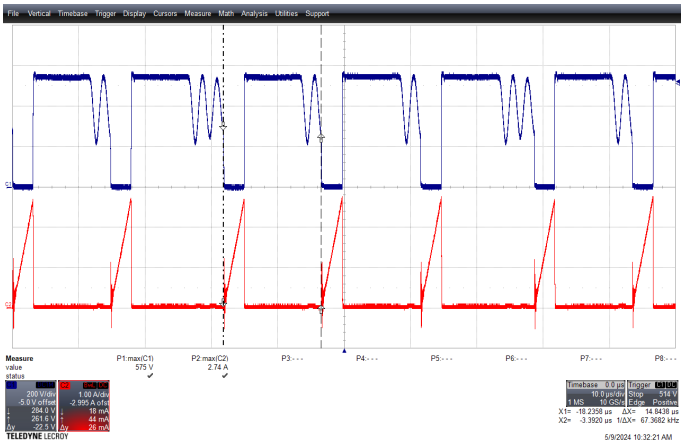


Figure 82 – Primary Drain Voltage and Current
198 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 575 V; I_{DSMAX}: 2.74 A

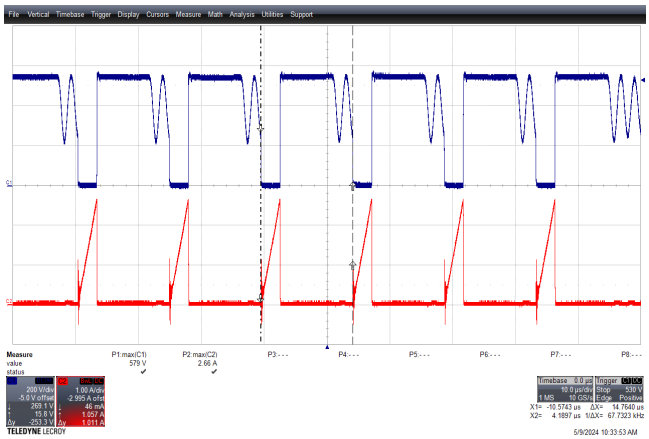


Figure 83 – Primary Drain Voltage and Current
230 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 579 V; I_{DSMAX}: 2.66 A

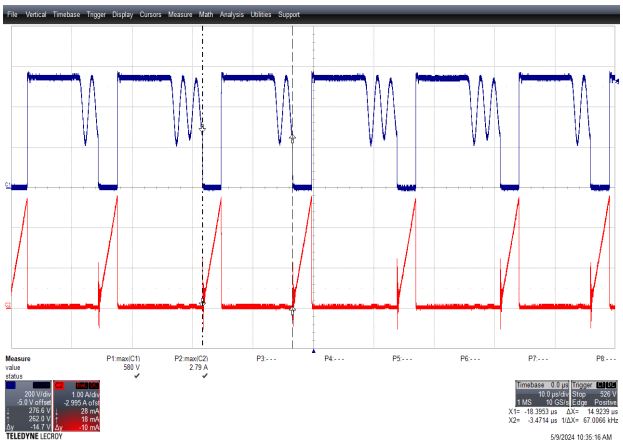


Figure 84 – Primary Drain Voltage and Current
265 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 580 V; I_{DSMAX}: 2.79 A

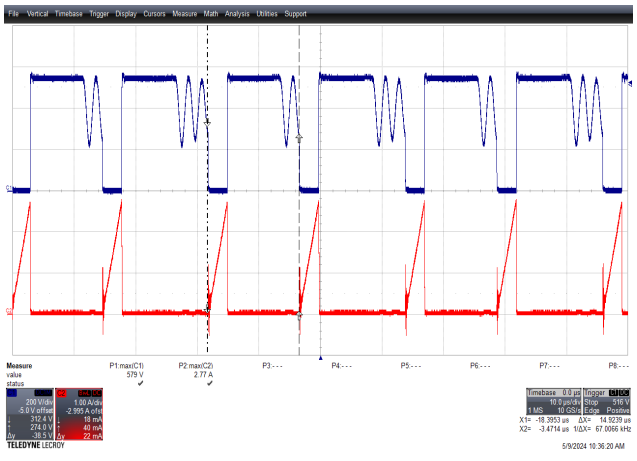


Figure 85 – Primary Drain Voltage and Current
277 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 579 V; I_{DSMAX}: 2.77 A

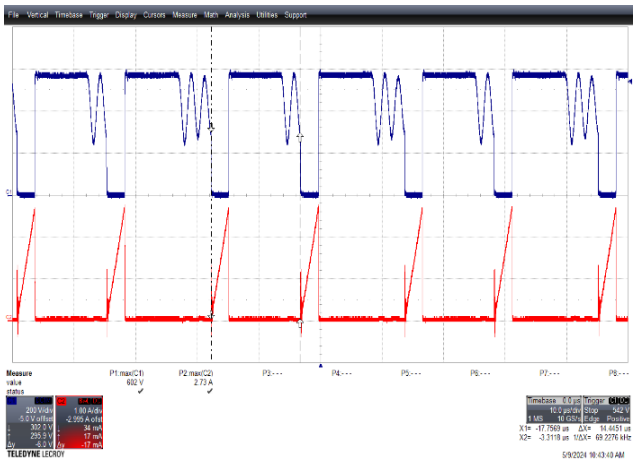


Figure 86 – Primary Drain Voltage and Current
305 VAC, 24 V 4.17 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
V_{DSMAX}: 602 V; I_{DSMAX}: 2.73 A

12.4.2 Flyback Primary Drain Voltage and Current at Start-up Full Load

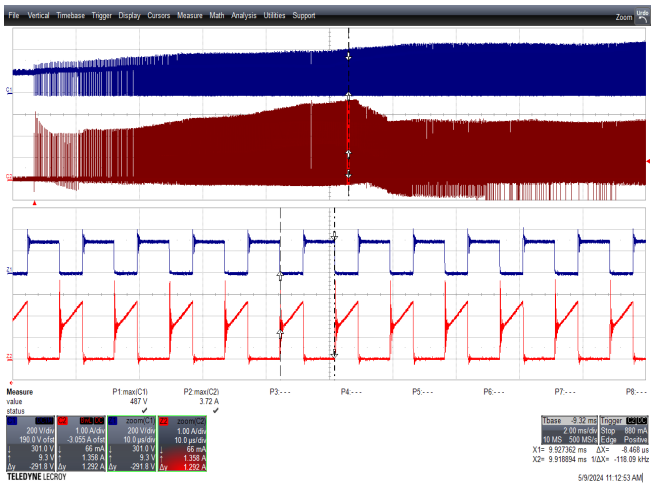


Figure 87 – Primary Drain Voltage and Current
140 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div.
(Zoom)
V_{DSMAX}: 487 V; I_{DSMAX}: 3.72 A

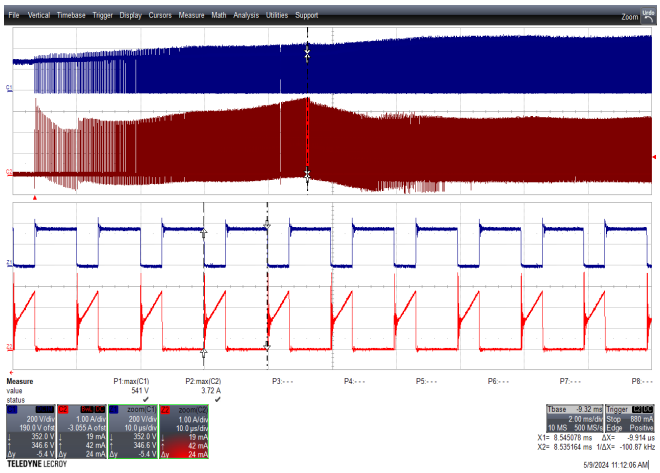


Figure 88 – Primary Drain Voltage and Current
140 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div.,10 µs / div. (Zoom)
V_{DSMAX}: 541 V; I_{DSMAX}: 3.72 A

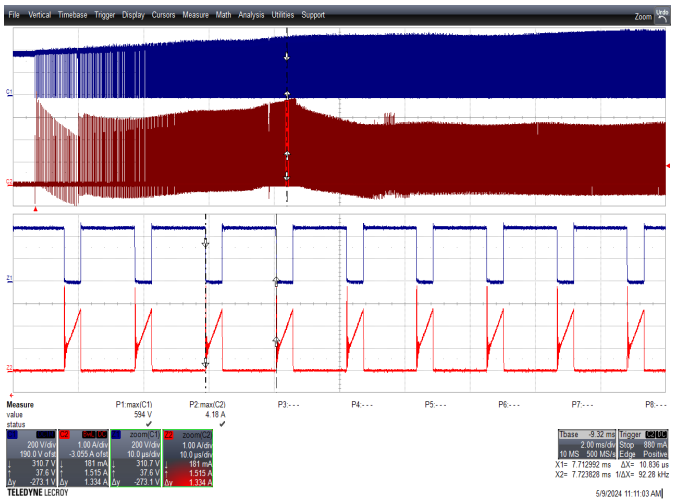


Figure 89 – Primary Drain Voltage and Current
265 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 10 µs / div. (Zoom)
V_{DSMAX}: 594 V; I_{DSMAX}: 4.18 A

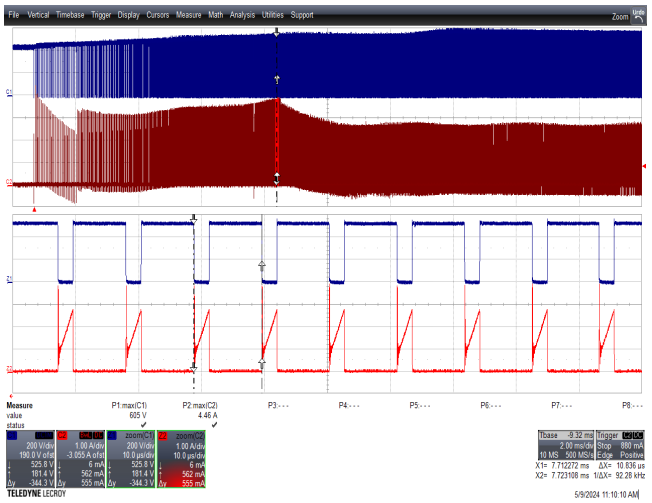


Figure 90 – Primary Drain Voltage and Current
305 VAC, 24 V 4.17 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div.,10 µs / div. (Zoom)
V_{DSMAX}: 605 V; I_{DSMAX}: 4.46 A

12.4.3 Flyback Primary Drain Voltage and Current at Transient Load

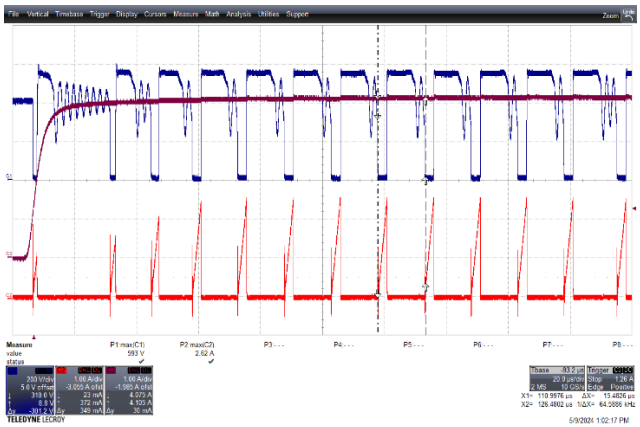


Figure 91 – Primary Drain Voltage and Current
140 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 20 µs / div.
V_{DSMAX}: 594 V; I_{DSMAX}: 2.62 A

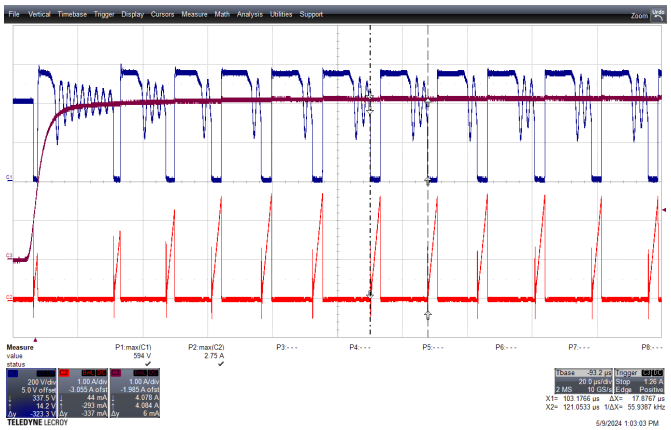


Figure 92 – Primary Drain Voltage and Current
198 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 20 µs / div.
V_{DSMAX}: 594 V; I_{DSMAX}: 2.75 A

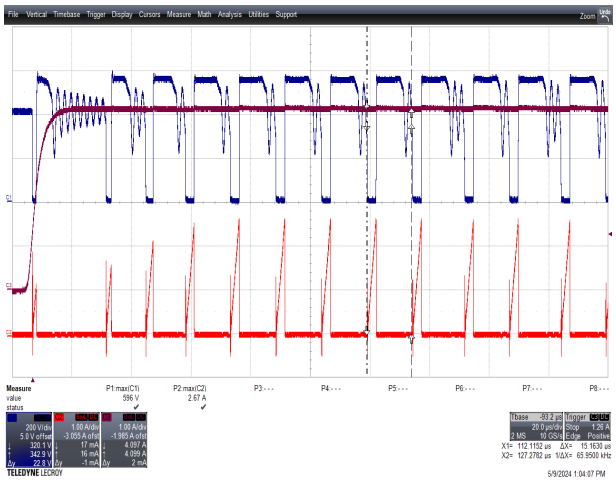


Figure 93 – Primary Drain Voltage and Current
265 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 20 µs / div.
V_{DSMAX}: 596 V; I_{DSMAX}: 2.67 A

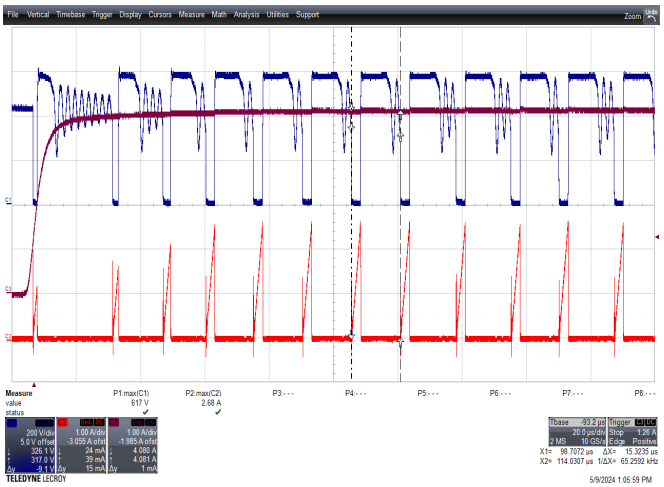


Figure 94 – Primary Drain Voltage and Current
305 VAC, 24 V 4.17 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 20 µs / div.
V_{DSMAX}: 617 V; I_{DSMAX}: 2.68 A

12.4.4 Flyback Primary Drain Voltage and Current During Output Short Circuit

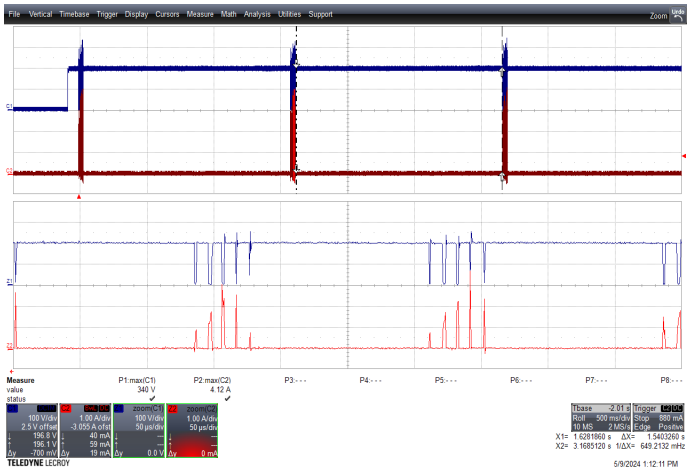


Figure 95 – Primary Drain Voltage and Current
140 VAC, Output Short Circuit
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 1 A / div., 500 ms / div.
V_{DSMAX}: 340 V; I_{DSMAX}: 4.12 A

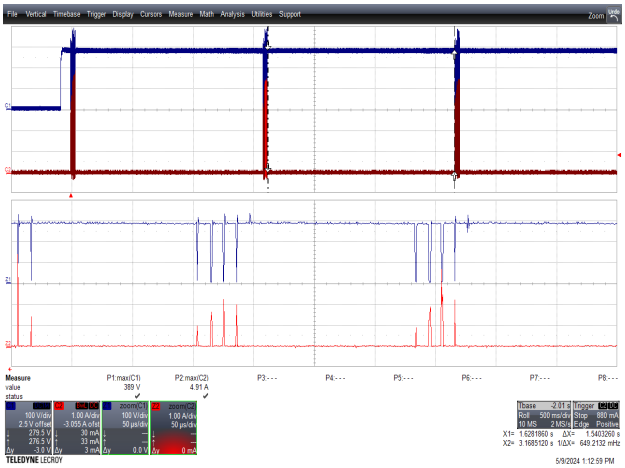


Figure 96 – Primary Drain Voltage and Current
189 VAC, Output Short Circuit
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 1 A / div., 500 ms / div.
V_{DSMAX}: 389 V; I_{DSMAX}: 4.91 A

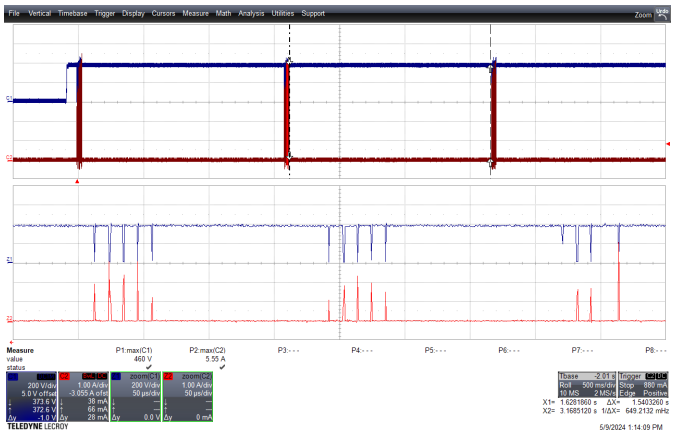


Figure 97 – Primary Drain Voltage and Current
265 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 500 ms / div.
V_{DSMAX}: 460 V; I_{DSMAX}: 5.55 A

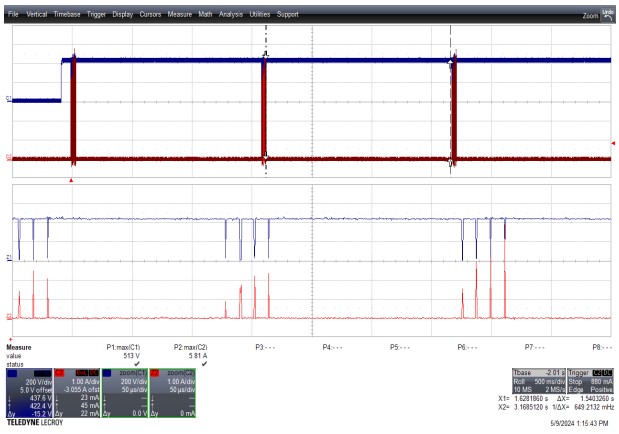


Figure 98 – Primary Drain Voltage and Current
305 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 1 A / div., 500 ms / div.
V_{DSMAX}: 513 V; I_{DSMAX}: 5.81 A

12.5 Flyback SR FET (Q2/Q3) Voltage Waveforms

12.5.1 Flyback SR FET (Q2/Q3) Voltage at Full Load Steady State

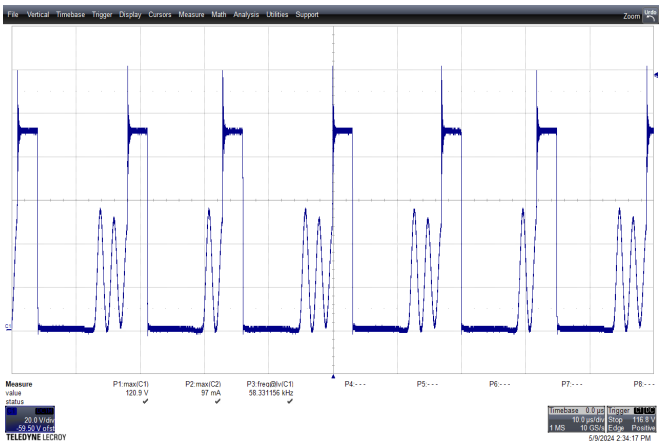


Figure 99 – SR FET Drain Voltage
140 VAC, 24 V 4.17 A Steady-State
Lower: V_{DS}, 20V / div., 10 µs / div.
V_{DSMAX}: 121 V

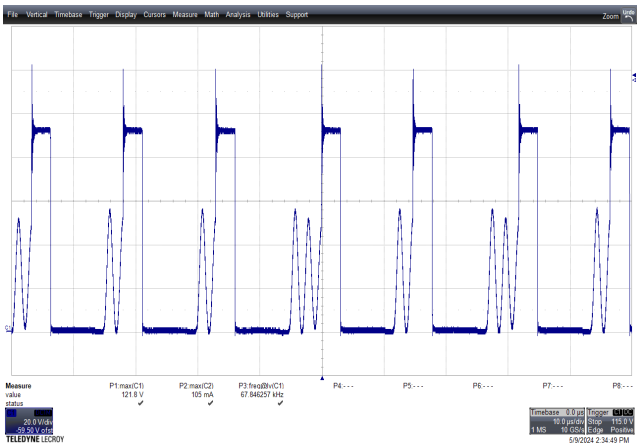


Figure 100 – SR FET Drain Voltage
198 VAC, 24 V 4.17 A Steady-State
Lower: V_{DS}, 20V / div., 10 µs / div.
V_{DSMAX}: 122 V

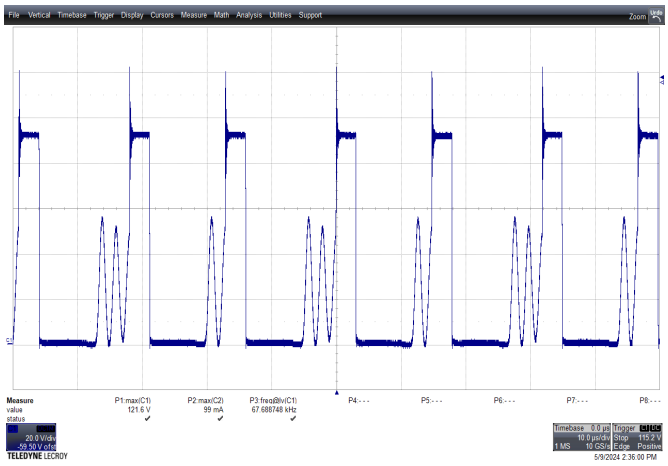


Figure 101 – SR FET Drain Voltage
265 VAC, 24 V 4.17 A Steady-State
Lower: V_{DS}, 20V / div., 10 µs / div.
V_{DSMAX}: 122 V

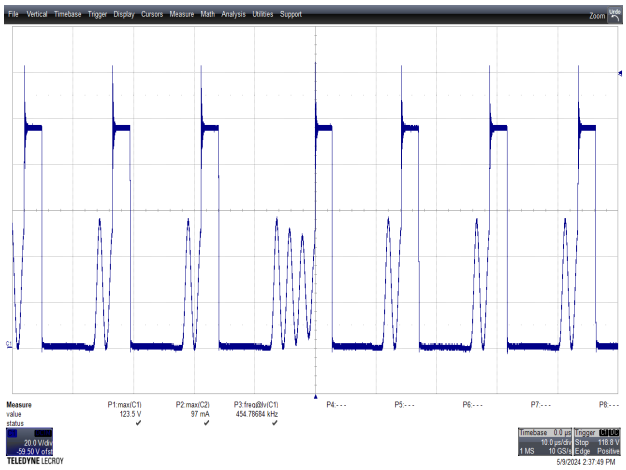


Figure 102 – SR FET Drain Voltage
305 VAC, 24 V 4.17 A Steady-State
Lower: V_{DS}, 20V / div., 10 µs / div.
V_{DSMAX}: 124 V

12.5.2 Flyback SR FET (Q2/Q3) Voltage at Full Load Start-up

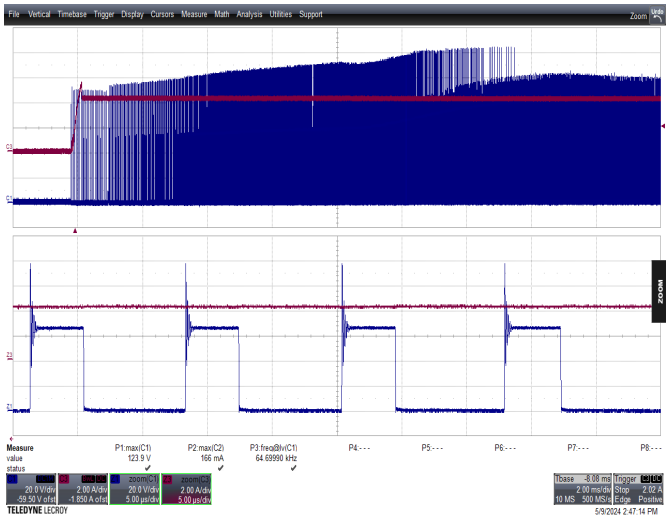


Figure 103 – SR FET Drain Voltage
198 VAC, 24 V 4.17 A Start-up
Upper: I_{OUT}, 2 A / div.
Lower: V_{DS}, 20 V / div., 5 µs / div (Zoom)
V_{DSMAX}: 124 V

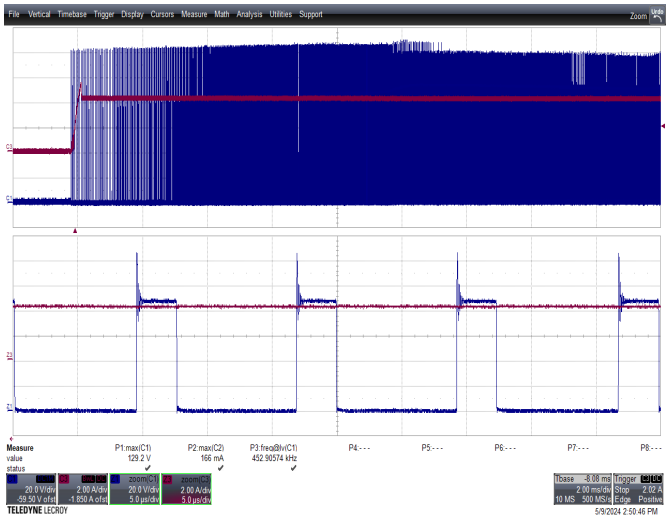


Figure 104 – SR FET Drain Voltage
305 VAC, 24 V 4.17 A Start-up
Upper: I_{OUT}, 2 A / div.
Lower: V_{DS}, 20 V / div., 5 µs / div (Zoom)
V_{DSMAX}: 129 V

12.5.3 Flyback SR FET (Q2/Q3) Voltage at Transient Load

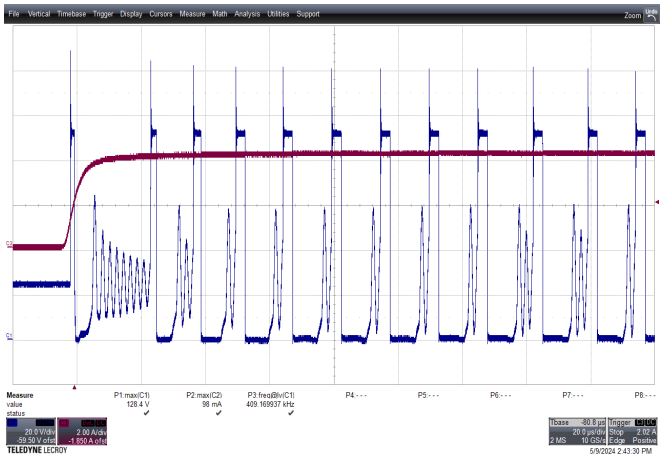


Figure 105 – SR FET Drain Voltage
198 VAC, 24 V 0 A - 4.17 A Step Load
Upper: I_{OUT}, 2 A / div., 20 µs / div.
Lower: V_{DS}, 20V / div.
V_{DSMAX}: 128 V

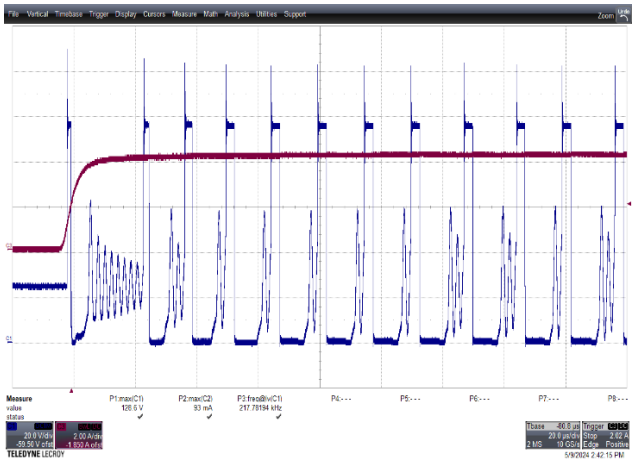


Figure 106 – SR FET Drain Voltage
305 VAC, 24 V 0 A - 4.17 A Step Load
Upper: I_{OUT}, 2 A / div., 200 µs / div.
Lower: V_{DS}, 50V / div.
V_{DSMAX}: 129 V

12.6 Load Transient Response

Output voltage was measured at the PSU output terminals T3 and T4.

12.6.1 0% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0 A – 4.17 A with 50% duty cycle and load current slew rate of 800 mA/µs.

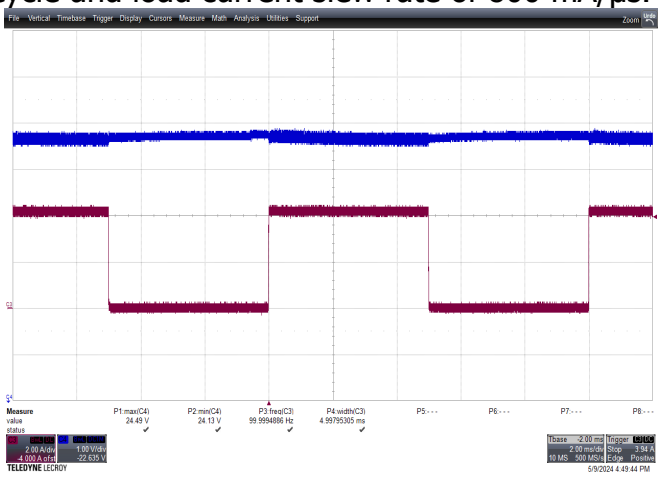


Figure 107 – 0-100% Dynamic Load
198 VAC, 24 V 0 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.5 V, V_{OMIN}: 24.1 V

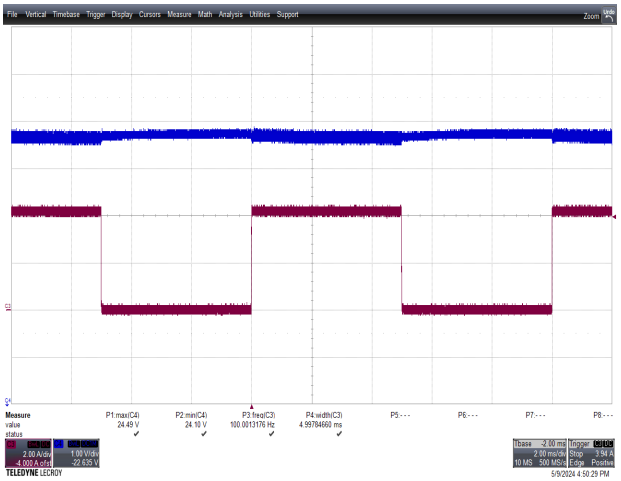


Figure 108 – 0-100% Dynamic Load
305 VAC, 24 V 0 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.5 V, V_{OMIN}: 24.1 V

12.6.2 10% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0.42 A – 4.17 A with 50% duty cycle and load current slew rate of 800 mA/µs.

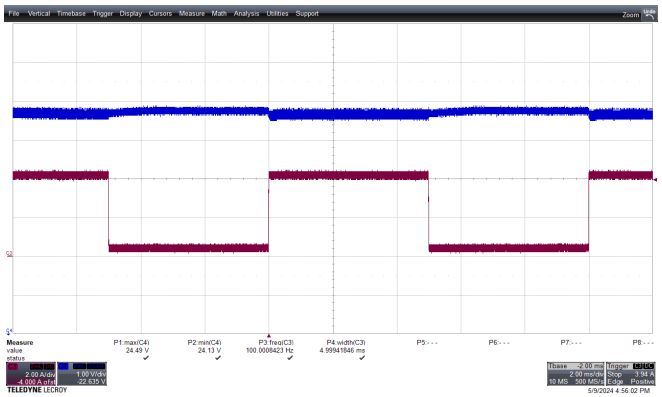


Figure 109 –10-100% Dynamic Load
198 VAC, 24 V 0.42 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.5 V, V_{OMIN}: 24.1 V

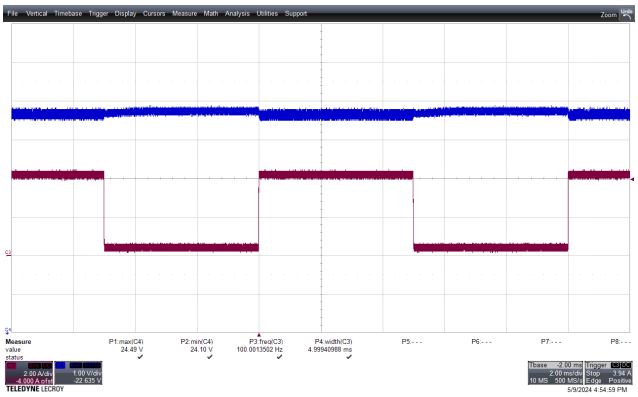


Figure 110 – 10-100% Dynamic Load
305 VAC, 24 V 0.42 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.5 V, V_{OMIN}: 24.1 V

12.6.3 50% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 2.08 A – 4.17 A with 50% duty cycle and load current slew rate of 800 mA/µs.

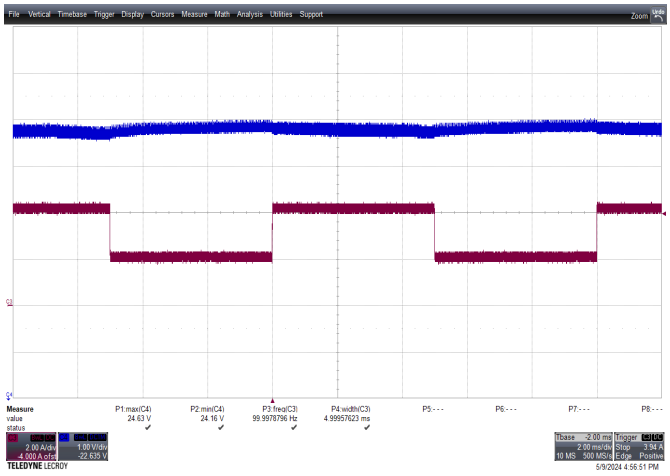


Figure 111 – 50-100% Dynamic Load
198 VAC, 24 V 2.08 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.6 V, V_{OMIN}: 24.2 V

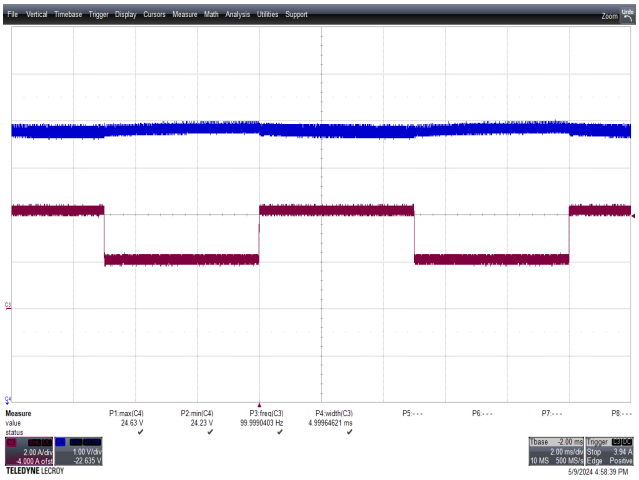


Figure 112 – 50-100% Dynamic Load
305 VAC, 24 V 2.08 A - 4.17 A Transient
Upper: V_{OUT}, 1 V / div., 2 ms / div.
Lower: I_{OUT}, 2 A / div.
V_{OMAX}: 24.6 V, V_{OMIN}: 24.2 V

12.7 Input Line AC On/Off Cycling Test

Set up: 1 s AC on, 1 s AC off

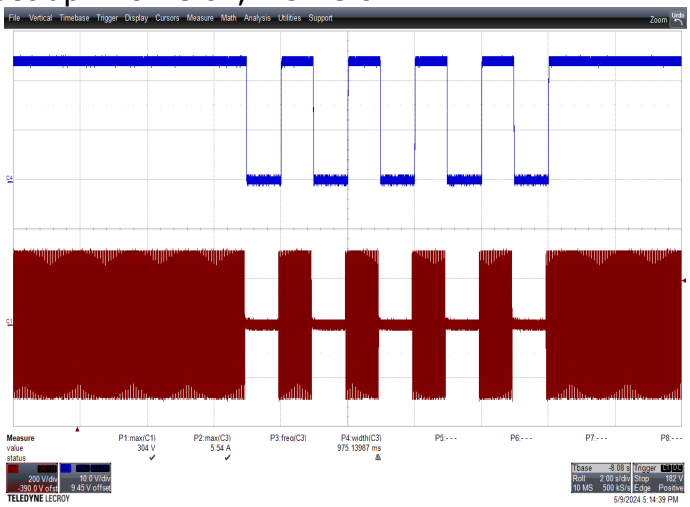


Figure 113 – AC On/Off Cycling
198 VAC, 24 V 4.17 A, AC On/Off
Upper: V_{OUT}, 10 V / div., 2 s / div.
Lower: V_{IN}, 200 V / div.
Remarks: No auto-restart

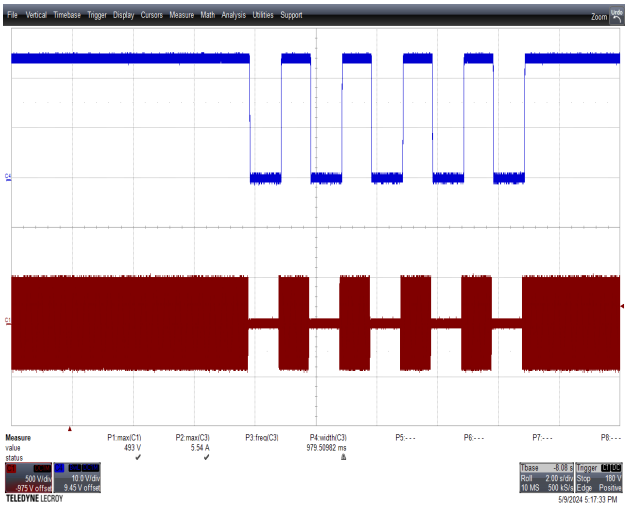


Figure 114 – Dynamic Load
305 VAC, 24 V 4.17 A, AC On/Off
Upper: V_{OUT}, 10 V / div., 2 s / div.
Lower: V_{IN}, 500 V / div.
Remarks: No auto-restart

12.8 Output Ripple Voltage Waveforms

12.8.1 Ripple Measurement Technique

To conduct output ripple measurements, a modified oscilloscope test probe must be used to reduce spurious signals caused by noise pickup.

The 4987BA probe adapter is equipped with two capacitors connected in parallel across the probe tip. These capacitors consist of one (1) 0.1 µF/50 V ceramic type and one (1) 10 µF/50 V aluminum electrolytic type. Since the aluminum electrolytic capacitor is polarized, proper polarity must be maintained across DC outputs (refer to the diagram below).

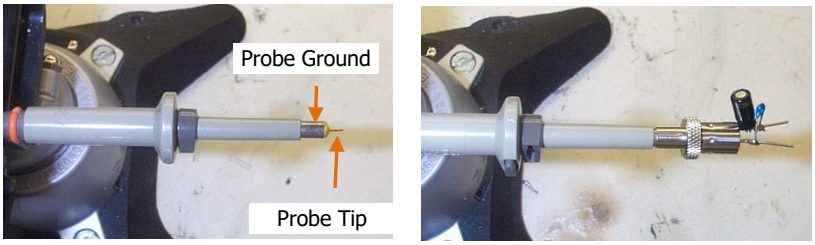


Figure 115 – Ripple voltage probe using Probe Master 4987A BNC Adapter

12.8.2 Output Ripple Voltage at 100% Load

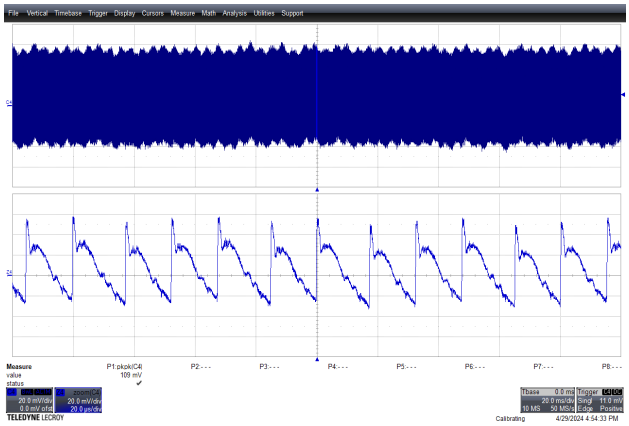


Figure 116 – Output Ripple Voltage
198 VAC, 24 V 4.17 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 109 mVp-p

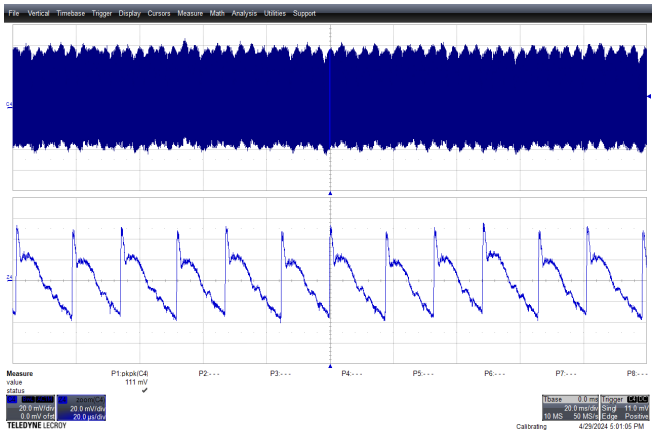


Figure 117 – Output Ripple Voltage
230 VAC, 24 V 4.17 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 111 mVp-p

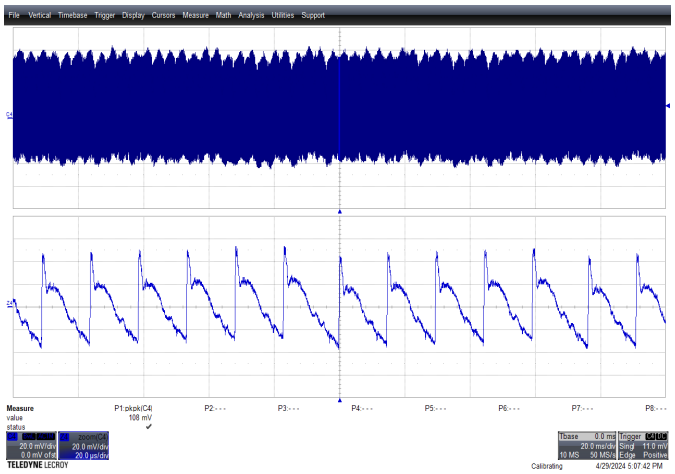


Figure 118 – Output Ripple Voltage
265 VAC, 24 V 4.17 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 108 mVp-p

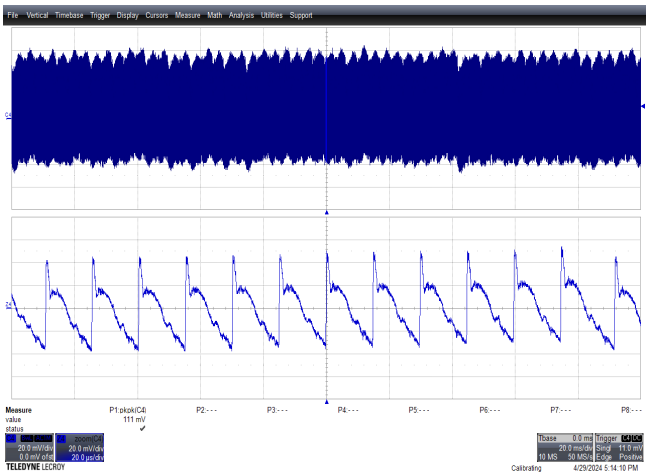


Figure 119 – SR FET Drain Voltage
277 VAC, 24 V 4.17 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 111 mVp-p

12.8.3 Output Ripple Voltage at 50% Load

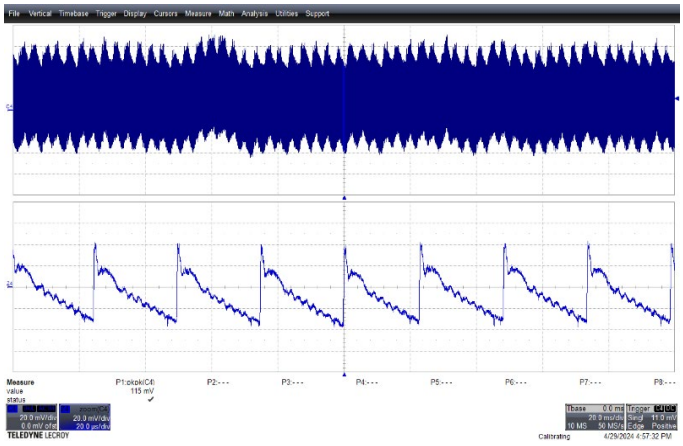


Figure 120 – Output Ripple Voltage
198 VAC, 24 V 2.08 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 115 mVp-p

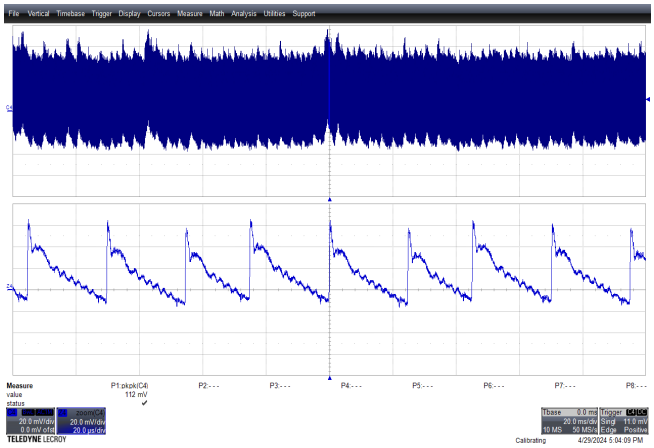


Figure 121 – Output Ripple Voltage
230 VAC, 24 V 2.08 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 112 mVp-p

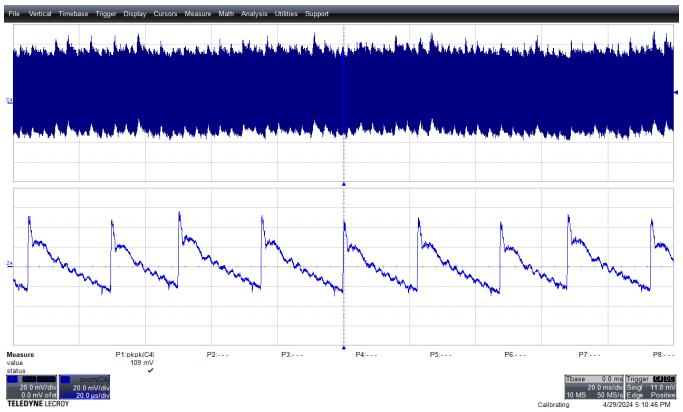


Figure 122 – Output Ripple Voltage
265 VAC, 24 V 2.08 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 109 mVp-p

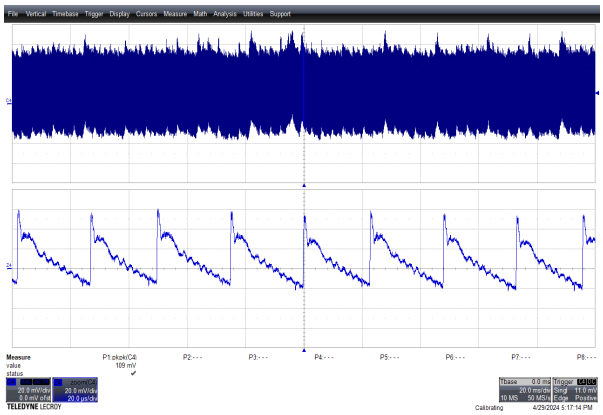


Figure 123 – SR FET Drain Voltage
277 VAC, 24 V 2.08 A Steady-State
V_{RIPPLE}, 20 mV / div., 20 µs / div. (Zoom)
V_{RIPPLE}: 109 mVp-p

13 Constant Voltage PWM Dimming

Dimming is achieved by varying the duty cycle of the output current. The dimming performance is demonstrated using a constant voltage DALI dimmer, ranging from 0.1% to 100% PWM duty cycle.

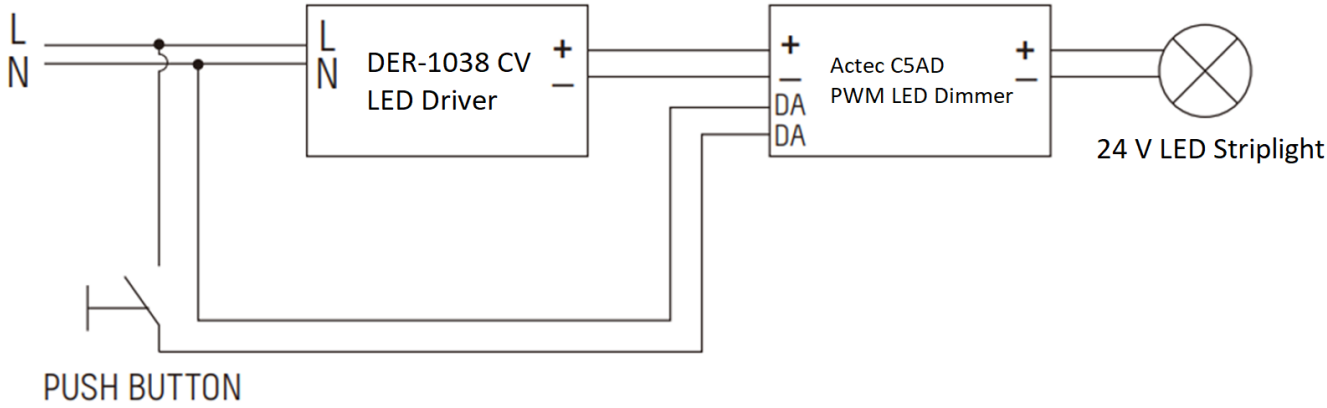


Figure 124 – PWM LED Dimming Test Set-up

13.1 PWM Dimming Waveforms

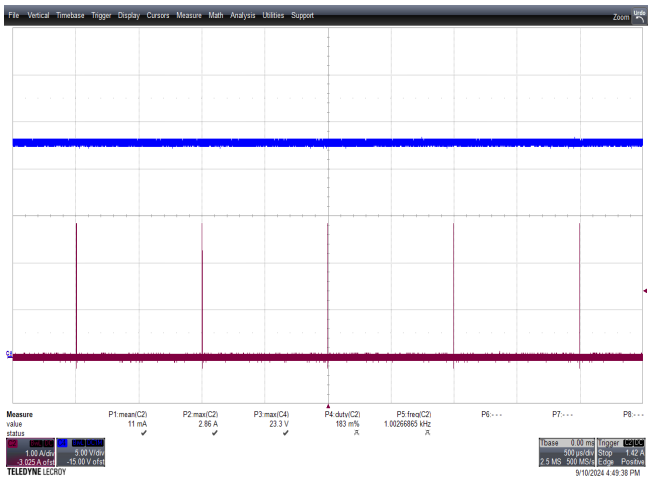


Figure 125 – PWM Dimming Waveform
230 VAC, 24 V LED 0.18 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 11 mA, V_{LED} = 23.3 V

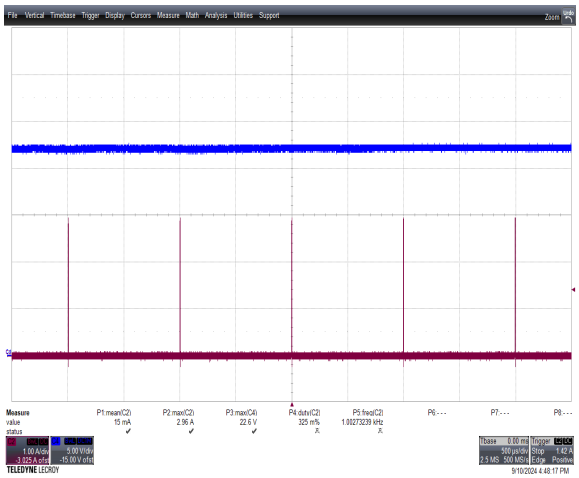


Figure 126 – PWM Dimming Waveform
230 VAC, 24 V LED 0.33 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 15 mA, V_{LED} = 22.6 V

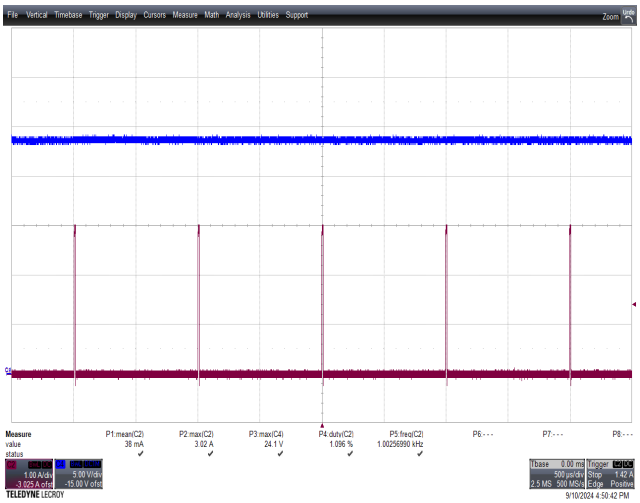


Figure 127 – PWM Dimming Waveform
230 VAC, 24 V LED 1.1 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 36 mA, V_{LED} = 24.1 V

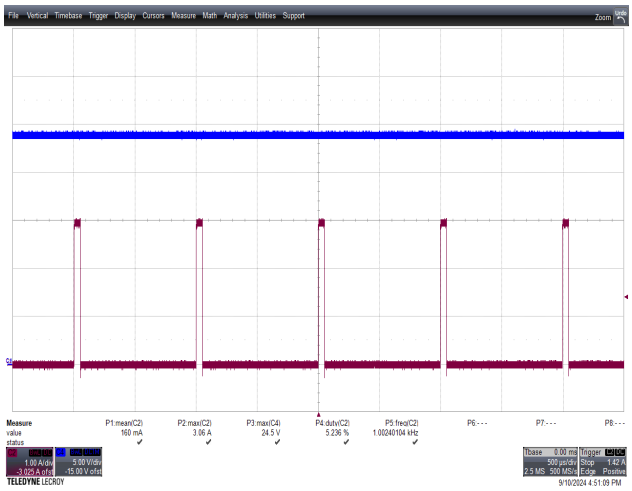


Figure 128 – PWM Dimming Waveform
230 VAC, 24 V LED 5.2 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 160 mA, V_{LED} = 24.5 V

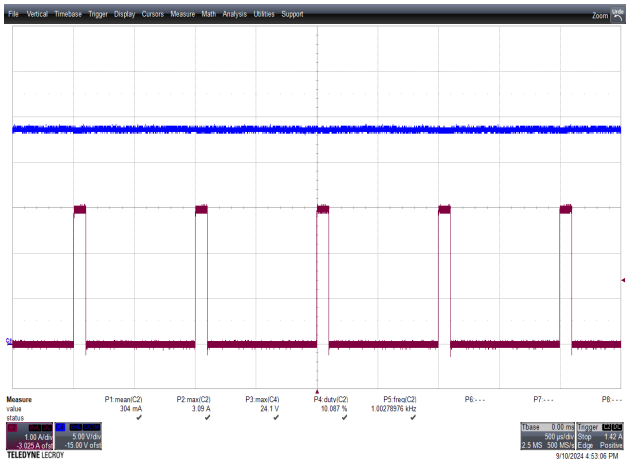


Figure 129 – PWM Dimming Waveform
230 VAC, 24 V LED 10 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 304 mA, V_{LED} = 24 V

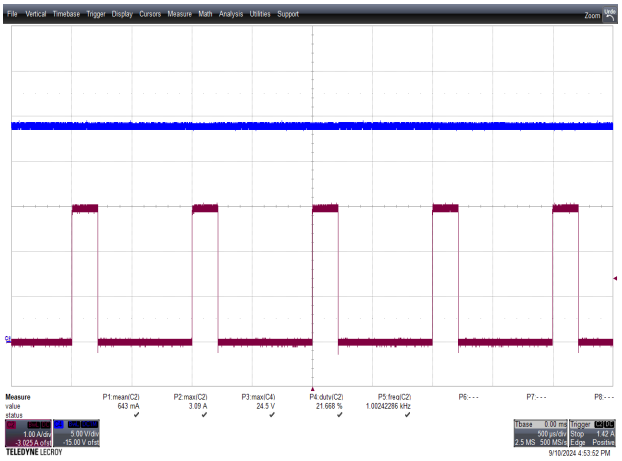


Figure 130 – PWM Dimming Waveform
230 VAC, 24 V LED 22 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 643 mA, V_{LED} = 24.5 V

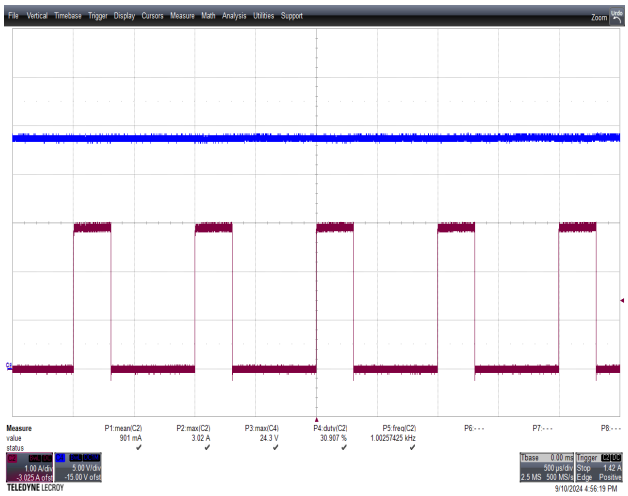


Figure 131 – PWM Dimming Waveform
230 VAC, 24 V LED 30 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 901 mA, V_{LED} = 24.3 V

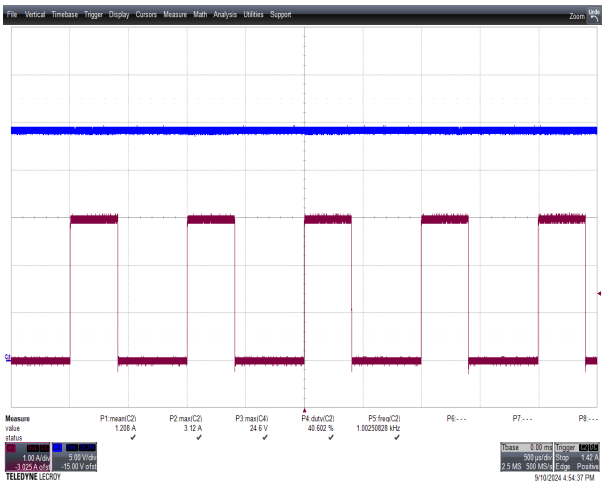


Figure 132 – PWM Dimming Waveform
230 VAC, 24 V LED 40 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 1.21 A, V_{LED} = 24.6 V

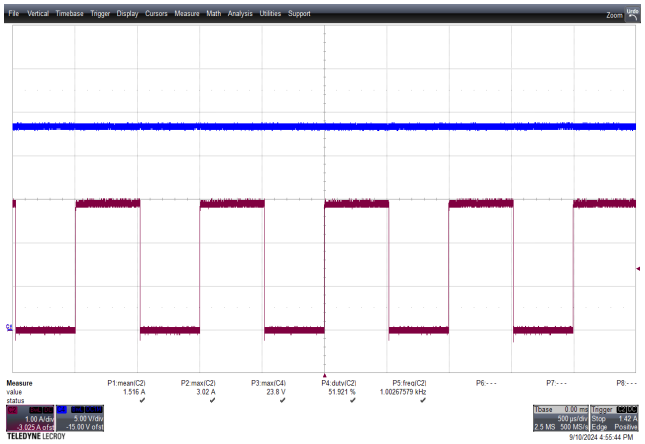


Figure 133 – PWM Dimming Waveform
230 VAC, 24 V LED 52 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 1.52 A, V_{LED} = 23.8 V

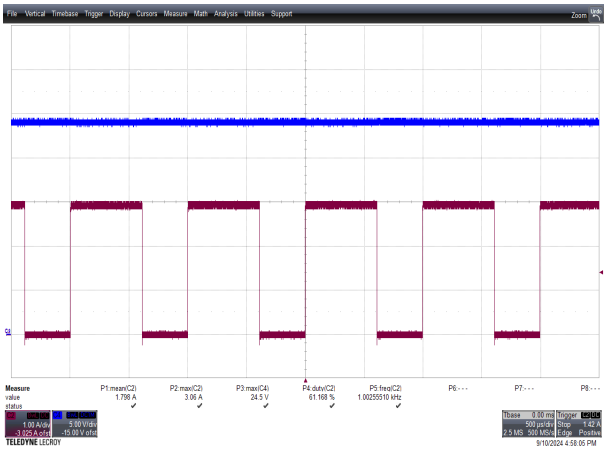


Figure 134 – PWM Dimming Waveform
230 VAC, 24 V LED 61 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 1.80 A, V_{LED} = 24.5 V

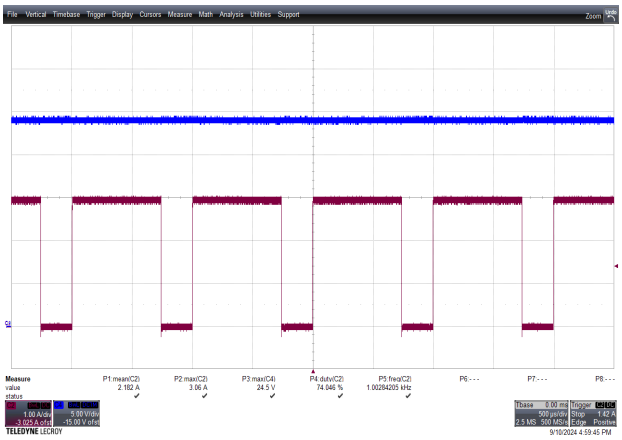


Figure 135 – PWM Dimming Waveform
230 VAC, 24 V LED 74 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 2.18 A, V_{LED} = 24.5 V

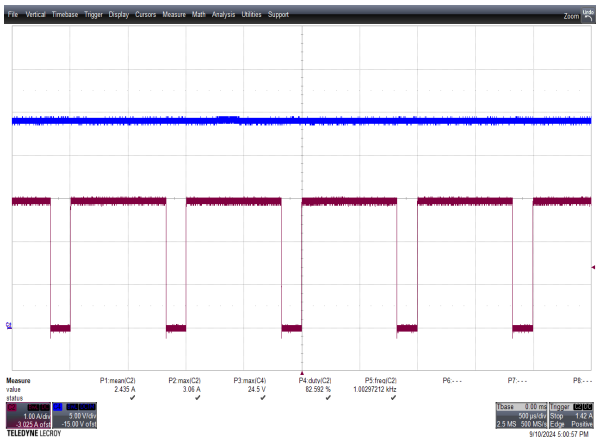


Figure 136 – PWM Dimming Waveform
230 VAC, 24 V LED 82.5 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 2.44 A, V_{LED} = 24.5 V

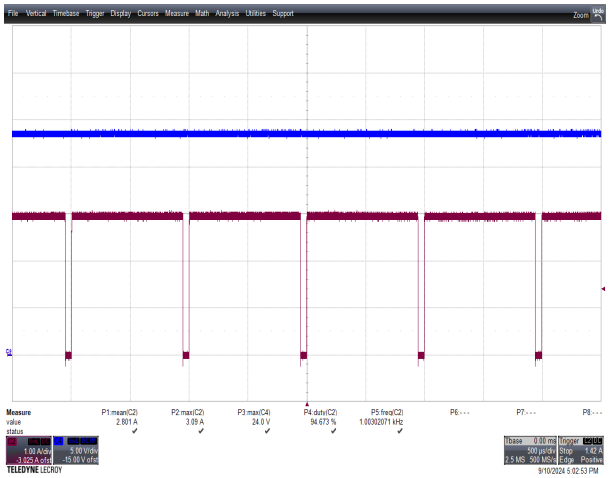


Figure 137 – PWM Dimming Waveform
230 VAC, 24 V LED 94.7 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 2.80 A, V_{LED} = 24 V

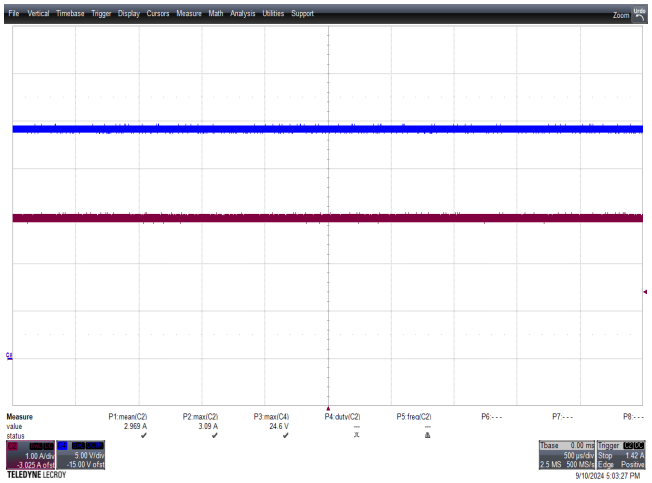


Figure 138 – PWM Dimming Waveform
230 VAC, 24 V LED 100 % Duty Cycle
V_{LED}: 5 V / div., 500 µs / div.
I_{OUT}: 1 A / div.
$I_{O(MEAN)}$ = 2.97 A, V_{LED} = 24.6 V

14 Conducted EMI

EMI scans were performed using 4.44 Ω fixed resistor load.

14.1 Test Set-up

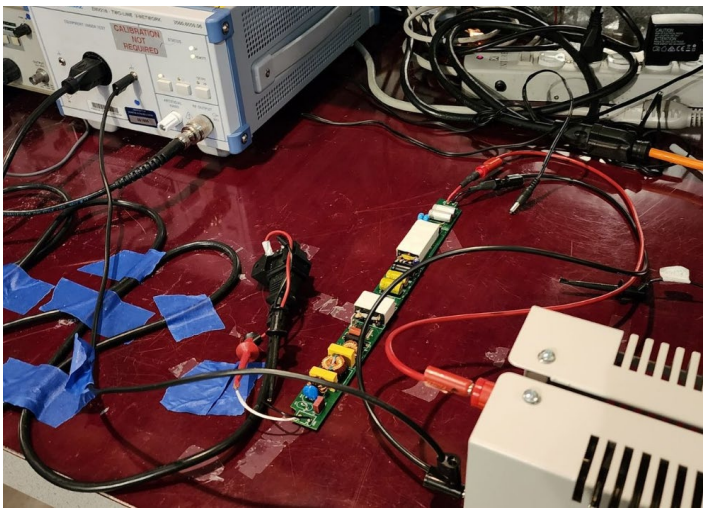


Figure 139 – Conducted EMI Test Set-up

14.2 Floating Output-Load Resistor

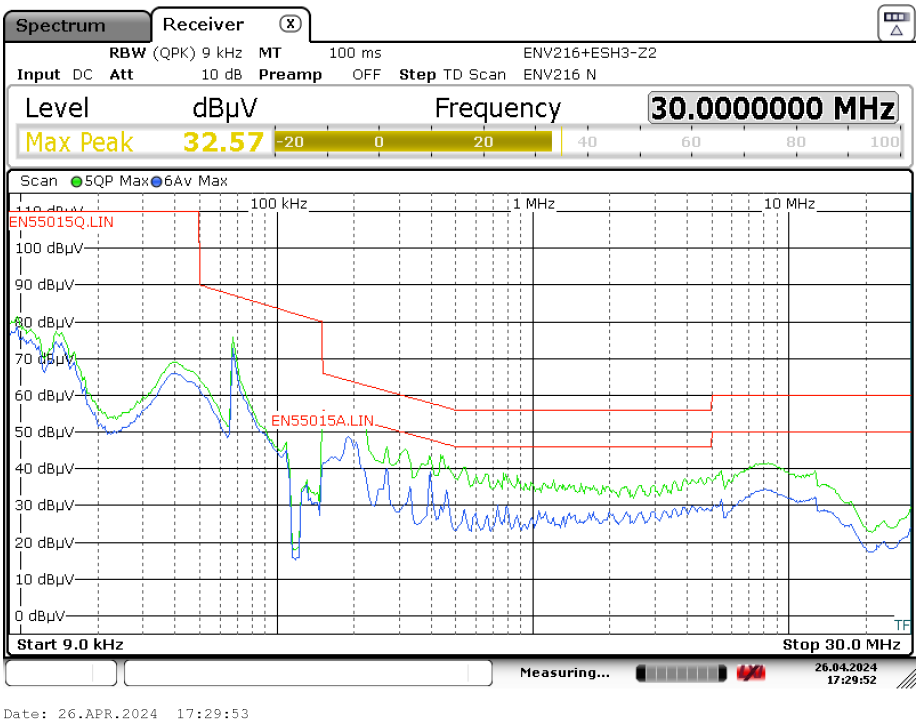


Figure 140 – Conducted EMI at 24 V 4.17 A (5.76 Ω-Floating), 230 VAC

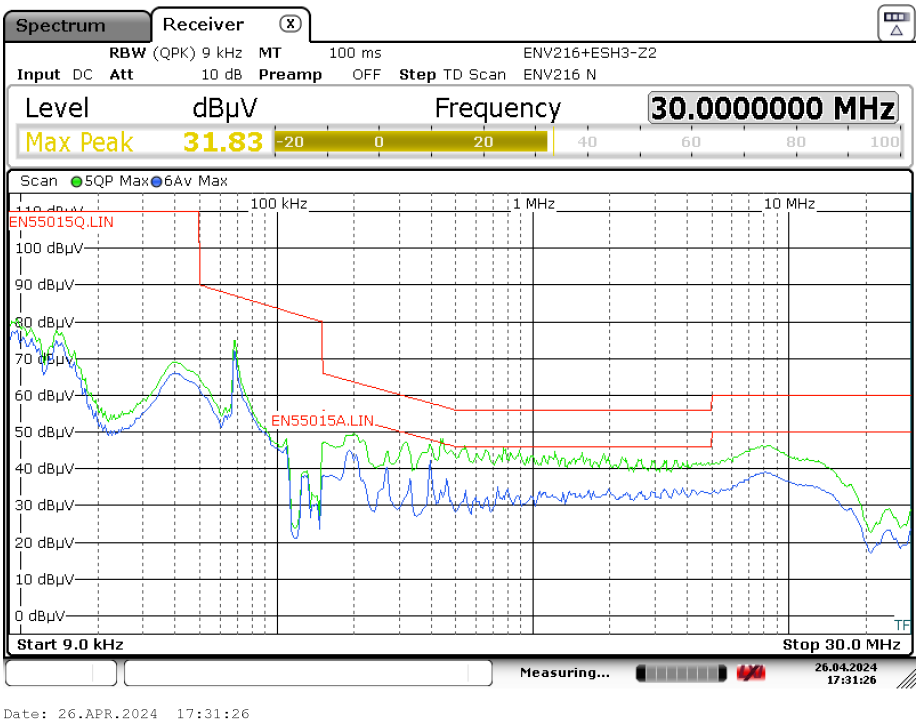


Figure 141 – Conducted EMI at 24 V 4.17 A (5.76 Ω-Grounded), 230 VAC

15 Line Surge

ESD was tested at 24 V output. Pass criterion: no permanent interruption of output.

15.1 Combination Wave Differential Mode Test

Pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2.5	90	2	10	PASS
230	-2.5	90	2	10	PASS
230	+2.5	270	2	10	PASS
230	-2.5	270	2	10	PASS
230	+2.5	0	2	10	PASS
230	-2.5	0	2	10	PASS

Table 14 – Combination Wave Differential Mode Test Data

15.2 Ring Wave Surge

ESD was tested at 24 V output. Pass criterion: no permanent interruption of output.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS

Table 15 – Ring Wave Surge Test Data

16 Electrostatic Discharge Test (ESD)

ESD testing was conducted at 24 V output. Pass criterion: no permanent interruption of output.

16.1 Air Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
115	+8	Output +	10	PASS
115	-8	Output +	10	PASS
115	+10	Output -	10	PASS
115	-10	Output -	10	PASS
115	+12	Output -	10	PASS
115	-12	Output -	10	PASS
115	+15	Output +	10	PASS
115	-15	Output +	10	PASS
115	+16.5	Output -	10	PASS
115	-16.5	Output -	10	PASS

Table 16 – Electrostatic Discharge Test Data

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Sep-24	MGM	A	Initial Release.	Apps & Mktg
28-Apr-26	SF	B	Update INN4277C-H182 to INN4276C-H182 in Bill of Materials line 62, page 15	Apps & Mktg

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