Design Example Report

Title	**130 W Isolated Flyback Power Supply with 197 W Peak Power using InnoSwitch™4 – QR, INN4277C – H181**
Specification	Input: 90 VAC – 132 VAC / 185 V – 265 VAC Nominal Output: 24 V / 5.4 A Peak Output: 24 V / 8.2 A
Application	Printer Applications
Author	Applications Engineering Department
Document Number	DER-1033
Date	September 16, 2025
Revision	B

Summary and Features

- 130 W continuous output power
- 197 W peak power capability for 100 ms duration
- No Heatsink up to 55 °C Operating Ambient
- >94 % Full Load Efficiency at 115 VAC and 230 VAC
- >375 mW Standby Input Power at 120 VAC, 7.5 V Output with 300 mW Load
- >100 mW Standby Input Power at 120 VAC, 7.5 V Output with 40 mW Load
- PowiGaN™ -based InnoSwitch4-QR benefits
    - Highly integrated switcher IC with integrated high-voltage switch, synchronous rectification and FluxLink™ feedback
    - GAN-based Integrated MOSFET enables heat sink-less design
    - Fast instantaneous transient response with 0%-100%-0% load step
    - Quasi-Resonant (QR) operation for high efficiency
    - Robust 750 V PowiGaN™ primary switch
    - Steady state switching frequency up to 155 kHz enables peak power delivery with reduced transformer size
    - Low components count (62 pcs)

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- Easily meets DOE6 and CoC Tier 2 efficiency requirements
- Integrated protection and reliability features
    - Open SR FET-gate detection
    - Fast input line UV/OV protection
    - Output overvoltage and undervoltage protection
    - Output over-current protection
    - Over-temperature protection (OTP)

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Table of Contents

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a low standby power 130 W isolated flyback power supply that can deliver up to 197 W peak power, utilizing the InnoSwitch4-QR flyback controller. The power supply can deliver a continuous output of 24 V / 5.4 A and has a short-term peak output of 24 V / 8.2 A within the low-line input range of 90 VAC – 132 VAC.

The InnoSwitch4-QR combines a high-voltage PowiGaN switch with both primary-side and secondary-side controllers in a single device. It can operate at a switching frequency of up to 155 kHz, making it suitable for applications with short-term peak power requirements without the need for a large flyback transformer.

The power supply is optimized for high efficiency and low standby power. It can operate up to 55°C ambient without the need for a metal heatsink.

For high-line applications, the DER-1033 can be easily modified to operate within a high input line range of 185 VAC – 265 VAC. The configuration and performance for high-line application are in the appendix section.

This document contains the power supply specification, schematic, bill of materials (BOM), transformer documentation, printed circuit layout, and performance data.

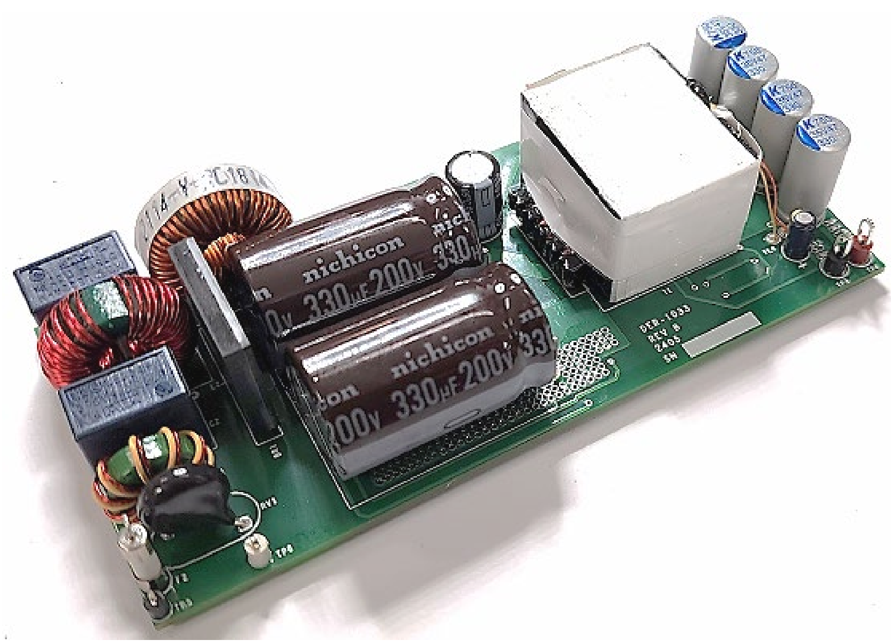


Figure 1 – Populated Circuit Board Photograph

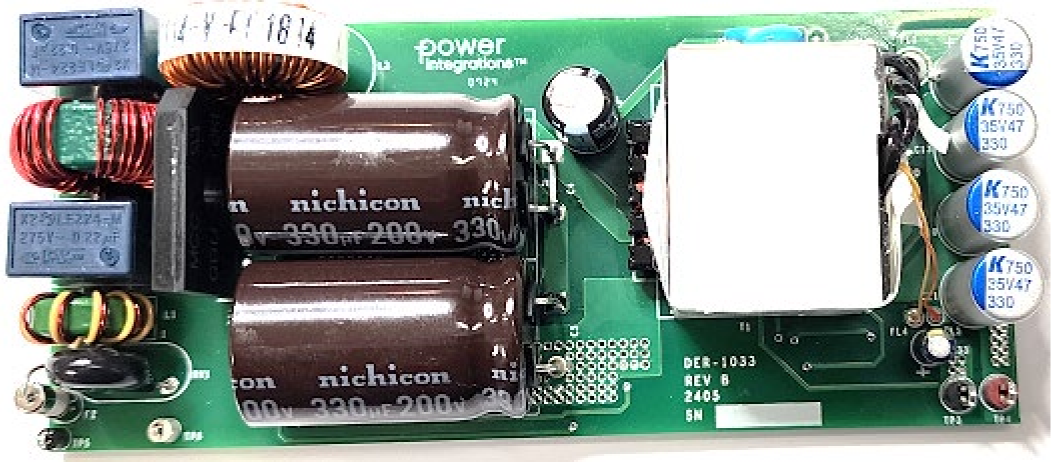


Figure 2 – Populated Circuit Board Photograph, Top Side

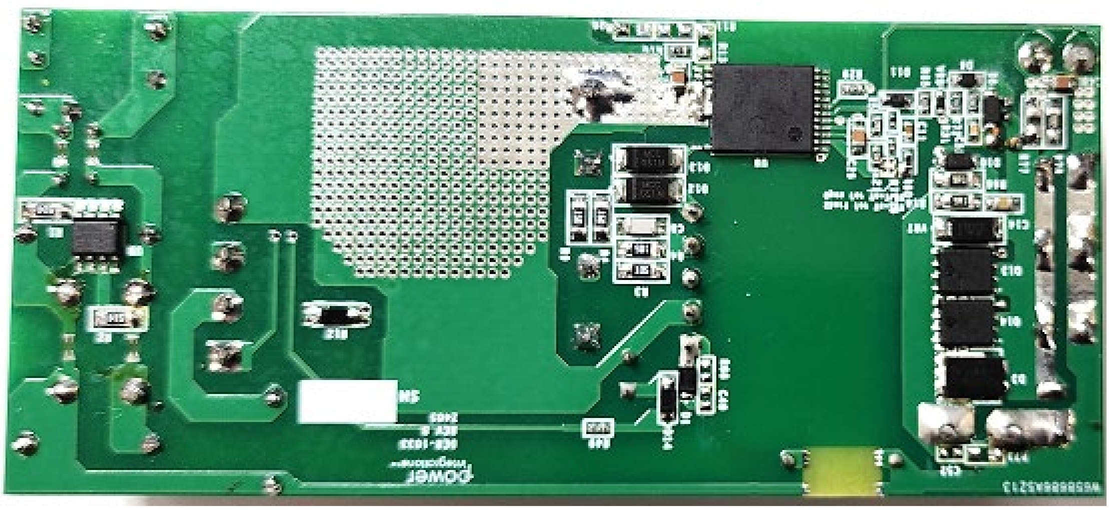


Figure 3 – Populated Circuit Board Photograph, Bottom Side

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						2 Wire – no P.E.
Voltage	V_{IN}	90		132	VAC	For 185 V - 265 V input requirements, please
Frequency	f_{LINE}		50/60		Hz	see the configuration in the appendix
7.5 V Standby Mode Output						
Output Voltage	V_{OUT}		7.5		V	±3%
Standby Input Power (40mW Load)	$P_{S(40mW)}$			100	mW	Measured at 120 VAC, 7.5V 40 mW Load
Standby Input Power (300mW Load)	$P_{S(300mW)}$			375	mW	Measured at 120 VAC, 7.5V 300 mW Load
No Load Input Power	$P_{no\text{-}Load}$			30	W	Measured at 120 VAC, 7.5V No Load
24 V Nominal Output						
Output Voltage	V_{OUT}		24		V	±3%
Output Voltage Ripple	V_{RIPPLE}			200	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	I_{OUT}			5.4	A	±3%
Full Load Efficiency	η		93		%	115 VAC, Vout is measured on the Board.
Continuous Output Power	$P_{OUT(28\ V)}$			130	W	
Peak Power	$P_{OMAX(28\ V)}$			197	W	100 ms Time Duration
Conducted EMI		Meets CISPR22B / EN55022B				Floating or Grounded Load
Operating Ambient Temperature	T_{AMB}	0		55	ºC	Free Convection, Sea Level.
Immunity	**Combination Wave**			2.5kV		Differential Mode
	Ring Wave			4kV		Differential Mode
	ESD			15kV		No damage Component

3 Schematic Diagram

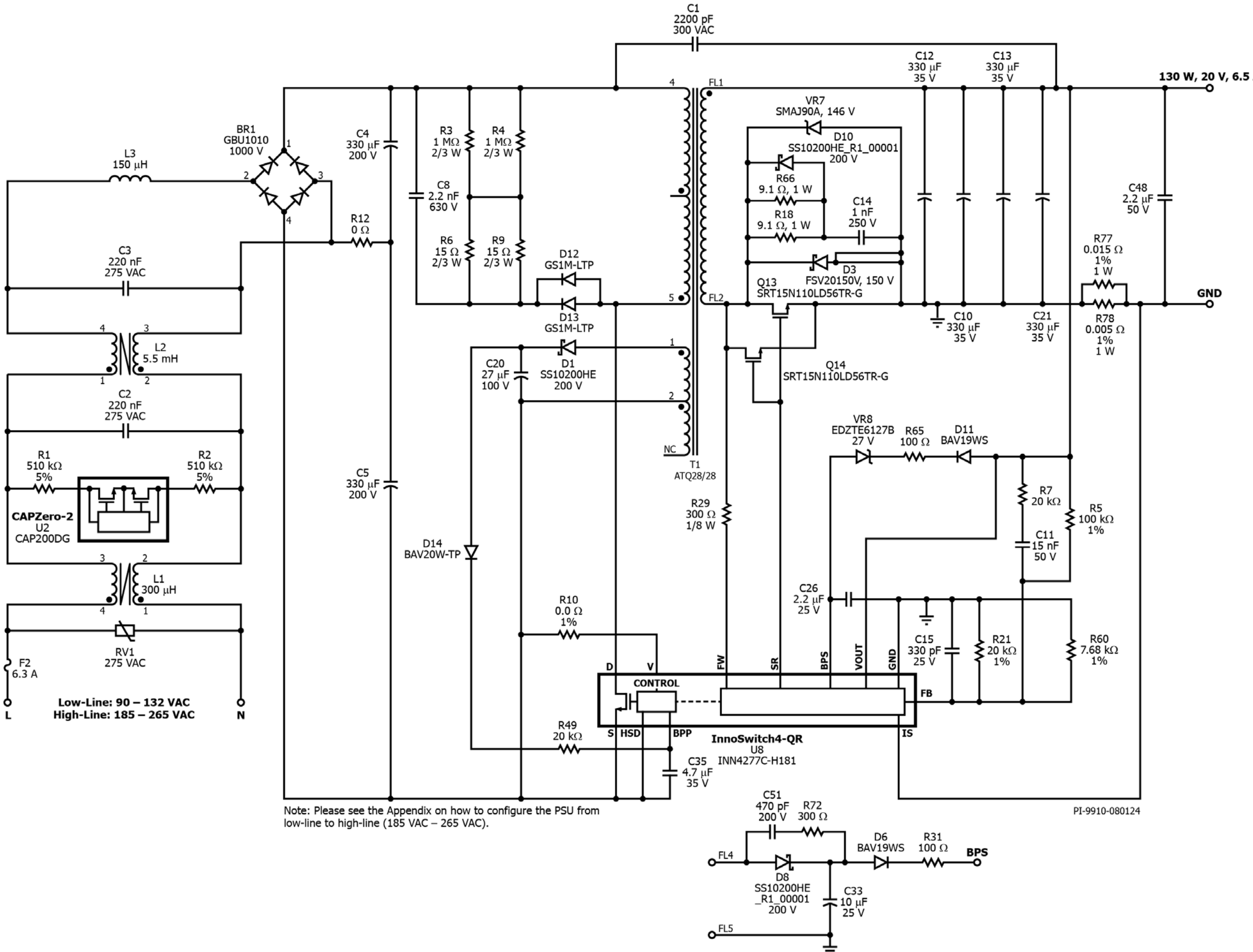


Figure 4 – Schematic Diagram.

4 Circuit Description

4.1 Input Rectification and EMI Filtering

Fuse F1 isolates the PSU circuitry and provides protection from component failure. RV1 protects the circuit from high voltage differential surge. The common mode chokes L1 and L2, along with the differential choke L3 and X-capacitors C2 and C3, attenuate common-mode and differential-mode noise generated by the PSU switching action. The bridge rectifier BR1, jumper resistor R12, and capacitors C4 and C5 form a voltage doubler rectifier circuit. Doubling the DC input bulk voltage significantly reduces the RMS power dissipation on the InnoSwitch4-QR primary switch and the flyback transformer, eliminating the need for a metal heatsink at high ambient temperatures. It is recommended to use low DCR inductors for L1, L2, and L3 due to the high charging peak current generated by the voltage doubler, which results in high RMS current.

To satisfy the safety extra low voltage (SELV) when the AC supply is disconnected, the CAP200DG (U9) automatically discharges the X capacitors C2 and C3 to the SELV level by connecting discharge resistors R1 and R2. When AC voltage is applied, the CAP200DG (U9) blocks current flow in the X capacitor safety discharge resistors R1 and R2, reducing power loss to almost zero mW. The inclusion of CAP200DG (U9) in this design is necessary to achieve low input standby power.

4.2 InnoSwitch4-QR Primary

This power supply is an isolated flyback converter. One end of the primary winding of transformer (T1) is connected to the rectified DC bus, while the other end is connected to the drain terminal of the switch inside the InnoSwitch4-QR IC (U8). The V pin of the IC (U1) is grounded to reduce power dissipation under light load conditions, as required for printer applications.

Diodes D12 and D13, resistors R6, R9, R3, and R4, along with capacitor C8, form a primary clamp circuit that reduces the leakage voltage spike across the primary switch inside the InnoSwitch4-QR (U8) during turn-off.

The flyback controller/switch IC U8 is self-starting, using an internal high-voltage current source to charge the capacitor (C35) connected to the BPP pin when HVDC is first applied. During normal operation, the primary-side block is powered from the primary auxiliary winding (Bias) of transformer T1. The auxiliary or bias supply is designed to meet the standby power requirement at a 7.5V output and needs to provide enough bias at full load with a 24V output. The auxiliary supply voltage is rectified by diode D1 and filtered by ceramic capacitor C20. It is recommended to use a Schottky diode to increase the bias voltage swing from 24 V to a 7.5 V output. Schottky diode rectifies the peak leakage spike at full load, generating higher bias voltage. Diode D14 is added to slightly decrease the bias voltage during standby mode (V_{OUT} = 7.5 V), providing very low supply current to U8. The supply current to the U8 BP pin must be less than 1 mA during standby mode operation to reduce standby input power. During full-load operation at 24 V, the supply current to the U8 BP pin must be greater than 3 mA to increase efficiency. Bias supply current limiting resistor R49 must be optimized to efficiently deliver bias current to U8 at full load and standby load.

Output regulation is achieved through cycle-by-cycle frequency and ILIM adjustment based on the output load. At high output load, the switching cycles and ILIM are higher, while at low output load or no-load, they are lower. The value of the PRIMARY BYPASS pin capacitor (C35) programs the IC ILIM setting, whether it is standard or increased. Once a cycle is enabled, the switch will remain on until the primary current ramps to the device current limit for the specific operating state. Due to peak power requirements, the ILimit setting needs to be increased with C35 = 4.7 uF.

4.3 InnoSwitch4-QR Secondary

The secondary side block of the InnoSwitch4-QR controller IC is powered by a 4.5 V (VBPS) internal regulator, which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor C26 and is internally fed from the internal voltage regulator. To minimize the power dissipation of the internal linear regulator, an auxiliary bias supply for the BPS is added. This is formed by D8, C33, D6, and R31. Additionally, an RC snubber (C51 and R72) is connected across D8 to reduce radiated EMI.

The secondary side of the InnoSwitch4-QR IC provides output voltage, output current sensing, and drive to a MOSFET for synchronous rectification. The transformer secondary is rectified by SRFETs Q13 and Q14 and filtered by capacitors C10, C12, C13, and C21.
To reduce high-frequency voltage ringing during the SRFET turn-off state, which would create radiated EMI and/or exceed the PIV ratings of Q13 and Q14, RC snubber components C14, R18, and R66 are employed. A Schottky rectifier diode, D10, is added to increase the efficiency of the output rectifier, improving component thermal performance without the need for a metal heatsink. At peak transient loads, the converter operates in continuous conduction mode (CCM), generating high leakage spikes across the SRFET. The TVS diode VR7 is necessary to reduce voltage stress across the SRFET during peak power and very fast transient loads.

The FORWARD pin connects to the negative edge detection block, which is used for both handshaking and timing to turn on the 2 SR FETs Q13 and Q14 connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The voltage sensed by resistor R29 on the FORWARD pin is used to determine when to turn off the SR FET in discontinuous mode operation. This occurs when the voltage across the RDS(ON) of the SR FET drops below zero volts. In CCM, the SR FET is turned off before the pulse request is sent to the primary to demand the next switching cycle, providing excellent synchronous operation without any overlap for the FET turn-off.

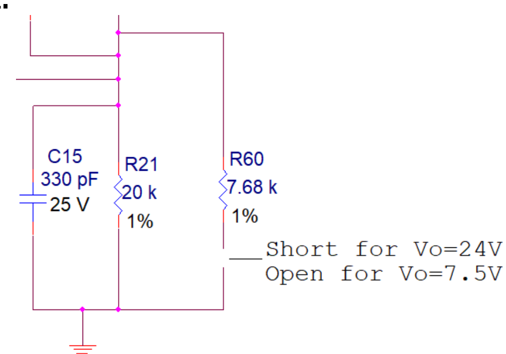
Output voltage is regulated through a feedback reference voltage of 1.27 V on the IC FB pin. Voltage divider resistors R5, R21 and R60 set the nominal output voltage to 24 V. Additionally, the RC phase boost (C11 and R7) helps to speed up the feedback voltage sensing, thereby reducing the ripple voltage. To demonstrate Low Standby Power mode, the output voltage is set to 7.5 V by disconnecting divider resistor R60.

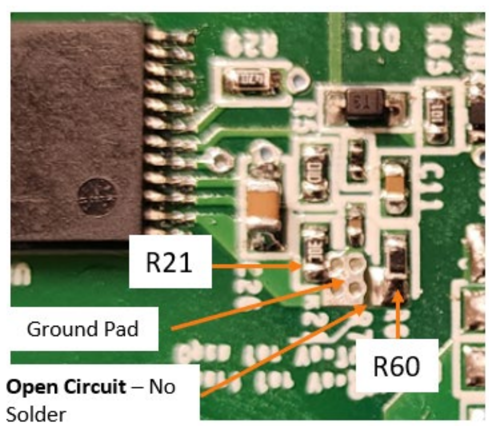
Current sense resistors R77 and R78, which are connected to the IS pin of the IC, set the OCP threshold to ≤ 9 A. The IC operates in AR mode once the voltage across the sense resistor reaches $I_{SV(TH)}$ (36 mV).

4.4 Standby Mode Setting

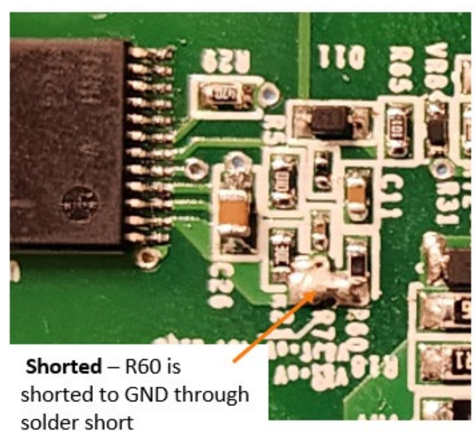
See below instructions on how to set the output voltage to 7.5 V for standby mode evaluations.

V_{OUT} = 24 V: Default nominal output voltage, R60 is shorted to GND through solder short
V_{OUT} = 7.5 V: For no load and standby mode operation. R60 is disconnected to GND by removing the solder short.





V_{OUT} = **7.5V** Setting for No load and standby Power test



V_{OUT} = **24V** Setting for nominal output load test

Figure 5 – V_{OUT} Selector Resistors

5 PCB Layout

The PCB uses FR4 material with a thickness of 1.6 mm and a double-sided copper layer with a thickness of 2.0 oz.

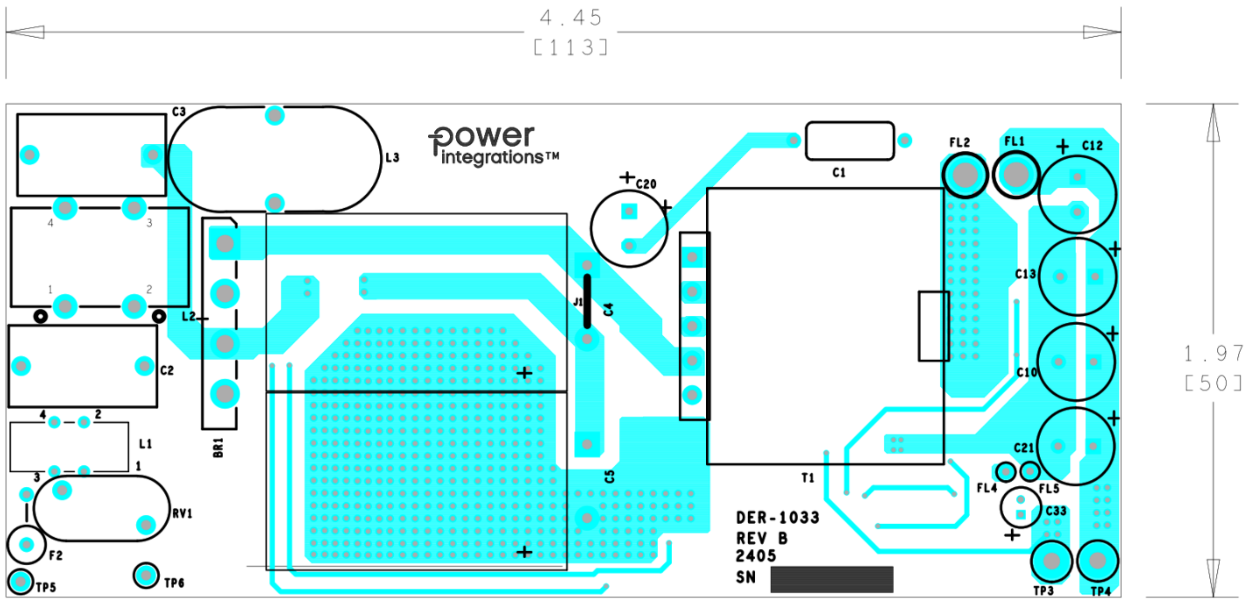


Figure 6 – Printed Circuit Layout, Top.

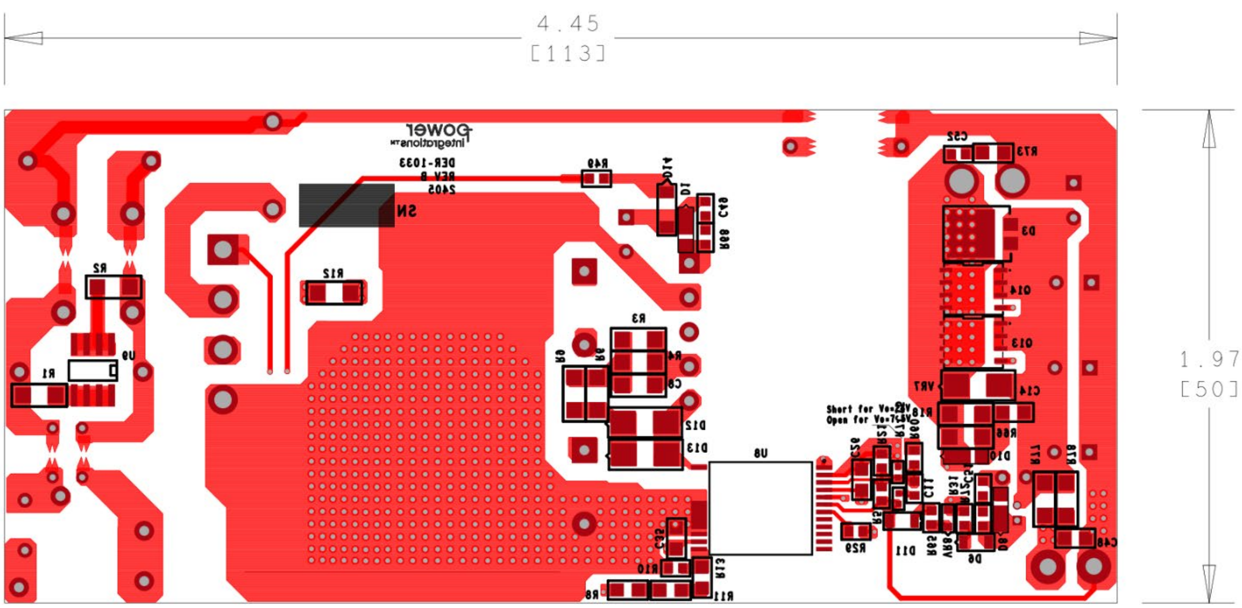


Figure 7 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Electrical Parts

Item Number	Part Reference	QTY	Description	Mfg Part Number	Mfg
1	BR1	1	Bridge Rectifier, Single Phase, Standard, 1 kV, Through Hole GBU	GBU1010	SMC Diode Solutions
2	C1	1	2200 pF, ±20%, 300VAC, Ceramic Capacitor E, Safety X1, Y1,Radial, Disc, 9mm diam, 10mm LS	DE1E3RA222MN4AP01F	Murata Electronics
3	C2 C3	2	220 nF, 275VAC, Film, X2	LE224-M	OKAYA ELECT IND CO. LTD.
4	C4 C5	2	330 µF, 200 V, Aluminum Electrolytic Capacitors, Radial, Can, 12000 Hrs @ 105°C, (18 x 30.5)	UCY2D331MHD6	Nichicon
5	C8	1	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115A A	TDK Corp
				885342008007	Würth Elektronik
6	C10 C12 C13 C21	4	330 µF, ±20%, 35 V, Aluminum - Polymer Capacitors Radial, Can, 20mOhm, 2000 Hrs @ 105°C, (8 x 16)	A750KW337M1VAAE020	KEMET
7	C11	1	15 nF, 50 V, Ceramic, X7R, 0603	CL10B153KB8NFNC	Samsung
				885012206090	Würth Elektronik
8	C14	1	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01 D	Murata
				885342207008	Würth Elektronik
9	C15	1	330pF, ±5%, 25V, Ceramic Capacitor, C0G, NP0, 0402 (1005 Metric)	C0402C331J3GAC7867	Kemet
10	C20	1	27 uF,±20%, 100 V, Al Electrolytic, Gen. Purpose, Can, (8mm x 13mm)	EEU-FS2A270B	Panasonic Electronic Components
			27 uF,±20%, 100 V Aluminum Electrolytic Capacitors Radial, Can 7000 Hrs @ 105°C, (8 x 11.5)	860040874001	Würth Elektronik
11	C26	1	OBSOLETE 2.2 uF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M125AB	TDK Corp
12	C33	1	10 uF, 25 V, Electrolytic, Gen. Purpose, (4 x7)	EEA-FC1E100	Panasonic Electronic Components
13	C35	1	4.7 µF, ±20%, 35V, Ceramic Capacitor X7R, 0805 (2012 Metric)	CGA4J1X7R1V475M125AE	TDK Corporation
14	C48	1	2.2 µF, ±10%, 50V, Ceramic Capacitor, X7R, 0805 (2012 Metric)	CGA4J3X7R1H225K125AE	TDK
15	C51	1	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
16	D1 D10	2	Diode, Schottky, 200 V, 1A, Surface Mount SOD-123HE	SS10200HE_R1_00001	Panjit International Inc.
17	D8	1	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes Inc
18	D3	1	Diode, Schottky, 150 V, 20A ,Surface Mount ,TO-277-3,TO-277, 3-PowerDFN	FSV20150V	onsemi
			200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes Inc
19	D6 D11	2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
20	D12 D13	2	1000 V, 1 A, DO-214AC	GS1M-LTP	Micro Commercial Co
21	D14	1	150 V, 0.2 A, SOD-123	BAV20W-TP	Micro Commercial Co
22	F2	1	6.3 A, 250 V, Slow, 3.6 mm x 10 mm, Axial	087706.3MXEP	Littelfuse
23	L1	1	CMC, 300 uH @ 100KHz, Toroidal, wound on 32-00315-00 toroidal core, using 10 turns #24 AWG wire per side	32-00429-00	Power Integrations
		1	Common Mode Choke	PM-PI0006	Premier Magnetics
24	L2	1	CMC, DER-1033, 5.5 mH, Common Mode Choke, wound on Toroid Core: 32-00343-00 (Green Color).	32-00464-00	Power Integrations
		1	Common Mode Choke	PM-PI0007	Premier Magnetics
25	L3	1	150uH, 3.4A, Vertical Toroidal	2114-V-RC	Bourns
26	Q13 Q14	2	MOSFET, N-Channel 150 V, 80 A (Ta), 157 W (Ta), Surface Mount 8-PDFN (5x6)	SRT15N110LD56TR-G	Shenzhen Sanrise Technology Co., LTD.
27	R1 R2	2	RES, 510 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J514V	Panasonic
28	R3 R4	2	RES, 1.0 M, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J105V	Panasonic
29	R5	1	RES,100 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	560112116004	Würth Elektronik
30	R6 R9	2	RES, 15 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J150V	Panasonic

			RES,100 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	560112116004	Würth Elektronik
31	R7	1	RES, 20 k, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ203X	Panasonic
32	R10	1	RES, 0 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
33	R12	1	RES, 0 Ohms Jumper, Chip Resistor 1206 (3216 Metric), Metal Element	JR1206X40E	Ohmite
34	R18 R66	2	RES, 9.1 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J9R1V	Panasonic
35	R21	1	RES, 20 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2002V	Panasonic
36	R29 R72	2	RES, 300 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ301V	Panasonic
37	R31 R65	2	RES, 100 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
38	R49	1	RES, 18.7 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1872V	Panasonic
39	R60	1	RES, 7.68 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7681V	Panasonic
40	R77	1	0.015 Ohm, ±1%, ±75ppm/°C, 1W, 1206 (3216 Metric), Current Sense,-55°C ~ 155°C	ERJ-8CWFR015V	Panasonic Electronic Components,
41	R78	1	RES, 5 mOhms, ±1%, 1W, Chip Resistor 1206 (3216 Metric), Pulse Withstanding Thick Film	CRF1206-FZ-R005ELF	Bourns Inc
42	RV1	1	275Vac, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
43	T1	1	Bobbin, ATQ28/18, Vertical, 4 pins. Mates with core 99-00071-00. Use 25-01224-00 for five pin version.		Power Integrations
			Transformer, 5 pins, 4 FL, WURTH	750345750	Würth Elektronik
44	U8	1	InnoSwitch4-QR, INN4277C-H181 ,230VDC,125W, insop-24D	INN4277C-H181	Power Integrations
45	U9	1	CAPZero-2, CAP200DG, SO-8C	CAP200DG	Power Integrations
46	VR7	1	TVS, 146V Clamp, 2.7A Ipp, Tvs Diode, Surface Mount DO-214AC (SMA)	SMAJ90A	Bourns Inc.
47	VR8	1	27 V, 5%, 150 mW, SOD 523	EDZTE6127B	Rohm Semi

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	TP3	1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
2	TP4	1	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone
3	TP5	1	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
4	TP6	1	Test Point, WHT,Miniature THRU-HOLE MOUNT	5002	Keystone

7 Flyback Transformer Design Spreadsheet

1	*ACDC_InnoSwitch4-QR_Flyback_050823; Rev.0.1; Copyright Power Integrations 2023*	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*InnoSwitch4 QR Single/Multi Output Flyback Design Spreadsheet*
2	**APPLICATION VARIABLES**					Design Title
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	180		180	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			HIGH LINE		Range of AC input voltage
7	LINEFREQ	60		60	Hz	AC Input voltage frequency
8	CAP_INPUT	330.0		330.0	uF	Input capacitor
9	VOUT	24.00		24.00	V	Output voltage at the board
10	CDC	0		0	mV	Cable drop compensation desired at full load
11	IOUT	8.200		8.200	A	Output current
12	POUT		Info	196.80	W	The specified output power exceeds the device power capability: Verify thermal performance if no other warnings
13	EFFICIENCY	0.92		0.92		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
14	FACTOR_Z			0.60		Z-factor estimate
15	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
19	**PRIMARY CONTROLLER SELECTION**					
20	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
21	DEVICE_GENERIC	INN4277		INN4277		Generic device code
22	DEVICE_CODE			INN4277C		Actual device code
23	POUT_MAX			145	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.29	Ω	Primary switch on time drain resistance at 100 degC
25	ILIMIT_MIN			3.505	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			3.810	A	Typical current limit of the primary switch
27	ILIMIT_MAX			4.115	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.25	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW			549.4	V	Peak drain voltage on the primary switch during turn-off. A 30V leakage spike voltage is assumed
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	135000	Warning	135000	Hz	Operation above 100kHz could result in output overload trigger
36	VOR	146.0		146.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			235.91	V	Valley of the minimum input AC voltage at full load

38	KP			0.71		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.383		Primary switch duty cycle
41	TIME_ON			4.80	us	Primary switch on-time
42	TIME_OFF			4.57	us	Primary switch off-time
43	LPRIMARY_MIN			257.6	uH	Minimum primary inductance
44	LPRIMARY_TYP			271.1	uH	Typical primary inductance
45	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
46	LPRIMARY_MAX			284.7	uH	Maximum primary inductance
48	**PRIMARY CURRENT**					
49	IPEAK_PRIMARY			4.103	A	Primary switch peak current
50	IPEDESTAL_PRIMARY			1.022	A	Primary switch current pedestal
51	IAVG_PRIMARY			0.879	A	Primary switch average current
52	IRIPPLE_PRIMARY			3.613	A	Primary switch ripple current
53	IRMS_PRIMARY			1.560	A	Primary switch RMS current
55	SECONDARY CURRENT					
56	IPEAK_SECONDARY			25.647	A	Secondary winding peak current
57	IPEDESTAL_SECONDARY			6.389	A	Secondary winding current pedestal
58	IRMS_SECONDARY			12.389	A	Secondary winding RMS current
62	**TRANSFORMER CONSTRUCTION PARAMETERS**					
63	**CORE SELECTION**					
64	CORE	ATQ28/18.1B		ATQ28/18.1B		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
65	CORE CODE			ATQ28/18.1B		Core code
66	AE			153.00	mm^2	Core cross sectional area
67	LE			47.70	mm	Core magnetic path length
68	AL			9800	nH/turns^2	Ungapped core effective inductance
69	VE			7298.0	mm^3	Core volume
70	BOBBIN			TBI-238-07271.17XX		Bobbin
71	AW			37.40	mm^2	Window area of the bobbin
72	BW			8.50	mm	Bobbin width
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			25		Primary turns
77	BPEAK			3194	Gauss	Peak flux density
78	BMAX			3028	Gauss	Maximum flux density
79	BAC			1319	Gauss	AC flux density (0.5 x Peak to Peak)

80	ALG			434	nH/turns^2	Typical gapped core effective inductance
81	LG			0.424	mm	Core gap length
83	**PRIMARY BIAS WINDING**					
84	NBIAS_PRIMARY			7		Primary bias winding number of turns
86	**SECONDARY WINDING**					
87	NSECONDARY	4		4		Secondary winding number of turns
89	**SECONDARY BIAS WINDING**					
90	NBIAS_SECONDARY			1		Secondary bias winding number of turns
94	**PRIMARY COMPONENTS SELECTION**					
95	LINE UNDERVOLTAGE					
96	BROWN-IN REQURED			140.40	V	Required AC RMS/DC line voltage brown-in threshold
97	RLS			7.30	MΩ	Connect two 3.65 MOhm resistors to the V-pin for the required UV/OV threshold
98	BROWN-IN ACTUAL			119.5V - 144.8V	V	Actual AC RMS/DC brown-in range
99	BROWN-OUT ACTUAL			106.2V - 131.8V	V	Actual AC RMS/DC brown-out range
100						
101	LINE OVERVOLTAGE					
102	OVERVOLTAGE_LINE		Warning	543.1V - 616.6V	V	The device voltage stress will be higher than 750V when overvoltage is trigerred
104	**PRIMARY BIAS DIODE**					
105	VBIAS_PRIMARY	40.0		40.0	V	Rectified primary bias voltage
106	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
107	VREVERSE_BIASDIODE_PRIMARY			146.54	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
108	CBIAS_PRIMARY			22	uF	Bias winding rectification capacitor
109	CBPP			4.70	uF	BPP pin capacitor
113	**SECONDARY COMPONENTS**					
114	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
115	RFB_LOWER			5.62	kΩ	Lower feedback resistor
116	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
118	**SECONDARY BIAS DIODE**					
119	USE_SECONDARY_BIAS	YES		YES		Use secondary bias winding for the design
120	VBIAS_SECONDARY			5.0	V	Rectified secondary bias voltage
121	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
122	VREVERSE_BIASDIODE_SECONDARY			19.93	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
123	CBIAS_SECONDARY			10	uF	Bias winding rectification capacitor
124	CBPS			2.20	uF	BPP pin capacitor
127	**MULTIPLE OUTPUT PARAMETERS**					
128	OUTPUT 1					
129	VOUT1			24.00	V	Output 1 voltage
130	IOUT1			8.20	A	Output 1 current
131	POUT1			196.80	W	Output 1 power

132	IRMS_SECONDARY1			12.389	A	Root mean squared value of the secondary current for output 1
133	IRIPPLE_CAP_OUTPUT1			9.287	A	Current ripple on the secondary waveform for output 1
134	NSECONDARY1			4		Number of turns for output 1
135	VREVERSE_RECTIFIER1			83.74	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
136	SRFET1	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET) for output 1
137	VF_SRFET1			0.057	V	SRFET on-time drain voltage for output 1
138	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
139	RDSON_SRFET1			7.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

8 Transformer Specification

8.1 Electrical Diagram

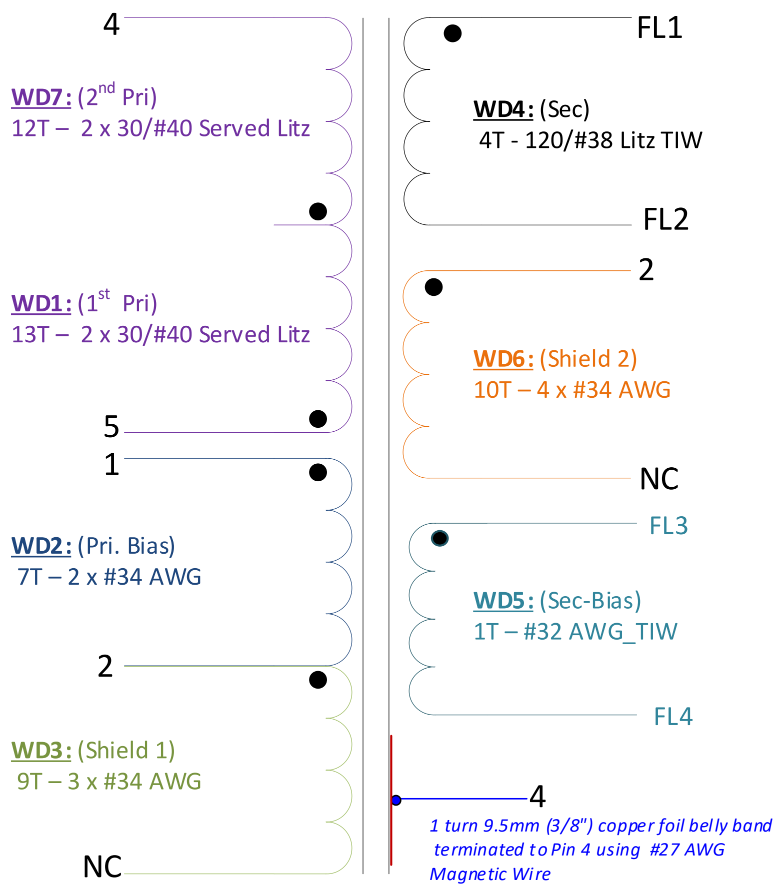


Figure 8 – Transformer Schematic.

8.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.	270 uH± 5%
Resonant Frequency	Between pin 5 and 4, other windings open	100KHz
Primary Leakage Inductance	Between pin 5 and 4, with pins: FL1-FL2 shorted (Twisted)	5 uH (max)

8.3 Materials

Item	Description
[1]	Core: ATQ28/18 P/N: 99-00071-00.
[2]	Bobbin: Bobbin, ATQ28/18, Vertical, 5 pins. P/N: 25-01170-00
[3]	Magnet wire: Served Litz 30/#40.
[4]	Magnet wire: #34 AWG, double coated.
[5]	Magnet wire: 120/#38, Litz_Triple Insulated Wire.
[7]	Magnet wire: #32 AWG, Triple Insulated Wire.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 8.6 mm width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 12.0 mm width
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 65mm x 33mm.
[10]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 36 mm width
[11]	Copper Foil: 2 mil thick, 9.5mm (3/8”).
[12]	Varnish: Dolph BC-359.

8.4 Transformer Build Diagrams

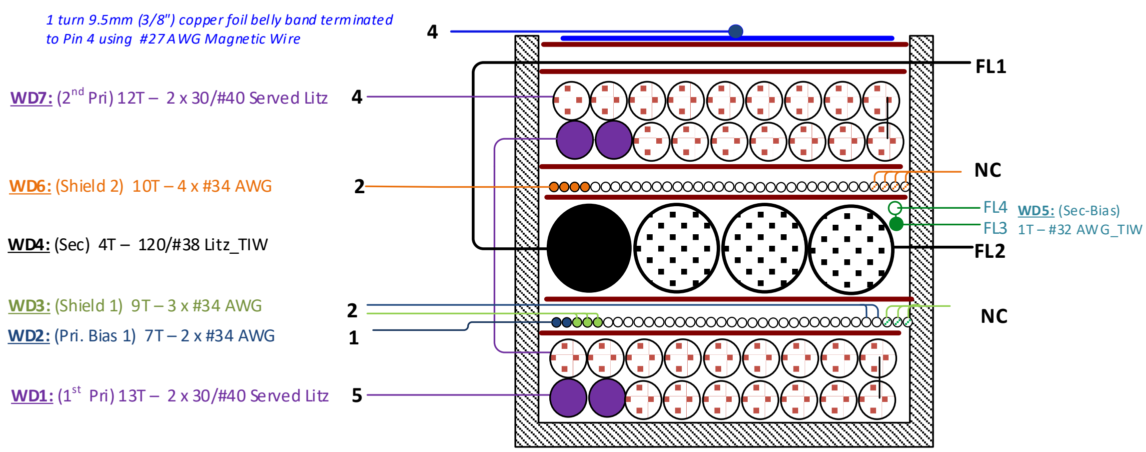


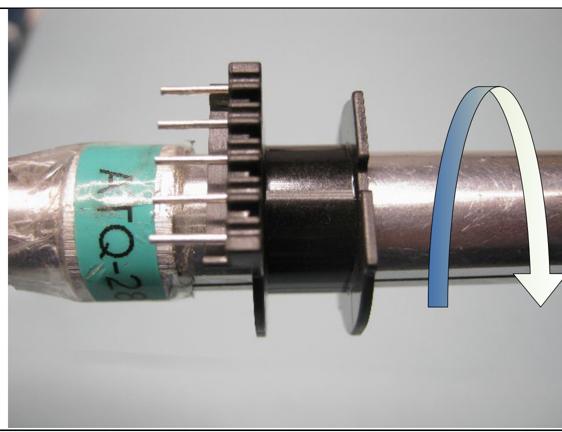
Figure 9 – Transformer Build Diagram.

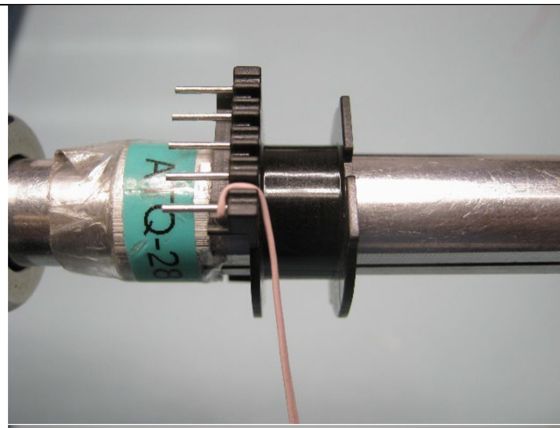
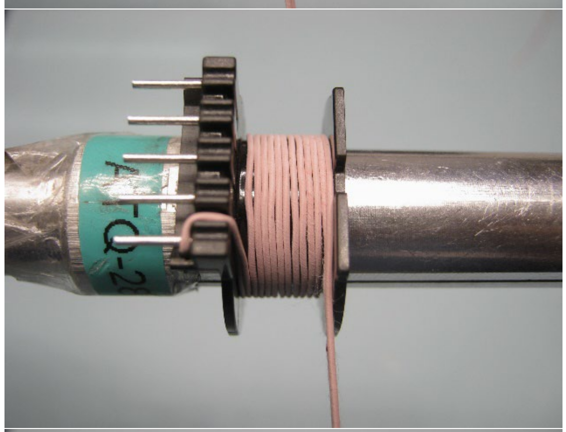
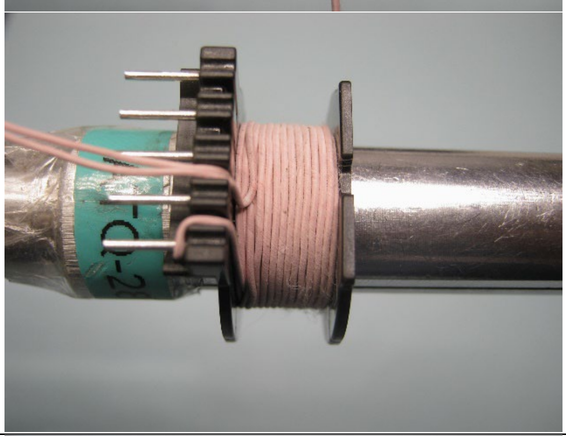
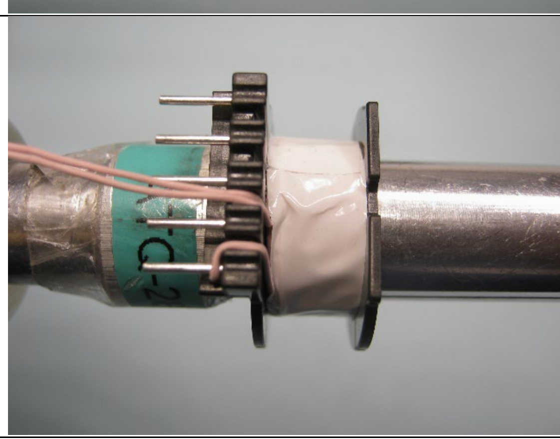
8.5 Winding Constructions

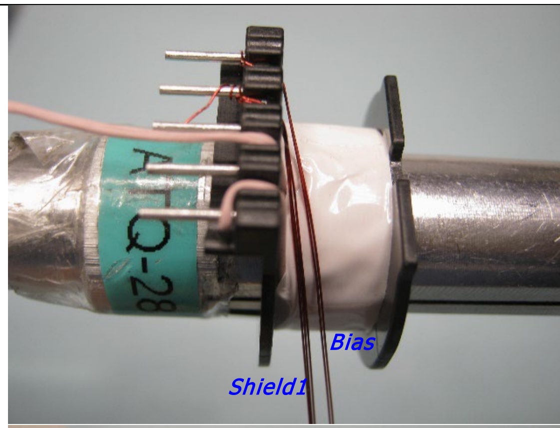
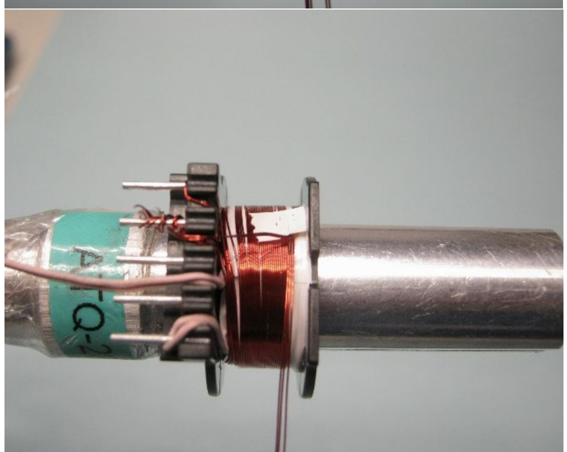
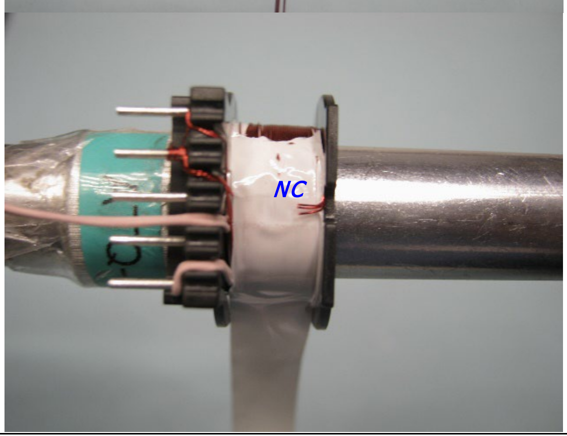
Winding preparation	Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**	Start at pin 5, wind 13 bifilar turns of wire item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD7-2nd Primary.
Insulation	1 layer of tape item [7].
WD2: Bias **&** **WD3: Shield1**	Use 2 wires item [4] start at pin 1 for Bias winding, also use 3 wires same item [4] start at pin 2 for Shield1 winding. Wind all 5 wires in parallel, at the 7th turn: - bring 2 wires for Bias winding to the left and terminate at pin 2, - continue winding 2 more turns for Shield1 winding and cut short 3 wires as no connect.

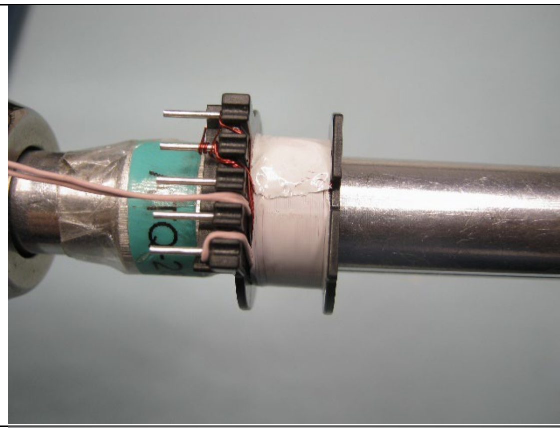
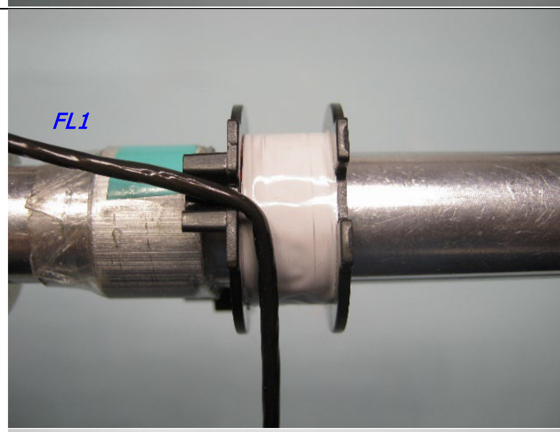
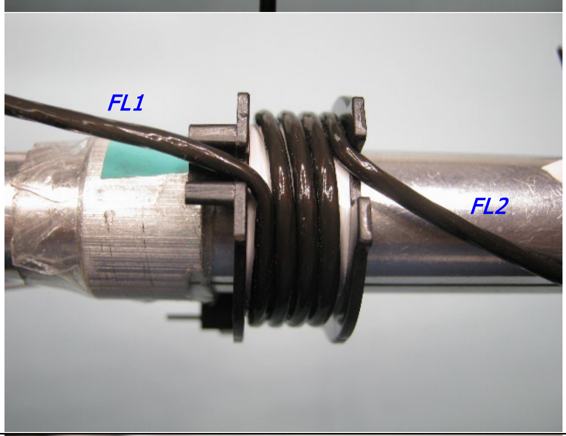
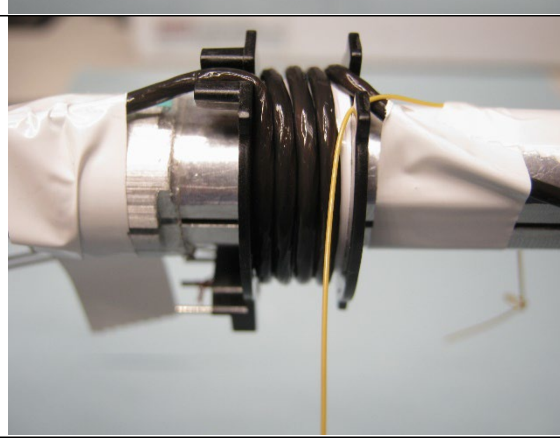
Insulation	1 layer of tape item [7].
WD4 Secondary	Start at left slot of secondary side, use wire item [5], leaving ~ 40mm floating, and mark as FL1.Wind 4 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 32mm floating, and mark FL2.
WD5 Sec - Bias	At right slot of secondary side, wind 1 turn of wire item [7], start as FL3 and end as FL4, and leave ~40mm floating for both ends.
Insulation	1 layer of tape item [7].
WD6 Shield2	Start at pin 2, wind 10 quad-filar turns of wire item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape item [7].
WD7 2nd Primary	Use floating wire from WD1-1st Primary, wind 12 bi-filar turns in 2 layers, from right to left and left to right. At the last turn, finish at pin 4.
Insulation	Bring floating wire marked as FL1 from Secondary winding to the left and secure with 2 layers of tape item [7].
Finish	Gap core halves to get 270uH and secure with tape item [8]. Wrap around transformer 1 layer of copper foil item [11], solder at joint to make a closed loop, and solder pin 4 with wire #27AWG to copper foil. Varnish with item [12]. Place 2 layers of tape item [9] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape item [8]. (*See pictures below*).

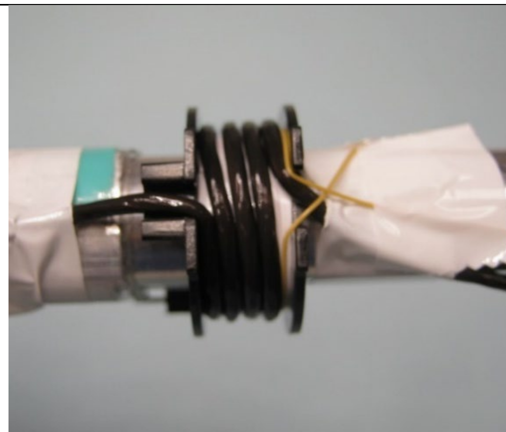
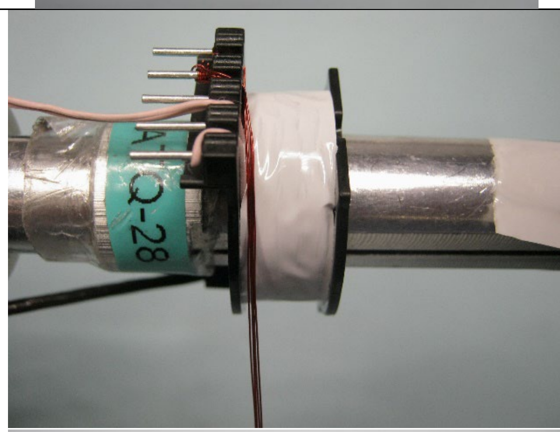
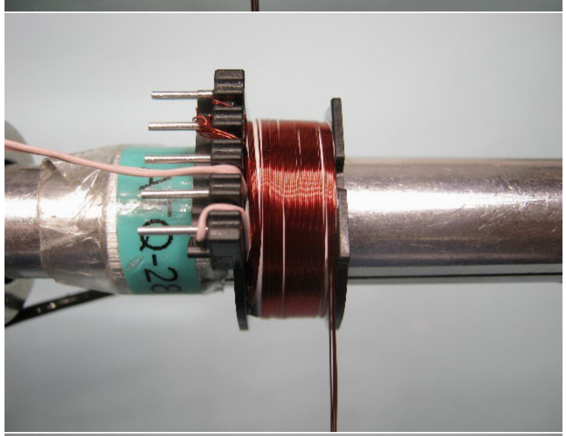
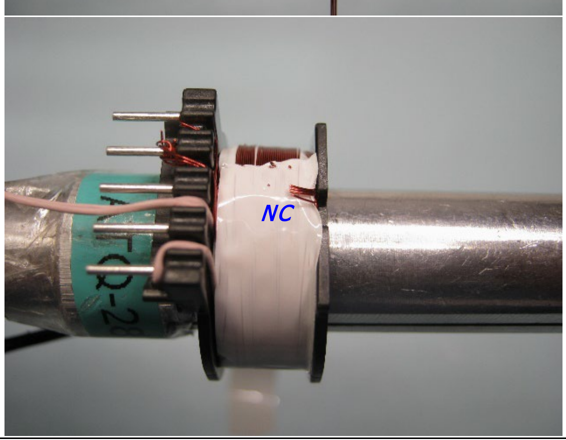
8.6 Winding Illustrations

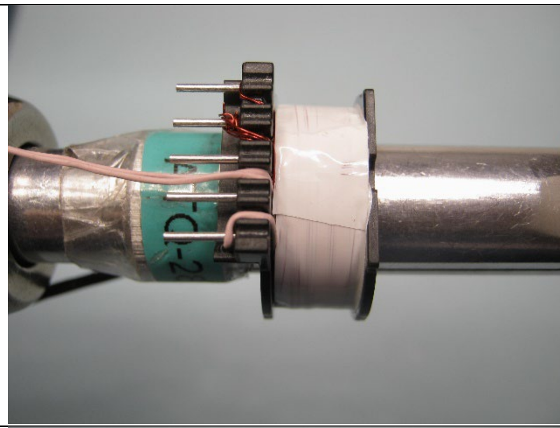
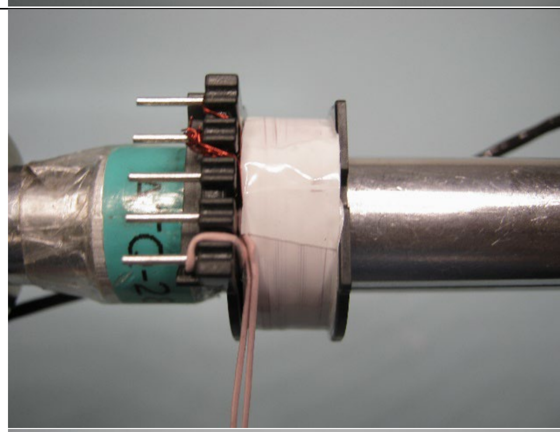
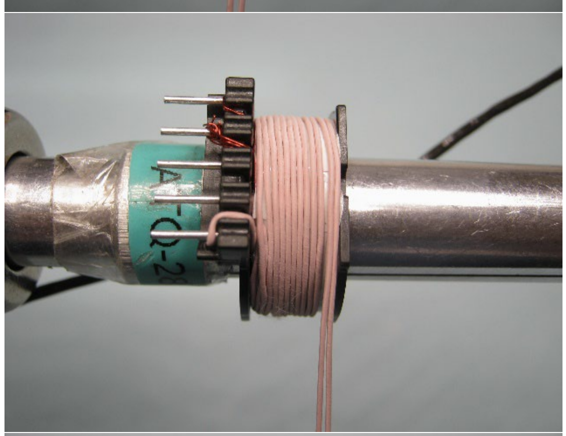
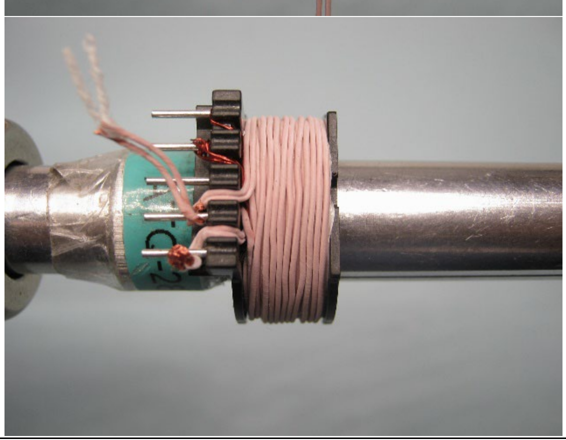
Winding preparation		Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.

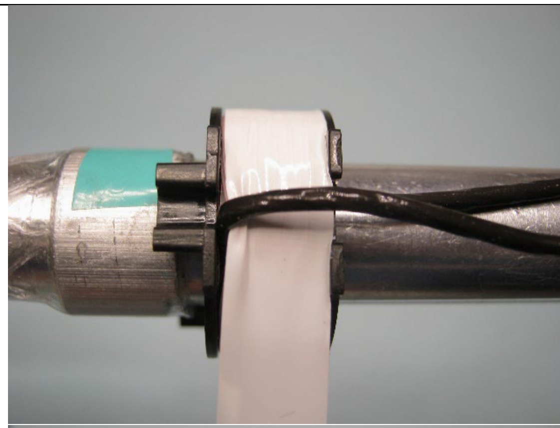
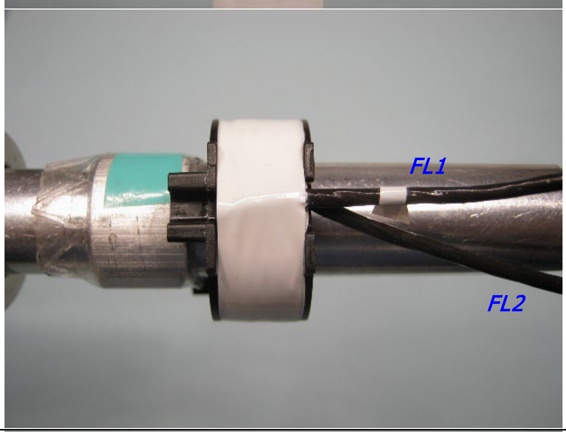
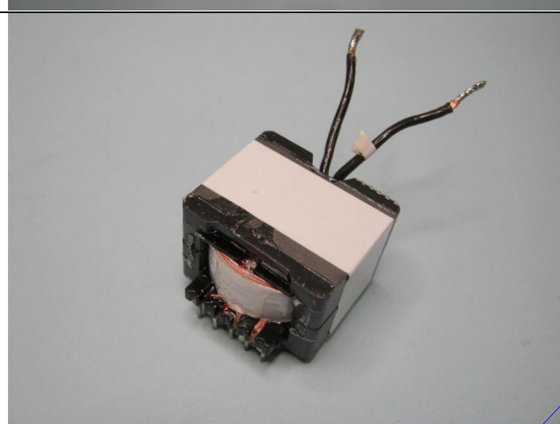
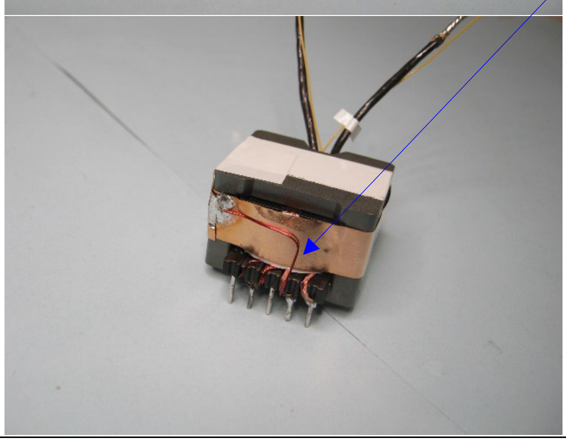
WD1 **1st Primary**	  	Start at pin 5, wind 13 bifilar turns of wire item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD7-2nd Primary.
Insulation		1 layer of tape item [7].

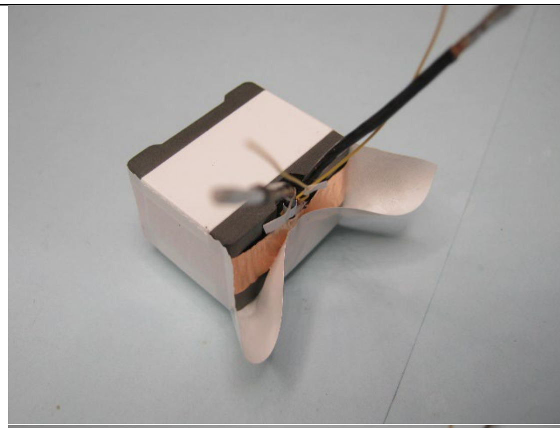
WD2: Bias & WD3: Shield1	   	Use 2 wires item [4] start at pin 1 for Bias winding, also use 3 wires same item [4] start at pin 2 for Shield1 winding. Wind all 5 wires in parallel, at the 7th turn: - bring 2 wires for Bias winding to the left and terminate at pin 2, - continue winding 2 more turns for Shield1 winding and cut short 3 wires as no connect.

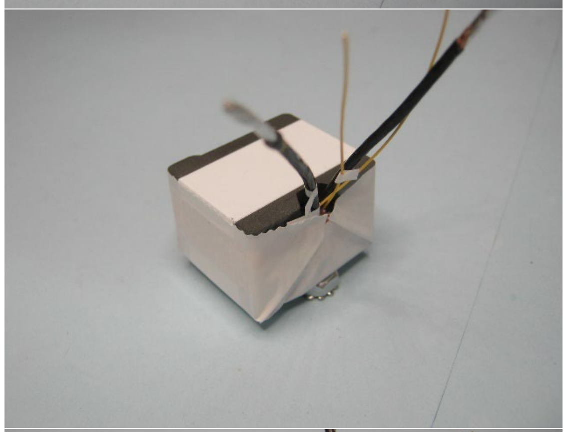
Insulation		1 layer of tape item [7].
WD4 **Secondary**	 	Start at left slot of secondary side, use wire item [5], leaving ~ 40mm floating, and mark as FL1.Wind 4 turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 32mm floating, and mark FL2.
WD5 **Sec - Bias**		At right slot of secondary side, wind 1 turn of wire item [7], start as FL3 and end as FL4, and leave ~40mm floating for both ends.

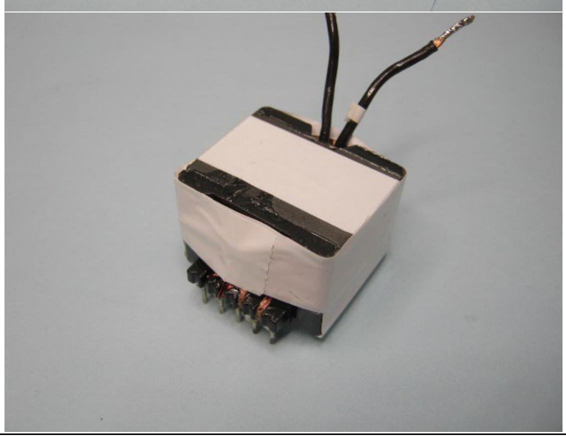
		
WD6 **Shield2**	   	Start at pin 2, wind 10 quad-filar turns of wire item [4], from left to right. At the last turn, cut short to leave as No-Connect.

Insulation		1 layer of tape item [7].
WD7 **2[nd] Primary**	  	Use floating wire from WD1-1[st] Primary, wind 12 bi-filar turns in 2 layers, from right to left and left to right. At the last turn, finish at pin 4.

Insulation	 	Bring floating wire marked as FL1 from Secondary winding to the left and secure with 2 layers of tape item [7].
Finish	 	Gap core halves to get 270uH and secure with tape item [8]. Wrap around transformer 1 layer of copper foil item [11], solder at joint to make a closed loop, and solder pin 4 with wire with wire #27 to copper foil. Varnish with item [12]. Place 2 layers of tape item [9] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape item [8]. (*See pictures below*).







9 Input Common Mode Choke (L2)

9.1 Electrical Diagram

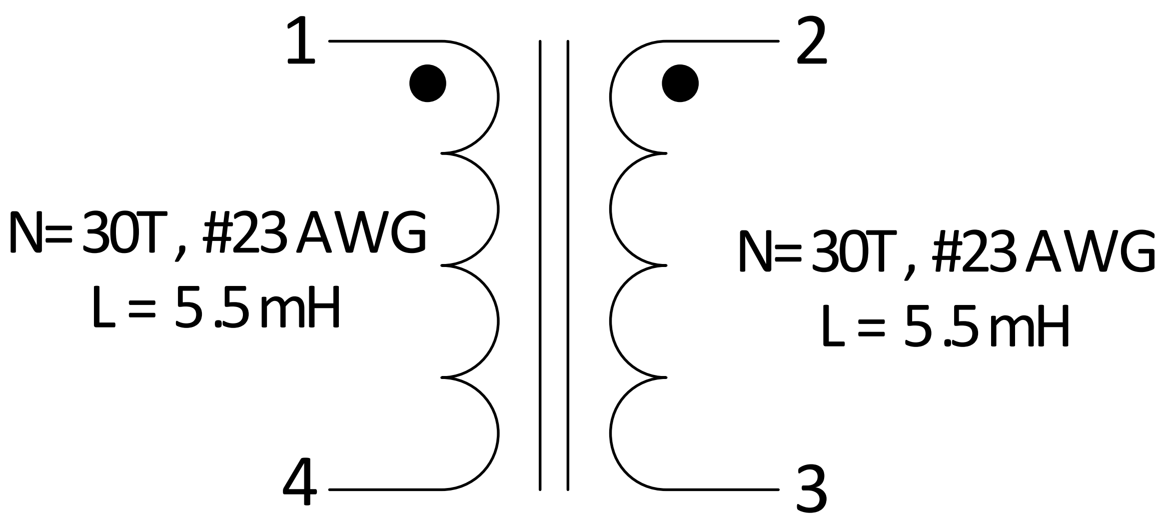


Figure 10 – Inductor Electrical Diagram.

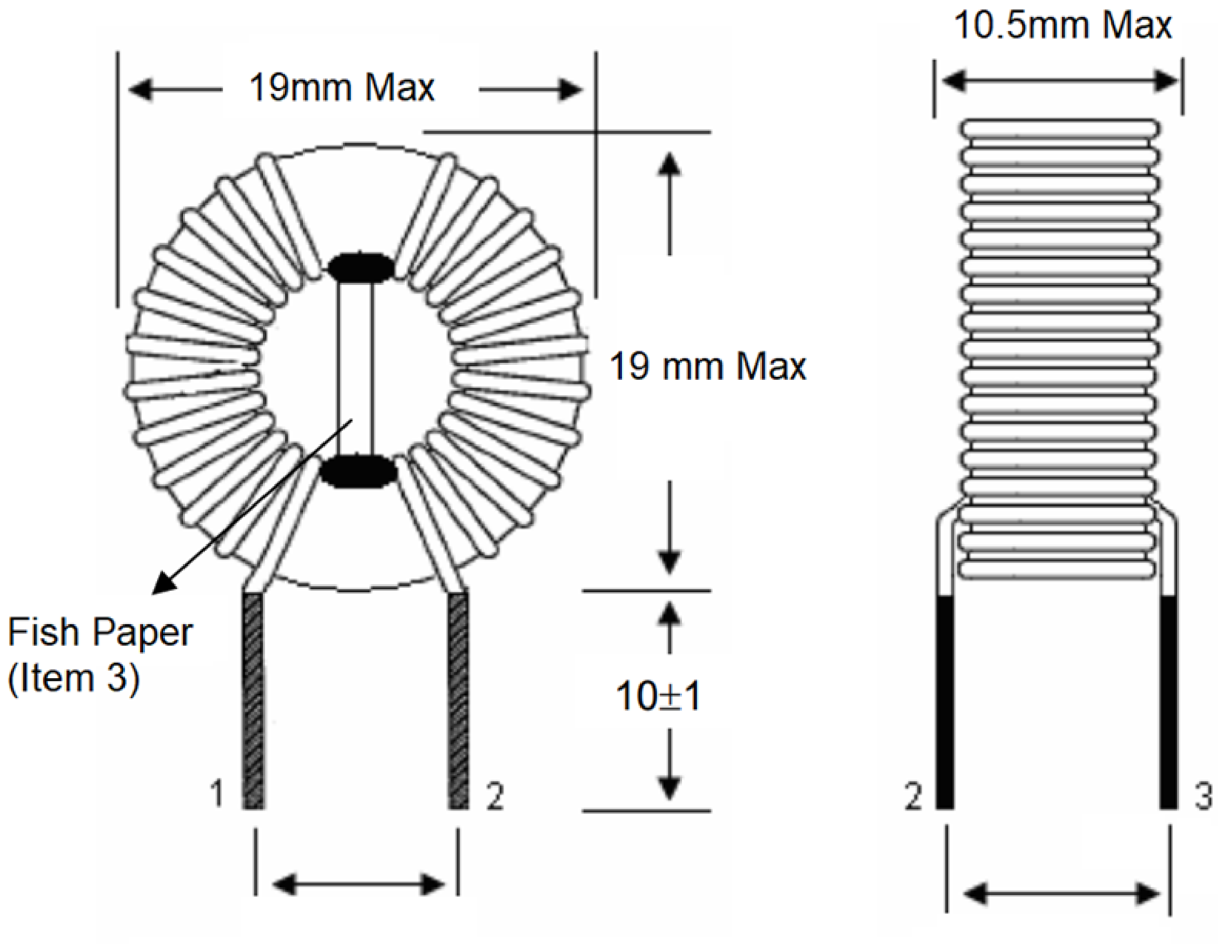
9.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	100 kHz Resonant frequency, between pin 1 and pin 4 or pin 2 and pin 3 with all other windings open.	5.5 mH
Tolerance	Tolerance of winding Inductance.	±20%

9.3 Materials

Item	Description
[1]	Toroid Core: 32-00343-00(Green)
[2]	Magnet Wire: #23 AWG
[3]	Fish Paper, 0.030" Thick, Cotton Rag, UL-94HB (P/N: 66-00042-00)

9.4 Inductor Build Diagram



S→F	WIRE	TURNS
1→4	AWG#23	30 T
2→3	AWG#23	30 T

Figure 11 – Inductor Build Diagram.

9.5 Inductor Construction

1. Insert and fix the fish paper insulator (Item 3) as shown in the figure.
2. Winding 1 – Start at Pin 1 and wind 38 turns of item 2 as shown in above figure. Finish the winding at Pin 4
3. Winding 2 – Start at Pin 2 and wind 38 turns of item 2 as shown in above figure. Finish the winding at Pin 3
4. Apply Varnish

10 Performance Data

Performance data were measured at room ambient temperature, with voltages taken at the board's input and output terminals unless otherwise specifically mentioned. The following input power measurement setups were used in measuring efficiency performance.

A. Power Meter Setting at Nominal Output Load > 5 W

For output power > 5W, the effect of voltage drop due to the input cable is noticeable, particularly at low input line. The below input power meter setting is recommended for accurate input power measurement.

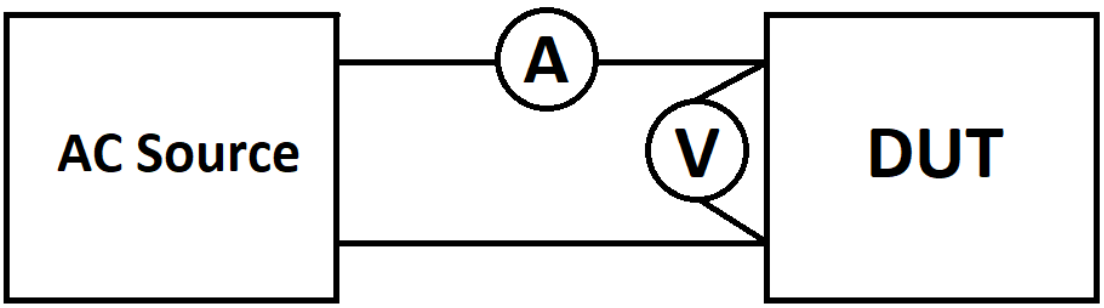


Figure 12 – Input Power meter setting for output load > 5W.

B. Power Meter Setting at No Load and Standby Mode (< 5 W)

For output power < 5 W, the effect of leakage current drawn by the voltmeter is noticeable, especially at high line. Below input power meter settings are recommended for accurate input power measurement.

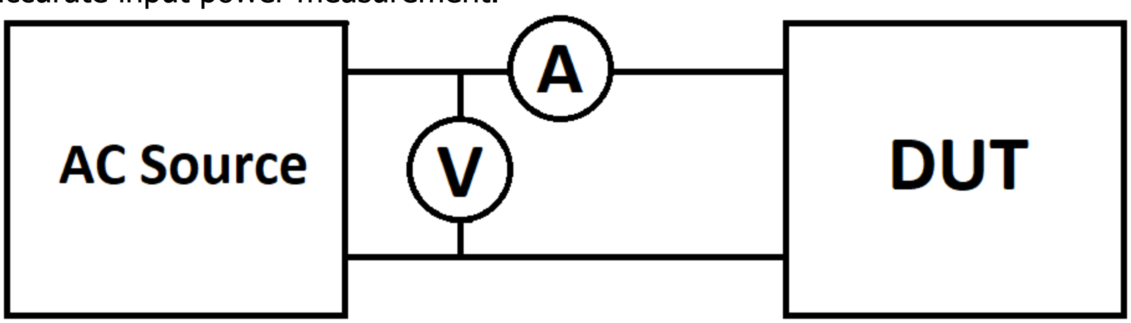


Figure 13 – Input Power meter setting for output load < 5W.

10.1 Efficiency at 24V Full Load

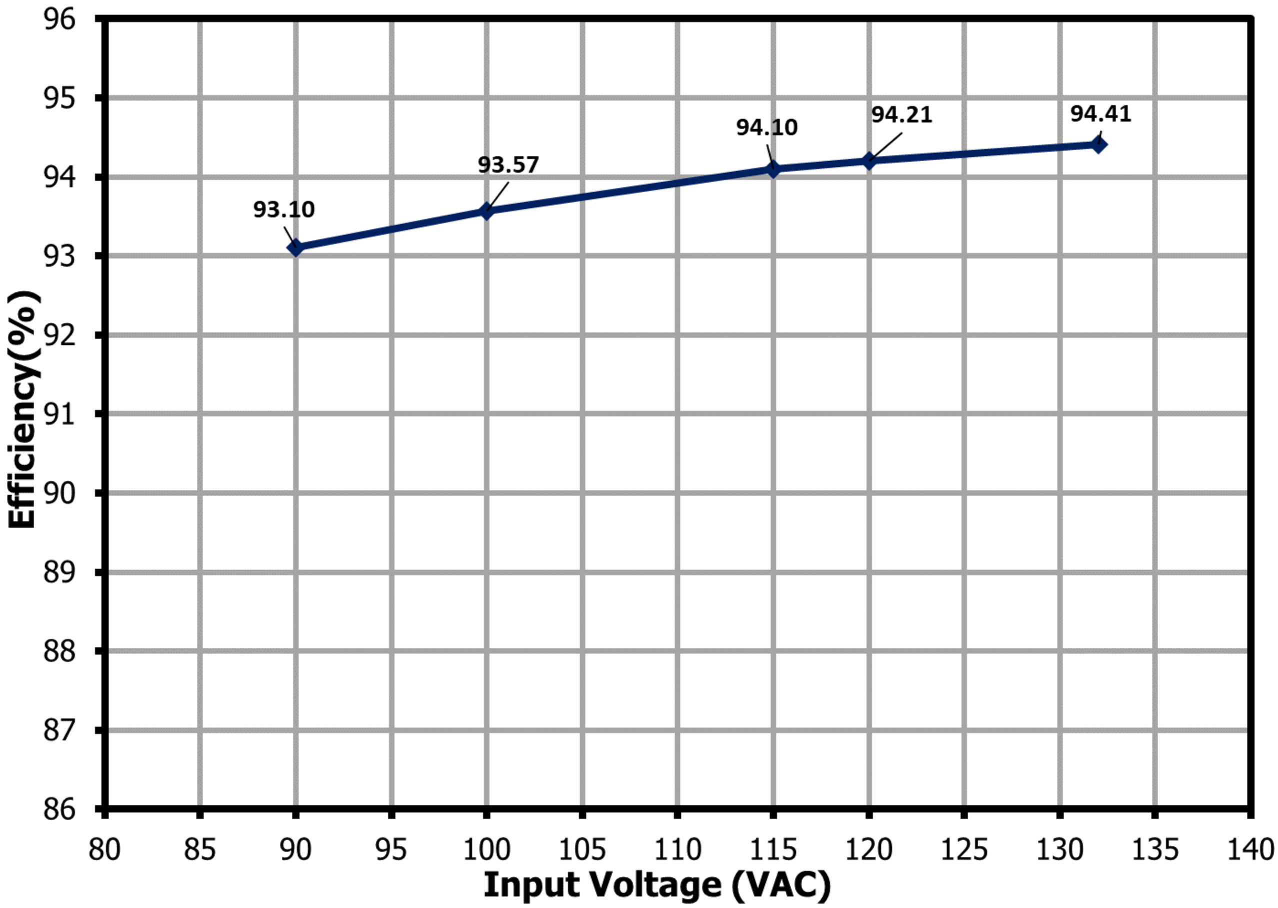


Figure 14 – Efficiency vs. Input Line Voltage at 24 V Output.

10.2 No-Load Input Power

No load input power was measured at 7.5 V output voltage setting using a Yokogawa WT310E power meter. The power meter is set at no load or standby mode measurement setting in Figure 13.

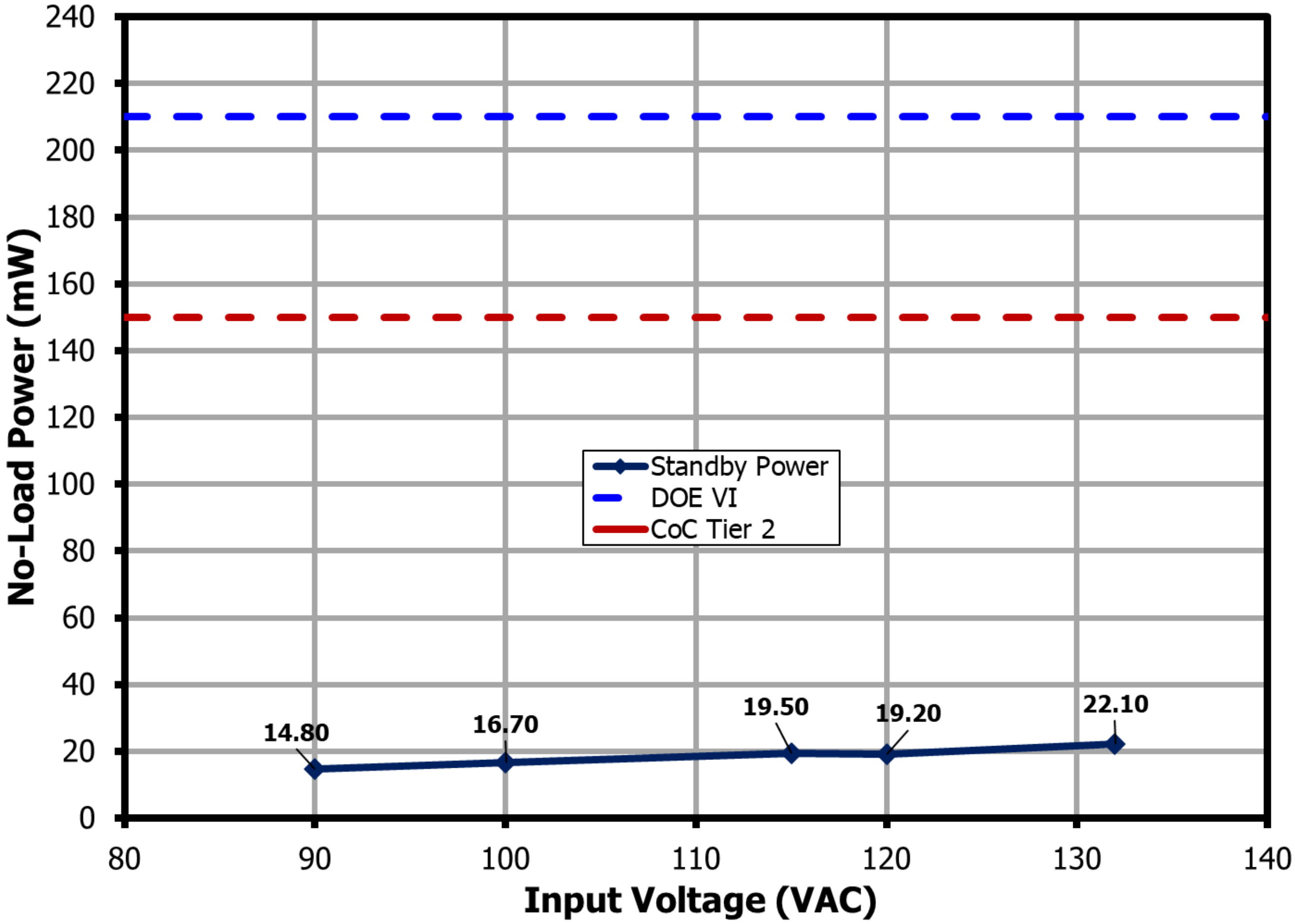


Figure 15 – No-Load Input Power vs. Input Line Voltage, V_{OUT} = 7.5 V.

10.3 Average Efficiency at 115VAC

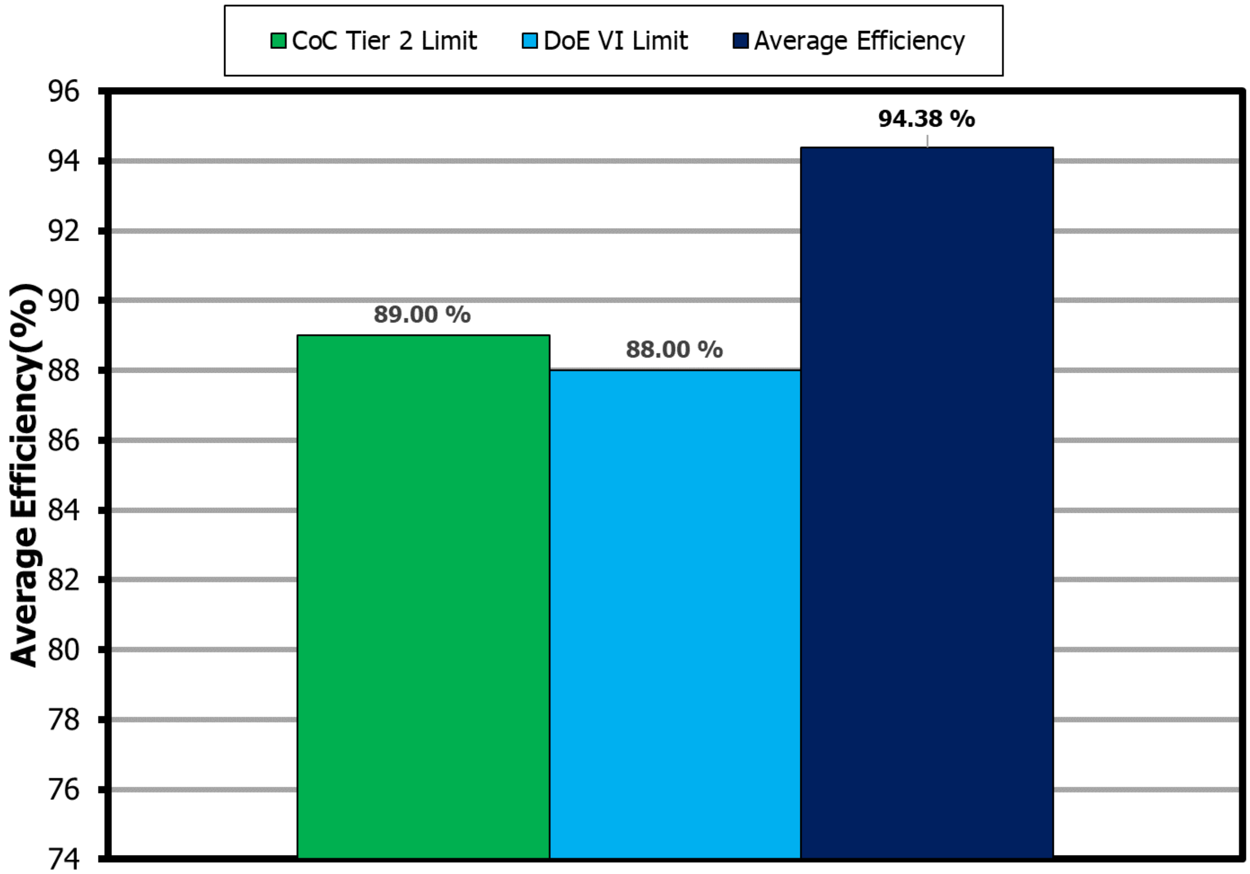


Figure 16 – Average Efficiency at 115 VAC, V_{OUT} = 24 V.

10.4 Efficiency at 10% Load, 115 VAC

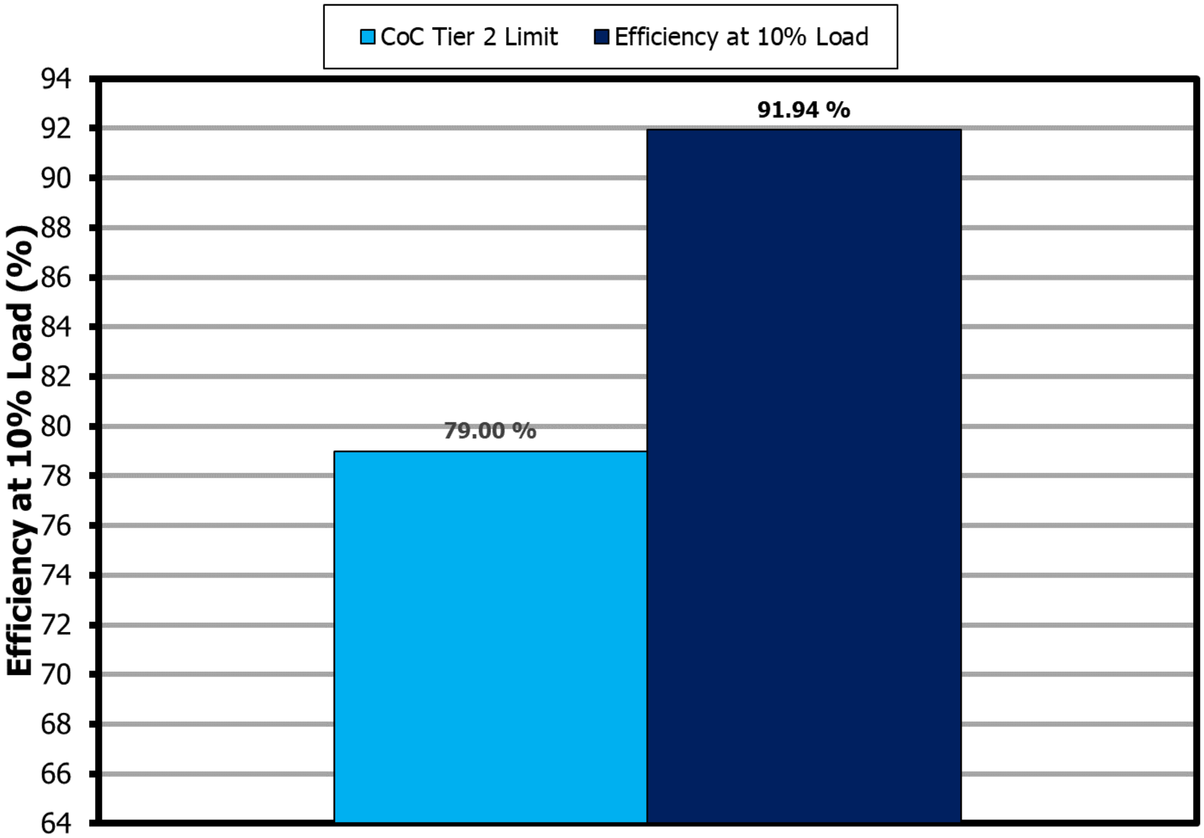


Figure 17 – Efficiency at 10% Load, 115 VAC, V_{OUT} = 24 V.

10.5 Full Load Line Regulation at 24 V 5.4 A Output

Output regulations were based on 24 V nominal output voltage.

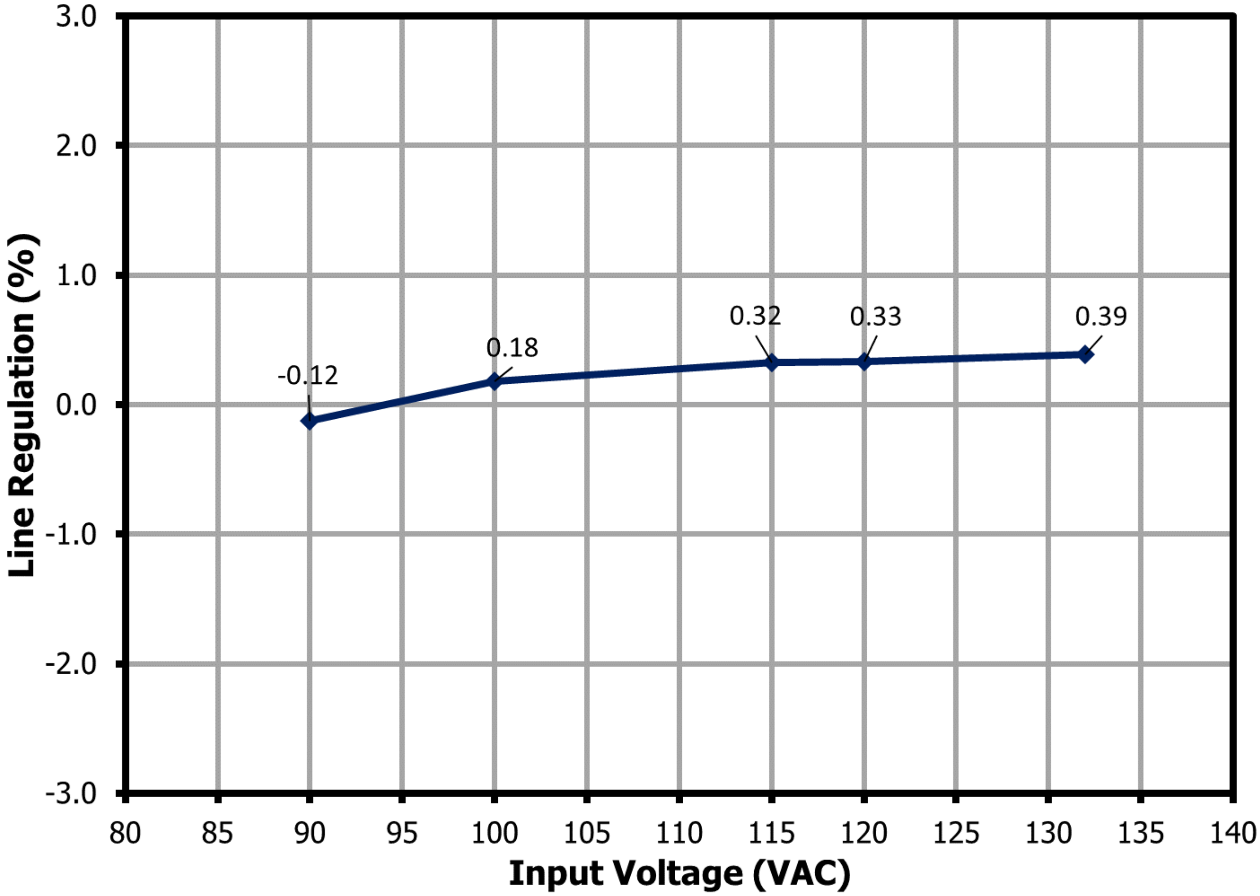


Figure 18 – Full Load Voltage Regulation vs. Input Line Voltage, V_{OUT} = 24 V 5.4 A.

10.6 Efficiency vs Load at 24 V 5.4 A

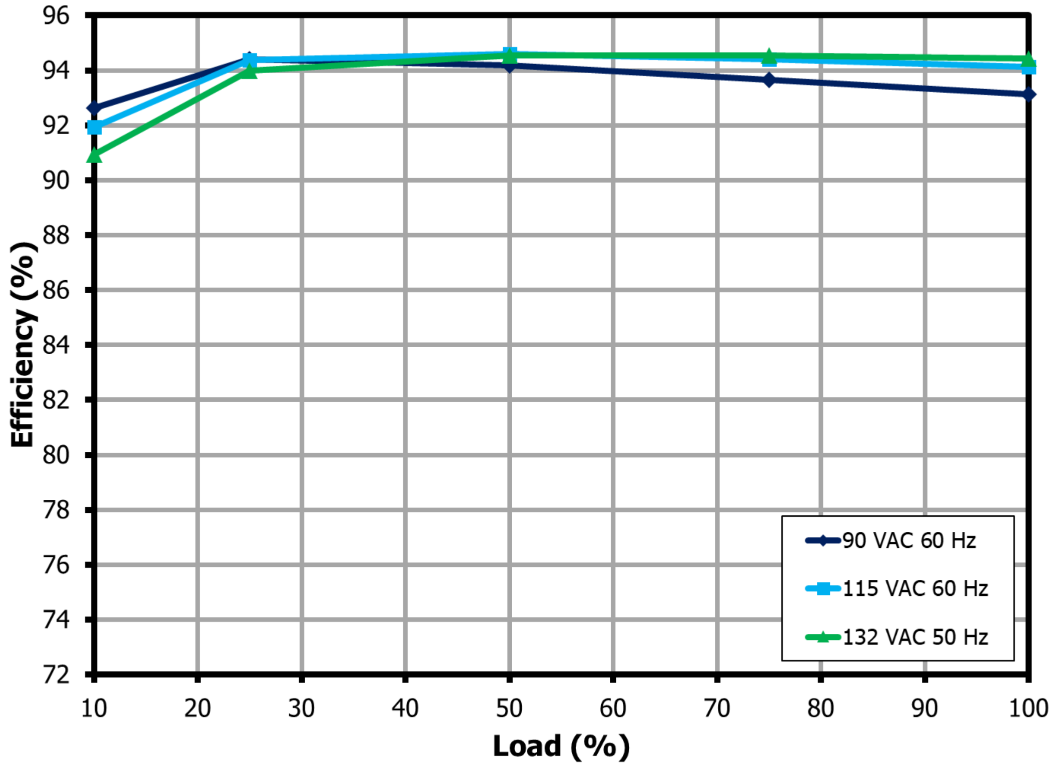


Figure 19 – Efficiency vs. % Load at 24 V 5.4 A.

10.7 Load Regulation at 24 V 5.4 A

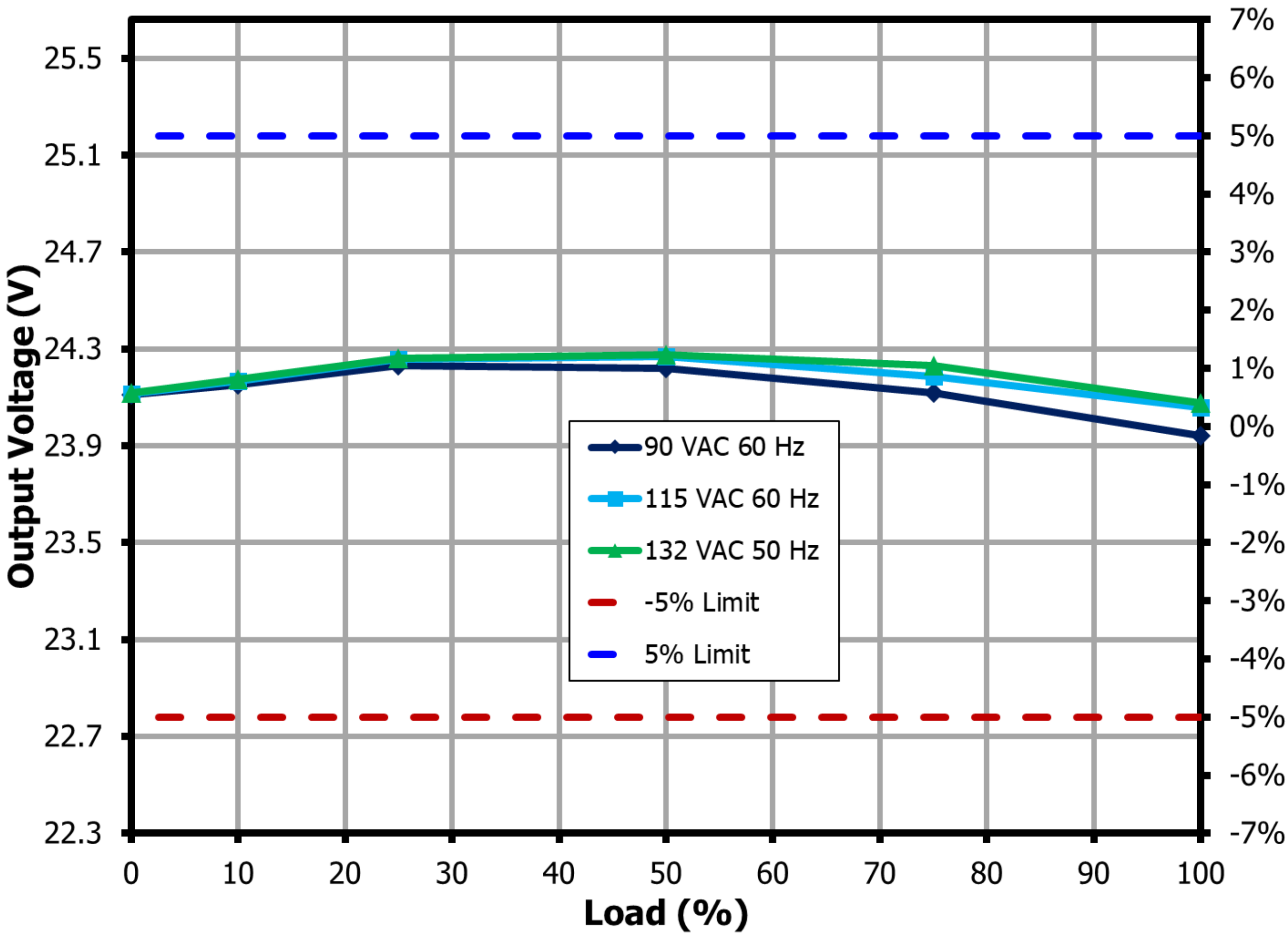


Figure 20 – Voltage Regulation vs. % Load at 24 V 5.4 A.

10.8 Output Ripple Voltage at 24 V

Output ripple voltage was measured at the end of 100 mΩ output cable.

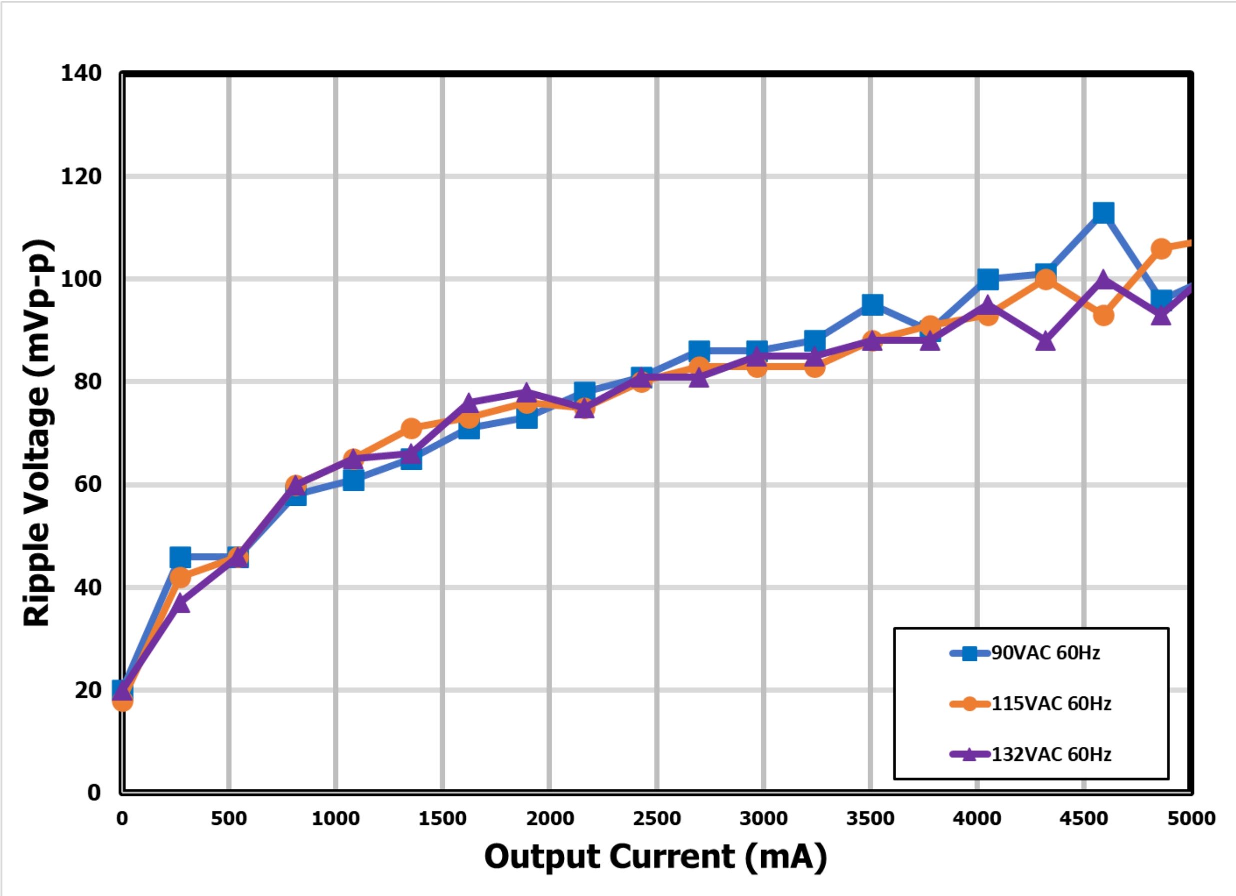


Figure 21 – Ripple voltage vs. Load at 24 V.

10.9 Standby Input Power at 40 mW Output Load

Standby input power was measured at 7.5 V output voltage setting using a Yokogawa WT310E power meter. The power meter is set at no load or standby mode measurement setting in Figure 13.

Input		Input Measurement		Output 1 Measurement				Efficiency
Vac (rms)	Freq (Hz)	Vin (rms)	Pin (W)	Vo (V)	Io (mA)	Po (W)	%V Reg	
90	60	90.0	0.06	7.61	5.49	0.04	1.49	65.5
100	60	100	0.06	7.61	5.45	0.04	1.49	64.1
115	60	115	0.06	7.61	5.41	0.04	1.49	62.3
120	60	120	0.06	7.61	5.42	0.04	1.49	62.0
132	60	132	0.07	7.61	5.42	0.04	1.51	59.4

Standby Input Power meets the < 100 mW requirement at 120 VAC

10.10 Standby Input Power at 300 mW Output Load

Standby input power was measured at 7.5V output voltage setting using a Yokogawa WT310E power meter. The power meter is set at no load or standby mode measurement setting in Figure 13.

Input		Input Measurement		Output 1 Measurement				Efficiency
Vac (rms)	Freq (Hz)	Vin (rms)	Pin (W)	Vo (V)	Io (mA)	Po (W)	%V Reg	
90	60	90.0	0.34	7.61	39.5	0.3	1.48	88.8
100	60	100	0.34	7.61	39.5	0.3	1.48	88.2
115	60	114	0.35	7.61	39.5	0.3	1.49	87.1
120	60	120	0.35	7.61	39.5	0.3	1.51	87.1
132	60	132	0.35	7.61	39.5	0.3	1.51	85.6

Standby Input Power meets the < 375 mW requirement at 120 VAC

10.11 Thermal Test

10.11.1 Thermal Scan at Room Ambient Temperature

The PSU was placed in a horizontal position inside an acrylic plastic housing. Thermal data were measured using a Flir IR camera.

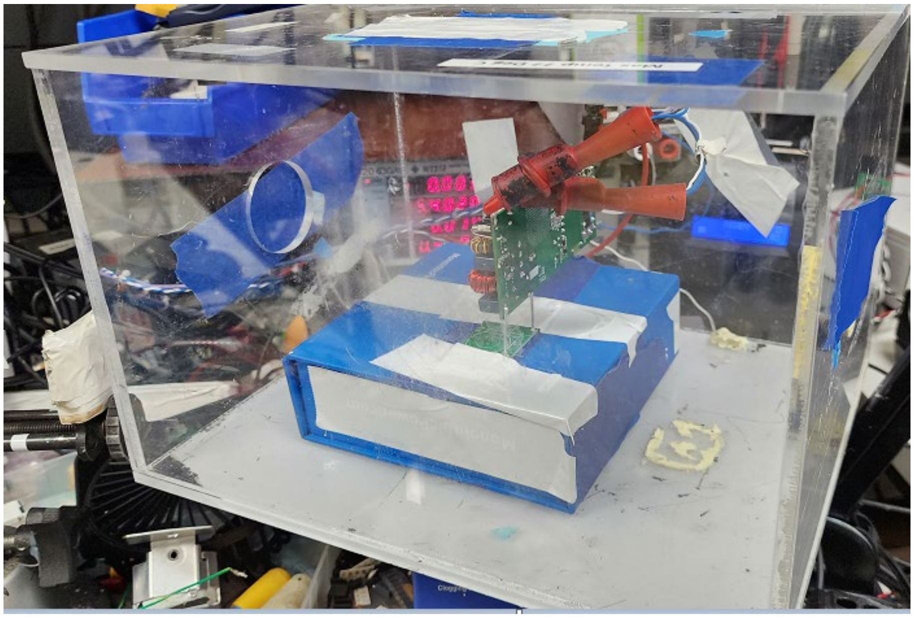


Figure 22 – Thermal Scan Test Set-up.

Thermal Scan Test Summary Data

Circuit Location	(°C)	
	90 VAC	**132 VAC**
	60 Hz	**60 Hz**
U8-Pri. (INNO4-QR)	79.8	82.4
U8-Sec. (INNO4-QR)	76.7	77.9
Q13/Q14-SRFET	75	77.2
D13/D12-Pri. Snubber	76.7	72.5
T1-Sec. Wire. (TRF)	86.9	88.8
T1- Ferrite Core. (TRF)	76.2	78.3
L2-(Input CMC)	101	68.2
BR1-(Bridge Diode)	85.9	67.3
L1-(HF Input CMC)	81	56.8
L3-(Diff. Choke)	77.6	61
Ambient Temperature	26	26

The components' temperatures are well within their thermal derating requirements.

10.11.2 Thermal Scan at 90 VAC 24 V / 5.4 A

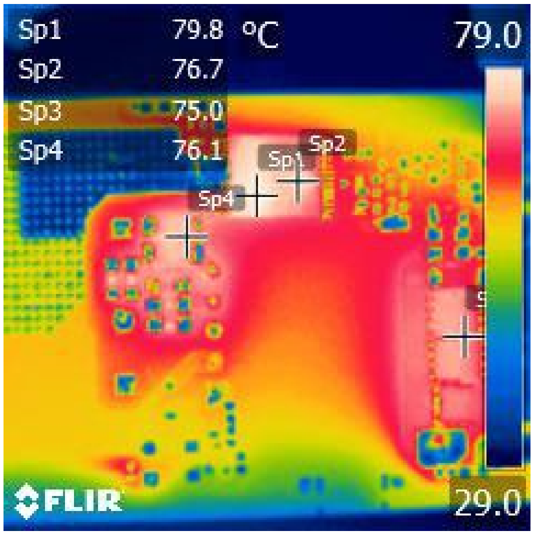


Figure 23 – Thermal Scan 90 V 24 V / 5.4 A.
Sp1: U8-Pri. (INNO4-QR): 79.8 °C
Sp2: U8-Sec. (INNO4-QR): 76.7 °C
Sp3: Q13/Q14-SRFET: 75 °C
Sp4: D13/D12-Pri. Snubber: 76.7 °C

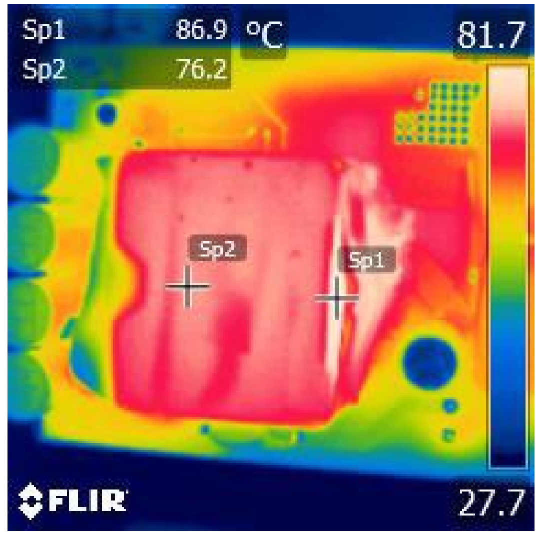


Figure 24 – Thermal Scan 90 V 24 V / 5.4 A
Sp1: T1-Sec. Wire. (TRF): 86.9 °C
Sp1: T1- Ferrite Core. (TRF): 76.2 °C

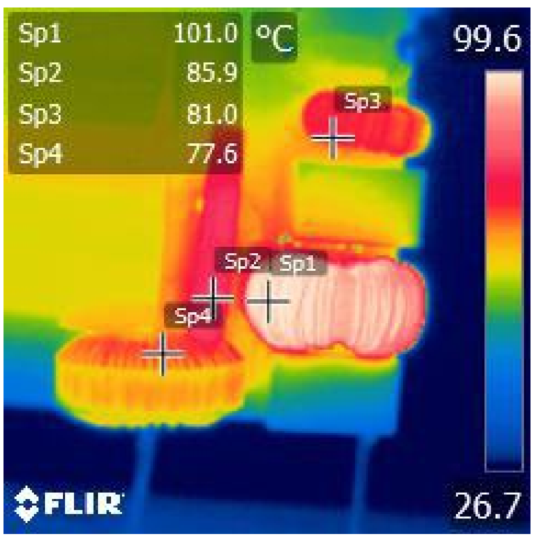


Figure 25 – Thermal Scan 90 V 24 V / 5.4 A.
Sp1: L2-(Input CMC): 101 °C
Sp2: BR1-(Bridge Diode): 85.9 °C
Sp3: L1-(HF Input CMC): 81 °C
Sp3: L3-(Diff. Choke): 77.6 °C

10.11.3 Thermal Scan at 132 VAC, 24 V / 5.4 A

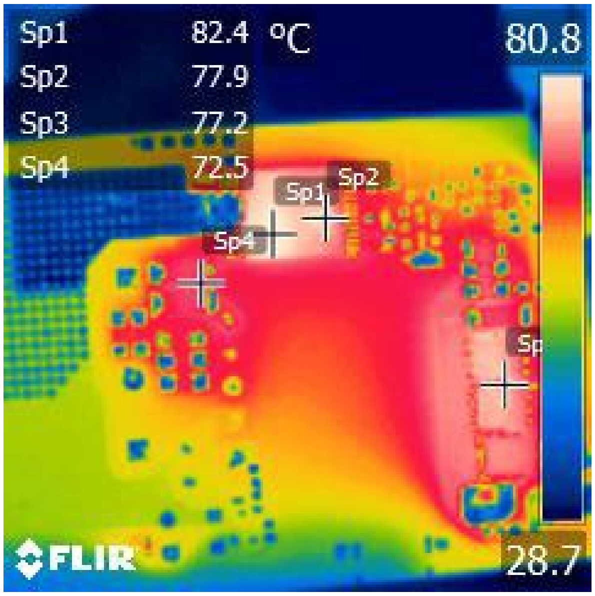


Figure 26 – Thermal Scan 132 VAC, 24 V / 5.4 A.
Sp1: U8-Pri. (INNO4-QR): 82.4 °C
Sp2: U8-Sec. (INNO4-QR): 77.9 °C
Sp3: Q13/Q14-SRFET: 77.2 °C
Sp4: D13/D12-Pri. Snubber: 72.5 °C

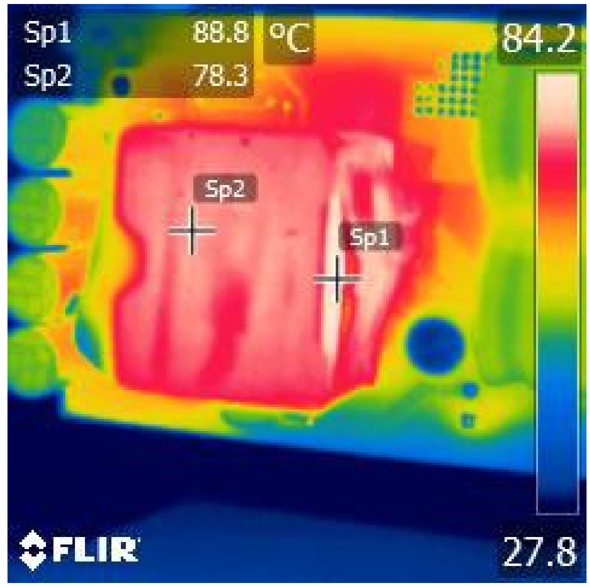


Figure 27 – Thermal Scan 132 VAC, 24 V / 5.4 A.
Sp1: T1-Sec. Wire. (TRF): 88.8 °C
Sp1: T1-Ferrite Core. (TRF): 78.3 °C

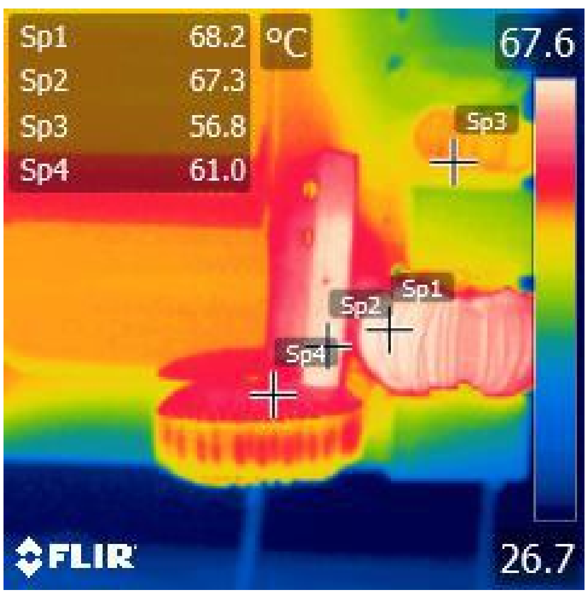
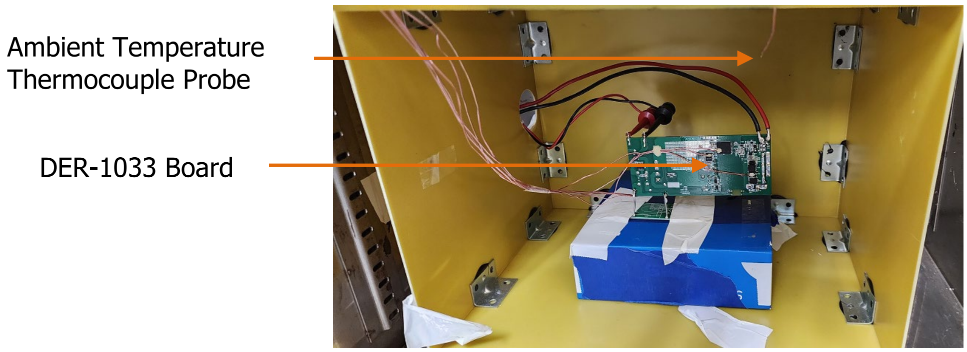


Figure 28 – Thermal Scan 132 VAC, 24 V / 5.4 A.
Sp1: L2-(Input CMC): 68.2 °C
Sp2: BR1-(Bridge Diode): 67.3 °C
Sp3: L1-(HF CMC): 56.8 °C
Sp4: L3-(Diff. Choke): 61 °C

10.11.4 Thermal Test at 55 °C Ambient

The PSU was placed in a horizontal position inside a closed box to prevent air flow from affecting the thermal measurement. Thermal data were measured using a thermocouple and a Yokogawa data logger.



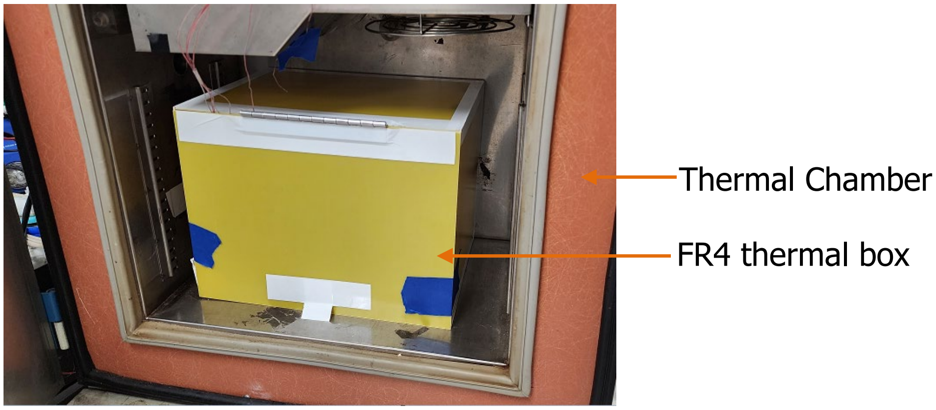


Figure 29 – Thermal Test Set-up.

Thermal Test Data

Circuit Location	(°C)	
	90 VAC 60 Hz	**132 VAC 60 Hz**
U8- Inno4-QR	104.9	106.9
Q13/Q14 - SRFET	101.2	103.5
D12/D13 - Snubber Diode	99.2	96.5
L2- Input CMC	115.1	91.6
T1 - Flyback TRF	103.3	106.3
BR1- Bridge Diode	103.9	90.2
Ambient Temperature	59.8	59.8

The components' temperatures are well within their thermal derating requirements.

11 Waveforms

11.1 Start-up Profile

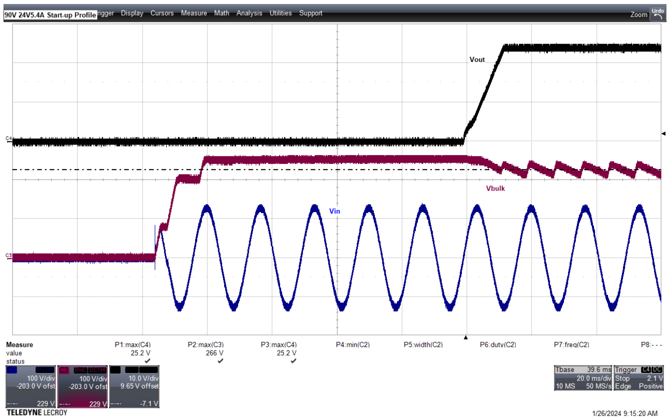


Figure 30 – Start-up Profile.
90 VAC, 24 V 5.4 A Start-up
Upper1: V_{OUT}, 10 V / div.
Uppe2: V_{BULK}, 100 V / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
$V_{BULK\ mean}$: 229 V; $t_{ON\ Delay}$: 100 ms

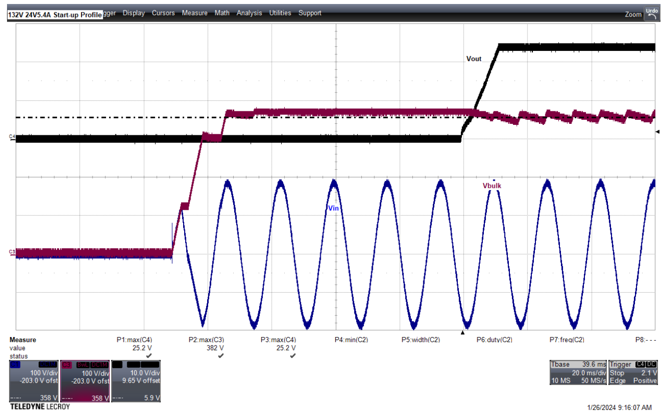


Figure 31 – Start-up Profile.
132 VAC, 24 V 5.4 A Start-up
Upper1: V_{OUT}, 10 V / div.
Uppe2: V_{BULK}, 100 V / div.
Lower: V_{IN}, 100 V / div., 20 ms / div.
$V_{BULK\ mean}$: 358 V; $t_{ON\ Delay}$: 90 ms

11.2 Primary Drain Voltage and Current

11.2.1 Primary Drain Voltage and Current at Steady State

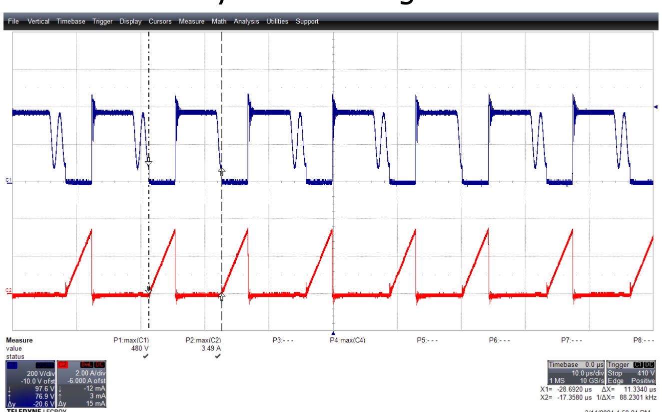


Figure 32 – Primary Drain Voltage and Current.
90 VAC, 24 V 5.4 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 10 us / div.
V_{DSMAX}: 480 V; I_{DSMAX}: 3.49 A

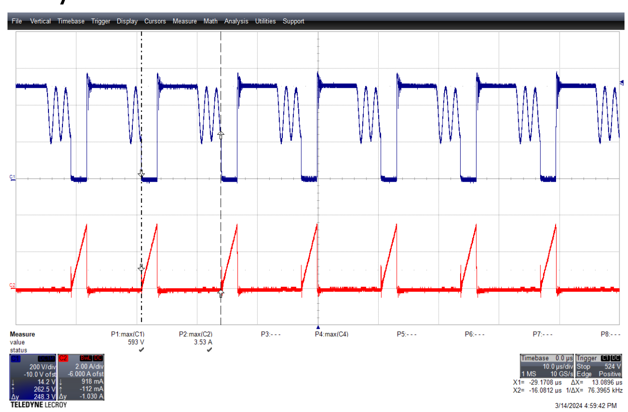


Figure 33 – Primary Drain Voltage and Current.
132 VAC, 24 V 5.4 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 10 us / div.
V_{DSMAX}: 593 V; I_{DSMAX}: 3.53 A

11.2.2 Primary Drain Voltage and Current at Start-up

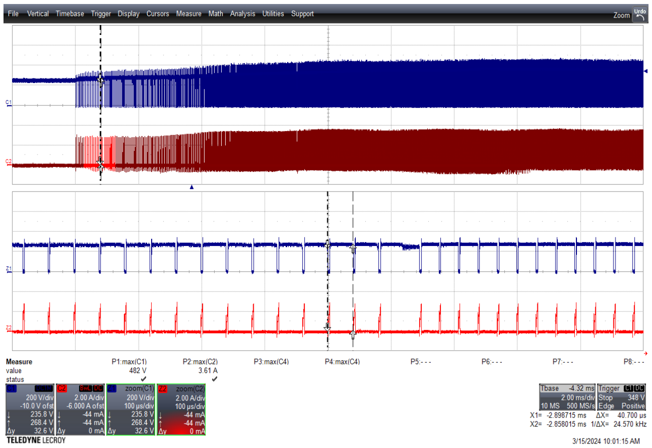


Figure 34 – Primary Drain Voltage and Current.
90 VAC, 24 V 5.4 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 2 ms / div.
V_{DSMAX}: 482 V; I_{DSMAX}: 3.61 A

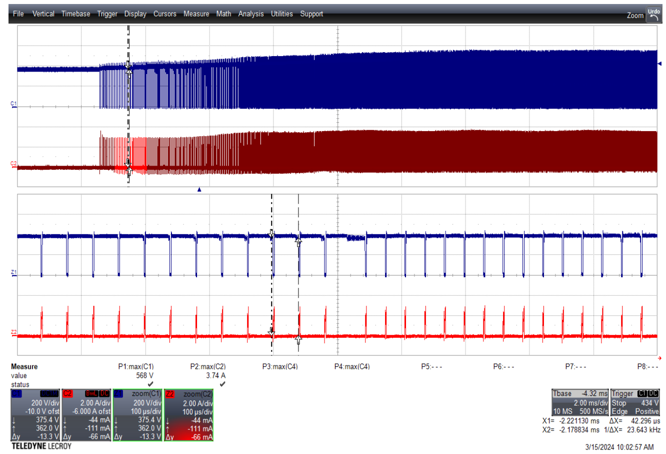


Figure 35 – Primary Drain Voltage and Current.
132 VAC, 24 V 5.4 A Start-up
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 2 ms / div.
V_{DSMAX}: 568 V; I_{DSMAX}: 3.74 A

11.2.3 Primary Drain Voltage and Current at Transient Load

Figure 36 – Primary Drain Voltage and Current.
90 VAC, 24 V 5.4 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 us / div.
V_{DSMAX}: 472 V; I_{DSMAX}: 4.68 A

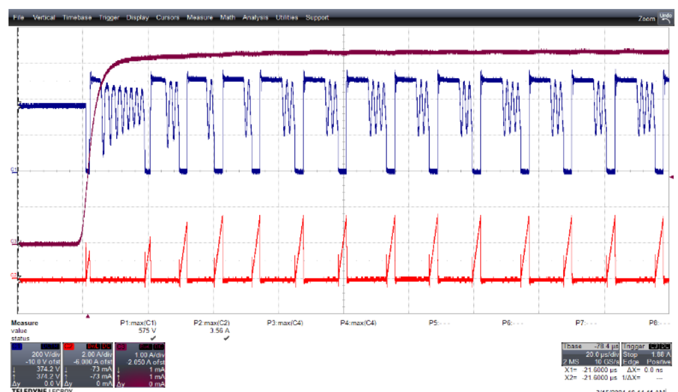


Figure 37 – Primary Drain Voltage and Current.
132 VAC, 24 V 5.4 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 us / div.
V_{DSMAX}: 575 V; I_{DSMAX}: 3.55 A

11.2.4 Primary Drain Voltage and Current at Peak Load

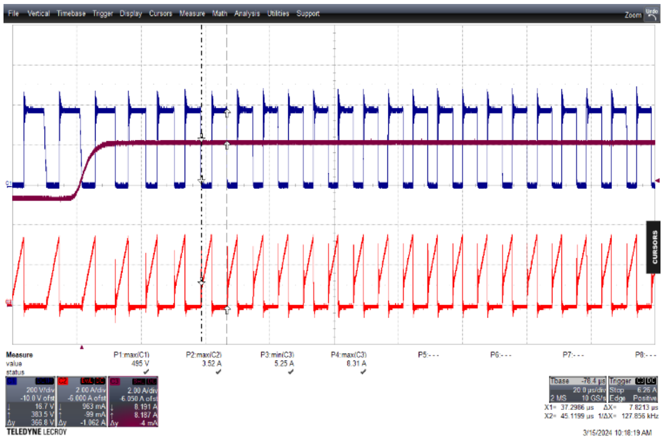


Figure 38 – Primary Drain Voltage and Current.
90 VAC, 24 V 5.4 A - 8.2 A Step Load
Upper1: I_{OUT}, 2 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 us / div.
V_{DSMAX}: 495 V; I_{DSMAX}: 3.52 A; I_{OMAX}: 8.31 A

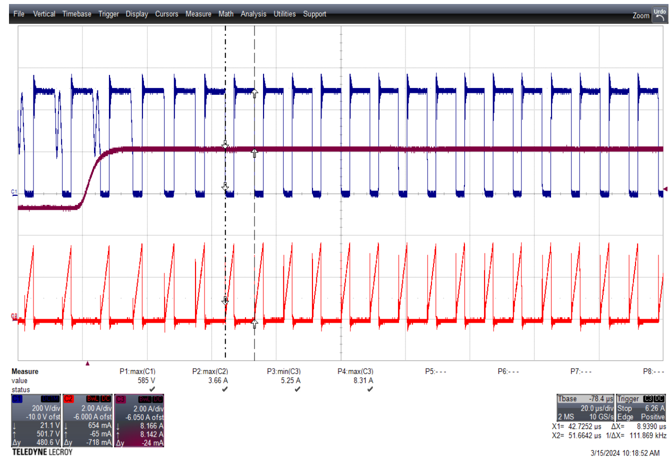


Figure 39 – Primary Drain Voltage and Current.
132 VAC, 24 V 5.4 A - 8.2 A Step Load
Upper1: I_{OUT}, 2 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 us / div.
V_{DSMAX}: 585 V; I_{DSMAX}: 3.66 A; I_{OMAX}: 8.31 A

11.2.5 Primary Drain Voltage and Current at Peak Transient Load

Figure 40 – Primary Drain Voltage and Current.
90 VAC, 24 V 0 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 200V / div.
V_{DSMAX}: 509 V

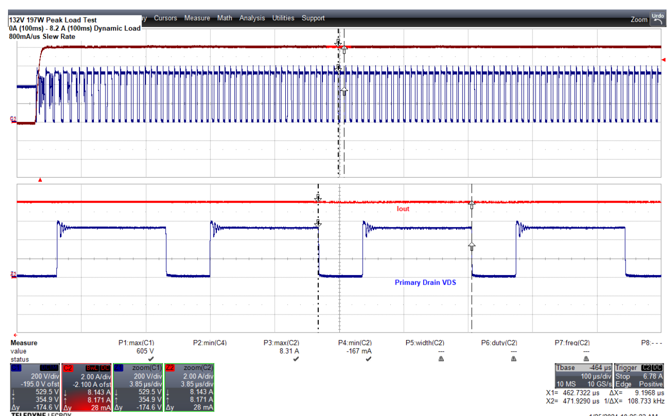


Figure 41 – Primary Drain Voltage and Current.
132 VAC, 24 V 0 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 200V / div.
V_{DSMAX}: 605 V

11.2.6 Primary Drain Voltage and Current During Output Short Circuit

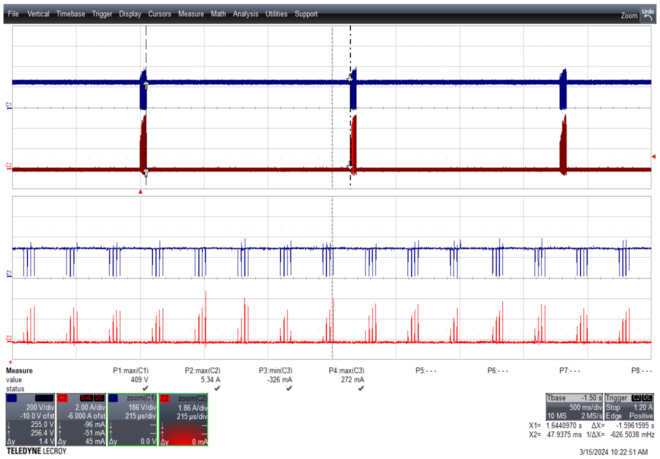


Figure 42 – Primary Drain Voltage and Current.
90 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 500 ms / div.
V_{DSMAX}: 409 V; I_{DSMAX}: 5.34 A

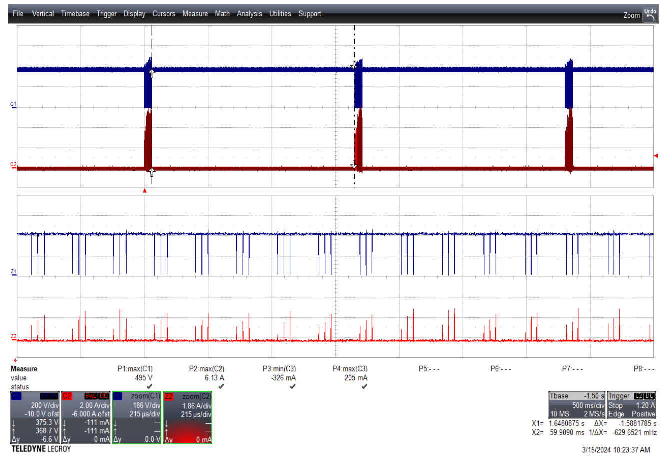


Figure 43 – Primary Drain Voltage and Current.
132 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 500 ms / div.
V_{DSMAX}: 495 V; I_{DSMAX}: 6.13 A

11.3 SR FET Voltage

11.3.1 SR FET Voltage at Full Load Steady State

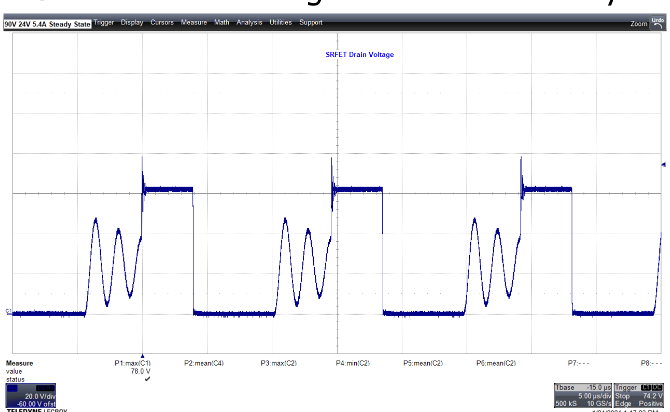


Figure 44 – SR FET Drain Voltage.
90 VAC, 24 V 5.4 A Steady-State
Lower: V_{DS}, 20V / div., 5 us / div.
V_{DSMAX}: 78 V

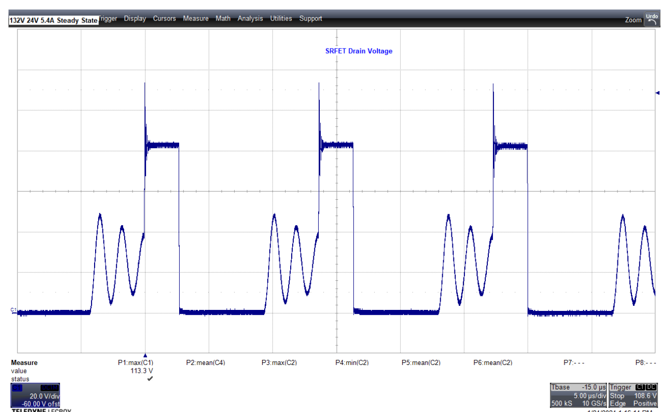


Figure 45 – SR FET Drain Voltage.
132 VAC, 24 V 5.4 A Steady-State
Lower: V_{DS}, 20V / div., 5 us / div.
V_{DSMAX}: 113.3 V

11.3.2 SR FET Voltage at Full Load Start-up

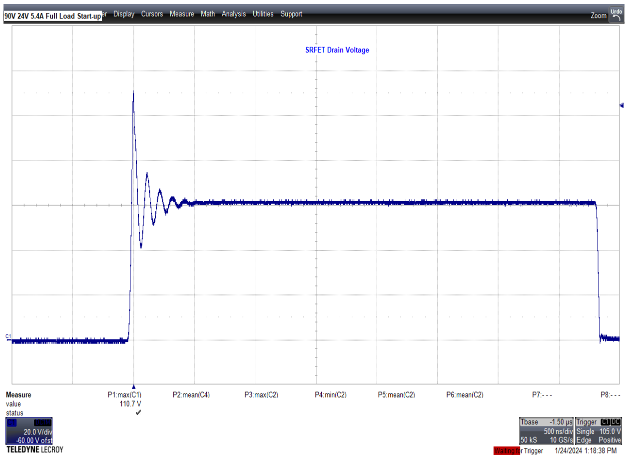


Figure 46 – SR FET Drain Voltage.
90 VAC, 24 V 5.4 A Start-up
Lower: V_{DS}, 20V / div., 500 ns / div.
V_{DSMAX}: 110.7 V

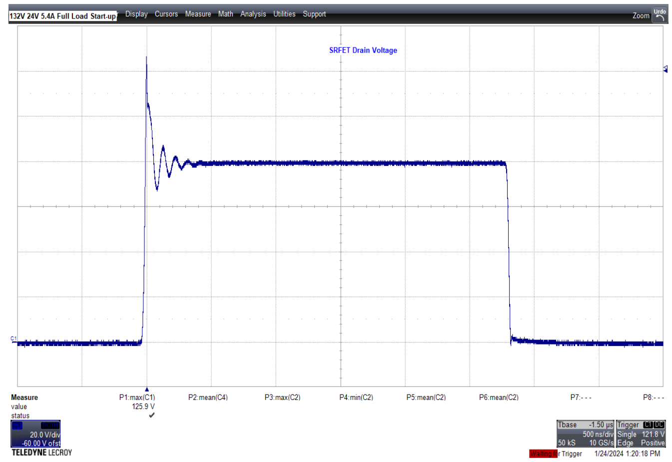


Figure 47 – SR FET Drain Voltage.
132 VAC, 24 V 5.4 A Start-up
Lower: V_{DS}, 20V / div., 500 ns / div.
V_{DSMAX}: 125.9 V

11.3.3 SR FET Voltage at Transient Load

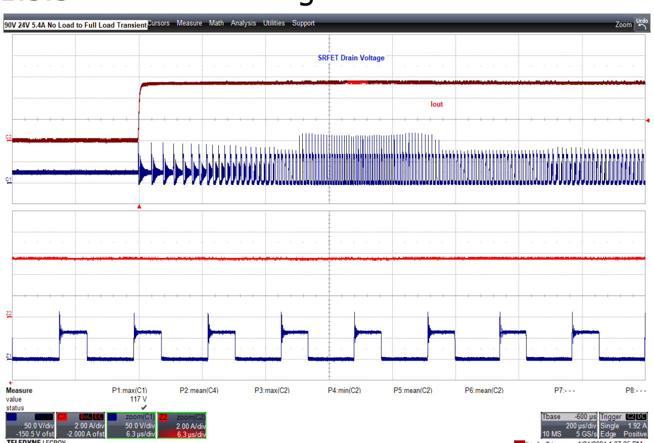


Figure 48 – SR FET Drain Voltage.
90 VAC, 24 V 0 A - 5.4 A Step Load
Upper: I_{OUT}, 2 A / div., 200 us / div.
Lower: V_{DS}, 50V / div.
V_{DSMAX}: 117 V

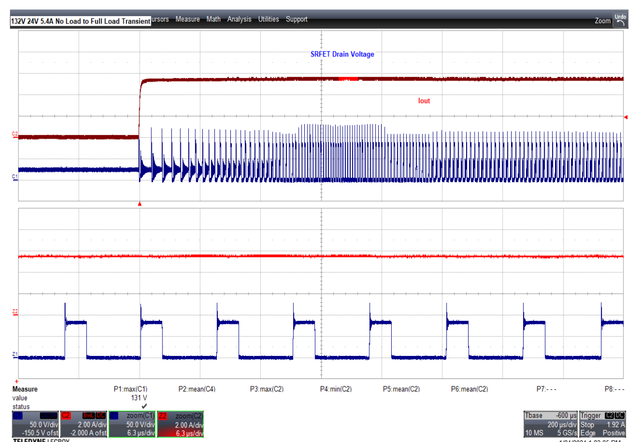


Figure 49 – SR FET Drain Voltage.
132 VAC, 24 V 0 A - 5.4 A Step Load
Upper: I_{OUT}, 2 A / div., 200 us / div.
Lower: V_{DS}, 50V / div.
V_{DSMAX}: 131 V

11.3.4 SR FET Voltage at Peak Load

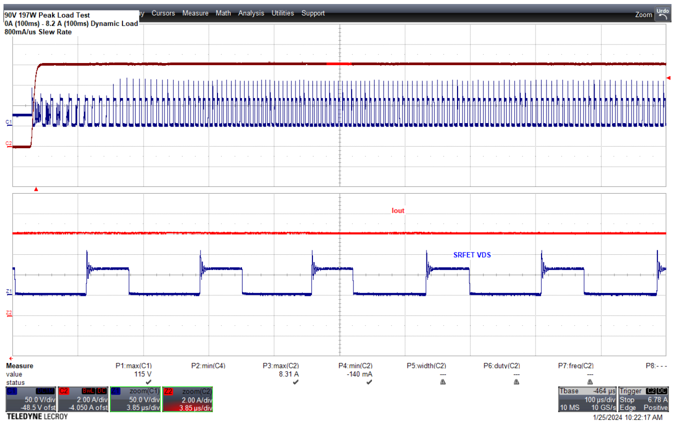


Figure 50 – SR FET Drain Voltage.
90 VAC, 24 V 0 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 50V / div.
V_{DSMAX}: 115 V

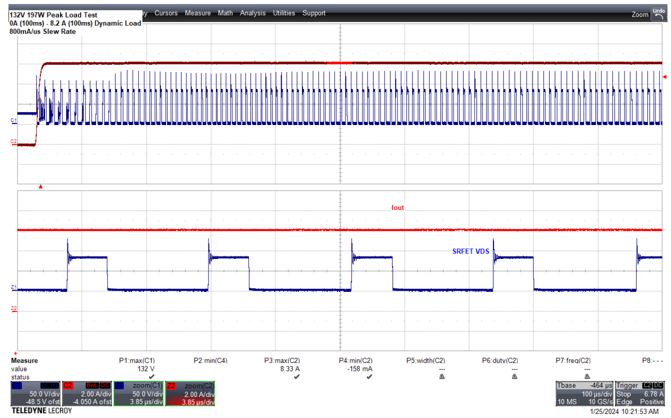


Figure 51 – SR FET Drain Voltage.
132 VAC, 24 V 0 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 50V / div.
V_{DSMAX}: 132 V

11.4 Input Bulk Voltage Waveform

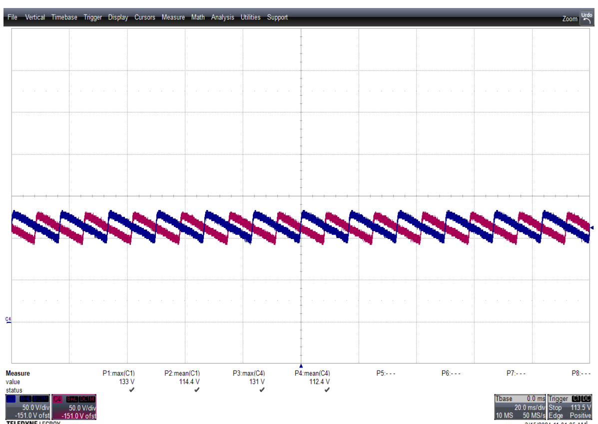


Figure 52 – Input Bulk Voltage.
90 VAC, 24 V 5.4 A Steady State
Upper: V_{C4}, 50 V / div., 20 ms / div.
Lower: V_{C5}, 50 V / div.
$V_{C4\ MEAN}$: 114.4 V, $V_{C5\ MEAN}$: 112.4 V

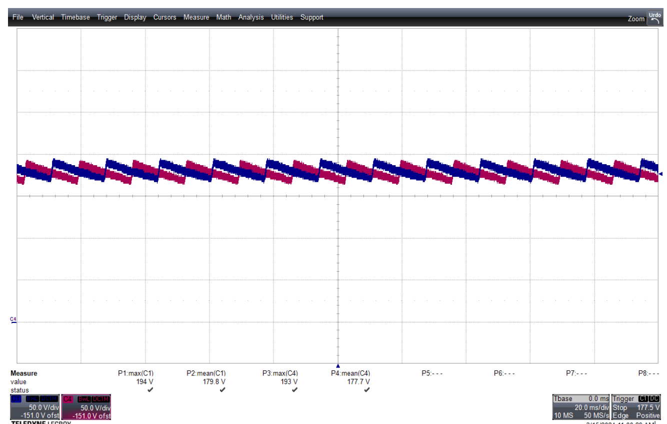


Figure 53 – Input Bulk Voltage.
132 VAC, 24 V 5.4 A Steady State
Upper: V_{C4}, 50 V / div., 20 ms / div.
Lower: V_{C5}, 50 V / div.
$V_{C4\ MEAN}$: 179.9 V, $V_{C5\ MEAN}$: 177.7 V

11.5 Load Transient Response

Output voltage was measured at the PSU output terminals T3 and T4.

11.5.1 0% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/µs.

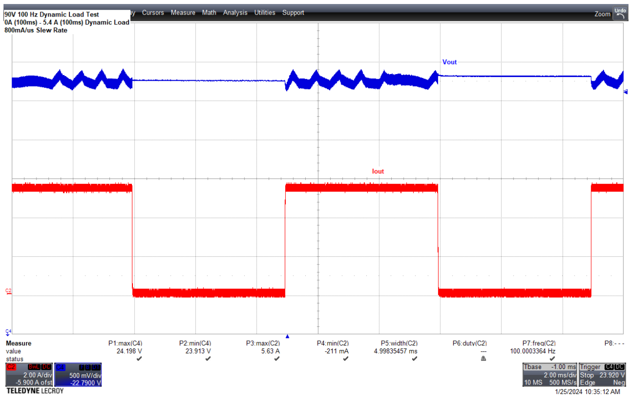


Figure 54 – (0% - 100%) Load Transient
90 VAC, 24 V 0 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.1 V; V_{OMAX}: 24.2 V

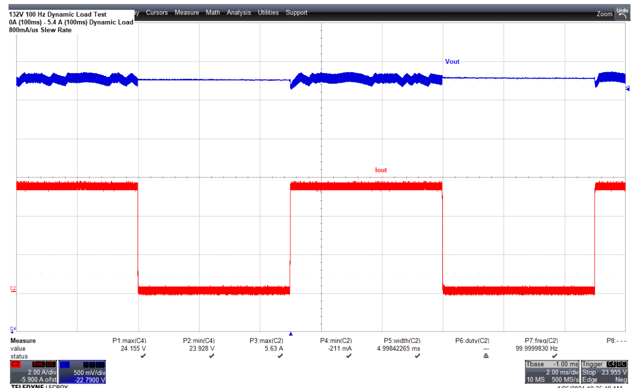


Figure 55 – (0% - 100%) Load Transient
132 VAC, 24 V 0 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.9 V; V_{OMAX}: 24.2 V

11.5.2 10% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0.54 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/µs.

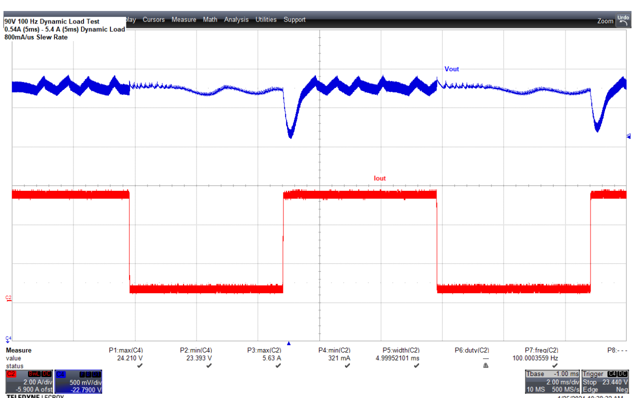


Figure 56 – (10% - 100%) Load Transient
90 VAC, 24 V 0.54 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.4 V; V_{OMAX}: 24.2 V

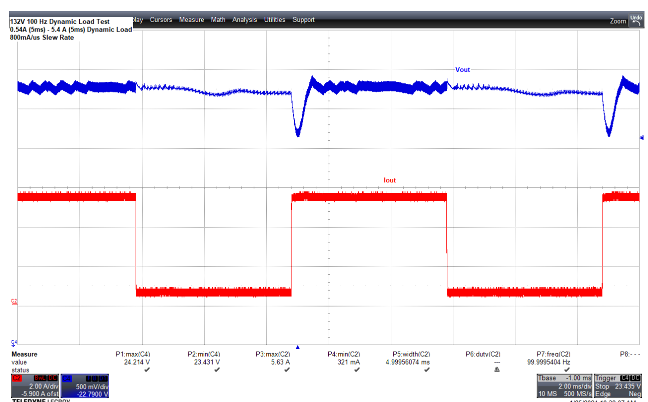


Figure 57 – (10% - 100%) Load Transient
132 VAC, 24 V 0.54 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.4 V; V_{OMAX}: 24.2 V

11.5.3 50% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 2.7 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/µs.

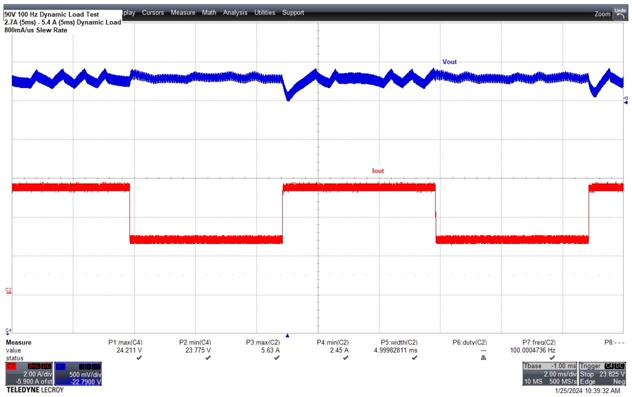


Figure 58 – (50% - 100%) Load Transient.
90 VAC, 24 V 2.7 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.2 V

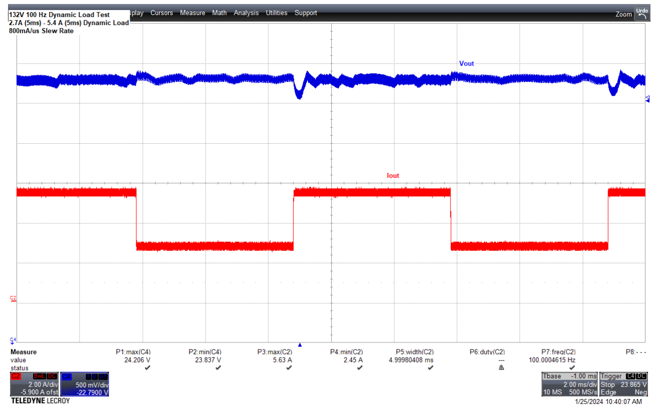


Figure 59 – (50% - 100%) Load Transient.
132 VAC, 24 V 2.7 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 500 mV / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.2 V

11.6 Peak Load Test

Output voltage was measured at the PSU output terminals T3 and T4.

11.6.1 0 A – 8.2 A Peak Load Transient

Set-up: 5 Hz dynamic load using Chroma 63113A E-load. 0 A – 8.2 A with 50% duty cycle and load current slew rate of 800 mA/µs.

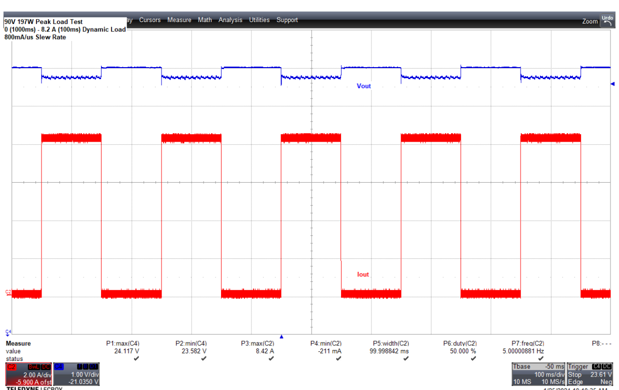


Figure 60 – (0 A – 8.2) A Load Transient.
90 VAC, 24 V 0 A – 8.2 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.6 V; V_{OMAX}: 24.1 V

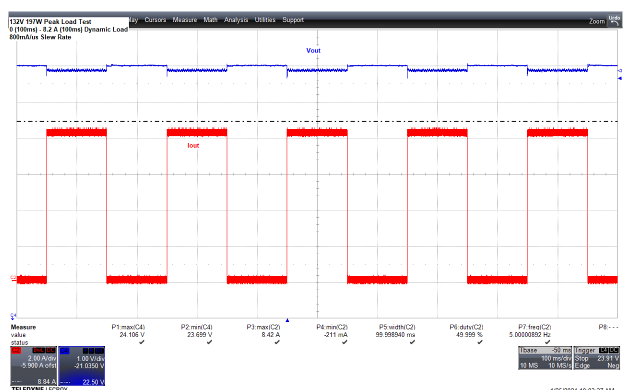


Figure 61 – (0 A – 8.2 A) Load Transient.
132 VAC, 24 V 0 A – 8.2 A Dynamic Load
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.7 V; V_{OMAX}: 24.1 V

11.6.2 5.4 A – 8.2 A Peak Load Transient

Set-up: 5 Hz dynamic load using Chroma 63113A E-load. 5.4 A – 8.2 A with 50% duty cycle and load current slew rate of 800 mA/µs.

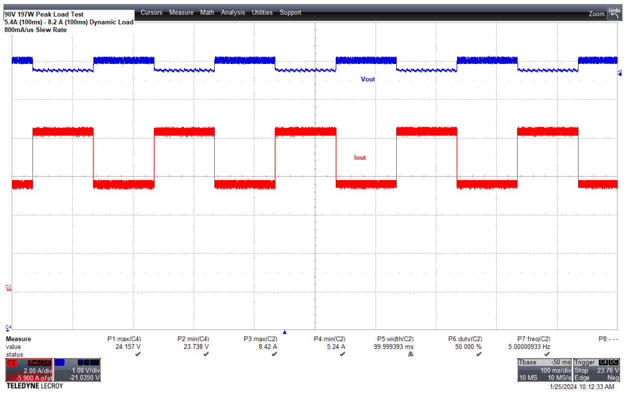


Figure 62 – (5.4 A – 8.2) A Load Transient
90 VAC, 24 V 5.4 A – 8.2 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.7 V; V_{OMAX}: 24.2 V

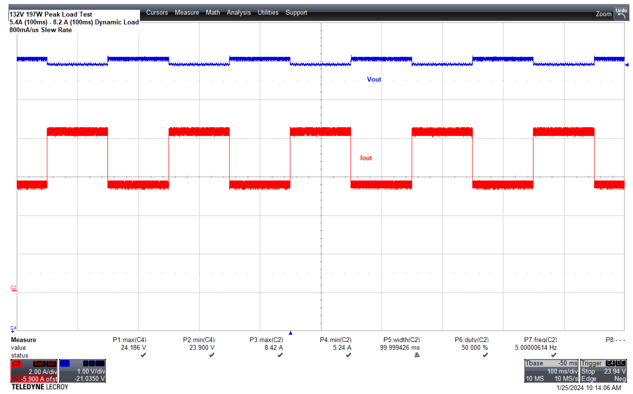


Figure 63 – (5.4 A – 8.2 A) Load Transient
132 VAC, 24 V 5.4 A – 8.2 A Dynamic Load
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.9 V; V_{OMAX}: 24.2 V

11.7 Overcurrent Protection Test

Using an E-load, the output load current is increased until the output voltage and current collapse.

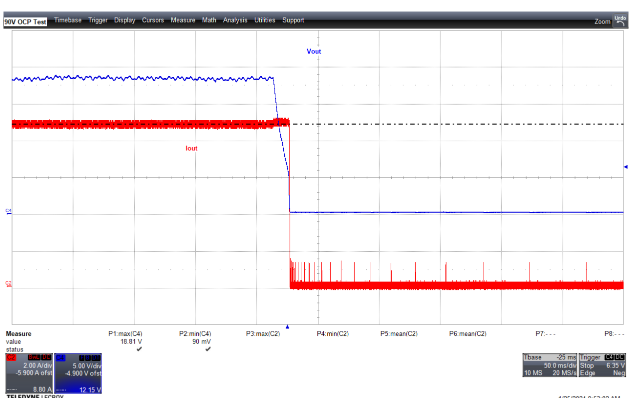


Figure 64 – Over Current Test
90 VAC, 24 V 5.4 A – OCP point.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 50 ms / div.
I_{OCP}: 8.8 A

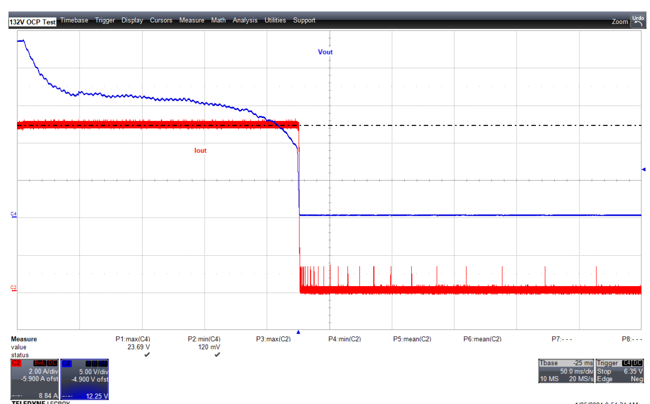


Figure 65 – Over Current Test
132 VAC, 24 V 5.4 A – OCP point.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 50 ms / div.
I_{OCP}: 8.84 A

11.8 Output Ripple Measurements

11.8.1 Ripple Measurement Technique

To conduct output ripple measurements, a modified oscilloscope test probe must be used to reduce spurious signals caused by noise pickup.

The 4987BA probe adapter is equipped with two capacitors connected in parallel across the probe tip. These capacitors consist of one (1) 0.1 µF/50 V ceramic type and one (1) 10 µF/50 V aluminum electrolytic type. Since the aluminum electrolytic capacitor is polarized, proper polarity must be maintained across DC outputs (refer to the diagram below).

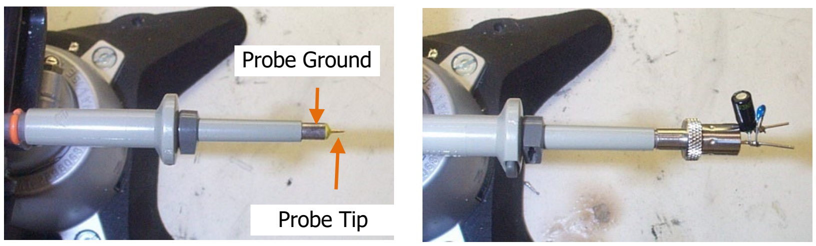


Figure 66 – Ripple voltage probe using Probe Master 4987A BNC Adapter.

11.8.2 Output ripple voltage at 90 VAC

Note: The output ripple voltage was measured at room ambient temperature at the end of a 100 mΩ output cable.

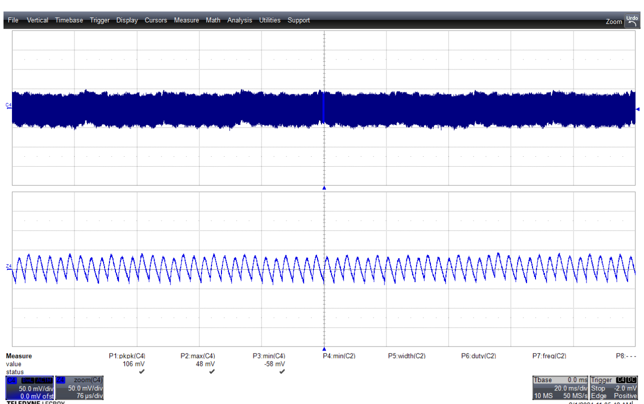


Figure 67 – Ripple Voltage, 100% Load.
90 VAC, 24 V 5.4 A Steady State.
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 106 mVp-p

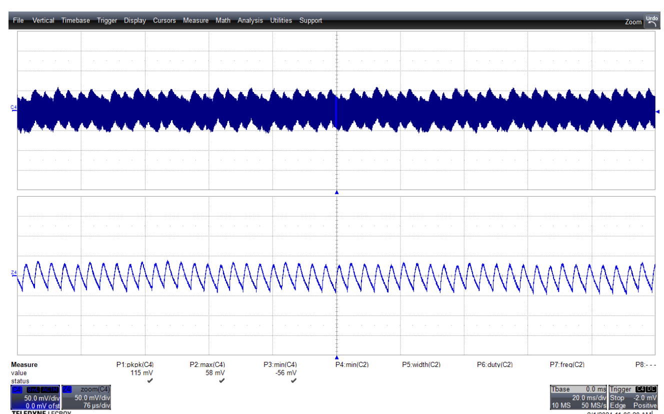


Figure 68 – Ripple Voltage, 75% Load.
90 VAC, 24 V 4.05 A Steady State
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 115 mVp-p

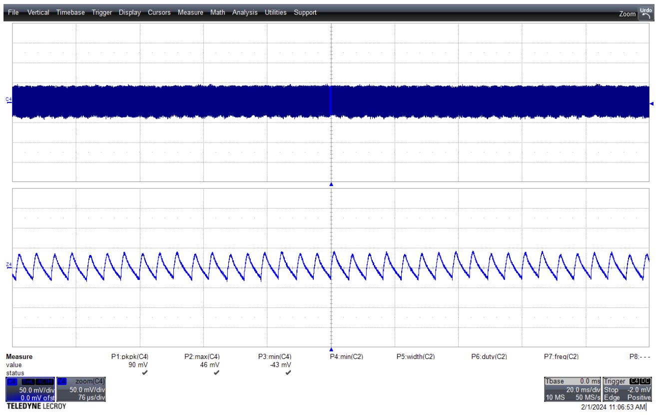


Figure 69 – Ripple Voltage, 50% Load.
90 VAC, 24 V 2.7 A Steady State
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 90 mVp-p

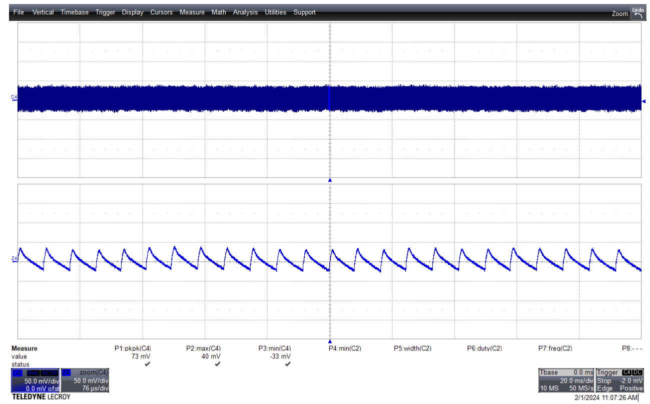


Figure 70 – Ripple Voltage, 25% Load.
90 VAC, 24 V 1.35 A Steady State
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 73 mVp-p

11.8.3 Output ripple voltage at 132 VAC

Note: The output ripple voltage was measured at room ambient temperature at the end of a 100 mΩ output cable.

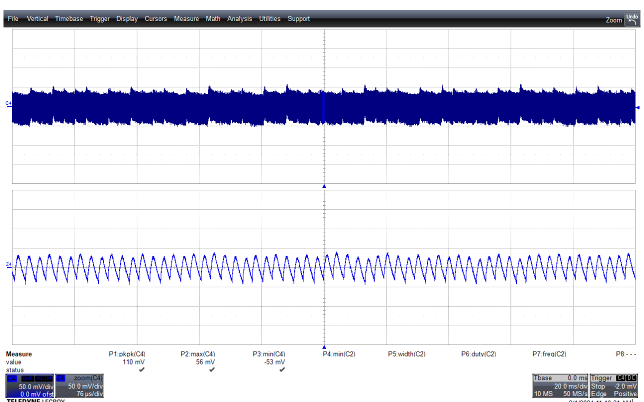


Figure 71 – Ripple Voltage, 100% Load.
132 VAC, 24 V 5.4 A Steady State.
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 110 mVp-p

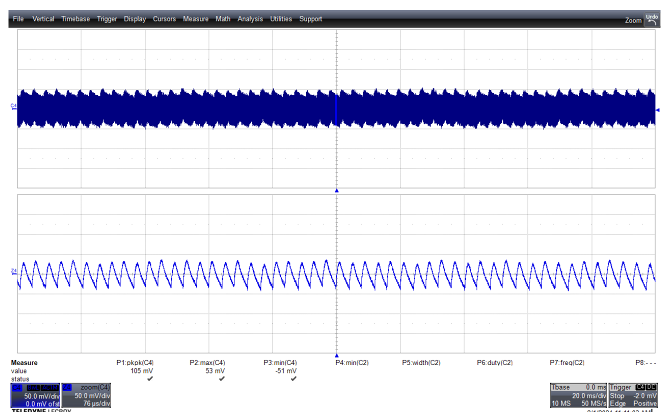


Figure 72 – Ripple Voltage, 75% Load.
132 VAC, 24 V 4.05 A Steady State
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 105 mVp-p

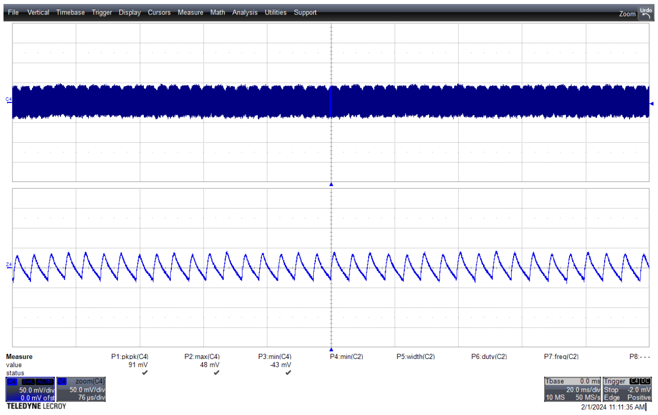


Figure 73 – Ripple Voltage, 50% Load
132 VAC, 24 V 2.7 A Steady State.
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 91 mVp-p

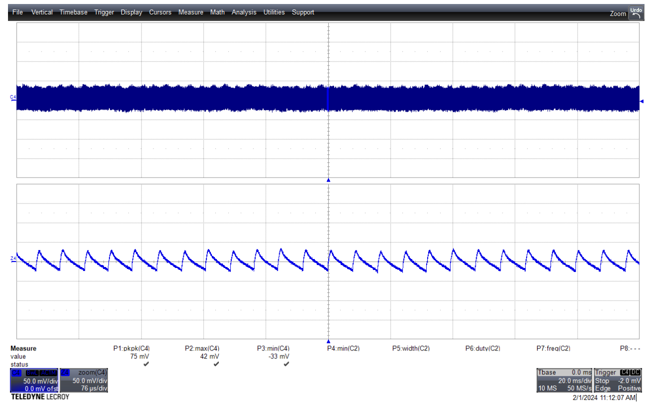


Figure 74 – Ripple Voltage, 25% Load
132 VAC, 24 V 1.35 A Steady State.
V_{RIPPLE}: 50 mV / div., 20 ms / div.
V_{RIPPLE}: 75 mVp-p

12 Conducted EMI

EMI scans are measured using 4.44 Ω fixed resistor load.

12.1 Test Set-up

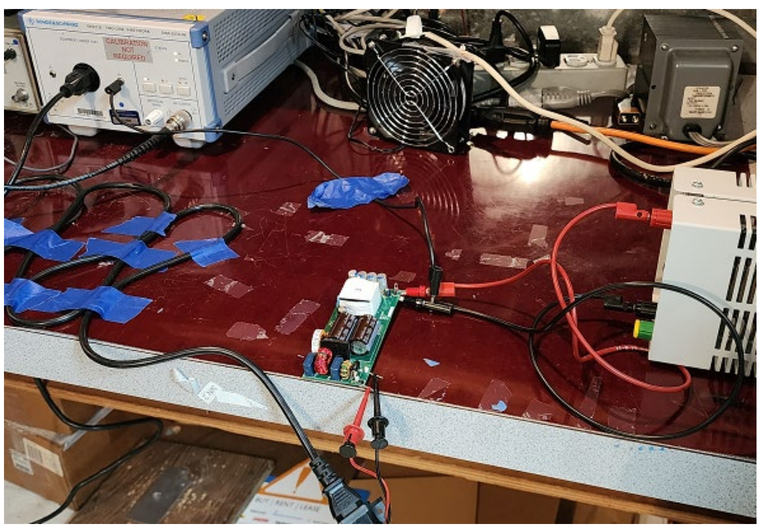


Figure 75 – Conducted EMI Test Set-up

12.2 Floating Output Load Resistor

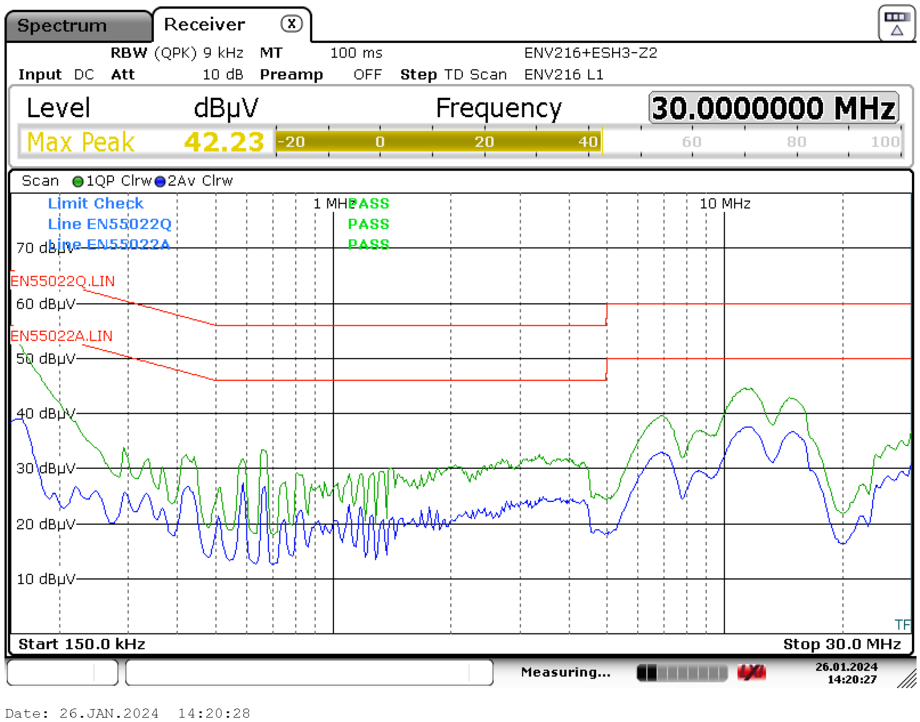


Figure 76 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Floating), 115 VAC Line 1.

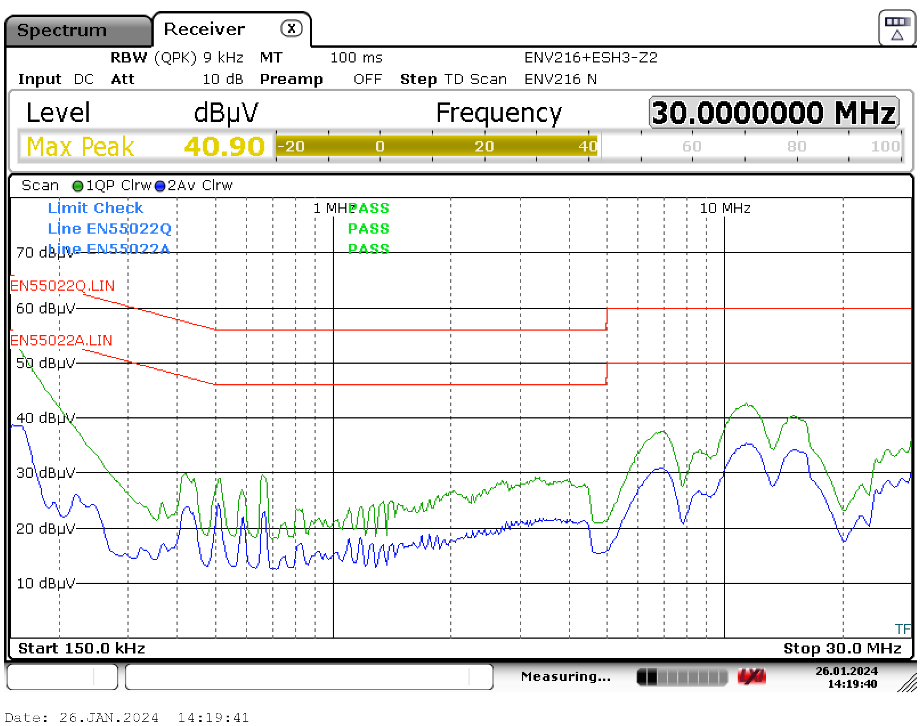
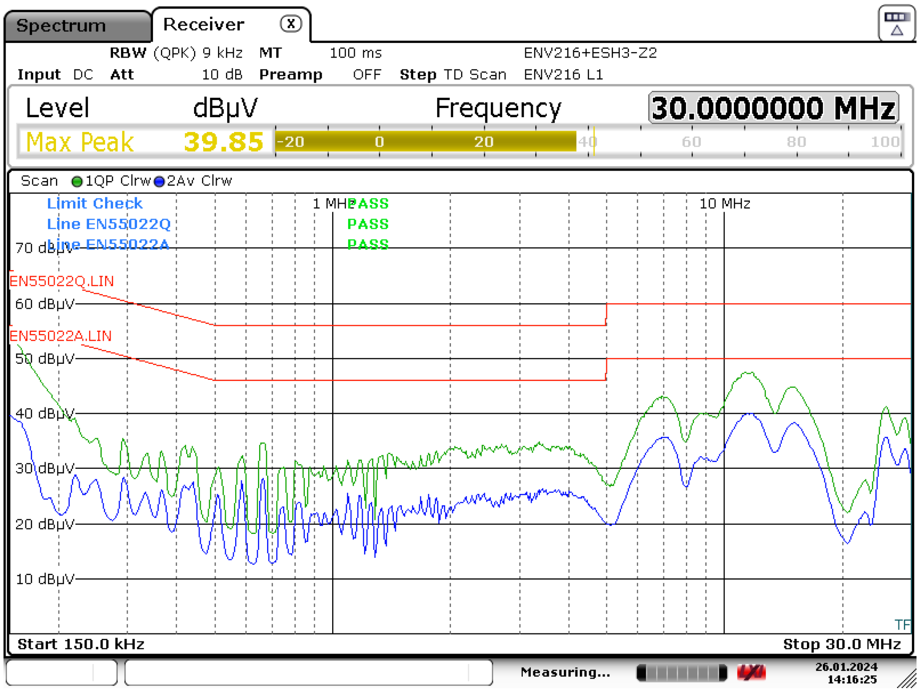


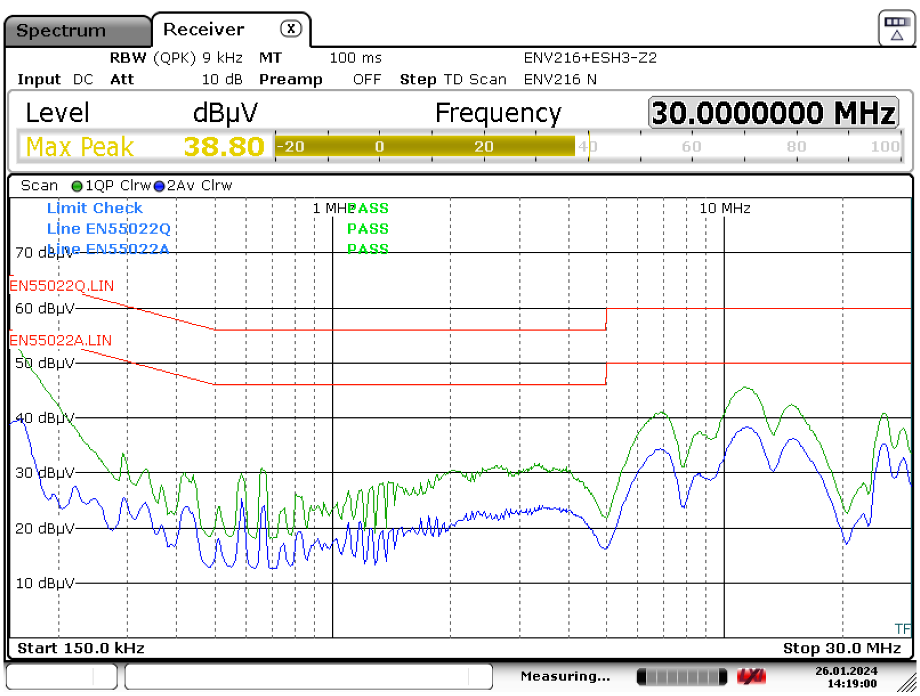
Figure 77 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Floating), 115 VAC Neutral.

12.3 Grounded Output Load Resistor



Date: 26.JAN.2024 14:16:25

Figure 78 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Grounded), 115 VAC Line 1.



Date: 26.JAN.2024 14:19:00

Figure 79 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Grounded), 115 VAC Neutral.

13 Line Surge

ESD was tested at 24 V output setting. Pass criterion is no permanent output interruption.

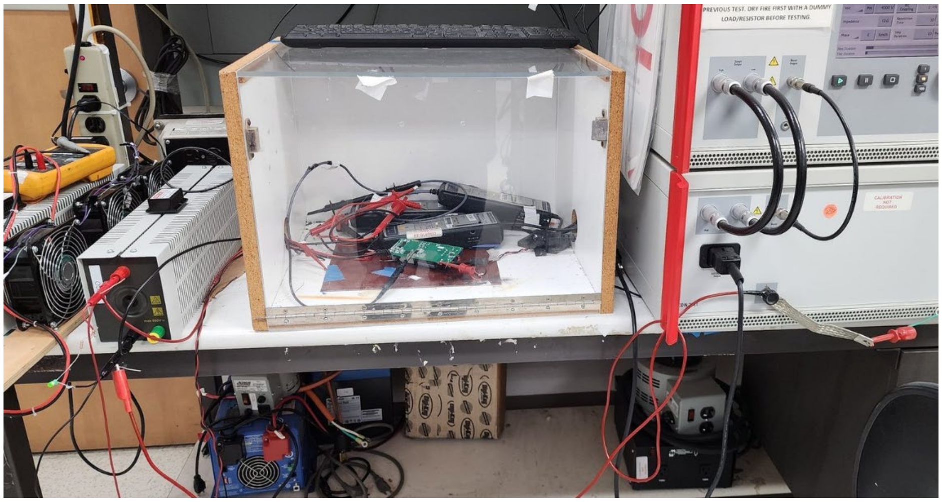


Figure 80 – Line Surge Test Set-up.

13.1 Combination Wave Differential Mode Test

Pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+2.5	90	2	10	PASS
115	-2.5	90	2	10	PASS
115	+2.5	270	2	10	PASS
115	-2.5	270	2	10	PASS
115	+2.5	0	2	10	PASS
115	-2.5	0	2	10	PASS

13.2 Ring Wave Surge

ESD was tested at 24 V output setting. Pass criterion is no permanent output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+2	90	12	10	PASS
115	-2	90	12	10	PASS
115	+2	270	12	10	PASS
115	-2	270	12	10	PASS
115	+2	0	12	10	PASS
115	-2	0	12	10	PASS

14 Electrostatic Discharge Test (ESD)

ESD testing was conducted at the 24 V output setting. The pass criterion is the absence of permanent output interruption.

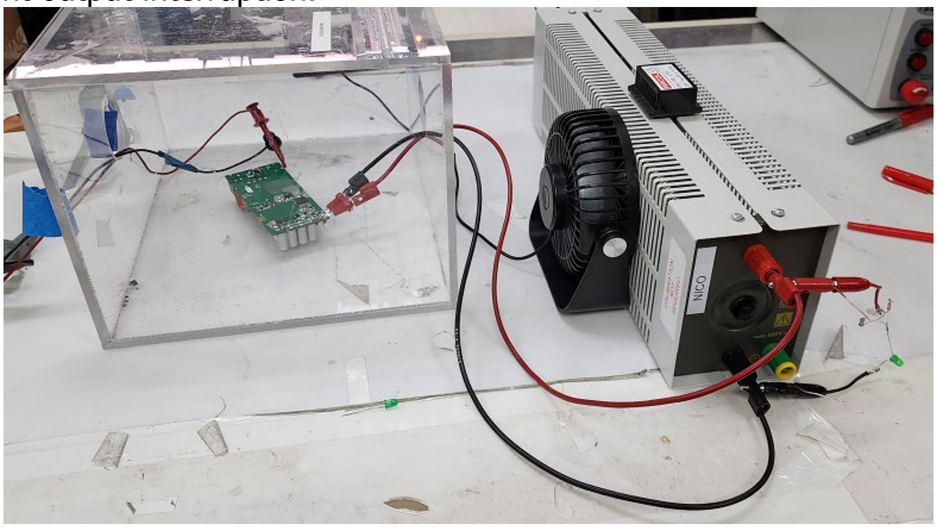


Figure 81 – ESD Test Set-up.

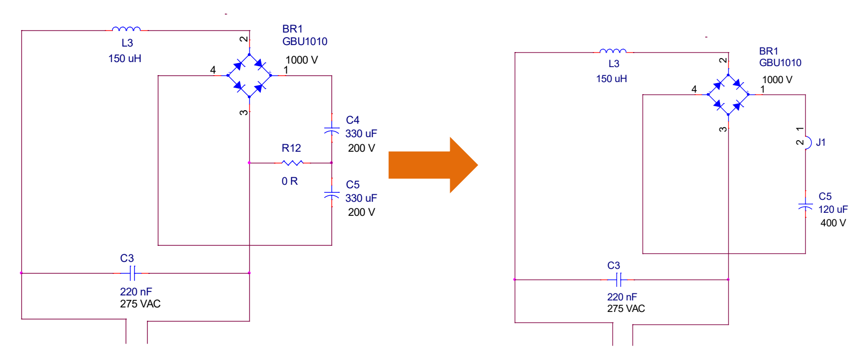
14.1 Air Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
115	+8	Output +	10	PASS
115	-8	Output +	10	PASS
115	+10	Output -	10	PASS
115	-10	Output -	10	PASS
115	+12	Output -	10	PASS
115	-12	Output -	10	PASS
115	+15	Output +	10	PASS
115	-15	Output +	10	PASS
115	+16.5	Output -	10	PASS
115	-16.5	Output -	10	PASS

15 Appendix

15.1 Procedure to Configure the DER-1033 Board for High Input Line Range of 185 VAC – 265 VAC

1. Remove C4
2. Connect a jumper wire, J1, across C4
3. Remove R12
4. Replace C5 with 120 uF / 400 V electrolytic capacitor.



LOW LINE ONLY
90 VAC – 132 VAC

HIGH LINE ONLY
185 VAC – 265 VAC

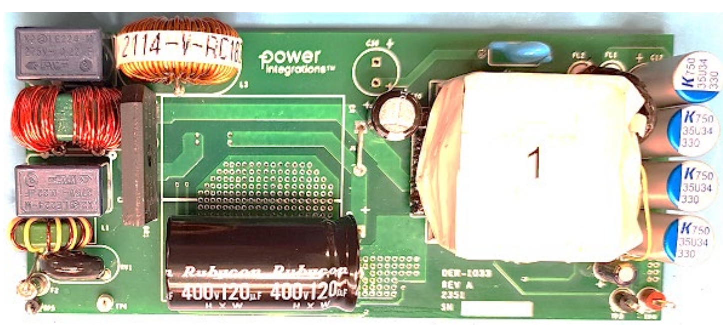


Figure 82 – Modified Board for High line (185 VAC – 265 VAC).

15.2 High Line Only Performance Data

15.2.1 Efficiency at 24 V Full Load

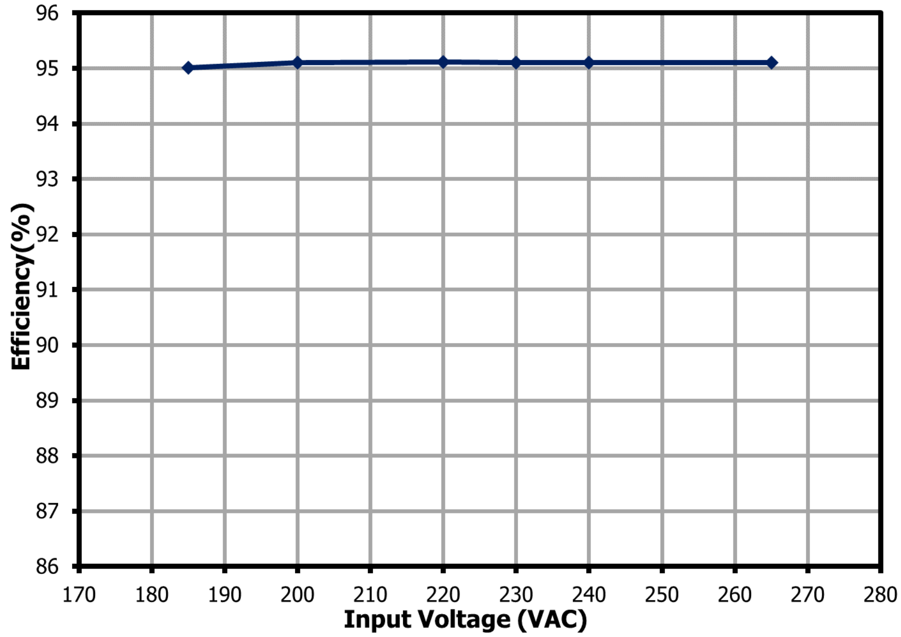


Figure 83 – Efficiency vs. Input Line Voltage, 24 V Output.

15.2.2 No-Load Input Power

No load input power was measured at 7.5 V output setting using a Yokogawa WT310E power meter at room ambient temperature.

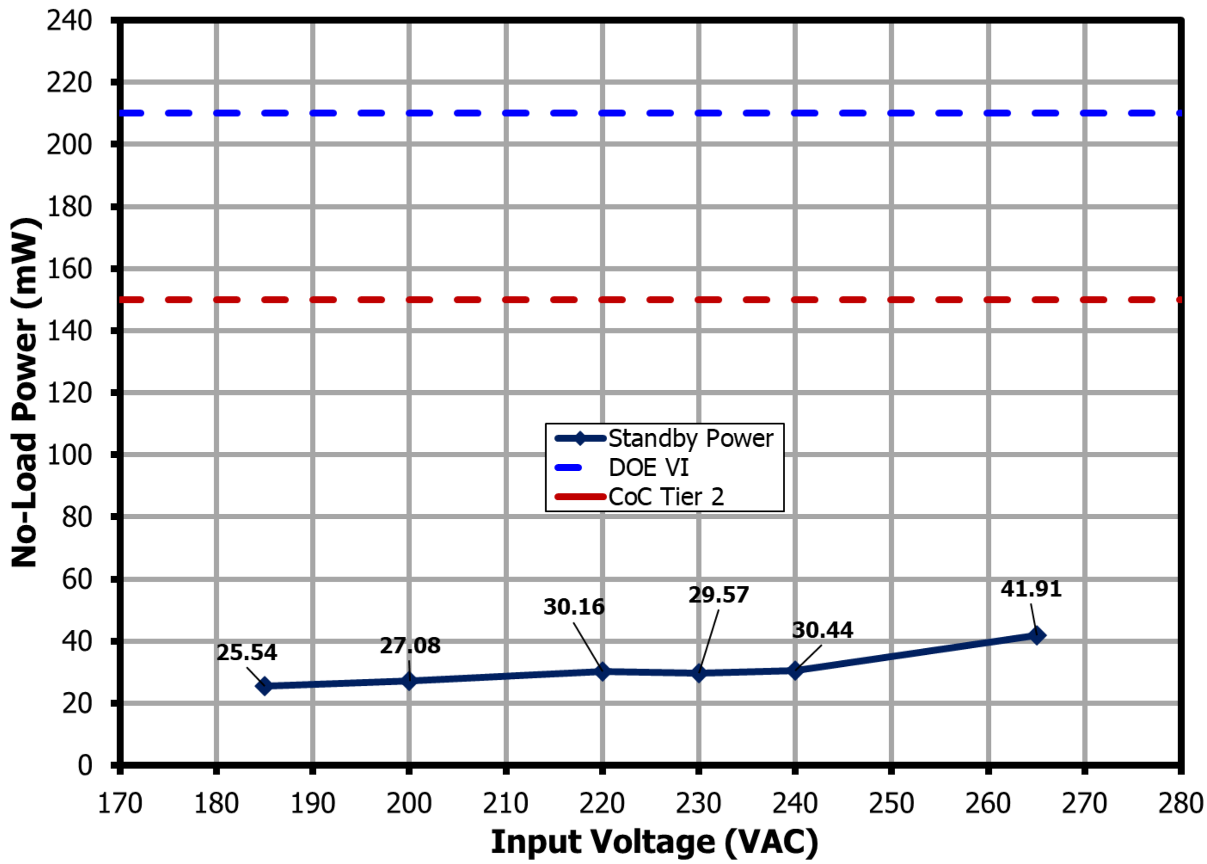


Figure 84 – No-Load Input Power vs. Input Line Voltage.

15.2.3 Average Efficiency at 230 VAC

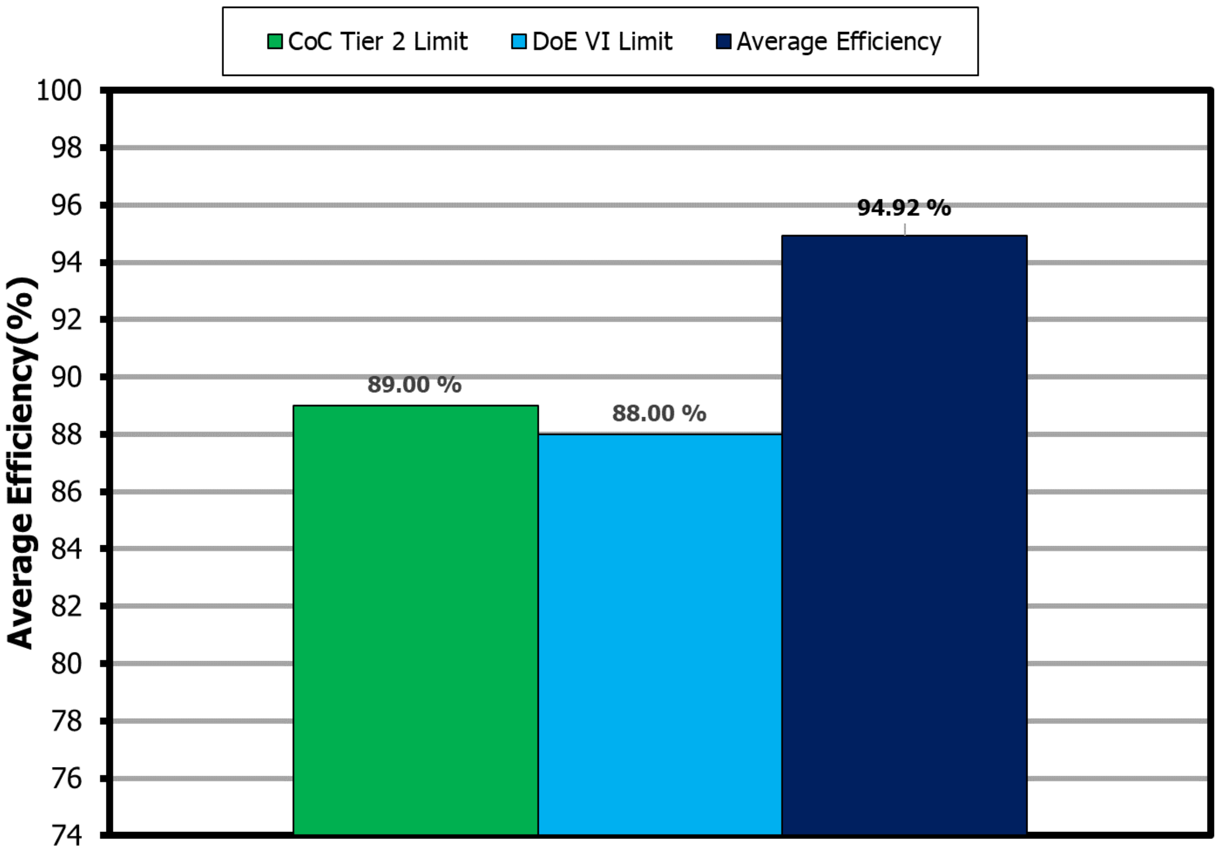


Figure 85 – Average Efficiency at 230 VAC, 24 V Output Voltage.

15.2.4 Efficiency at 10% Load, 230 VAC

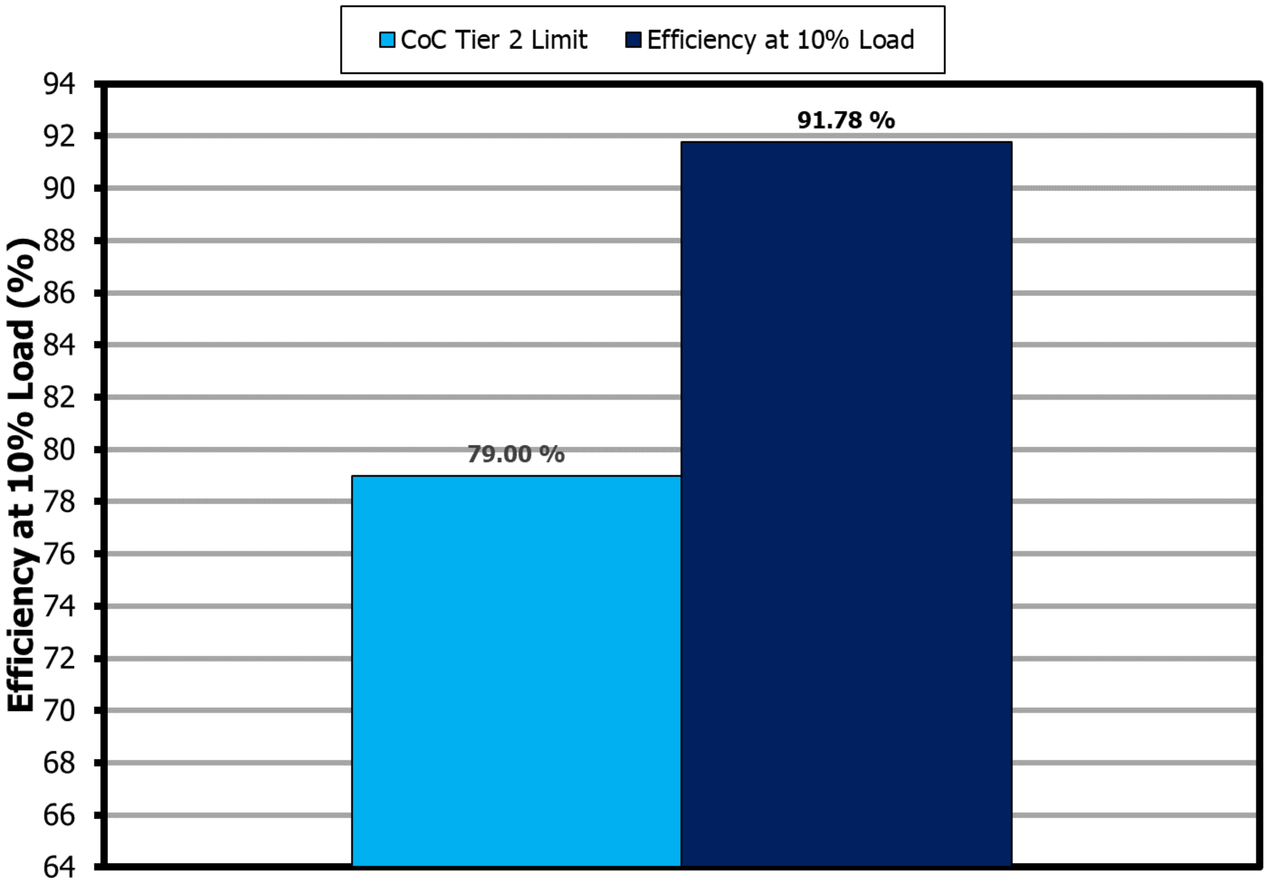


Figure 86 – Efficiency at 10% Load, 230 VAC 24 V Output.

15.2.5 Full Load Line Regulation

Note: Line regulation percentages were based on 24 V, the nominal output voltage.

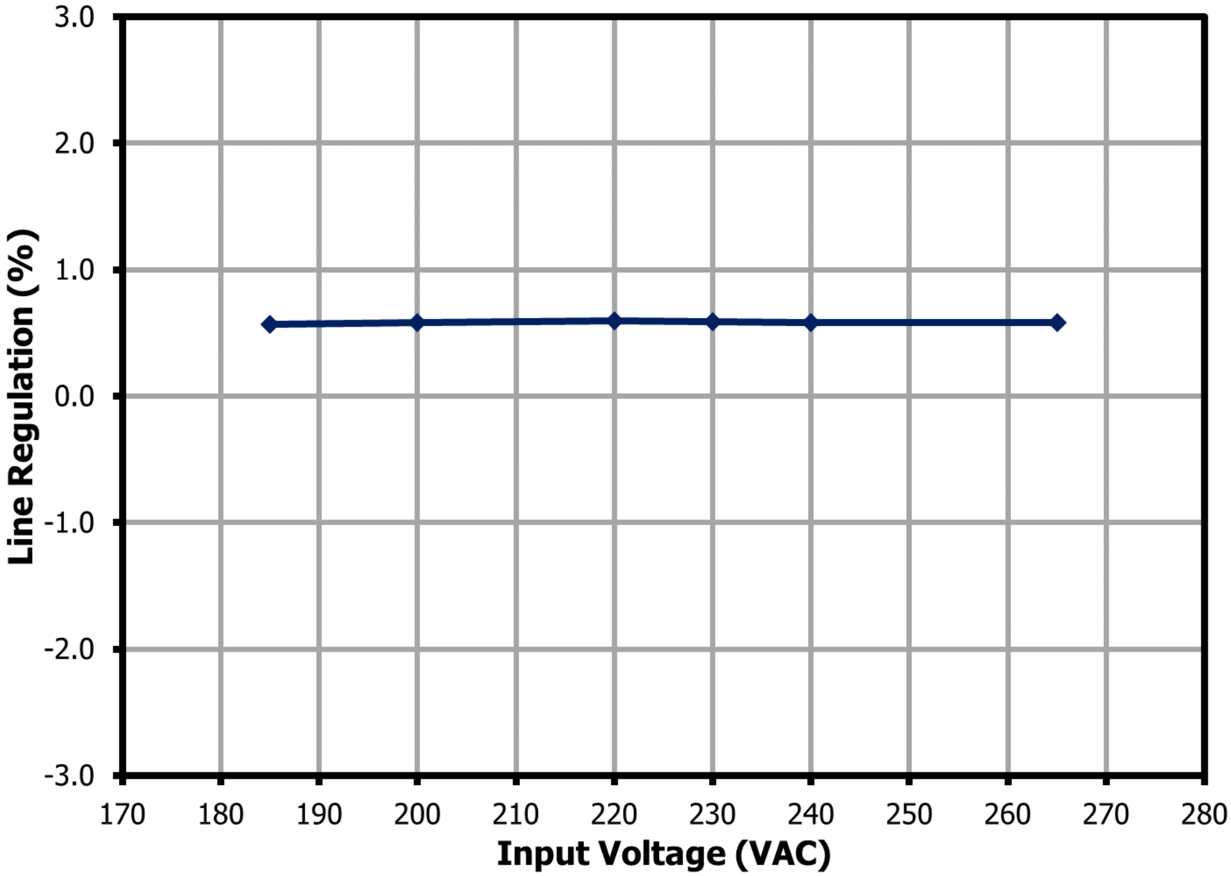


Figure 87 – Full Load Line Regulation vs. Input Line Voltage.

15.2.6 Efficiency vs Load at 24 V output

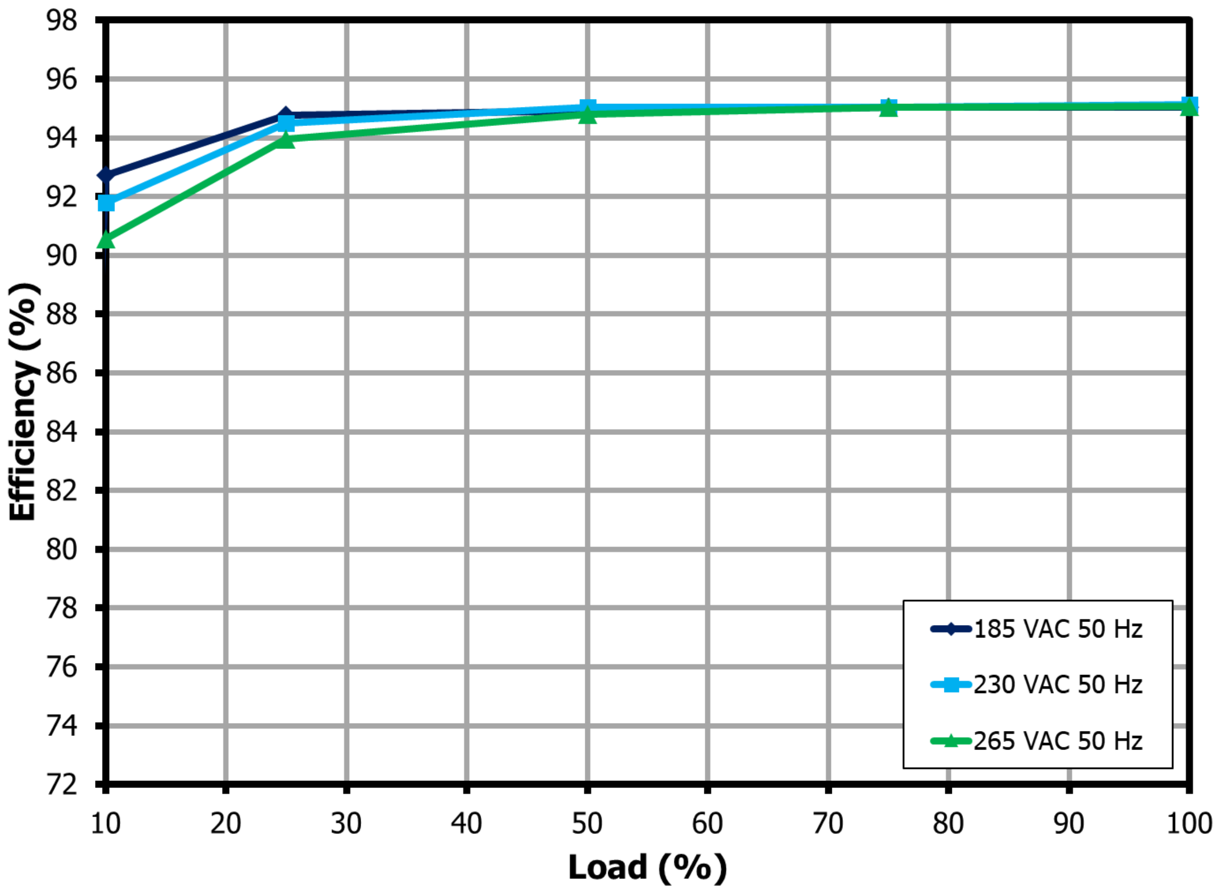


Figure 88 – Efficiency vs. Load at 24 V Output.

15.2.7 Load Regulation at 24 V

Output voltage was measured at the PSU output terminals TP3 and TP4.

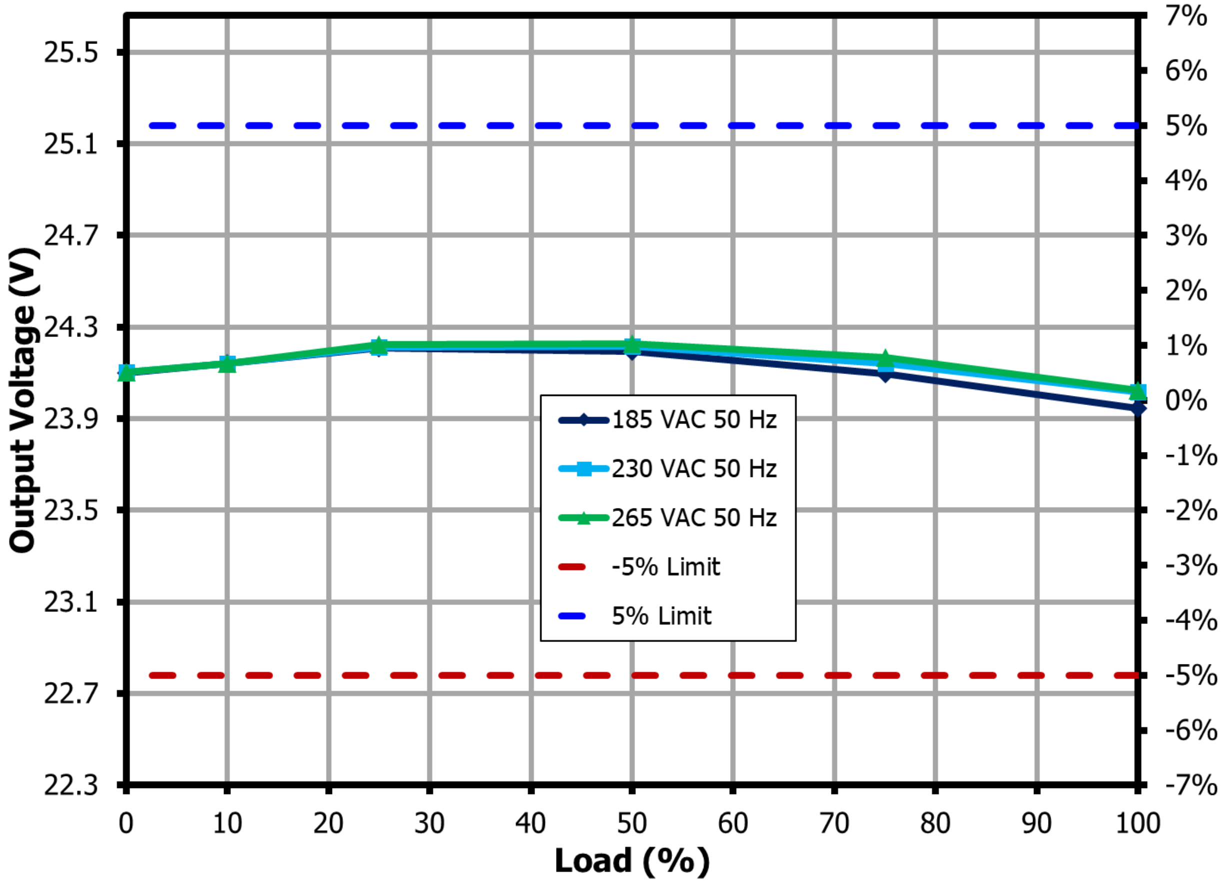


Figure 89 – Voltage Regulation vs. % Load at 24 V.

15.2.8 Output Ripple Voltage at 24 V

Output ripple voltage was measured at the end of 100 mΩ output cable.

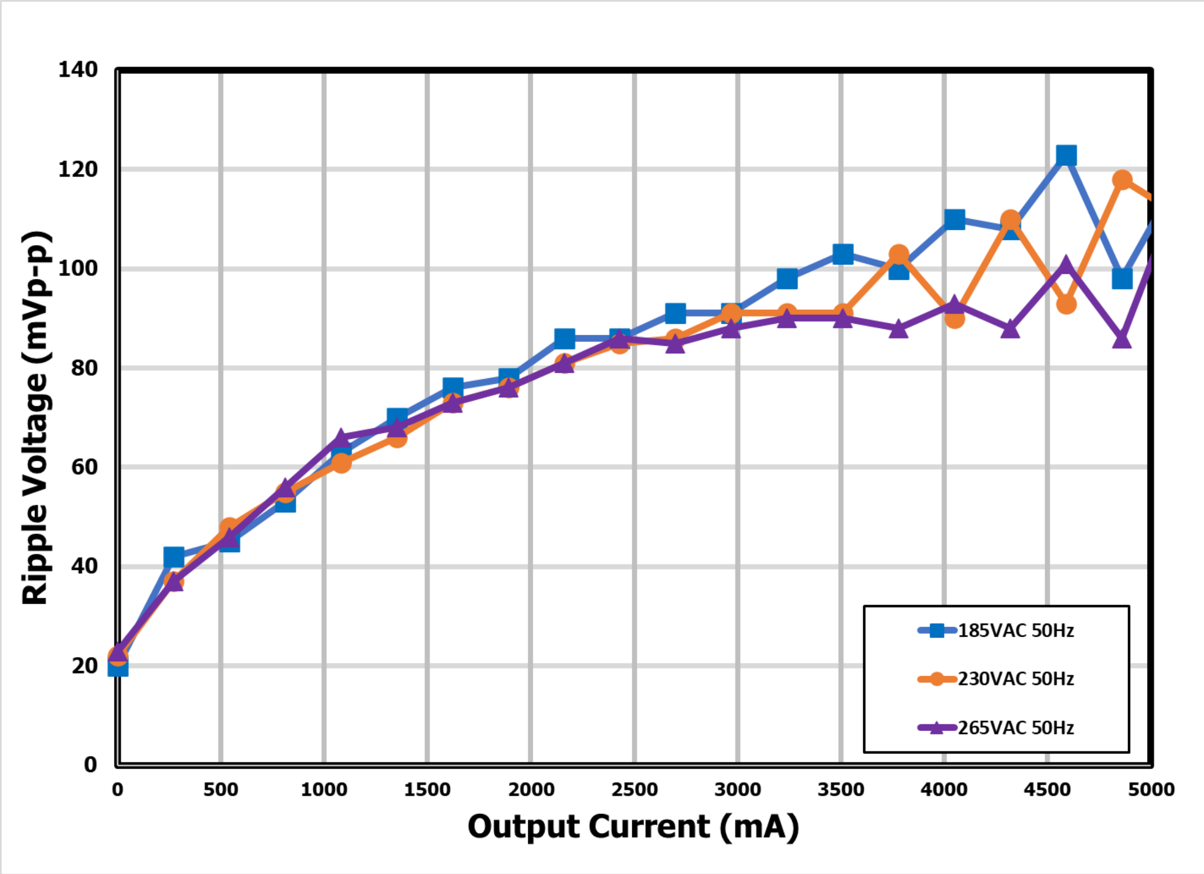


Figure 90 – Ripple voltage vs. Load at 24 V.

15.2.9 Standby Input Power at 40 mW Output Load

Standby input power was measured at 7.5 V output voltage setting using a Yokogawa WT310E power meter. The power meter is set at no load or standby mode measurement setting in Figure 13.

Input		Input Measurement		Output 1 Measurement				Efficiency
Vac (rms)	Freq (Hz)	Vin (rms)	Pin (W)	Vo (V)	Io (mA)	Po (W)	%V Reg	
185	50	184.95	**0.072**	7.64	5.38	0.04	0.58	57
200	50	199.96	**0.075**	7.64	5.37	0.04	0.58	54.87
220	50	220.02	**0.078**	7.64	5.34	0.04	0.58	52.14
230	50	229.97	**0.08**	7.65	5.32	0.04	0.59	50.75
240	50	240	**0.082**	7.65	5.31	0.04	0.59	49.21
265	50	264.98	**0.092**	7.65	5.29	0.04	0.61	43.79

Remarks: Standby Input Power meets the < 100 mW requirement at 230 VAC.

15.2.10 Standby Input Power at 300 mW Output Load

Standby input power was measured at 7.5 V output voltage setting using a Yokogawa WT310E power meter. The power meter is set at no load or standby mode measurement setting in Figure 13.

Input		Input Measurement		Output 1 Measurement				Efficiency
Vac (rms)	Freq (Hz)	Vin (rms)	Pin (W)	Vo (V)	Io (mA)	Po (W)	%V Reg	
185	50	184.95	**0.353**	7.64	39.38	0.3	0.57	85.31
200	50	199.96	**0.357**	7.64	39.37	0.3	0.58	84.23
220	50	220.02	**0.363**	7.65	39.36	0.3	0.59	82.81
230	50	229.97	**0.365**	7.65	39.35	0.3	0.59	82.41
240	50	240.01	**0.37**	7.65	39.34	0.3	0.59	81.39
265	50	264.98	**0.384**	7.65	39.34	0.3	0.59	78.36

Remarks: Standby Input Power meets the < 375 mW requirement at 230 VAC

15.2.11 Thermal Scan at Room Ambient Temperature

The PSU was placed in a horizontal position inside an acrylic plastic housing. Thermal data were measured using a Flir IR camera.

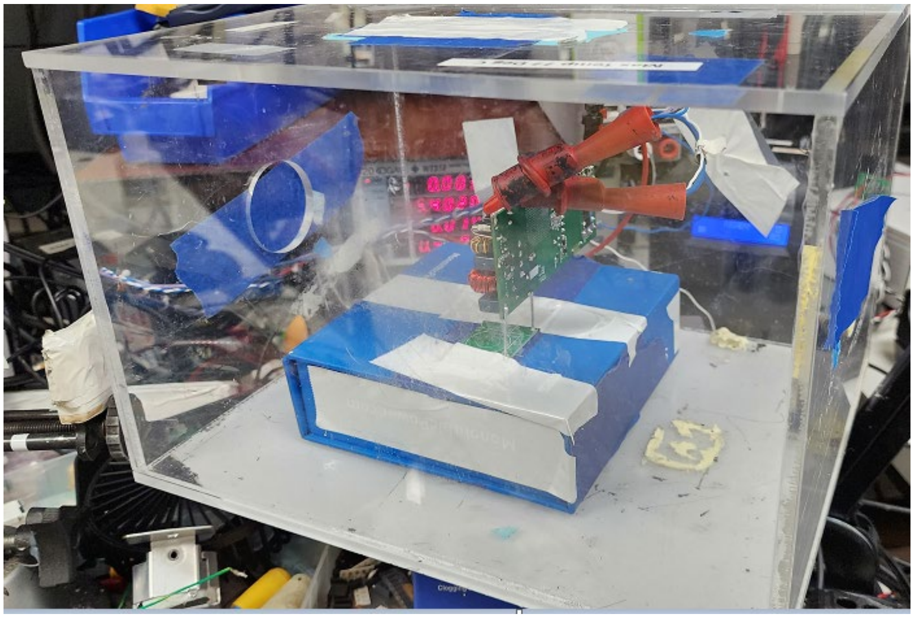


Figure 91 – Thermal Scan Test Set-up.

Thermal Scan Test Summary Data

Circuit Location	(°C)	
	185 VAC	**265 VAC**
	50 Hz	**50 Hz**
U8-Pri. (INNO4-QR)	77.1	82.5
U8-Sec. (INNO4-QR)	80.8	83.7
Q13/Q14-SRFET	74.1	75.5
D13/D12-Pri. Snubber	70.9	70.3
T1-Sec. Wire. (TRF)	75.2	77.6
T1- Ferrite Core. (TRF)	74.8	77.1
L2-(Input CMC)	57.3	52.6
BR1-(Bridge Diode)	66.7	59.2
L1-(HF Input CMC)	48	47
L3-(Diff. Choke)	48.9	44.5
Ambient Temperature	26	26

15.2.11.1 Thermal Scan at 185 VAC 24 V / 5.4 A

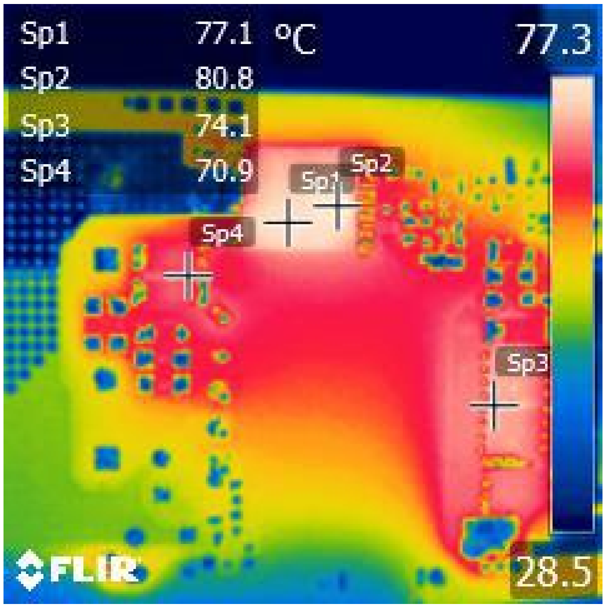


Figure 92 – Thermal Scan 185 V 24 V / 5.4 A.
Sp1: U8-Pri. (INNO4-QR): 77.1 °C
Sp2: U8-Sec. (INNO4-QR): 80.8 °C
Sp3: Q13/Q14-SRFET: 74.1 °C
Sp4: D13/D12-Pri. Snubber: 70.9 °C

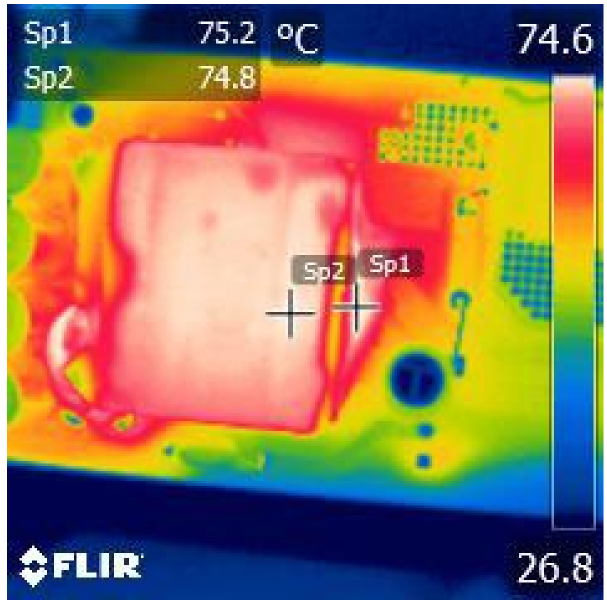


Figure 93 – Thermal Scan 185 V 24 V / 5.4 A.
Sp1: T1-Sec. Wire. (TRF): 75.2 °C
Sp1: T1- Ferrite Core. (TRF): 74.8 °C

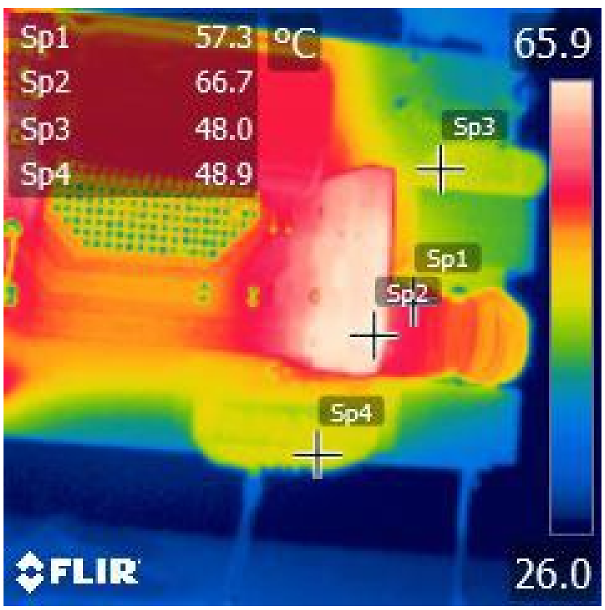


Figure 94 – Thermal Scan 185 V 24 V / 5.4 A.
Sp1: L2-(Input CMC): 57.3 °C
Sp2: BR1-(Bridge Diode): 66.7 °C
Sp3: L1-(HF Input CMC): 48 °C
Sp3: L3-(Diff. Choke): 48.9 °C

15.2.11.2 Thermal Scan at 265 VAC, 24 V / 5.4 A

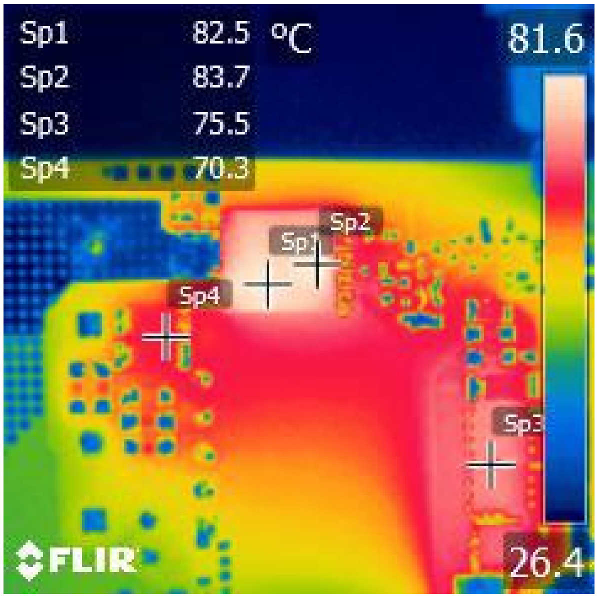


Figure 95 – Thermal Scan 265 VAC, 24 V / 5.4 A.
Sp1: U8-Pri. (INNO4-QR): 82.5 °C
Sp2: U8-Sec. (INNO4-QR): 83.7 °C
Sp3: Q13/Q14-SRFET: 75.5 °C
Sp4: D13/D12-Pri. Snubber: 70.3 °C

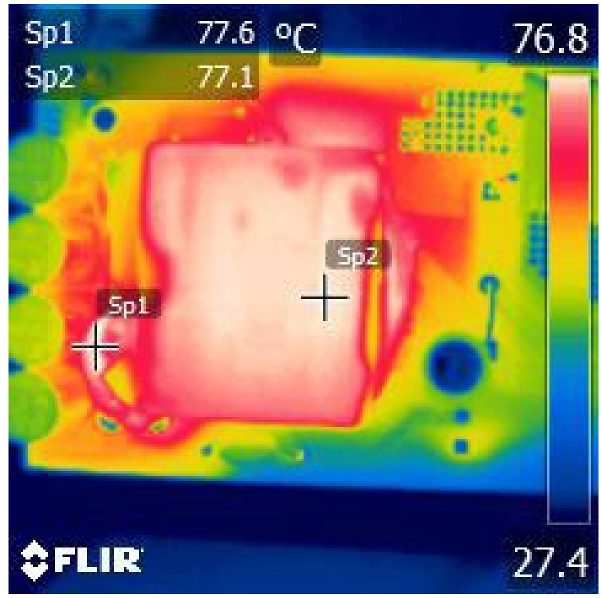


Figure 96 – Thermal Scan 265 VAC, 24 V / 5.4 A.
Sp1: T1-Sec. Wire. (TRF): 77.6 °C
Sp1: T1-Ferrite Core. (TRF): 77.1 °C

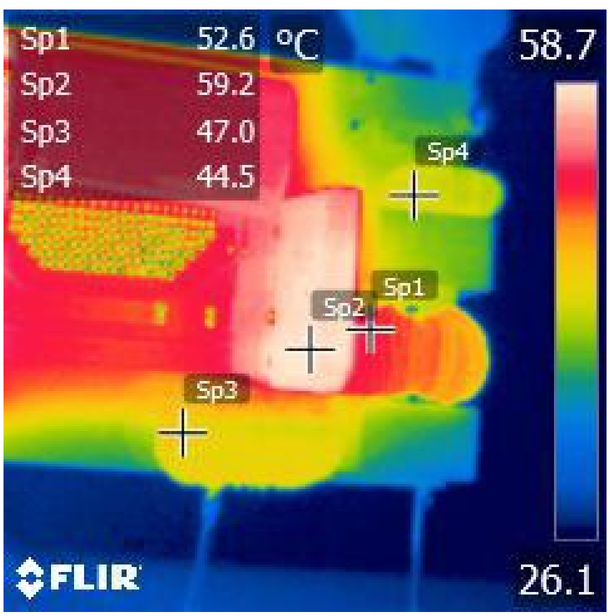


Figure 97 – Thermal Scan 265 VAC, 24 V / 5.4 A.
Sp1: L2-(Input CMC): 52.6 °C
Sp2: BR1-(Bridge Diode): 59.2 °C
Sp3: L1-(HF CMC): 47 °C
Sp4: L3-(Diff. Choke): 44.5 °C

15.3 Waveforms at High Input Line

15.3.1 Primary Drain Voltage and Current

15.3.1.1 Primary drain voltage and current at steady State

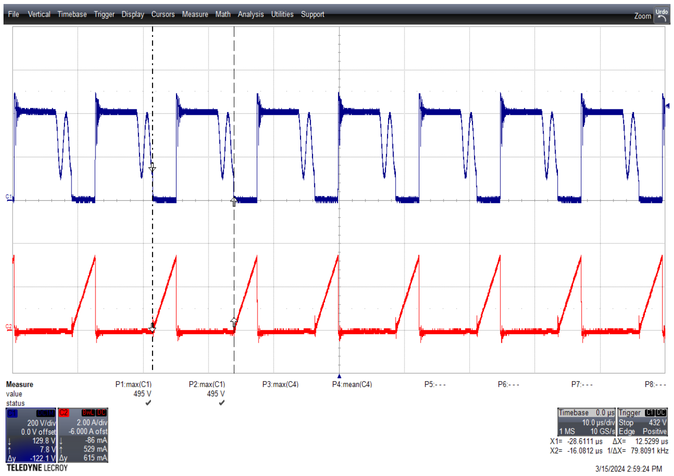


Figure 98 – Primary Drain Voltage and Current.
185 VAC, 24 V 5.4 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 10 µs / div.
V_{DSMAX}: 495 V

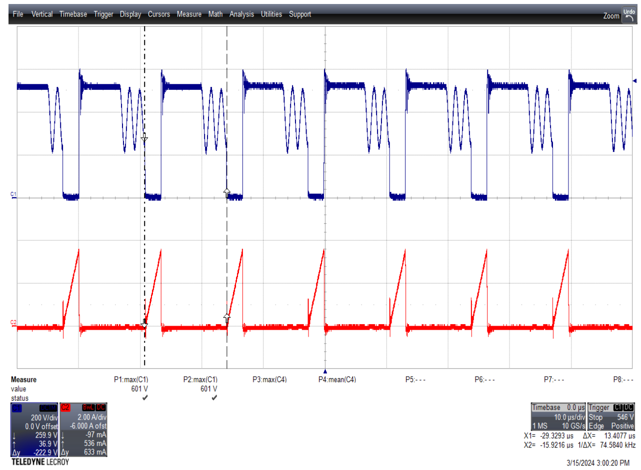


Figure 99 – Primary Drain Voltage and Current.
265 VAC, 24 V 5.4 A Steady-State
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 10 µs / div.
V_{DSMAX}: 601 V

15.3.1.2 Primary Drain Voltage at Start-up

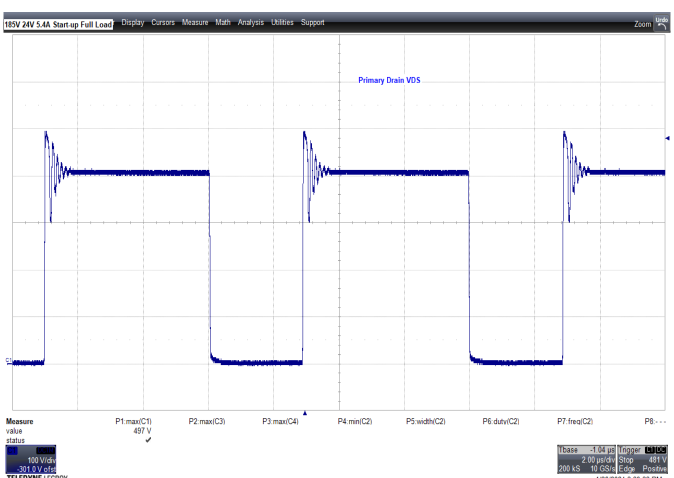


Figure 100 – Primary Drain Voltage and Current.
185 VAC, 24 V 5.4 A Start-up
Upper: V_{DS}, 100 V / div., 2 µs/div.
V_{DSMAX}: 497 V

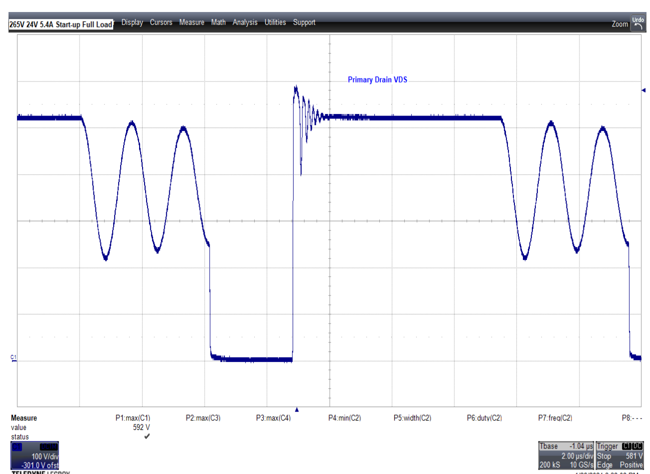


Figure 101 – Primary Drain Voltage and Current.
265 VAC, 24 V 5.4 A Start-up
Upper: V_{DS}, 100 V / div., 2 µs/div.
V_{DSMAX}: 592 V

15.3.1.3 Primary Drain Voltage and Current at Transient Load

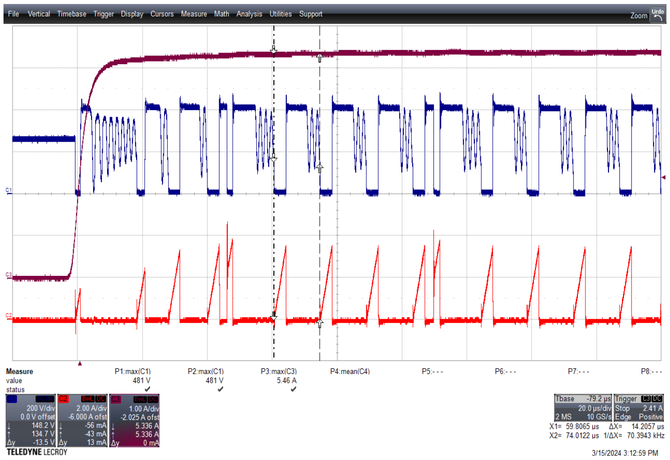


Figure 102 – Primary Drain Voltage and Current.
185 VAC, 24 V 5.4 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 µs / div.
V_{DSMAX}: 481 V; I_{DSMAX}: 5.46 A

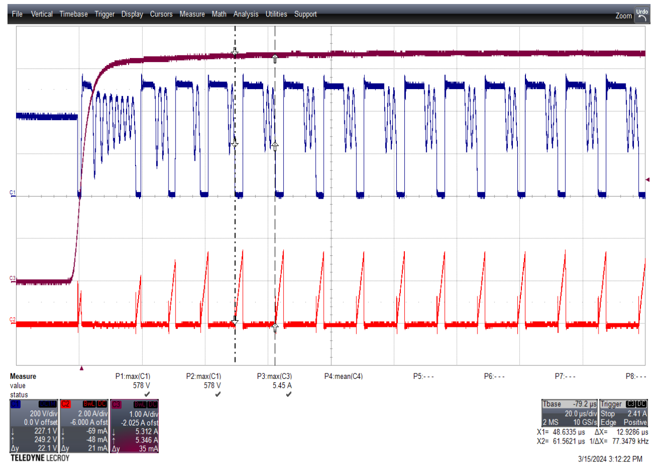


Figure 103 – Primary Drain Voltage and Current.
265 VAC, 24 V 5.4 A Step Load
Upper1: I_{OUT}, 1 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 µs/ div.
V_{DSMAX}: 578 V; I_{DSMAX}: 5.45 A

15.3.1.4 Primary Drain Voltage and Current at Peak Load

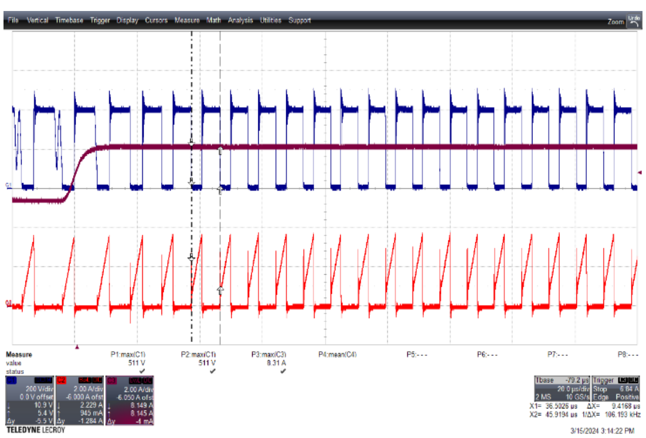


Figure 104 – Primary Drain Voltage and Current.
185 VAC, 24 V 5.4 A - 8.2 A Step Load
Upper1: I_{OUT}, 2 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 µs / div.
V_{DSMAX}: 511 V; I_{OMAX}: 8.31 A

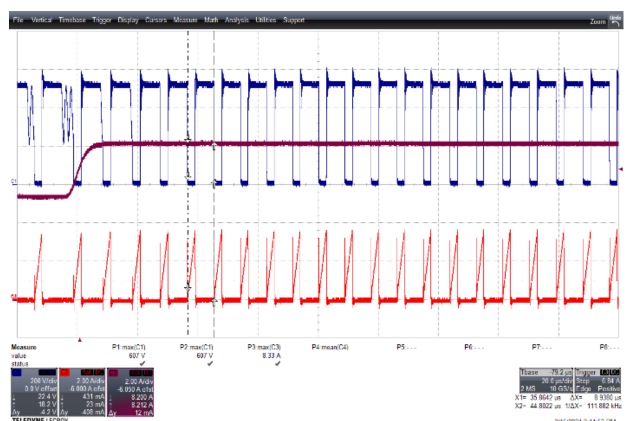


Figure 105 – Primary Drain Voltage and Current.
265 VAC, 24 V 5.4 A - 8.2 A Step Load
Upper1: I_{OUT}, 2 A / div.
Uppe2: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 20 µs / div.
V_{DSMAX}: 607 V; I_{OMAX}: 8.33 A

15.3.1.5 Primary Drain Voltage and Current at Peak Load

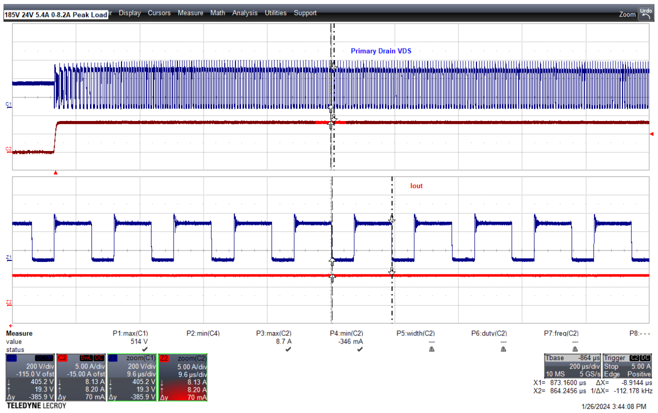


Figure 106 – Primary Drain Voltage and Current.
185 V, 24 V 0 A – 8.2 A Step Load
Upper: V_{DS}, 200 V / div.
Lower: I_{OUT}, 5 A / div., 200 us / div.
V_{DSMAX}: 514 V

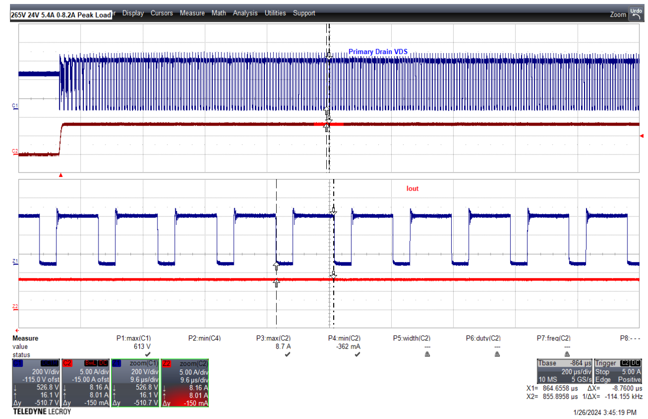


Figure 107 – Primary Drain Voltage and Current.
265 VAC, 24 V 0 A – 8.2 A Step Load
Upper: V_{DS}, 200 V / div.
Lower: I_{OUT}, 5 A / div., 200 us / div.
V_{DSMAX}: 613 V

15.3.1.6 Primary Drain Voltage and Current During Output Short Circuit

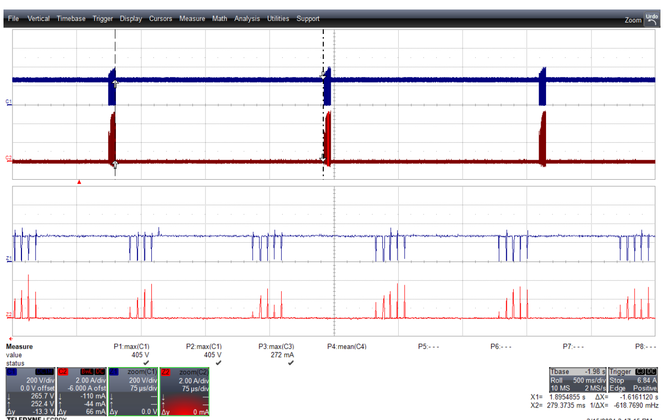


Figure 108 – Primary Drain Voltage and Current.
185 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 500 ms / div.
V_{DSMAX}: 405 V

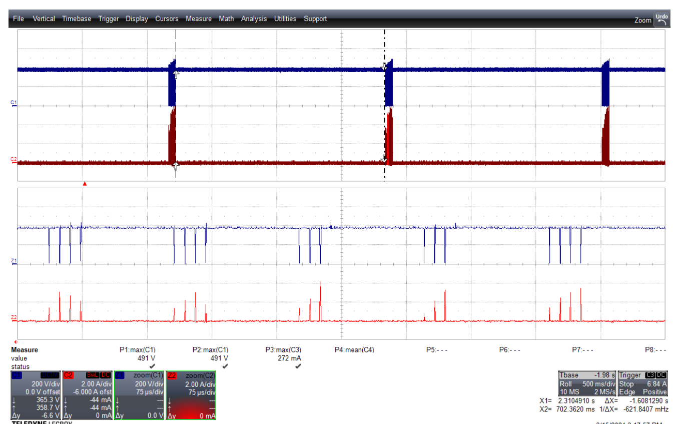


Figure 109 – Primary Drain Voltage and Current.
265 VAC, Output Short Circuit
Upper: V_{DS}, 200 V / div.
Lower: I_{DS}, 2 A / div., 500 ms / div.
V_{DSMAX}: 491 V

15.3.2 SR FET Voltage

15.3.2.1 SR FET Voltage at Transient Load

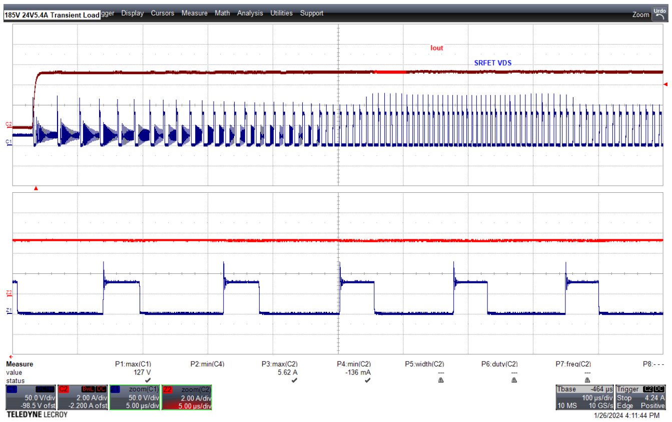


Figure 110 – SR FET Drain Voltage.
185 VAC, 24 V 0 A - 5.4 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 50 V / div.
V_{DSMAX}: 127 V

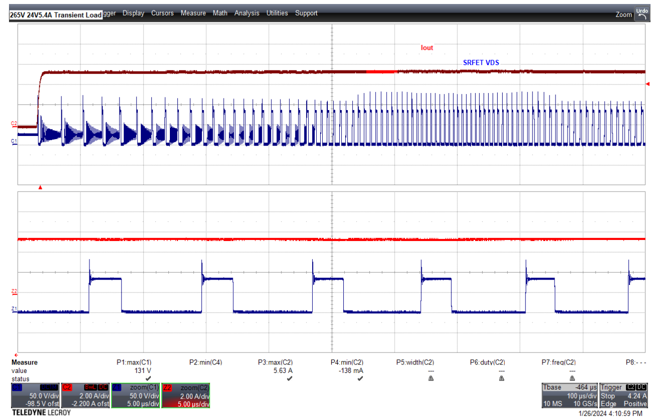


Figure 111 – SR FET Drain Voltage.
265 VAC, 24 V 0 A - 5.4 A Step Load
Upper: I_{OUT}, 2 A / div., 100 us / div.
Lower: V_{DS}, 50 V / div.
V_{DSMAX}: 131 V

15.3.2.2 SR FET voltage at peak load

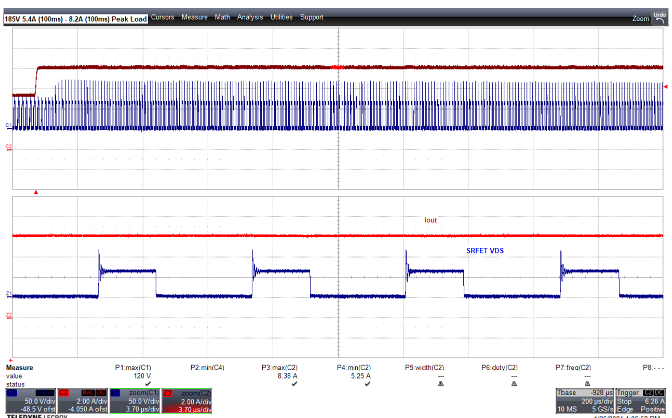


Figure 112 – SR FET Drain Voltage.
185 VAC, 24 V 5.4 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 200 us / div.
Lower: V_{DS}, 50 V / div.
V_{DSMAX}: 120 V

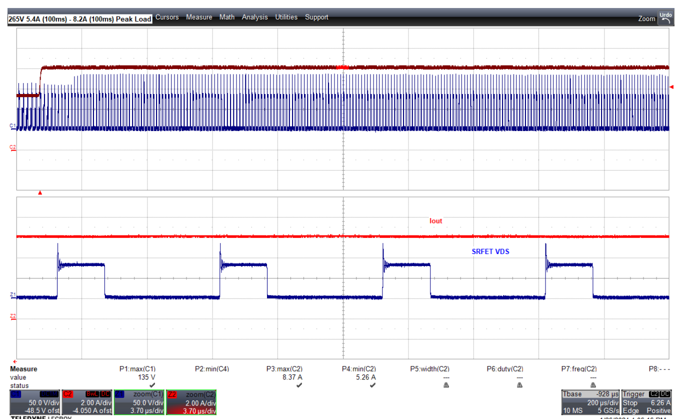


Figure 113 – SR FET Drain Voltage.
265 VAC, 24 V 5.4 A – 8.2 A Step Load
Upper: I_{OUT}, 2 A / div., 200 us / div.
Lower: V_{DS}, 50 V / div.
V_{DSMAX}: 135 V

15.4 Load Transient Response

Output voltage was measured at the PSU output terminals T3 and T4.

15.4.1 0% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/µs.

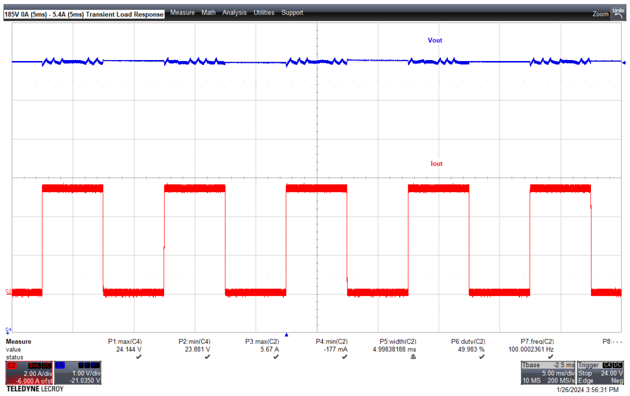


Figure 114 – 0% - 100% Load Transient.
185 VAC, 24 V 0 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 5 ms / div.
V_{OMIN}: 23.9 V; V_{OMAX}: 24.1 V

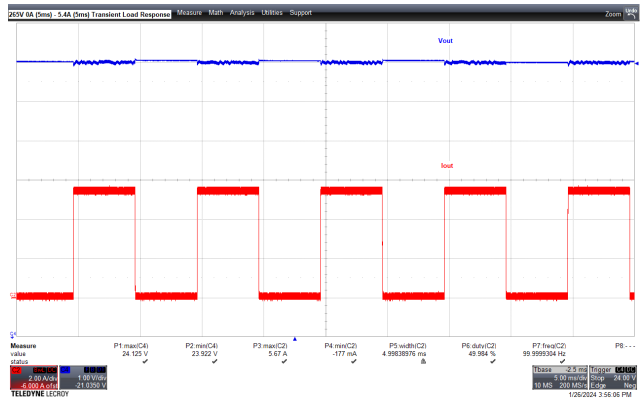


Figure 115 – 0% - 100% Load Transient.
265 VAC, 24 V 0 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 2 ms / div.
V_{OMIN}: 23.9 V; V_{OMAX}: 24.1 V

15.4.2 10% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 0.54 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/µs.

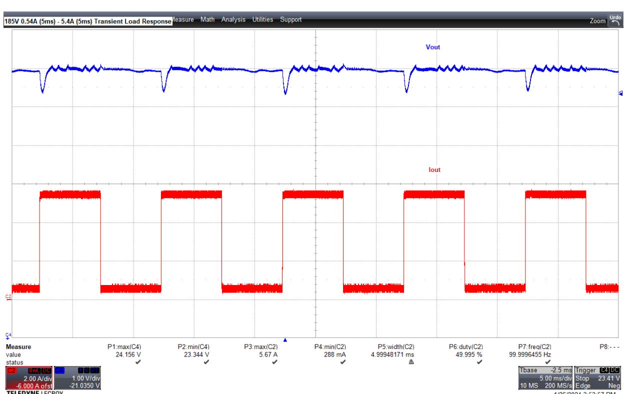


Figure 116 – 10% - 100% Load Transient.
185 VAC, 24 V 0.54 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 5 ms / div.
V_{OMIN}: 23.3 V; V_{OMAX}: 24.2 V

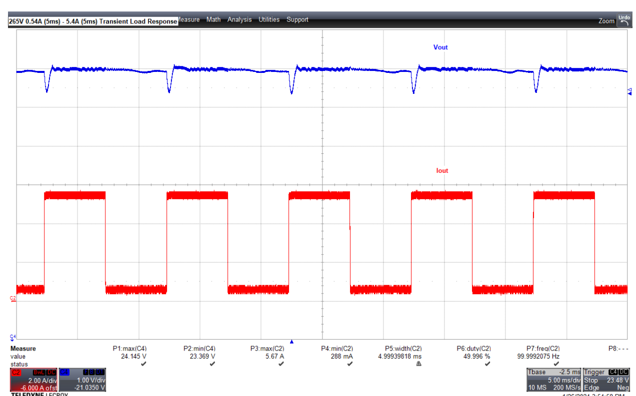


Figure 117 – 10% - 100% Load Transient.
265 VAC, 24 V 0.54 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 5 ms / div.
V_{OMIN}: 23.4 V; V_{OMAX}: 24.1 V

15.4.3 50% - 100% Load Transient

Set-up: 100 Hz dynamic load using Chroma 63113A E-load. 2.7 A – 5.4 A with 50% duty cycle and load current slew rate of 800 mA/us.

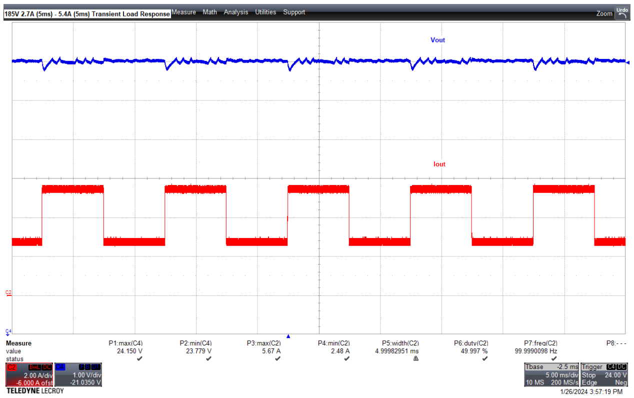


Figure 118 – (50% - 100%) Load Transient.
185 VAC, 24 V 2.7 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 5 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.2 V

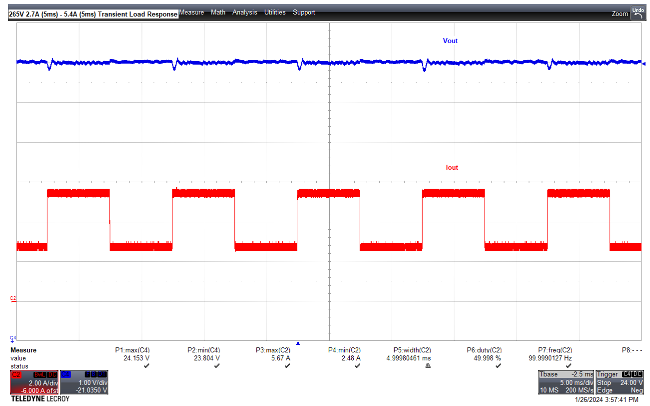


Figure 119 – (50% - 100%) Load Transient.
265 VAC, 24 V 2.7 A – 5.4 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 5 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.2 V

15.5 Peak Load Test

Output voltage was measured at the PSU output terminals T3 and T4.

15.5.1 0 A – 8.2 A Peak Load Transient

Set-up: 5 Hz dynamic load using Chroma 63113A E-load. 0 A – 8.2 A with 50% duty cycle and load current slew rate of 800 mA/µs.

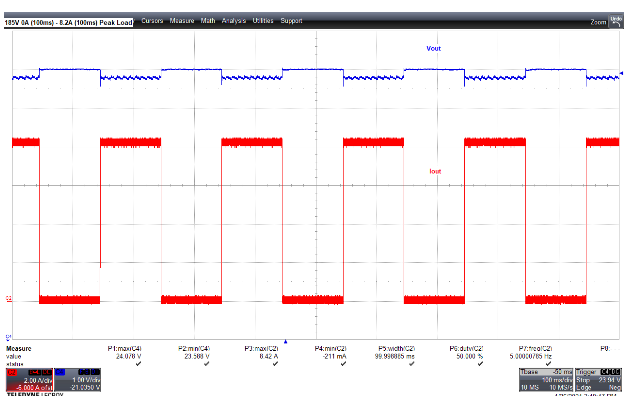


Figure 120 – (0 A – 8.2) A Load Transient.
185 VAC, 24 V 0 A – 8.2 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.2 V; V_{OMAX}: 24.1 V

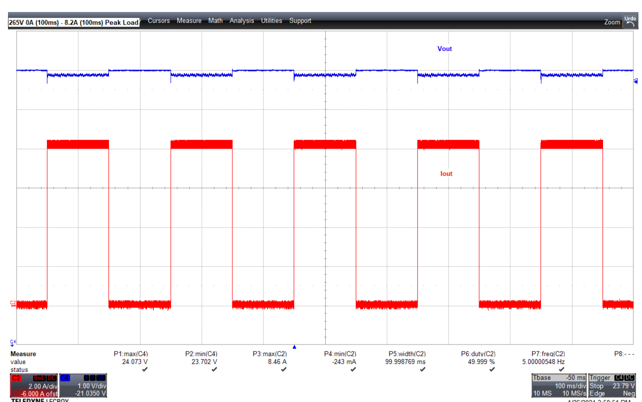


Figure 121 – (0 A – 8.2 A) Load Transient.
265 VAC, 24 V 0 A – 8.2 A Dynamic Load
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.7 V; V_{OMAX}: 24.1 V

15.5.2 5.4 A – 8.2 A Peak Load Transient

Set-up: 5 Hz dynamic load using Chroma 63113A E-load. 5.4 A – 8.2 A with 50% duty cycle and load current slew rate of 800 mA/µs.

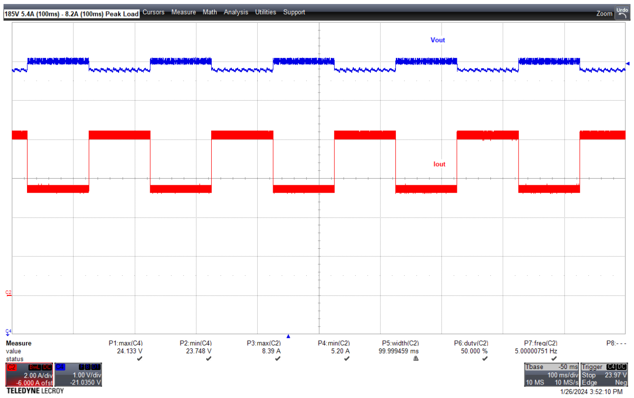


Figure 122 – (5.4 A – 8.2) A Load Transient.
185 VAC, 24 V 5.4 A – 8.2 A Dynamic Load.
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.1 V

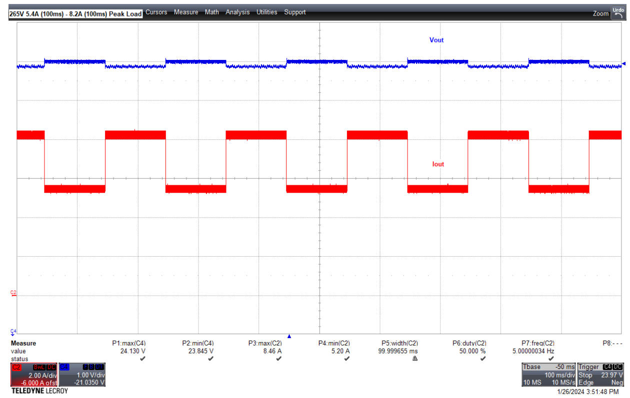


Figure 123 – (5.4 A – 8.2 A) Load Transient.
265 VAC, 24 V 5.4 A – 8.2 A Dynamic Load
Upper: V_{OUT}, 1 V / div.
Lower: I_{LOAD}, 2 A, 100 ms / div.
V_{OMIN}: 23.8 V; V_{OMAX}: 24.1 V

15.6 Conducted EMI

EMI scans are measured using 4.44 Ω fixed resistor load.

15.6.1 Test Set-up

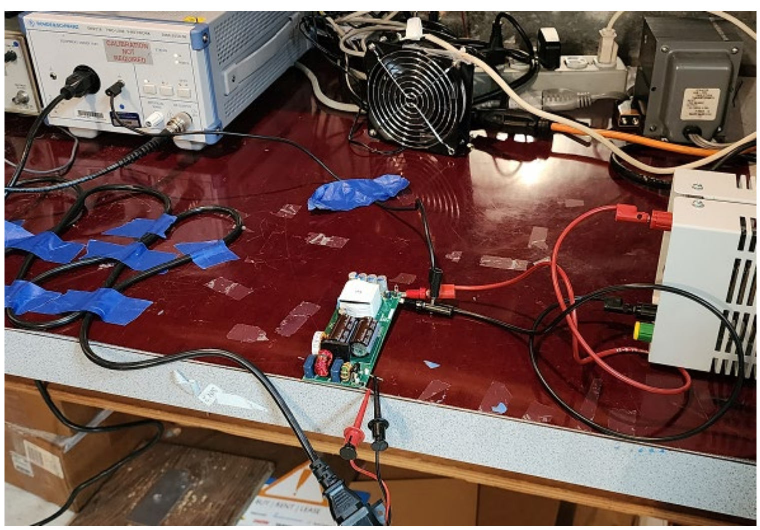


Figure 124 – Conducted EMI Test Set-up.

15.6.2 Floating Output Load Resistor

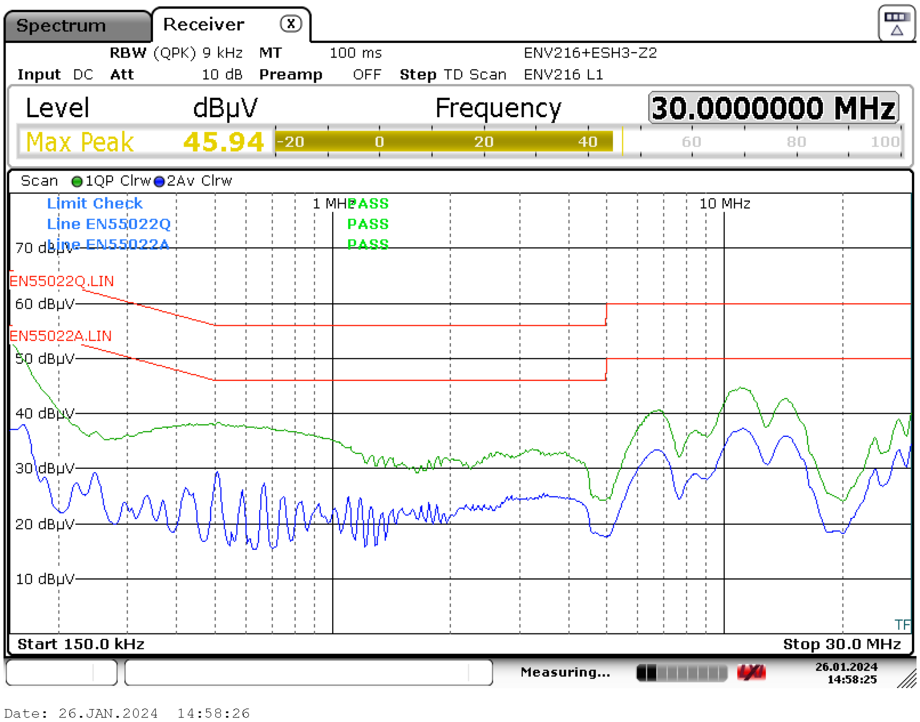


Figure 125 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Floating), 230 VAC Line 1.

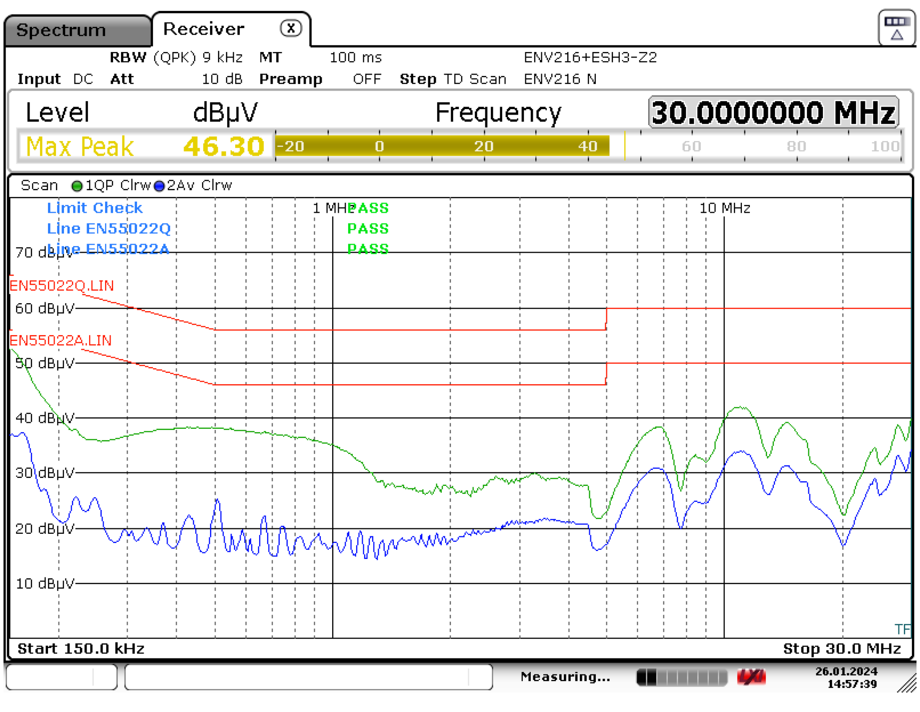


Figure 126 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Floating), 230 VAC Neutral.

15.6.3 Grounded Output Load Resistor

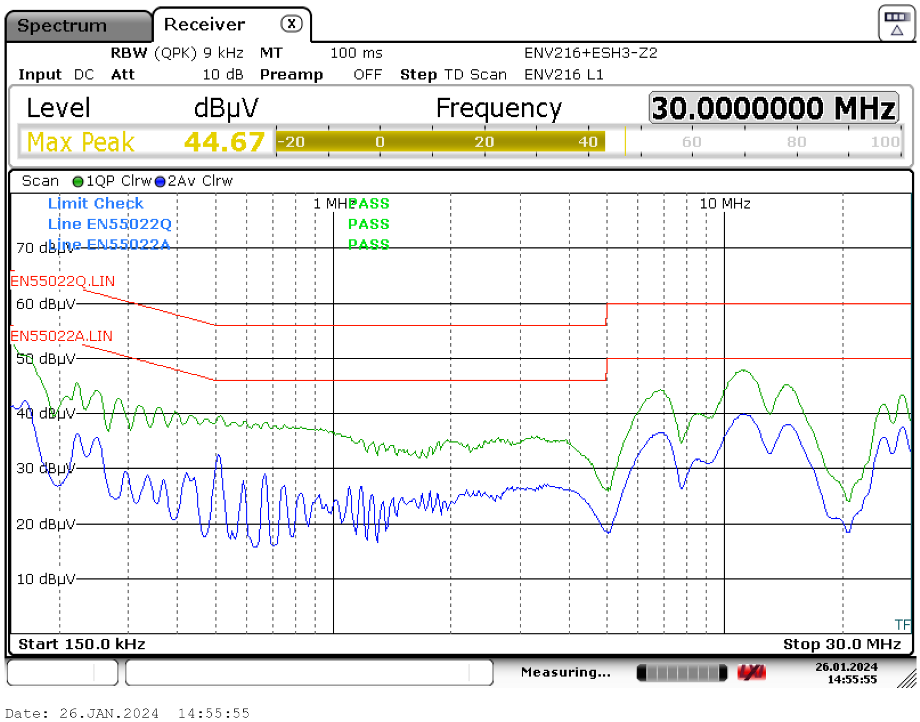


Figure 127 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Grounded), 230 VAC Line 1.

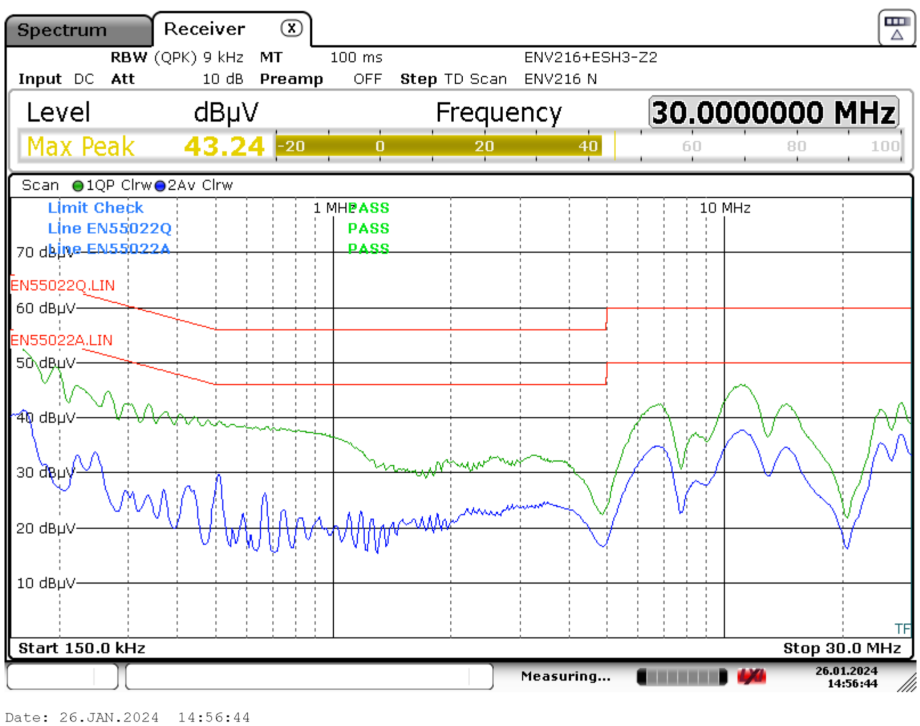


Figure 128 – Conducted EMI at 24 V 5.4 A (4.44 Ω-Grounded), 230 VAC Neutral.

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
30-Mar-24	MGM	0.1	Initial Release.	Apps & Mktg
16-Sep-25	RC /MM	B	BOM alternate parts inclusion.	Apps & Mktg

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