Design Example Report

Title	**356 W, 89 V CV-CC Isolated Flyback Using TOPSwitchGaN (TOP7078E)**
Specification	165 – 265 VAC Input; 89 V / 4 A CV/CC, and 12 V Aux. Outputs
Application	Tools and E-bike charger
Author	Applications Engineering Department
Document Number	DER-1019
Date	June 18, 2026
Revision	B

Summary and Features

- 356 W continuous output power
- > 91% full load efficiency at 230 VAC
- > 91 % average efficiency at 230 VAC
- Ultrawide constant current region (88 V – 0 V)
- Low component count: 89 pcs
- Excellent transient load response
- TOPSwitchGaN™ protection features:
  - Output short circuit protection
  - Over temperature protection (OTP)
  - Line undervoltage and overvoltage protection
  - Robust 800 V rated PowiGaN™ for high surge withstand
- Meets 4 kV Combination wave, Ring wave and Electric Fast Transient (EFT)
- Meets CISPR 22 Class B EMI with > 5 dB margin.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a flyback converter that provides an isolated output of 356 W at 89 V intended for an e-bike battery charger application. This power supply utilizes the TOP7078E IC from the TOPSwitchGaN family of ICs.

TOPSwitchGaN IC integrates an 800 V PowiGaN switch and a multi-mode flyback controller capable of operating in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), enabling high-efficiency from light load to full load.

The power supply delivers an 89 V constant-voltage output and provides constant-current charging down to 0 V across an input range is 165 VAC to 265 VAC. The design is optimized for high efficiency.

The report contains the power supply specification, bill of materials (BOM), transformer construction, schematic and printed circuit board (PCB) layout, along with performance data and circuit waveforms.

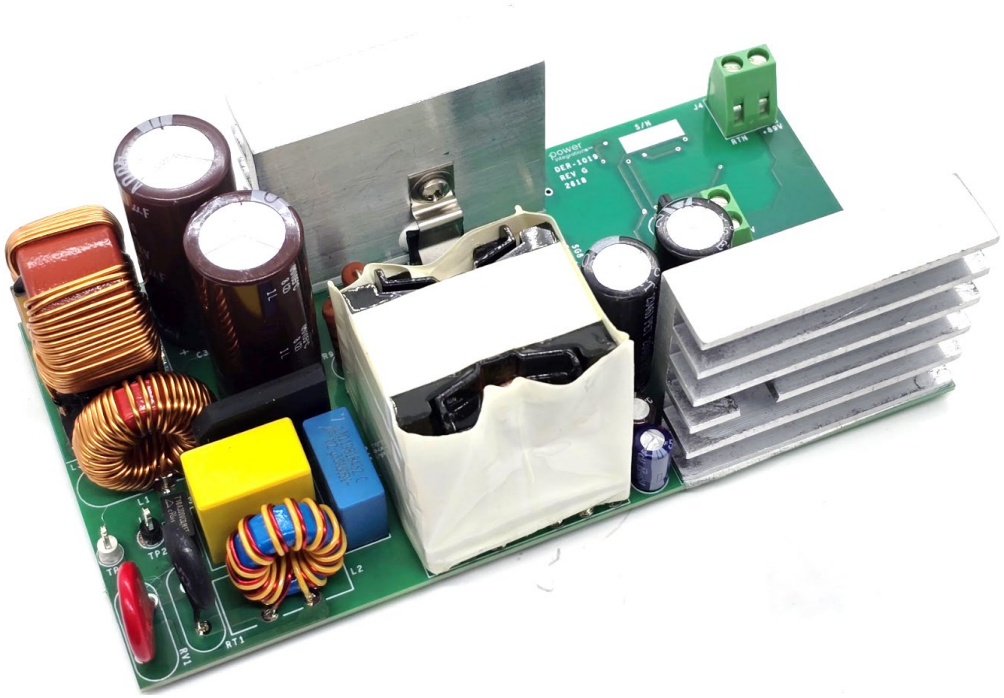


Figure 1 – Populated Circuit Board, Oblique View.

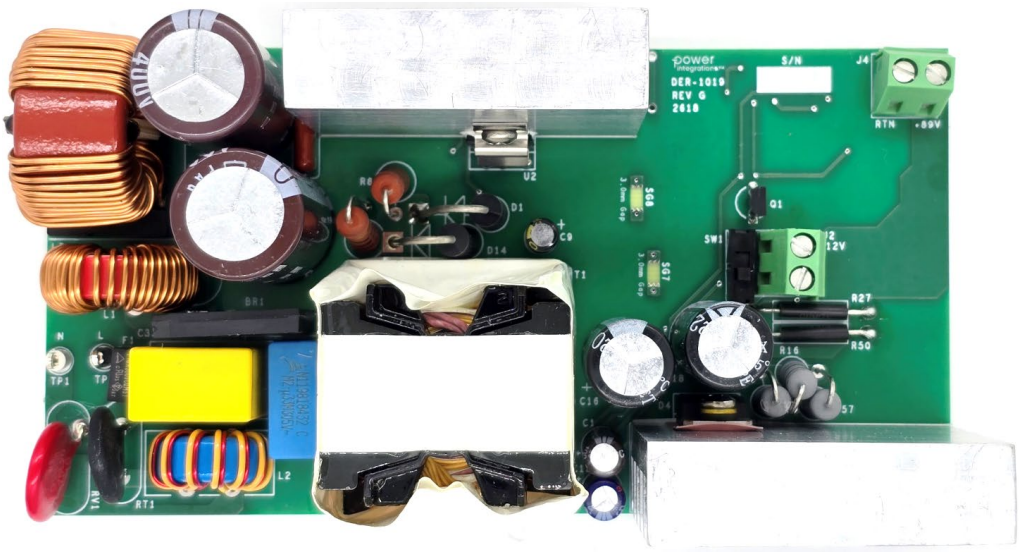


Figure 2 – Populated Circuit Board, Top Side.

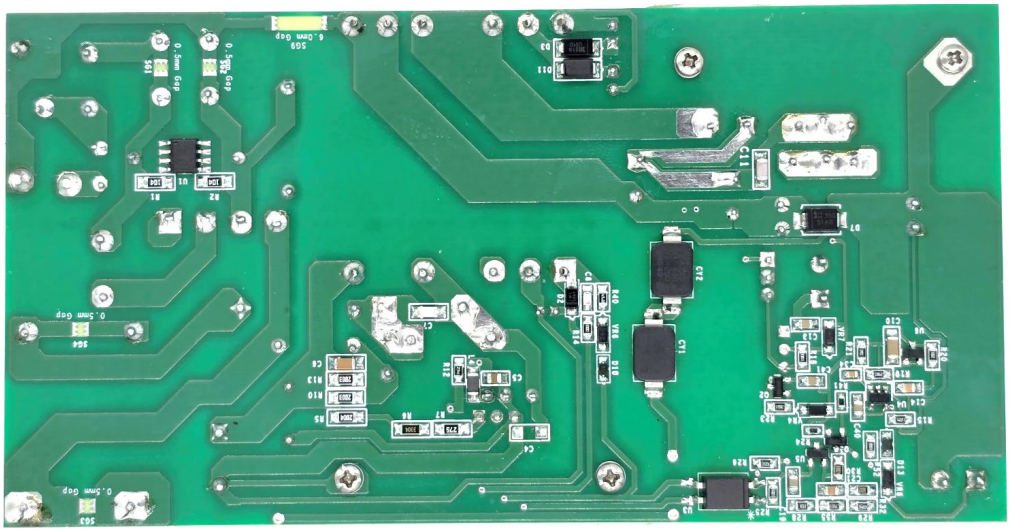


Figure 3 – Populated Circuit Board, Bottom Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	165	230	265	VAC	2 wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
Charger Output						
Output Voltage (CV/CC)	V_{OUT}		89		V	±3%
Output Current	I_{OUT}		4		A	±3%
Output Power	P_{OUT}			356	W	
Constant Output Current	I_{CC}		4.2		A	±3%
Constant Current Region	V_{CC}	88		0	V	4.2 A Constant Current
Output Ripple Voltage (CV)	V_{Ripple}			500	mVp-p	25 °C Ambient, 20 MHz BW
Auxiliary Fan Driver Voltage	V_{FAN}		12.5		V	
Auxiliary Fan driver Current	I_{FAN}			100	mA	
Efficiency						
Full Load	η_{FL}	91			%	230 VAC, With 12 V Fan
Average Efficiency	η_{AVE}	91			%	230 VAC, With 12 V Fan
No Load Input Power	P_{NL}			400	mW	230 VAC, Without 12 V Fan
Immunity						
Conducted EMI		CISPR22B / EN55022B				Fixed Resistor Load (floating)
Combination Wave Surge (L/N)				±4	kV	Source impedance: 2 Ω
Ring Wave				±4	kV	Source impedance: 12 Ω
EFT/Burst (5 kHz, 100 kHz)				±4	kV	120 seconds duration
ESD				±16.5	kV	
Operating Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

Table 1 – Power Supply Specification.

3 Schematic

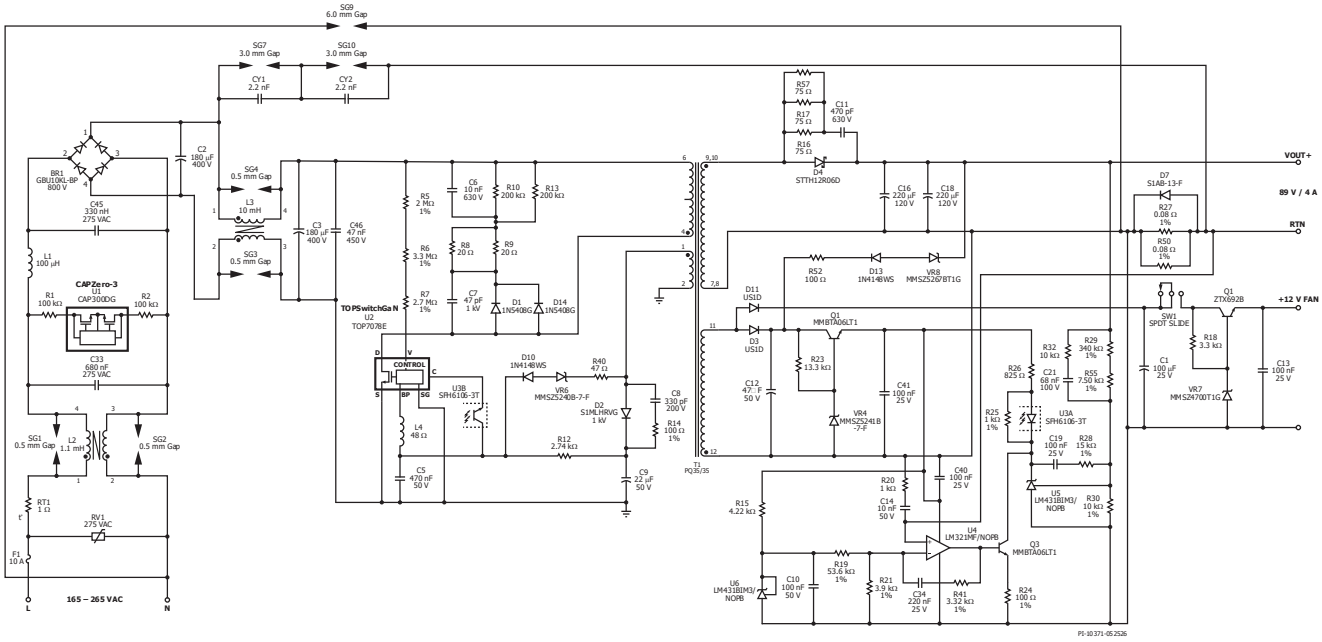


Figure 4 – Schematic.

4 Circuit Description

4.1 Input Rectification and EMI Filtering

Fuse F1 isolates the Power Supply Unit (PSU) circuitry and provides protection in the event of component failure. RV1 protects the circuit against high-voltage line surges. The NTC thermistor RT1 limits inrush current during start-up.

X-Capacitors C33 and C45 together with common mode choke (CMC) L2 form a π-filter that attenuates both common mode and differential mode noise in the >5 MHz region of the conducted EMI spectrum. BR1 provides full-wave AC rectification. C2, L3, and C3 form a second π-filter that reduces the flyback converter's DC-bus ripple voltage and attenuates both differential-mode and common-mode noise generated by switching. In addition, the TOPSwitchGaN frequency-jitter feature further reduces conducted EMI.

4.2 Zero Loss Automatic X-Capacitor Discharge CAPZero™-3

To satisfy the Safety Extra-Low Voltage (SELV) when the AC supply is disconnected, the CAP300DG (U1) automatically discharges the X capacitors C33 and C45 to a safe level by connecting discharge resistors R1 and R2. When AC voltage is applied, the CAP300DG (U1) blocks current flow in the X capacitor safety discharge resistors, reducing power loss to less than 5 mW.

4.3 Flyback Converter Circuit Using TOPSwitchGaN

Line undervoltage and overvoltage thresholds are determined by the current supplied from resistors R5, R6, and R57 to the V pin. The primary RCD snubber, formed by D1, D14, R8, R9, R10, R13, and C6, minimizes the primary-side voltage spike caused by the transformer's leakage inductance. A small ceramic capacitor C7 is added across snubber diodes D1 and D14 to reduce high-frequency ringing, which would otherwise contribute to radiated EMI. A 47 nF bypass capacitor, C46 was added to reduce the effective loop area of the bulk capacitor (C3), Transformer (T1) and TOPSwitchGaN (U2) for better EMI and noise immunity.

The TOPSwitchGaN IC is self-powered at start-up through an internal high-voltage current source connected to the DRAIN (D), which supplies current to the internal primary bypass regulator to charge the BYPASS pin capacitor (C5) when AC input is first applied. A ferrite bead (L4) is added to improve noise immunity from events such as ring wave, EFT and ESD. During normal operation, the controller is powered from the bias winding of transformer T1. The bias winding output is rectified by diode D2 and filtered by C9. Resistor R12 limits the current supplied to the BYPASS pin of the TOPSwitchGaN IC (U2), disabling the internal high-voltage current source once sufficient bias voltage is reached.

Primary-side sensed overvoltage protection (OVP) is implemented using Zener diode VR6, current-limiting resistor R40, and blocking diode D10 connected from the bias winding to the BYPASS pin. If an output overvoltage occurs, the increased bias winding voltage causes VR2

to conduct, injecting additional current into the BYPASS pin. When this current exceeds the shutdown threshold (I_{SD}), the TOPSwitchGaN IC stops switching and enters auto-restart mode. Auto-restart will continue until the output voltage returns to within regulation.

When the primary switch is off (flyback phase), output rectifier diodes D4 conduct transformer flyback current from the secondary winding, delivering energy to the output. Output capacitors C16 and C18 filter the rectified waveform to produce a stable DC output voltage.

The RC snubber network, composed of C11 and R16, R17 and R57 limits voltage stress across D4, suppresses high-frequency ringing, and improves both conducted and radiated EMI performance. Diode D7 protects the current-sense resistors R27 and R50 from excessive current during output short-circuits.

4.4 Secondary Feedback Circuit

During startup an auxiliary bootstrap supply, consisting of Zener diode VR8, current-limiting resistor R52, and blocking diode D13, provides the initial secondary-side bias voltage to the feedback circuitry. Once the secondary bias winding develops sufficient voltage, it forward-biases diode D3 and simultaneously reverse-biases blocking diode D13, allowing the dedicated secondary auxiliary forward-bias supply to take over operation.

A forward-bias auxiliary supply is used instead of a flyback-derived bias so that a stable secondary bias voltage is available across the entire output-voltage range—from 0 V to 89 V. Diode D3 rectifies the voltage from the auxiliary winding during the primary MOSFET's on-time. This rectified voltage is smoothed by capacitor C12, which filters ripple and provides a stable DC rail for the secondary control circuitry.

A linear regulator composed of transistor Q2, Zener diode VR4, resistor R23, and ceramic smoothing capacitor C41 further conditions this rail, producing a regulated 10.5 V supply for the secondary-side feedback components. This regulated bias voltage ensures stable conditions for the feedback comparators, precision references, and optocoupler-drive circuitry, resulting in accurate constant-voltage and constant-current regulation across line and load.

Optocoupler U3 provides the isolated feedback path that delivers the regulation signal to the primary-side controller in the TOPSwitchGaN IC. Current flowing through the optocoupler's U3A is limited by resistor R26, which protects the diode.

Constant-voltage regulation is controlled by the 2.5 V precision shunt regulator U5, which monitors the output voltage through the divider formed by R29, R55, and R30. Once the voltage at the reference pin reaches 2.5 V, U5 sinks current, driving the U3A optocoupler LED and sending the regulation signal to the primary-side control IC.

The RC compensation network R28 and C19 stabilizes the feedback loop by limiting the TL431's (U5) high-frequency gain, improving phase margin, and slows the output start-up

ramp. This compensation also prevents oscillation that would otherwise increase output-voltage ripple and degrade the transient load response.

A phase-boost RC network connected across the upper divider resistors R29 and R55 provides of phase advancement to improve transient response. This network also slows the output-voltage rise at full load, ensuring the primary switch has sufficient time to deliver full power during start-up.

Constant-current regulation is controlled by comparator U4 together with the pull-down NPN transistor Q3. The reference voltage applied to the inverting input of U4 is derived from the 2.5 V shunt regulator U6. This 2.5 V reference is reduced to 170 mV by the voltage-divider network R19 and R21 which minimizes power dissipation across the output current-sense resistors R27 and R50. Bias current for the shunt regulator U6 is supplied via R15.

The constant-current (I_{CC}) set point is established at 4.2 A using a current sense resistor.

$$R_{SENSE} = \frac{170\ \text{mV}}{I_{CC}} = 40\ \text{m}\Omega$$

The voltage drop across the sense resistors R27 and R50 is applied to the non-inverting input of U4. Comparator U4 continuously compares this current-sense voltage against the 170 mV reference. When the sensed voltage exceeds 170 mV (indicating that the load current has reached the CC limit), the power supply moves from to constant voltage to constant-current regulation. At this point, the pull-down NPN transistor Q3 conducts, sinking current through the optocoupler LED, which signals the primary-side controller to reduce output power. This maintains a regulated constant output current across the entire output-voltage range (0 V to 88 V).

The RC network R20 and C14 provides a short delay and filters the current-sense signal during no-load to full-load transients, preventing undershoot and avoiding interruption of power-delivery.

Resistor R24 introduces local negative feedback, preventing the NPN transistor Q3 from switching abruptly and reducing the risk of oscillation within the comparator loop. Resistor R25, connected across optocoupler U3A, slows the optocoupler LED turn-on during startup, allowing additional time for the feedback loop to stabilize before current regulation begins.

The 12 V supply for the cooling-fan is also derived from the secondary forward-bias winding, rectified by D11 and filtered by C1. A linear regulator formed by Q1, VR7, and R18 provides a regulated 12.5 V output when operating from 165 V to 265 V AC.

5 PCB Layout

Layers: 2 Layer
Board Thickness: 1.6 mm
Copper Thickness: 2 oz
Material: FR4

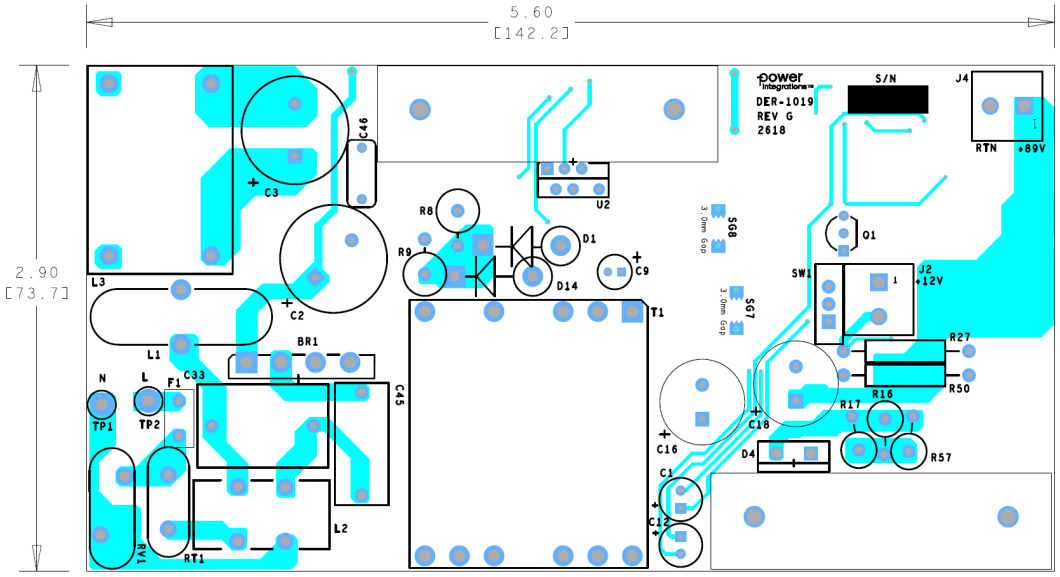


Figure 5 – Printed Circuit Board Layout, Top.

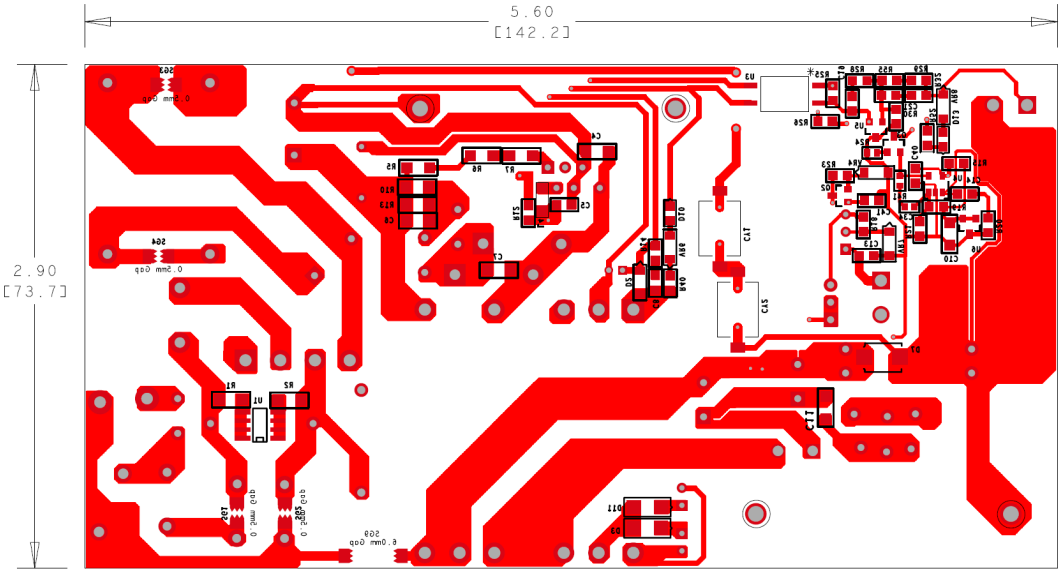


Figure 6 – Printed Circuit Board Layout, Bottom.

Note: C4 is not populated circuit location

6 Bill of Materials

Item No.	Ref Des.	Qty.	Description	Manufacturer	Mfr. Part Number
1	BR1	1	Bridge Rectifier, Single Phase, Standard, 800 V, Through Hole GBU	Micro Commercial Co	GBU10KL-BP
2	C1	1	100 µF, 25 V, Electrolytic, Very Low ESR, 130 mOhm, (6.3 x 11)	Nippon Chemi-Con	EKZE250ELL101MF11D
3	C2 C3	2	180 µF, 400 V, Electrolytic, Low ESR, (18 x 40)	Nippon Chemi-Con	EPAG401ELL181MM40S
4	C5	1	0.47 µF, ±10%, 50 V, Ceramic, X7R, 0805 (2012 Metric), -55 °C ~ 125 °C	TDK Corp	CGA4J3X7R1H474K125AB
5	C6	1	10 nF, 630 V, Ceramic, X7R, 1206	Kemet	C1206C103KBRACTU
6	C7	1	47 pF, 1000 V, Ceramic, NP0, 1206	Kemet	C1206C470JDGACTU
7	C8	1	330 pF ±5% 200 V Ceramic Capacitor C0G, NP0 0805 (2012 Metric)	Kemet	C0805C331J2GACAUTO
8	C9	1	22 µF, 50 V, Aluminum Electrolytic Capacitors, Radial, Can 2000 Hrs @ 85 °C, (5 x 11), LS 2 mm	Panasonic Electronic Components	EEU-FM1H220H
9	C10	1	100 nF, 50 V, Ceramic, X7R, 1206	Yageo	CC1206KRX7R9BB104
10	C11	1	470 pF, 1000 V, Ceramic, COG, 1206	Vishay-Vitramon	VJ1206A471JXGAT5Z
11	C12	1	47 µF, 50 V, Electrolytic, Gen. Purpose, (6.3 x 11.2)	Panasonic	ECA-1HM470
12	C13 C19 C40 C41	4	100 nF, 25 V, Ceramic, X7R, 0805	AVX Corp	08053C104KAT2A
13	C14	1	10 nF, 50 V, Ceramic, X7R, 0805	Kemet	C0805C103K5RACTU
14	C16 C18	2	220 µF, ±20%, 120 V, Aluminum Electrolytic Capacitors, Radial, Can, 6000 Hrs @ 105 °C, (12.5 x 30)	KYOCERA AVX	REF1230221M120K
15	C21	1	68 nF, 50 V, Ceramic, X7R, 0805	Kemet	C0805C683K5RACTU
16	C33	1	680 nF, 275 VAC, Film, MPX Series, X2	Carli	PX684K3ID6
17	C34	1	220 nF, 25 V, Ceramic, X7R, 0603	AVX	06033D224KAT2A
18	C45	1	330 nF, ±20%, 310 VAC, 630 VDC, Film, X2	Epcos	B32922C3334M000
19	C46	1	47 nF, 450 VDC, 5%, Film	Duratech	MEXXD2470
20	CY1 CY2	2	2200 pF, ±20%, 440 VAC, X1, Y1, Ceramic Capacitor F, Gull-Wing, Nonstandard SMD	Murata Electronics	DK1F3EA222M86RAH01
21	D1 D14	2	1000 V, 3 A, Rectifier, DO-201AD	ON Semiconductor	1N5408G
22	D2	1	Diode, Standard, 1000 V, 1 A, Surface Mount, Sub SMA	TAIWAN SEMICONDUCTOR	S1MLHRVG
23	D3 D11	2	DIODE ULTRA FAST, SW, 200 V, 1 A, SMA	Diodes, Inc	US1D-13-F
24	D4	1	600 V, 12 A, Ultrafast Recovery, 45 ns, TO-220AC	ST Semiconductor	STTH12R06D
25	D7	1	50 V, 1 A, Standard Recovery, GPP, SMB	Diode Inc.	S1AB-13-F
26	D10 D13	2	DIODE, GEN PURP, 75 V, 150 MA, SOD323	Diodes Inc	1N4148WS-7-F
27	F1	1	10 A, 300 VAC, Fuse, Board Mount, Through Hole, MST, 8.35 x 4.30 x 7.7 mm	Conquer	MST 10A 300V
28	L1	1	100 µH, 5 A, INDUCTOR TORD HI AMP 100 µH VERT	Wurth Elect Inc	7447070
29	L2	1	Toroidal Custom CMC, Output, 1.1 mH	Power Integrations	32-00669-000
30	L3	1	10 mH, 5 A, Common Mode Choke	Wurth Elect Inc	744825510
31	L4	1	Ferrite Bead, 48 Ohms @ 100 MHz, 1 Power Line, 6 A, 5 mOhm, 1206 (3216 Metric)	Würth Elektronik	782763480
32	Q1	1	NPN, Power BJT, 70 V, 1 A, TO-92	Zetex Inc	ZTX692B
33	Q2 Q3	2	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	Infineon Tech	MMBTA06LT1
34	R1 R2	2	RES, 100k, 5%, 2/3 W, Thick Film, 1206	Panasonic	ERJ-P08J104V
35	R5	1	RES, 2 M, 1%, 1/4 W, Moisture Resistant, Thick Film, 1206 (3216 Metric)	Yageo	AC1206FR-072ML
36	R6	1	RES, 3.30 M, 1%, 1/4 W, Thick Film, 1206	Rohm Semiconductor	KTR18EZPF3304
37	R7	1	RES, 2.7 M, 5%, 1/4 W, Thick Film, 1206	YAGEO	RC1206FR-072M7L

38	R8 R9	2	RES, 20 Ohms, ±5%, 3 W, Through Hole Resistor Axial, Flame Retardant Coating, Pulse Withstanding, Safety Metal Film	TE Connectivity Passive Product	RR03J20RTB
39	R10 R13	2	RES, 200 k, 1%, 1/4 W, Thick Film, 1206	Panasonic	ERJ-8ENF2003V
40	R12	1	RES, 2.74 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF2741V
41	R14	1	RES, 100 Ohms ±1% 0.125 W, 1/8 W Chip Resistor, 0805 (2012 Metric), Thick Film	Stackpole Electronics Inc	RMCF0805FT100R
42	R15	1	RES, 4.22 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF4221V
43	R16 R17 R57	3	RES, 75 R, 5%, 2 W, Metal Oxide	Yageo	RSF200JB-75R
44	R18	1	RES, 3.30 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF3301V
45	R19	1	RES, 53.6 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF5362V
46	R20	1	RES, 1 k, 5%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6GEYJ102V
47	R21	1	RES, 3.9 k, 5%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6GEYJ392V
48	R23	1	RES, 13.3 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF1332V
49	R24	1	RES, 100 R, 1%, 1/10 W, Thick Film, 0603	Panasonic	ERJ-3EKF1000V
50	R25	1	RES, 1.00 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF1001V
51	R26	1	RES, 825 R, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF8250V
52	R27 R50	2	RES, 0.080 R, CURRENT SENSE, 2 W	Ohmite	12FR080E
53	R28	1	RES, 15 k, 5%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6GEYJ153V
54	R29	1	RES, 340 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF3403V
55	R30 R32	2	RES, 10.0 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF1002V
56	R40	1	RES, 47.0 R, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF47R0V
57	R41	1	RES, 3.32 k, 1%, 1/10 W, Thick Film, 0603	Panasonic	ERJ-3EKF3321V
58	R52	1	RES, 100 Ohms ±1% 0.25 W, 1/4 W Chip Resistor 0805 (2012 Metric), Moisture Resistant Thick Film	KOA Speer Electronics, Inc.	RK73H2ATTD1000F
59	R55	1	RES, 7.50 k, 1%, 1/8 W, Thick Film, 0805	Panasonic	ERJ-6ENF7501V
60	RT1	1	NTC Thermistor, 1 Ohms, 9 A	Epcos (TDK)	B57237S109M
61	RV1	1	275 VAC, 75 J, 14 mm, RADIAL	Littlefuse	V275LA20AP
62	T1	1	Bobbin, PQ35/35, Vertical, 12 pins (Almost identical to 25-00919-00)	TDK	B65882B0012T001
63	U1	1	CAPZero-3, CAP300DG, SO-8C	Power Integrations	CAP300DG
64	U2	1	TOPSwitchGaN, TOP7078E, eSIP-7C	Power Integrations	TOP7078E
65	U3	1	Optoisolator, Transistor Output, 5300 Vrms, 1 Channel, 4-SMD, Gull Wing	Vishay Semiconductor Opto Division	SFH6106-3T
66	U4	1	OP AMP SINGLE LOW PWR SOT23-5	Texas Instruments	LM321MF/NOPB
67	U5 U6	2	IC, REG ZENER SHUNT ADJ SOT-23	National Semiconductor	LM431BIM3/NOPB
68	VR4	1	DIODE ZENER 11 V 500 MW SOD123	Diodes, Inc	MMSZ5241B-7-F
69	VR6	1	DIODE ZENER 10 V 500 MW SOD123	Diodes, Inc	MMSZ5240B-7-F
70	VR7	1	13 V, 5%, 500 MW, SOD-123	ON Semiconductor	MMSZ4700T1G
71	VR8	1	DIODE, ZENER, 75 V, 500 MW, SOD123	ON Semi	MMSZ5267BT1G

Table 2 – Electrical Parts.

Item No.	Part Reference	Qty.	Description	Manufacturer	Mfr. Part Number
1	TP1	1	Test Point, WHT, THRU-HOLE MOUNT	Keystone	5012
2	TP2	1	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
3	SW1	1	SWITCH SLIDE SPDT 30V.2A PC MNT	E-Switch	EG1218
4	SCREW1 SCREW2 SCREW3 SCREW4	4	SCREW MACHINE PHIL 2-56 X 0.250" SS	Olander Co.	2C25PPMS
5	J2 J4	2	2 Position (1 x 2) header, 5 mm (0.196) pitch, Vertical, Screw - Rising Cage Clamp	Phoenix Contact	1715022
6	Fan	1	Fan, 12 VDC, 100 mA, Square – 50 mm L x 50 mm H, 15 mm wide, 12.5 CFM, 2 Wire Leads	GDSTIME	GDA5015

Table 3 – Miscellaneous Parts.

7 Flyback Transformer Design Spreadsheet

1	ACDC_TOPSwitch-GaN_Flyback_102425; Rev.0.4; Copyright Power Integrations 2025	INPUT	INFO	OUTPUT	UNITS	TOPSwitch-GaN Single/Multi Output Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	165		165	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			230 VAC (±30%)		Range of AC input voltage
7	LINEFREQ			60	Hz	AC Input voltage frequency
8	CAP_INPUT	240.0		360.0	μF	Input capacitor
9	VOUT	89.00		89.00	V	Output voltage at the board
10	IOUT	4.040		4.040	A	Output current
11	POUT			359.56	W	Output power
12	EFFICIENCY	0.91		0.91		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.60		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
18	**PRIMARY CONTROLLER SELECTION**					
19	PACKAGE_DEVICE	eSIP		eSIP		Device Package
20	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
21	DEVICE_GENERIC	AUTO		TOP7078		Generic device code
22	DEVICE_CODE			TOP7078E		Actual device code
23	POUT_MAX			400	W	Power capability of the device based on thermal performance
24	RDSON_100DEG			0.23	Ω	Primary switch on time drain resistance at 100 °C
25	ILIMIT_MIN			7.905	A	Minimum current limit of the primary switch
26	ILIMIT_TYP			8.500	A	Typical current limit of the primary switch
27	ILIMIT_MAX			9.095	A	Maximum current limit of the primary switch
28	VDRAIN_BREAKDOWN			800	V	Device breakdown voltage
29	VDRAIN_ON_PRSW			0.48	V	Primary switch on time drain voltage
30	VDRAIN_OFF_PRSW		Warning	655.4	V	The peak repetitive drain voltage on the switch is higher than 650 V: Decrease the device VOR
34	**WORST CASE ELECTRICAL PARAMETERS**					
35	FSWITCHING_MAX	130000		128000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage.
36	VOR	122.0		122.0	V	Secondary voltage reflected to the primary when the primary switch turns off
37	VMIN			199.80	V	Valley of the minimum input AC voltage at full load

38	KP			0.74		Measure of continuous/discontinuous mode of operation
39	MODE_OPERATION			CCM		Mode of operation
40	DUTYCYCLE			0.380		Primary switch duty cycle
41	TIME_ON_MAX			12.50	µs	Primary switch on-time
42	TIME_ON_AT_FSWITCHING_MAX			2.97	µs	Primary switch on-time at FSWITCHING_MAX
43	TIME_OFF			4.85	µs	Primary switch off-time at 165 VAC, 359.56 W, and 130000 Hz.
44	LPRIMARY_MIN			97.2	µH	Minimum primary inductance
45	LPRIMARY_TYP			104.6	µH	Typical primary inductance
46	LPRIMARY_TOL	7.0		7.0	%	Primary inductance tolerance
47	LPRIMARY_MAX			111.9	µH	Maximum primary inductance
49	**PRIMARY CURRENT**					
50	IPEAK_PRIMARY			9.066	A	Primary switch peak current
51	IPEDESTAL_PRIMARY			2.065	A	Primary switch current pedestal
52	IAVG_PRIMARY			1.911	A	Primary switch average current
53	IRIPPLE_PRIMARY			8.067	A	Primary switch ripple current
54	IRMS_PRIMARY			3.417	A	Primary switch RMS current
56	**SECONDARY CURRENT**					
57	IPEAK_SECONDARY			12.553	A	Secondary winding peak current
58	IPEDESTAL_SECONDARY			2.859	A	Secondary winding current pedestal
59	IRMS_SECONDARY			6.048	A	Secondary winding RMS current
63	**TRANSFORMER CONSTRUCTION PARAMETERS**					
64	CORE SELECTION					
65	CORE	PQ35		PQ35		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
66	CORE CODE			PQ35/35-3C95		Core code
67	AE			190.00	mm^2	Core cross sectional area
68	LE			86.10	mm	Core magnetic path length
69	AL			6600	nH/turns^2	Ungapped core effective inductance
70	VE			16300.0	mm^3	Core volume
71	BOBBIN			CPV-PQ35/35-1S-12P-Z		Bobbin
72	AW			146.64	mm^2	Window area of the bobbin
73	BW			20.80	mm	Bobbin width
74	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
76	**PRIMARY WINDING**					
77	NPRIMARY			18		Primary turns
78	BPEAK			3071	Gauss	Peak flux density
79	BMAX			2931	Gauss	Maximum flux density
80	BAC			1284	Gauss	AC flux density (0.5 x Peak to Peak)
81	ALG			323	nH/turns^2	Typical gapped core effective inductance
82	LG			0.704	mm	Core gap length

84	**PRIMARY BIAS WINDING**					
85	NBIAS_PRIMARY			2	turns	Primary bias winding number of turns
87	**SECONDARY WINDING**					
88	NSECONDARY	13		13	turns	Secondary winding number of turns
90	**SECONDARY BIAS WINDING**					
91	NBIAS_SECONDARY			3	turns	Secondary bias winding number of turns
95	**PRIMARY COMPONENTS SELECTION**					
96	LINE UNDERVOLTAGE					
97	BROWN-IN REQURED	76.00		76.00	V	Required AC RMS/DC line voltage brown-in threshold
98	RLS			7.84	MΩ	Connect two 3.92 MOhm resistors to the V-pin for the required UV/OV threshold
99	BROWN-IN ACTUAL			62.9V - 77.6V	V	Actual AC RMS/DC brown-in range
100	BROWN-OUT ACTUAL			53.6V - 66.9V	V	Actual AC RMS/DC brown-out range
102	**LINE OVERVOLTAGE**					
103	OVERVOLTAGE_LINE			295.1V - 331.2V	V	Actual AC RMS/DC line over-voltage range
105	**PRIMARY BIAS DIODE**					
106	VBIAS_PRIMARY			12.0	V	Rectified primary bias voltage
107	VF_BIAS_PRIMARY			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE_PRIMARY			55.18	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS_PRIMARY			22	µF	Bias winding rectification capacitor
110	CBP			0.47	µF	BP pin capacitor
114	**SECONDARY COMPONENTS**					
115	VREF_REG	2.50		2.50	V	Reference voltage of the feedback
116	RFB_UPPER	347.50		347.50	kΩ	Upper feedback resistor (connected to the first output voltage)
117	RFB_LOWER			10.00	kΩ	Lower feedback resistor
119	**SECONDARY BIAS DIODE**					
120	USE_SECONDARY_BIAS	YES		YES		Use secondary bias winding for the design
121	VBIAS_SECONDARY	15.0		15.0	V	Rectified secondary bias voltage
122	VF_BIAS_SECONDARY			0.70	V	Bias winding diode forward drop
123	VREVERSE_BIASDIODE_SECONDARY			77.23	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
124	CBIAS_SECONDARY			10	µF	Bias winding rectification capacitor
127	**MULTIPLE OUTPUT PARAMETERS**					
128	OUTPUT 1					
129	VOUT1			89.00	V	Output 1 voltage
130	IOUT1			4.04	A	Output 1 current
131	POUT1			359.56	W	Output 1 power
132	VD1			0.70	V	Forward voltage drop of diode for output 1
133	NS1			13.00	turns	Number of turns for output 1
134	ISPEAK1			12.55	A	Instantaneous peak value of the secondary current for output 1

135	ISRMS1			6.048	A	Root-mean-squared value of the secondary current for output 1
136	ISRIPPLE1			4.500	A	Current ripple on the secondary waveform for output 1
137	PIV1_CALCULATED			430.00	V	Computed peak inverse voltage stress on the diode for output 1
138	OUTPUT_RECTIFIER1	AUTO		DEXS-1106S		Recommended diode for output 1.
139	PIV1_RATING			600.00	V	Peak inverse voltage rating on the diode for output 1
140	TRR1			30.00	ns	Reverse recovery time of the diode for output 1
141	IFM1			10.00	A	Maximum forward continuous current of the diode for output 1
142	PLOSS_DIODE1			13.19	W	Maximum diode power loss for output 1

Table 4 – TOPSwitchGaN Flyback Transformer Design Spreadsheet.

8 Flyback Transformer Specification

8.1 Electrical Diagram

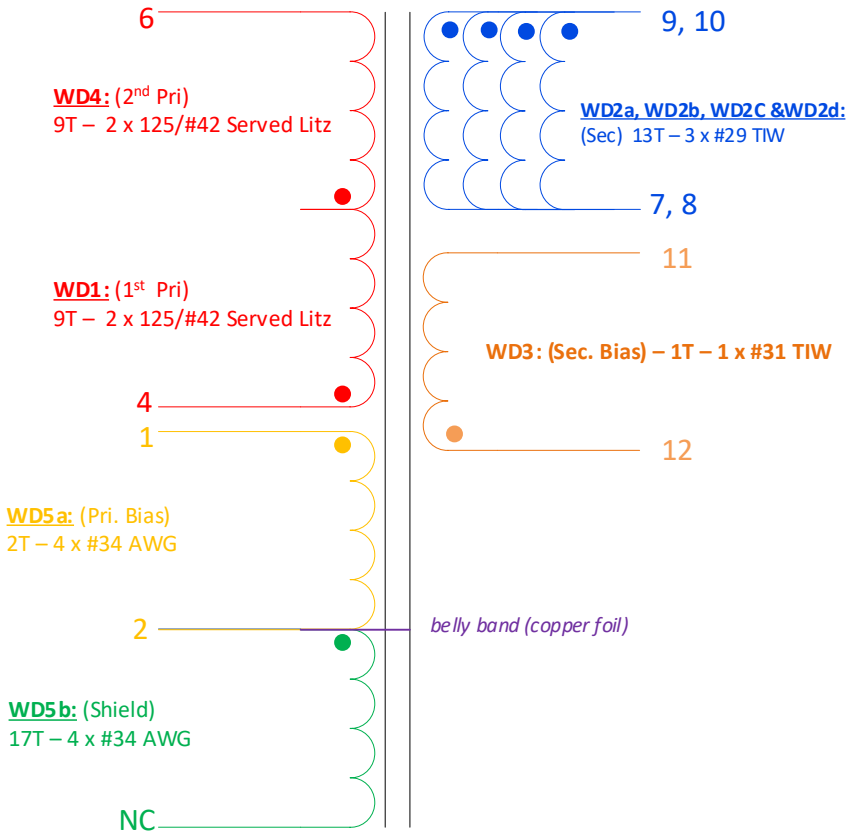


Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 4 to pin 6, with all other Windings open.	105 µH +/-5.0%
Maximum Primary Leakage	Measured between Pin 4 to Pin 6, with all other Windings shorted.	1.0 µH
Electrical Strength	60 Hz 1 second, from pins 1, 2, 4, 6 to pins 7, 8, 9, 10, 11, 12.	3000 VAC

Table 5 – Transformer Electrical Specification.

8.3 Materials

Item	Description
[1]	Core: PQ35, TDK-PC95.
[2]	Bobbin: PQ35/35-Vert-12 pins (6/6); MyCoilTech, PI#: 25-01125-00; or equivalent.
[3]	Magnet wire: #34 AWG, double coated.
[4]	Magnet wire: 125/#42 Served Litz.
[5]	Magnet wire: #29AWG_TIW.
[6]	Magnet wire: #31AWG_TIW.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 22.0 mm width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 12.0 mm width.
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 36.0 mm width.
[10]	Copper foil: 2 mil thick, 12 m wide.
[11]	Varnish: Dolph BC-359.

Table 6 – Transformer Materials List.

8.4 Transformer Build Diagram

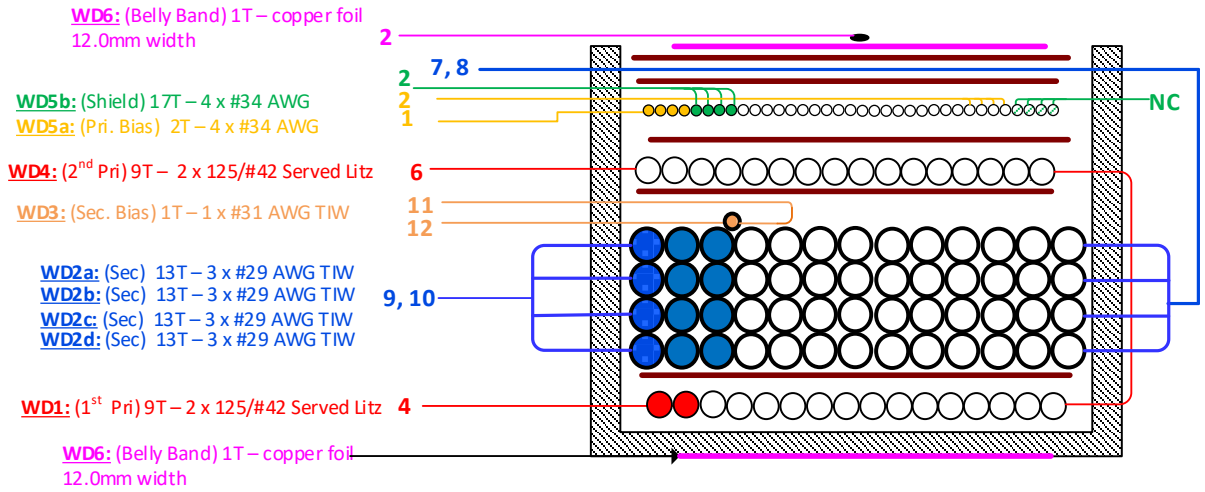
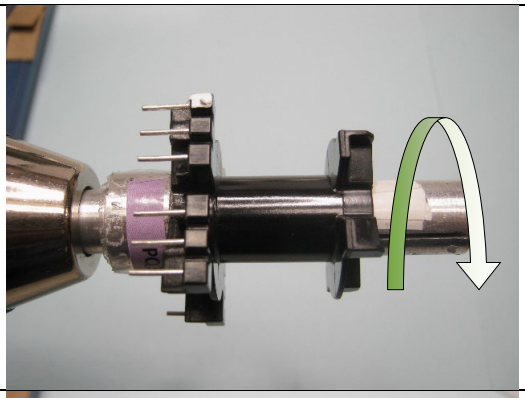
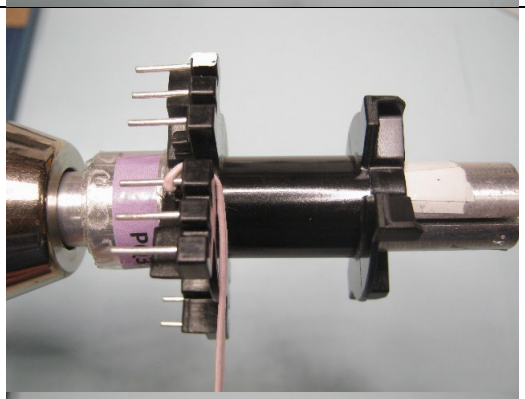
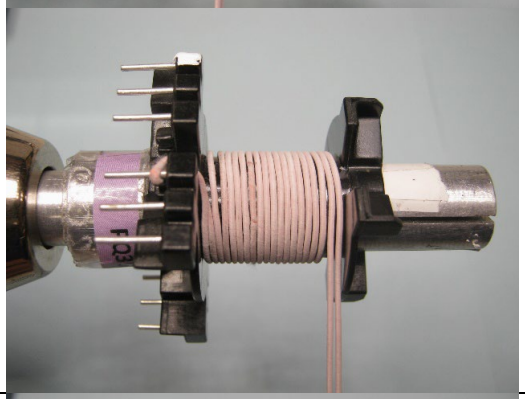
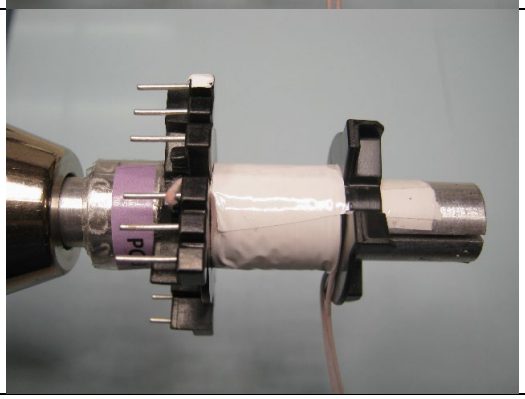


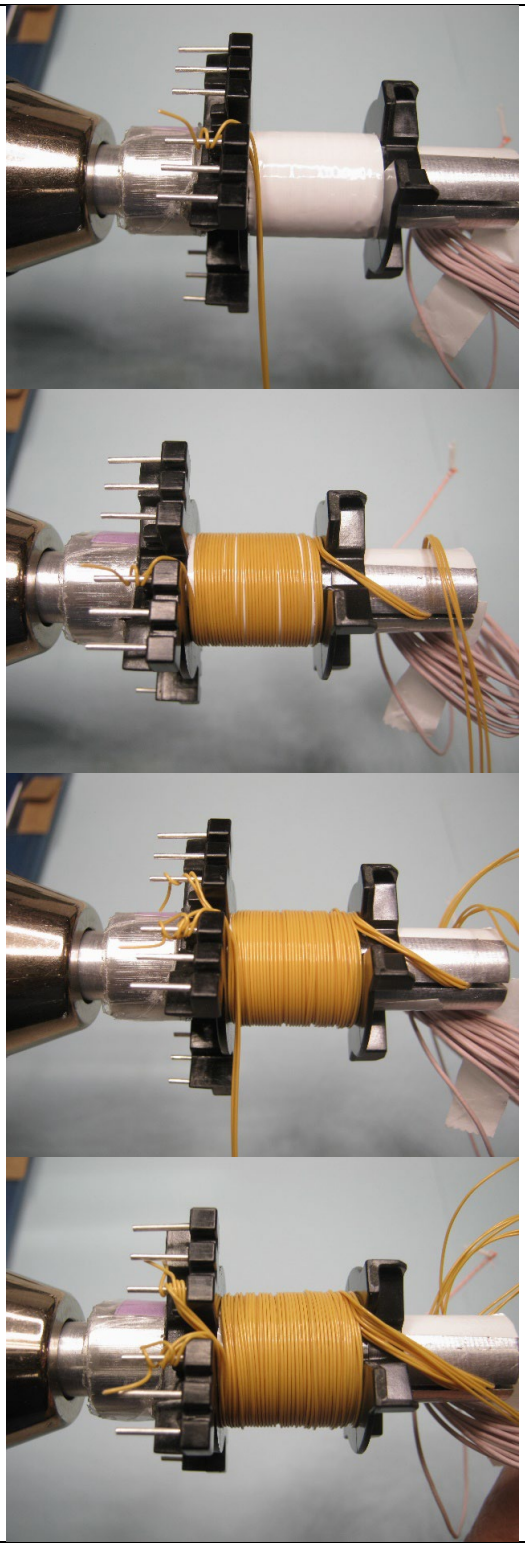
Figure 8 – Transformer Build Diagram.

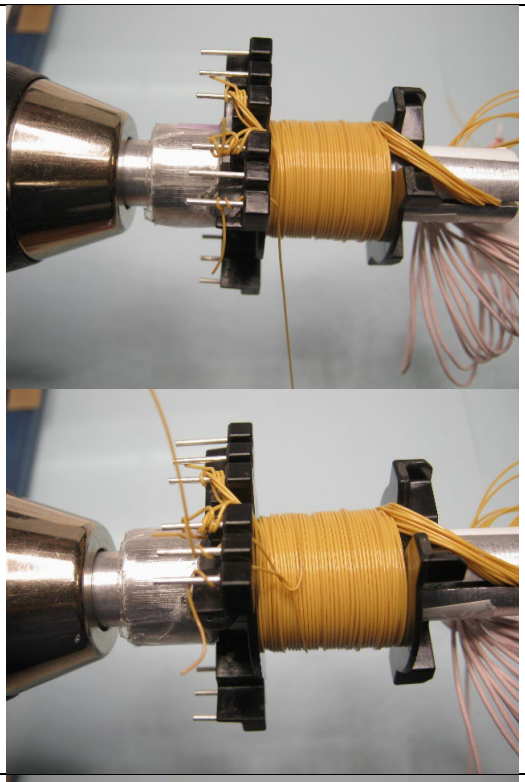
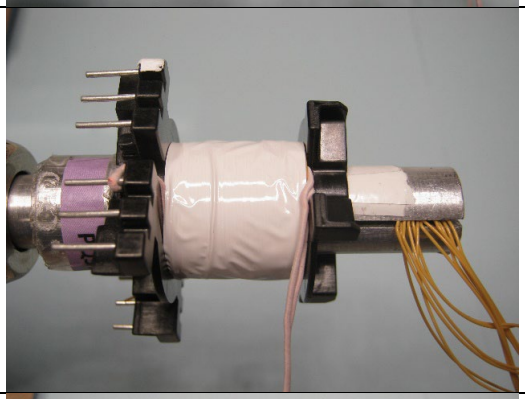
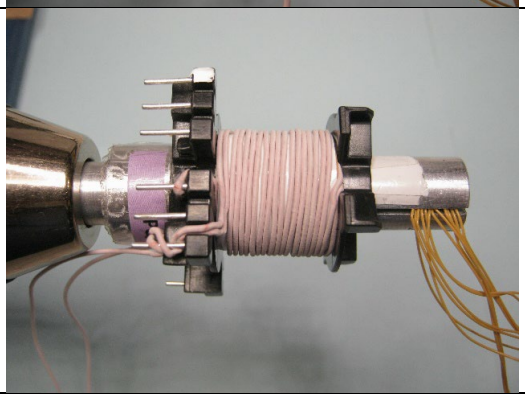
8.5 Winding Instructions

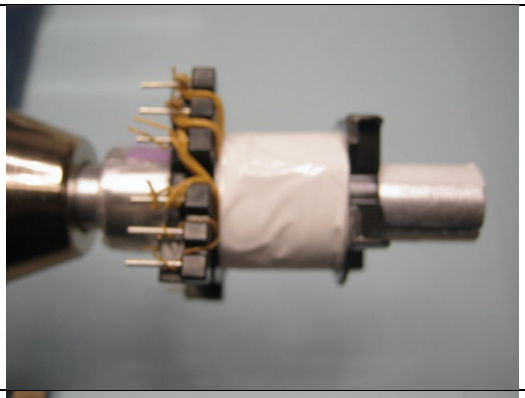
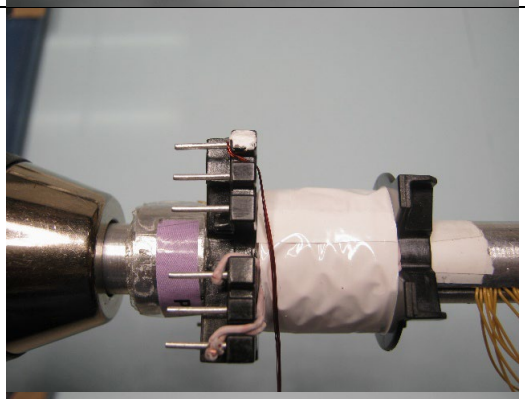
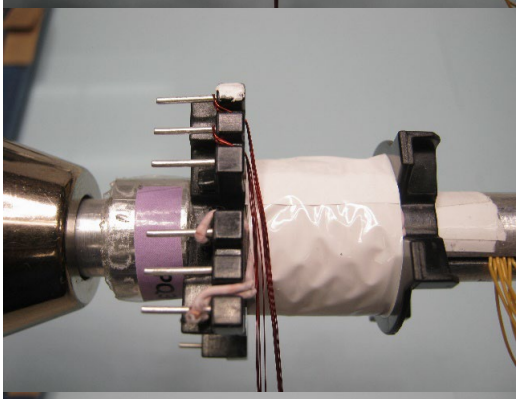
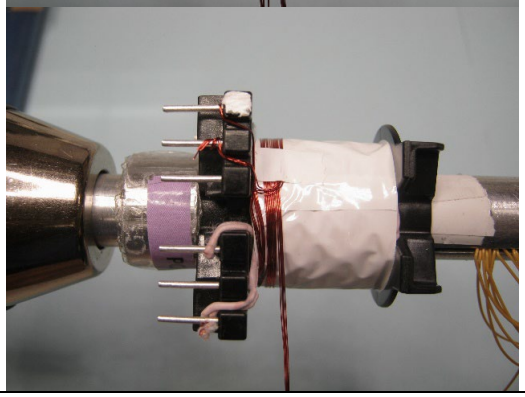
WD1 1st Primary	Start at pin 4, use 2 wires item [4] wind 9 turns in 1 layer, from left to right, spread the wires evenly across the width of bobbin. At the last turn, exit the wires, and leave enough length of wire-floating for WD4-2nd Primary.
Insulation	1 layer of tape item [7].
WD2a, WD2b, WD2c, WD2d Secondary	Use 3 wires item [5], start at pin 10, wind 13 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40 mm floating for WD2a. Repeat the same winding above on top previous winding for WD2b. Also repeat the same winding above for WD2c, WD2d but start at pin 9.
WD3 Sec-Bias	Start at pin 12, wind 1 turn of wire item [6] and end at pin 11, should cross or twist end lead with start lead before termination to pins.
Insulation	1 layer of tape item [7].
WD4 2nd Primary	Use floating wires from WD1-1st Primary, wind 9 turns from right to left, spread the wires evenly across the width of bobbin, and finish at pin 6.
Insulation	1 layer of tape item [7].
WD5a: Bias & WD5b: Shield	Use 4 wires item [3] start at pin 1 for Bias winding, also use 4 wires same item [3] start at pin 2 for Shield winding. Wind all 8 wires in parallel, - at the 2nd turn, place 1 small pcs of tape to hold all wires, bring 4 wires for Bias winding to the left and terminate at pin 2, - continue winding to 17th turn, cut short 4 wires for Shield1 Winding as No-Connect
Insulation	1 layer of tape item [7] and bring fly wires from Secondary windings to left and terminate at pins 7 and 8.
Finish	Gap core halves to get 105 μH. Place 2 layers of tape item [8] inside and 1 layer outside on core which is placed on pin side of bobbin. (Refer to the images in the Winding Illustrations section) Secure cores with tape. Place 1 turn copper foil of tape item [10] around body of transformer for WD6, solder at join to make close loop. Soler wire item [3] to copper foil and pin 2. Wrap around the body of transformer 2 layers of tape item [9] Varnish with item [10].

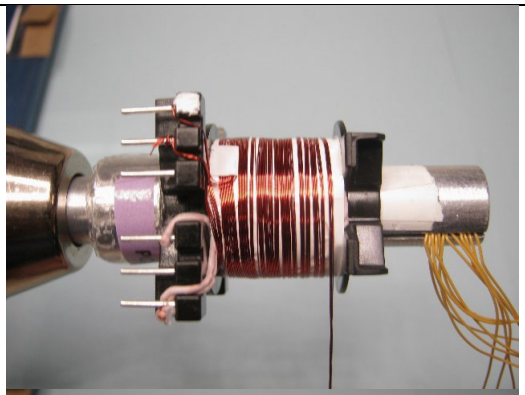
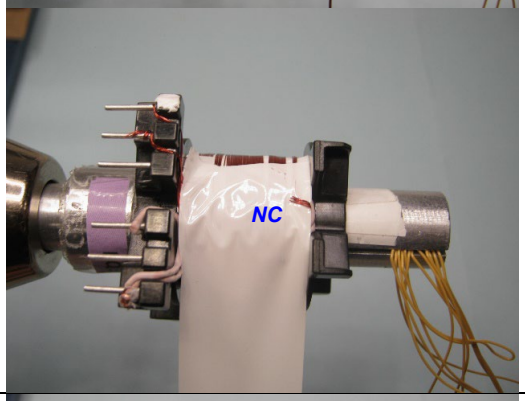
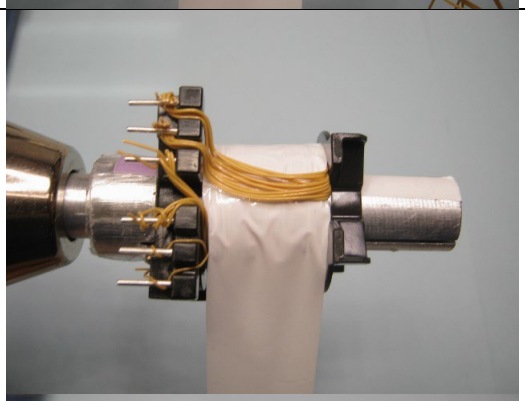
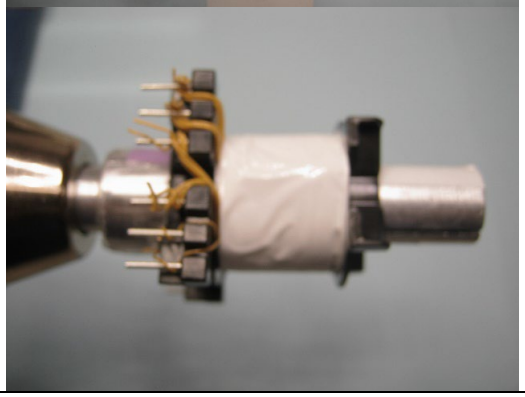
8.6 Winding Illustrations

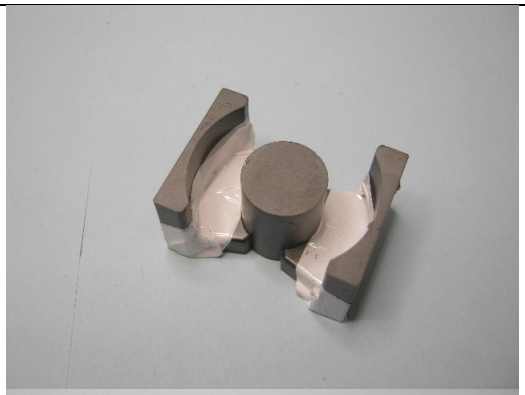
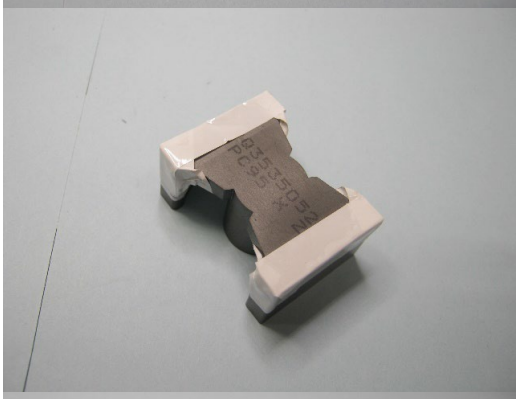
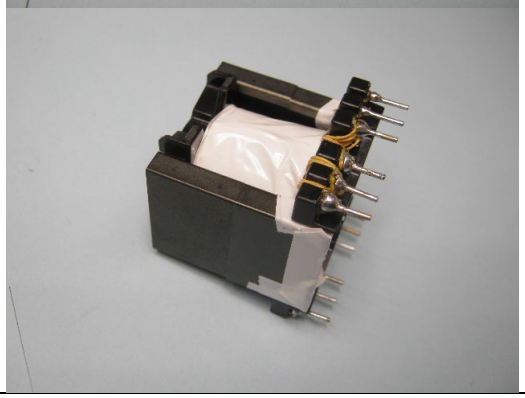
Winding preparation		Position the bobbin item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.
WD1 **1st Primary**	 	Start at pin 4, use 2 wires item [4] wind 9 turns in 1 layer, from left to right, spread the wires evenly across the width of bobbin. At the last turn, exit the wires, and leave enough length of wire-floating for WD4-2nd Primary.
Insulation		1 layer of tape item [7].

WD2a, WD2b, WD2c, WD2d Secondary		Use 3 wires item [5], start at pin 10, wind 13 turns, from left to right with tight tension. At the last turn, exit the wire on right slot and leave ~ 40 mm floating for WD2a. Repeat the same winding above on top previous winding for WD2b. Also repeat the same winding above for WD2c, WD2d but start at pin 9.

WD3 **Sec-Bias**		Start at pin 12, wind 1 turn of wire item [6] and end at pin 11, should cross or twist end lead with start lead before termination to pins.
Insulation		1 layer of tape item [7].
WD4 **2nd Primary**		Use floating wires from WD1-1st Primary, wind 9 turns from right to left, spread the wires evenly across the width of bobbin, and finish at pin 6.

Insulation		1 layer of tape item [7].
WD5a: Bias **&** **WD5b: Shield**	  	Use 4 wires item [3] start at pin 1 for Bias winding, also use 4 wires same item [3] start at pin 2 for Shield winding. Wind all 8 wires in parallel, - at the 2nd turn, place 1 small pcs of tape to hold all wires, bring 4 wires for Bias winding to the left and terminate at pin 2, - continue winding to 17th turn, cut short 4 wires for Shield1 Winding as No-Connect

	 	
Insulation	 	1 layer of tape item [7] and bring fly wires from Secondary windings to left and terminate at pins 7 and 8.

Finish		  	Gap core halves to get 105 μH. Place 2 layers of tape item [8] inside and 1 layer outside on core which is placed on pin side of bobbin. *(see pictures beside).*

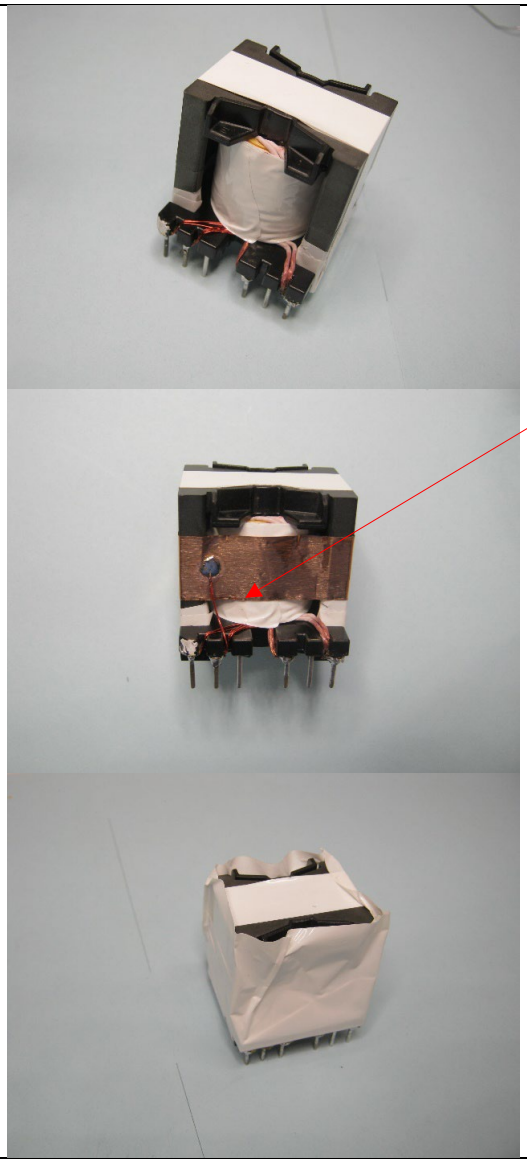
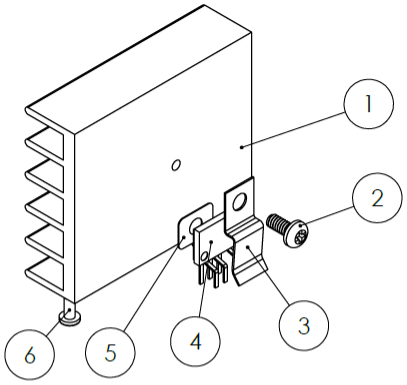
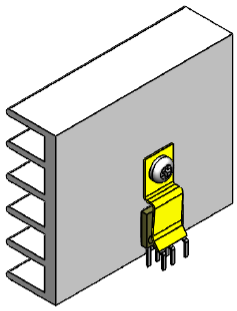
Finish (cont'd)		Secure cores with tape. Place 1 turn copper foil of tape item [10] around body of transformer for WD6, solder at join to make close loop. Solder wire item [3] to copper foil and pin 2. Wrap around the body of transformer 2 layers of tape item [9] Varnish with item [10].

Table 7 – Transformer Winding Illustrations.

9 Heatsink Assembly

9.1 TOPSwitchGaN IC Heatsink Assembly





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00423-00	DER-1019_revE_TopSwitch HEATSINK	1
2	75-00001-00	Machine screw #4-40 x .250	1
3	60-00042-00	eSIP-7C Edge Clip	1
4	10-01639-00	TOPSwitchGaN, TOP7078E, eSIP-7C	1
5	66-00120-00	Wakefield_Thermal_Joint_Compound	1
6	75-00173-00	SCREW #2-56 X .250	2

MATERIAL:
trimmed from heat sink stock
P/I: 61-00387-00

Drawn By: Hung D Nguyen

Date: Jan 27 2026

Checked by: Loi

General Tolerances

.XX ± .01

Do not Scale Drawing

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138

DER 1019 TOPSW Heat Sink Assembly

PI Part NO. 61-00423-02

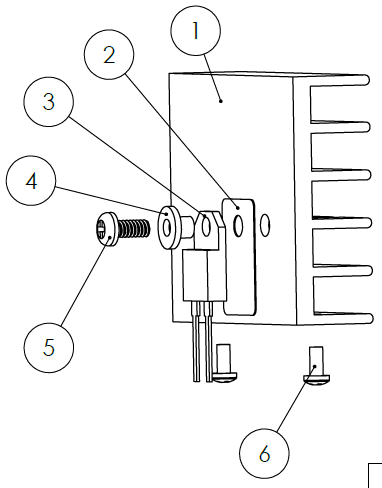
REV A

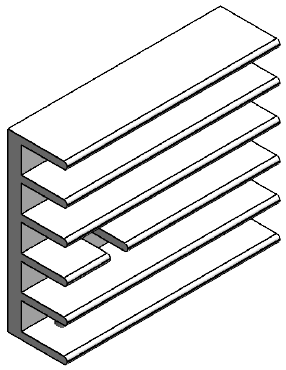
WEIGHT:

SHEET 1 OF 1

Figure 9 – Heatsink Assembly and BOM.

9.2 Flyback Output Diode (D4) Heatsink Assembly





ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00424-00	DER-1019_revE_Diodes HEATSINK	1
2	66-00096-00	THERMAL PAD-BER103, 0.009-THK	1
3	15-00823-00	600 V, 12 A, Ultrafast Recovery, 45 ns, TO-220AC	1
4	75-00154-00	Washer,Shoulder, #4, 0.125 Shoulder x 0.140 Dia, Polyphenylene Sulfide PPS	1
5	75-00001-00	Machine screw #4-40 x .250	1
6	75-00173-00	SCREW #2-56 X .250	2

MATERIAL:
trimmed from heat sink stock
P/I: 61-00387-00

Drawn By: Hung D Nguyen

Date: Jan 27 2026

Checked by: Loi

General Tolerances

.XX ± .01

Do not Scale Drawing

power integrations

5245 Hellyer Avenue.
San Jose, CA 95138

DER 1019 Diode Heat Sink Assembly

PI Part NO. 61-00424-02

REV A

WEIGHT:

SHEET 1 OF 1

Figure 10 – Output Diode (D4) Heatsink Assembly and BOM.

10 Plastic Housing Mechanical Outline

10.1 Top Case Mechanical Outline

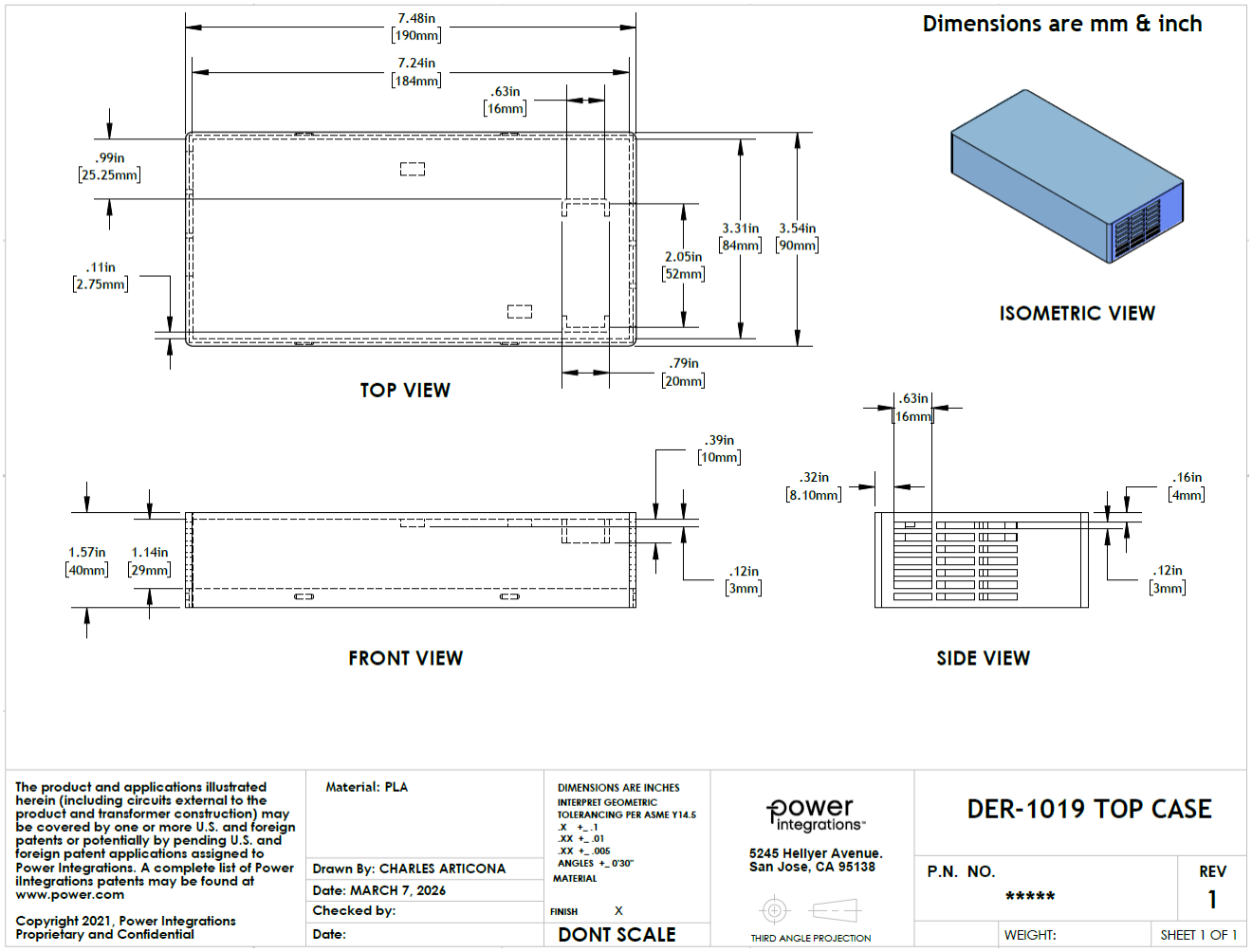


Figure 11 – Top Case Mechanical Outline.

10.2 Bottom Case Mechanical Outline

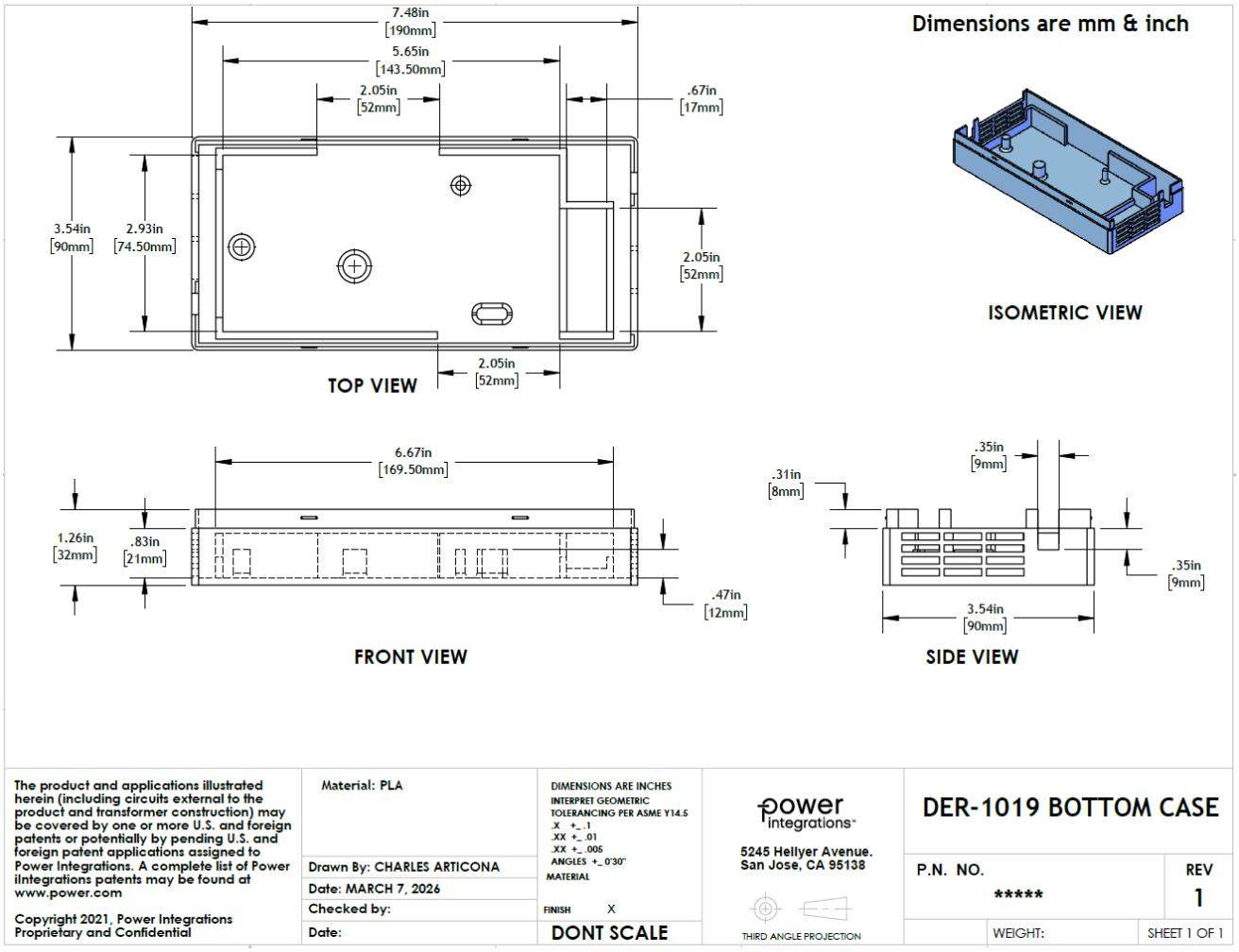


Figure 12 – Top Case Mechanical Outline.

11 Performance Data

11.1 Efficiency at Full Load

Note: Testing was performed with the DER-1019 unit mounted inside the plastic enclosure and operating a 12 V, 0.1 A (1.2 W) cooling fan powered by the unit. The 1.2 W fan consumption is not included as part of the useful output load and is treated as a loss in the efficiency measurement. Excluding the fan power consumption increases the measured full load efficiency by approximately 0.3%.

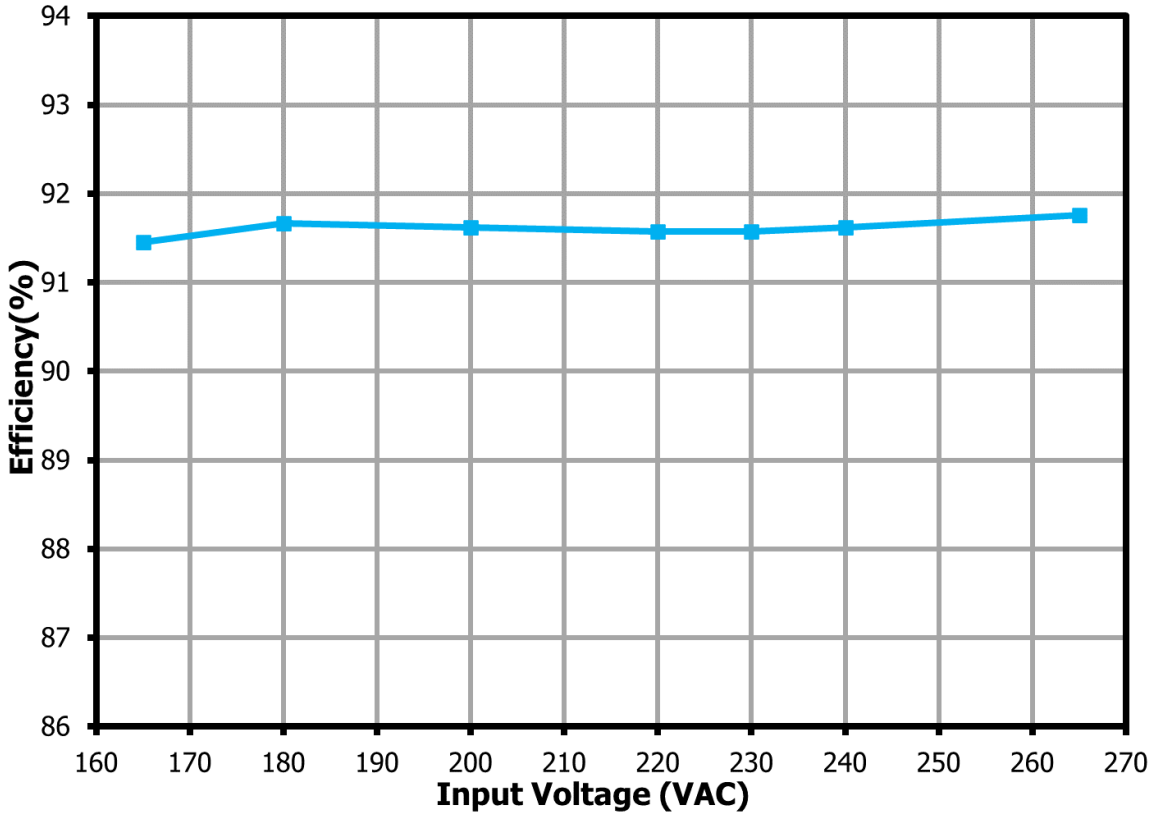


Figure 13 – Efficiency vs. Input Line Voltage at Full Load.

11.2 Efficiency vs Output Load

Note: Testing was performed with the DER-1019 unit mounted inside the plastic enclosure and operating a 12 V, 0.1 A (1.2 W) cooling fan powered by the unit. The 1.2 W fan consumption is not included as part of the useful output load and is treated as a loss in the efficiency measurement. Excluding the fan power consumption increases the measured full load efficiency by approximately 0.3%.

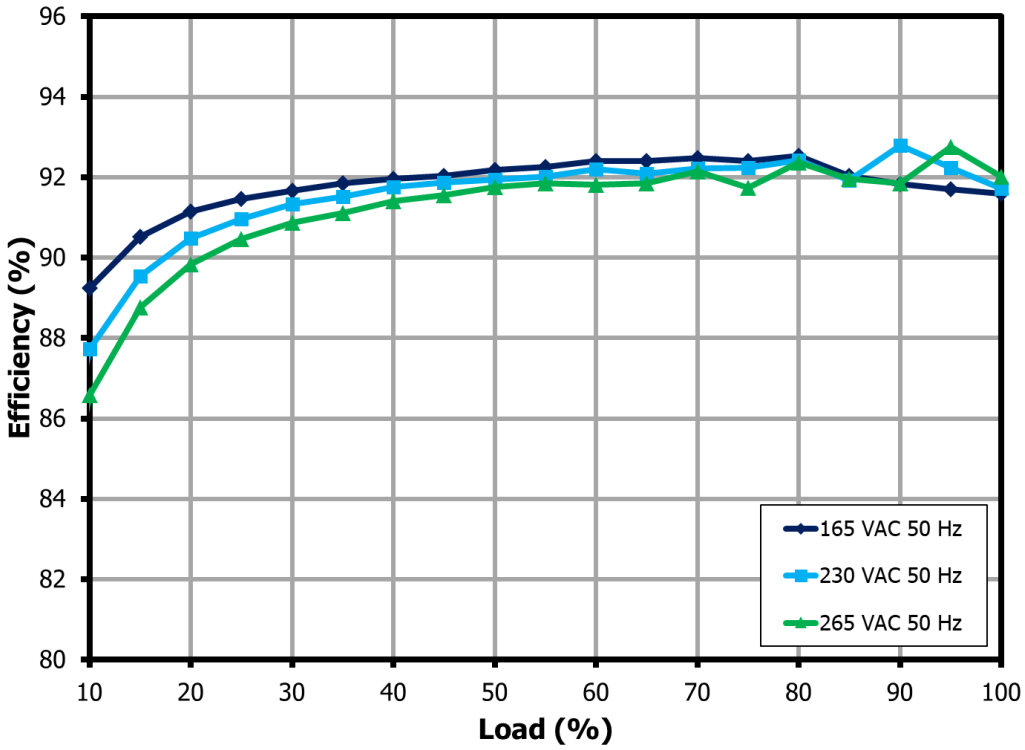


Figure 14 – Efficiency vs. Output Load.

11.3 Output Voltage Regulation vs Input Line

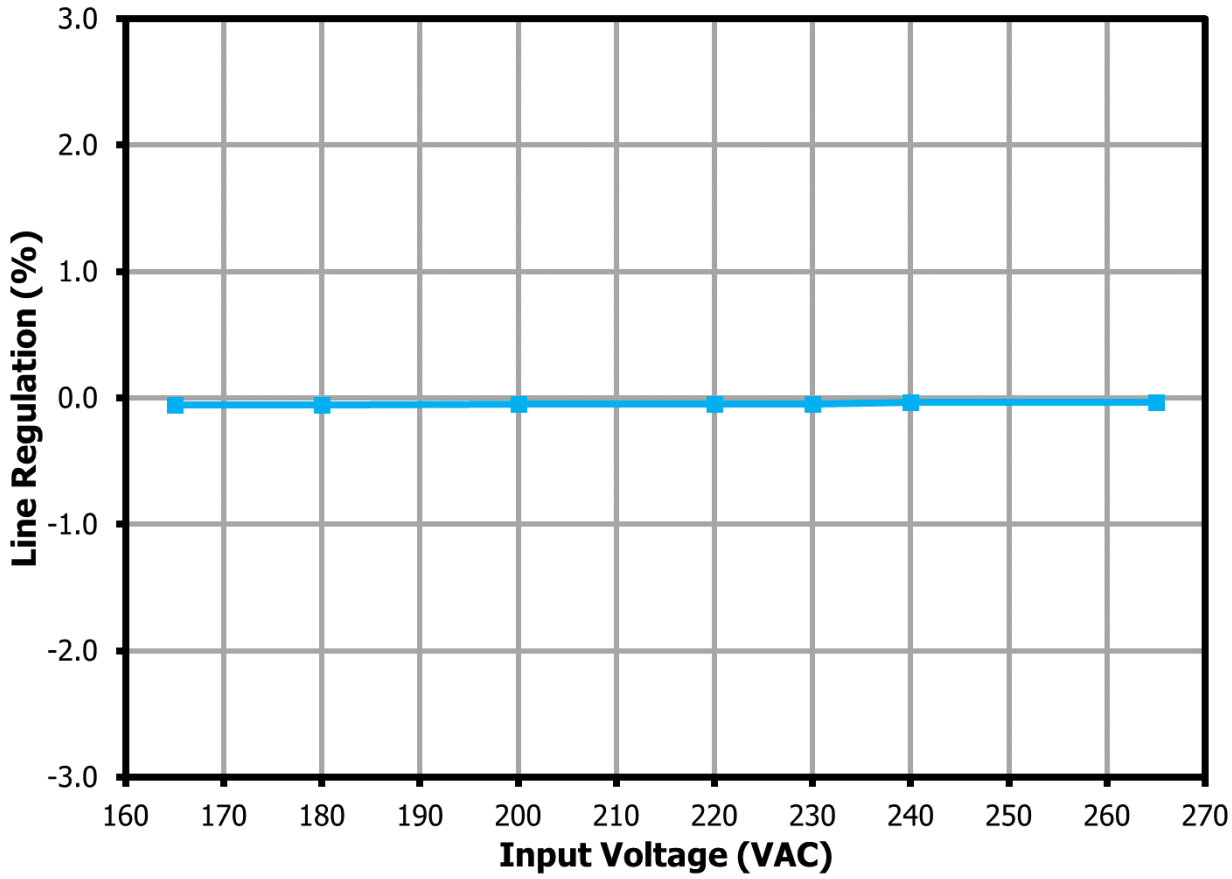


Figure 15 – Output Voltage Regulation vs Input Line at Full Load.

11.4 Output Voltage Regulation vs Output Load

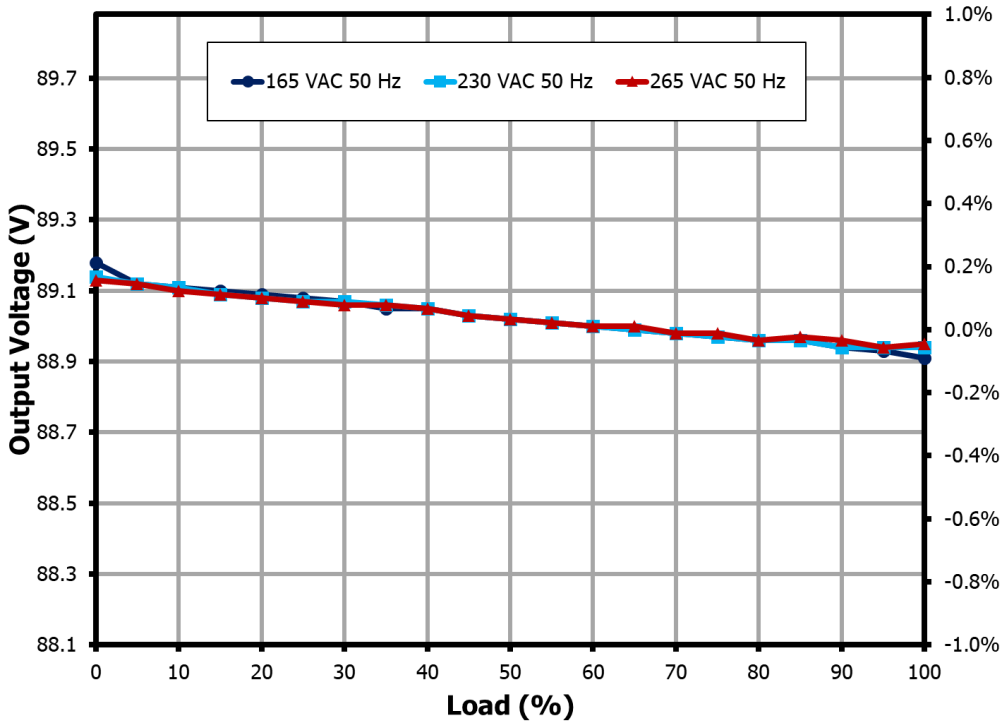


Figure 16 – Output Voltage Regulation vs Output Load.

11.5 Energy Efficiency Performance

11.5.1 Average Efficiency

The DER-1019 design easily meets the DOE Level VI average-efficiency requirements, with approximately 4% margin.

Note: Testing was performed with the DER-1019 unit mounted inside the plastic enclosure and operating a 12 V, 0.1 A (1.2 W) cooling fan, powered by the unit. The 1.2 W fan consumption is not included as part of the useful output load and is treated as a loss in the efficiency measurement. Excluding the fan power consumption increases the measured full load efficiency by approximately 0.3%.

Input: 165 VAC							
Load	**P_{IN}**	**Vo**	**Io**	**Po**	**Efficiency**	**Average Efficiency**	**DOE6 Limit**
(%)	**(W)**	**(V)**	**(A)**	**(W)**	**(%)**	**(%)**	**(%)**
100	390	88.9	4.01	357	91.5	**91.9**	87.5
75	289	89.0	3.00	267	92.3		
50	193	89.0	2.00	178	92.1		
25	97	89.1	1.00	89	91.5		
10	39	89.1	0.39	35	89.3	---	---
Input: 230 VAC							
Load	**P_{IN}**	**Vo**	**Io**	**Po**	**Efficiency**	**Average Efficiency**	**DOE6 Limit**
(%)	**(W)**	**(V)**	**(A)**	**(W)**	**(%)**	**(%)**	**(%)**
100	389	89.0	4.01	357	91.6	**91.7**	87.5
75	290	89.0	3.00	267	92.2		
50	194	89.0	2.00	178	91.9		
25	98	89.1	1.00	89	91.1		
10	40	89.1	0.39	35	87.7	---	---
Input: 265 VAC							
Load	**P_{IN}**	**Vo**	**Io**	**Po**	**Efficiency**	**Average Efficiency**	**DOE6 Limit**
(%)	**(W)**	**(V)**	**(A)**	**(W)**	**(%)**	**(%)**	**(%)**
100	388	89.0	4.01	357	91.9	**91.5**	87.5
75	291	89.0	3.00	267	91.7		
50	194	89.0	2.00	178	91.7		
25	98	89.1	1.00	89	90.6		
10	40	89.1	0.39	35	86.6	---	---

Table 8 – Average Efficiency.

11.5.2 No Load Input Power

Tested without the 12 V cooling fan. The DER-1019 design easily meets the DOE Level VI no load input power requirements (500 mW).

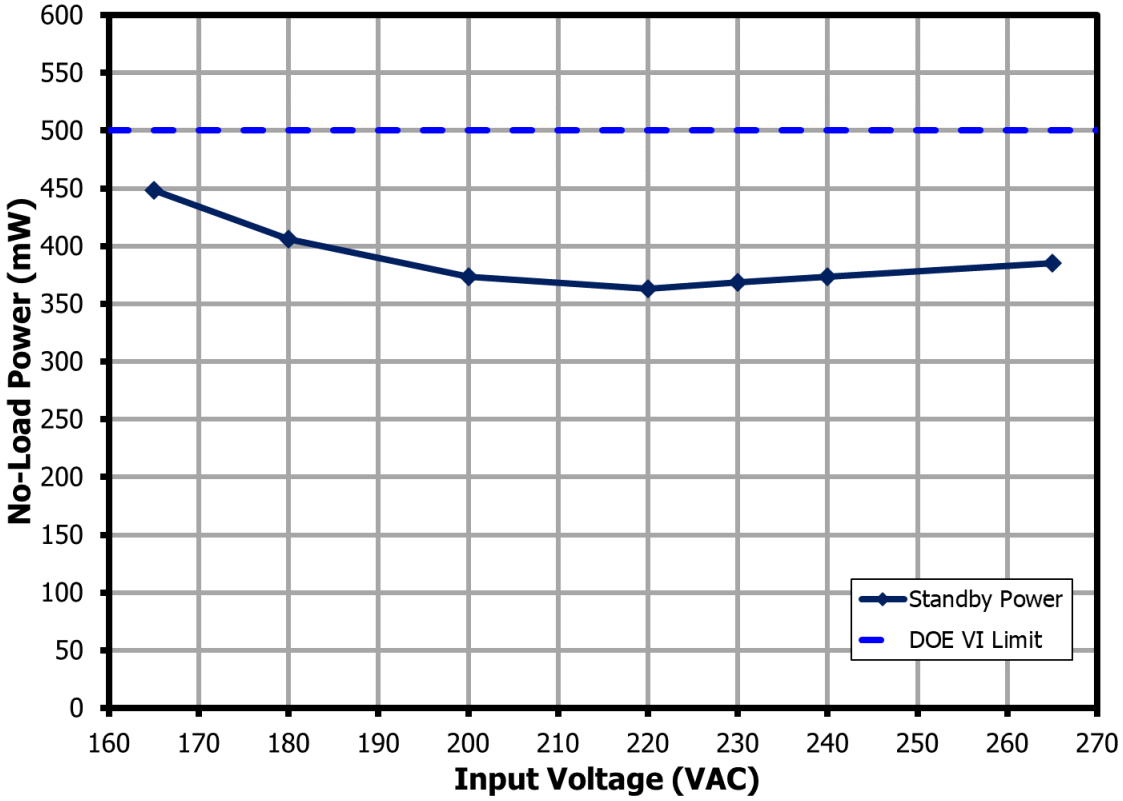


Figure 17 – No Load Input Power vs. Input Voltage.

11.6 Output Ripple Voltage vs. Output Load

Output ripple voltage is measured on the board using a voltage probe which has an added 47 µF electrolytic capacitor and a 100 nF ceramic capacitor connected across the probe tip to reduce periodic and random noise. See Section 12.8 for the test setup and ripple-voltage waveforms.

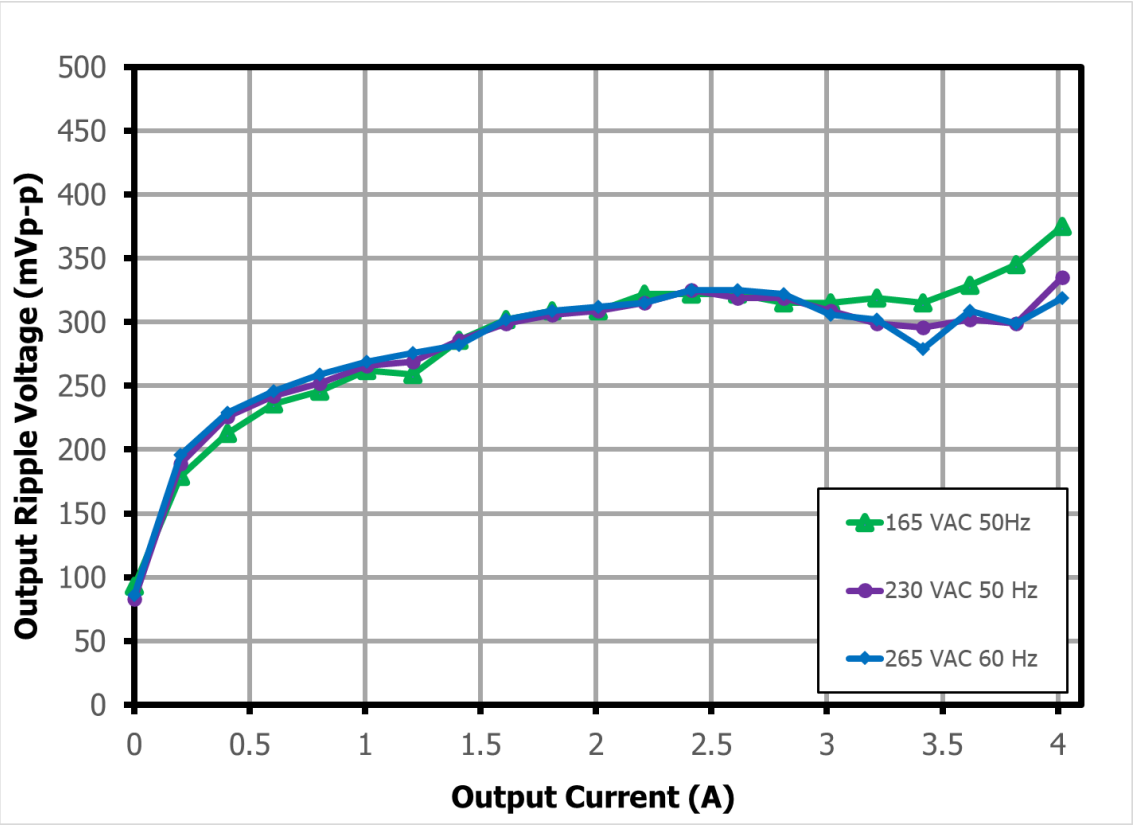


Figure 18 – Output Ripple Voltage vs Output Load Current.

11.7 Dynamic Load Performance Data

Various frequency dynamic load response was measured using an electronic load in dynamic-constant-current mode. This test shows PSU performance by describing output overshoot and undershoot during load steps. The duty cycle was 50% and the load-step slew rate was in 800 mA/μs. The output-voltage waveform was measured directly on the board. See sample waveforms on section 12.

11.7.1 0% - 100% Dynamic Load

1 kHz, 50% Duty Cycle, 0 - 100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN\ (RMS)}$	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.53	196	89.9	87.4	1.01	-1.80
200	50	200	2.26	196	89.9	87.2	1.01	-2.02
230	60	230	2.04	196	89.9	87.4	1.01	-1.80
265	50	265	1.82	195	89.9	87.4	1.01	-1.80
500 Hz, 50% Duty Cycle, 0 - 100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN\ (RMS)}$	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.36	196	89.9	87.4	1.01	-1.80
200	50	200	2.46	196	89.9	87.5	1.01	-1.69
230	60	230	2.04	195	89.9	87.5	1.01	-1.69
265	50	265	1.95	195	89.9	87.5	1.01	-1.69
200 Hz, 50% Duty Cycle, 0 - 100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN\ (RMS)}$	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.59	196	89.9	87.5	1.01	-1.69
200	50	200	2.40	196	89.9	87.5	1.01	-1.69
230	60	230	2.08	195	89.9	87.5	1.01	-1.69
265	50	265	1.89	195	89.9	87.5	1.01	-1.69
10Hz, 50% Duty Cycle, 0 - 100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN\ (RMS)}$	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.71	164	89.9	87.4	1.01	-1.80
200	50	200	2.66	194	89.9	87.4	1.01	-1.80
230	60	230	2.38	168	89.9	87.5	1.01	-1.69
265	50	265	2.30	188	89.9	87.5	1.01	-1.69

Table 9 – Overshoot/Undershoot Voltage Data During 0-100% Dynamic Loading.

11.7.2 10% - 100% Dynamic Load

1 kHz, 50% Duty Cycle, 10% -100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.68	215	89.9	87.4	1.01	-1.80
200	50	200	2.54	215	89.9	87.2	1.01	-2.02
230	60	230	2.25	215	89.9	87.4	1.01	-1.80
265	50	265	2.10	214	89.9	87.4	1.01	-1.80
500 Hz, 50% Duty Cycle, 10% -100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.53	214	89.9	87.5	1.01	-1.69
200	50	200	2.61	215	89.9	87.5	1.01	-1.69
230	60	230	2.25	215	89.9	87.5	1.01	-1.69
265	50	265	2.00	214	89.9	87.5	1.01	-1.69
200 Hz, 50% Duty Cycle, 10% -100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	2.92	215	89.9	87.4	1.01	-1.80
200	50	200	2.59	215	89.9	87.5	1.01	-1.69
230	60	230	2.31	216	89.9	87.5	1.01	-1.69
265	50	265	2.15	214	89.9	87.5	1.01	-1.69
10 Hz, 50% Duty Cycle, 10% -100% Dynamic Load								
Input		**Input Measurement**			**V_{OUT}**		**% V_{OUT}**	
VAC (RMS)	Freq (Hz)	V_{IN} (RMS)	L_{IN} (mA)	P_{IN} (W)	MAX	MIN	MAX	MIN
165	50	165	3.05	208	90	87.5	1.12	-1.69
200	50	200	2.89	186	89.9	87.5	1.01	-1.69
230	60	230	2.70	194	89.9	87.4	1.01	-1.80
265	50	265	2.36	205	89.9	87.5	1.01	-1.69

Table 10 – Overshoot/Undershoot Voltage Data During 10-100% Dynamic Loading.

11.8 Output CVCC Characteristic Curve

Note: The constant-voltage/constant-current (CVCC) characteristic curve was measured using an electronic load (E-load) configured in constant-resistance (CR) mode. CVCC measurements at very low output voltage could not be captured due to E-load limitations. However, manual measurements confirmed that constant-current regulation remains accurate down to zero volts output.

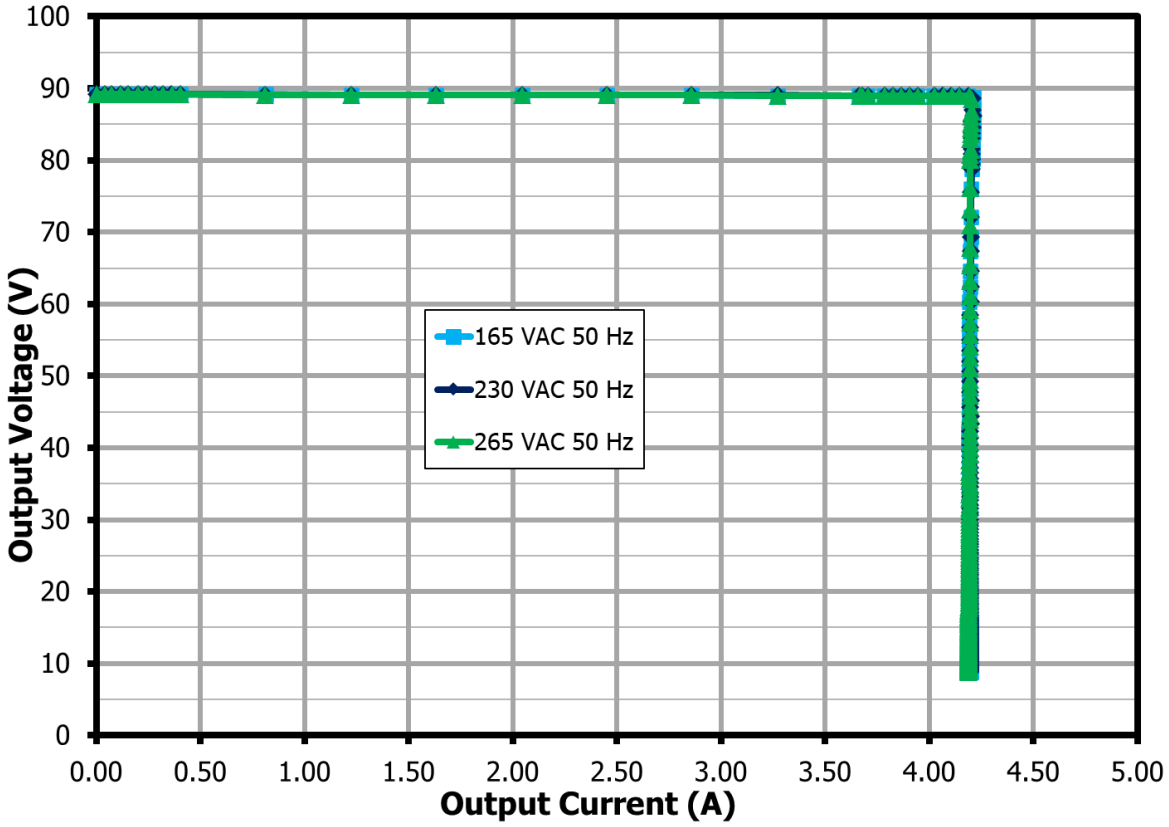


Figure 19 – CV/CC Curve at Different Input Line.

11.9 Thermal Performance at 40 °C Ambient Temperature

The power supply unit (PSU) was placed inside an enclosed plastic housing and then positioned in an environmental chamber set to a static temperature of 40 °C. The unit was powered using an E-load delivering 356 W output power. The component thermal profile was recorded after until unit stabilized.

Note: A 12 V, 0.1 A (1.2 W) cooling fan was required during thermal testing. The TOPSwitchGaN IC OTP would be triggered if the fan was not connected.

Part Reference	Qty.	Description	Manufacturer	Mfr. Part Number
Fan	1	Fan, 12 VDC, 100 mA, Square – 50 mm L x 50 mm H, 15 mm wide, 12.5 CFM, 2 Wire Leads	GDSTIME	GDA5015

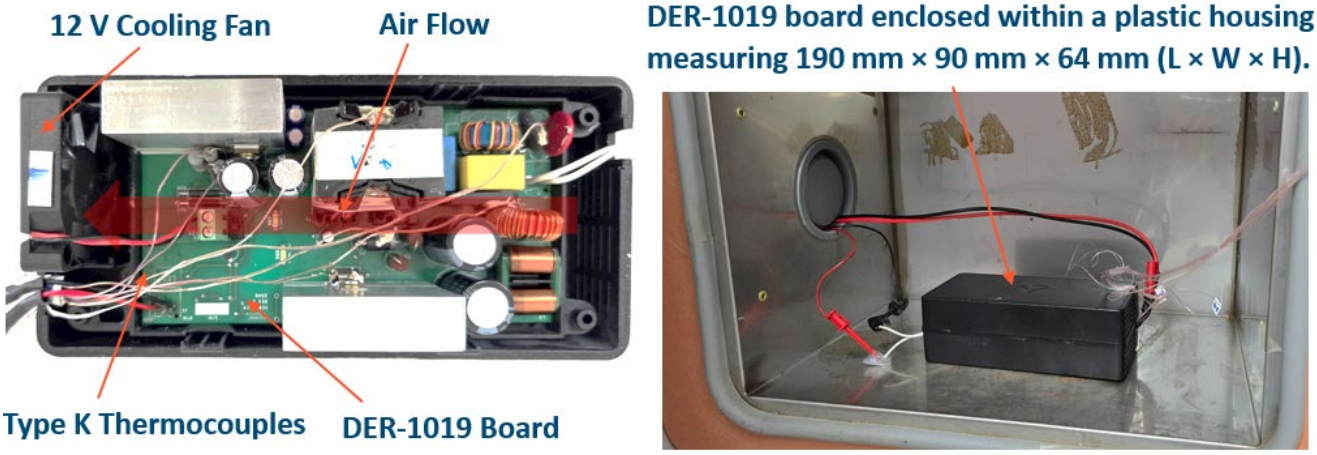


Figure 20 – Thermal Scan Test Set-up at 40 °C Ambient.

11.9.1 Thermal Test Data Summary at 40 °C Ambient Temperature

The thermal scan data in Table 11 shows that components remained well below their maximum temperature ratings across the entire input voltage range.

Item	Component Description	Thermal Data (°C)		
		165 VAC	230 VAC	265 VAC
1	BR1 - Bridge Diode	117	94	90
2	D4 - Output Diode	108	102	104
3	T1- Flyback Transformer	97	94	102
4	U2 - TOPSwitchGaN	88	88	83
5	D1 - Primary Snubber Diode	86	78	78
6	RT1 - Inrush Current Limiter	125	110	109
7	AMB - Ambient Operating Temperature	42	42	43

Table 11 – Thermal Test Data at 40 °C Ambient Temperature.

11.9.2 Component Thermal Profile at 40 °C Ambient Temperature

The thermal charts in the following figures illustrate the temperature profile of the DER-1019 heating components. All component temperatures stabilized after 60 minutes, and the measured values remained well below their specified limits.

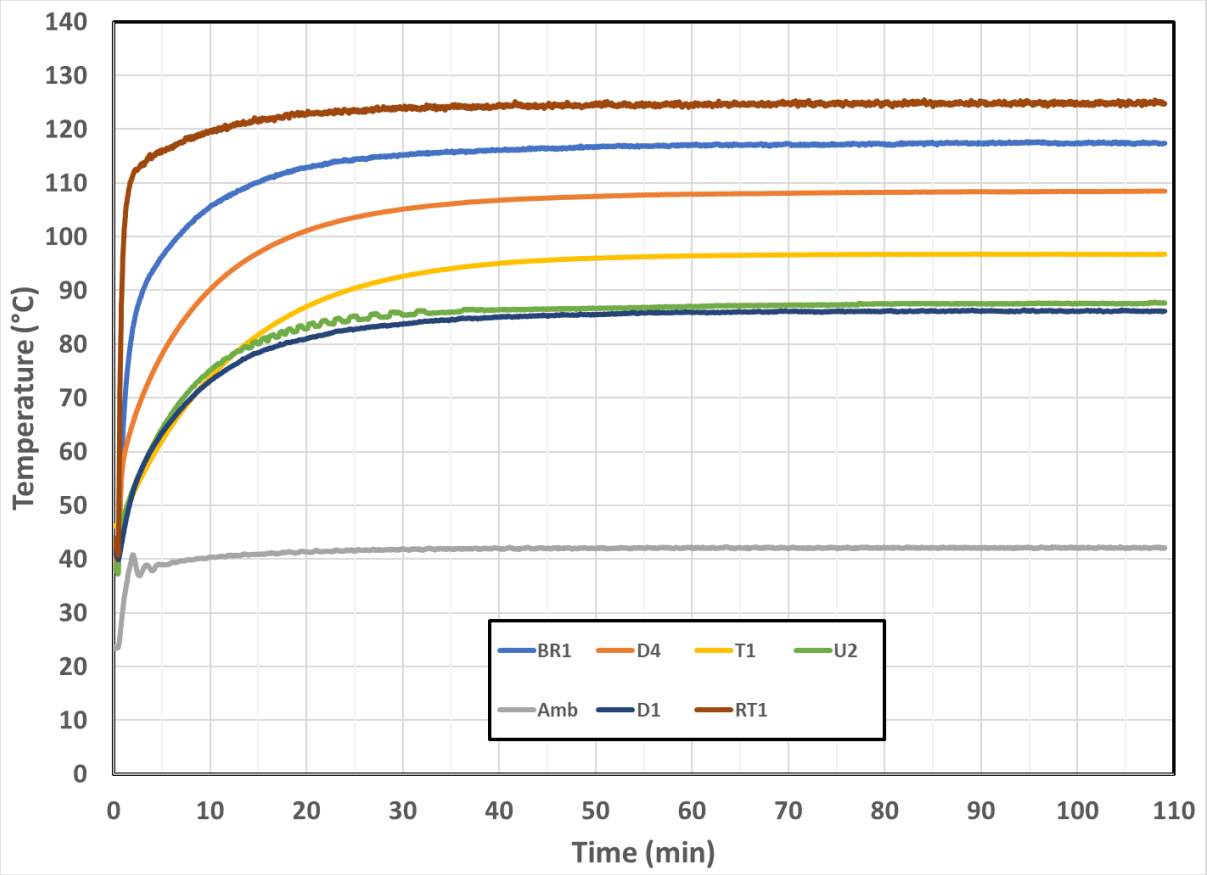


Figure 21 – Thermal Profile at 165 VAC, Full Load.

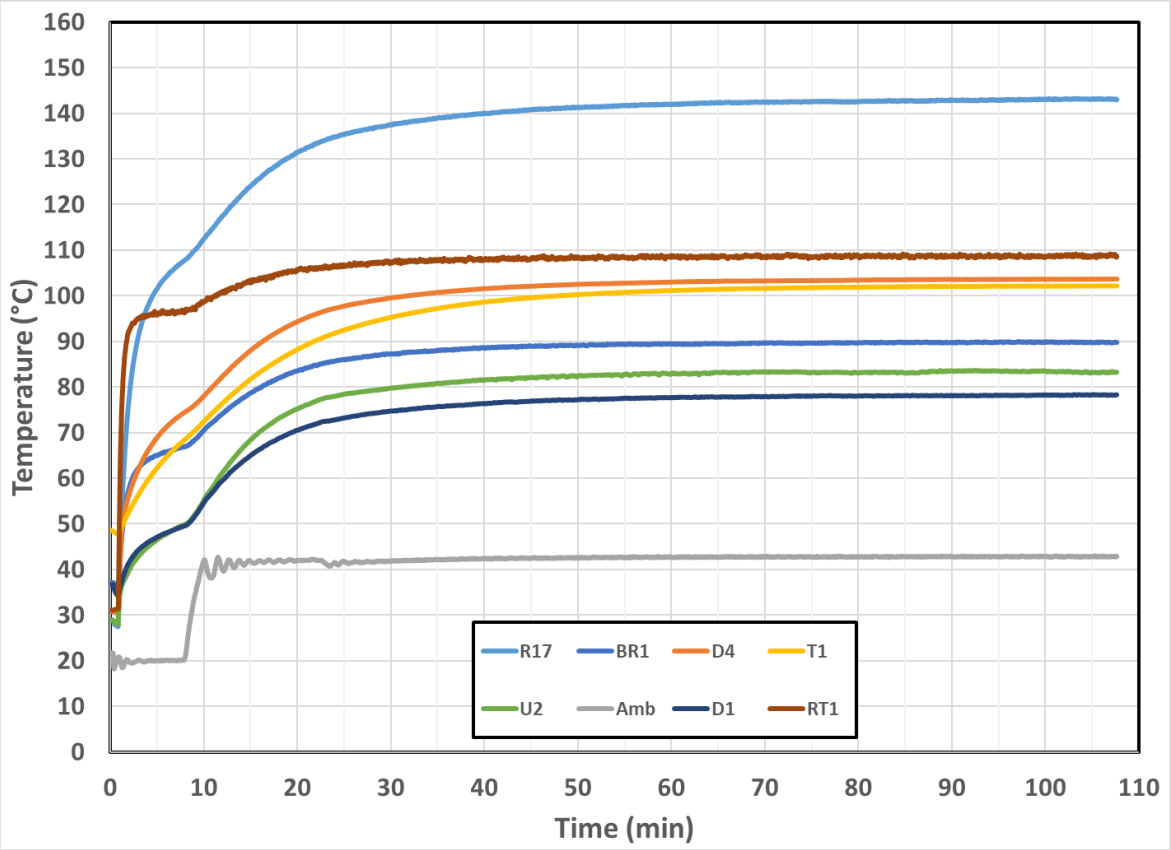


Figure 22 – Thermal Profile at 230 VAC, Full Load.

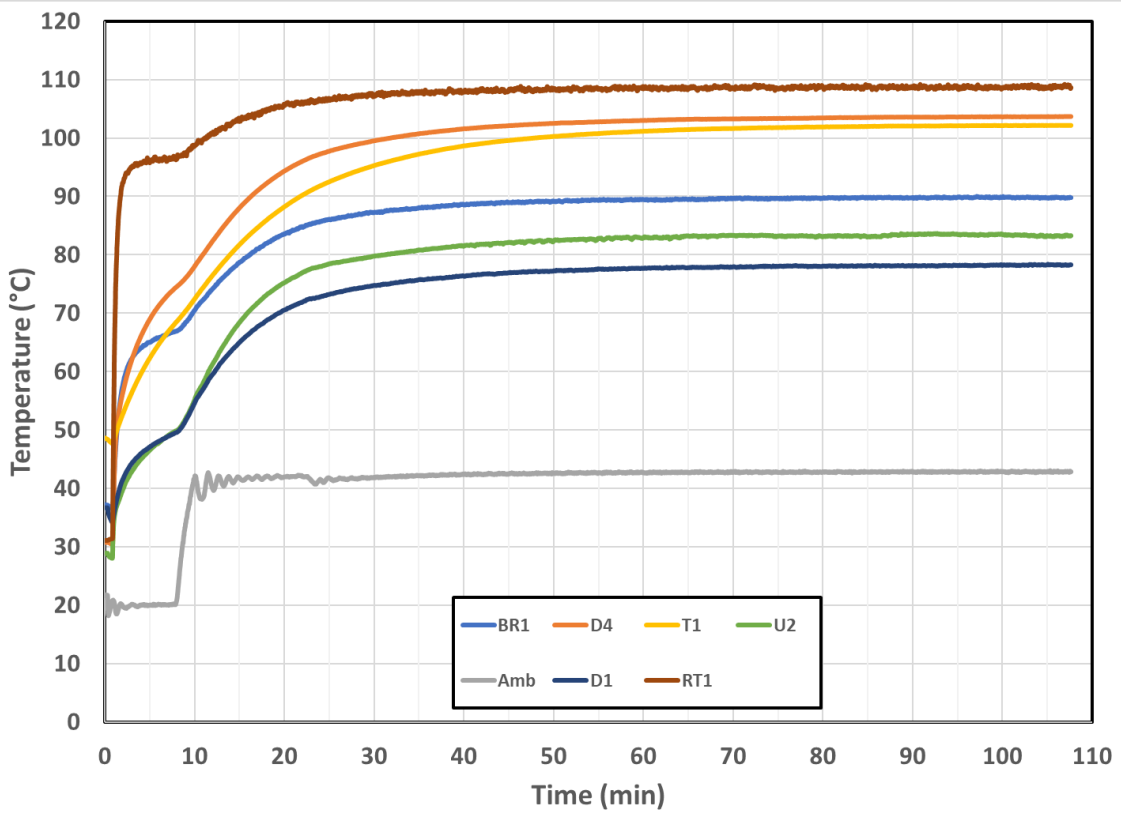


Figure 23 – Thermal Profile at 265 VAC, Full Load.

12 Waveforms

12.1 Output Voltage Profile at Full-Load Start-Up

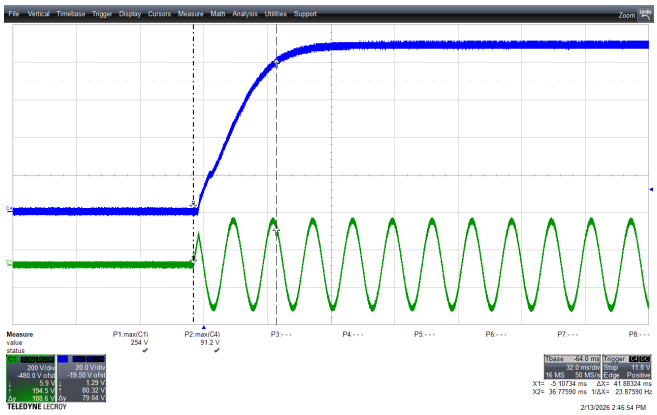


Figure 24 – 165 VAC, 50 Hz. Full-Load Start-Up.
CH1: I_{OUT}, 200 V / div., 32 ms / div.
CH4: V_{OUT}, 20 V / div., 32 ms / div.
$t_{ON\ Delay}$ = 42 ms
$V_{OUT\ Max}$ = 91.2 V

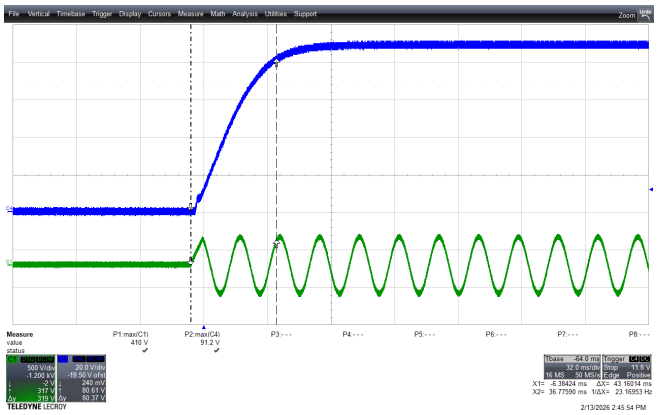


Figure 25 – 265 VAC, 50 Hz, Full-Load Start-Up.
CH1: I_{OUT}, 200 V / div., 32 ms / div.
CH4: V_{OUT}, 20 V / div., 32 ms / div.
$t_{ON\ Delay}$ = 43 ms
$V_{OUT\ Max}$ = 91.2 V

12.2 Output Voltage During Step Line Transient

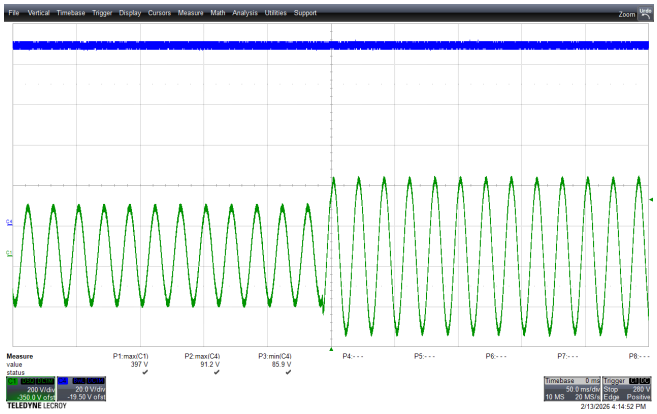


Figure 26 – 165 VAC – 265 V, Step Line Transient.
CH1: I_{OUT}, 200 V / div., 50 ms / div.
CH4: V_{OUT}, 20 V / div., 50 ms / div.
$V_{OUT\ Max}$ = 91.2 V
$V_{OUT\ Min}$ = 85.9 V

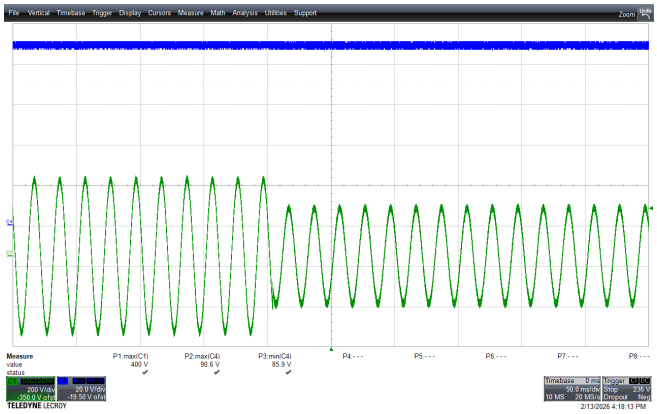


Figure 27 – 265 VAC – 165 V, Step Line Transient.
CH1: I_{OUT}, 200 V / div., 50 ms / div.
CH4: V_{OUT}, 20 V / div., 50 ms / div.
$V_{OUT\ Max}$ = 90.6 V
$V_{OUT\ Min}$ = 85.9 V

12.3 Output Voltage Profile During 1 s On/Off AC Cycling

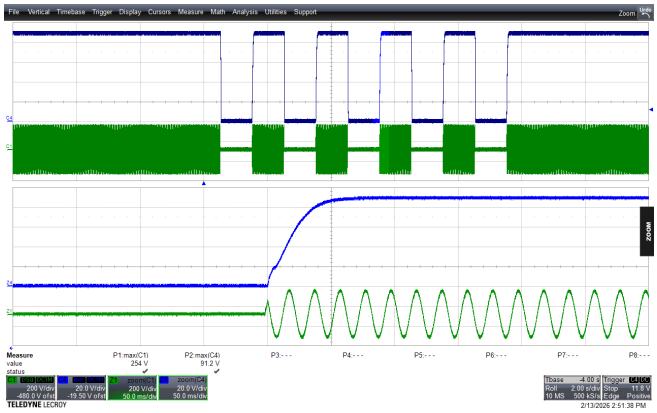


Figure 28 – 165 VAC 50 Hz, 1s On/Off Cycling.
CH1: I_{OUT}, 200 V / div., 2 s / div.
CH4: V_{OUT}, 20 V / div., 2 s / div.
Zoom-in: 50 ms / div.
$V_{OUT\ Max}$ = 91.2 V
$V_{IN\ Max}$ = 254 V

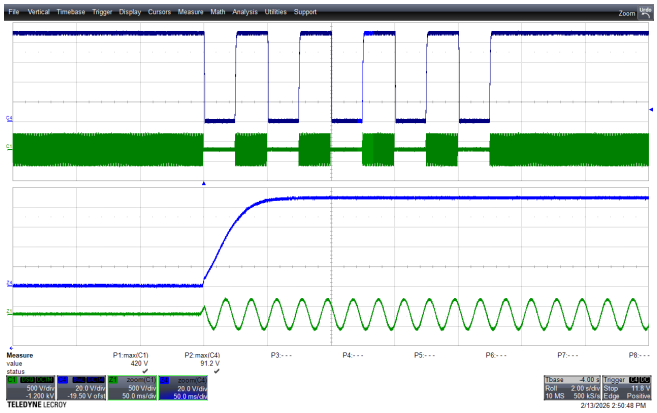


Figure 29 – 265 VAC Hz, 1s On/Off Cycling.
CH1: I_{OUT}, 200 V / div., 2 s / div.
CH4: V_{OUT}, 20 V / div., 2 s / div.
Zoom-in: 50 ms / div.
$V_{OUT\ Max}$ = 91.2 V
$V_{IN\ Max}$ = 420 V

12.4 Output Voltage Profile During 500 ms On/Off AC Cycling

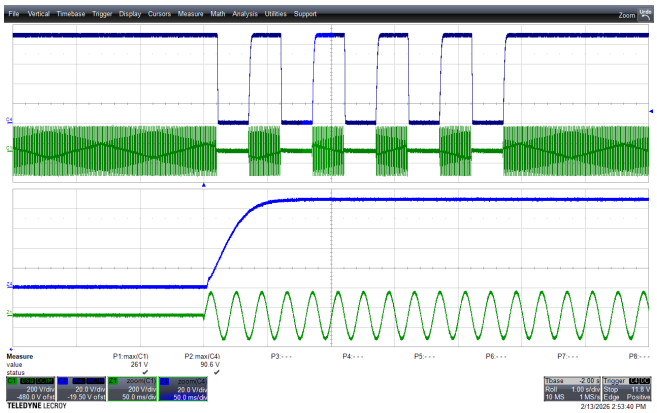


Figure 30 – 165 VAC 50 Hz, 500 ms On/Off Cycling.
CH1: I_{OUT}, 200 V / div., 1 s / div.
CH4: V_{OUT}, 20 V / div., 1 s / div.
Zoom-in: 50 ms / div.
$V_{OUT\ Max}$ = 90.6 V
$V_{IN\ Max}$ = 261 V

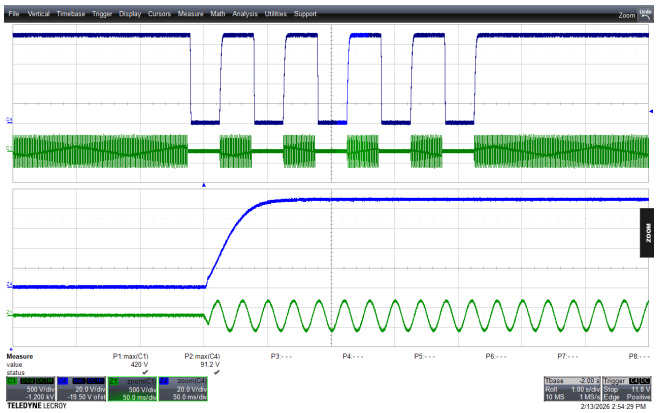


Figure 31 – 265 VAC 50 Hz, 500 ms On/Off Cycling.
CH1: I_{OUT}, 200 V / div., 1 s / div.
CH4: V_{OUT}, 20 V / div., 1 s / div.
Zoom-in: 50 ms / div.
$V_{OUT\ Max}$ = 91.2 V
$V_{IN\ Max}$ = 420 V

12.5 Primary Drain Voltage and Current

12.5.1 Steady State Operation

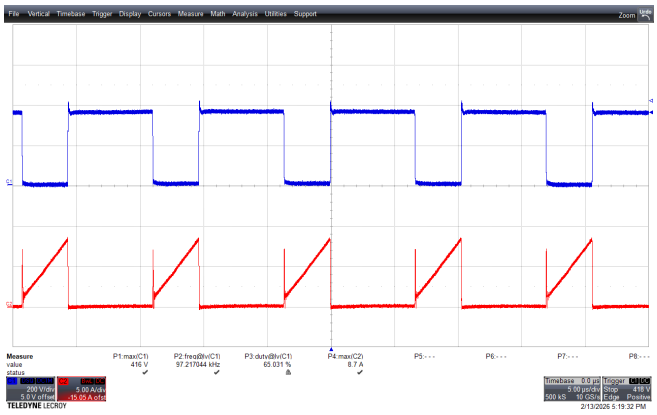


Figure 32 – 165 VAC, 50 Hz, Full Load Normal.
CH1: V_{DS}, 200 V / div., 5 us / div.
CH2: I_{DS}, 5 A / div., 5 us / div.
$V_{DS\ Max}$ = 416 V
$I_{DS\ Max}$ = 8.7 A

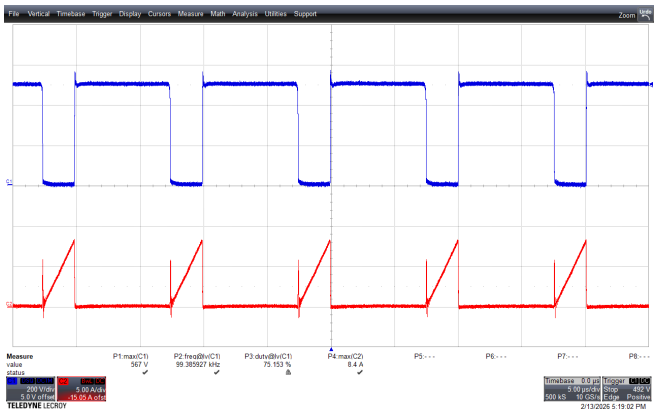


Figure 33 – 265 VAC, 50 Hz Full Load Normal.
CH1: V_{DS}, 200 V / div., 5 us / div.
CH2: I_{DS}, 5 A / div., 5 us / div.
$V_{DS\ Max}$ = 567 V
$I_{DS\ Max}$ = 8.4 A

12.5.2 Start-up Operation

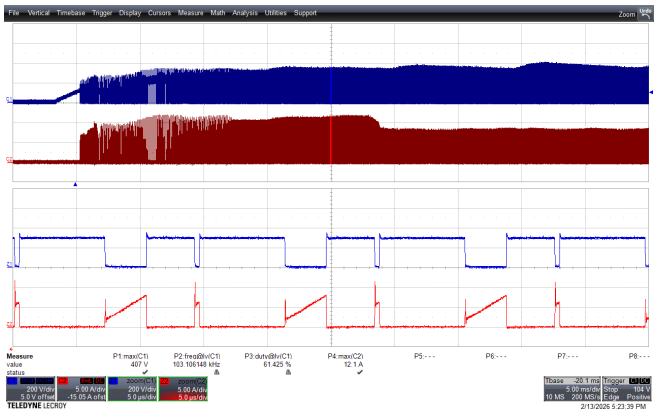


Figure 34 – 165 VAC, 50 Hz Full Load, Start-up.
CH1: V_{DS}, 200 V / div., 5 ms / div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom in: 5 us / div.
$V_{DS\ Max}$ = 407 V
$I_{DS\ Max}$ = 12.1 A

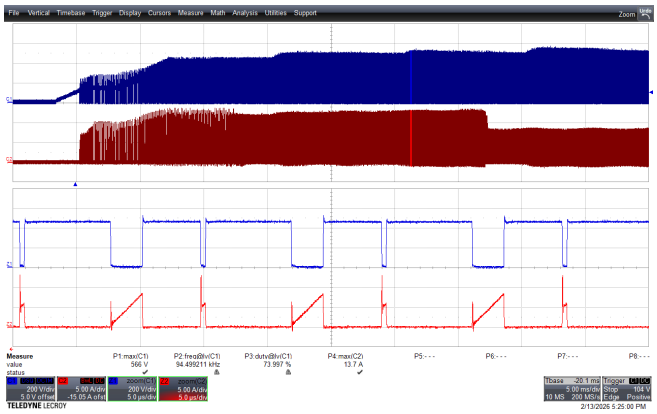


Figure 35 – 265 VAC, 50 Hz Full Load, Start-up.
CH1: V_{DS}, 200 V / div., 5 ms / div.
CH2: I_{DS}, 5 A / div., 5 ms / div.
Zoom in: 5 us / div.
$V_{DS\ Max}$ = 566 V
$I_{DS\ Max}$ = 13.7 A

12.5.3 Step-Load Transient

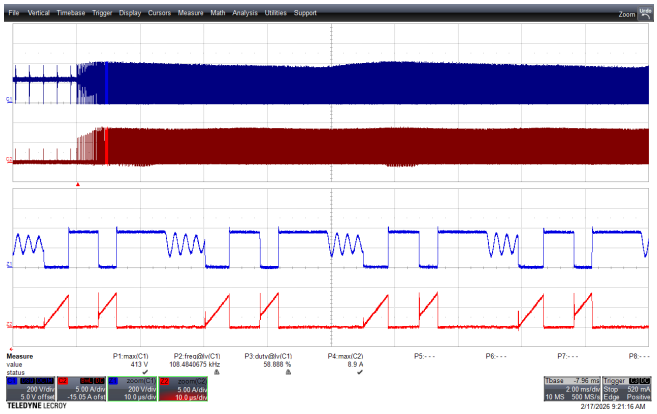


Figure 36 – 165 VAC, 50 Hz 0 -100% Step Load.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
Zoom in: 10 us / div.
$V_{DS\ Max}$ = 413 V
$I_{DS\ Max}$ = 8.9 A

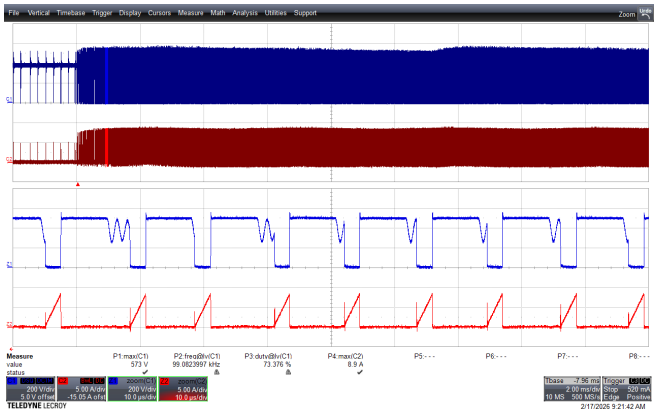


Figure 37 – 265 VAC, 50 Hz 0 -100% Step Load.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
Zoom in: 10 us / div.
$V_{DS\ Max}$ = 573 V
$I_{DS\ Max}$ = 8.9 A

12.5.4 Input Line Transient

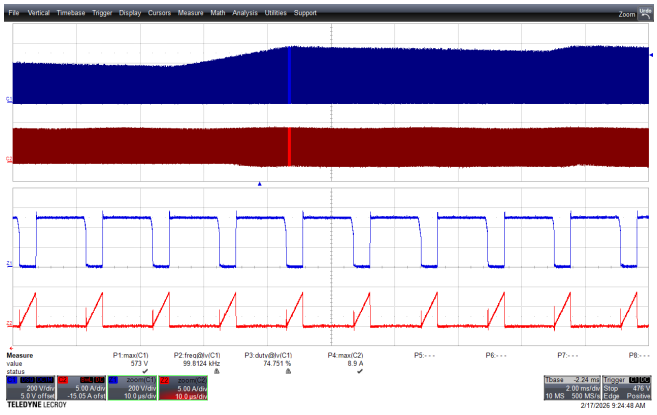


Figure 38 – 165 VAC – 265 VAC Step Line Transient.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
Zoom in: 10 us / div.
$V_{DS\ Max}$ = 573 V
$I_{DS\ Max}$ = 8.9 A

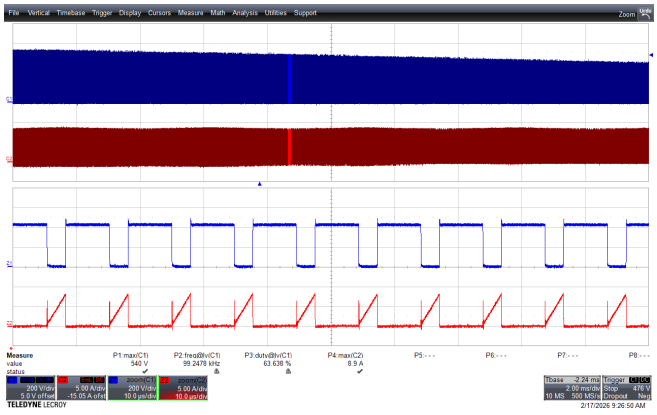


Figure 39 – 265 VAC – 165 VAC Step Line Transient.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
Zoom in: 10 us / div.
$V_{DS\ Max}$ = 540 V
$I_{DS\ Max}$ = 8.9 A

12.6 .Power Supply Protection Features Test

12.6.1 Start-Up Under Short-Circuit Condition

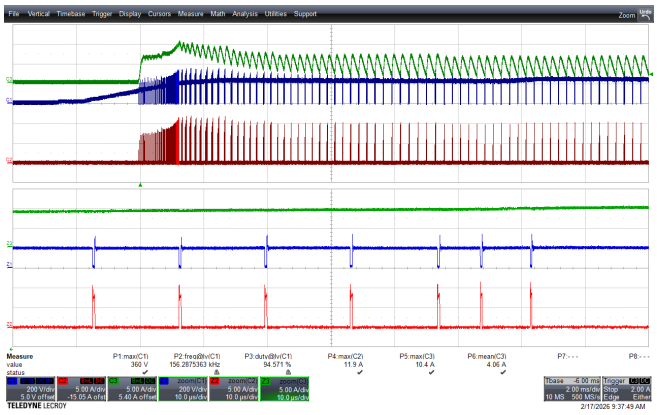


Figure 40 – 165 VAC, 50 Hz. Start-up Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
$V_{DS\ Max}$ = 360 V I_O = 4.06 A
$I_{DS\ Max}$ = 11.9 A I_{OMAX} = 10.4 A

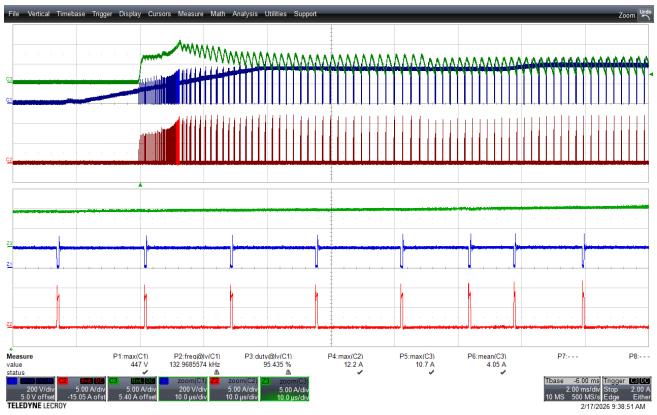


Figure 41 – 265 VAC, 50 Hz. Start-up Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
$V_{DS\ Max}$ = 447 V I_O = 4.05 A
$I_{DS\ Max}$ = 12.2 A I_{OMAX} = 10.7 A

12.6.2 Output Short-Circuit Steady State Condition

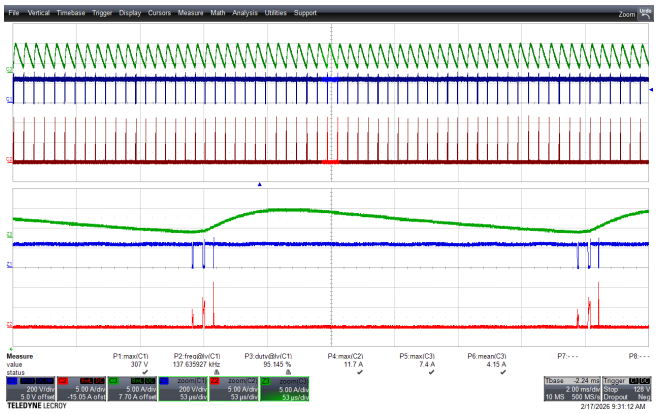


Figure 42 – 165 VAC, 50 Hz. Short – Steady State.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
$V_{DS\ Max}$ = 307 V
$I_{DS\ Max}$ = 11.7 A

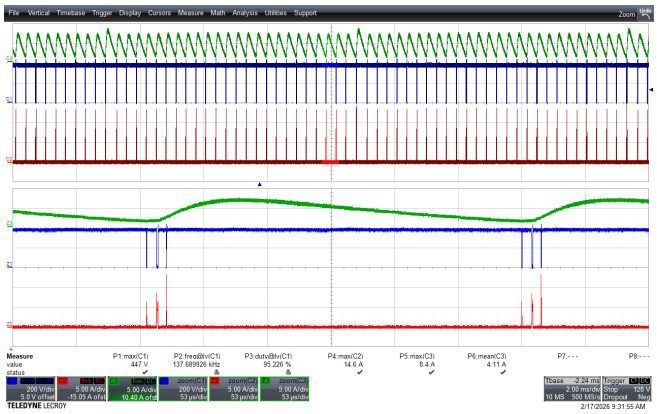


Figure 43 – 265 VAC, 50 Hz. Short – Steady State.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
$V_{DS\ Max}$ = 447 V
$I_{DS\ Max}$ = 12.2 A

12.6.3 Full-Load Running Output Short-Circuit Test

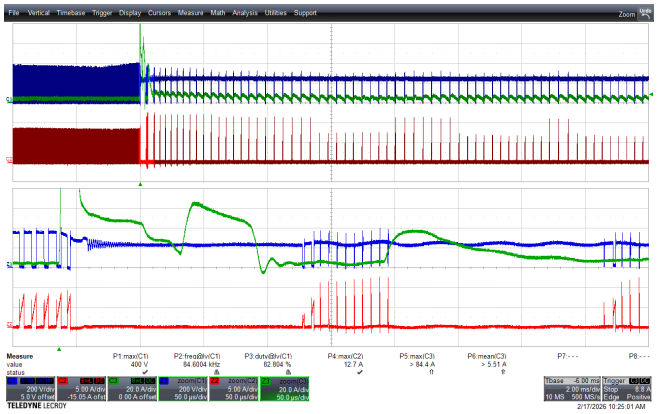


Figure 44 – 165 VAC, 50 Hz. Full Load – Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 20 A / div., 2 ms / div.
$V_{DS\ Max}$ = 400 V
$I_{DS\ Max}$ = 12.7 A

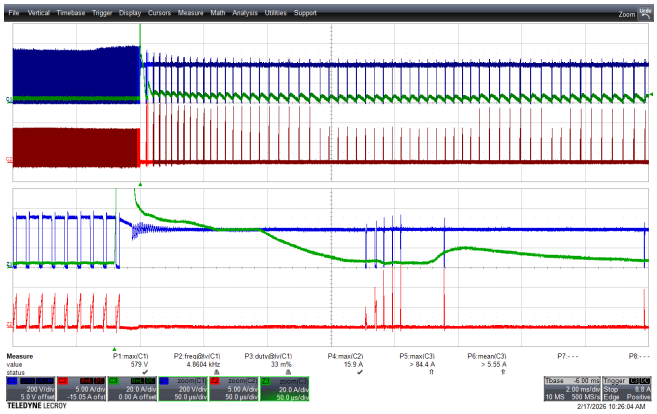


Figure 45 – 265 VAC, 50 Hz. Full Load – Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 s / div.
CH2: I_{OUT}, 20 A / div., 2 ms / div.
$V_{DS\ Max}$ = 579 V
$I_{DS\ Max}$ = 15.9 A

12.6.4 No-Load Running Output Short-Circuit Test

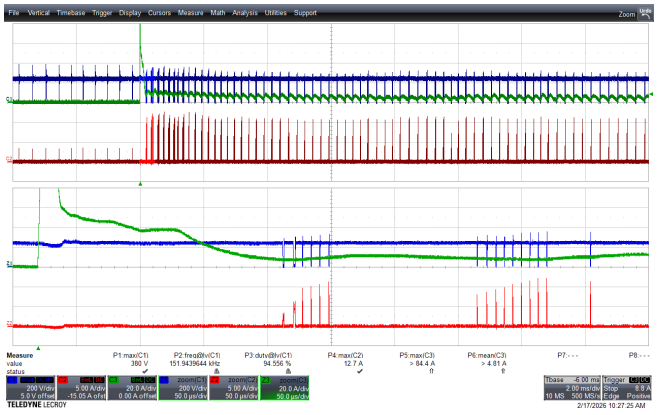


Figure 46 – 165 VAC, 50 Hz. No Load – Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 ms / div.
CH2: I_{OUT}, 20 A / div., 2 ms / div.
$V_{DS\ Max}$ = 380 V
$I_{DS\ Max}$ = 12.7 A

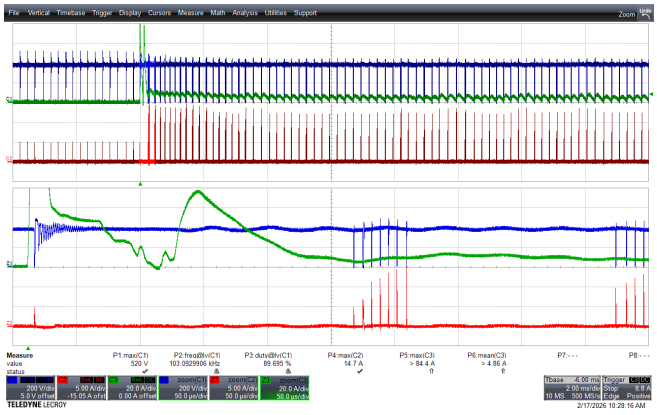


Figure 47 – 265 VAC, 50 Hz. No Load – Short.
CH1: V_{DS}, 200 V / div., 2 ms / div.
CH2: I_{DS}, 5 A / div., 2 s / div.
CH2: I_{OUT}, 20 A / div., 2 ms / div.
$V_{DS\ Max}$ = 520 V
$I_{DS\ Max}$ = 14.7 A

12.6.5 Input Line Overvoltage and Overvoltage Recovery Test

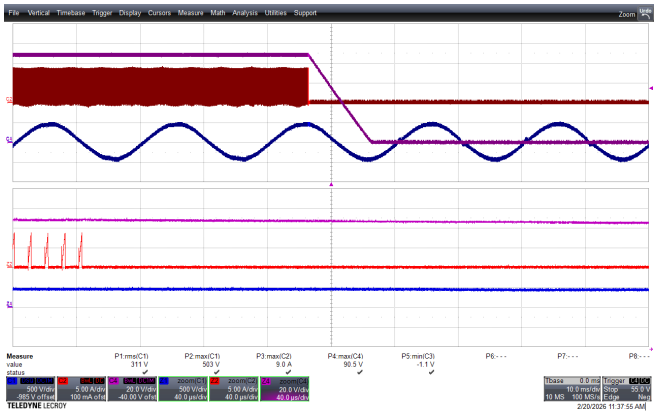


Figure 48 – Line Overvoltage at Full Load.
CH1: V_{IN}, 500 V / div., 10 ms / div.
CH2: I_{DS}, 5 A / div., 10 ms / div.
CH4: V_{OUT}, 20 V / div., 10 ms / div.
Zoom In: 40 µs / div.
$V_{IN-OVP\ RMS}$ = 311 V
$V_{OUT\ Max}$ = 90.5 V

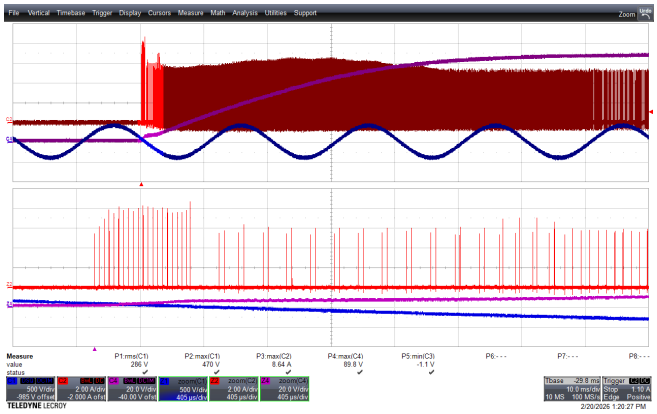


Figure 49 – Line Overvoltage Recovery at Full Load.
CH1: V_{IN}, 500 V / div., 10 ms / div.
CH2: I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 20 V / div., 10 ms / div.
Zoom In: 405 µs / div.
$V_{IN-OVP\ REC.\ RMS}$ = 286 V
$V_{OUT\ Max}$ = 89.9 V

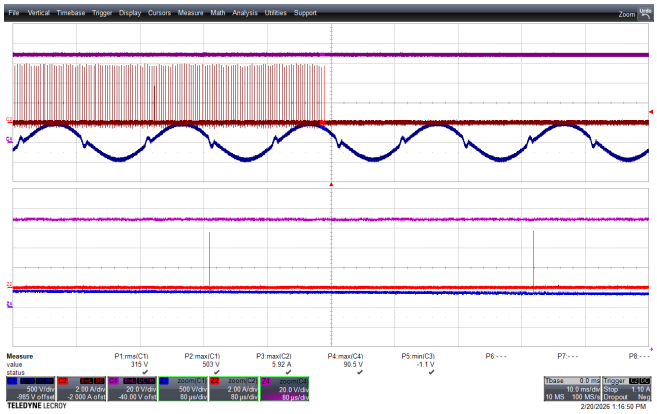


Figure 50 – Line Overvoltage at No Load.
CH1: V_{IN}, 500 V / div., 10 ms / div.
CH2: I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 20 V / div., 10 ms / div.
Zoom In: 80 µs / div.
$V_{IN-OVP\ RMS}$ = 311 V
$V_{OUT\ Max}$ = 90.5 V

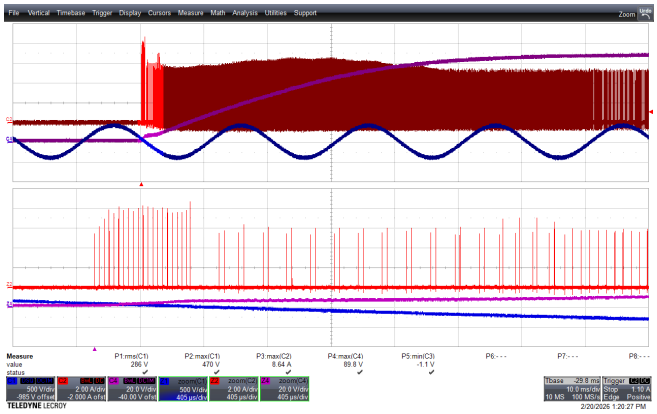


Figure 51 – Line Overvoltage Recovery at No Load.
CH1: V_{IN}, 500 V / div., 10 ms / div.
CH2: I_{DS}, 2 A / div., 10 ms / div.
CH4: V_{OUT}, 20 V / div., 10 ms / div.
Zoom In: 405 µs / div.
$V_{IN-OVP\ REC.\ RMS}$ = 286 V
$V_{OUT\ Max}$ = 89.9 V

12.6.6 Output Overvoltage Test

This test verified the operation of the output overvoltage protection circuit together with the TOPSwitchGaN IC BYPASS-pin fault shutdown threshold current (I_{SD}). The test was performed by intentionally connecting a 10 kΩ resistor across the output-voltage-regulator feedback resistor R30, thereby increasing the output voltage by approximately 25%.

Figure 52 – 165 VAC, No Load. Output Overvoltage.
CH2: I_{DS}, 2 A / div., 200 ms / div.
CH4: V_{OUT}, 20 V / div., 200 ms / div.
Zoom In: 1.48 ms / div.
$I_{DS\ max}$ = 13.0 A
$V_{OUT\ Max}$ = 105.7 V

Figure 53 – 265 VAC, No Load. Output Overvoltage.
CH2: I_{DS}, 2 A / div., 200 ms / div.
CH4: V_{OUT}, 20 V / div., 200 ms / div.
Zoom In: 1.48 ms / div.
$I_{DS\ max}$ = 10.1 A
$V_{OUT\ Max}$ = 105.7 V

12.7 Flyback Output Diode Voltage Stress

12.7.1 Output Diode Voltage Stress at Steady State

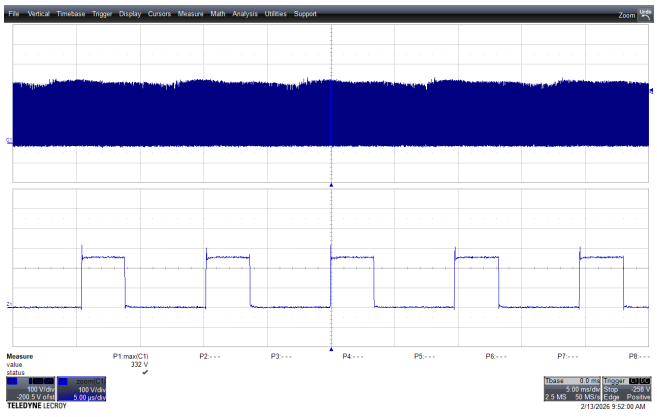


Figure 54 – 165 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 332 V
Voltage Stress: 55.3%

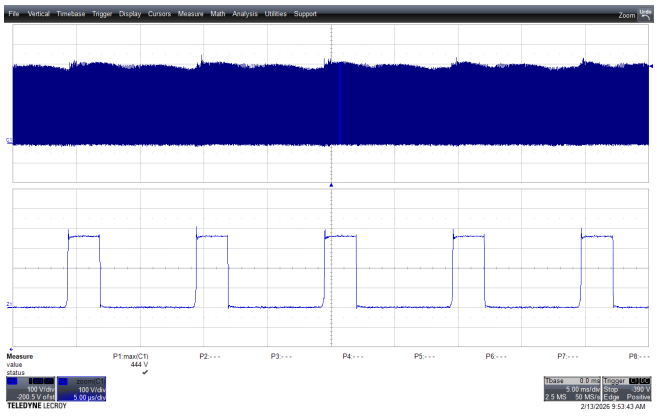


Figure 55 – 265 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 444 V
Voltage Stress: 74%

12.7.2 Output Diode Voltage Stress During Start-up Full Load

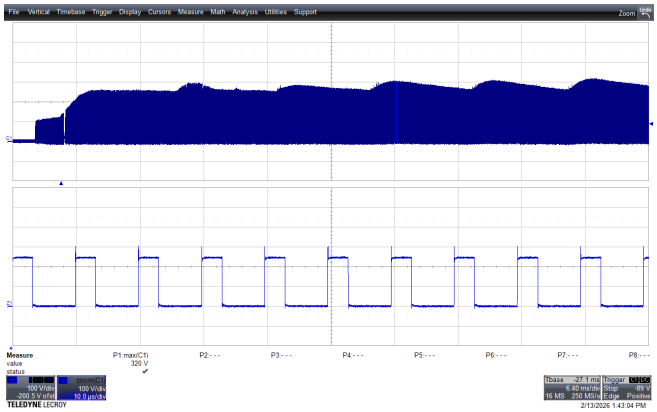


Figure 56 – 165 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 320 V
Voltage Stress: 53.3%

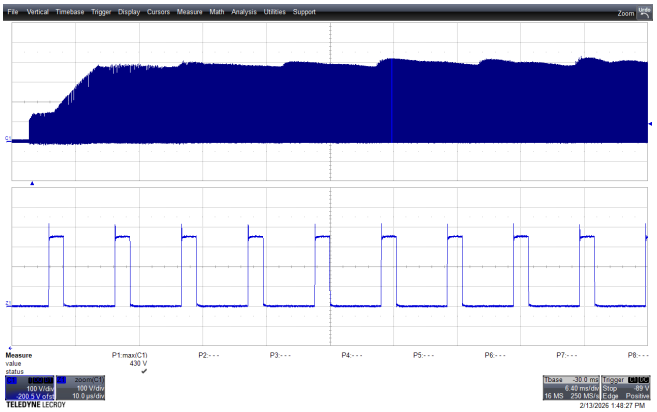


Figure 57 – 265 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 430 V
Voltage Stress: 71.7%

12.7.3 Output Diode Voltage Stress During No Load to Full Load Transient

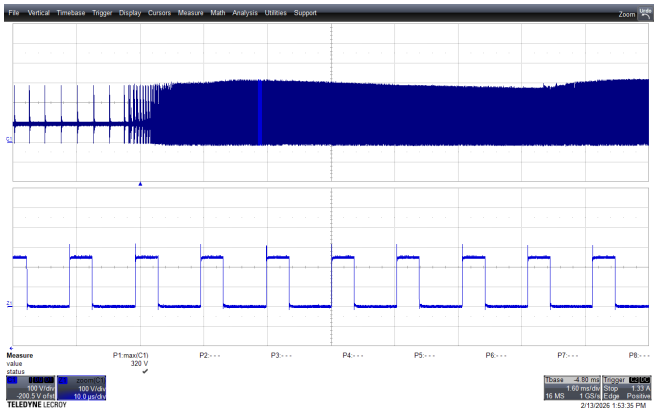


Figure 58 – 165 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 320 V
Voltage Stress: 53.3%

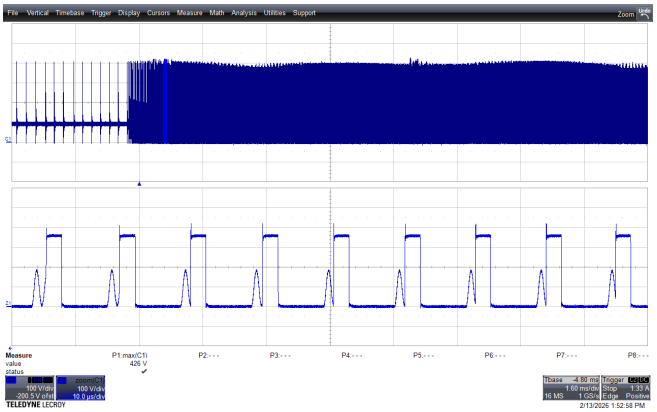


Figure 59 – 265 VAC, 50 Hz. Full Load Normal.
CH1: V_{DIODE}, 100 V / div., 5 ms / div.
$V_{DIODE\ Max}$ = 426 V
Voltage Stress: 71%

12.8 Output Ripple Voltage Waveforms

12.8.1 Ripple Voltage Measurement Set-up

Output ripple voltage was measured using a voltage probe with 47 µF electrolytic capacitor and a 100 nF ceramic capacitor connected across the probe tip to reduce periodic and random noise.

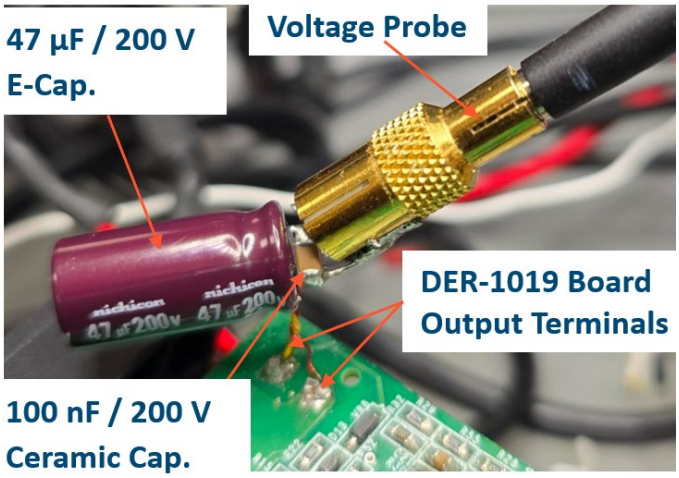


Figure 60 – Ripple Voltage Measurement Set-up Picture.

12.8.2 Output Ripple Voltage Waveforms

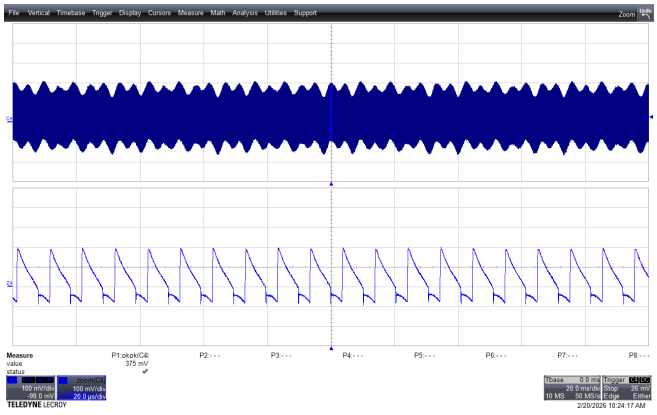


Figure 61 – 165 VAC, 60 Hz. 4 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 375 mV pk-pk

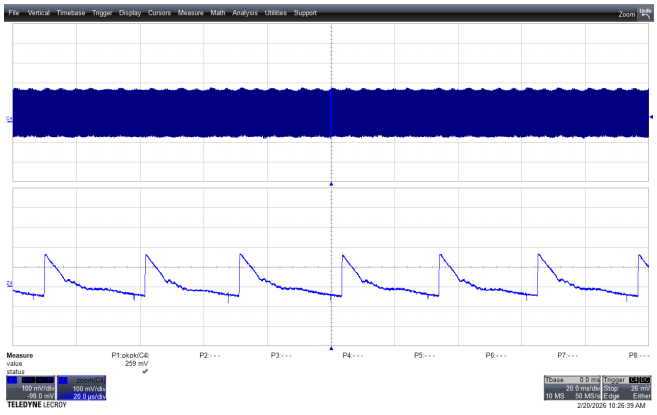


Figure 62 – 165 VAC, 60 Hz. 1 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 259 mV pk-pk

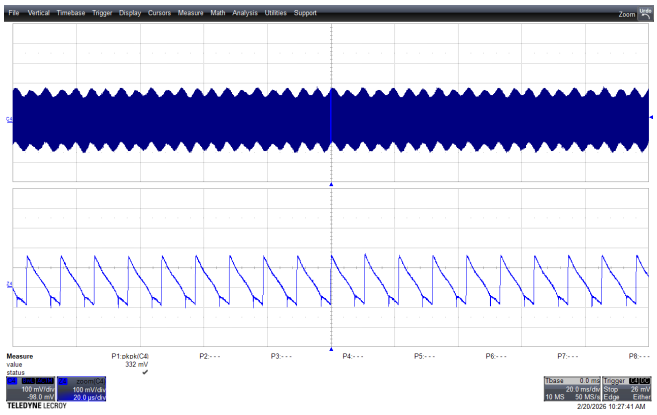


Figure 63 – 230 VAC, 60 Hz. 4 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 332 mV pk-pk

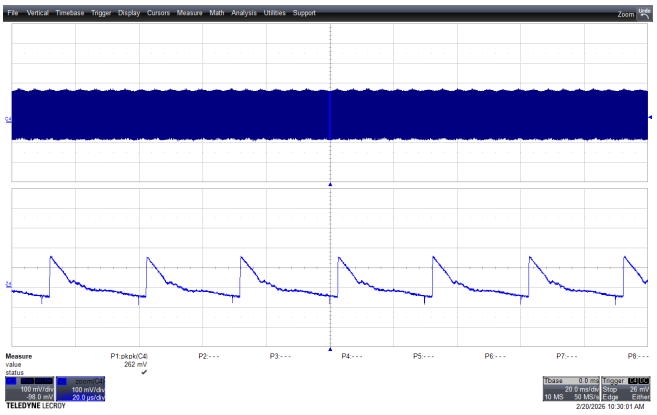


Figure 64 – 230 VAC, 60 Hz. 1 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 262 mV pk-pk

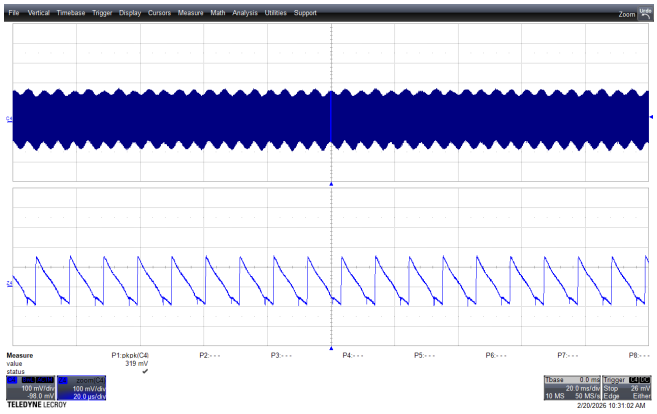


Figure 65 – 265 VAC, 60 Hz. 4 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 319 mV pk-pk

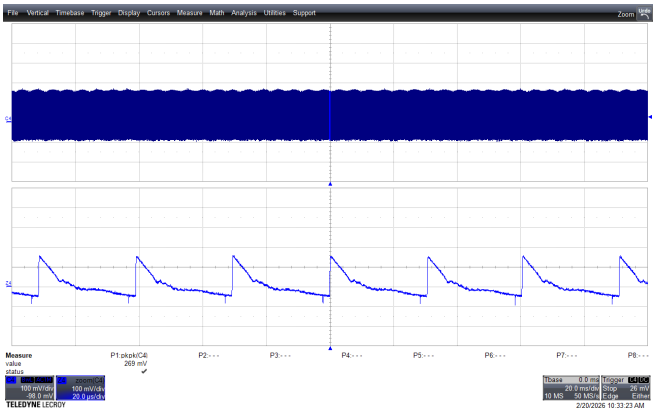


Figure 66 – 265 VAC, 60 Hz. 1 A Load.
CH1: V_{RIPPLE}, 100 mV / div., 20 ms / div.
Zoom In: 20 µs / div.
V_{RIPPLE} = 269 mV pk-pk

12.9 Transient Load Response

Transient load response was measured using an electronic load in dynamic constant-current mode at various frequencies. This test showed the PSU's performance by monitoring output overshoot and undershoot during load steps. The duty cycle was set to 50% and the load-step slew rate was 800 mA/µs. The output-voltage waveform was measured directly on the board.

12.9.1 1 kHz, Dynamic Load Response

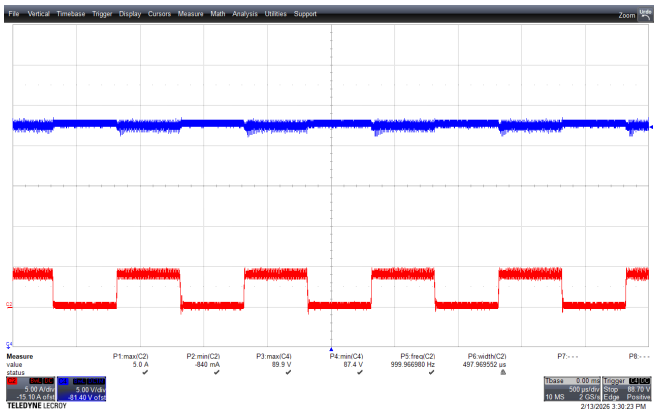


Figure 67 – 230 VAC, 0 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 500 µs / div.
CH1: V_{OUT}, 5 V / div., 500 µs / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.2 V

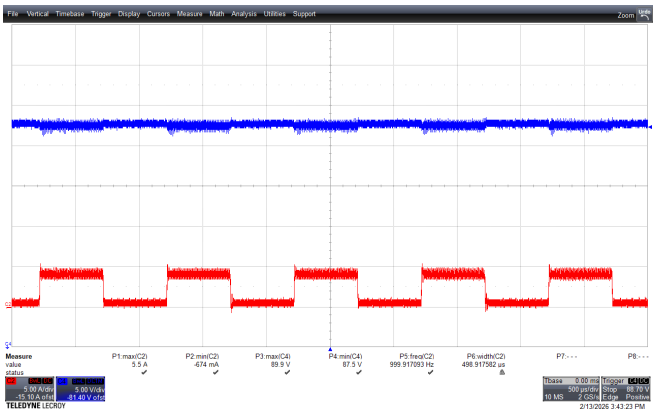


Figure 68 – 230 VACS, 0.4 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 500 µs / div.
CH1: V_{OUT}, 5 V / div., 500 µs / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.4 V

12.9.2 500 Hz, Dynamic Load Response

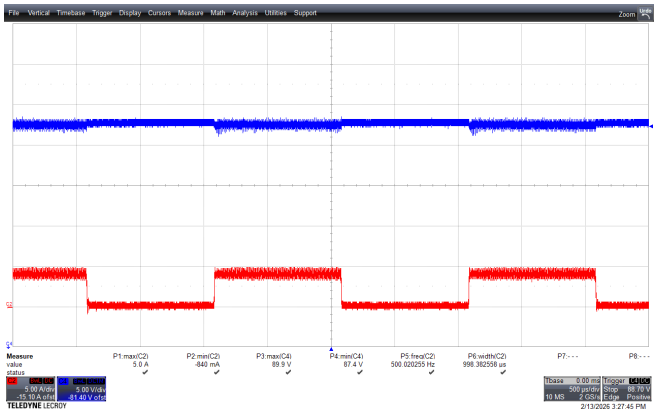


Figure 69 – 230 VAC, 0 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 500 µs / div.
CH1: V_{OUT}, 5 V / div., 500 µs / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.4 V

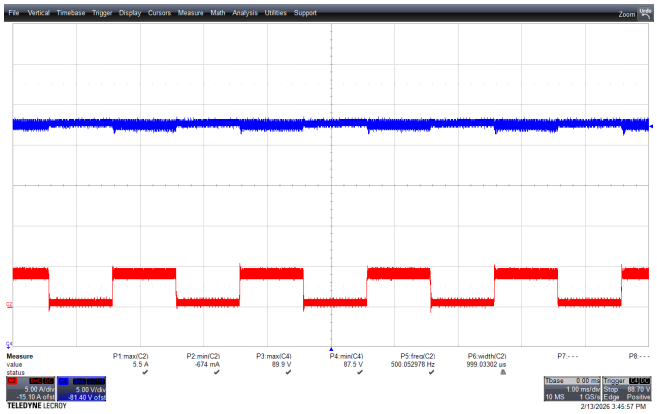


Figure 70 – 230 VACS, 0.4 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 500 µs / div.
CH1: V_{OUT}, 5 V / div., 500 µs / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.5 V

12.9.3 200 Hz, Dynamic Load Response

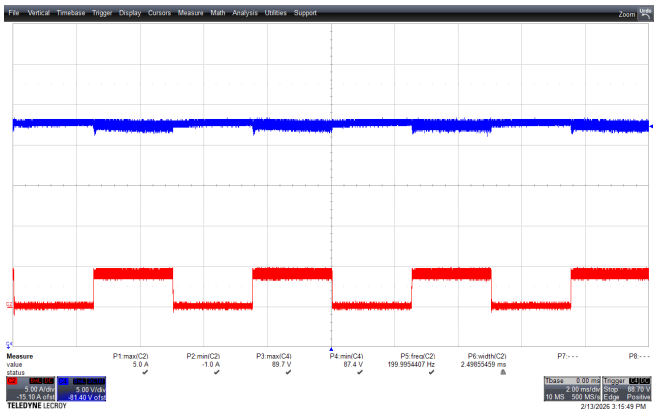


Figure 71 – 230 VAC, 0 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
CH1: V_{OUT}, 5 V / div., 2 ms / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.4 V

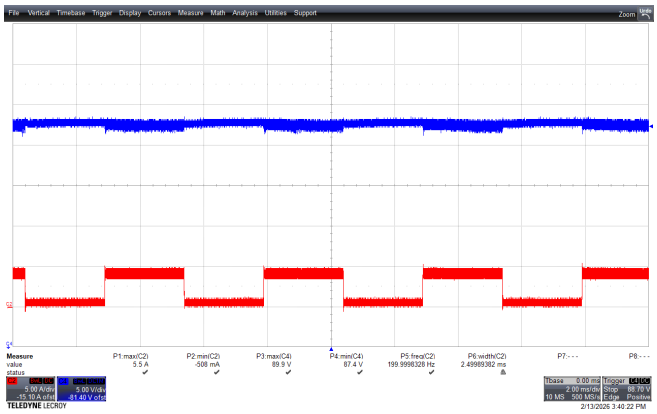


Figure 72 – 230 VACS, 0.4 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 2 ms / div.
CH1: V_{OUT}, 5 V / div., 2 ms / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.4 V

12.9.4 10 Hz, Dynamic Load Response

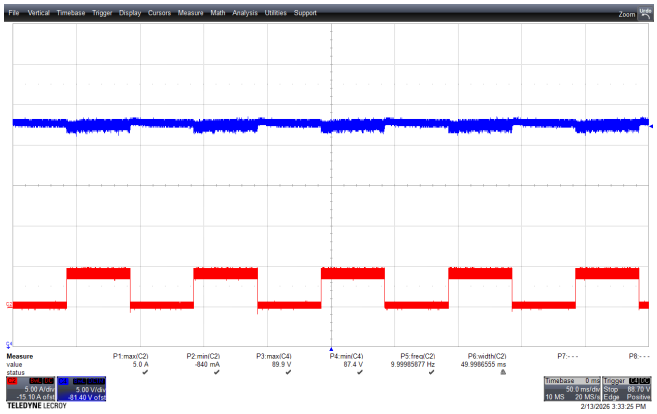


Figure 73 – 230 VAC, 0 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 50 ms / div.
CH1: V_{OUT}, 5 V / div., 50 ms / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.4 V

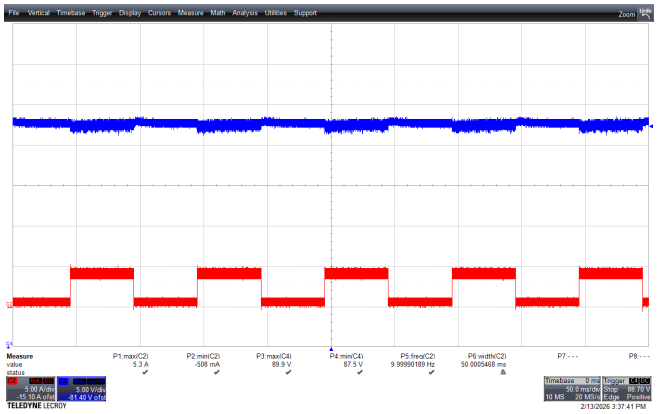


Figure 74 – 230 VACS, 0.4 – 4 A Dynamic Load.
CH2: I_{OUT}, 5 A / div., 50 ms / div.
CH1: V_{OUT}, 5 V / div., 50 ms / div.
$V_{OUT\ Max}$ = 89.9 V
$V_{OUT\ Min}$ = 87.5 V

12.10 Brown-in / Brown-out Test at 36 V LED

12.10.1 Brown-in / Brown-out Test at 36 V LED

No overheating or component damage was observed during brown-in and brown-out testing.

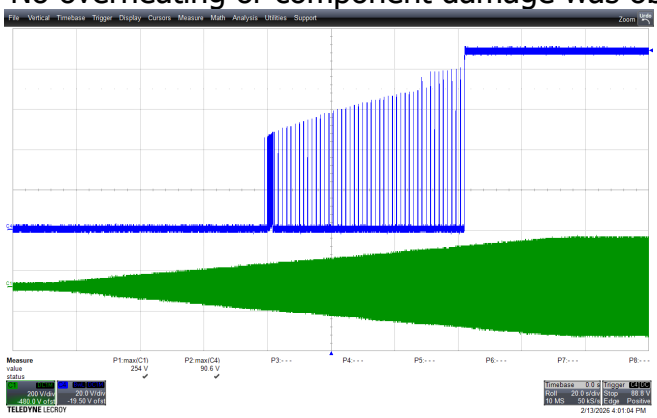


Figure 75 – Brown in, 0 - 165 V, 1 V / s, Full Load.
CH1: V_{IN}, 200 V / div., 20 s / div.
CH4: V_{OUT}, 20 V / div., 20 s / div.

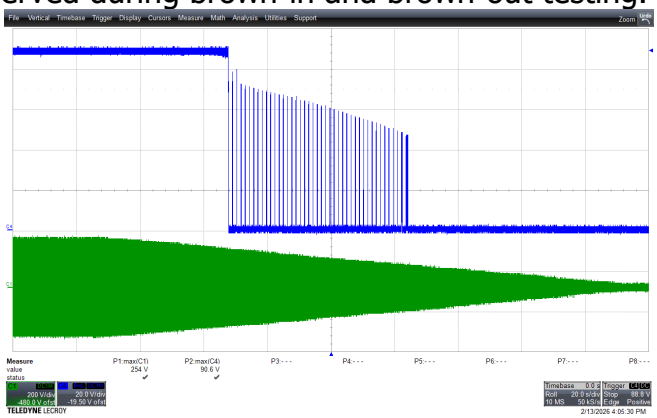


Figure 76 – Brown out, 165 - 0 V, 1 V / s, Full Load.
CH1: V_{IN}, 200 V / div., 20 s / div.
CH4: V_{OUT}, 20 V / div., 20 s / div.

13 Conducted EMI

EMI scans were performed at 230 VAC using a 22.2 Ω fix resistor load.

13.1 Test Set-up

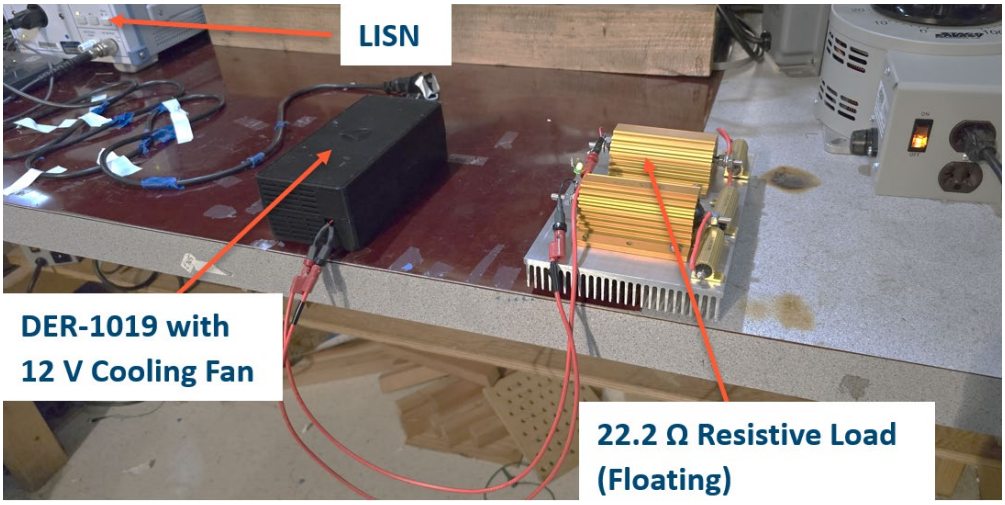


Figure 77 – Conducted EMI Test Set-up.

13.2 Conducted EMI Scan

The unit passed EN 55022 Class B with > 6 dB margin on the neutral line and > 5 dB margin on the live line.

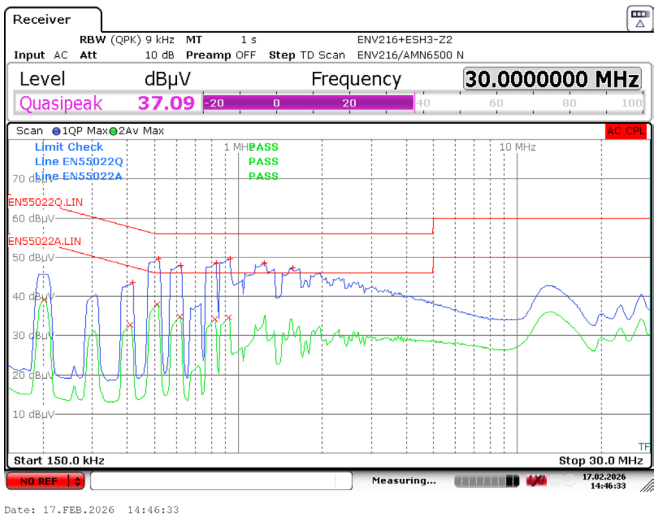


Figure 78 – Neutral Line Conducted EMI Scan.

Trace1: EN55022Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	201.7500 kHz	39.25 N	-14.29 dB
2 Average	411.0000 kHz	32.80 N	-14.83 dB
1 Quasi Peak	417.7500 kHz	43.43 N	-14.06 dB
2 Average	512.2500 kHz	37.98 N	-8.02 dB
1 Quasi Peak	519.0000 kHz	49.52 N	-6.48 dB
2 Average	615.7500 kHz	34.76 N	-11.24 dB
1 Quasi Peak	622.5000 kHz	47.96 N	-8.04 dB
2 Average	822.7500 kHz	34.10 N	-11.90 dB
1 Quasi Peak	834.0000 kHz	48.48 N	-7.52 dB
2 Average	926.2500 kHz	34.69 N	-11.31 dB
1 Quasi Peak	933.0000 kHz	49.61 N	-6.39 dB
1 Quasi Peak	1.2435 MHz	48.54 N	-7.46 dB
1 Quasi Peak	1.5675 MHz	47.18 N	-8.82 dB

Figure 79 – Neutral Line 1 Conducted EMI Test Data.

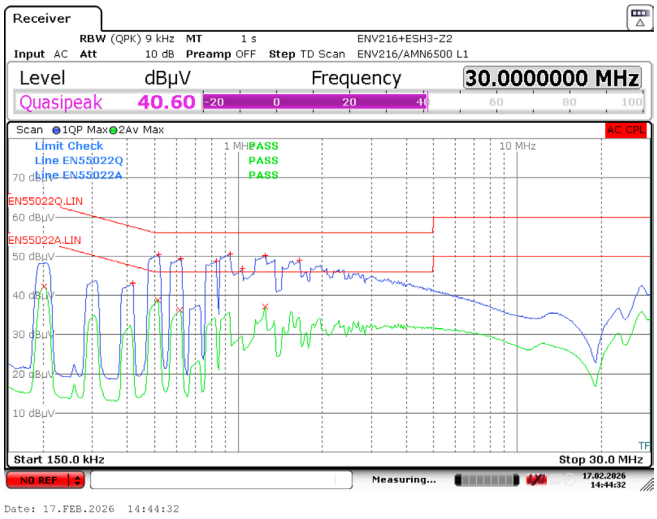


Figure 80 – Line 1 Conducted EMI Scan.

Trace1: EN55022Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	201.7500 kHz	42.24 L1	-11.30 dB
1 Quasi Peak	417.7500 kHz	43.08 L1	-14.41 dB
2 Average	514.5000 kHz	38.75 L1	-7.25 dB
1 Quasi Peak	519.0000 kHz	50.31 L1	-5.69 dB
2 Average	615.7500 kHz	36.21 L1	-9.79 dB
1 Quasi Peak	622.5000 kHz	49.30 L1	-6.70 dB
1 Quasi Peak	834.0000 kHz	48.70 L1	-7.30 dB
1 Quasi Peak	933.0000 kHz	50.50 L1	-5.50 dB
1 Quasi Peak	1.0365 MHz	46.87 L1	-9.13 dB
1 Quasi Peak	1.2458 MHz	50.15 L1	-5.85 dB
2 Average	1.2458 MHz	37.07 L1	-8.93 dB
1 Quasi Peak	1.6598 MHz	48.81 L1	-7.19 dB

Figure 81 – Line 1 Peak Conducted EMI Test Data.

14 Line Surge Immunity

The unit was powered up at a 230 V input and subjected to ±4000 V ring-wave, combination-wave, and EFT surge tests, with 10 strikes applied for each condition.

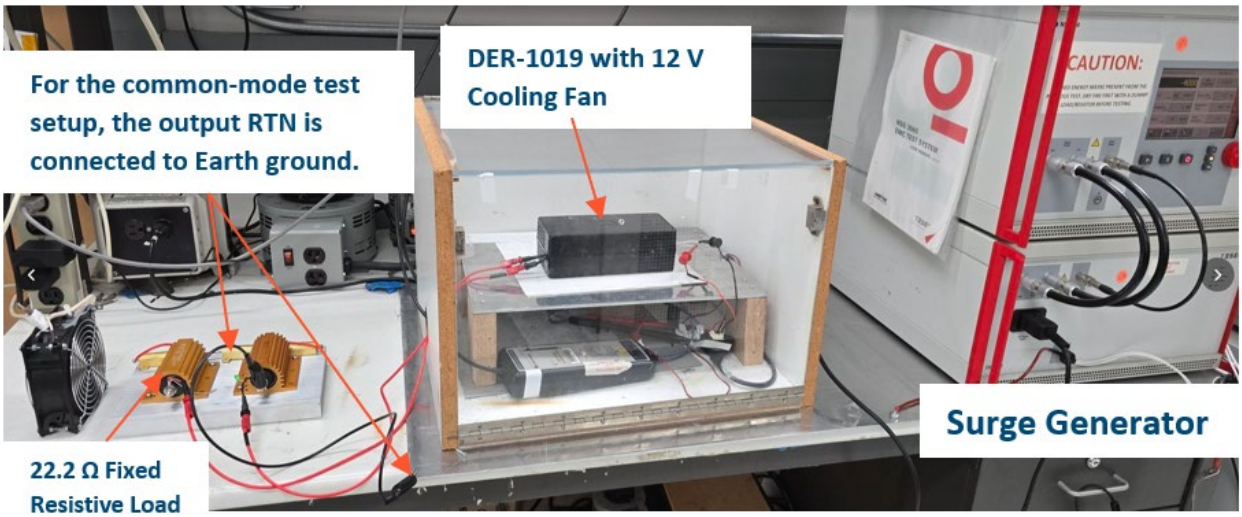


Figure 82 – Surge Immunity Test Set-up.

14.1 Combination Wave Differential Mode Surge

The unit passed the 4 kV differential surge test with no auto restart (AR), no output interruption, and no damaged components observed.

AC Input Voltage (VAC)	Surge Voltage (kV)	Coupling	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4000	L to N	0	2	10	PASS – No AR
230	-4000	L to N	0	2	10	PASS – No AR
230	+4000	L to N	90	2	10	PASS – No AR
230	-4000	L to N	90	2	10	PASS – No AR
230	+4000	L to N	270	2	10	PASS – No AR
230	-4000	L to N	270	2	10	PASS – No AR

Table 12 – Combination Wave Differential Mode Surge.

14.2 Ring Wave Surge

The unit passed the 4 kV ring-wave surge test in both differential-mode and common-mode setups, with no auto restart (AR), no output interruption, and no component damage.

14.2.1 Ring Wave Differential Mode

AC Input Voltage (VAC)	Surge Voltage (kV)	Coupling	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4000	L to N	0	12	10	PASS – No AR
230	-4000	L to N	0	12	10	PASS – No AR
230	+4000	L to N	90	12	10	PASS – No AR
230	-4000	L to N	90	12	10	PASS – No AR
230	+4000	L to N	270	12	10	PASS – No AR
230	-4000	L to N	270	12	10	PASS – No AR

Table 13 – Ring Wave Surge-Differential Mode Test Results.

14.2.2 Ring Wave Common Mode Surge

AC Input Voltage (VAC)	Surge Voltage (V)	Coupling	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+4000	L, N, PE	0	12	10	PASS – No AR
230	-4000	L, N, PE	0	12	10	PASS – No AR
230	+4000	L, N, PE	90	12	10	PASS – No AR
230	-4000	L, N, PE	90	12	10	PASS – No AR
230	+4000	L, N, PE	270	12	10	PASS – No AR
230	-4000	L, N, PE	270	12	10	PASS – No AR

Table 14 – Ring Wave Surge – Common Mode Test Results.

14.3 EFT/Burst Immunity Test

The unit passed the 4 kV EFT test in both differential-mode and common-mode setups, with no auto-restart events, no output interruption, and no component damage.

14.3.1 Differential Mode Coupling

Surge Voltage	Phase	Coupling	Frequency	Burst Time	Burst Period	Test Duration	Result
+4000 V	0º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	0º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	0º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR
–4000 V	0º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR
+4000 V	90º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	90º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	90º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR
–4000 V	90º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR
+4000 V	270º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	270º	L to N	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	270º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR
–4000 V	270º	L to N	100 kHz	750 μs	300 ms	120 s	PASS – No AR

Table 15 – Differential Mode EFT/Burst Immunity Test Results.

14.3.2 Common Mode Coupling

Surge Voltage	Phase	Coupling	Frequency	Burst Time	Burst Period	Test Duration	Result
+4000 V	0º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	0º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	0º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR
–4000 V	0º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR
+4000 V	90º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	90º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	90º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR
–4000 V	90º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR
+4000 V	270º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
–4000 V	270º	L, N, PE	5 kHz	15 ms	300 ms	120 s	PASS – No AR
+4000 V	270º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR
–4000 V	270º	L, N, PE	100 kHz	750 µs	300 ms	120 s	PASS – No AR

Table 16 – Common Mode EFT/Burst Immunity Test Results.

15 ESD Immunity

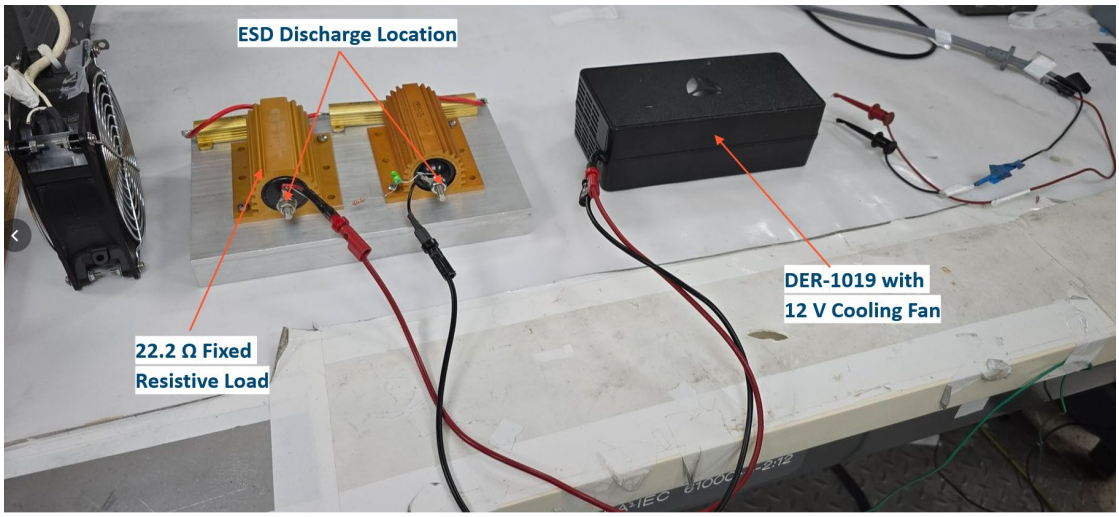


Figure 83 – ESD Immunity Test Set-up.

15.1 Air Discharge ESD Test

The unit passed the ESD test at 16.5 kV air discharge and 8.8 kV contact discharge, with no auto-restart events, no output interruption, and no component damage.

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	8	Output +	10	PASS - No AR
230	-8	Output +	10	PASS - No AR
230	8	Output -	10	PASS - No AR
230	-8	Output -	10	PASS - No AR
230	12	Output +	10	PASS - No AR
230	-12	Output +	10	PASS - No AR
230	12	Output -	10	PASS - No AR
230	-12	Output -	10	PASS - No AR
230	15	Output +	10	PASS - No AR
230	-15	Output +	10	PASS - No AR
230	15	Output -	10	PASS - No AR
230	-15	Output -	10	PASS - No AR
230	16.5	Output +	10	PASS - No AR
230	-16.5	Output +	10	PASS - No AR
230	16.5	Output -	10	PASS - No AR
230	-16.5	Output -	10	PASS - No AR

Table 17 – ESD Immunity Air Discharge Test.

15.2 Contact Discharge ESD Test

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	8.8	Output +	10	PASS - No AR
230	-8.8	Output +	10	PASS - No AR
230	8.8	Output -	10	PASS - No AR
230	-8.8	Output -	10	PASS - No AR

Table 18 – ESD Immunity Contact Discharge Test.

16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
17-Mar-26	MGM/JMR/MA	A	Initial Release.	Apps & Mktg
18-June-26	MGM	B	Update C2 and C3, Remove C4 and Add C46	Apps & Mktg

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