Design Example Report

Title	**100 W Isolated Flyback Power Supply with Adjustable 5 – 28 V Output Using InnoSwitch™5-Pro INN5376F-H901**
Specification	180 VAC – 265 VAC Output: (100W) 5 V / 5 A; 9 V / 5 A; 15 V / 5 A; 20 V / 5 A; 28 V / 3.57 A Outputs 90 VAC – 132 VAC Outputs (65W) 5 V / 3.25 A; 9 V / 3.25 A; 15 V / 3.25 A; 20 V / 3.25 A; 28 V / 2.32 A
Application	Programmable Industrial Power Supply
Author	Applications Engineering Department
Document Number	DER-1001
Date	May 14, 2025
Revision	A

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Summary and Features

- Comprehensive protection features with fault monitoring and telemetry reporting of power supply status.
- Advanced SR FET control enables Zero voltage switching (ZVS) across line and output voltage range.
  - Easily meets DOE6 and CoC v5 2016 average efficiency requirements
  - 5 V output: 92.5% at 115 VAC (16.25 W) (10.7% margin); 92.6% at 230 VAC (25 W) (10.8% margin)
  - 20 V output: 92.3% at 115 VAC (65 W) (3.3% margin); 93.5% at 230 VAC (100 W) (4.49% margin)
  - 28 V output: 91% at 115 VAC (65 W) (2.05% margin); 92.8% at 230 VAC (100 W) (3.81% margin)
- Meets CoC v5 2016 10% requirements with >8% margin
- <35 mW no-load input power at 230 VAC
- Easily meets CISPR22 / EN55022 Class B conducted EMI
  - >5 dB margin -worst case (28 V / 3.57 A (100 W), 230 VAC)
- High power density: 11.13 W / inch^3 without enclosure (3.31" x 2.95" x 0.92" form factor)
- Only 84 electrical components

Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This design engineering report describes a power supply using InnoSwitch5-Pro INN5376F-H901 IC. This report primarily presents the design and implementation of a programmable wide-output voltage power supply, utilizing a generic micro controller (in this case Microchip PIC16F18325) for control.

The microcontroller controls the InnoSwitch5-Pro via an I^{2}C interface, programming its command and telemetry registers. This design dynamically adjusts the rated output power capability for both high and low line by utilizing secondary-side input line sensing feature in the InnoSwitch5-Pro IC.

This report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, transformer documentation, and performance data. The firmware used with this report enables constant voltage (CV), constant current (CC), and constant power modes (CP) available with the InnoSwitch5-Pro family.

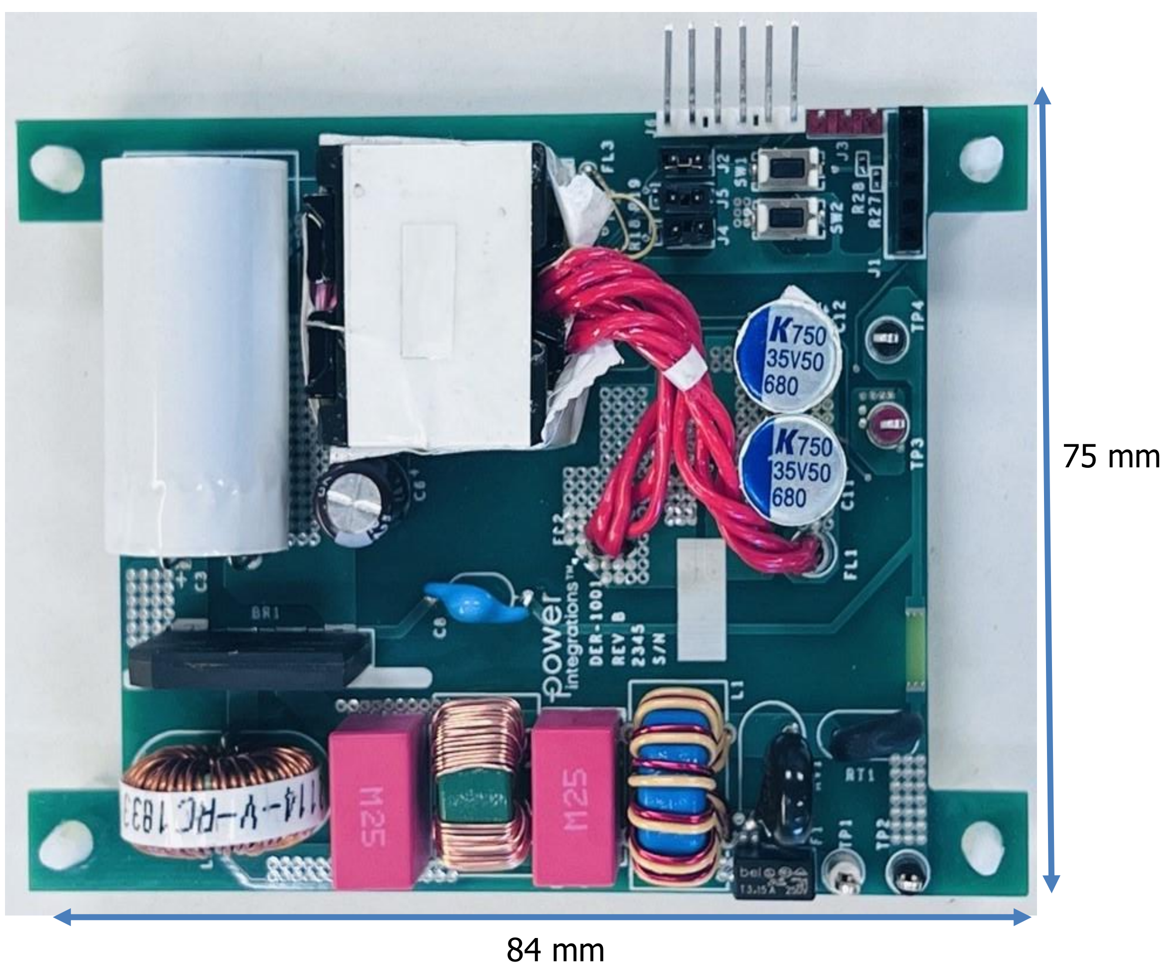


Figure 1 – Populated Circuit Board- Top.

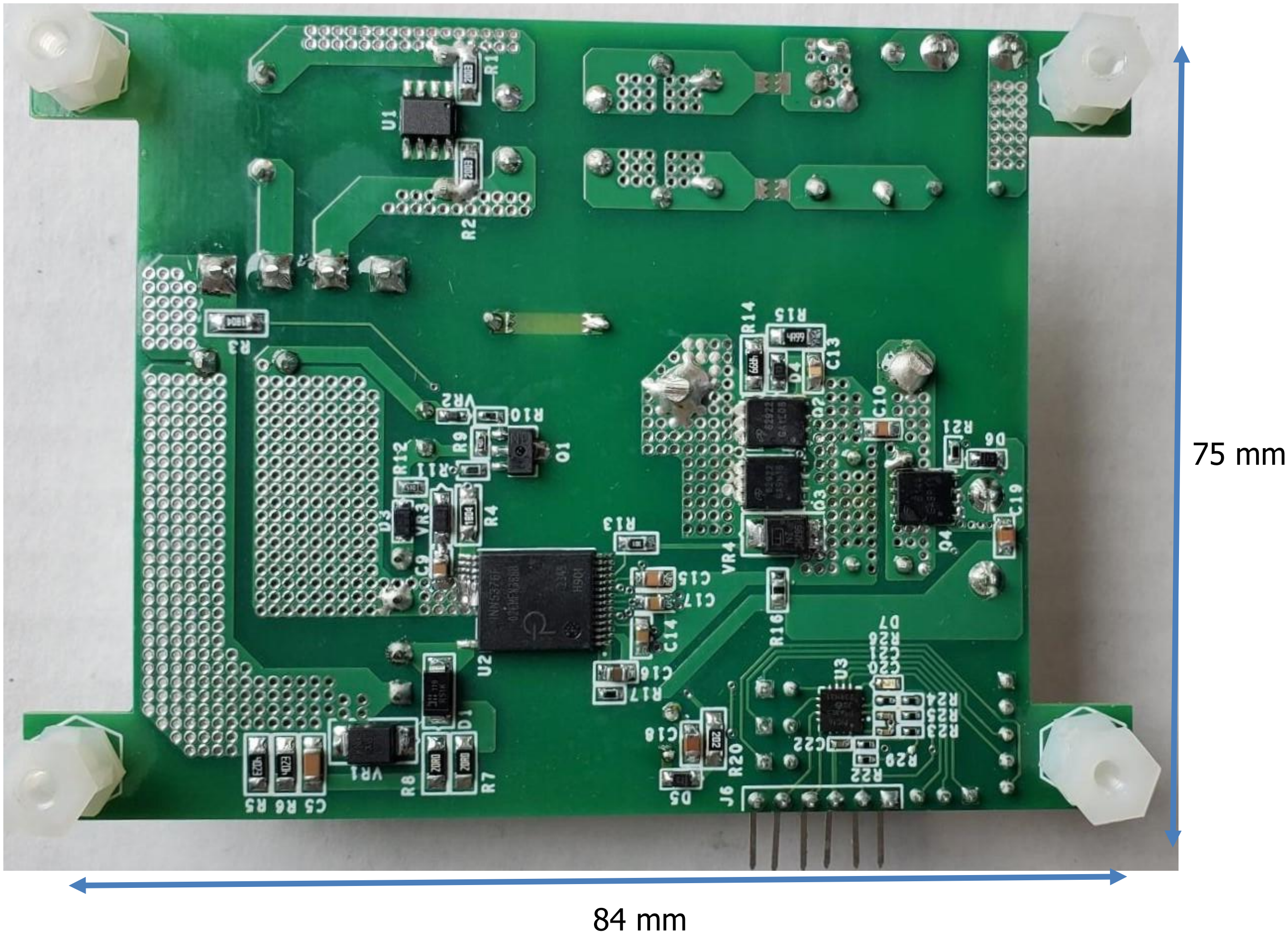


Figure 2 – Populated Circuit Board - Bottom.

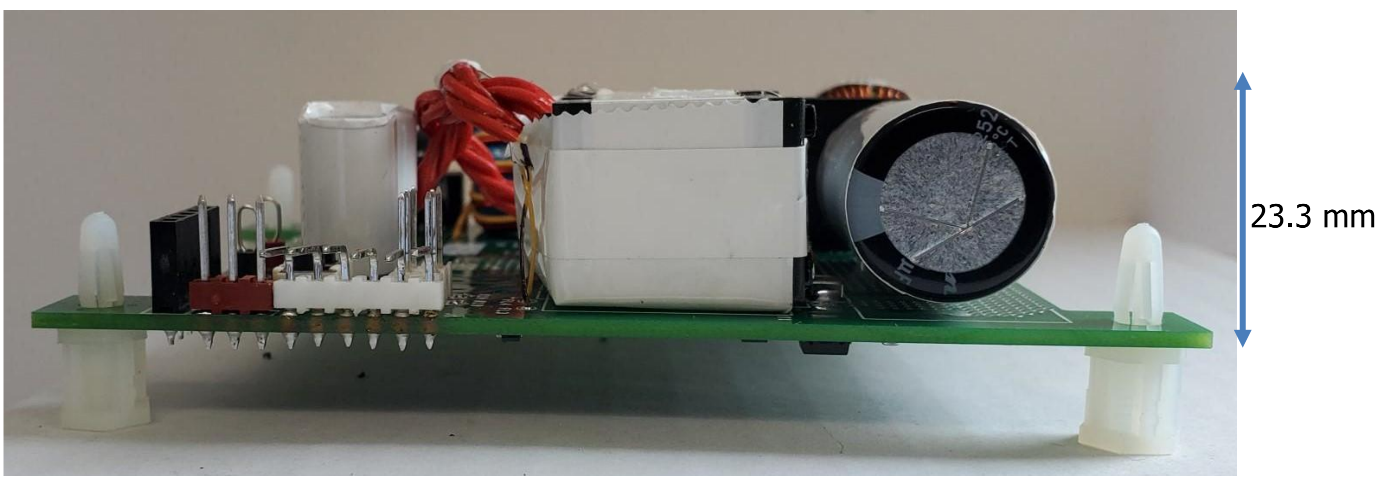


Figure 3 – Populated Circuit Board (Side View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design for high-line input range. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	180		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				35	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			5.0	A	±3%
Average Efficiency	η_{5V}		92		%	Measured at 230 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(5\ V)}$			25	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			5.0	A	±3%
Average Efficiency	η_{9V}		93		%	Measured at 230 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(9\ V)}$			45	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			5.0	A	±3%
Average Efficiency	η_{15V}		93		%	Measured at 230 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(15\ V)}$			75	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			5.0	A	±3%
Average Efficiency	η_{20V}		93		%	Measured at 230 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(20\ V)}$			100	W	
28 V Setting						
Output Voltage	$V_{OUT(28\ V)}$		28.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(28\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(28\ V)}$			3.57	A	±3%
Average Efficiency	η_{28V}		92		%	Measured at 230 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(28\ V)}$			100	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

The table below represents the minimum acceptable performance of the design for low-line input range. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				20	mW	Measured at 115 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(5\ V)}$			3.25	A	±3%
Average Efficiency	η_{5V}		92		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(5\ V)}$			16.2	W	
9 V Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			100	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(9\ V)}$			3.25	A	±3%
Average Efficiency	η_{9V}		92		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(9\ V)}$			29.2	W	
15 V Setting						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(15\ V)}$			3.25	A	±3%
Average Efficiency	η_{15V}		92		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(15\ V)}$			48.7	W	
20 V Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(20\ V)}$			3.25	A	±3%
Average Efficiency	η_{20V}		92		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(20\ V)}$			65	W	
28 V Setting						
Output Voltage	$V_{OUT(28\ V)}$		28.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(28\ V)}$			75	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT(28\ V)}$			2.32	A	±3%
Average Efficiency	η_{28V}		91		%	Measured at 115 VAC from AC Receptacle to Output Terminals.
Continuous Output Power	$P_{OUT(28\ V)}$			65	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Note A: Output voltage ripple is measured at the end of 100 mΩ cable with the probe with decoupling capacitors 47 μF electrolytic and 100 nF ceramic in parallel.
B: Output current limit accuracy is within ±150 mA for operating current between 1 A and 3 A, or ±5% for operating current >3 A.

Note: The output terminals in this design do not support a USB Type-C connector. To use this design for a charger / adapter with a different shape and form factor, changes in the circuit board layout must be made to meet the target specifications for EMI, ESD, and line surge performance.

The summary of output capabilities of the power supply at low-line and high-line are listed in the table below.

Output Voltage (V)	Rated Output Current (A) @90 VAC to 132 VAC	Rated Output Current (A) @180 VAC to 265 VAC
5	3.25	5
9	3.25	5
15	3.25	5
20	3.25	5
28	2.32	3.57

Table 1. Maximum programmable output current under low-line and high-line input voltage for different programmable outputs.

Note: The source capabilities for low line are defined for 90-132 VAC, the power supply delivers low line output voltage/current for AC input voltage <180 VAC.

3 Schematic

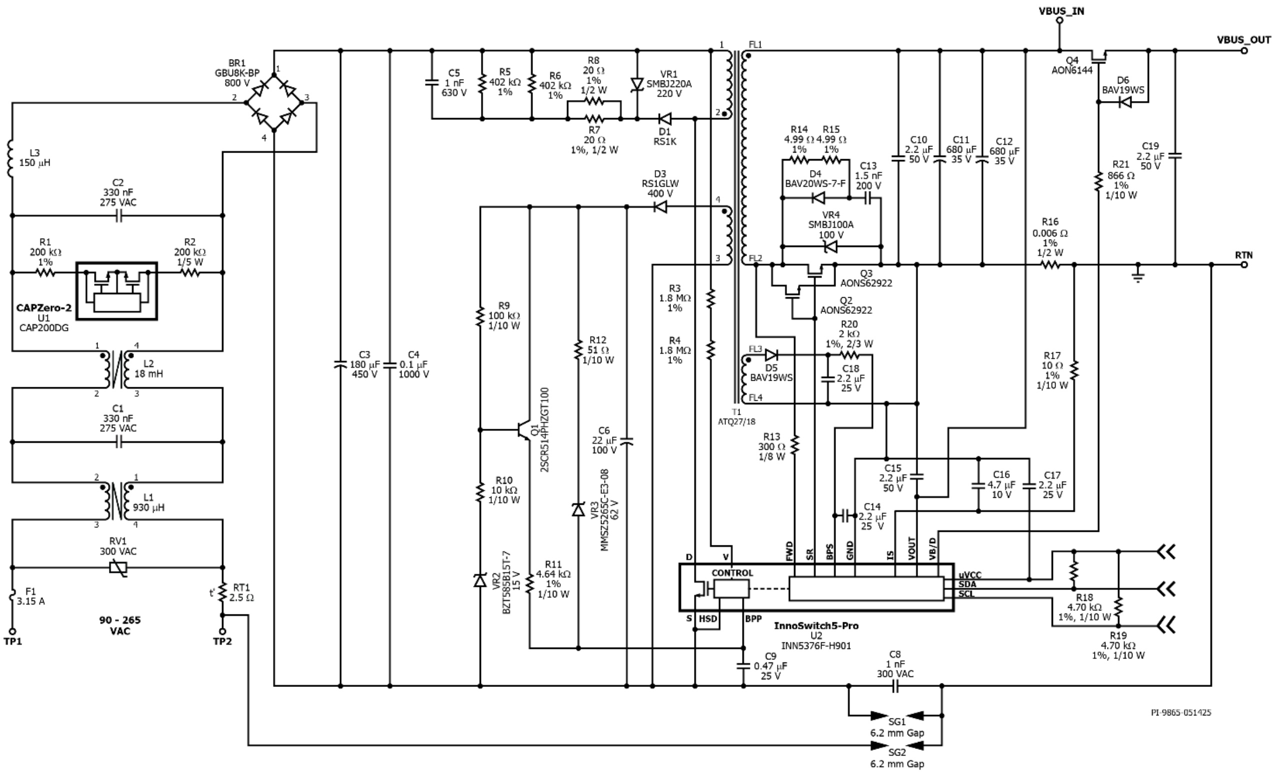


Figure 4 – Schematic for Power Conversion Stage.

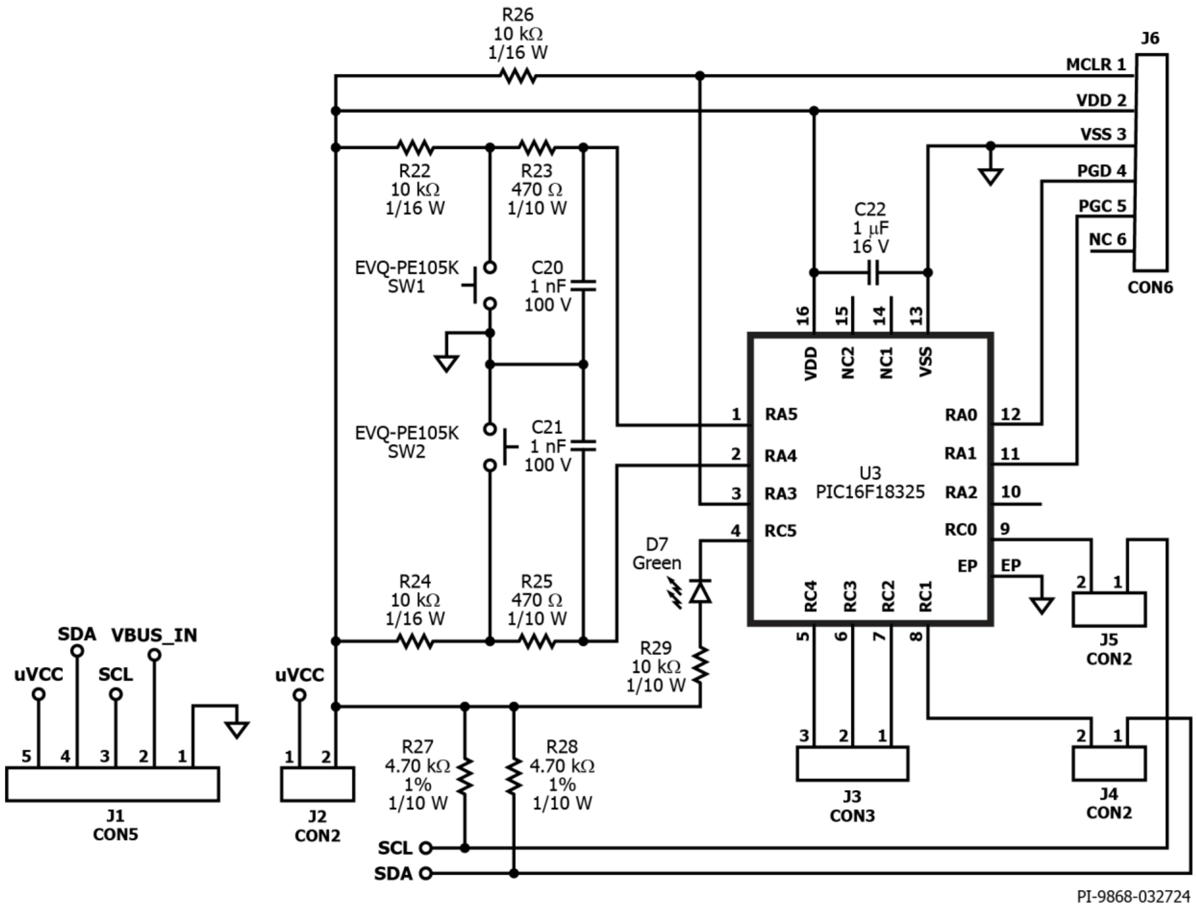


Figure 5 –Schematic for Microcontroller Stage.

4 Circuit Description

4.1 Input Rectifier and EMI Filter

Input fuse F1 isolates the circuit and protects against component failure. Metal Oxide Varistor (MOV) RV1 provides protection during line surge events by clamping the input voltage seen by the power supply. Thermistor RT1 limits the inrush current when the power supply is connected to line. Common mode chokes L1, L2 and Y capacitor C8 provide common mode noise filtering while X capacitors C1, C2 and differential choke L3 provide differential mode EMI filtering. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the bulk capacitor C3. Capacitor C4 serves as a high frequency filter capacitor, providing a low impedance path for high frequency switching currents.

4.2 InnoSwitch5-Pro IC Primary

One end of the transformer primary is connected to the rectified DC bus. The other end is connected to the drain terminal of the switch inside the InnoSwitch5-Pro IC (U2). Resistors R3 and R4 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage which is sensed via the V-pin.

A primary clamp formed by diode D1, capacitor C5, resistors R5 to R8 limit the peak drain voltage across U2 at the instant of its turn-off. Energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C5. Varistor VR1 is used to protect the InnoSwitch5-Pro IC from excessive drain voltages when the power supply is subjected to abnormal input conditions.

The InnoSwitch5-Pro IC primary controller turns on the primary switch upon receiving a switching request from the secondary-side through FluxLink™ - a proprietary isolated communication link within the InnoSwitch IC that uses Magneto-inductive coupling to transmit data.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C9 when AC input is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output from the auxiliary (or bias) winding is rectified using diode D3 and filtered by capacitor C6. A linear regulator circuit comprised of BJT Q1, R9, R10, R11, and Zener diode VR2 ensures that sufficient current flows through R11 into the BPP pin of the InnoSwitch5-Pro IC. When sufficient current is injected to the BPP pin by this means, the internal current source of U2 (fed by the drain pin) is disabled. This ensures that power consumption is minimized during normal operation.

Zener diode VR3 offers primary sensed output overvoltage protection. The output of the auxiliary winding tracks the output voltage of the converter. When an overvoltage at the output of the converter occurs, the auxiliary winding voltage increases and causes breakdown of VR3. This causes excess current to flow into the BPP pin of InnoSwitch5-Pro IC. When the input current exceeds the I_{SD} threshold, the InnoSwitch5-Pro will latch off to prevent any further increase in output voltage. Resistor R12 limits the current injected into BPP pin when output overvoltage protection is triggered.

4.3 InnoSwitch5-Pro IC Secondary

The secondary-side of the InnoSwitch5-Pro IC provides sensing for both output voltage and load current, and provides gate-drive for synchronous rectification and the switch on the output bus. Voltage across the transformer's secondary winding is rectified by the secondary-side synchronous rectifier FETs (SR FETs) Q2 and Q3, and filtered by capacitors C10, C11 and C12. High frequency ringing across the SR FETs arising during switching transients are reduced via an RCD snubber, R14, R15, C13, and D4 to limit radiated EMI. Diode D4 minimizes the dissipation in resistors R14 and R15.

The gates of Q2 and Q3 are turned on by the secondary-side SR pin on IC U2, based on the secondary winding voltage sensed via resistor R13 which is connected between the drain of the SR FET and the FWD pin of the IC.

In continuous conduction mode (CCM), the SR FET is turned off just prior to the secondary-side requesting a new switching cycle from the primary. In discontinuous conduction mode of operation (DCM), the SR FET is turned off when magnitude of voltage drop across SR FET falls below a threshold of approximately $V_{SR(TH)}$. In the SR -Zero Voltage Switching (SR-ZVS) mode of operation, the SR FET is turned on for a pre-programmed duration, followed by SR FET turn off at another pre-programmed point prior to secondary sending a switching request to the primary. Secondary-side control of the turn on of both the SR and the primary-side power switch avoids any possibility of cross conduction and provides extremely reliable synchronous rectifier operation while maximizing efficiency.

The secondary-side controller is powered from either the secondary winding Forward-pin voltage or the output voltage of the power supply. For this design, a secondary bias winding circuit is used when the output voltage ≥9 V to further improve the Innoswitch5-Pro thermal performance and increase system efficiency. The bias winding output is rectified by diode D5 and filtered by capacitor C18. Resistor R20 limits the current flowing into the BPS pin of U2. Capacitor C14 is connected to the BPS pin of InnoSwitch5-Pro IC and provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R16. This measured voltage is filtered with resistor R17 and capacitor C16, and applied to the IC as a potential across IS and SECONDARY GROUND pins. An internal current sense threshold of up to 32 mV (configured by the microcontroller via I^2C interface) is used to reduce losses. Once the threshold is exceeded, the InnoSwitch5-Pro IC responds (depending on its configuration) to either maintain a fixed output current by using variable frequency and variable primary switch peak current limit control scheme to maintain a fixed output current or to shut down the power supply. The response is programmable using microcontroller via I^{2}C interface.

For constant current (CC) operation, when the output voltage drops below 5 V, the secondary-side controller inside InnoSwitch5-Pro IC will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the voltage which appears across secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C14 via resistor R13 on the FWD pin. Voltage is controlled by an internal regulator connected to the BPS pin. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level, the unit enters auto-restart until the output load is reduced.

When output current is below the CC threshold, the converter operates in constant voltage mode. Output voltage is monitored by the VOUT pin of InnoSwitch5-Pro IC. In a similar approach to that used for constant current regulation, the output voltage is also compared to an internal voltage threshold set via the integrated secondary controller of the InnoSwitch5-Pro IC and microcontroller IC and switching cycles requested as required. Output voltage regulation is achieved by a variable frequency, variable primary-switch peak-current-limit control scheme. Capacitor C15 is used as decoupling capacitor for the VOUT pin.

An N-channel MOSFET Q4 functions as the bus switch which connects or disconnects the output of the flyback converter to the power supply output. MOSFET Q4 is controlled by the VB/D pin on the InnoSwitch5-Pro IC. Diode D6 is connected across the Source and Gate terminals of Q4 and resistor R21 is placed between Gate terminal of Q4 and VB/D pin to provide a discharge path for the bus voltage when Q4 is turned off. Capacitor C19 is used at the output for ESD protection.

4.4 Microchip Microcontroller

This design uses PIC16F18325-I/JQ microcontroller. This device is powered directly from the uVCC pin of InnoSwitch5-Pro IC (U2). Communication between these 2 devices occurs through I^{2}C interface, using SCL and SDA lines by which it sets command registers, to control CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold of the InnoSwitch5-Pro IC, respectively. The status of InnoSwitch5-Pro IC is read by the microcontroller from telemetry registers, also using the I^{2}C interface.

The 2 pin connectors J2, J4 and J5 are provided to connect/disconnect the uVCC, SDA, SCL connections between the PIC microcontroller and InnoSwitch5-Pro IC respectively. When using the PIC microcontroller to issue commands to the InnoSwitch5-Pro IC, these jumpers must be connected as shown in Figure 6 . If a different microcontroller is used, these jumpers can be removed to allow the connection of a different microcontroller to the appropriate pins on the InnoSwitch5-Pro IC.

4.5 Digital Control

In this design, PIC16F18325 is the I^2C master and InnoSwitch5-Pro IC is the slave device. Output of the InnoSwitch5-Pro IC powers the MCU directly from its uVCC output pin.

The PIC16F18325 microcontroller communicates via its I^2C lines to the SDA and SCL pins (which are both 3.3 V and 5 V compatible) of the InnoSwitch5-Pro IC. SDA and SCL inputs require pull-up resistors (R18 and R19 respectively) connected to the uVCC pin. The uVCC pin has a decoupling capacitor C17.

The MCU enables dynamic control of output voltage, current and configurable features (CVO, fault responses, line sensing, DCM only, SR-ZVS etc) through the I^2C Bus. The I^2C clock frequency is set to 400 kHz on this design.

4.5.1 SR-ZVS Feature

To improve efficiency and eliminate the switching losses, SR-ZVS mode of operation is enabled throughout the operating line and output voltage range. The InnoSwitch5-Pro features a line voltage sensing capability, where the microcontroller on secondary side calculates the line voltage based on the measured TON and TOFF parameters. Both the SR-ZVS ON and SR-ZVS Delay time can be adjusted through I^2C commands. The SR-ZVS ON and SR-ZVS Delay parameters used in this design are shown in Table.2.

Output Voltage (V)	**SR-ZVS parameters at Low Line**		**SR-ZVS parameters at High Line**	
	Delay count	**ON count**	**Delay count**	**ON count**
5	4	18	4	31
9	4	8	4	19
15	4	5	4	10
20	4	4	4	7
28	4	3	4	5

Table 2. SR-ZVS ON and Delay parameters

4.6 Headers and Jumpers Settings

Headers J2, J4, J5 and jumpers J2_1, J4_1, J5_1 shown in Figure 6 establish uVCC, SDA and SCL connections respectively between the PIC Microcontroller and InnoSwitch5-Pro. When jumpers are placed on their respective headers, connection is established and I^2C communication can occur between the two.

Jumper	Description	Settings
J1	InnoSwitch5-Pro I^2C Lines Header	When J4_1 and J5_1 are removed, an external I^2C master can be connected through this header.
J2_1	uVCC and MCU Supply Jumper	Provides power from the uVCC output pin of the InnoSwitch5-Pro to the microcontroller.
J3	MCU GPIO Header	These pins can be used to change the mode (CV change/VKP change/CC change) as described in section 4.7 of this report.
J4_1, J5_1	I^2C Lines Isolation Jumper	Connects SDA and SCL lines from the MCU to the InnoSwitch5-Pro IC.
J6	PICkit3 Programming Header	For MCU firmware update using PICkit3 in-circuit debugger/programmer. NOTE: To successfully connect to PICkit3, make sure to connect the (Δ) marked pins of PICkit3 and J6.

Table 3. Description of jumpers available on board

4.7 Switches

Two tactile switches are present on the board. When idle, the switches are pulled high (+3.3 V). When pressed, they are grounded. On each button press, I^2C commands are generated to make changes in the response of the circuit based on the configuration of the J3 (CON3) connector as described in Table 4.

Configuration #	Pin Connection of J3	Mode
1	Pins 1, 2, 3 Open	CV Change
2	Pins 1 and 2 Shorted	V_{KP} Change
3	Pins 2 and 3 Shorted	CC Change

Table 4. Header (J3) Configuration settings

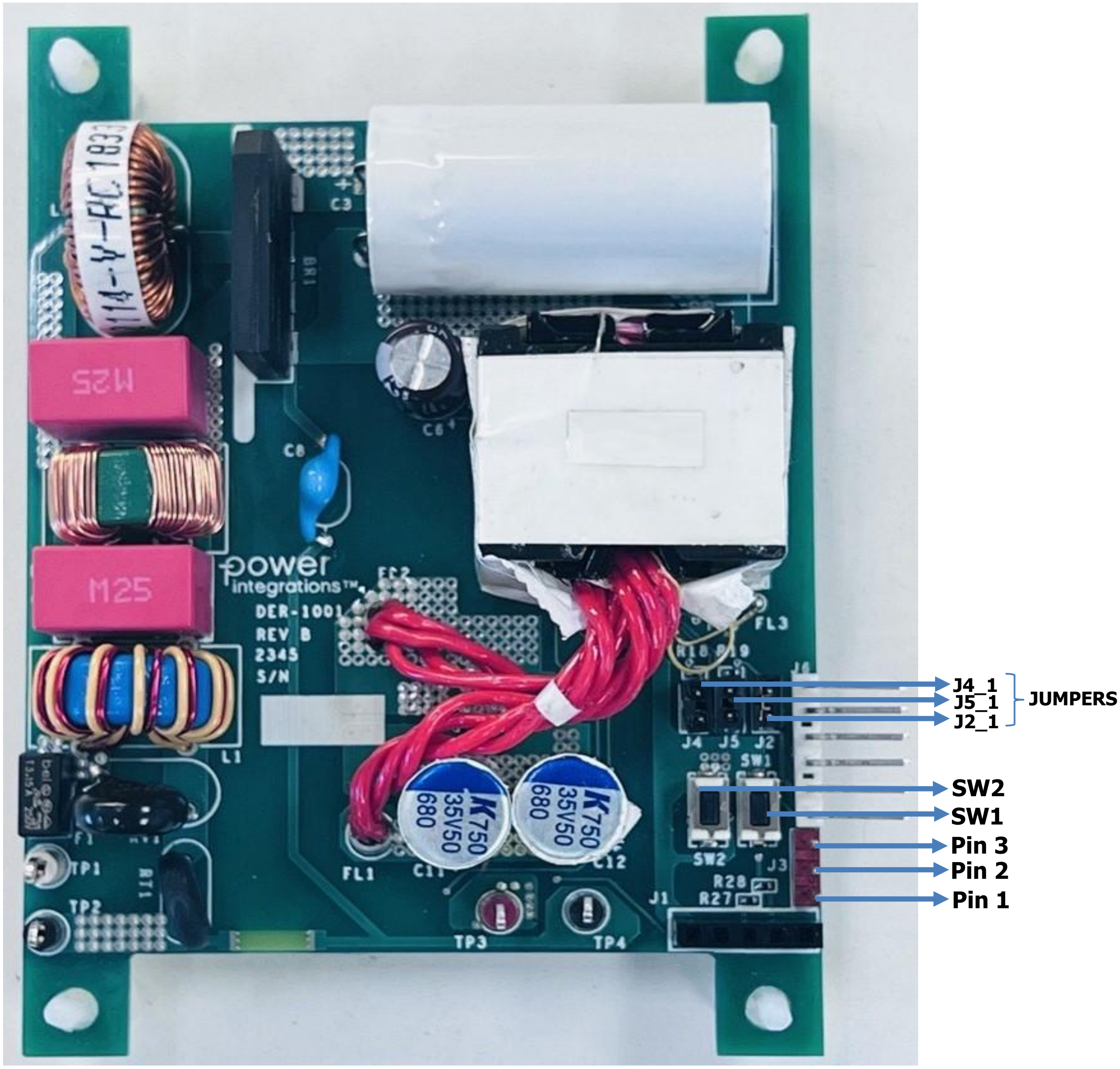


Figure 6 – Board top view with jumper and switch locations.

J2, J4 and J5 are 2 pin connectors. J2_1, J4_1 and J5_1 are their respective jumpers. If the PIC microcontroller on board is used to send commands to InnoSwitch5-Pro IC, these jumpers must be connected.

4.7.1 CV Change

Configuration 1: Pins 1, 2 and 3 open (Not connected)

Identification: Green LED always ON
Function: CV value change
Switch 1 (SW1) Functions:

Action	Function
Single Click	Increment Voltage State
Double Click	Go to 5 V State
Long Press (~5sec)	Enter Low Power Mode

Switch 2 (SW2) Functions:

Action	Function
Single Click	Decrement Voltage State
Double Click	Go to 28 V State
Long Press (~2sec)	Exit Low Power Mode

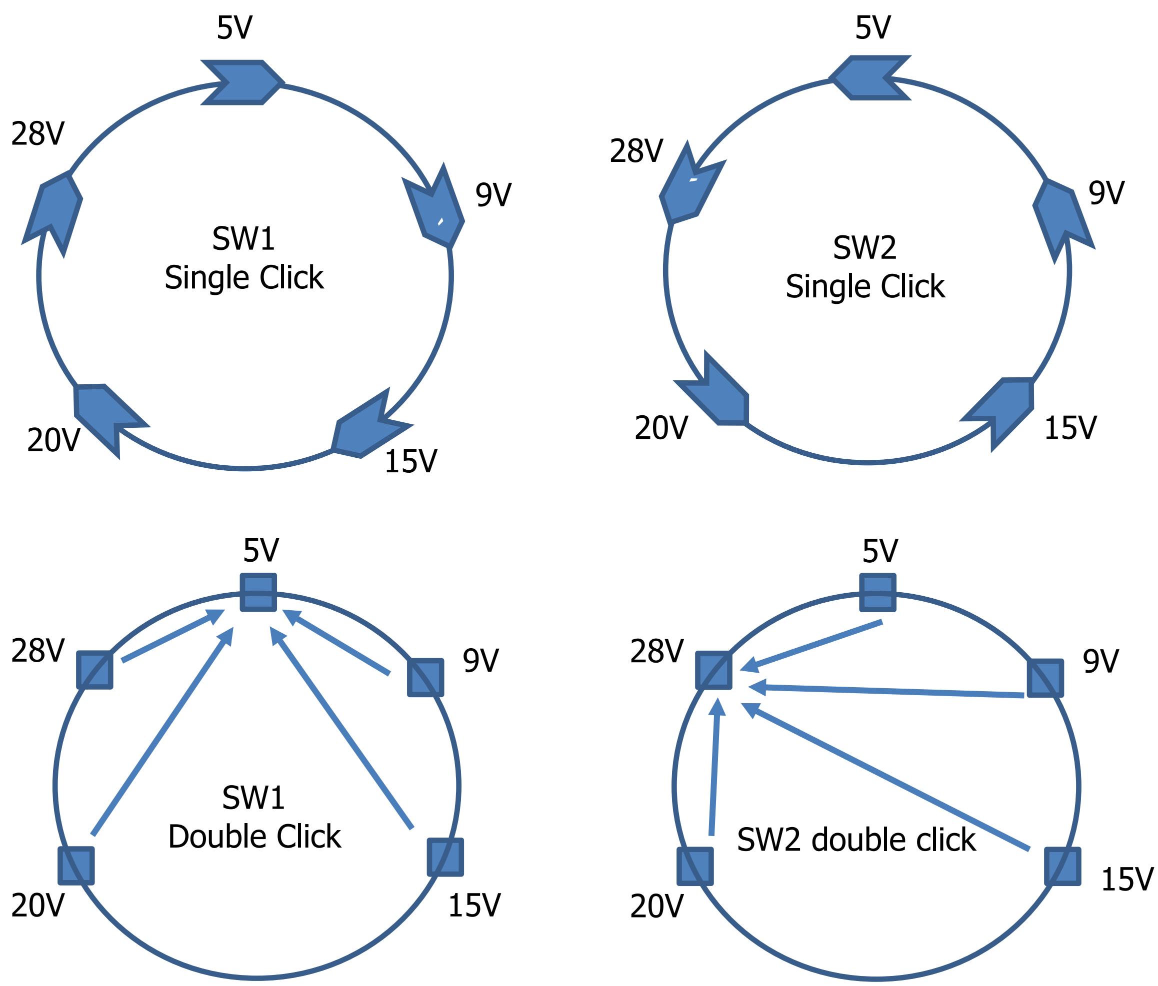


Figure 7a – Output voltage control through Switches (SW1 and SW2)

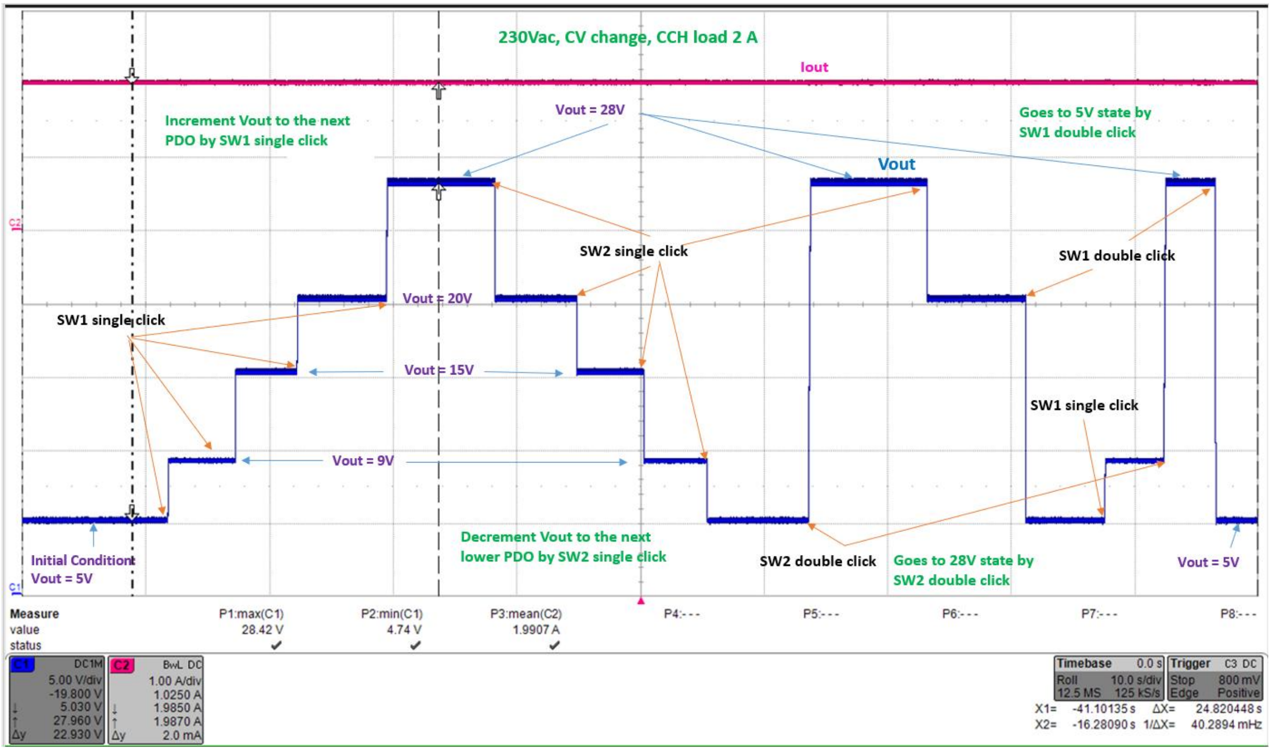


Figure 7b – Waveform Showing CV Change in response to SW1 and SW2 operation.

4.7.2 V_{KP} Change

Configuration 2: Pins 1 and 2 shorted

Identification: Green LED blinks slow (every 1s)
Function: V_{KP} value change
Switch 1 (SW1) Functions:

Action	Function
Single Click	Increment V_{KP} by 1 V
Double Click	Increment V_{KP} by 10 V
Long Press (~5s)	Enter Low Power Mode

Switch 2 (SW2) Functions:

Action	Function
Single Click	Decrement V_{KP} by 1 V
Double Click	Decrement V_{KP} by 10 V
Long Press (~2s)	Exit Low Power Mode

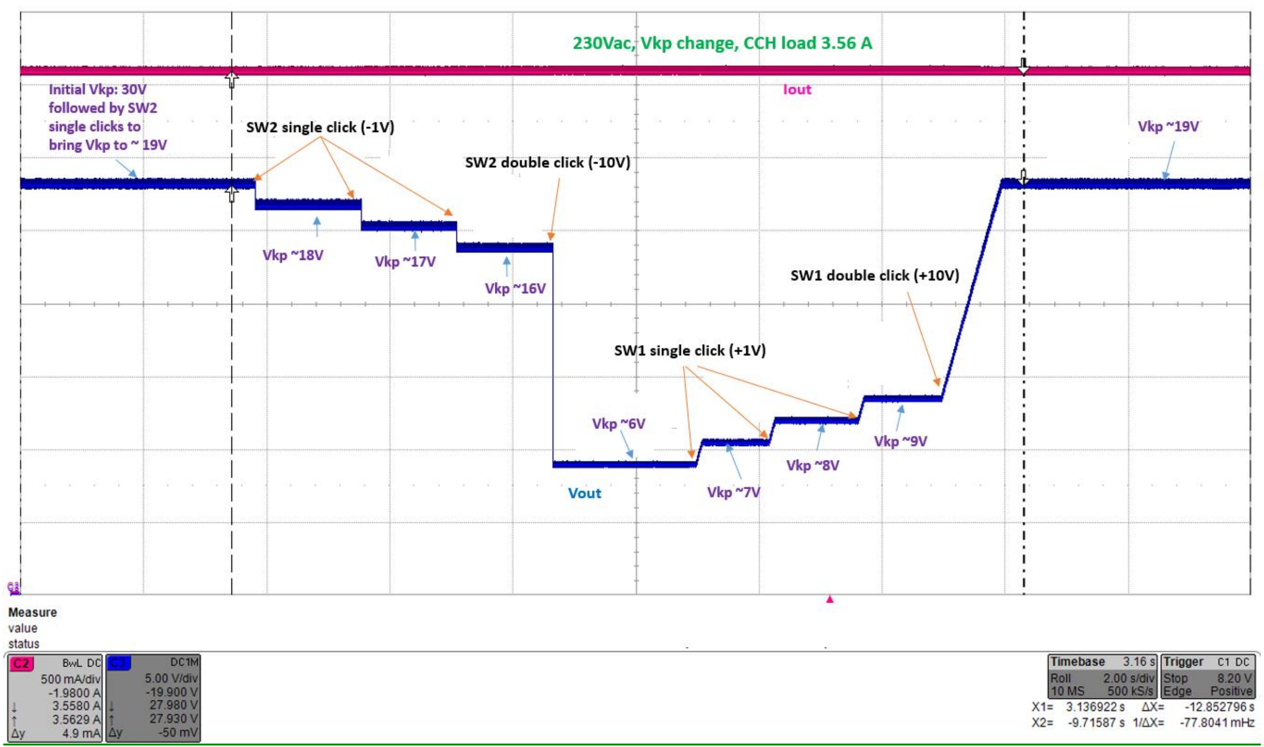


Figure 8 – Waveform Representing V_{KP} Change.

The waveform in Figure 8 shows the response of output voltage with respect to change in V_{KP} and load current. The power supply is operating at a full-scale current of 5.33A.

4.7.3 CC Change

Configuration 3: Pins 2 and 3 shorted

Identification: Green LED blinks fast (every 300ms)
Function: CC value change
Switch 1 (SW1) Functions:

Action	Function
Single Click	Increment CC by 50 mA
Double Click	Increment CC by 250 mA
Long Press (~5s)	Enter Low Power Mode

Switch 2 (SW2) Functions:

Action	Function
Single Click	Decrement CC by 50 mA
Double Click	Decrement CC by 250 mA
Long Press (~2s)	Exit Low Power Mode

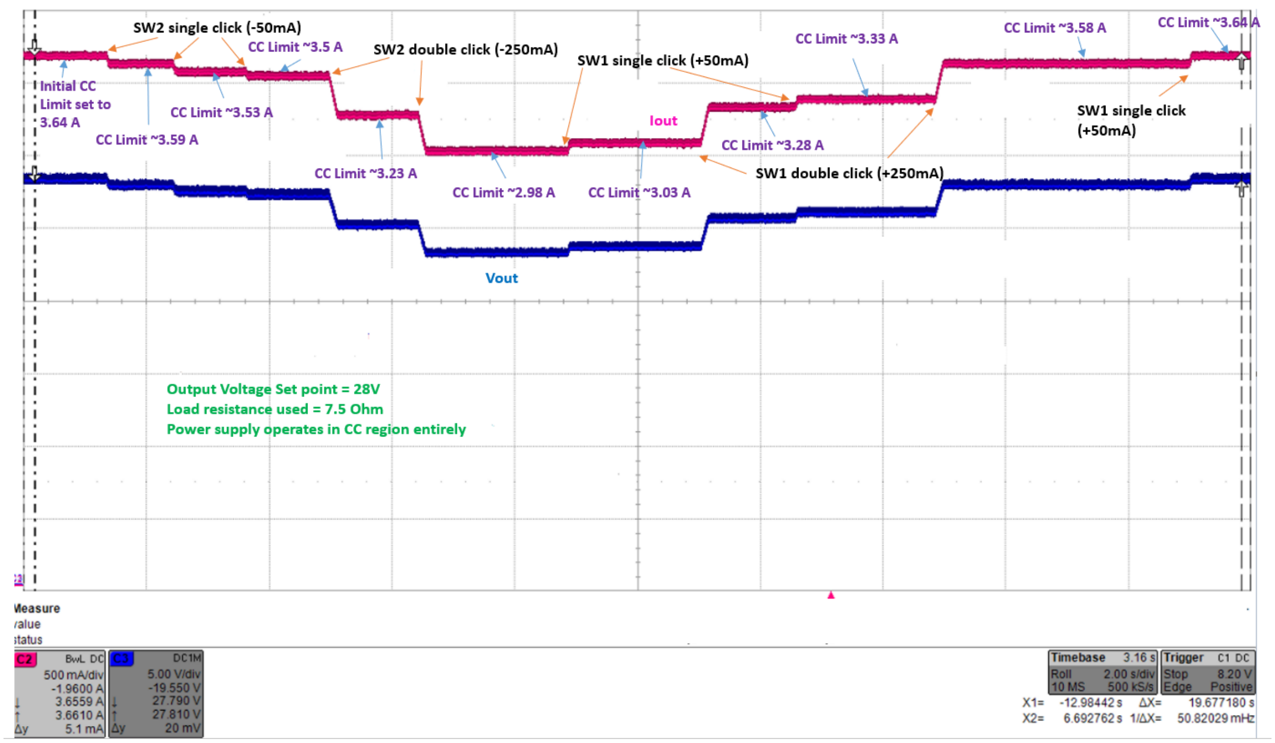


Figure 9 – Waveform Showing CC Change.

4.7.4 Bus Switch ON/OFF

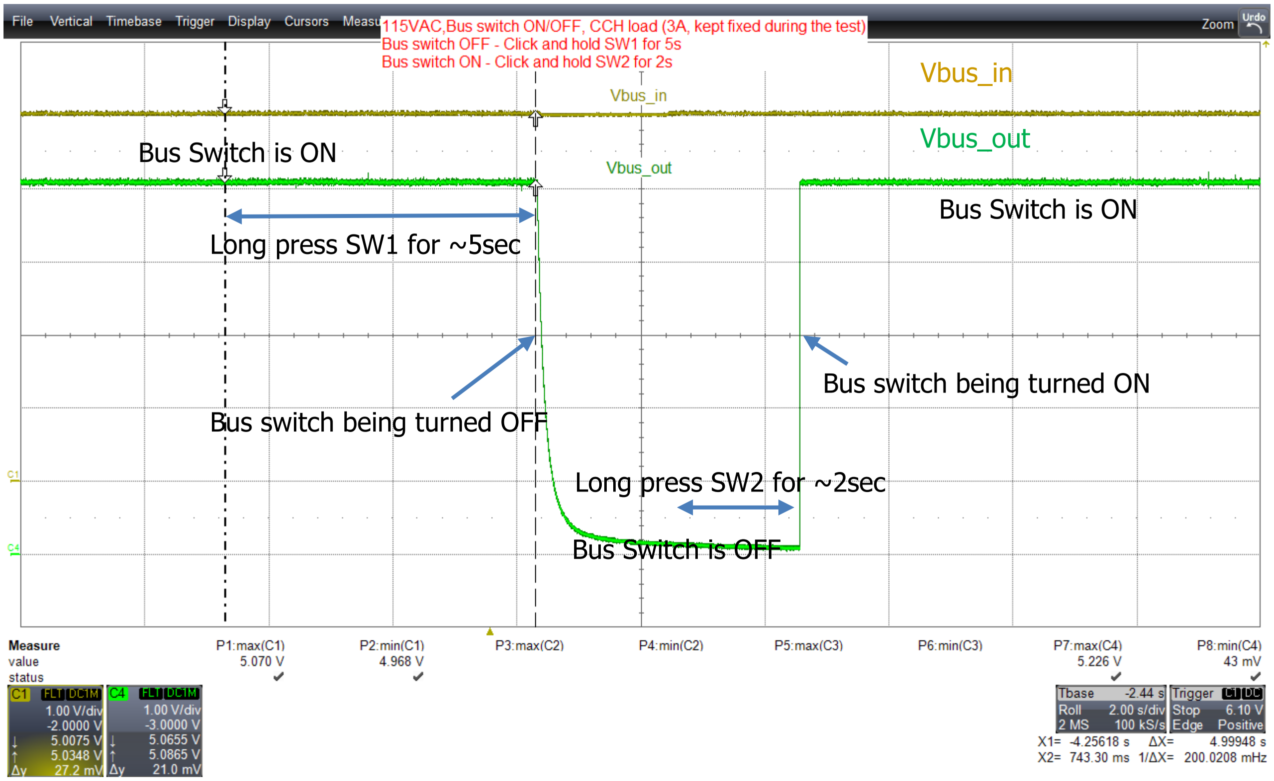


Figure 10 – Waveform Showing Bus Switch ON/OFF.

To open the bus switch, irrespective of the initial input/output voltages, load condition, long press SW1 (~5s). Bus switch can be enabled back when SW2 is pressed for ~2s. The waveform in Figure 10 demonstrates bus switch being disabled and re-enabled.

When initially at output voltages other than 5 V, the output voltage is first brought to 5 V and then the bus switch is opened. While closing the bus switch, output voltage would remain at 5 V unless CV is manually changed by the user by pressing SW1 / SW2.

4.7.5 Low Power Mode

To reduce power consumption at no-load, the low power mode can be enabled. Irrespective of the initial input/output voltages, load condition, connections of Pins 1, 2 and 3 (whether in CV / V_{KP} / CC change mode), the power supply will enter low power mode when SW1 is pressed for ~5s. Idle mode is exited when SW2 is pressed for ~2s. The waveform in Figure 11 demonstrates entering and exiting low power mode.

In low power mode, output voltage is set to 5 V, the bus switch is opened, and current consumption of the PIC microcontroller is significantly reduced.

When initially starting with an output voltage other than 5 V, the output voltage is brought to 5 V and before the bus switch opened. When exiting low power mode, the bus switch will be closed and will remain at 5 V unless CV is manually changed using SW1 / SW2.

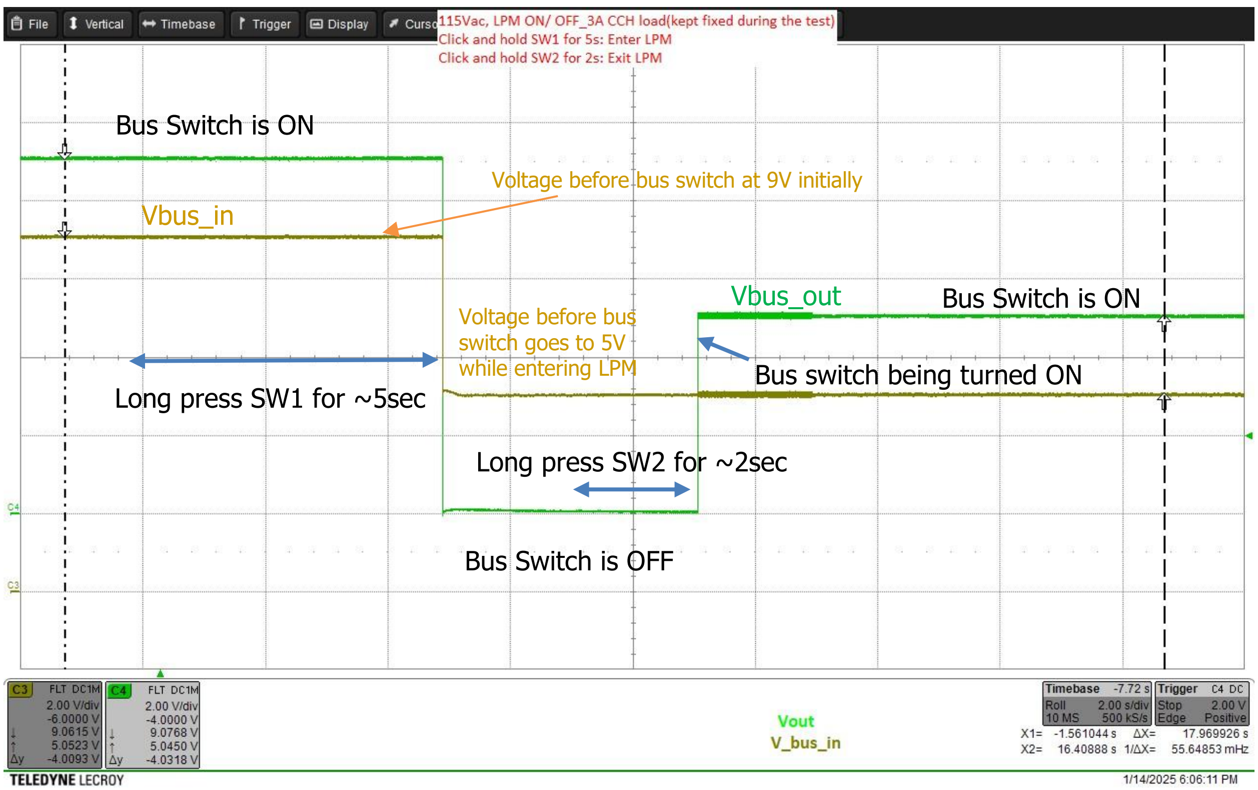


Figure 11 – Waveform Showing LPM Enable/Disable

5 PCB Layout

Material: FR4, 2 oz copper, 1.6 mm thick

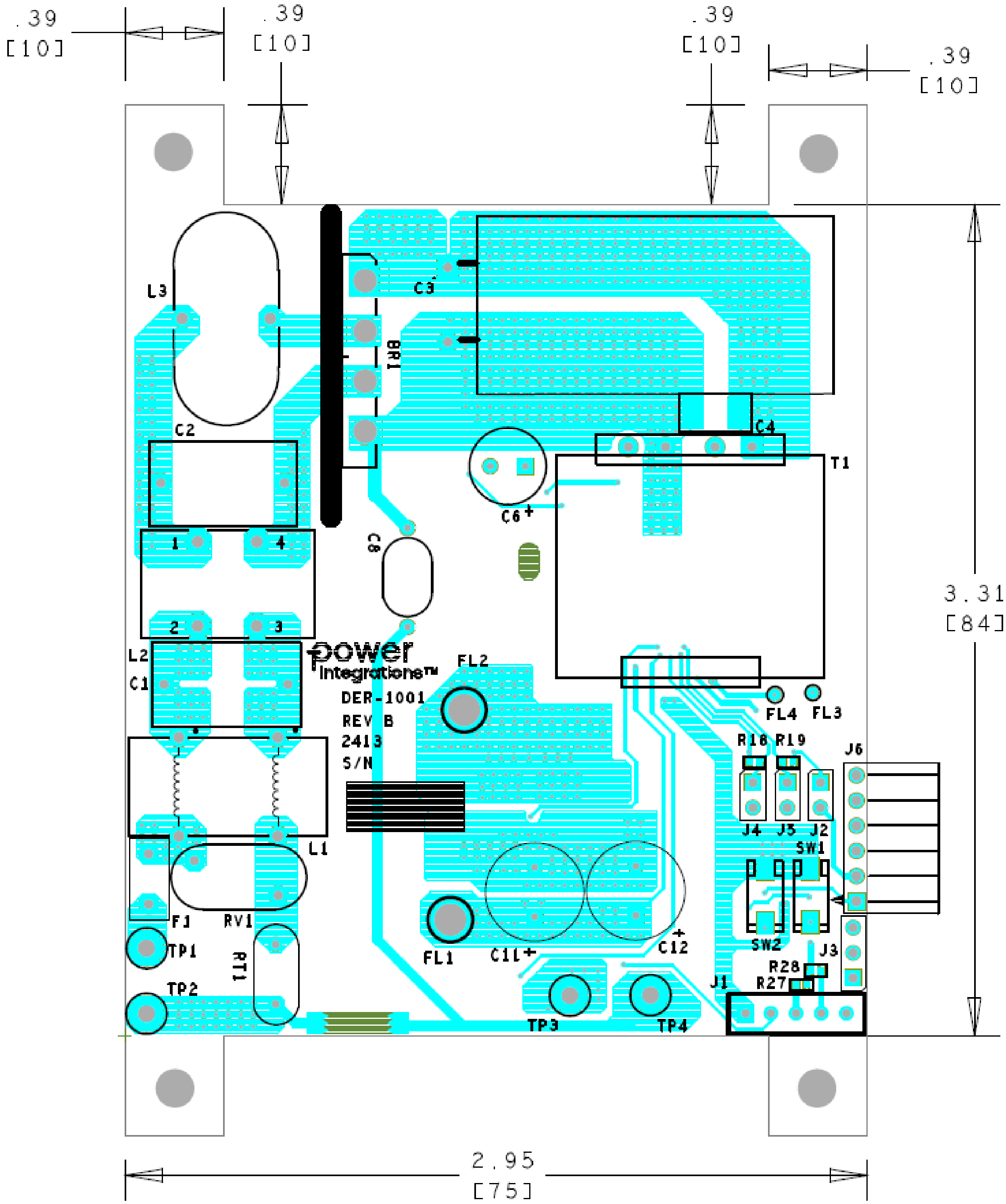


Figure 12 – Printed Circuit Layout, Top.

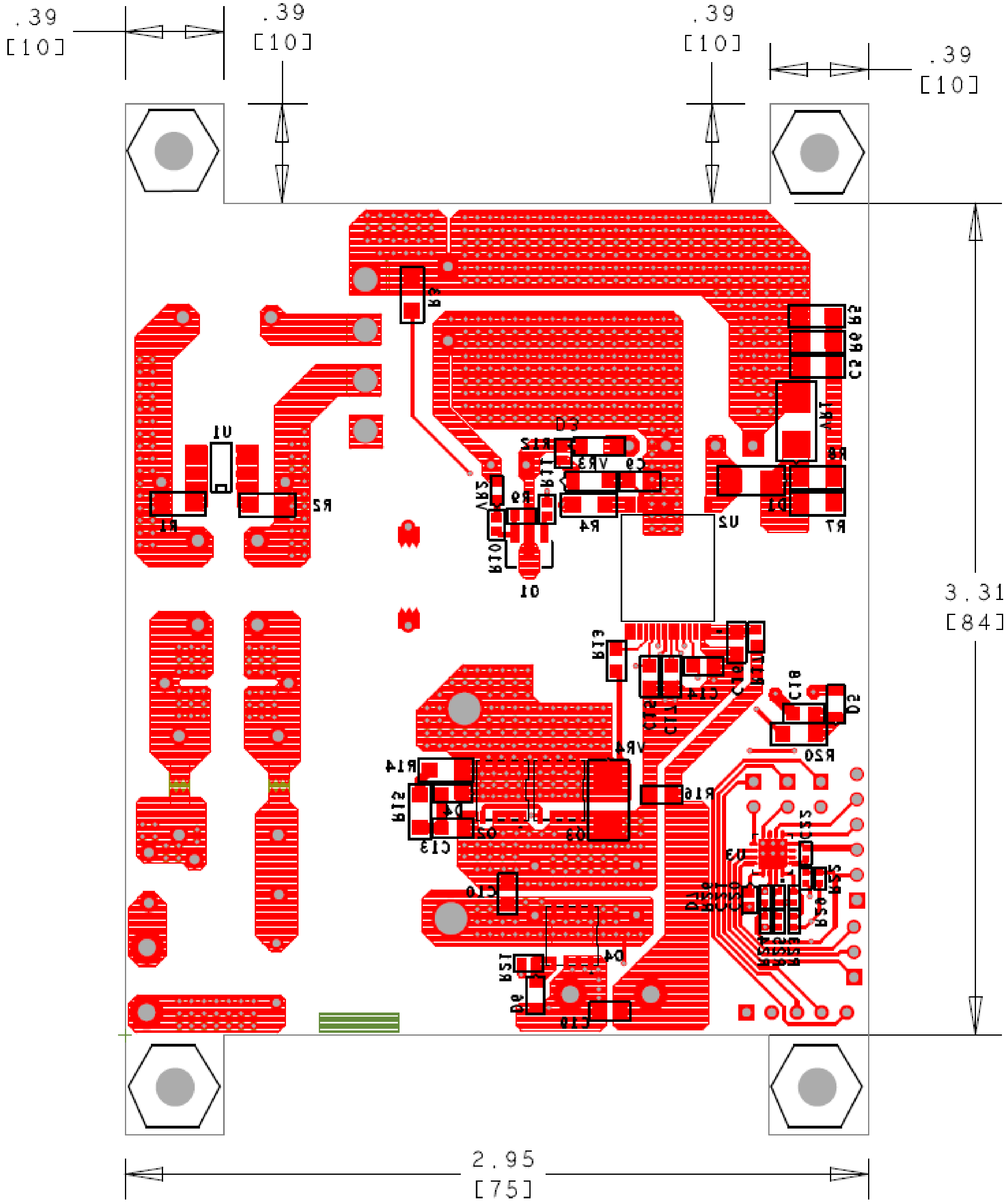


Figure 13 – Printed Circuit Layout, Bottom.

6 Bill of Materials

6.1 Electrical parts

Item	Qty.	Ref Des	Description	Mfr. Part Number	Manufacturer
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	2	C1 C2	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
3	1	C3	180 μF, 420 V, Aluminum Electrolytic Capacitors, Radial, Can, 3000 Hrs @ 105°C, (18 x 35)	420HXW180MEFR18X35	Rubycon
4	1	C4	0.1 μF, ±10%, 1000 V (1 kV), Ceramic Capacitor X7R, 1812	C1812C104KDRAC7800	KEMET
5	1	C5	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
6	1	C6	22 μF, 100 V, Electrolytic, Gen. Purpose, (8 x 11.5)	UPS2A220MPD1TD	Nichicon
7	1	C8	1 nF, ±10% ,300VAC, X1, Y1, Ceramic Capacitor B, Radial, Disc	DE1E3RA102MN4AP01F	Murata
8	1	C9	0.47 μF, ±10%,25 V, Ceramic Capacitor, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
9	3	C10 C15 C19	2.2 μF, ±10%, 50 V, Ceramic, X7R, 0805	UMK212BB7225KG-T	Taiyo Yuden
10	2	C11 C12	680 μF, ±20%, 35 V, Aluminum - Polymer Capacitors, Radial, Can, 18 mΩ, 2000 Hrs @ 105°C (10 x 18)	A750MW687M1VAAE018	KEMET
11	1	C13	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
12	2	C14 C17	2.2 μF, ±10%, 25 V, Ceramic, X7R, 0805	CL21B225KAFNFNE	Samsung
13	1	C16	4.7 μF, 10 V, Ceramic, X5R, 0805	C0805C475K8PACTU	Kemet
14	1	C18	2.2 μF, ±10%, 25 V, Ceramic Capacitor X7R, 0805	CL21B225KAFNFNE	Samsung
15	2	C20 C21	1 nF 100 V, Ceramic, X7R, 0402	GCM155R72A102KA37D	Murata
16	1	C22	1 μF, ±10%, 16 V, X5R, 0402	CL05A105KO5NNNC	Samsung
17	1	D1	800 V, 1 A, Fast Recovery, 250 ns, SMA	RS1K-13-F	Diodes, Inc.
18	1	D3	Diode, General Purpose, 400 V, 1 A, SMT SOD-123W	RS1GLW	Taiwan Semi
19	1	D4	Diode, 200 V, 200 mA, SMT SOD-323	BAV20WS-7-F	ON Semi
20	2	D5 D6	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
21	1	D7	LED, GREEN, 525 nm, 3.2 V, 20 mA,2 60.5 mcd, RECT, CLEAR, 0603	LTST-C194TGKT	Lite-On
22	1	F1	3.15 A, 250 V, Slow, RST	RST 3.15-BULK	Belfuse
23	1	L1	930 μH, 10%, Toroidal Common Mode Input Choke	32-00463-00	Power Integrations
24	1	L2	Custom, CMC, 18mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire	04291-T231	Sumida
25	1	L3	150 μH, 3.4 A, Vertical Toroidal	2114-V-RC	Bourns
26	1	Q1	NPN, 80 V 0.7 A, MEDIUM POWER, TO-243AA, SOT-89	2SCR514PHZGT100	Rohm Semi
27	2	Q2 Q3	MOSFET, N-CH, 120 V, 85 A (at VGS = 10 V), Trench Power AlphaSGT 120 V TM technology, DFN5X6	AONS62922	Alpha & Omega Semi
28	1	Q4	MOSFET, N-CH, 40 V, 100 A (Tc), 78 W (Tc), Surface Mount, 8DFN, 8-DFN (5x6)	AON6144	Alpha & Omega Semi
29	2	R1 R2	RES, 200 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2003V	Panasonic
30	2	R3 R4	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
31	2	R5 R6	RES, 402 kΩ, ±1%, 0.25W, 1/4W, Chip 1206 Thick Film	RC1206FR-07402KL	Rohm Semi
32	2	R7 R8	RES, 20 Ω, 1%, 1/2 W, Thin Film, 1206	RNCP1206FTD20R0	Stackpole
33	1	R9	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
34	1	R10	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
35	1	R11	RES, 4.64 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4641V	Panasonic
36	1	R12	RES, 51 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ510V	Panasonic
37	1	R13	RES, 300 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
38	2	R14 R15	4.99 Ω, ±1%, ¼ W Chip Resistor, 1206, Moisture Resistant, Thick Film	RC1206FR-074R99L	Yageo
39	1	R16	RES, 0.006 Ω, ±1%, 0.5W, 1/2W, 805, Current Sense, Thick Film, ±300ppm/°C, -55°C ~ 155°C	ERJ-6LWFR006V	Panasonic
40	1	R17	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic

41	4	R18 R19 R27 R28	RES, 4.70 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4701X	Panasonic
42	1	R20	RES, 2 kΩ, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J202V	Panasonic
43	1	R21	RES, 866 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8660V	Panasonic
44	4	R22 R24 R26 R29	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
45	2	R23 R25	RES, 470, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ471X	Panasonic
46	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SL10 2R505	Ametherm
47	1	RV1	300 VAC, 60 J, 10 mm, RADIAL	ERZ-V10D471	Panasonic
48	2	SW1 SW2	SWITCH TACTILE SPST-NO 0.05A 12V	EVQ-PE105K	Panasonic
49	1	T1	Custom, DER-1001 Flyback Transformer, ATQ27/18.4		Power Integrations
50	1	U1	CAPZero-2, SO-8C	CAP200DG	Power Integrations
51	1	U2	InnoSwitch5-Pro, InSOP-T28D	INN5376F-H901	Power Integrations
52	1	U3	IC, PIC, PIC®, XLP™, 16F Microcontroller IC, 8-Bit, 32 MHz, 14 KB (8K x 14,) FLASH 16-UQFN (4x4)	PIC16F18325-I/JQ	Microchip
53	1	VR1	TVS DIODE, 220 VWM, 356VC, SMB	SMBJ220A	Bourns
54	1	VR2	Zener Diode,15 V, ±2%, 350 mW, SMT SOD-523	BZT585B15T-7	Diodes, Inc.
55	1	VR3	Zener Diode, 62 V, 500 mW, ±2%, SMT SOD-123	MMSZ5265C-E3-08	Vishay
56	1	VR4	162 V Clamp, 3.7 A Ipp, Unidrirectional TVS Diode, SMT DO-214AA (SMBJ)	SMBJ100A	Littelfuse
57	3	J2 J4 J5	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-03-2021	Molex
58	1	J3	3 Position (1 x 3) header, 0.1 pitch, Vertical	22-28-4030	Molex
59	3	J2_1, J4_1 J5_1	Jumpers, 2 position, PHBR 15 AU, BLACK	382811-6	Amp/Tyco Elect.

6.2 Mechanical Parts

Item	Qty.	Ref Des	Description	Mfr. Part Number	Mfr.
1	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
2	1	TP2 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
4	1	J1	5 Position (1 x 5) Female header, 0.1 pitch, 00.126" (3.20 mm), Vertical, Au	PPPC051LFBN-RC	Sullins
5	1	J6	6 Position (1 x 6) header, 0.1 pitch, R/A Tin	22-05-2061	Molex
6	4	POST-CRKT_BRD_6-32_HEX1-POST-CRKT_BRD_6-32_HEX4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	27FTP00375A	Essentra

7 Transformer Specification (T1)

7.1 Electrical Diagram

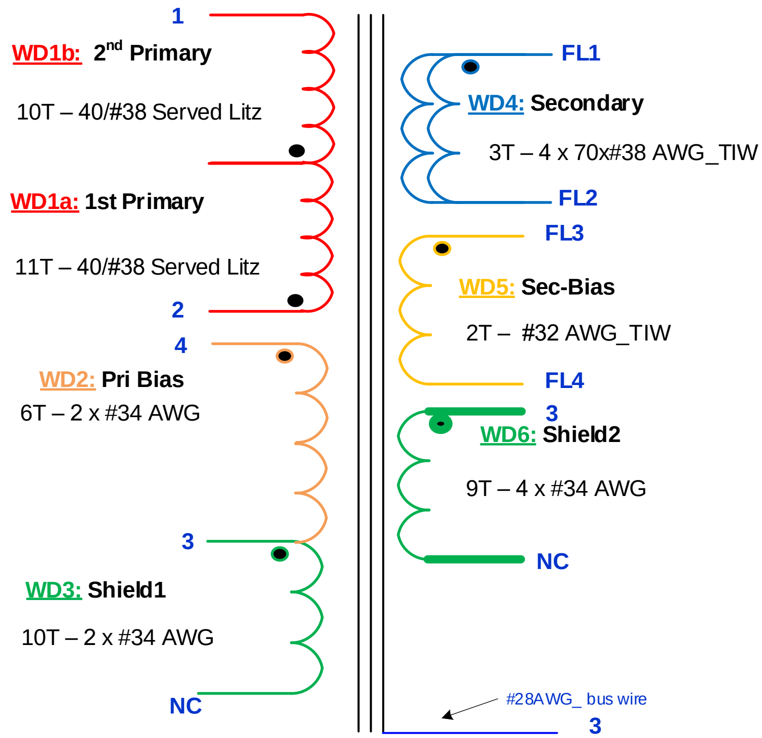


Figure 14 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	Across shorted primary windings (pins 1, 2, 3, 4) to shorted secondary windings (FL1, FL2, FL3, FL4) 60 secs, 60 Hz, 1 mA max	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 1.0 V test level.	296 μH ±5%
Resonant Frequency	Pins 1-2, all other open.	1000 kHz (Min.)
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	3.5 μH

7.3 Transformer Build Diagram

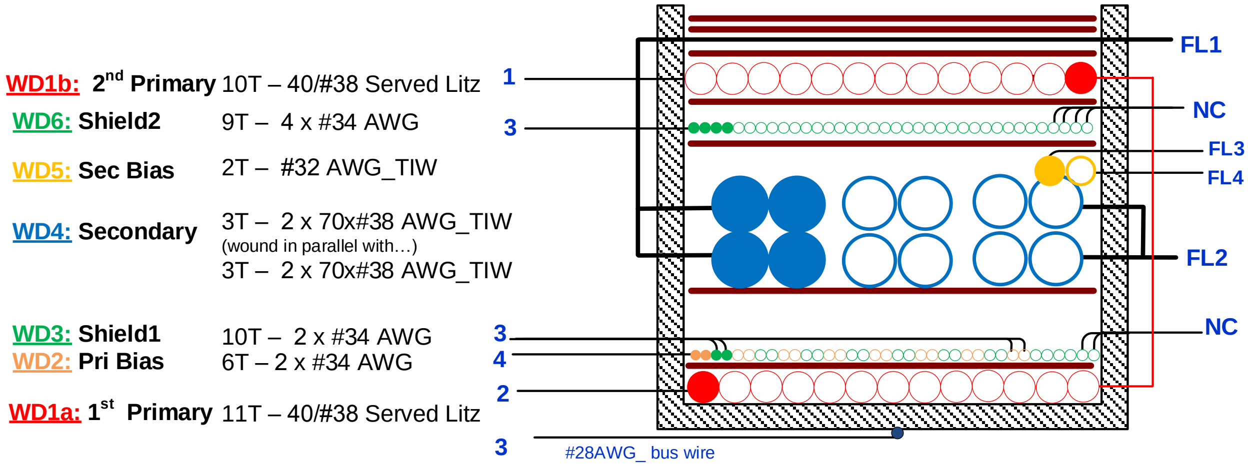
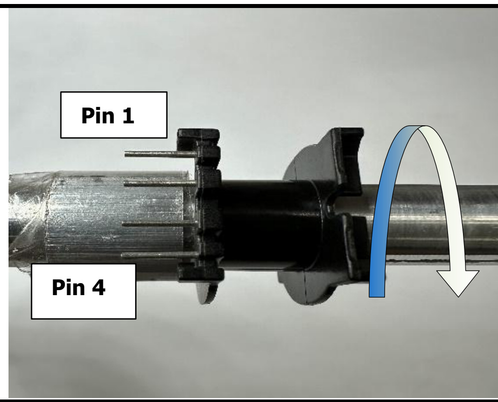
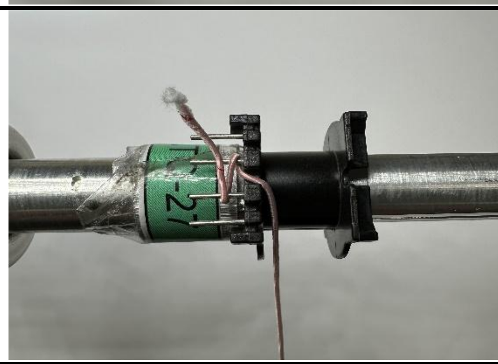
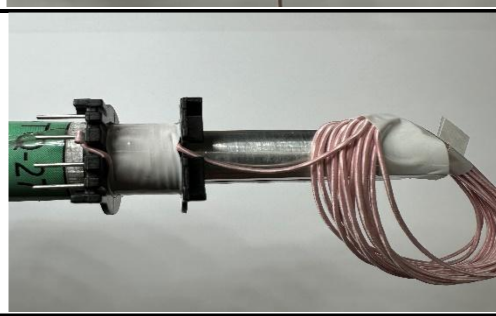
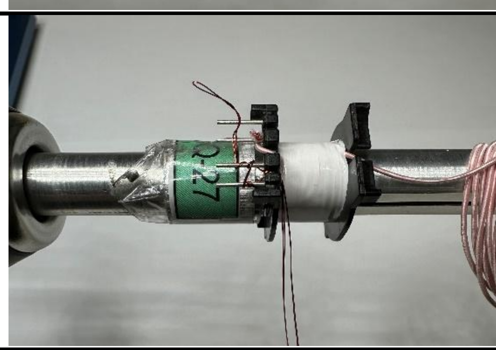


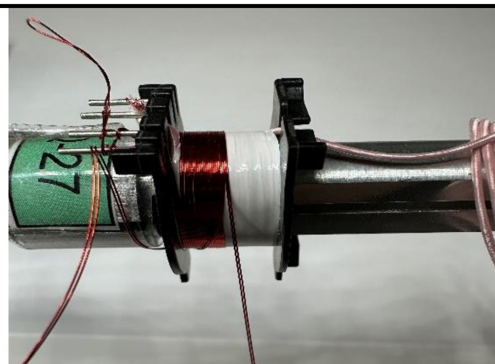
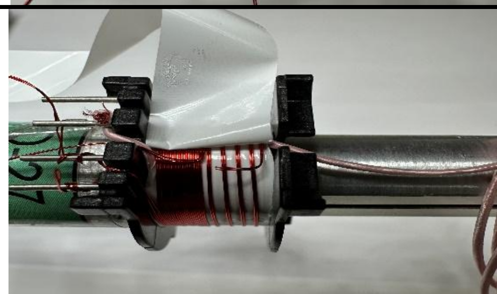
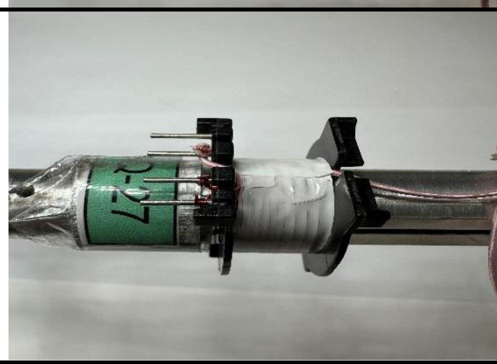
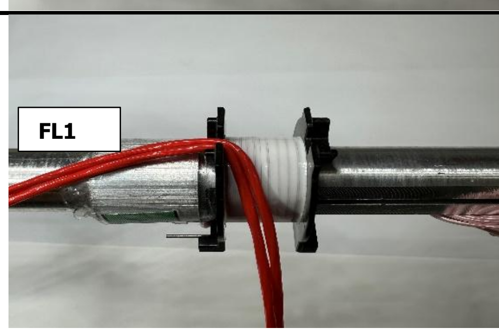
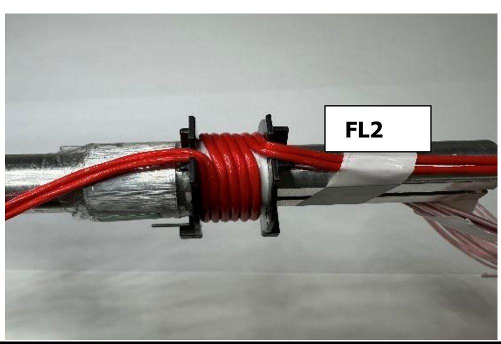
Figure 15 – Transformer Build Diagram.

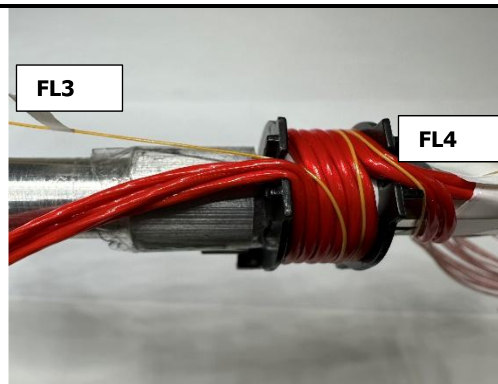
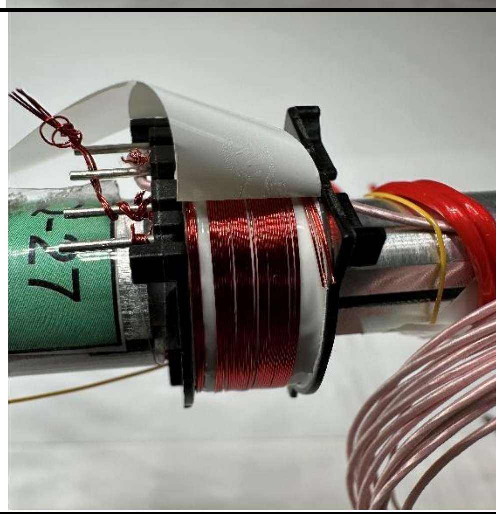
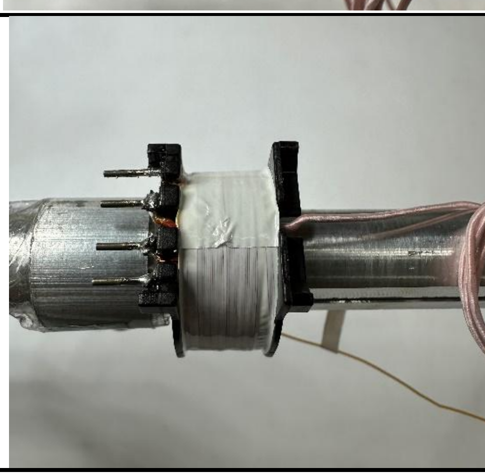
7.4 List of Materials

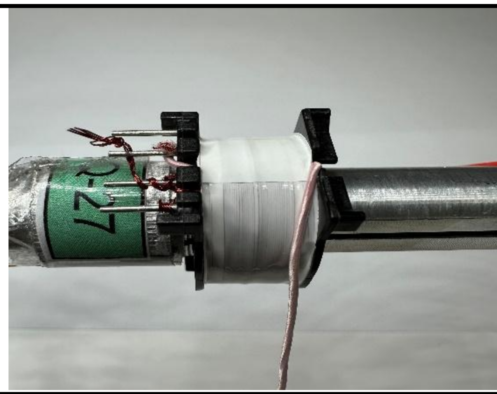
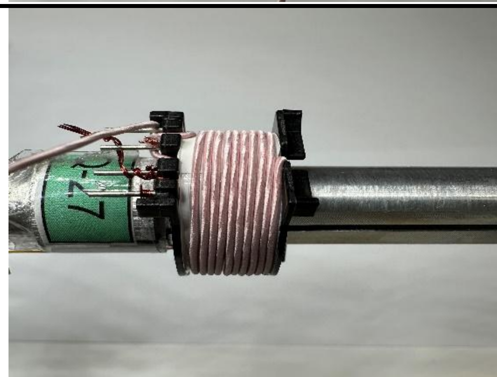
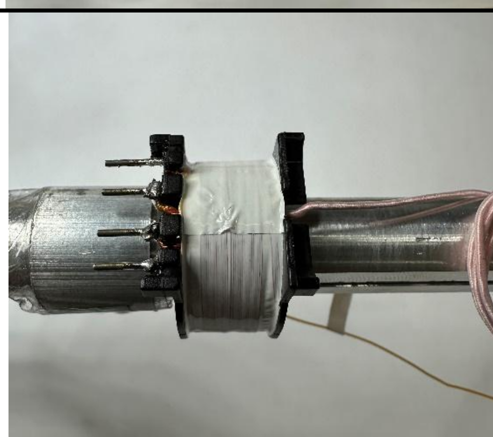
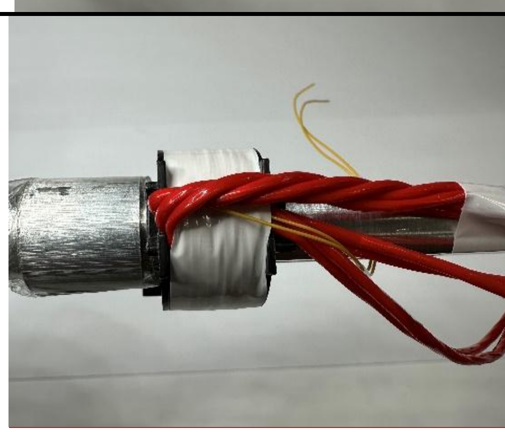
Item	Description
[1]	Core: ATQ27/18.4, Material 3C95. Hwahe.
[2]	Bobbin. ATQ27/18.4 - 4pins. PI#: 25-01178-00.
[3]	Served Litz Wire: #40/AWG#38
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: 70 x #38 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #32 AWG, Triple Insulated Wire.
[7]	Tape: 3M 1350F-1 Polyester Film, 1 mil Thick, 11.2 mm Wide.
[8]	Tape: 3M 1350F-1 Polyester Film, 1 mil Thick, 36 mm Wide.
[9]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper.
[10]	Glue: Loctite, 409, Gel, Mf #:40904; or Equivalent.
[11]	Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or Equivalent.
[12]	Varnish: Dolph BC-359; or Equivalent.

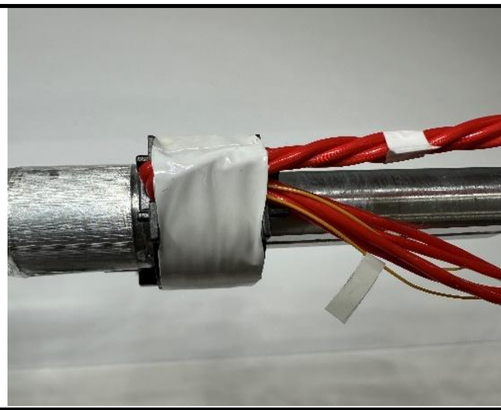
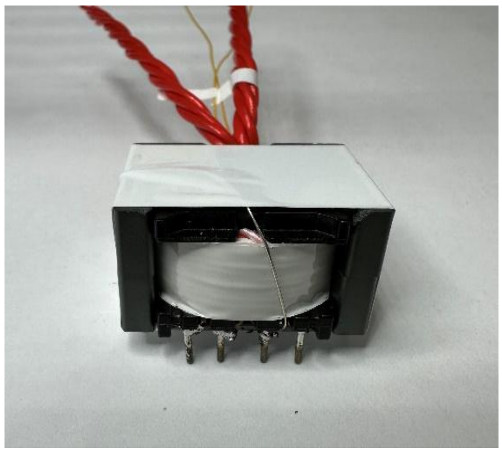
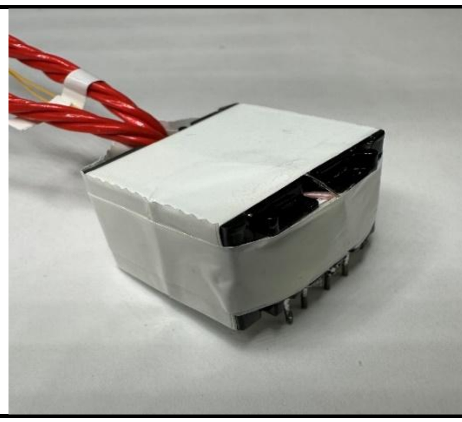
7.5 Transformer Illustrations

Winding Preparation		Position the bobbin Item [2] on the mandrel, pins facing on the left side of the winding machine. Winding direction is clockwise.
WD1a Primary 1		Start at pin 2, wind 11 turns of wire Item [3], from left to right in 1 layer. At the last turn leave enough length of wire-floating for WD1b-2nd Primary.
Insulation		1 layer of tape Item [7].
WD2: Bias & WD3: Shield1		Use 2 wires Item [4]. Start at pin 4 for Bias winding. Also use 2 wires of same Item [4] for WD3-Shield1 winding. Start at pin 3, winding left to right direction. Wind all 4 wires in parallel for 6 turns, then at the last turn terminate Bias winding at pin 3.

		
		Continue WD3 Shield1 winding for 4 turns more. Cut the wire at the last turn, leave at least 3 mm of excess to tuck it in the layer of tape.
Insulation		1 layer of tape Item [7].
WD4 Secondary	 	Switch to the other side of bobbin, WD4 Start from floating wire Item [5] marked FL1. Take 2 strands in parallel and wind 3 turns, from left to right. At the last, turn exit the wires at the right slot and mark it as FL2. Repeat the above process one more time on top of the secondary winding that was just wound.

WD5 Secondary Bias		Use triple insulated wire Item [6] and start from the left side (marked as FL3) and wind 2 turns to the right. At the last turn, exit the wire at the right slot, leave 2 inches of wire and mark it as FL4.
Insulation		1 layer of tape Item [7].
WD6 Shield 2		Start with 4 strands of wire Item [4] at pin 3 and wind 9 turns from left to right. At the last turn cut wires and leave wires straight down.
Insulation		1 layer of tape Item [7].

WD1b **2nd Primary**		Use the floating wire from WD1a-Primary 1, wind 10 turns from right to left. Terminate the wire at pin 1.
		
Insulation		1 layer of tape Item [7].
FL1 **Secondary Wires**		Fold the 4 strands of secondary winding start marked as FL1 and secondary bias winding start marked as FL3 to the right.

		Secure the folded wires with 2 layers of tape Item [7].
Finish		Gap the core halves to get 296 μH. Solder pin 3 with bus-wire Item [9] then lean along core halves and secure with tape. Apply Glue [10] between 2 core halves and Epoxy [11] between Bobbin and Core
Varnish & Complete Transformer		Varnish with Item [12]. Place 2 layers of tape Item [8] at the bottom of transformer and wrap up to cover secondary-side of transformer.

8 Common Mode Choke Specifications

8.1 930 µH Common Mode Choke (L1)

8.1.1 Electrical Diagram

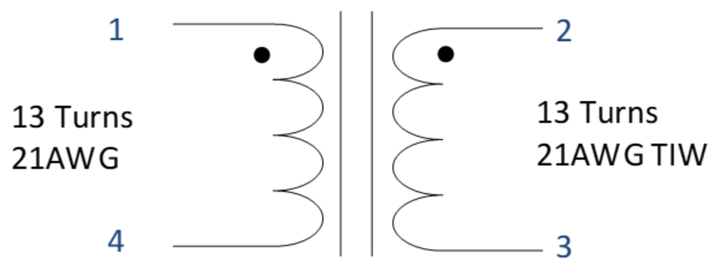


Figure 16 – Inductor Electrical Diagram.

8.1.2 Electrical Specifications

Inductance	1-4 or 2-3, measured at 100 kHz, 0.4 V_{RMS}	**930uH, ±10%**

8.1.3 List of Materials

Item	Description
[1]	Ferrite Core Toroid: EPCOS (TDK) T16-9.3-6.3.
[2]	Magnet Wire: #21 AWG, Double Coated.
[3]	Magnet Wire: #21 AWG, Triple Insulated Wire.

8.1.4 Winding Instructions

Wind 13 turns of Items [2] and [3] together as shown in the figure.	

9 Transformer Design Spreadsheet

9.1 100 W Design Spreadsheet

1	ACDC_InnoSwitch5-Pro_ SRZVS_Flyback_113023; Rev.0.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch5-Pro USB-PD Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			180	V	Minimum AC input voltage
5	VIN_MAX			265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Input voltage range
7	FLINE	50		50	Hz	AC Input voltage frequency
8	CAP_INPUT	180.0		180.0	uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	28.00		28.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	3.570		3.570	A	Output current 1
13	POUT1			100.00	W	Output power 1
14	EFFICIENCY1	0.94		0.94		Converter efficiency for output 1
15	Z_FACTOR1	0.65		0.65		Z-factor for output 1
16	TYPE	PDO		PDO		The voltage entered is a standard PDO(Power Delivery Object)
18	**SET-POINT 2**					
19	VOUT2	20.00		20.00	V	Output voltage 2
20	IOUT2	5.000		5.000	A	Output current 2
21	POUT2			100.00	W	Output power 2
22	EFFICIENCY2	0.93		0.93		Converter efficiency for output 2
23	Z_FACTOR2	0.65		0.65		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
26	**SET-POINT 3**					
27	VOUT3	15.00		15.00	V	Output voltage 3
28	IOUT3	5.000		5.000	A	Output current 3
29	POUT3			75.00	W	Output power 3
30	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
31	Z_FACTOR3	0.65		0.65		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
34	**SET-POINT 4**					
35	VOUT4	9.00		9.00	V	Output voltage 4
36	IOUT4	5.000		5.000	A	Output current 4
37	POUT4			45.00	W	Output power 4
38	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
39	Z_FACTOR4	0.65		0.65		Z-factor for output 4
40	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
42	**SET-POINT 5**					
43	VOUT5	5.00		5.00	V	Output voltage 5
44	IOUT5	5.000		5.000	A	Output current 5
45	POUT5			25.00	W	Output power 5
46	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
47	Z_FACTOR5	0.65		0.65		Z-factor for output 5
48	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)

91	**PRIMARY CONTROLLER SELECTION**					
92	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
93	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
94	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
95	DEVICE_GENERIC	INN5376F		INN5376F		Generic device code
96	DEVICE_CODE			INN5376F		Device code
97	PDEVICE_MAX			125	W	Device maximum power capability
98	RDSON_100DEG			0.35	Ω	Primary switch on-time resistance at 100°C
99	ILIMIT_MIN			2.697	A	Primary switch minimum current limit
100	ILIMIT_TYP			2.900	A	Primary switch typical current limit
101	ILIMIT_MAX			3.103	A	Primary switch maximum current limit
102	VDRAIN_ON_PRSW			0.17	V	Primary switch on-time voltage drop
103	VDRAIN_OFF_PRSW			684.3	V	Peak drain voltage on the primary switch during turn-off
107	**WORST CASE ELECTRICAL PARAMETERS**					
108	FSWITCHING_MAX	102130	Info	102130	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
109	VOR	196.0		196.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
110	VMIN			218.78	V	Valley of the rectified minimum input AC voltage at full load
111	KP			1.192		Measure of continuous/discontinuous mode of operation
112	MODE_OPERATION			DCM		Mode of operation
113	DUTYCYCLE			0.358		Primary switch duty cycle
114	TIME_ON			4.27	us	Primary switch on-time
115	TIME_OFF			6.32	us	Primary switch off-time
116	LPRIMARY_MIN			281.1	uH	Minimum primary magnetizing inductance
117	LPRIMARY_TYP			295.9	uH	Typical primary magnetizing inductance
118	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
119	LPRIMARY_MAX			310.7	uH	Maximum primary magnetizing inductance
121	**PRIMARY CURRENT**					
122	IAVG_PRIMARY			0.480	A	Primary switch average current
123	IPEAK_PRIMARY			3.035	A	Primary switch peak current
124	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
125	IRIPPLE_PRIMARY			3.035	A	Primary switch ripple current
126	IRMS_PRIMARY			0.985	A	Primary switch RMS current
128	**SECONDARY CURRENT**					
129	IPEAK_SECONDARY			21.242	A	Secondary winding peak current
130	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
131	IRMS_SECONDARY			8.612	A	Secondary winding RMS current
132	IRIPPLE_CAP_OUT			7.012	A	Output capacitor ripple current
136	**TRANSFORMER CONSTRUCTION PARAMETERS**					
137	**CORE SELECTION**					
138	CORE	CUSTOM		CUSTOM		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
139	CORE NAME	ATQ27/18.4		ATQ27/18.4		Core code
140	AE	126.0		126.0	mm^2	Core cross sectional area
141	LE	51.2		51.2	mm	Core magnetic path length
142	AL	6037		6037	nH	Ungapped core effective inductance per turns squared
143	VE	6453		6453	mm^3	Core volume
144	BOBBIN NAME	ATQ27/18.4		ATQ27/18.4		Bobbin name
145	AW	56.2		56.2	mm^2	Bobbin window area
146	BW	10.40		10.40	mm	Bobbin width
147	MARGIN			0.0	mm	Bobbin safety margin
149	**PRIMARY WINDING**					
150	NPRIMARY			21		Primary winding number of turns
151	BPEAK			3799	Gauss	Peak flux density
152	BMAX			3527	Gauss	Maximum flux density

153	BAC			1764	Gauss	AC flux density (0.5 x Peak to Peak)
154	ALG			671	nH	Typical gapped core effective inductance per turns squared
155	LG			0.210	mm	Core gap length
157	**PRIMARY BIAS WINDING**					
158	NBIAS_PRIMARY			6		Primary bias winding number of turns
160	**SECONDARY WINDING**					
161	NSECONDARY	3		3		Secondary winding number of turns
163	**SECONDARY BIAS WINDING**					
164	NBIAS_SECONDARY			2		Secondary bias winding number of turns
168	**PRIMARY COMPONENTS SELECTION**					
169	RCD CLAMP					
170	LLEAK			2.96	uH	Primary winding leakage inductance
171	CSWNODE			15.00	pF	Primary switching node capacitance (InnoSwitch Coss + Transformer lumped winding capacitance)
172	CCLAMP			1.17	nF	Primary clamp capacitor
173	RCLAMP			83.96	kΩ	Primary Clamp Resistor
175	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
176	BROWN-IN REQURED	70.00		70.00	V	Required AC RMS/DC line brown-in threshold
177	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
178	BROWN-IN ACTUAL			59V – 71.4V	V	Actual AC RMS/DC brown-in threshold using standard resistors
179	BROWN-OUT ACTUAL			52.5V -65V	V	Actual AC RMS/DC brown-out threshold using standard resistors
180	OVERVOLTAGE_LINE			265.6V - 301.5V	V	Actual AC RMS/DC line over-voltage threshold
182	**PRIMARY BIAS WINDING**					
183	VBIAS_PRIMARY			9.00	V	Rectified primary bias voltage at the cable-disconnect (5V) set-point
184	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
185	VREVERSE_BIASDIODE_PRIMARY			162.68	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
186	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
187	CBPP			0.47	uF	BPP pin capacitor
191	**SECONDARY COMPONENTS SELECTION**					
192	**RECTIFIER**					
193	VDRAIN_OFF_SRFET			81.34	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
194	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
195	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
196	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
198	**SECONDARY BIAS WINDING**					
199	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
200	VBIAS_SECONDARY			9.00	V	Rectified secondary bias voltage at full load
201	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
202	VREVERSE_BIASDIODE_SECONDARY			44.56	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
203	CBIAS_SECONDARY			2.20	uF	Secondary bias winding rectification capacitor
204	CBPS			2.20	uF	BPS pin capacitor

9.2 65 W Design Spreadsheet

1	ACDC_InnoSwitch5-Pro_ SRZVS_Flyback_113023; Rev.0.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch5-Pro USB-PD Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN			90	V	Minimum AC input voltage
5	VIN_MAX			180	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Input voltage range
7	FLINE	50		50	Hz	AC Input voltage frequency
8	CAP_INPUT	180.0		180.0	uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	28.00		28.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	2.320		2.320	A	Output current 1
13	POUT1			65.00	W	Output power 1
14	EFFICIENCY1	0.94		0.94		Converter efficiency for output 1
15	Z_FACTOR1	0.65		0.65		Z-factor for output 1
16	TYPE	PDO		PDO		The voltage entered is a standard PDO(Power Delivery Object)
18	**SET-POINT 2**					
19	VOUT2	20.00		20.00	V	Output voltage 2
20	IOUT2	3.250		3.250	A	Output current 2
21	POUT2			65.00	W	Output power 2
22	EFFICIENCY2	0.93		0.93		Converter efficiency for output 2
23	Z_FACTOR2	0.65		0.65		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
26	**SET-POINT 3**					
27	VOUT3	15.00		15.00	V	Output voltage 3
28	IOUT3	3.250		3.250	A	Output current 3
29	POUT3			48.75	W	Output power 3
30	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
31	Z_FACTOR3	0.65		0.65		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
34	**SET-POINT 4**					
35	VOUT4	9.00		9.00	V	Output voltage 4
36	IOUT4	3.250		3.250	A	Output current 4
37	POUT4			29.25	W	Output power 4
38	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
39	Z_FACTOR4	0.65		0.65		Z-factor for output 4
40	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
42	**SET-POINT 5**					
43	VOUT5	5.00		5.00	V	Output voltage 5
44	IOUT5	3.250		3.250	A	Output current 5
45	POUT5			16.25	W	Output power 5
46	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
47	Z_FACTOR5	0.65		0.65		Z-factor for output 5
48	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
91	**PRIMARY CONTROLLER SELECTION**					
92	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
93	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode

94	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
95	DEVICE_GENERIC	INN5376F		INN5376F		Generic device code
96	DEVICE_CODE			INN5376F		Device code
97	PDEVICE_MAX			125	W	Device maximum power capability
98	RDSON_100DEG			0.35	Ω	Primary switch on-time resistance at 100°C
99	ILIMIT_MIN			2.697	A	Primary switch minimum current limit
100	ILIMIT_TYP			2.900	A	Primary switch typical current limit
101	ILIMIT_MAX			3.103	A	Primary switch maximum current limit
102	VDRAIN_ON_PRSW			0.17	V	Primary switch on-time voltage drop
103	VDRAIN_OFF_PRSW			549.9	V	Peak drain voltage on the primary switch during turn-off
107	**WORST CASE ELECTRICAL PARAMETERS**					
108	FSWITCHING_MAX	71917	Info	71917	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
109	VOR	196.0		196.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
110	VMIN			100.53	V	Valley of the rectified minimum input AC voltage at full load
111	KP			1.243		Measure of continuous/discontinuous mode of operation
112	MODE_OPERATION			DCM		Mode of operation
113	DUTYCYCLE			0.529		Primary switch duty cycle
114	TIME_ON			8.83	us	Primary switch on-time
115	TIME_OFF			6.63	us	Primary switch off-time
116	LPRIMARY_MIN			281.1	uH	Minimum primary magnetizing inductance
117	LPRIMARY_TYP			295.9	uH	Typical primary magnetizing inductance
118	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
119	LPRIMARY_MAX			310.7	uH	Maximum primary magnetizing inductance
121	**PRIMARY CURRENT**					
122	IAVG_PRIMARY			0.680	A	Primary switch average current
123	IPEAK_PRIMARY			2.890	A	Primary switch peak current
124	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
125	IRIPPLE_PRIMARY			2.890	A	Primary switch ripple current
126	IRMS_PRIMARY			1.144	A	Primary switch RMS current
128	**SECONDARY CURRENT**					
129	IPEAK_SECONDARY			20.229	A	Secondary winding peak current
130	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
131	IRMS_SECONDARY			6.776	A	Secondary winding RMS current
132	IRIPPLE_CAP_OUT			5.945	A	Output capacitor ripple current
136	**TRANSFORMER CONSTRUCTION PARAMETERS**					
137	**CORE SELECTION**					
138	CORE	CUSTOM		CUSTOM		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
139	CORE NAME	ATQ27/18.4		ATQ27/18.4		Core code
140	AE	126.0		126.0	mm^2	Core cross sectional area
141	LE	51.2		51.2	mm	Core magnetic path length
142	AL	6037		6037	nH	Ungapped core effective inductance per turns squared
143	VE	6453		6453	mm^3	Core volume
144	BOBBIN NAME	ATQ27/18.4		ATQ27/18.4		Bobbin name
145	AW	56.2		56.2	mm^2	Bobbin window area
146	BW	10.40		10.40	mm	Bobbin width
147	MARGIN			0.0	mm	Bobbin safety margin
149	**PRIMARY WINDING**					
150	NPRIMARY			21		Primary winding number of turns
151	BPEAK			3800	Gauss	Peak flux density
152	BMAX			3348	Gauss	Maximum flux density
153	BAC			1674	Gauss	AC flux density (0.5 x Peak to Peak)
154	ALG			671	nH	Typical gapped core effective inductance per turns squared
155	LG			0.210	mm	Core gap length

157	**PRIMARY BIAS WINDING**					
158	NBIAS_PRIMARY			6		Primary bias winding number of turns
160	**SECONDARY WINDING**					
161	NSECONDARY	3		3		Secondary winding number of turns
163	**SECONDARY BIAS WINDING**					
164	NBIAS_SECONDARY			2		Secondary bias winding number of turns
168	**PRIMARY COMPONENTS SELECTION**					
169	RCD CLAMP					
170	LLEAK			2.96	uH	Primary winding leakage inductance
171	CSWNODE			15.00	pF	Primary switching node capacitance (InnoSwitch Coss + Transformer lumped winding capacitance)
172	CCLAMP			1.06	nF	Primary clamp capacitor
173	RCLAMP			131.47	kΩ	Primary Clamp Resistor
175	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
176	BROWN-IN REQURED			70.00	V	Required AC RMS/DC line brown-in threshold
177	RLS			3.56	MΩ	Connect two 3.4 MOhm resistors to the V-pin for the required UV/OV threshold
178	BROWN-IN ACTUAL			59V – 71.4V	V	Actual AC RMS/DC brown-in threshold using standard resistors
179	BROWN-OUT ACTUAL			52.5V -65V	V	Actual AC RMS/DC brown-out threshold using standard resistors
180	OVERVOLTAGE_LINE			265.6V - 301.5V	V	Actual AC RMS/DC line over-voltage threshold
182	**PRIMARY BIAS WINDING**					
183	VBIAS_PRIMARY			9.00	V	Rectified primary bias voltage at the cable-disconnect (5V) set-point
184	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
185	VREVERSE_BIASDIODE_PRIMARY			124.29	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
186	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
187	CBPP			0.47	uF	BPP pin capacitor
191	**SECONDARY COMPONENTS SELECTION**					
192	**RECTIFIER**					
193	VDRAIN_OFF_SRFET			62.15	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
194	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
195	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
196	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
198	**SECONDARY BIAS WINDING**					
199	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
200	VBIAS_SECONDARY			9.00	V	Rectified secondary bias voltage at full load
201	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
202	VREVERSE_BIASDIODE_SECONDARY			31.76	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
203	CBIAS_SECONDARY			2.20	uF	Secondary bias winding rectification capacitor
204	CBPS			2.20	uF	BPS pin capacitor

10 Performance Data

Note 1: Output voltages measured on the board.
2: Measurements taken at room temperature (approximately 24 °C)

10.1 No-Load Input Power at 5 V_{OUT} (Low Power Mode Enabled)

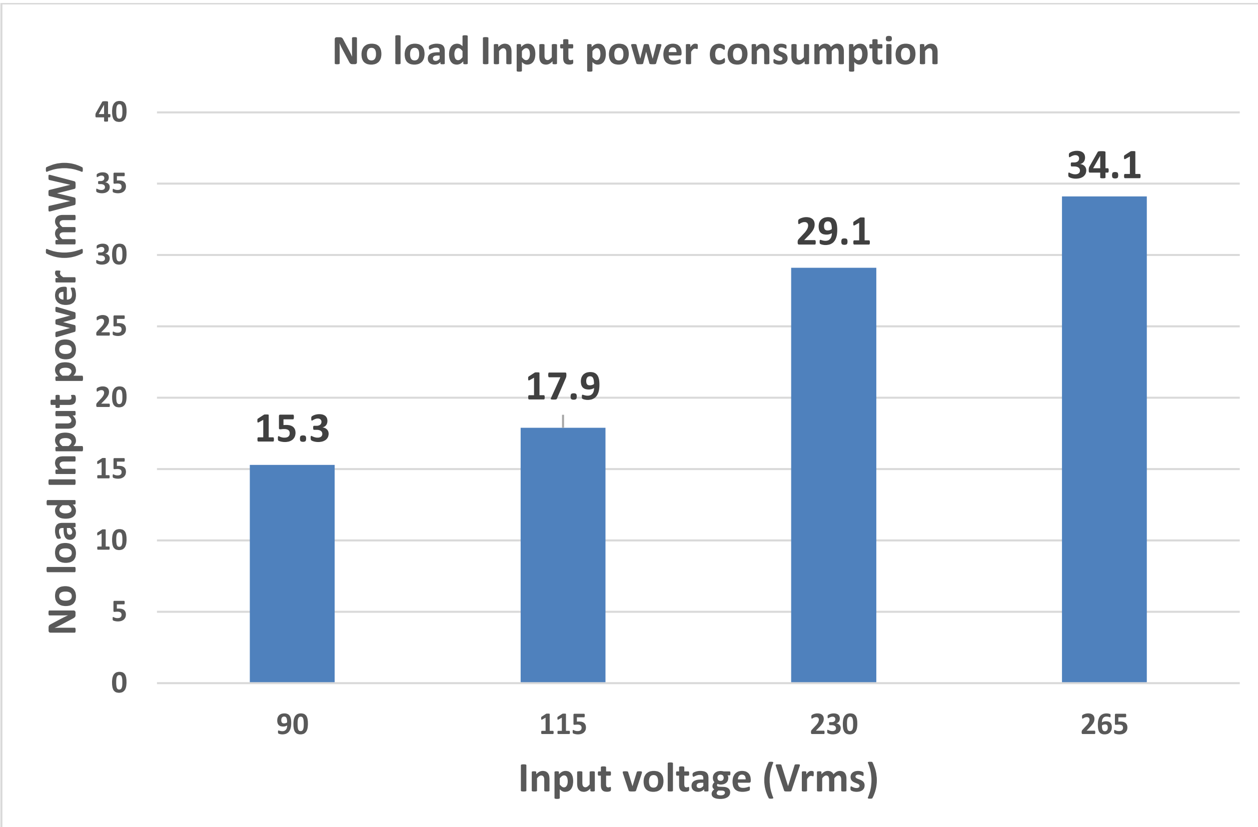


Figure 17 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.2 Efficiency Across Line (on Board)

10.2.1 100 W Rated Power (High Line Input)

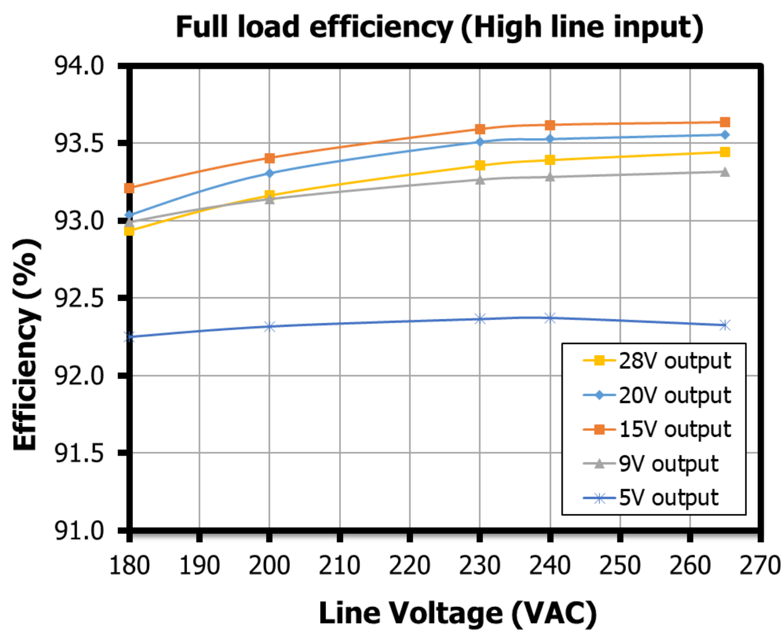


Figure 18 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, 20 V and 28 V Output with High Line Input, Room Temperature.

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			180 VAC	200 VAC	230 VAC	265 VAC
5	5	25	92.3	92.3	92.4	92.3
9	5	45	93.0	93.1	93.3	93.3
15	5	75	93.2	93.4	93.6	93.6
20	5	100	93.0	93.3	93.5	93.6
28	3.57	100	92.9	93.2	93.4	93.4

10.2.2 65 W Rated Power (Low Line Input)

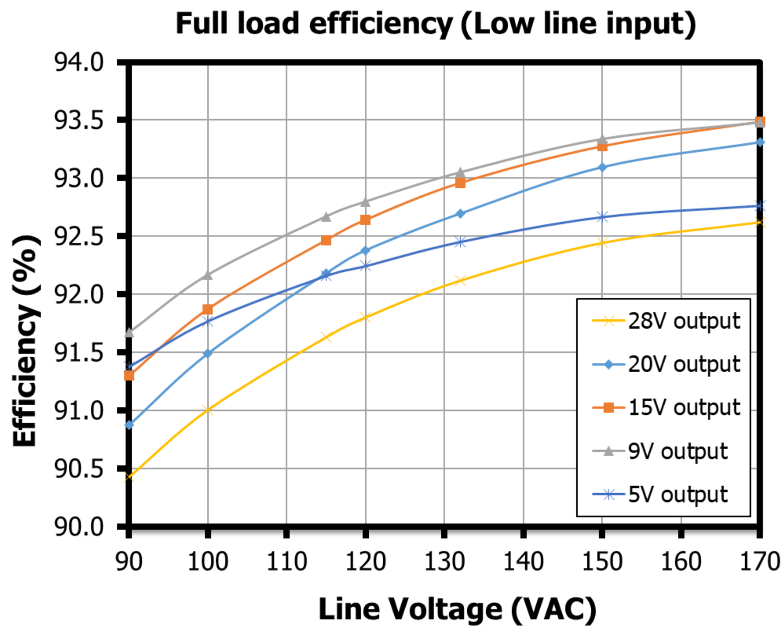


Figure 19 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, 20 V and 28 V Output with Low Line Input, Room Temperature.

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	150 VAC	170 VAC
5	3.25	16.3	91.4	92.2	92.7	92.8
9	3.25	29.3	91.7	92.7	93.3	93.5
15	3.25	48.8	91.3	92.5	93.3	93.5
20	3.25	65	90.9	92.2	93.1	93.3
28	2.32	65	90.4	91.6	92.4	92.6

10.3 Average and 10% Load Efficiency (on Board)

10.3.1 Efficiency Requirements

V_{OUT} (V)	Model (V)	Test Effective Power (W)	Average 2016 New EISA2007	Average Jan-16 CoC v5 Tier 2	10% Load Jan-16 CoC v5 Tier 2
5	<6	25	81.4%	81.8%	72.5%
9	>6	45	86.6 %	87.3%	77.3%
15	>6	75	87.7%	88.9%	78.9%
20	>6	100	88.0%	89.0%	79.0%
28	>6	100	88.0%	89.0%	79.0%

10.3.2 Efficiency Performance Summary (on Board)

V_{OUT} (V)	Current (A)	Average Efficiency (%)		10% Load Efficiency (%)	
		230 VAC	265 VAC	230 VAC	265 VAC
5	5	92.6	92.5	90.9	90.0
9	5	93.5	93.4	91.3	90.7
15	5	93.7	93.7	91.3	90.9
20	5	93.5	93.5	90.7	90.4
28	3.57	92.8	92.8	87.4	87.1

V_{OUT} (V)	Current (A)	Average Efficiency (%)		10% Load Efficiency (%)	
		90 VAC	115 VAC	90 VAC	115 VAC
5	3.25	91.9	92.5	91.4	91.4
9	3.25	92.2	93.0	91.3	91.5
15	3.25	91.8	92.7	90.0	90.3
20	3.25	91.4	92.3	88.9	89.3
28	2.32	90.2	91.1	83.9	84.2

10.3.3 Average and 10% Load Efficiency at 230 VAC (on Board)

10.3.3.1 Output: 5 V / 5 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	5.00	5.00	92.4	**92.6**
75	4.99	3.75	92.8	
50	5.00	2.49	92.9	
25	5.01	1.24	92.4	
10	5.02	0.49	**90.9**	

10.3.3.2 Output: 9 V / 5 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	9.01	5.00	93.3	**93.5**
75	9.03	3.75	93.6	
50	9.04	2.49	93.7	
25	9.05	1.24	93.3	
10	9.06	0.49	**91.3**	

10.3.3.3 Output: 15 V / 5 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.0	5.00	93.6	**93.7**
75	15.1	3.75	93.8	
50	15.1	2.49	93.8	
25	15.1	1.24	93.4	
10	15.1	0.49	**91.3**	

10.3.3.4 Output: 20 V / 5 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	20.1	5.00	93.5	**93.5**
75	20.1	3.75	93.7	
50	20.1	2.49	93.6	
25	20.1	1.24	93.2	
10	20.1	0.49	**90.7**	

10.3.3.5 Output: 28 V / 3.57 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	28.0	3.57	93.3	**92.8**
75	28.0	2.67	93.3	
50	28.0	1.78	92.9	
25	28.0	0.88	91.7	
10	28.0	0.34	**87.4**	

10.3.4 Average and 10% Load Efficiency at 115 VAC (on Board)

10.3.4.1 Output: 5 V / 3.25 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	4.98	3.24	92.1	**92.5**
75	5.00	2.43	92.5	
50	5.01	1.62	92.8	
25	5.02	0.81	92.6	
10	5.02	0.31	**91.4**	

10.3.4.2 Output: 9 V / 3.25 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	9.03	3.24	92.6	**93.0**
75	9.04	2.43	93.0	
50	9.05	1.62	93.3	
25	9.06	0.81	93.1	
10	9.06	0.31	**91.5**	

10.3.4.3 Output: 15 V / 3.25 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.1	3.24	92.5	**92.7**
75	15.1	2.43	92.8	
50	15.1	1.62	93.0	
25	15.1	0.81	92.5	
10	15.1	0.31	**90.3**	

10.3.4.4 Output: 20 V / 3.25 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	20.1	3.24	92.2	**92.3**
75	20.1	2.43	92.4	
50	20.1	1.62	92.5	
25	20.1	0.81	92.1	
10	20.1	0.31	**89.3**	

10.3.4.5 Output: 28 V / 2.32 A

Load (%)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	28.1	2.31	91.6	**91.1**
75	28.1	1.74	91.6	
50	28.1	1.15	91.3	
25	28.1	0.57	89.7	
10	28.1	0.22	**84.2**	

10.4 Line Regulation (on Board)

Note: Cable Drop Compensation (CDC) used for all output voltage conditions = 0 mV

10.4.1 Output: 5 V / 5 A (High Line Input)

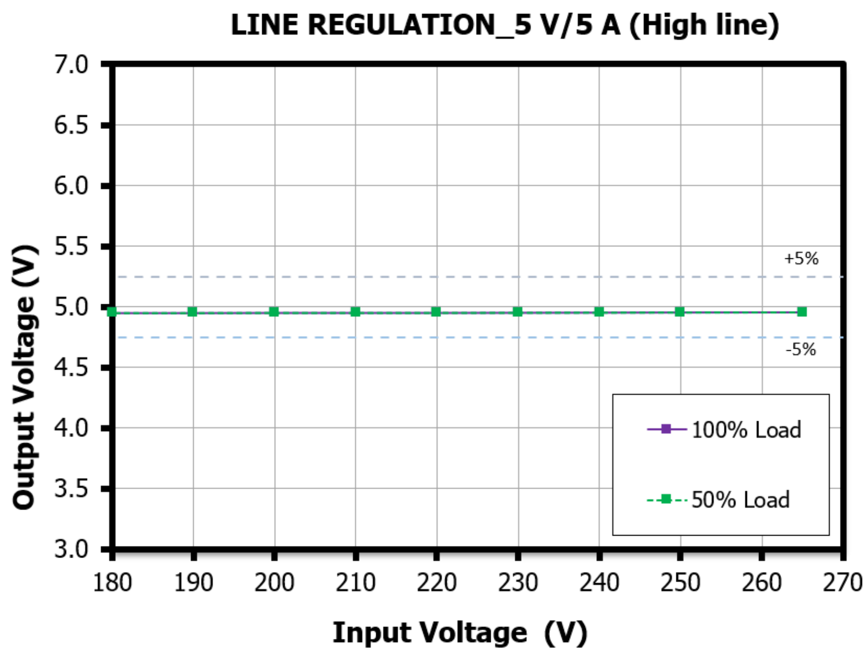


Figure 20 – Output Voltage vs. Input Line Voltage (High Line) for 5 V Output, Room Temperature.

10.4.2 Output: 20 V / 5 A (High Line Input)

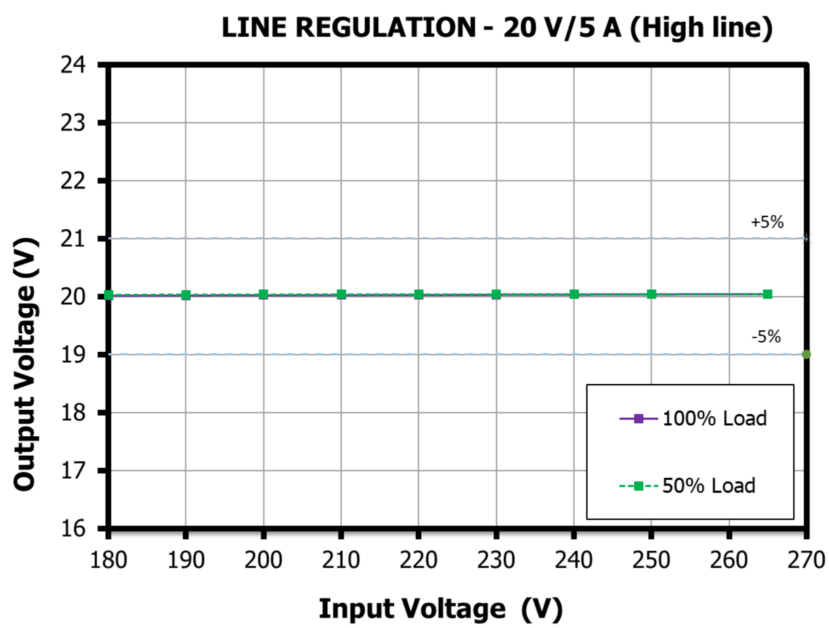


Figure 21 – Output Voltage vs. Input Line Voltage (High Line) for 20 V Output, Room Temperature.

10.4.3 Output: 28 V / 3.57 A (High Line Input)

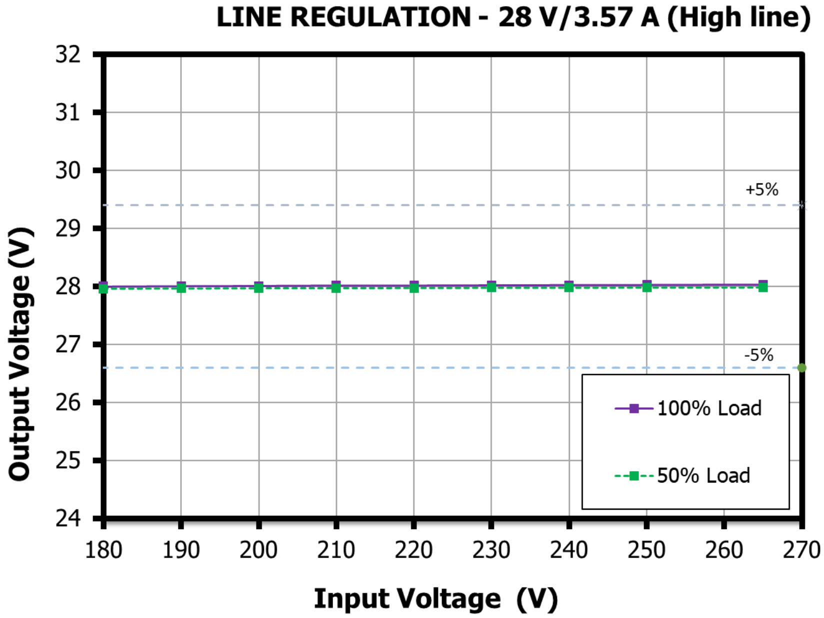


Figure 22 - Output Voltage vs. Input Line Voltage (High Line) for 28 V Output, Room Temperature.

10.4.4 Output: 5 V / 3.25 A (Low Line Input)

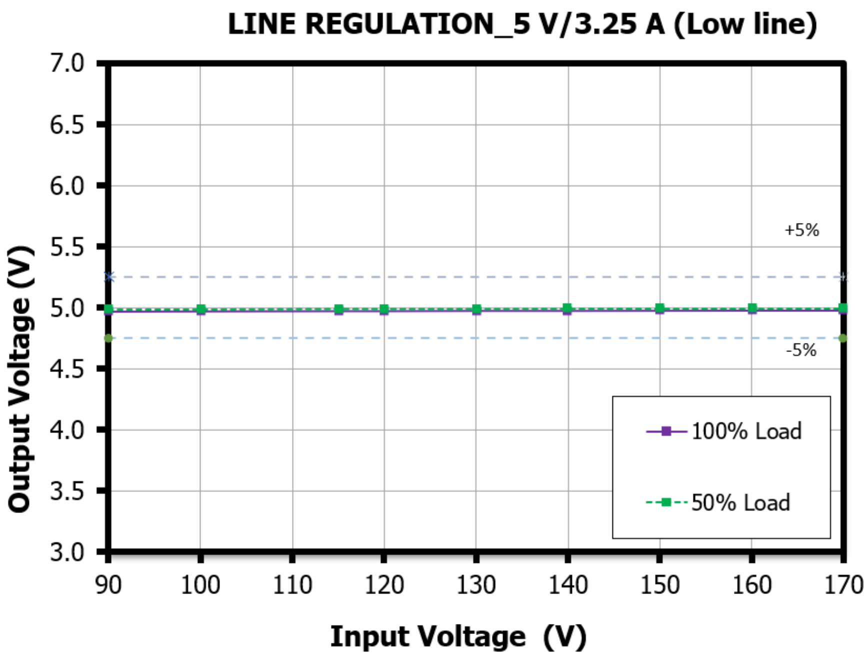


Figure 23 - Output Voltage vs. Input Line Voltage (Low Line) for 5 V Output, Room Temperature.

10.4.5 Output: 20 V / 3.25 A (Low Line Input)

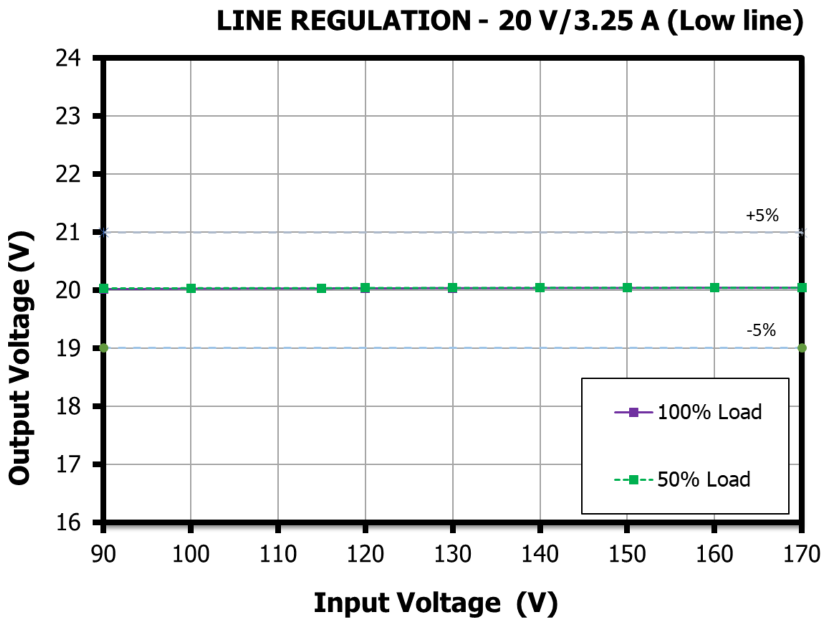


Figure 24 – Output Voltage vs. Input Line Voltage (Low Line) for 20 V Output, Room Temperature.

10.4.6 Output: 28 V / 2.32 A (Low Line Input)

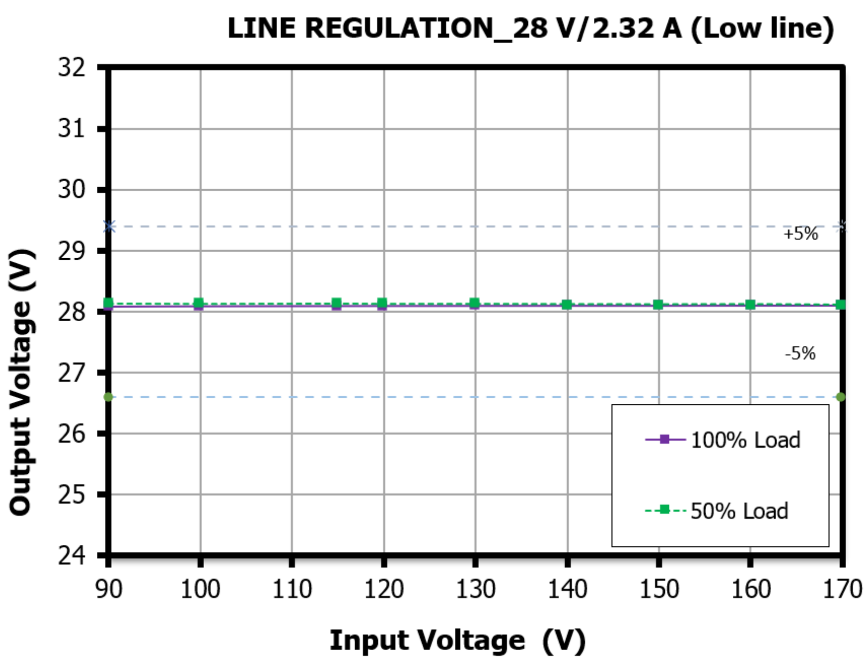


Figure 25 – Output Voltage vs. Input Line Voltage (Low Line) for 28 V Output, Room Temperature.

10.5 Load Regulation (on Board)

Note: In this design, CDC was set to 0 mV. CDC setting can be adjusted via the I^{2}C interface to match performance requirements for applications such as USB PD specifications for acceptable voltage range of 5 V operation, vSafe5V (4.75 V to 5.5 V, measured on-board).

10.5.1 100W rated power, High Line Input

10.5.1.1 Output: 5 V / 5 A

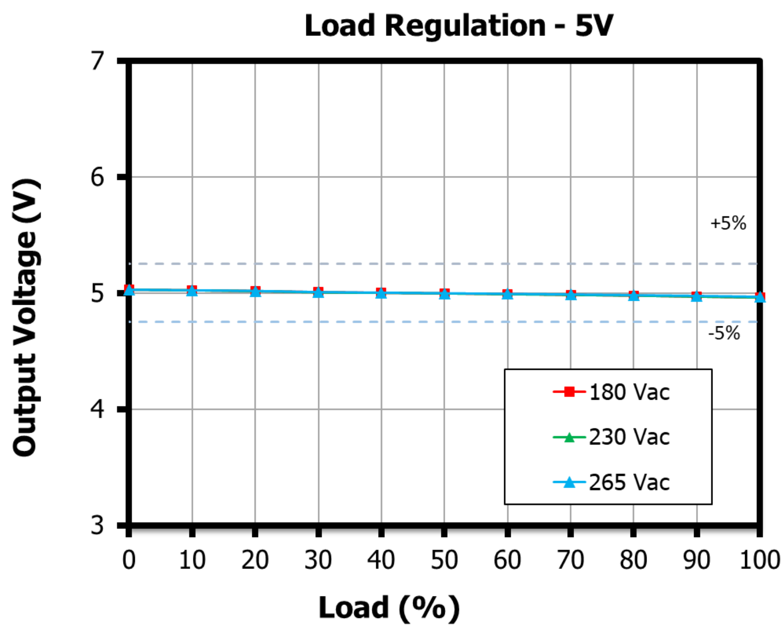


Figure 26 – Output Voltage vs. Load for 5 V Output, Room Temperature.

10.5.1.2 Output: 9 V / 5 A

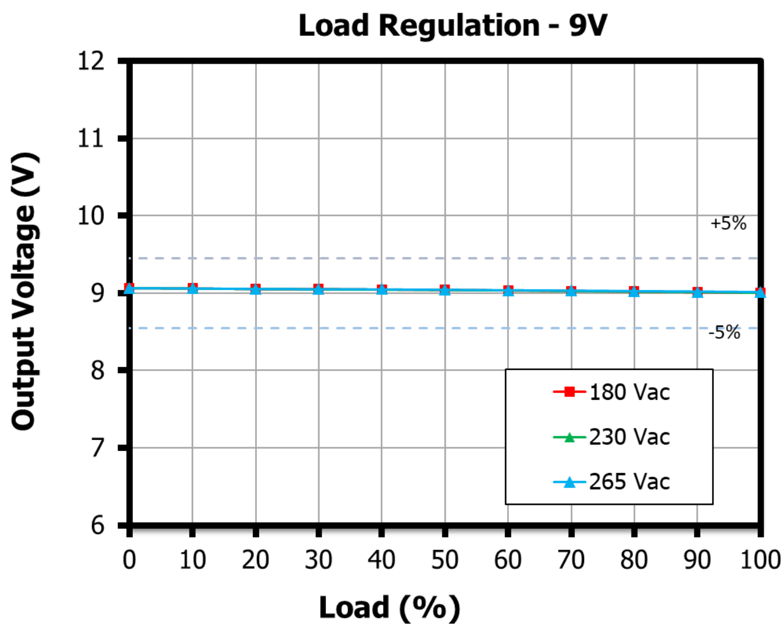


Figure 27 – Output Voltage vs. Load for 9 V Output, Room Temperature.

10.5.1.3 Output: 15 V / 5 A

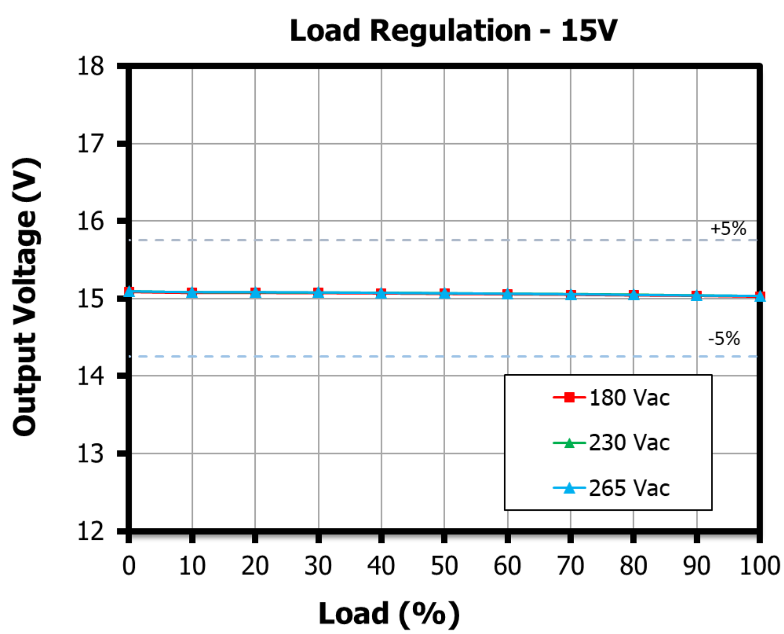


Figure 28 – Output Voltage vs. Load for 15 V Output, Room Temperature.

10.5.1.4 Output: 20 V / 5 A

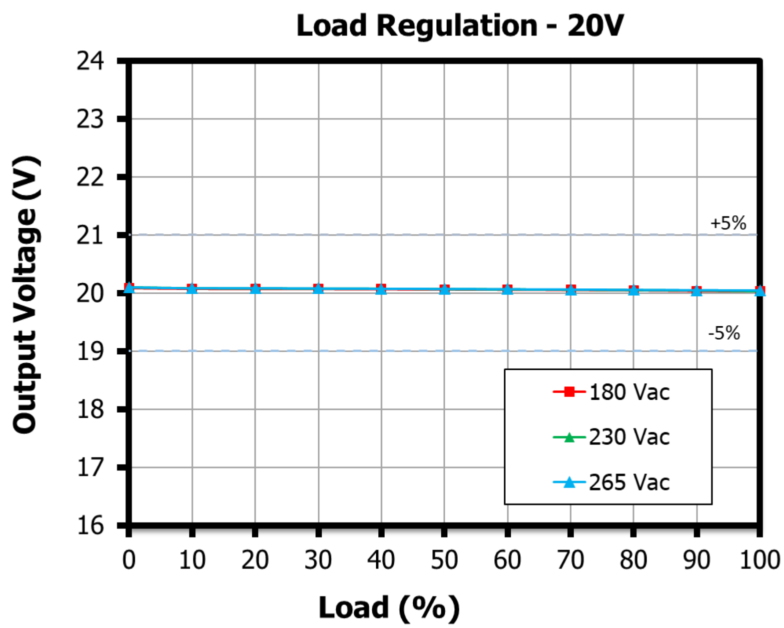


Figure 29 – Output Voltage vs. Load for 20 V Output, Room Temperature.

10.5.1.5 Output: 28 V / 3.57 A

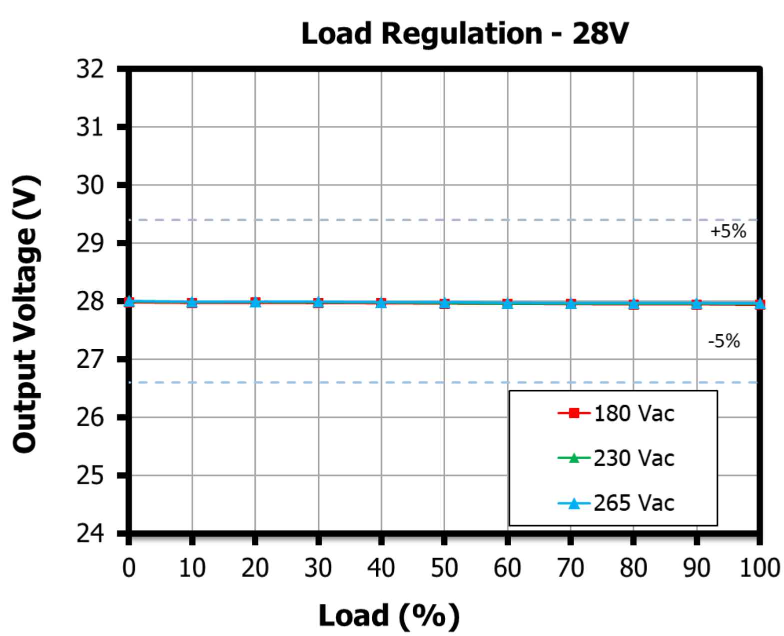


Figure 30 – Output Voltage vs. Load for 28 V Output, Room Temperature.

10.5.2 65W rated power, Low Line Input

10.5.2.1 Output: 5 V / 3.25 A

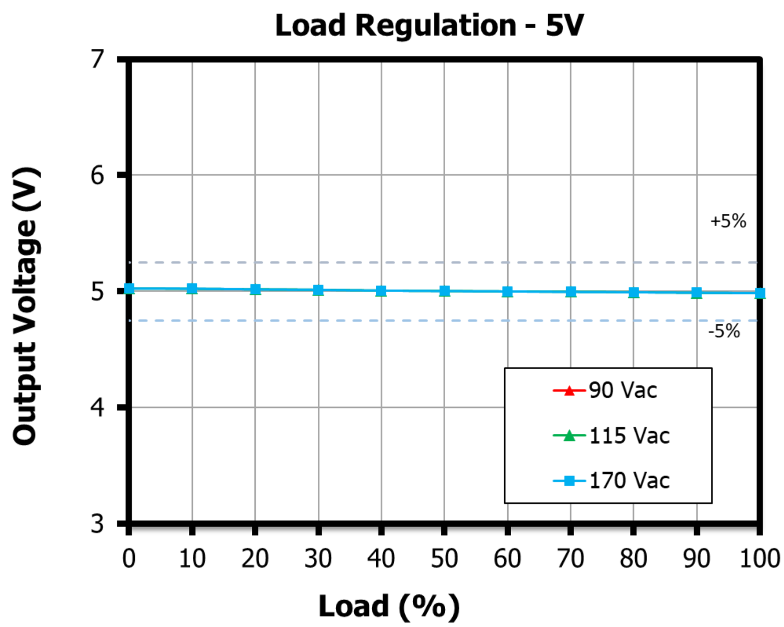


Figure 31 – Output Voltage vs. Load for 5 V Output, Room Temperature.

10.5.2.2 Output: 9 V / 3.25 A

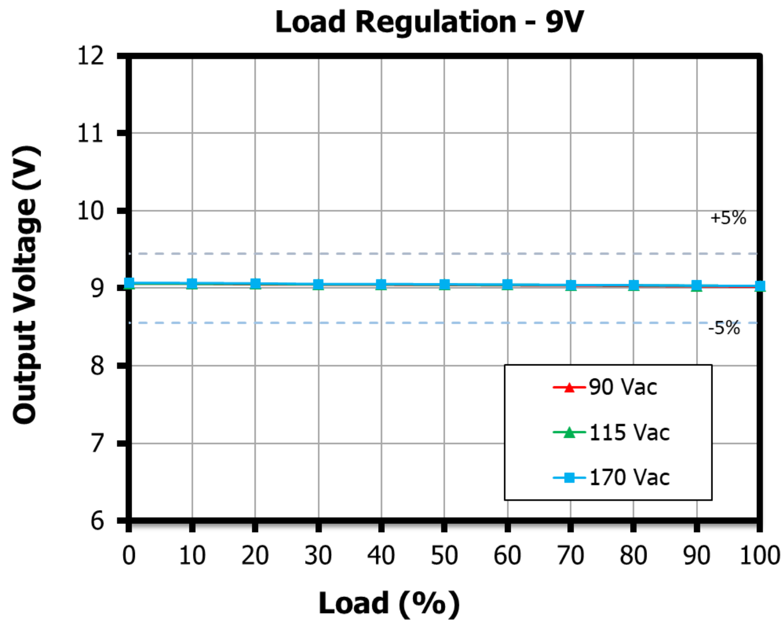


Figure 32 – Output Voltage vs. Load for 9 V Output, Room Temperature.

10.5.2.3 Output: 15 V / 3.25 A

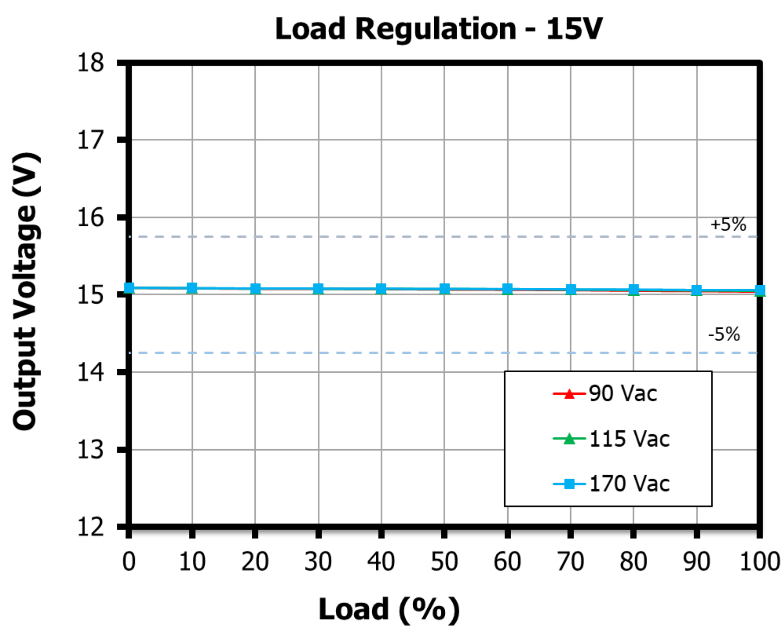


Figure 33 – Output Voltage vs. Load for 15 V Output, Room Temperature.

10.5.2.4 Output: 20 V / 3.25 A

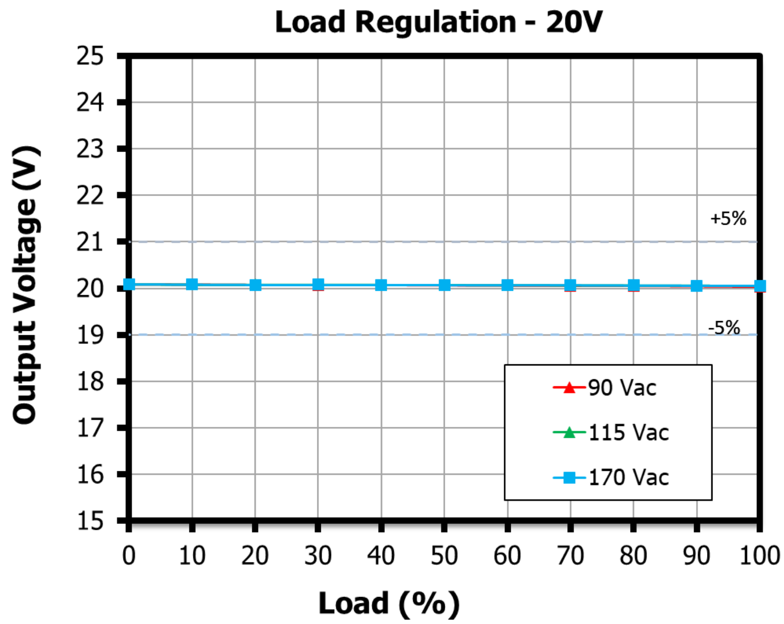


Figure 34 – Output Voltage vs. Load for 20 V Output, Room Temperature.

10.5.2.5 Output: 28 V / 2.32 A

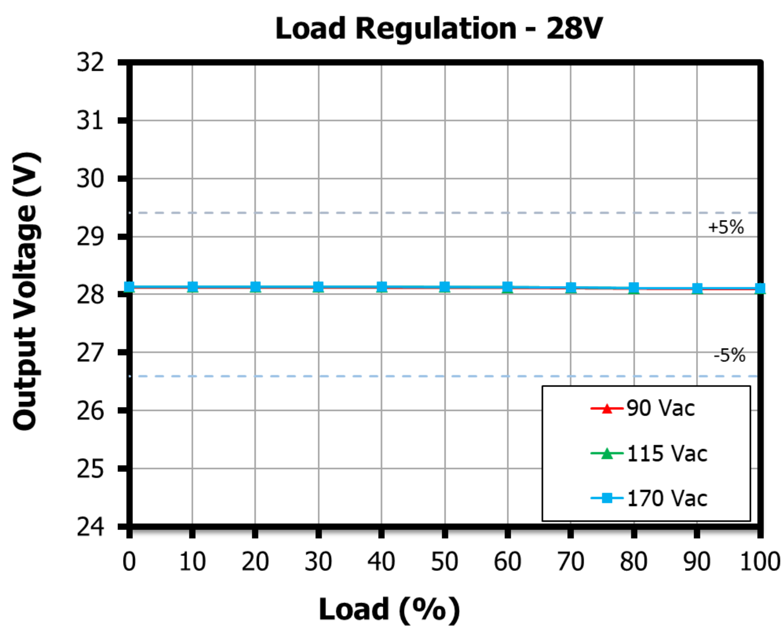


Figure 35 – Output Voltage vs. Load for 28 V Output, Room Temperature.

11 Thermal Performance - Open Case

Note: The performance data below is for open-case operation at room temperature following a one-hour soak for each load and line condition.

11.1 Output: 20 V / 5 A (180 VAC)

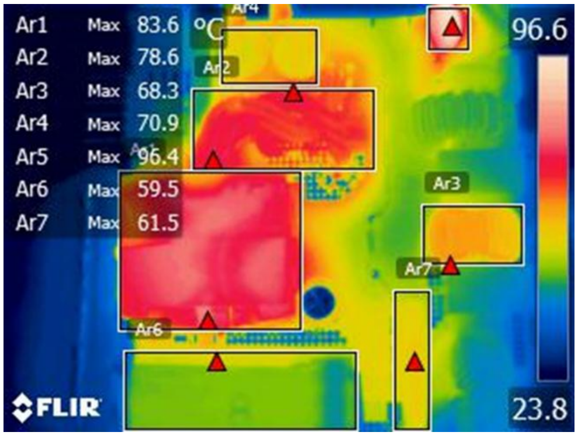


Figure 36 – Top Thermal Image.
Ar1: Transformer core = 83.6 °C.
Ar2: Transformer Winding = 78.6 °C.
Ar3: Common Mode Choke L2 = 68.3 °C.
Ar4: Output capacitor = 70.9 °C.
Ar5: Thermistor = 96.4 °C.
Ar6: Bulk cap = 59.5 °C.
Ar7: Input Bridge Rectifier = 61.5 °C

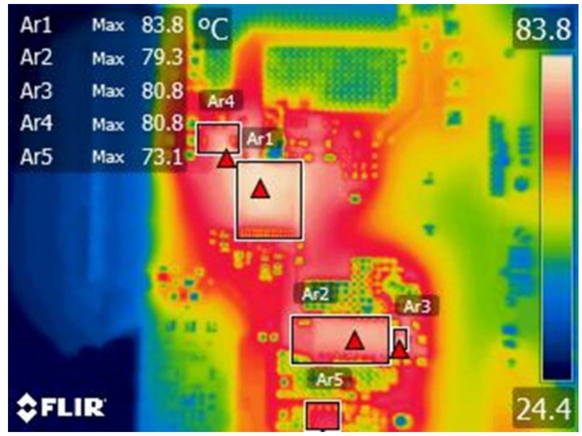


Figure 37 – Bottom Thermal Image.
Ar1: InnoSwitch5-Pro = 83.8 °C.
Ar2: SR FETs = 79.3 °C.
Ar3: Sec. Snubber Diode = 80.8 °C.
Ar4: Primary Clamp Diode = 80.8 °C.
Ar5: Bus switch = 73.1 °C.

Ambient = 25 °C.

11.2 Output: 20 V / 5 A (265 VAC)

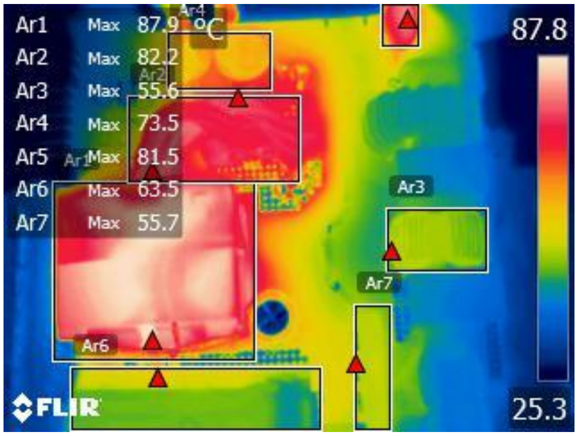


Figure 38 – Top Thermal Image.
Ar1: Transformer core = 87.9 °C.
Ar2: Transformer Winding = 82.2 °C.
Ar3: Common Mode Choke L2 = 55.6 °C
Ar4: Output capacitor = 73.5 °C.
Ar5: Thermistor = 81.5 °C.
Ar6: Bulk cap = 63.5 °C.
Ar7: Input Bridge Rectifier = 55.7 °C

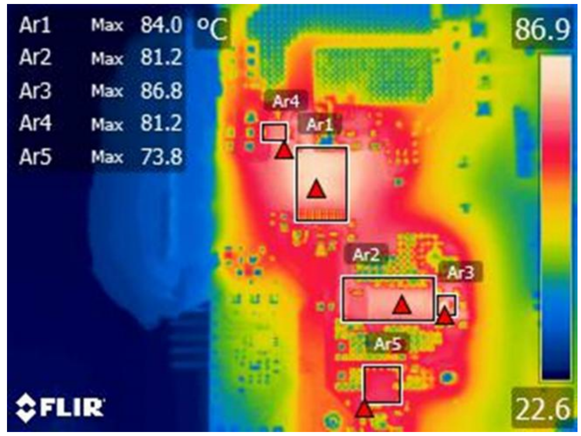
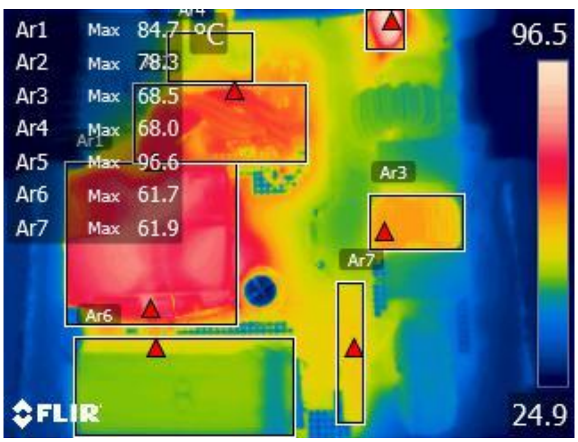


Figure 39 – Bottom Thermal Image.
Ar1: InnoSwitch5-Pro = 84 °C.
Ar2: SR FETs = 81.2 °C.
Ar3: Sec. Snubber Diode = 86.8 °C.
Ar4: Primary Clamp Diode = 81.2 °C.
Ar5: Bus switch = 73.8 °C.

Ambient = 25 °C.

11.3 Output: 28 V / 3.57 A (180 VAC)



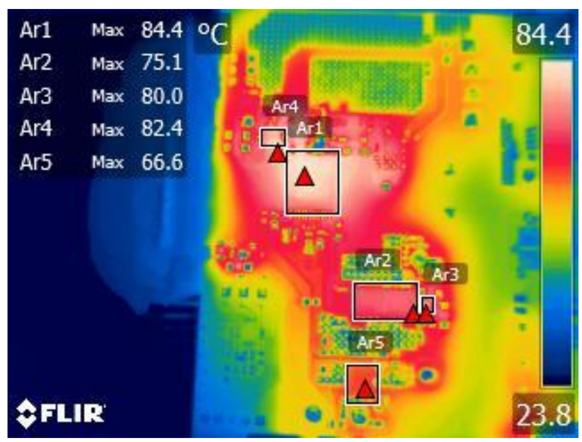


Figure 40 – Top Thermal Image.
Ar1: Transformer core = 84.7 °C.
Ar2: Transformer Winding = 78.3 °C.
Ar3: Common Mode Choke L2 = 68.5 °C.
Ar4: Output capacitor = 68 °C.
Ar5: Thermistor = 96.6 °C.
Ar6: Bulk cap = 61.7 °C.
Ar7: Input Bridge Rectifier = 61.9 °C.

Figure 41 – Bottom Thermal Image.
Ar1: InnoSwitch5-Pro = 84.4 °C.
Ar2: SR FETs = 75.1 °C.
Ar3: Sec. Snubber Diode = 80 °C.
Ar4: Primary Clamp Diode = 82.4 °C.
Ar5: Bus switch = 66.6 °C.

Ambient = 25 °C.

11.4 Output: 28 V / 3.57 A (265 VAC)

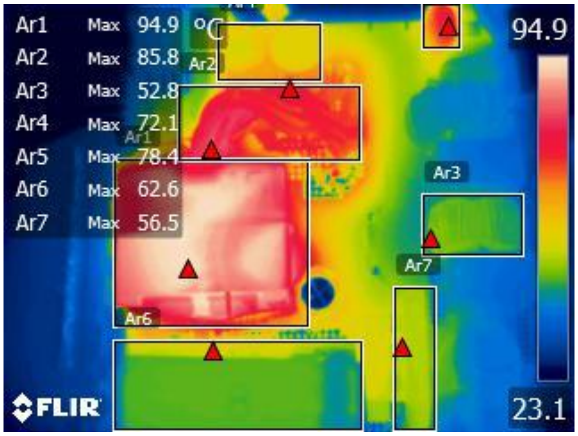


Figure 42 – Top Thermal Image.
Ar1: Transformer core = 95 °C.
Ar2: Transformer Winding = 85.8 °C.
Ar3: Common Mode Choke L2 = 53 °C.
Ar4: Output capacitor = 72 °C.
Ar5: Thermistor = 78.4 °C.
Ar6: Bulk cap = 62.6 °C.
Ar7: Input Bridge Rectifier = 56.5 °C.

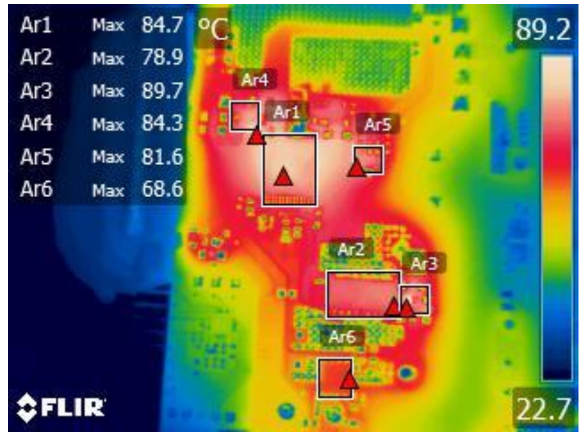


Figure 43 – Bottom Thermal Image.
Ar1: InnoSwitch5-Pro = 84.7 °C.
Ar2: SR FETs = 78.9 °C.
Ar3: Sec. Snubber Diode = 89.7 °C.
Ar4: Primary Clamp Diode = 84.3 °C.
Ar5: Primary Bias BJT = 81.6 °C.
Ar6: Bus switch = 68.6 °C.

Ambient = 25 °C.

12 Waveforms

12.1 Start-up

Note: Measurements taken at room temperature

12.1.1 Primary FET Voltage and Current Waveforms

Figure 44 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 0 A Load (V_{DS}_pri:246 V)
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 100 V / div.
Time: 200 µs / div. (Zoom: 20 µs / div.)

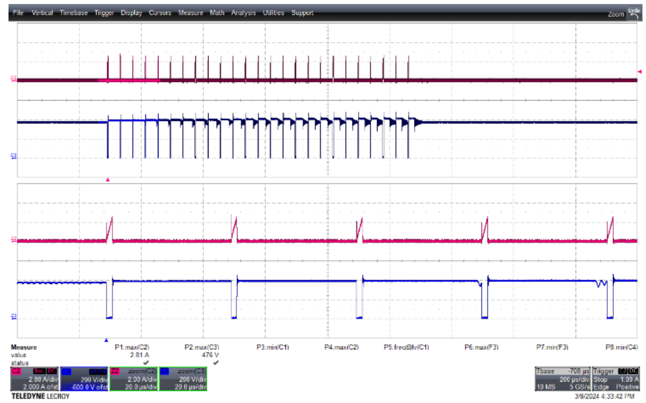


Figure 45 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 0 A Load (V_{DS}_pri:476 V)
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 200 µs / div. (Zoom: 20 µs / div.)

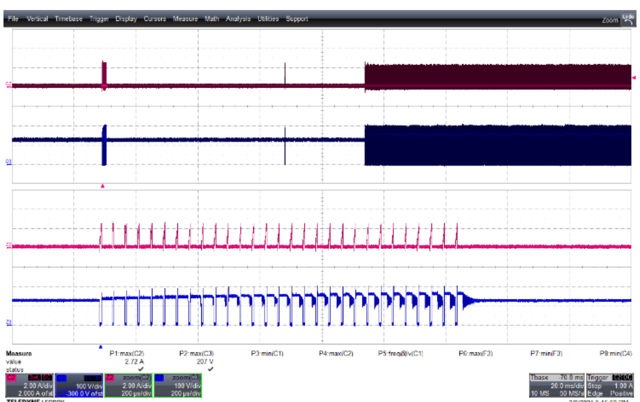


Figure 46 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 3.25 A Load (V_{DS}_pri:207 V)
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 100 V / div.
Time: 20 ms / div. (Zoom: 200 µs / div.)

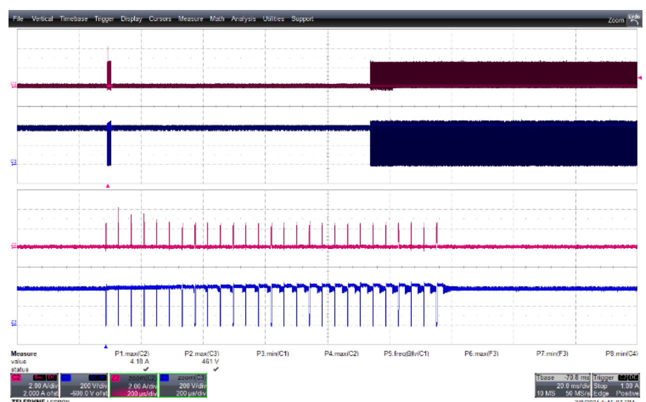


Figure 47 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 5 A Load (V_{DS}_pri:461 V)
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 ms / div. (Zoom: 200 µs / div.)

12.1.2 SR FET Voltage Waveform

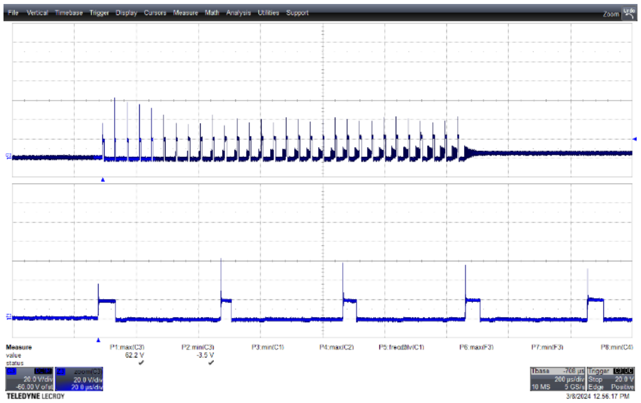


Figure 48 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 0 A Load (V_{DS_SR}:62.2 V).
C3: V_{DRAIN_SR}, 20 V / div.
Time: 200 µs / div. (Zoom: 20 µs / div.)

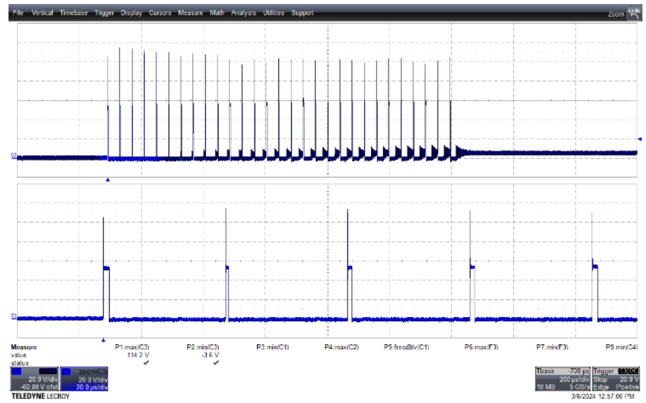


Figure 49 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 0 A Load (V_{DS_SR}:114.2 V).
C3: V_{DRAIN_SR}, 20 V / div.
Time: 200 µs / div. (Zoom: 20 µs / div.)

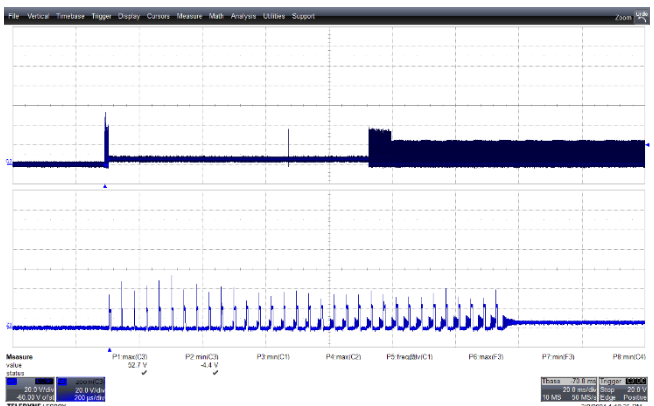


Figure 50 – SR FET Voltage Waveforms.
90 VAC, 5.0 V, 3.25 A Load (V_{DS_SR}:52.7V).
C3: V_{DRAIN_SR}, 20 V / div.
Time: 20 ms / div. (Zoom: 200 µs / div.)

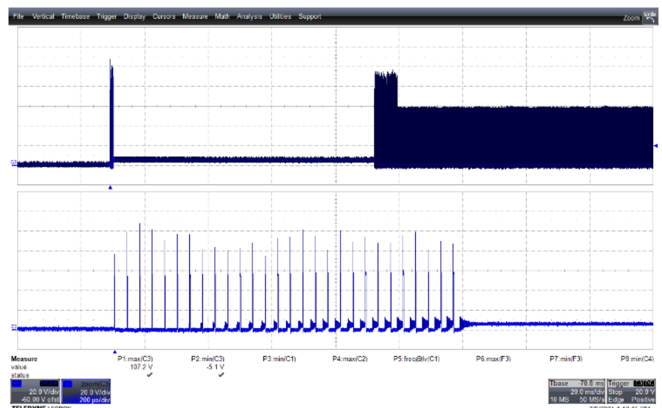


Figure 51 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 5 A Load (V_{DS_SR}:107.2V).
C3: V_{DRAIN_SR}, 20 V / div.
Time: 20 ms / div. (Zoom: 200 µs / div.)

12.2 Steady-State Switching Waveforms

Note: Measurements taken at room temperature

12.2.1 Primary Drain Voltage and Current During Steady-State Operation.

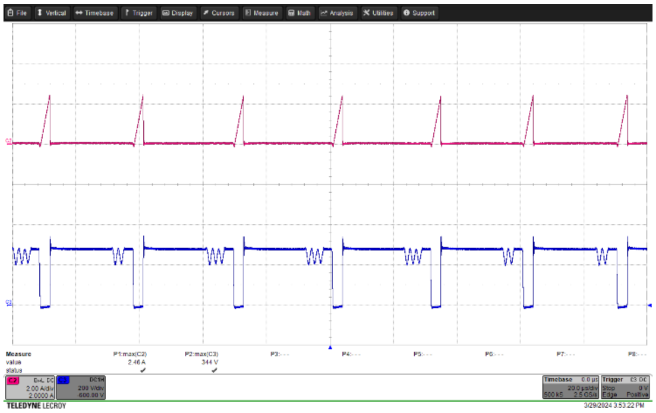


Figure 52 – Drain voltage and current Waveforms.
180 VAC, 5.0 V, 5 A Load
V_{DS}_pri: 344 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 µs / div.

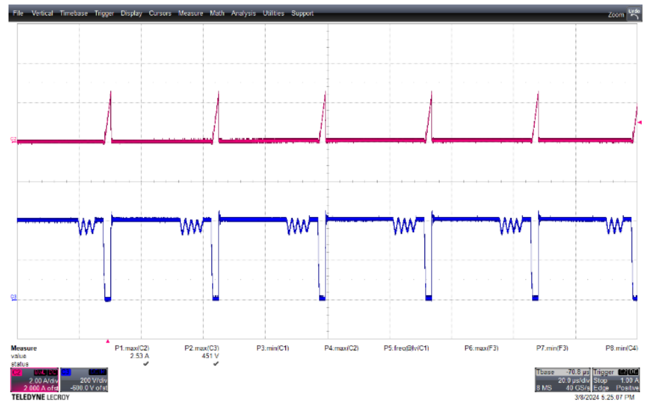


Figure 53 – Drain voltage and current Waveforms.
265 VAC, 5.0 V, 5 A Load
V_{DS}_pri: 451 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 µs / div.

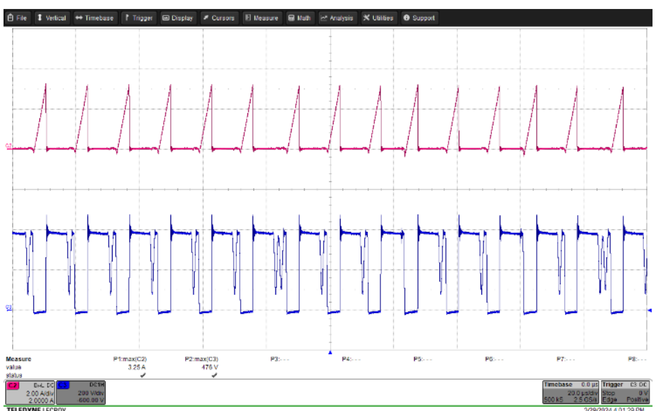


Figure 54 – Drain voltage and current Waveforms.
180 VAC, 20.0 V, 5 A Load
V_{DS}_pri: 476 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 µs / div.

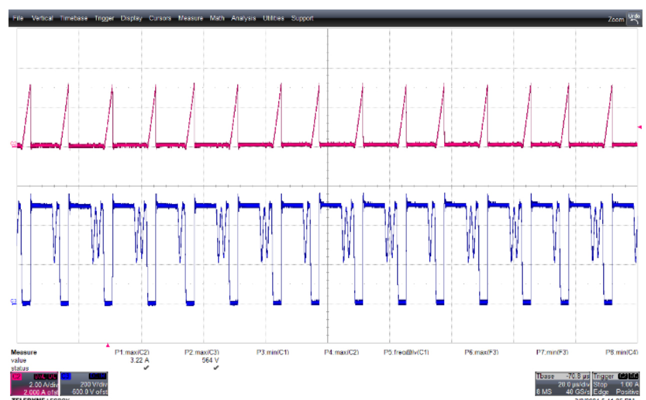


Figure 55 – Drain voltage and current Waveforms.
265 VAC, 20.0 V, 5 A Load
V_{DS}_pri: 564 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 µs / div.

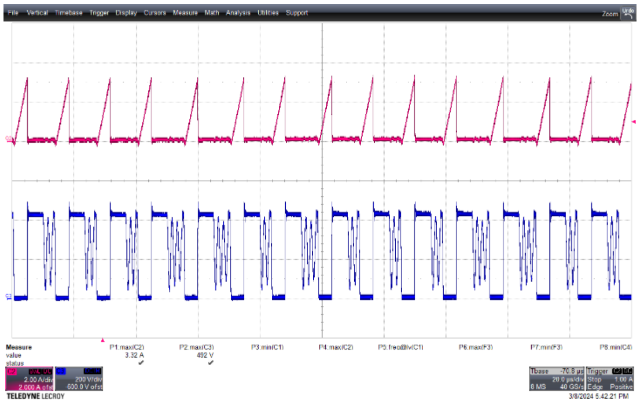


Figure 56 – Drain voltage and current Waveforms.
180 VAC, 28.0 V, 3.57 A Load
V_{DS}_pri: 492 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 μs / div.

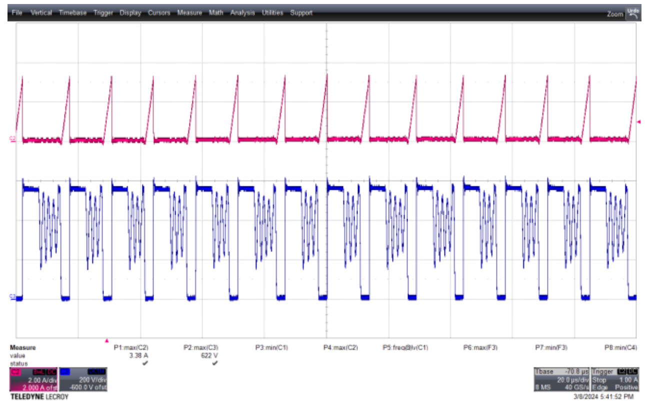


Figure 57 – Drain voltage and current Waveforms.
265 VAC, 28.0 V, 3.57 A Load
V_{DS}_pri: 622 V
C2: I_{DRAIN}, 2 A / div.
C3: V_{DRAIN_PRI}, 200 V / div.
Time: 20 μs / div.

12.2.2 SR FET Waveforms in Steady-State

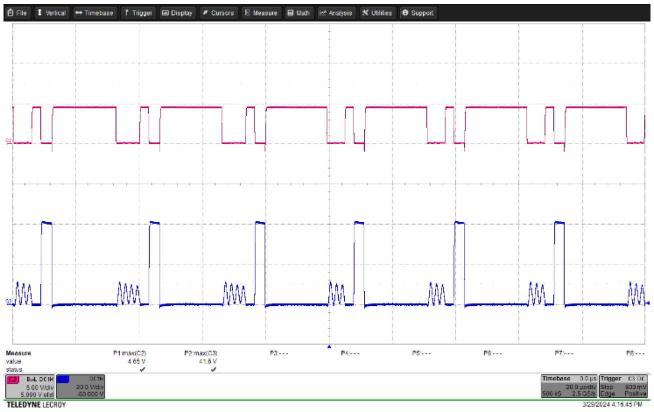


Figure 58 – SR FET Voltage Waveforms.
180 VAC, 5.0 V, 5 A Load
V_{DS_SR}=41.6 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 μs / div.

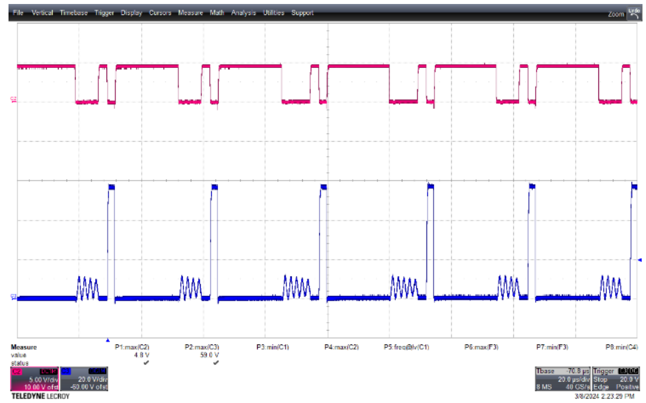


Figure 59 – SR FET Voltage Waveforms.
265 VAC, 5.0 V, 5 A Load
V_{DS_SR}=59 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 μs / div.

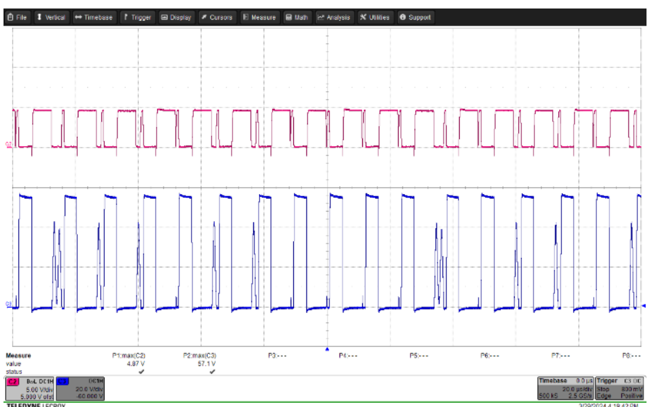


Figure 60 – SR FET Voltage Waveforms.
180 VAC, 20.0 V, 5 A Load
V_{DS_SR}=57.1 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 μs / div.

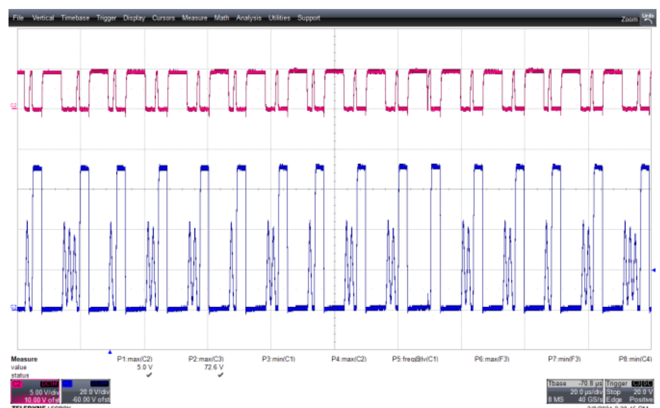


Figure 61 – SR FET Voltage Waveforms.
265 VAC, 20.0 V, 5 A Load
V_{DS_SR}=72.6 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 μs / div.

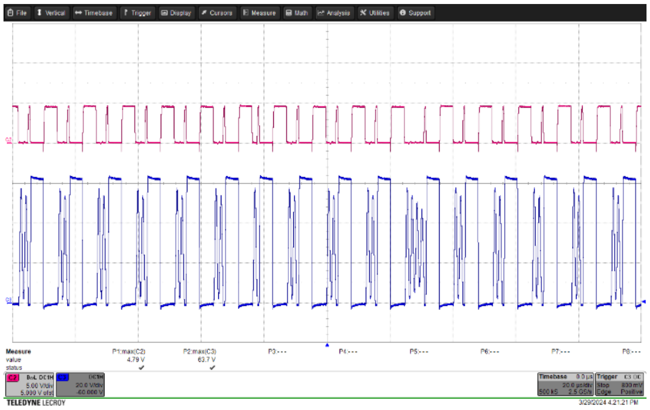


Figure 62 – SR FET Voltage Waveforms.
180 VAC, 28.0 V, 3.57 A Load
V_{DS_SR}=63.7 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 µs / div.

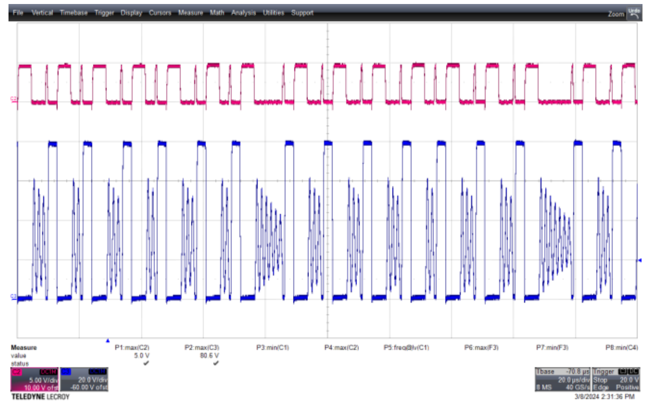


Figure 63 – SR FET Voltage Waveforms.
265 VAC, 28.0 V, 3.57 A Load
V_{DS_SR}=80.6 V
C2: SR V_{GS}, 5 V / div.
C3: V_{DRAIN}, 20 V / div.
Time: 20 µs / div.

12.3 Load Transient Response

Note 1: Output voltages measured on the board.
2: Measurements taken at room temperature.

12.3.1 Output: 5 V / 5 A

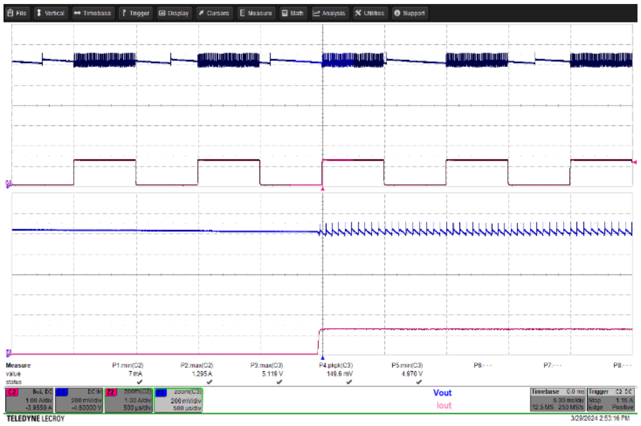


Figure 64 – Transient Response.
180 VAC, 5.0 V, 0 – 1.25 A Load Step.
$VOUT_{MIN}$: 4.97 V, $VOUT_{MAX}$: 5.12 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

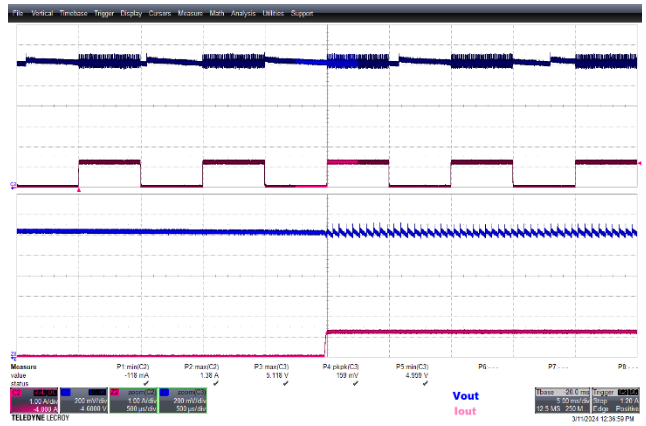


Figure 65 – Transient Response.
265 VAC, 5.0 V, 0 – 1.25 A Load Step.
$VOUT_{MIN}$: 4.96 V, $VOUT_{MAX}$: 5.12 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

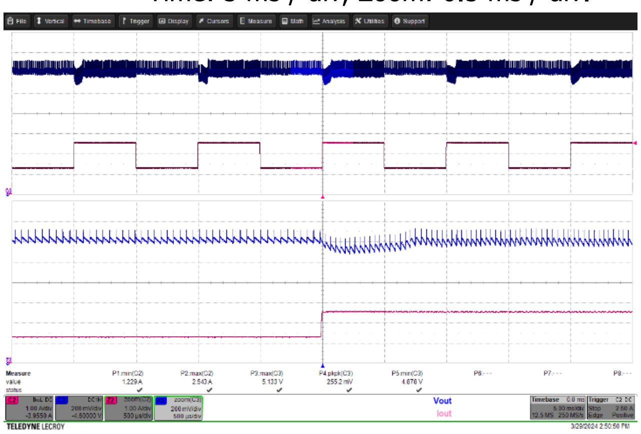


Figure 66 – Transient Response.
180 VAC, 5.0 V, 1.25 – 2.5 A Load Step.
$VOUT_{MIN}$: 4.88 V, $VOUT_{MAX}$: 5.13 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

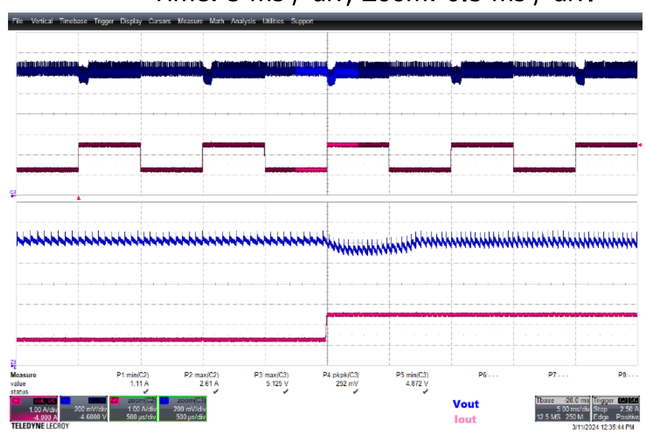


Figure 67 – Transient Response.
265 VAC, 5.0 V, 1.25 – 2.5 A Load Step.
$VOUT_{MIN}$: 4.87 V, $VOUT_{MAX}$: 5.13 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

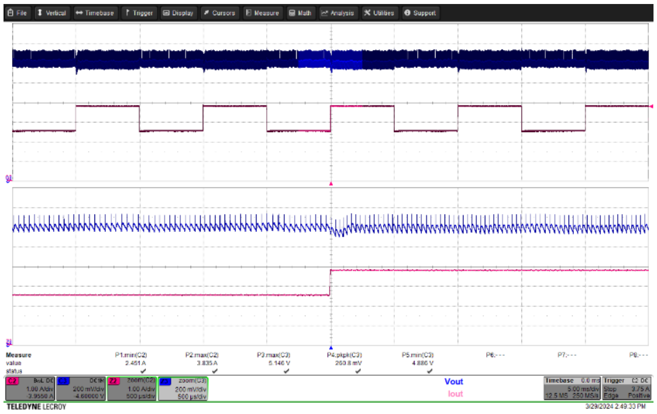


Figure 68 – Transient Response.
180 VAC, 5.0 V, 2.5 – 3.75 A Load Step.
$VOUT_{MIN}$: 4.89 V, $VOUT_{MAX}$: 5.15 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms/div, Zoom: 0.5 ms / div.

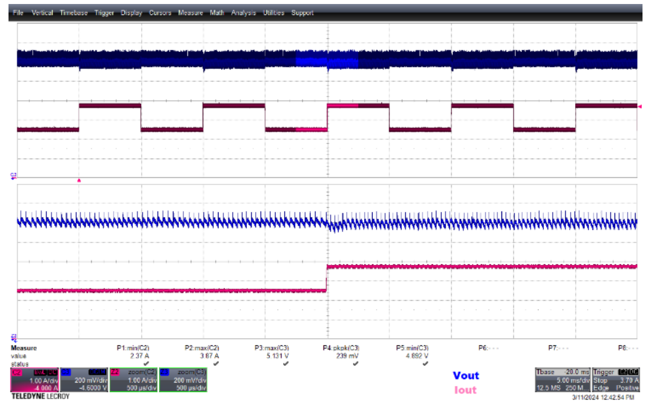


Figure 69 – Transient Response.
265 VAC, 5.0 V, 2.5 –3.75 A Load Step.
$VOUT_{MIN}$: 4.89 V, $VOUT_{MAX}$: 5.13 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms/div, Zoom: 0.5 ms / div.

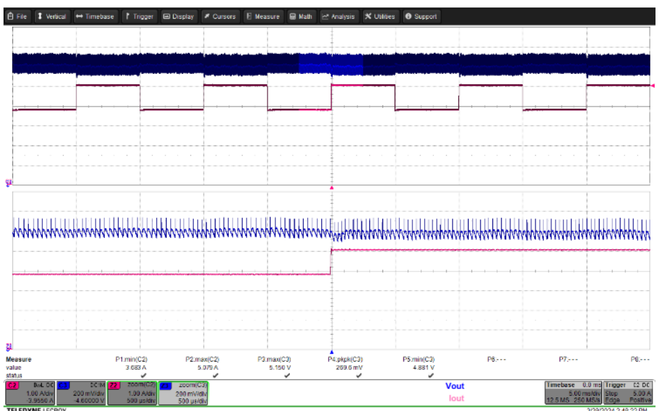


Figure 70 – Transient Response.
180 VAC, 5.0 V, 3.75 – 5 A Load Step.
$VOUT_{MIN}$: 4.88 V, $VOUT_{MAX}$: 5.15 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

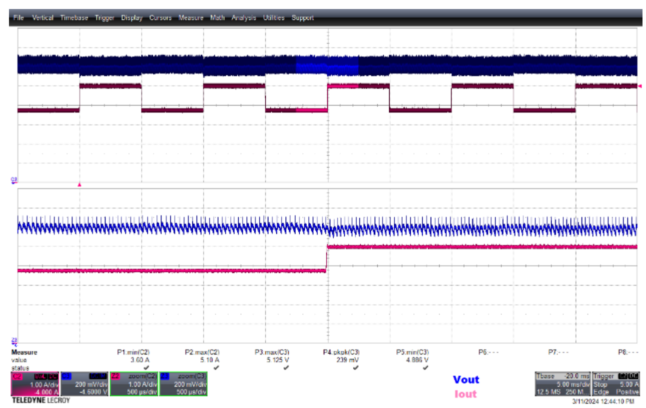


Figure 71 – Transient Response.
265 VAC, 5.0 V, 3.75 – 5 A Load Step.
$VOUT_{MIN}$: 4.89 V, $VOUT_{MAX}$: 5.13 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

12.3.2 Output: 20 V / 5 A

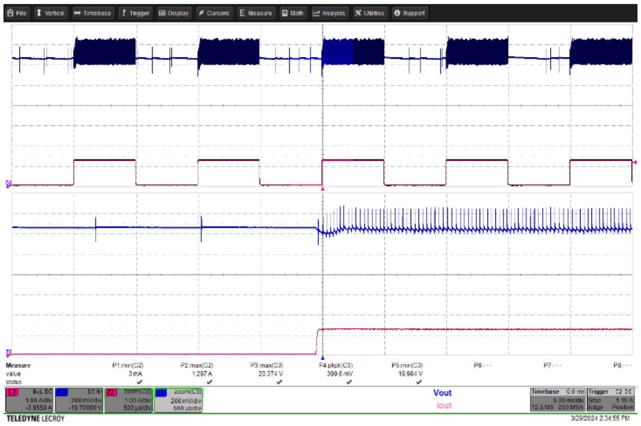


Figure 72 – Transient Response.
180 VAC, 20.0 V, 0 – 1.25 A Load Step.
$VOUT_{MIN}$: 20.0 V, $VOUT_{MAX}$: 20.4 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

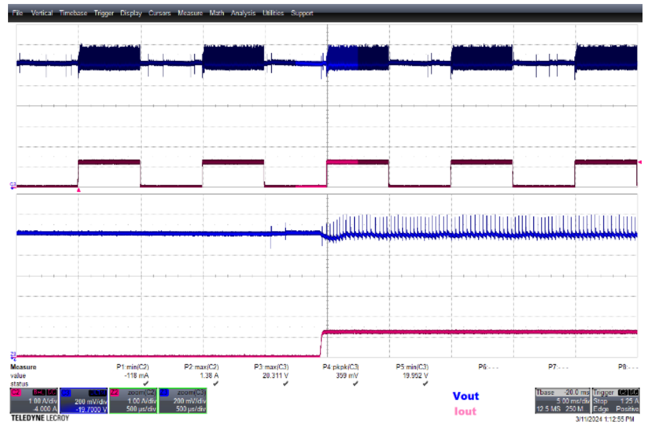


Figure 73 – Transient Response.
265 VAC, 20.0 V, 0 – 1.25 A Load Step.
$VOUT_{MIN}$: 20.0 V, $VOUT_{MAX}$: 20.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div

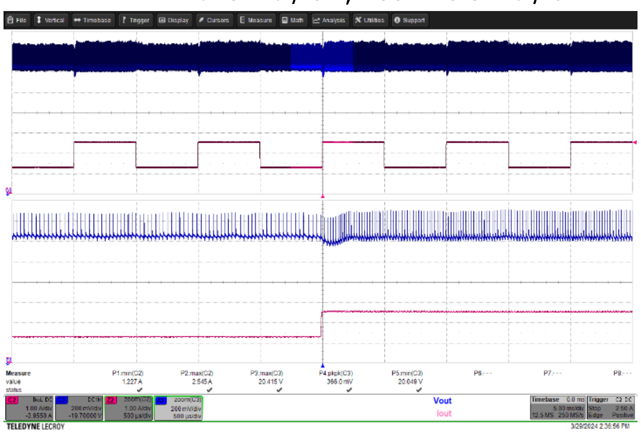


Figure 74 – Transient Response.
180 VAC, 20.0 V, 1.25 – 2.5 A Load Step.
$VOUT_{MIN}$: 20.1 V, $VOUT_{MAX}$: 20.4 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div

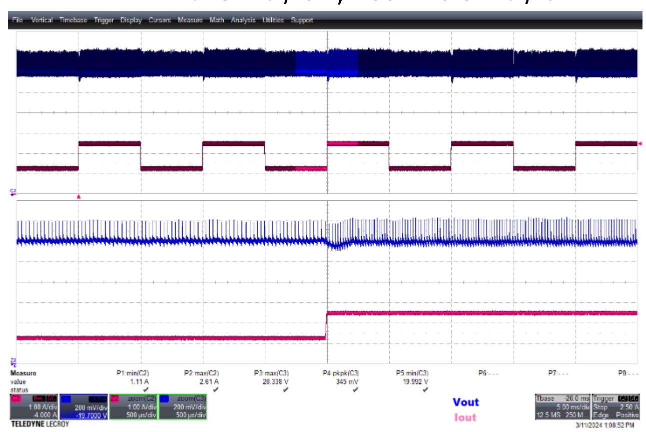


Figure 75 – Transient Response.
265 VAC, 20.0 V, 1.25 – 2.5 A Load Step.
$VOUT_{MIN}$: 20.0 V, $VOUT_{MAX}$: 20.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div

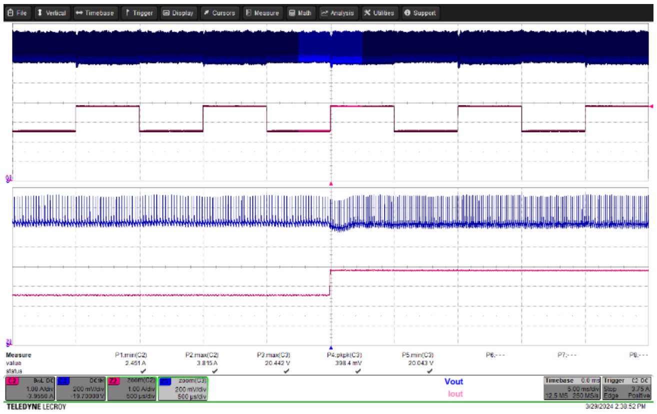


Figure 76 – Transient Response.
180 VAC, 20.0 V, 2.5 – 3.75 A Load Step.
VOUT$_{MIN}$: 20.0 V, VOUT$_{MAX}$: 20.4 V.
C2: I$_{LOAD}$, 1 A / div.
C3: V$_{OUT}$, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div

Figure 77 – Transient Response.
265 VAC, 20.0 V, 2.5 – 3.75 A Load Step.
VOUT$_{MIN}$: 20.0 V, VOUT$_{MAX}$: 20.4 V.
C2: I$_{LOAD}$, 1 A / div.
C3: V$_{OUT}$, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div

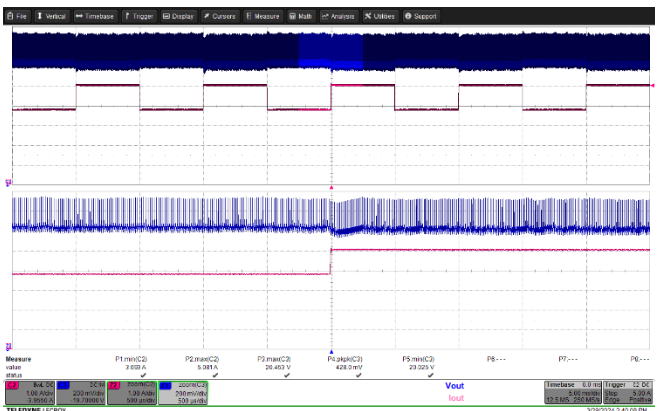


Figure 78 – Transient Response.
180 VAC, 20.0 V, 3.75 – 5 A Load Step.
VOUT$_{MIN}$: 20.0 V, VOUT$_{MAX}$: 20.5 V.
C2: I$_{LOAD}$, 1 A / div.
C3: V$_{OUT}$, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

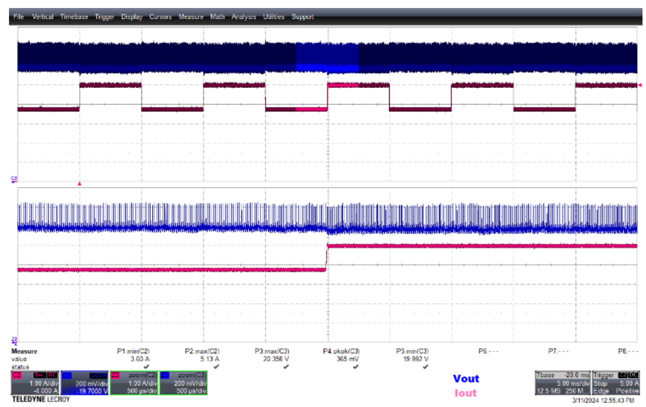


Figure 79 – Transient Response.
265 VAC, 20.0 V, 3.75 – 5 A Load Step.
VOUT$_{MIN}$: 20.0 V, VOUT$_{MAX}$: 20.4 V.
C2: I$_{LOAD}$, 1 A / div.
C3: V$_{OUT}$, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

12.3.3 Output: 28 V / 3.57 A

Figure 80 – Transient Response.
180 VAC, 28.0 V, 0 – 0.89 A Load Step.
$VOUT_{MIN}$: 27.9 V, $VOUT_{MAX}$: 28.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

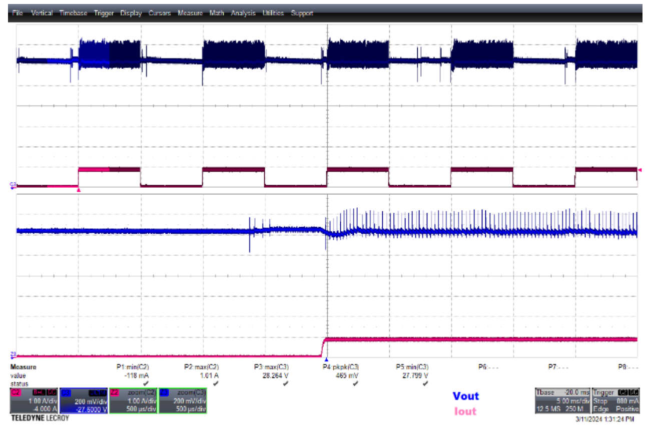


Figure 81 – Transient Response.
265 VAC, 28.0 V, 0 – 0.89 A Load Step.
$VOUT_{MIN}$: 27.8 V, $VOUT_{MAX}$: 28.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

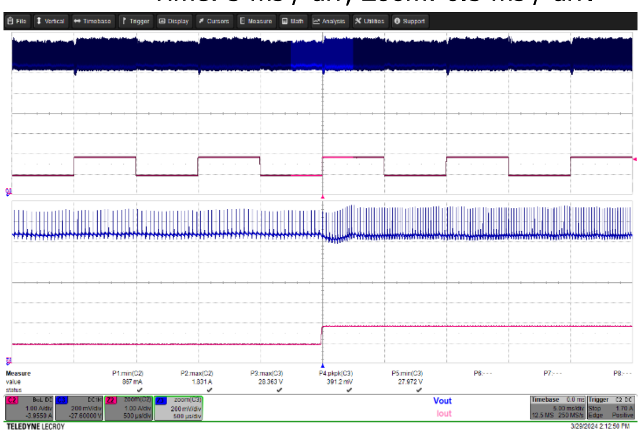


Figure 82 – Transient Response.
180 VAC, 28.0 V, 0.89 – 1.79 A Load Step.
$VOUT_{MIN}$: 28.0 V, $VOUT_{MAX}$: 28.4 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

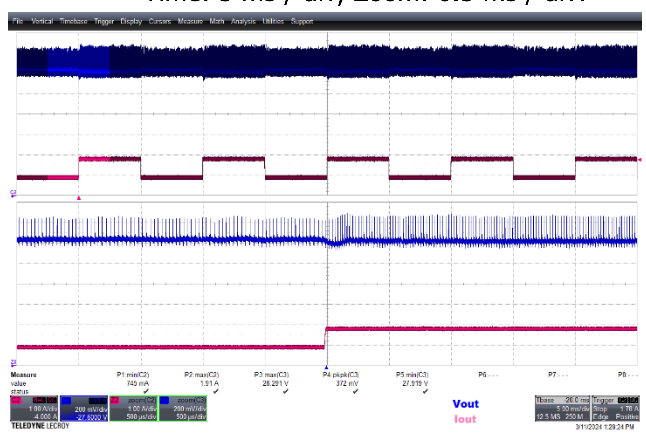


Figure 83 – Transient Response.
265 VAC, 28.0 V, 0.89 – 1.79 A Load Step.
$VOUT_{MIN}$: 27.9 V, $VOUT_{MAX}$: 28.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

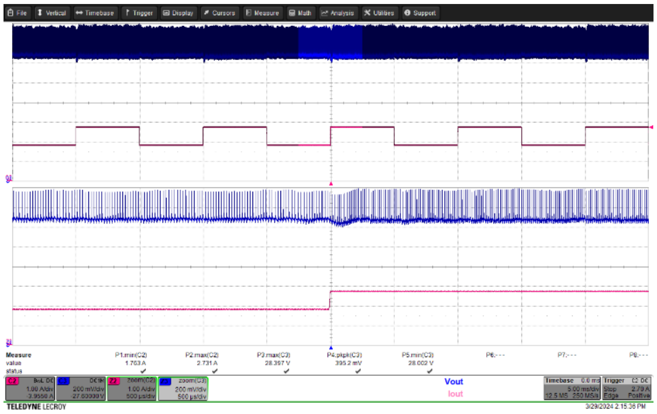


Figure 84 – Transient Response.
180 VAC, 28.0 V, 1.79 – 2.68 A Load Step.
$VOUT_{MIN}$: 28.0 V, $VOUT_{MAX}$: 28.4 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

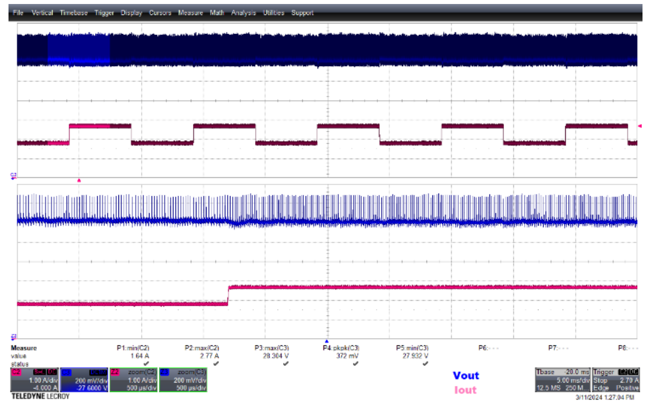


Figure 85 – Transient Response.
265 VAC, 28.0 V, 1.79 – 2.68 A Load Step.
$VOUT_{MIN}$: 27.9 V, $VOUT_{MAX}$: 28.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

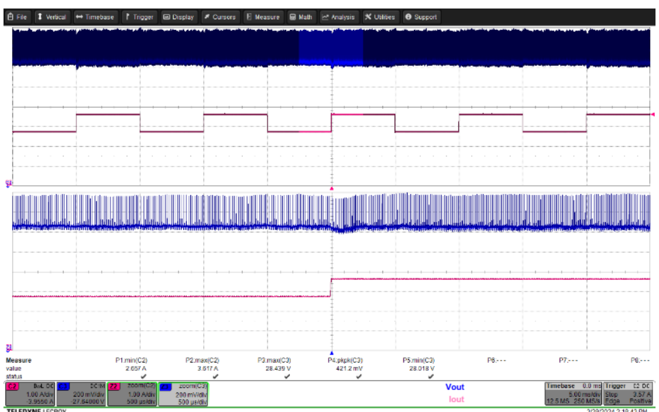


Figure 86 – Transient Response.
180 VAC, 28.0 V, 2.68 – 3.57 A Load Step.
$VOUT_{MIN}$: 28.0 V, $VOUT_{MAX}$: 28.4 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

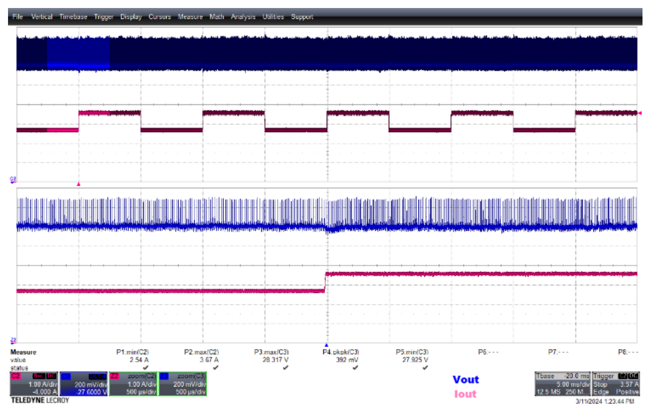


Figure 87 – Transient Response.
265 VAC, 28.0 V, 2.68 – 3.57 A Load Step.
$VOUT_{MIN}$: 27.9 V, $VOUT_{MAX}$: 28.3 V.
C2: I_{LOAD}, 1 A / div.
C3: V_{OUT}, 0.2 V / div.
Time: 5 ms / div, Zoom: 0.5 ms / div.

13 Output Ripple Measurements

13.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals caused by pick-up. Details of the probe modification are provided below.

The 4987BA probe adapter modified by having two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

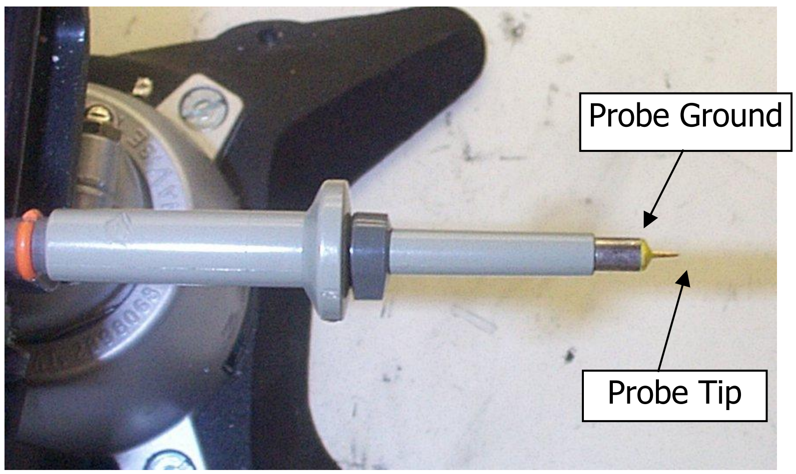


Figure 88 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

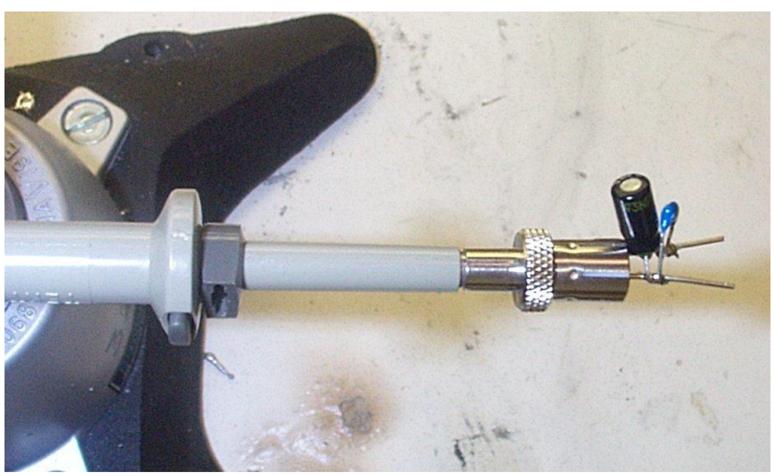


Figure 89 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987BA BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.2 Output Voltage Ripple Waveforms

Note 1: Output voltages captured at the end of 100mΩ cable
2: Measurements taken at room temperature

13.2.1 Output: 5 V

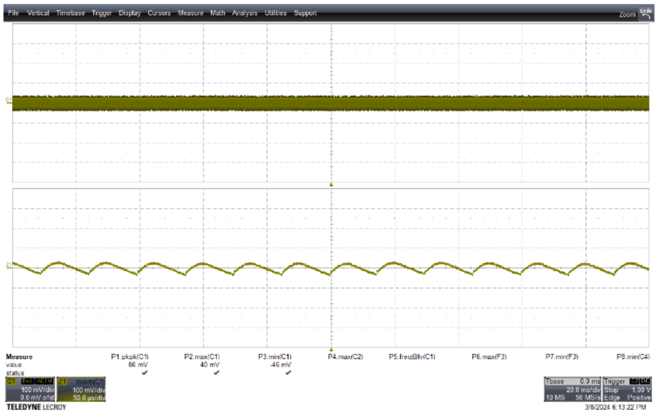


Figure 90 – Output Ripple. PK-PK = 86 mV.
90 VAC_{IN} 5.0 V, 3.25 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

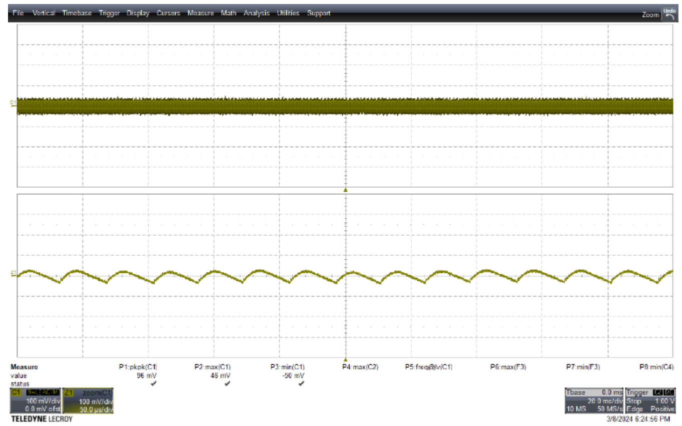


Figure 91 – Output Ripple. PK-PK = 96 mV.
170 VAC_{IN} 5.0 V, 3.25 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

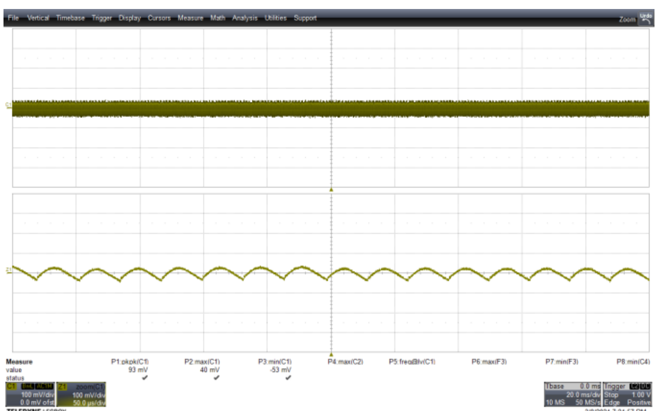


Figure 92 – Output Ripple. PK-PK = 93 mV.
180 VAC_{IN} 5.0 V, 5 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

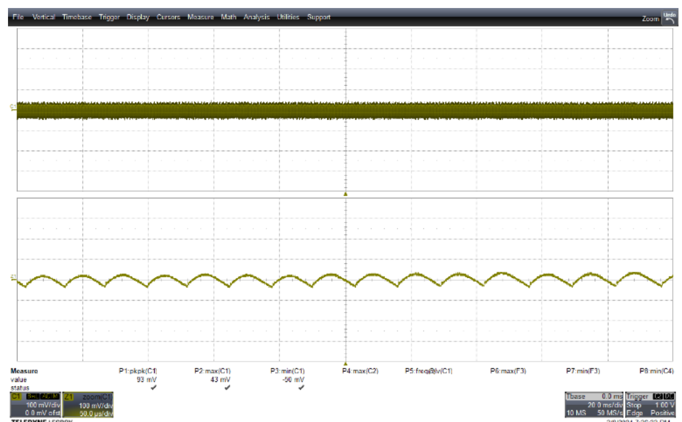


Figure 93 – Output Ripple. PK-PK = 93 mV.
265 VAC_{IN} 5.0 V, 5 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

13.2.2 Output: 20 V

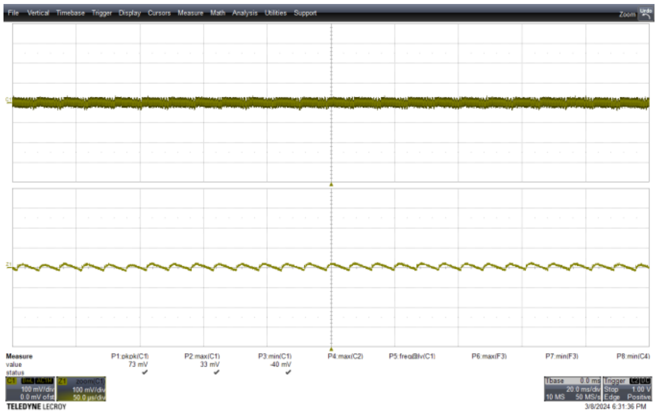


Figure 94 – Output Ripple. PK-PK = 73 mV.
90 VAC_{IN} 20.0 V, 3.25 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

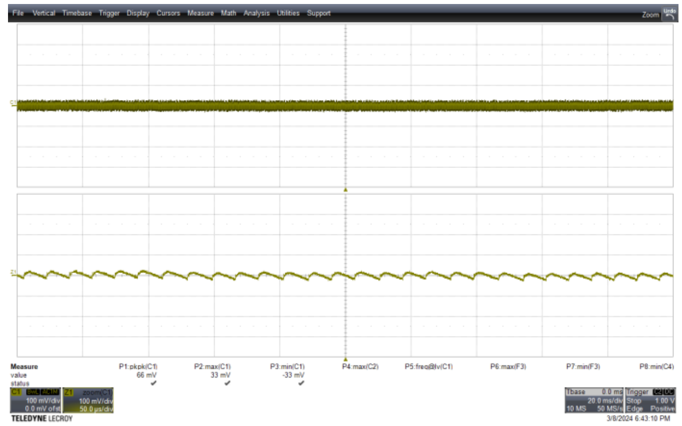


Figure 95 – Output Ripple. PK-PK = 66 mV.
170 VAC_{IN} 20.0 V, 3.25 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

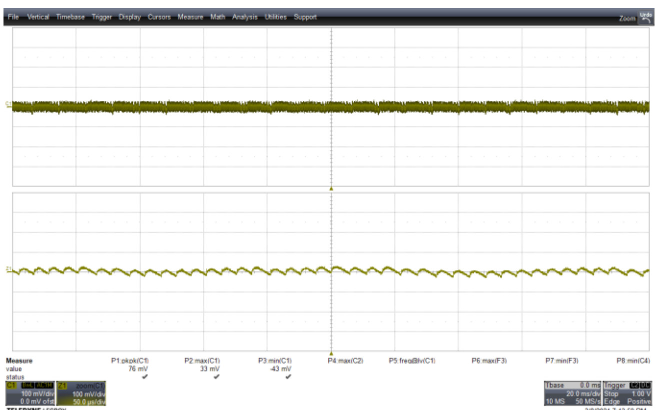


Figure 96 – Output Ripple. PK-PK = 76 mV.
180 VAC_{IN} 20.0 V, 5 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

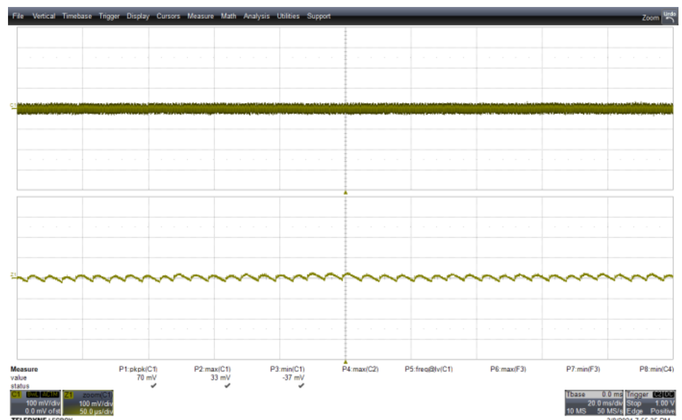


Figure 97 – Output Ripple. PK-PK = 70 mV.
265 VAC_{IN} 20.0 V, 5 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

13.2.3 Output: 28 V

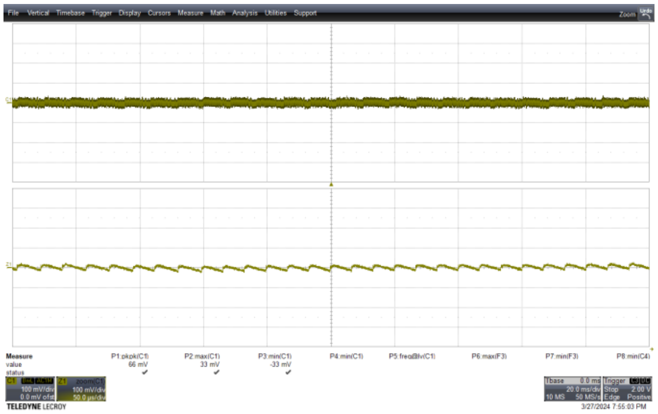


Figure 98 – Output Ripple. PK-PK = 66 mV.
90 VAC_{IN} 28.0 V, 2.32 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

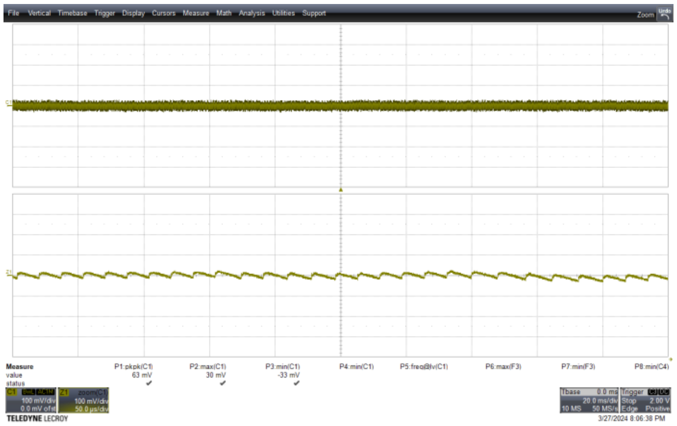


Figure 99 – Output Ripple. PK-PK = 63 mV.
170 VAC_{IN} 28.0 V, 2.32 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

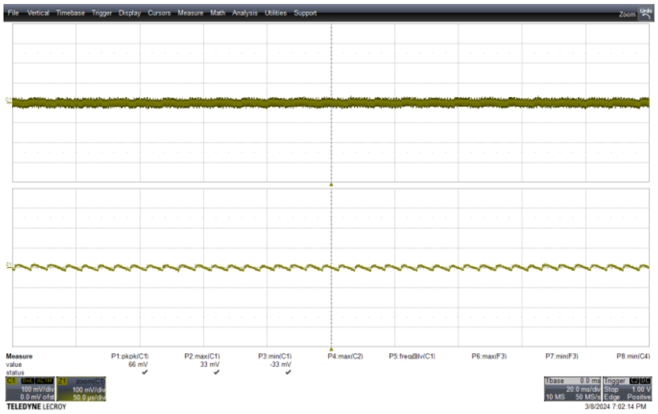


Figure 100 – Output Ripple. PK-PK = 66 mV.
180 VAC_{IN} 28.0 V, 3.57 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

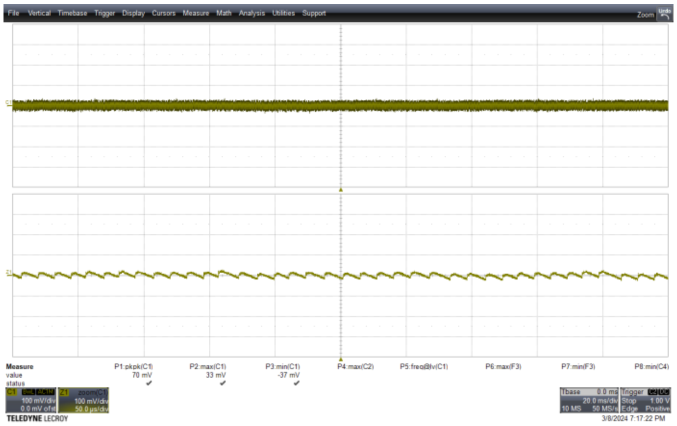


Figure 101 – Output Ripple. PK-PK = 70 mV.
265 VAC_{IN} 28.0 V, 3.57 A Load.
V_{OUT}, 100 mV / div., 20 ms / div.
Zoom: 50 µs / div.

13.3 Output Voltage Ripple Amplitude

Note 1: Output voltages captured at the end of 100mΩ cable
2: Measurements taken at room temperature

13.3.1 Output: 5 V / 5 A, High Line Input

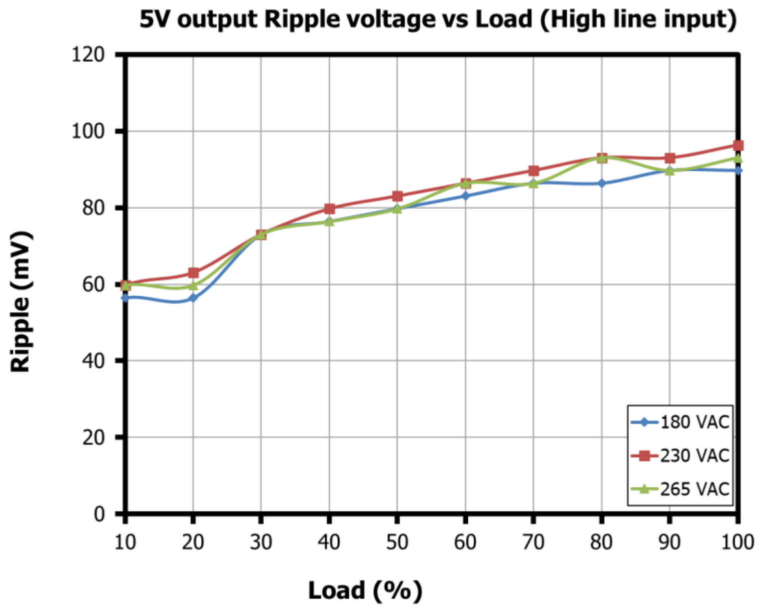


Figure 102 – 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.2 Output: 20 V / 5 A, High Line Input

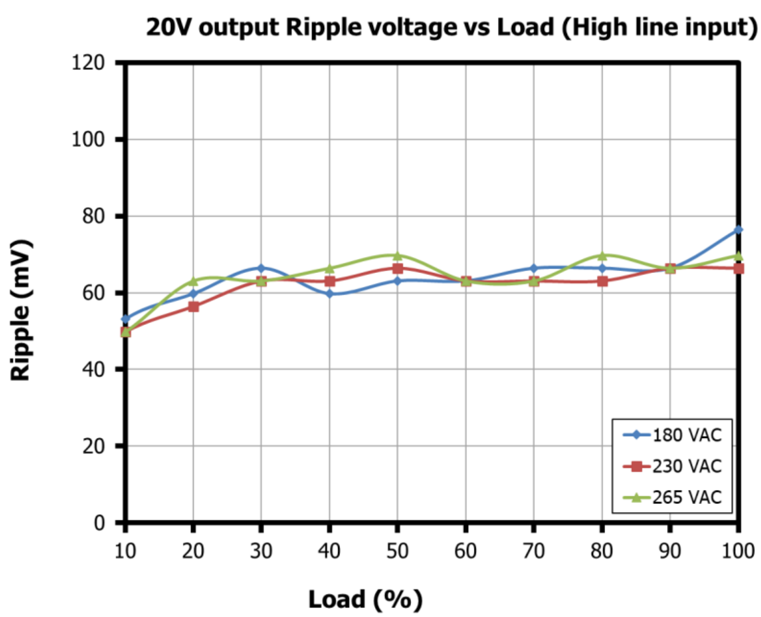


Figure 103 **–** 20 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.3 Output: 28 V / 3.57 A, High Line Input

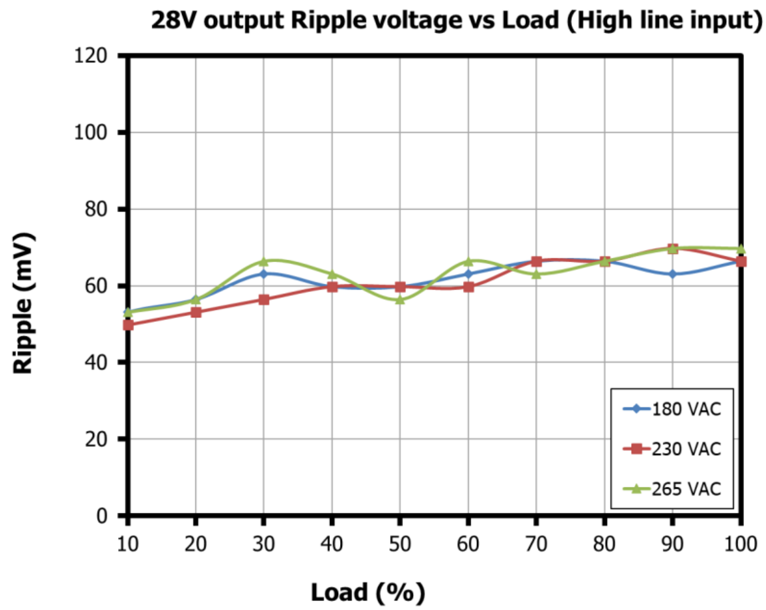


Figure 104 – 28 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.4 Output: 5 V / 3.25 A, Low Line Input

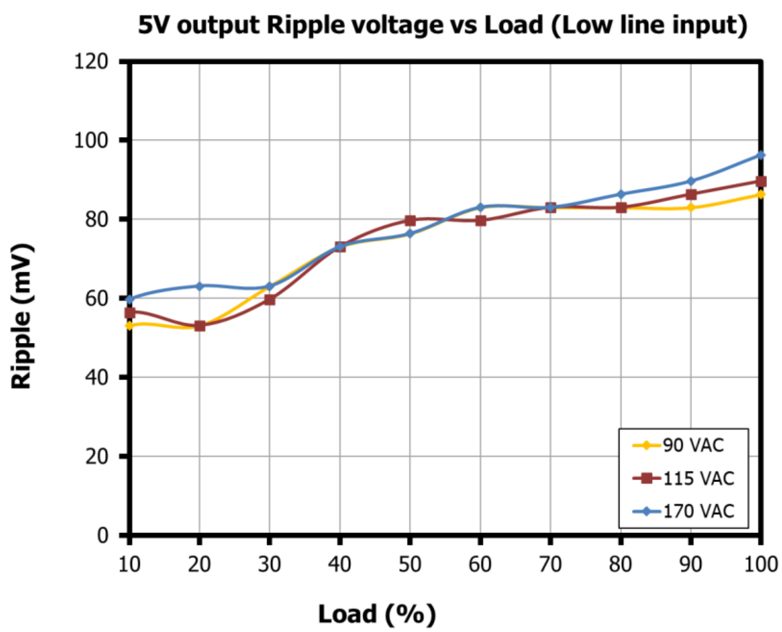


Figure 105 **–** 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.5 Output: 20 V / 3.25 A, Low Line Input

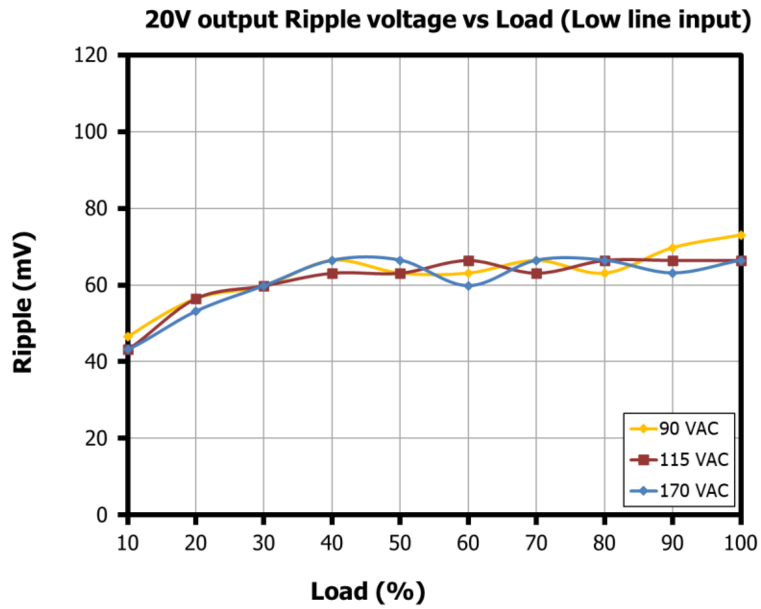


Figure 106 – 20 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

13.3.6 Output: 28 V / 2.32 A, Low Line Input

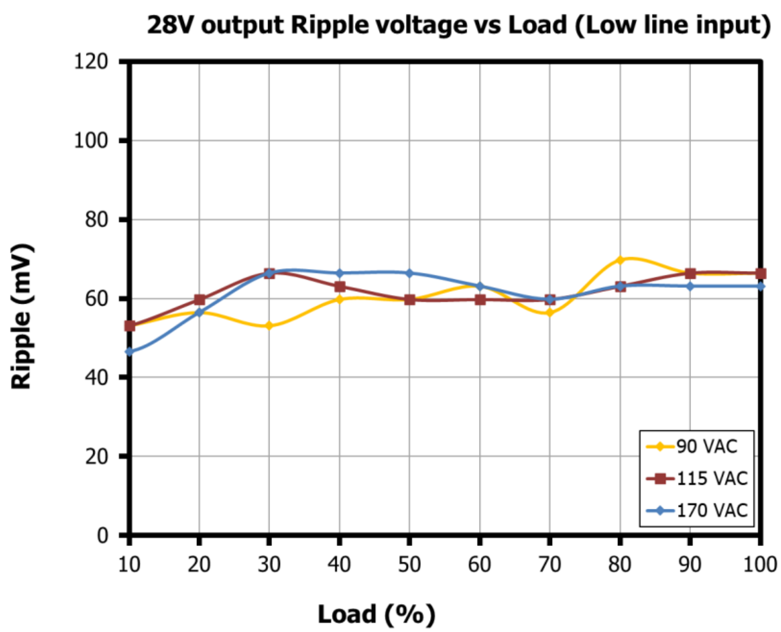


Figure 107 – 28 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

14 CV/CC Profile

CVCC profiles were recorded at room temperature with the output voltage measured on the board. The PIC microcontroller is configured such that the constant current limit of InnoSwitch5-Pro is set above the rated output current 5 A by +100 mA i.e. constant current limit is set to 5.1 A.

14.1 Output: 5 V / 5 A (High Line Input)

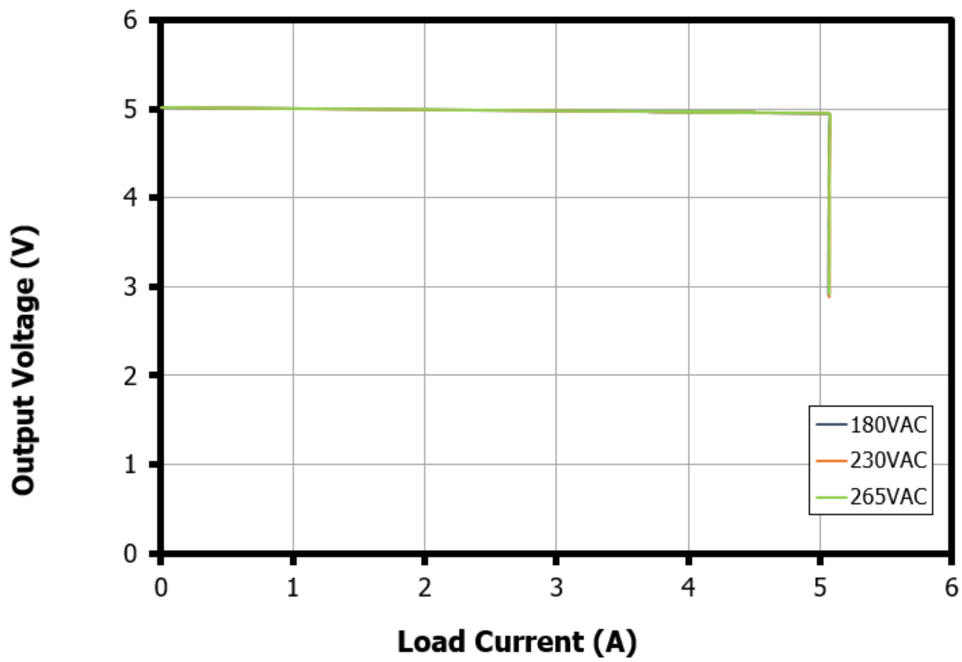


Figure 108 – CV/CC Profile with Output 5 V / 5 A, High Line Input.

14.2 Output: 20 V / 5 A (High Line Input)

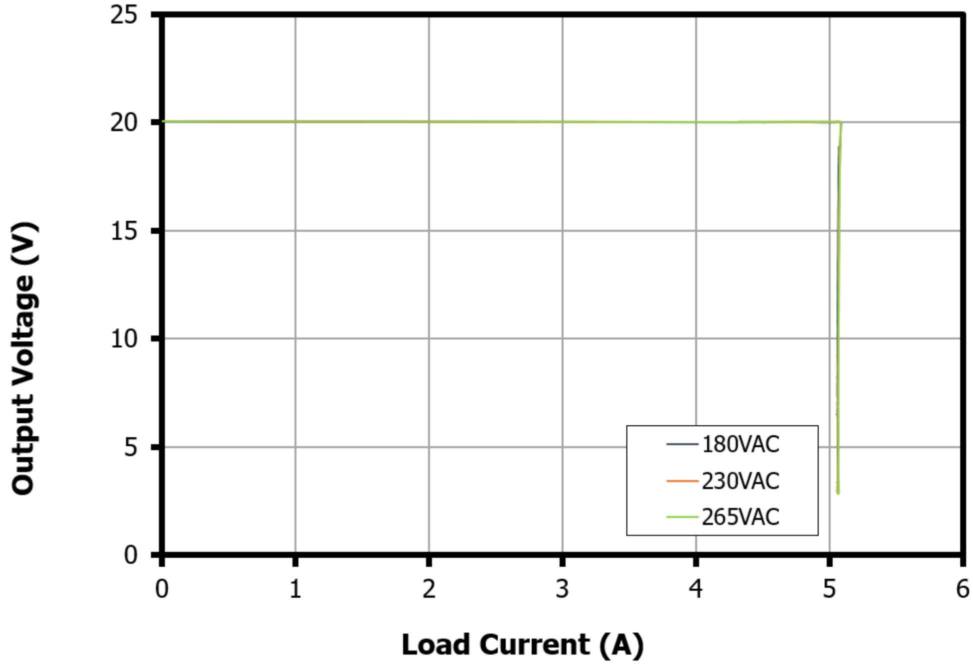


Figure 109 – CV/CC Profile with Output 20 V / 5 A, High Line Input.

14.3 Output: 28 V / 3.57 A (High Line Input)

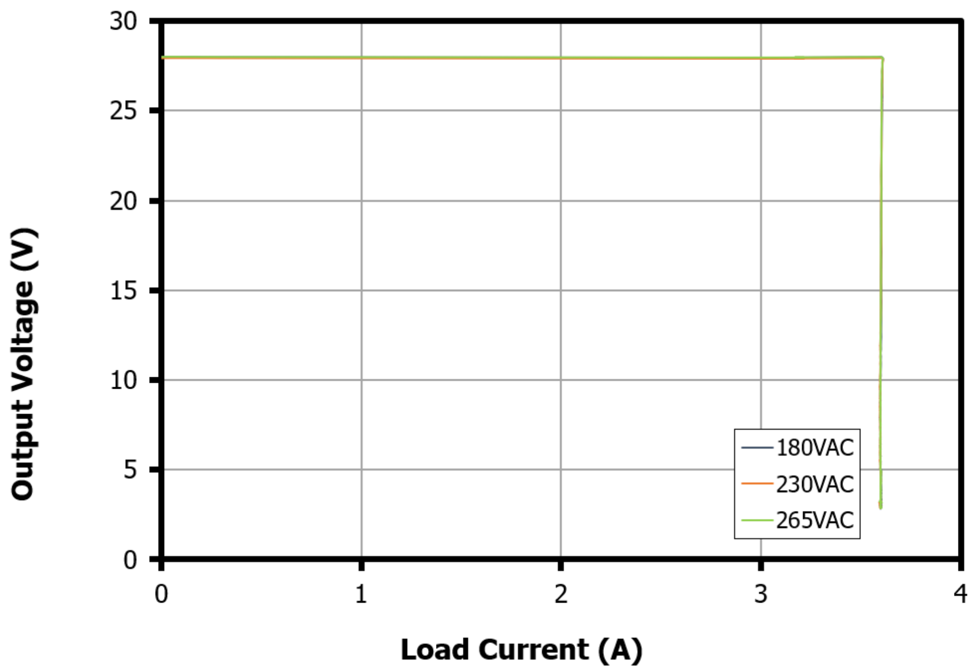


Figure 110 – CV/CC Profile with Output 28 V / 3.57 A, High Line Input.

14.4 Output: 5 V / 3.25 A (Low Line Input)

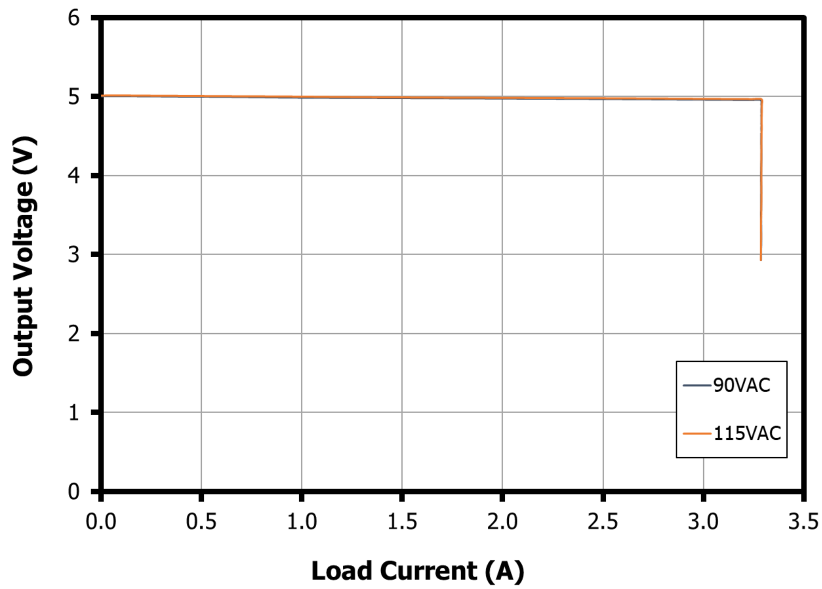


Figure 111 – CV/CC Profile with Output 5 V, 3.25 A.

14.5 Output: 20 V / 3.25 A (Low Line Input)

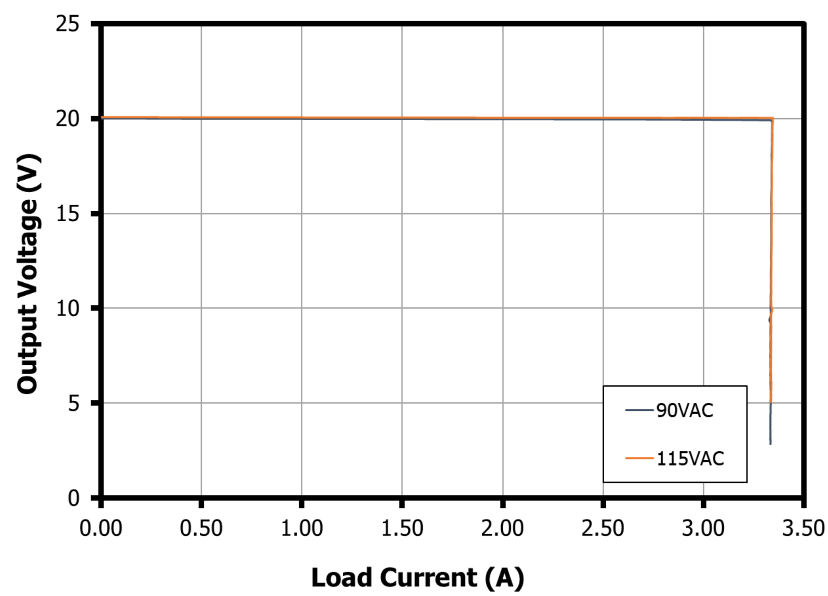


Figure 112 – CV/CC Profile with Output 20 V, 3.25 A.

14.6 Output: 28 V / 2.32 A (Low Line Input)

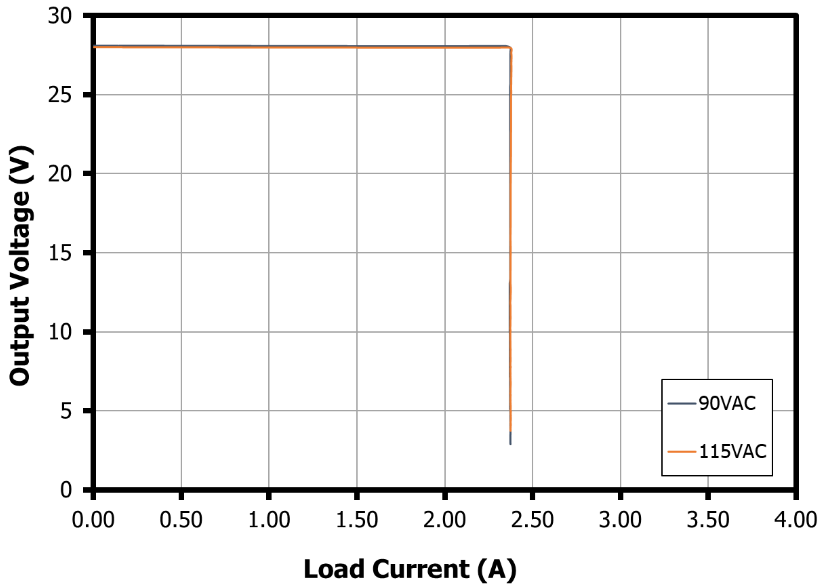


Figure 113 – CV/CC Profile with Output 28 V, 2.32 A.

15 Conducted EMI

15.1 Earth Floating (QPK / AV)

15.1.1 Output: 5 V / 5 A

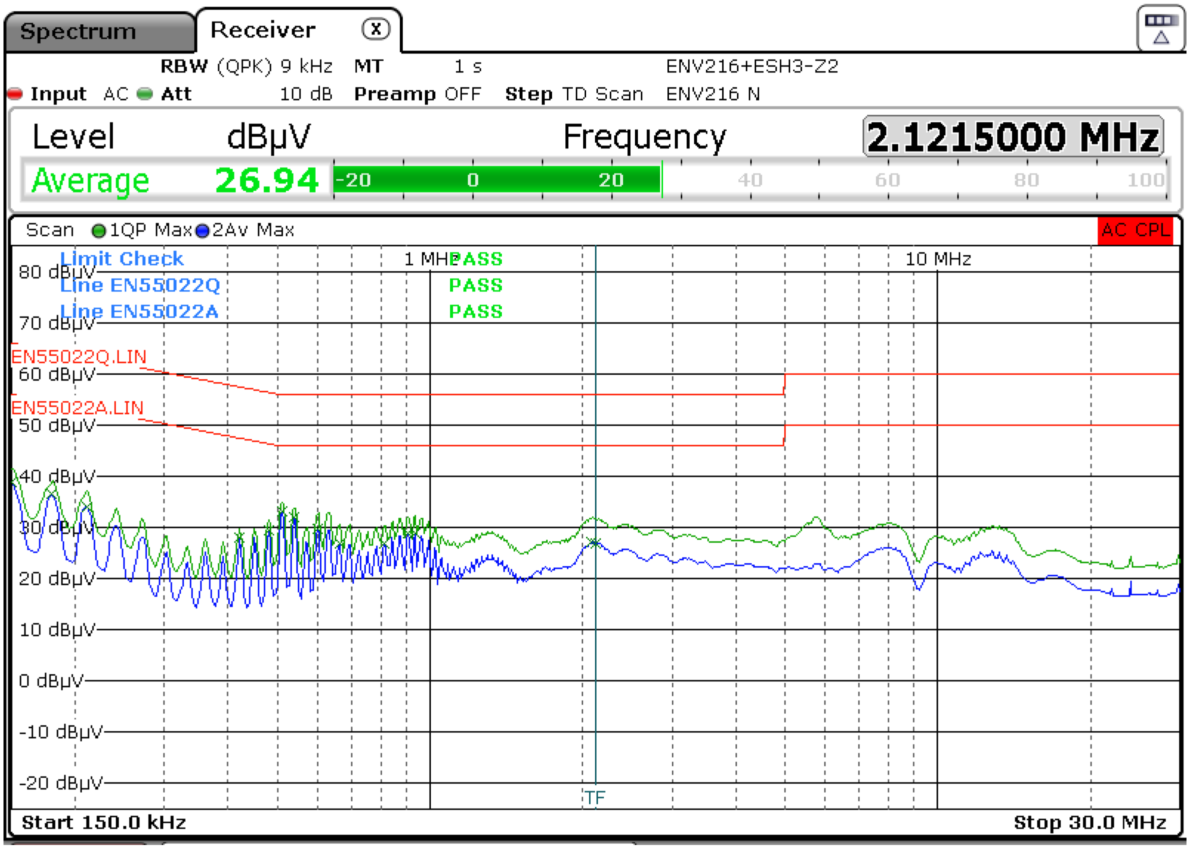


Figure 114 – Floating Ground EMI, 5 V / 5 A Load (Line/Neutral) @230VAC input

15.1.2 Output: 20 V / 5 A

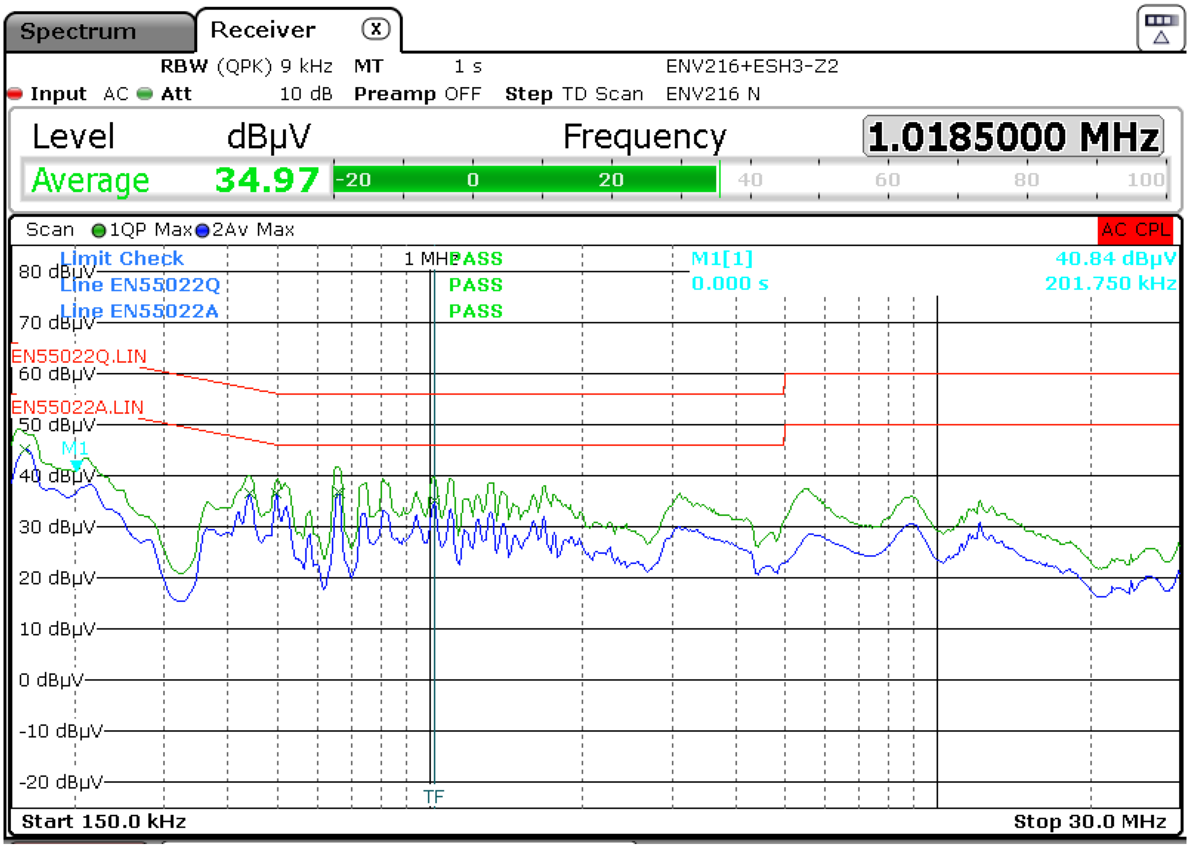


Figure 115 –Floating Ground EMI, 20 V / 5 A Load (Line/Neutral) @230VAC input

15.1.3 Output: 28 V / 3.57 A

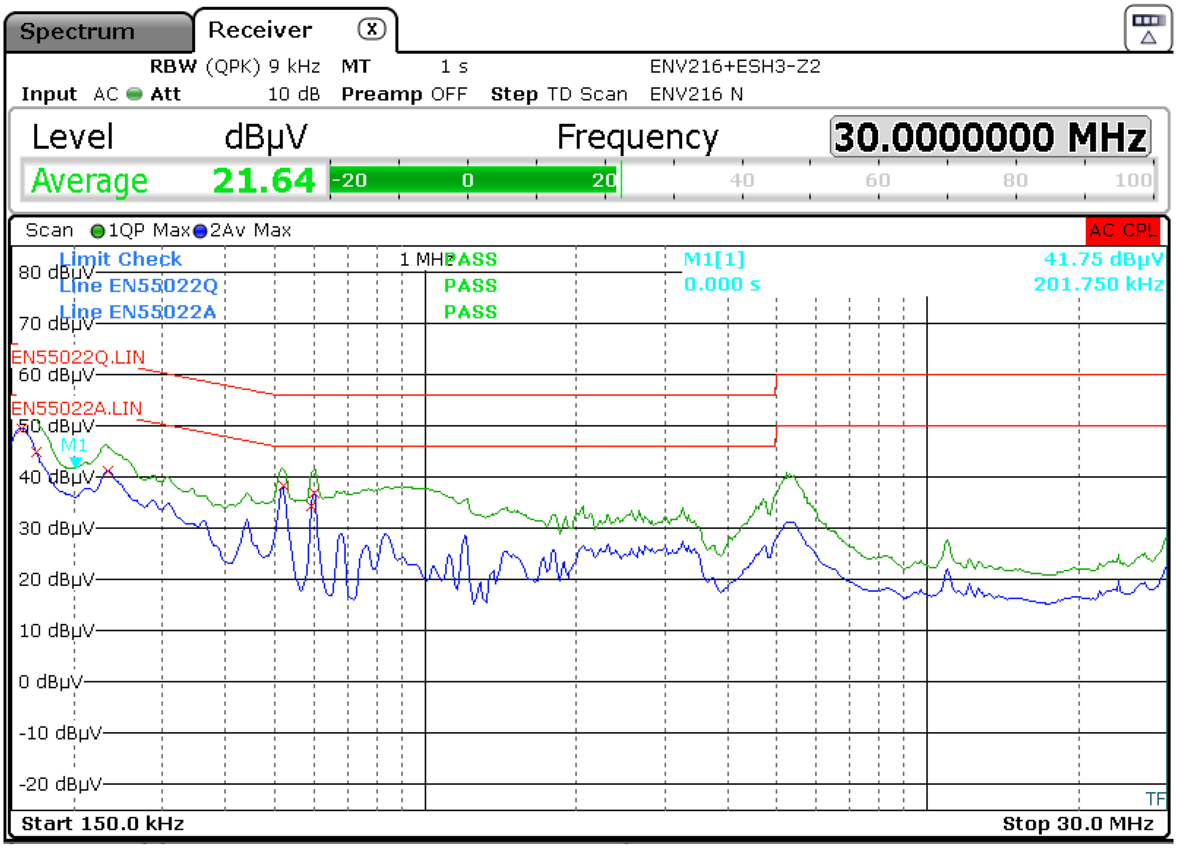


Figure 116 –Floating Ground EMI, 28 V / 3.57 A Load (Line/Neutral) @230VAC input

16 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination-wave and ring-wave surges at various line phase angles with 10 strikes for each condition. Note that AR might be observed due to line OV/UV protection mechanism being triggered during the test, which is a normal protection feature of the InnoSwitch5-Pro IC.

16.1 Differential Mode Surge (L1 to L2), 265 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 28 V / 3.57 A (Pass / Fail)
+1000	L1 to L2	0	Pass
-1000	L1 to L2	0	Pass
+1000	L1 to L2	90	Pass
-1000	L1 to L2	90	Pass
+1000	L1 to L2	180	Pass
-1000	L1 to L2	180	Pass
+1000	L1 to L2	270	Pass
-1000	L1 to L2	270	Pass

16.2 Common Mode Surge (L1 to PE), 265 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 28 V / 3.57 A (Pass / Fail)
+2000	L1 to PE	0	Pass
-2000	L1 to PE	0	Pass
+2000	L1 to PE	90	Pass
-2000	L1 to PE	90	Pass
+2000	L1 to PE	180	Pass
-2000	L1 to PE	180	Pass
+2000	L1 to PE	270	Pass
-2000	L1 to PE	270	Pass

16.3 Common Mode Surge (L2 to PE), 265 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 28 V / 3.57 A (Pass / Fail)
+2000	L2 to PE	0	Pass
-2000	L2 to PE	0	Pass
+2000	L2 to PE	90	Pass
-2000	L2 to PE	90	Pass
+2000	L2 to PE	180	Pass
-2000	L2 to PE	180	Pass
+2000	L2 to PE	270	Pass
-2000	L2 to PE	270	Pass

16.4 Common Mode Surge (L1, L2 to PE), 265 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 28 V / 3.57 A (Pass / Fail)
+2000	L1, L2 to PE	0	Pass
-2000	L1, L2 to PE	0	Pass
+2000	L1, L2 to PE	90	Pass
-2000	L1, L2 to PE	90	Pass
+2000	L1, L2 to PE	180	Pass
-2000	L1, L2 to PE	180	Pass
+2000	L1, L2 to PE	270	Pass
-2000	L1, L2 to PE	270	Pass

17 Electrostatic Discharge

The unit was tested with ±8.8 kV contact discharge and ±16.5 kV air discharge at the output VBUS, output GND, on-board, with 10 strikes for each condition. A test failure was defined as an interruption of output (latch-off) that needs operator intervention to recover, or a complete loss of function which is not recoverable.

17.1 Contact Discharge, 265 VAC Input

Discharge Voltage (kV)	ESD Strike Location (On Board)	Test Result 5 V / 0 A	Test Result 5 V / 5 A	Test Result 20 V / 5 A	Test Result 28 V / 0 A	Test Result 28 V / 3.57 A
+8.8	Output VBUS	Pass	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass	Pass
-8.8	Output VBUS	Pass	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass	Pass

17.2 Air Discharge, 265 VAC Input

Discharge Voltage (kV)	ESD Strike Location (On Board)	Test Result 5 V / 0 A	Test Result 5 V / 5 A	Test Result 20 V / 5 A	Test Result 28 V / 0 A	Test Result 28 V / 3.57 A
+16.5	Output VBUS	Pass	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass	Pass
-16.5	Output VBUS	Pass	Pass	Pass	Pass	Pass
	Output GND	Pass	Pass	Pass	Pass	Pass

18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
14-May-25	RK, SC	A	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

For patent information, Life support policy, trademark information and to access a list of Power Integrations worldwide Sales and engineering support locations and services, please use the links below.

https://www.power.com/company/sales/sales-offices