BridgeSwitch-2 Family

High-Voltage, Self-Powered, Half-bridge Motor Driver with Integrated Device Protection and System Monitoring

Product Highlights

Highest Performance and Design Flexibility

- Up to 99% efficient
  - Eliminates external heat sink at rated continuous RMS current
- 600 V N-channel power FREDFETs
  - Ultra-soft, fast recovery body-diode
- Controlled FREDFET switching speed reduces EMI
- Accurate instantaneous phase current information output (IPH)
  - Eliminates external sensing and amplification circuitry
- Self-biased low-side and high-side drivers
  - Eliminates need for auxiliary power supply
- Small footprint surface mount InSOP-24C package
  - Exposed pads enable efficient heat transfer to PCB
- Less than 4 mW power consumption from a 325 VDC bus in Sleep Mode when self-supplied
- Error Flag (EF) provides warning of severe system and device faults
- Reduced MCU I/O pin count through complementary PWM control with inverse logic INL and /INH control inputs
  - Option for active high INL and INH inputs

Safety and Reliability Features

- Adjustable cycle-by-cycle current limit for both FREDFETs
- Internal dual level thermal overload protection
- Self-configuring system level monitoring input
  - DC bus overvoltage and four level DC bus undervoltage
  - System temperature
- Adaptive dead time
- Simultaneous conduction lockout protection
- Selectable latching or hysteretic over-temperature and sustained over-current protection

Status Interface (FAULT)

- Bi-directional bussed open drain single wire interface
- Provides device specific status updates to system MCU
  - Successful power-up
  - Internal over-current or temperature faults
  - System level faults
- Status query through system MCU
- Device fault reset through system MCU

Applications

- 1 or 3-phase high-voltage PM and BLDC motor drives
- Appliances including dish washers, refrigerators and ceiling fans
- Fans in high efficiency air conditioners
- Circulation pumps

Description

The BridgeSwitch™-2 family of integrated half-bridge ICs dramatically simplifies the development and production of high-voltage motor drives. It incorporates two high-voltage N-channel power FREDFETs with low and high-side drivers in a single small-outline package. The internal power FREDFETs feature ultra-soft and ultra-fast body diodes ideally suited for hard switched inverter drives. Both drivers are self-supplied eliminating the need for an external auxiliary power supply. The low-profile, compact surface mount package offers extended creepage distances and allows heat sinking of both power FREDFETs through the printed circuit board.

BridgeSwitch-2 ICs provide a unique instantaneous phase current output signal simplifying implementation of sensorless control schemes.

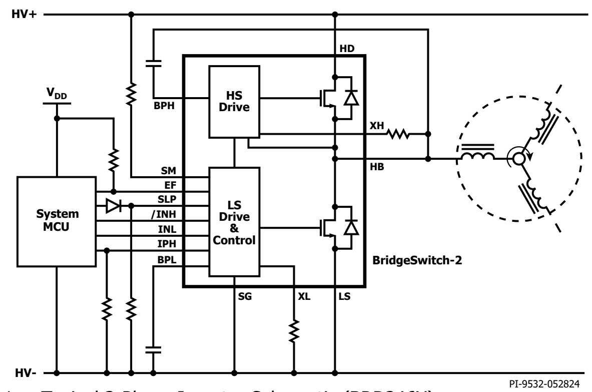


Figure 1. Typical 3-Phase Inverter Schematic (BRD246X).

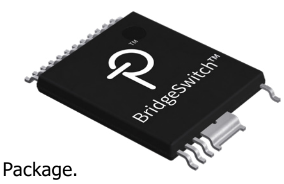


Figure 2. InSOP-24C Package.

Product Family

Product[3]	FREDFET DC Output Current[1]	Continuous Phase RMS Current[2]
BRD2x60C	1.0 A	0.22 A
BRD2x61C	1.7 A	0.50 A
BRD2x63C	3.0 A	0.75 A
BRD2x65C	5.5 A	1.00 A
BRD2x67C	11.5 A	1.33 A

Table 1. Phase Output Current Family Table.

Notes:

1. Continuous DC output current per FREDFET, calculated at 25 °C case and 125 °C junction temperature. Normally limited by internal circuitry.
2. Continuous phase RMS current, internal self-supply, 340 V bus, trapezoidal commutation with 10 kHz high-side PWM, PCB heat sinking with 50 °C case temperature rise.
3. Package. C: InSOP-24C.

Product Family	Reporting	IPH Current Information
BRD216x	FAULT & ID	-
BRD226x	FAULT & ID	Yes
BRD236x	EF	-
BRD246x	EF	Yes

Table 2. Product Family Functional Overview.

BridgeSwitch-2 offers internal fault protection and external system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two-level thermal overload protection. External system level monitoring includes DC bus sensing with four undervoltage levels and one overvoltage level as well as supporting external sensors such as an NTC. The bi-directional bussed single wire status interface reports observed status changes.

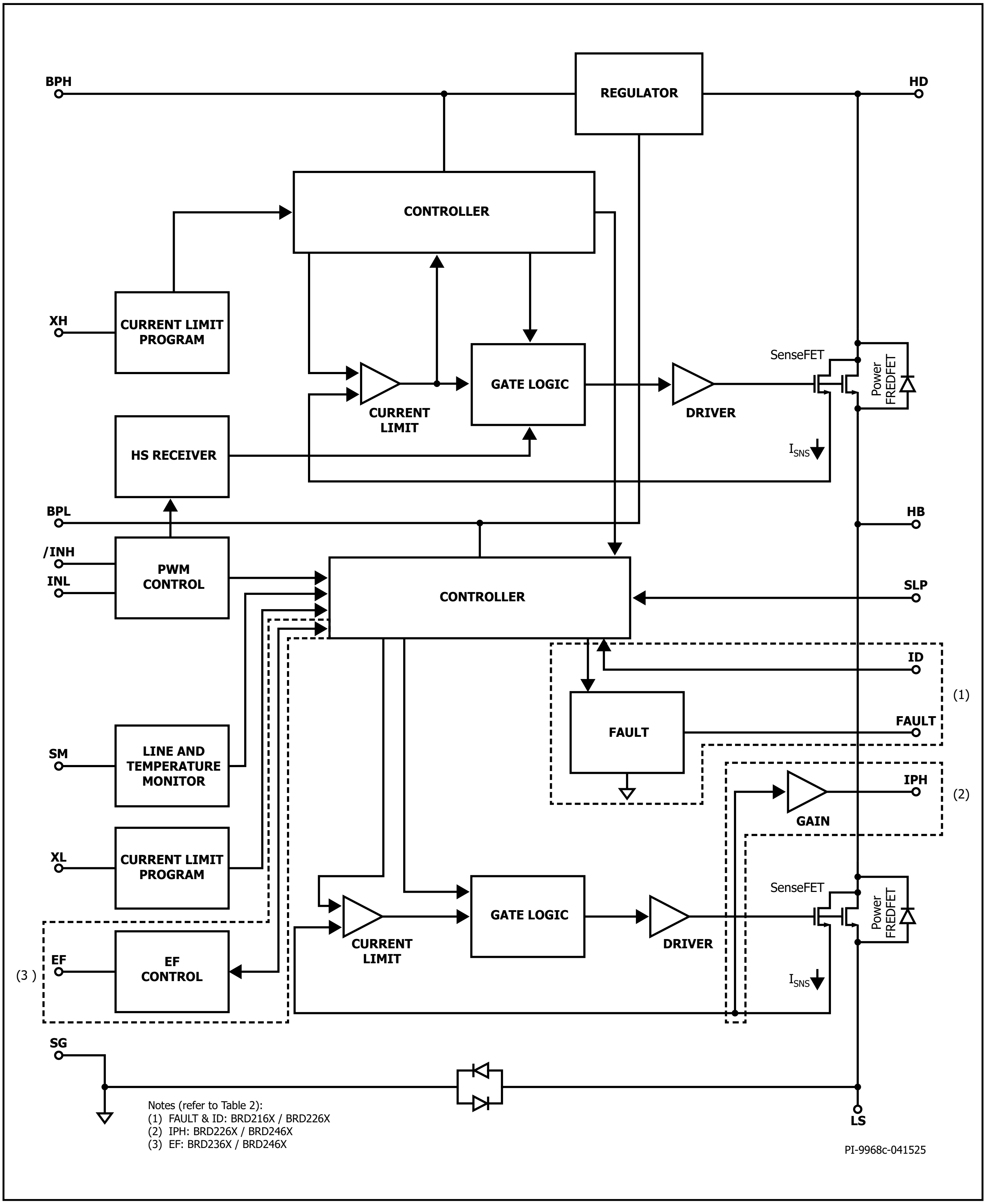


Figure 3. Functional Block Diagram BRD2X6X.

Pin Functional Description

HIGH-SIDE DRAIN (HD) Exposed Pad
The HD exposed pad is the electrical connection to the high-side power FREDFET Drain connection. It is also the input for the internal low-side and high-side self-supply circuitry.

EXTERNAL CURRENT LIMIT LOW-SIDE (XL) Pin (Pin 1)
This pin connects to a resistor to set the cycle-by-cycle current limit for the low-side power FREDFET.

PHASE CURRENT OUTPUT (IPH) Pin (Pin 2, BRD226X/ BRD246X)
This pin connects to a small signal resistor and provides low-side FREDFET Drain current information. The pin should be connected to SYSTEM GROUND if the function is not used. Function is not available with BRD216X/BRD236X.

SIGNAL GROUND (SG) Pin (Pins 3 and 10)
These pins are the ground reference connection for low-side controller small signal pins and the system micro-controller.

BYPASS LOW-SIDE (BPL) Pin (Pin 4)
This pin connects to the external bypass capacitor for the low-side controller and FREDFET Gate driver.

CONTROL INPUT LOW-SIDE (INL) Pin (Pin 5)
Active high logic level control input for the low-side power FREDFET.

CONTROL INPUT HIGH-SIDE (/INH or INH) Pin (Pin 6)
Active low logic level control (BRD2X6XC, default) or active high logic level control (BRD2X6XC-H450) input for the high-side power FREDFET.

STATUS COMMUNICATION (FAULT) Pin (Pin 7, BDR216X/ BDR226X)
This open Drain pin connects to an I/O port of the system micro-controller to provide a status update. The pin should be connected to SIGNAL GROUND if the function is not used.

SYSTEM MONITOR (SM) Pin (Pin 8)
This pin is a self-configuring system monitor input. It configures itself into a high-voltage bus sense input if a resistor is connected to the high-voltage bus at power-up. It configures itself into an external temperature sense input if a resistance is connected to SYSTEM GROUND at power-up. The pin should be connected to SYSTEM GROUND if the function is not used.

SLEEP MODE AND PROGRAMMING (SLP) Pin (Pin 9)
This pin is the control input for entering the device into a deep sleep mode. An external programming resistor is used to select either hysteretic or latching shutdown protection during over-temperature or sustained over-current faults. This pin should be left floating if the sleep mode and programming functions are not used.

DEVICE ID (ID) Pin (Pin 11 BRD216X/BRD226X)
This pin programs the device ID at power-up. This pin should be left floating if the function is not used.

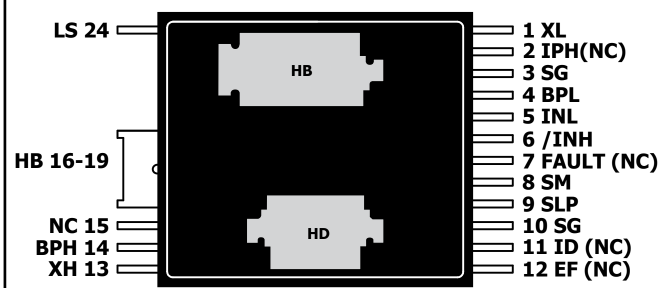


Figure 4. Pin Configuration for C Package (InSOP-24C) (Bottom View).

ERROR FLAG (EF) Pin (Pin 12, BRD236X/BRD246X)
This open DRAIN pin flags severe device level faults. It also serves as a reset signal input for optionally selected latching shutdown protection. This pin should be left floating if the functions are not used.

EXTERNAL CURRENT LIMIT HIGH-SIDE (XH) Pin (Pin 13)
This pin connects to a resistor to set the cycle-by-cycle current limit for the high-side power FREDFET. The resistor is referenced to the HALF BRIDGE CONNECTION.

BYPASS HIGH-SIDE (BPH) Pin (Pin 14)
This pin connects to the external bypass capacitor for the high-side FREDFET Gate driver. The capacitor is referenced to the HALF BRIDGE CONNECTION.

HALF-BRIDGE CONNECTION (HB) (Pin 16-19)
This pin connects to the node formed by the Source of the high-side power FREDFET and to the Drain of the low-side power FREDFET. It is also the reference for the BYPASS HIGH-SIDE and the EXTERNAL CURRENT LIMIT HIGH-SIDE pins.

LOW-SIDE SOURCE (LS) (Pin 24)
This pin is the low-side power FREDFET Source connection. It connects to the SIGNAL GROUND through a Kelvin connection.

NOT CONNECTED (NC) Pins
BRD216X - Pin 2, Pin 12 and Pin 15
BRD226X - Pin 12 and Pin 15
BRD236X - Pin 2, Pin 7,Pin 11 and Pin 15
BRD246X - Pin 7, Pin 11 and Pin 15

These NC pins are not connected and should be left floating.

BridgeSwitch-2 Functional Description

BridgeSwitch-2 combines two high-voltage power FREDFETs, gate drivers and controllers into a single package. The FREDFETs are connected in a half-bridge configuration where their body-diode structure (ultra-soft and ultra-fast recovery) makes them ideal for hard-switched inverter-based motor drivers.

To reduce external components, the drive controllers feature integrated high-voltage current sources, allowing them to draw current directly from the high-voltage DC Bus. The high-side controller provides status update to the low-side controller which generates an instantaneous phase-current output signal (BRD226X/BRD246X). This unique capability allows the implementation of a sensorless motor control scheme. The controllers also ensure that the FREDFET turn-off is faster than turn-on resulting in an optimal balance between thermal performance and EMI.

BridgeSwitch-2 offers integrated fault protection and system level monitoring via a bi-directional single-wire status interface bus. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs as well as two-level thermal overload protection. BridgeSwitch-2 offers sophisticated DC-bus sensing, providing four undervoltage levels and one overvoltage level, and can also support external sensors such as an NTC. Figures 3 shows the functional block diagram of the device along with key features.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pin Regulator

When self-supplied, the LOW-SIDE BYPASS (BPL) and the HIGH-SIDE BYPASS (BPH) pins have internal regulators that charge the C_{BPL} and C_{BPH} capacitors to V_{BPL} and V_{BPH} voltages respectively. A current source connected to HIGH-SIDE DRAIN (HD) pad charges the C_{BPL} capacitor. Another current source connected to HD pad charges the C_{BPH} capacitor whenever the low-side FREDFET turns on.

Both current sources start charging once the HD pad voltage reaches $V_{HD(START)}$ (min. 50 V). The BPL and BPH pins are the internal supply voltage nodes for the low-side and high-side controllers as well as gate drivers. When the low-side or high-side FREDFETs are on, the device operates from the energy stored in the C_{BPL} pin capacitor or the C_{BPH} capacitor, respectively.

Internal shunt regulators clamp the BPL pin to $V_{BPL(SHUNT)}$ and the BPH pin to $V_{BPH(SHUNT)}$ when current is provided to the BPL and BP pins from an external DC source through resistors R_{SL} and R_{SH} (see Figure 5).

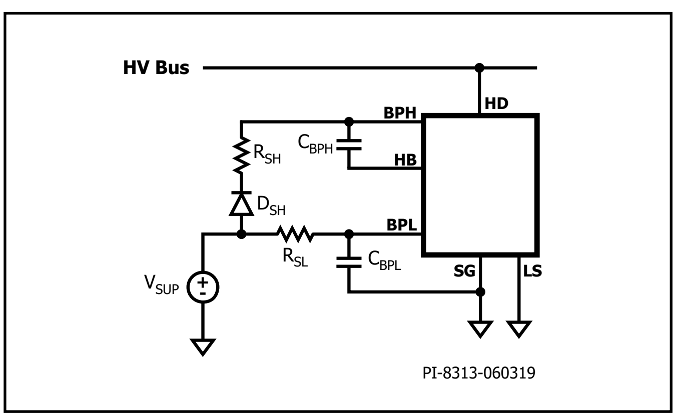


Figure 5. External BPL Pin and BPH Pin Power Supply Example.

External supply voltage V_{SUP} is greater than bypass shunt regulator voltage $V_{BPX(SHUNT)}$ plus the voltage drop of the bootstrap diode D_{SH}. A typical value is V_{SUP} = 15 V. Resistors R_{SL} and R_{SH} limit the external supply current to less than 12 mA (1.5 mA recommended). Connecting BPL or BPH pins from separate devices is not recommended. External supply mode operation is recommended for PWM frequencies above 20 kHz.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pin Undervoltage Threshold

The BPL and BPH pin undervoltage circuits disable the respective power FREDFET when either the BPL or BPH pin voltage drops below V_{BPL}-$V_{BPL(HYST)}$ or V_{BPH}-$V_{BPH(HYST)}$ respectively during steady-state operation. If either the BPL or BPH pin voltage falls below this threshold, it must rise back up to V_{BPL} or V_{BPH} respectively to enable power FREDFET switching.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pins Capacitor Selection

Capacitors connected to the BYPASS LOW-SIDE pin and BYPASS HIGH-SIDE pin supply bias current for the low-side and the high-side controller and deliver the required Gate charge for turning on the low-side or the high-side power FREDFET. The BYPASS HIGH-SIDE pin capacitor supplies the high-side controller bias current over a time interval which is a function of the high-side commutation duty ratio and the PWM frequency. The recommended maximum voltage ripple on the BYPASS HIGH-SIDE pin capacitor over this time interval is 250 mV. The minimum required capacitance value for both bypass low-side and bypass high-side is 1 μF. The recommended bypass low-side capacitance is 1 μF.

Application operating conditions determine the required BYPASS HIGH-SIDE capacitance to keep ripple voltage below 250 mV. Figure 6 depicts the minimum recommended BYPASS HIGH-SIDE pin capacitance as function of high-side commutation duty ratio D_{HS} and PWM frequency.

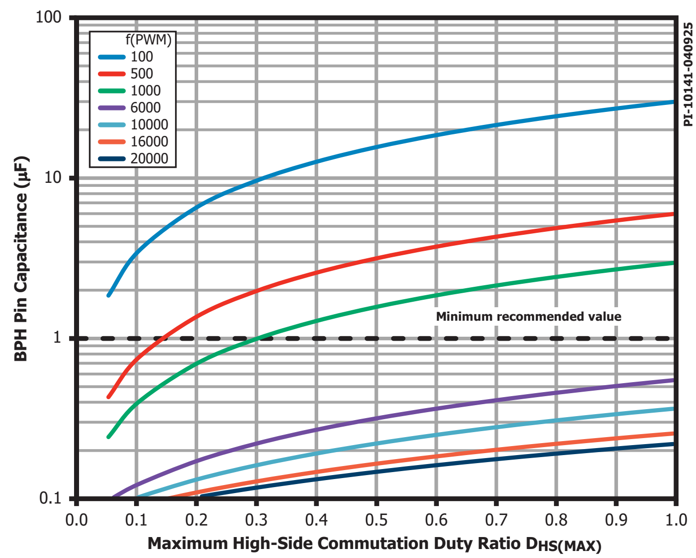


Figure 6. BYPASS HIGH-SIDE Pin Capacitance vs. High-Side Commutation Duty Ratio and PWM Frequency.

Note that multilayer chip capacitors (MLCC) can exhibit a significant DC bias characteristic. Selecting a BYPASS HIGH-SIDE pin capacitor (according to Figure 6) needs to take into account the possible capacitance reduction when biasing at V_{BPH}. Refer to the respective capacitor data sheet for details.

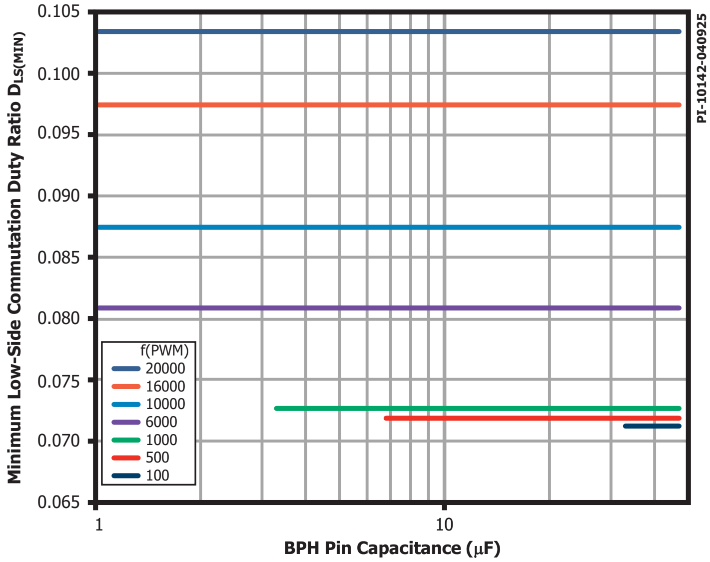


Figure 7. Minimum Low-Side Commutation Duty Ratio vs. BYPASS HIGH-SIDE Pin Capacitance and Low-Side PWM Frequency to Ensure Sufficient High-Side Self-Supply Current (High-Side Commutation Duty Ratio ≤ 0.90).

The capacitor on the BYPASS HIGH-SIDE pin recharges every time the low-side power FREDFET turns on. To ensure sufficient high-side self-supply current, the low-side power FREDFET on-time (a function of chosen bypass high-side capacitance, low-side commutation duty ratio D_{LS} and PWM frequency), should meet the minimum low-side commutation duty ratio requirement $D_{LS(MIN)}$ shown in Figure 7. The maximum recommended voltage ripple of 250 mV across the high-side bypass capacitor limits the minimum capacitance at lower PWM frequencies.

The minimum low-side commutation duty ratio $D_{LS(MIN)}$ depicted in Figure 7 scales with the applicable maximum high-side commutation duty ratio. For example, the minimum low-side commutation duty ratio $D_{LS(MIN)}$ in an application operating at f_{PWM} = 6 kHz and a maximum high-side commutation duty ratio of $D_{HS(MAX)}$ = 0.90 is $D_{LS(MIN)}$ = 0.072. If the same application operates at a maximum high-side duty ratio of $D^*_{HS(MAX)}$ = 0.95, then the $D_{LS(MIN)}$ increases by a factor of 0.95/0.90, making the new value of $D^*_{LS(MIN)}$ = 0.076.

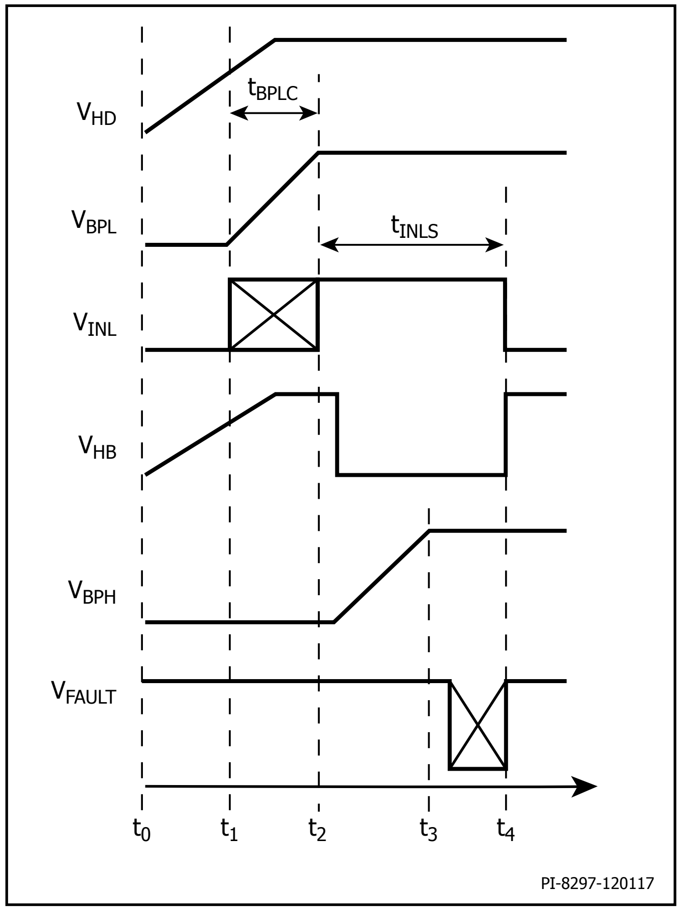


Figure 8. Recommended Power-Up Sequence with Self-supplied Operation.

Time Point	Activity
t_0	• High-voltage DC bus is applied
t_1	• Internal current source starts charging BPL pin capacitor once HD pin voltage reaches $V_{HD(START)}$ • System MCU may start setting low-side power FREDFET control signal INL to high
t_2	• BPL pin voltage reaches V_{BPL} (typically 12.8 V) • Device determines external device settings • Internal Gate drive logic turns on low-side power FREDFET after device setup completes and once INL becomes high or if it is high already • Internal current source starts charging BPH pin capacitor
t_3	• BPH pin voltage reaches V_{BPH} with respect to HB pin (typically 12.8 V) • Device starts communicating successful power-up through FAULT pin Note: The device does not send a status update if the internal power-up sequence did not complete successfully.
t_4	• BridgeSwitch-2 is ready for steady-state operation (indicated by communicated status update starting at time point t_3) • System MCU turns off low-side power FREDFET

Table 3. Power-Up Sequence with Self-Supplied Operation.

Power-Up Sequence with Self-Supply

For commutation BridgeSwitch-2 devices have self-supply which supports PWM frequencies of up to 20 kHz. For operation at PWM frequencies above 20 kHz, it is recommended that an external supply such as that shown in Figure 5 be used. To ensure that sufficient voltage appears across the BYPASS LOW-SIDE pin capacitor and the BYPASS HIGH-SIDE pin capacitor at inverter start-up, the system micro-controller (MCU) should follow the power-up sequence depicted in Figure 8.

Table 3 lists activities occurring during the recommended power-up sequence.

The BYPASS LOW-SIDE pin capacitor C_{BPL}, the BPL pin charge current $I_{CH1(LS)}$, and the BYPASS LOW-SIDE pin voltage V_{BPL} determine the charging time t_{BPLC} starting at time point t_1 (Figure 8):

$$t_{BPLC} = t_2 - t_1 = \frac{C_{BPL} \times V_{BPL}}{I_{CH1(LS)}}$$

The system MCU manages the power-up sequence by controlling the time point t_2 and duration t_{INLS} for turning the low-side power FREDFET on and off. The MCU may pull the INL pin high any time after the full DC bus voltage is available (from time point t_1). However, the BridgeSwitch IC enables power MOSFET switching only after the BYPASS LOW-SIDE pin voltages reaches V_{BPL} (typically 12.8 V) and setup completes.

A minimum on-time for the low-side FREDFET (t_{INLS}) is required to ensure sufficient charging of the BPH pin capacitor, to allow for device set-up, and to permit the completion of a status update via the FAULT pin. It is controlled by the system MCU and depends on the capacitance C_{BPH}:

$$t_{INLS} = t_4 - t_2 \geq \frac{C_{BPH} \times V_{BPH}}{I_{CH1(HS)}} + 1\,\text{ms}$$

This power-up sequence should also be followed after a latching shutdown, when in order to restart, the MCU sends a FAULT latch reset command (see Table 10 for details).

Gate Drive Control Inputs

The low-side and high-side power FREDFETs are controlled through INL and /INH logic inputs. Both inputs are compatible with 3.3 V and 5 V CMOS logic levels. The low-side power FREDFET is edge-triggered and latches on or off by transitions of the high INL signal during steady-state operation. In a similar fashion the high-side power FREDFET is controlled by the active low /INH signal. The INL input has an internal weak pull-down and the /INH input has an internal weak pull-up. This prevents accidental power FREDFET turn-on in the event that one or both control inputs are floating.

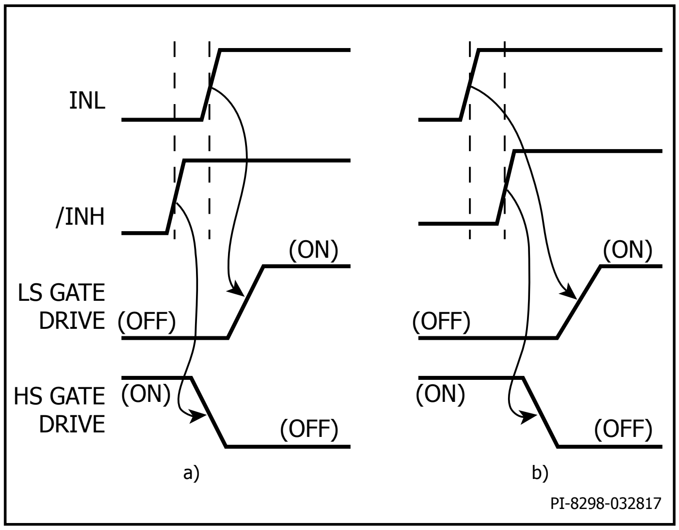


Figure 9. Simultaneous Conduction Lockout a) Not Active b) Active.

BridgeSwitch-2 provides simultaneous-conduction lockout protection. A latch inhibits turn-on of the low-side power FREDFET Gate drive circuit until the rising edge of the high-side control signal /INH has occurred (see Figure 9). The latch also inhibits turn-on of the high-side power FREDFET Gate drive circuitry until the falling edge of the low-side control signal INL has occurred.

The inverse logic polarity of INL and /INH control inputs allows the option to tie both together in order to control both power FREDFETs with a single PWM signal. To prevent the possibility of FREDFET cross conduction, the integrated Gate-drive circuit inserts dead times as shown in Figure 10. The falling edge of the low-side power FREDFET control input INL reaching 50% of its initial value triggers the t_{DLH} timer (Dead-Time low-side power FREDFET off to high-side power FREDFET on). The integrated Gate control logic enables turning on the high-side FREDFET Gate drive only after t_{DLH} expires. The rising edge of the high-side power FREDFET control input /INH reaching 50% of its final value triggers the t_{DHL} timer (Dead Time high-side power FREDFET off to low-side power FREDFET on). The integrated Gate control logic enables turning on of the low-side FREDFET Gate drive only after t_{DHL} expires.

Devices with active high INL and INH control inputs are optionally available as feature code H450 (refer to page 33). If active low is required, no feature code is necessary.

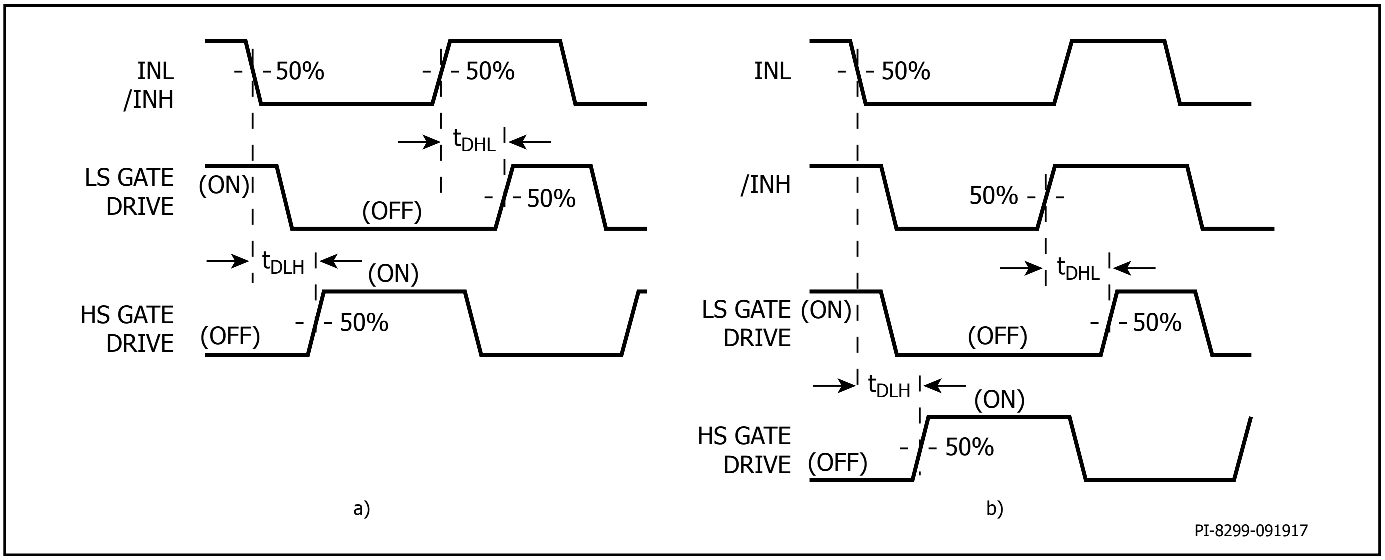


Figure 10. Adaptive Dead Time a) INL and /INH Inputs Tied Together b) INL and /INH Inputs Separate.

Device Internal High-Side Status Update

The BridgeSwitch-2 high-side controller provides status updates to the low-side controller. The status update reports triggering of device level protection such as high-side power FREDFET over current or low-side power FREDFET over-temperature WARNING or shutdown. Status update also includes device faults such as XH pin short or open circuit and loss of high-side power. The high-side controller provides an internal status update every time the low-side power FREDFET turns on. To ensure correct internal status updates, the system micro-controller must to set the INL control input high for at least $t_{INLH(COM)}$ (see Figure 25 for details). INL input turn-on control signals shorter than $t_{INHL(COM)}$ may cause incomplete internal status updates followed by the device reporting a "HS Driver not ready" status update (see Table 7).

Adjustable Cycle-by-Cycle Current Limit

BridgeSwitch-2 devices feature cycle-by-cycle current limit protection for both, the low-side and the high-side power FREDFET. As soon as the power FREDFET current exceeds the respective current limit level threshold and after the leading edge blanking timer t_{LEB} expires, the device turns off the power FREDFET. The FREDFET stays off until a turn-off edge followed by a turn-on edge is received at the respective INL or /INH control input. The device will also report the corresponding over-current fault either through the FAULT pin (BRD216X/BRD226X, see Table 7 for details) or the EF pin (BRD236X/BRD246X, see Table 11 for details).

The current limit level is set at device power-up by the value of the external small signal resistors R_{XL} and R_{XH} (see Figure 1) connected to either the XL pin and to the XH pin respectively. Programming voltage levels at XL and XH pins are internally pulled to SG or HB, respectively, once the device is ready for steady-state operation (refer to time point t_4 in Figure 8).

Table 4 shows the relationship between the resistor connected to the XL pin or XH pin and the selected current limit threshold level normalized to the default current limit level $I_{LIM(DEF)}$.

A resistor connected to the SLP pin (refer to Table 6) allows changing the default cycle-by-cycle handling of sustained low-side FREDFET over-current faults to a latching shutdown when the BridgeSwitch-2 IC detects sixteen consecutive switch cycles that each trigger over-current protection. After the device has entered the optionally programmed sustained over-current latching shutdown mode, the system MCU can re-enable FREDFET switching by sending the fault-latch-reset command through the FAULT bus (BRD216X/BRD226X, see Table 10 for details) or by pulling the ERROR FLAG bus high (BRD236X/BRD246X, see Figure 21 and 22 for details). Alternatively operation may resume after a full power-up sequence initiated by the system MCU.

R_{XL}/R_{XH} (kΩ)[2]	$I_{LIMIT(NORM)}$	R_{XL}/R_{XH} (kΩ)[2]	$I_{LIMIT(NORM)}$
≤20[1]	Fault	280	0.68 × $I_{LIM(DEF)}$
42.2	1.00 × $I_{LIM(DEF)}$	442	0.60 × $I_{LIM(DEF)}$
68.1	0.92 × $I_{LIM(DEF)}$	806	0.52 × $I_{LIM(DEF)}$
110	0.84 × $I_{LIM(DEF)}$	Open	$I_{LIM(MIN)}$
174	0.76 × $I_{LIM(DEF)}$		

Table 4. Current Limit Selection.

Notes:

1. Constitutes XL/XH pin short-circuit fault, device inhibits switching.
2. The recommended resistance tolerance is ±1%.

FREDFET switching is disabled for R_{XL} or R_{XH} values smaller than 20 kΩ which causes the BridgeSwitch IC to provide either a LS driver not ready or a HS driver not ready status update through the FAULT pin (refer to Table 6). This prevents inverter malfunction in the event that the programming resistor is accidentally short-circuited. The device continues to accept LS FREDFET turn-on signals in case it detects a short-circuit at the XH pin. A detected short-circuit at the XL pin will eventually cause the HS FREDFET switching to cease operation as well because the BPH pin capacitor is only re-charged when the LS FREDFET turns on. The device selects the lowest current limit threshold when the XL pin or XH pin is left floating.

Connecting capacitors to the XL pin or XH pin is not recommended.

Device Over-Temperature Protection

BridgeSwitch-2 devices feature integrated dual level thermal overload protection. The device monitors the temperature of the low-side power FREDFET. It will send a status update through the STATUS COMMUNICATION pin (BRD216X/BRD226X) as soon as the low-side FREDFET reaches the lower Device Warning Temperature level T_{WA} (see Table 7 for details). Depending on the fault handling mode selected on the SLP pin (refer to Table 6), the device either disables FREDFET switching permanently once the FREDFET temperature exceeds the Device Shutdown Temperature threshold T_{SD} or enters a hysteretic shutdown mode to prevent device damage. Devices configured for hysteretic shutdown mode automatically re-enable switching when the FREDFET temperature has dropped to the thermal shutdown restart temperature $T_{RES(H)}$.

In addition, the BridgeSwitch IC will either report the over-temperature fault through the FAULT pin (BRD216X/BRD226X) or flag the fault on the EF pin (BRD236X/BRD246X). System level monitoring through the SYSTEM MONITOR pin continues and the device will report any additional status changes through the STATUS COMMUNICATION pin. The system MCU can re-enable FREDFET switching by sending the fault-latch-reset command through the FAULT bus (BRD216X/BRD226X, see Table 9 for details) or by pulling the ERROR FLAG bus high (BRD236X/ BRD246X, see Figures 21 and 22 for details). Alternatively operation may resume after a full power-up sequence initiated by the system MCU.

Phase Current Information Output

BridgeSwitch-2 BRD226X and BRD246X devices feature instantaneous motor winding phase current information through a resistor connected to the PHASE CURRENT OUTPUT pin as shown in Figure 11. The voltage across the small signal resistor is an analog representation of the low-side power FREDFET Drain to Source channel current. The system MCU can digitize this voltage and use it (for example) as an input to a motor control algorithm. The device supports independent phase current information through individual IPH pin resistors as shown in Figure 11.

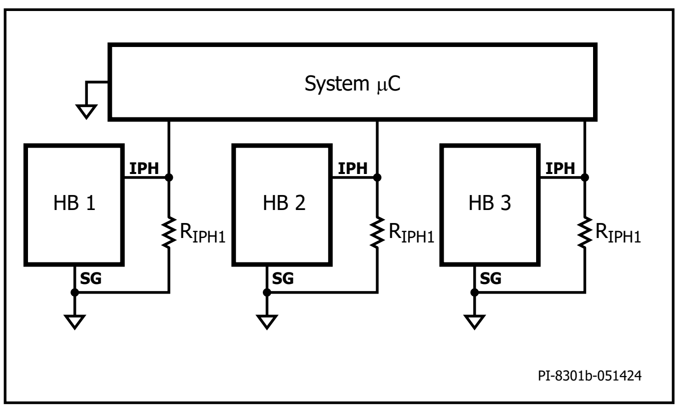


Figure 11. Phase Current Information through IPH Pin with BRD226X and BRD246X.

The Phase Current Output Gain g_{IPH} and the resistor R_{IPH} connected to the PHASE CURRENT OUTPUT determine the voltage amplitude V_{IPH} at a given phase current I_{PHASE}:

$$V_{IPH} = R_{IPH} \times I_{PHASE} \times g_{IPH}$$

Maximum permissible voltage amplitude of V_{IPH} is 3.0 V.

External Current Sensing

All BridgeSwitch-2 devices support discrete low-side FREDFET current sensing through an external current sense resistor in series with the LS pin. Figure 12 depicts an example of one possible implementation.

Voltage V_{SHUNT} is a direct representation of the motor winding current I_{MOTOR}. Resistor R1 and R2 set the gain of external amplifier U1. Resistor R3, C1, C2, and C3 provide noise filtering. Resistor R4 adds a DC offset V_{OFFSET} to the amplifier U1 output signal V_{OP}.

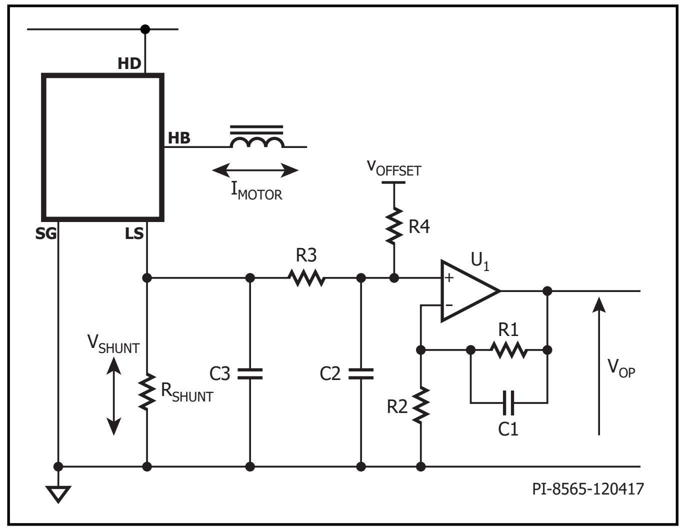


Figure 12. Example of External Current Sense Circuit.

$$V_{OP} = \left(1 + \frac{R1}{R2}\right)\frac{V_{OFFSET} \times R3 + I_{MOTOR} \times R_{SHUNT} \times R4}{R3 + R4}$$

The voltage differential V_{SHUNT} between SG and LS pins should not exceed ±0.33 V. Current sense resistor R_{SHUNT} in series with the LS pin should be sized appropriately to achieve this.

System Monitor Input

BridgeSwitch-2 provides system level status updates through the SYSTEM MONITOR input. The SM pin can be used to track either the high-voltage (HV) DC bus voltage (see Figure 13) or the temperature of an external component through an NTC thermistor (see Figure 15). The SM pin is self-configuring. It automatically detects the type of external connection and adopts the appropriate circuit configuration at power-up.

High-Voltage DC Bus Monitoring

The SYSTEM MONITOR pin continuously monitors the high-voltage DC bus voltage level by sensing the current into this pin. The current I_{SM} into the SM pin is a representation of the high-voltage bus voltage level V_{BUS}:

$$I_{SM} = \frac{V_{BUS} - V_{SM}}{R_{HV1}}$$

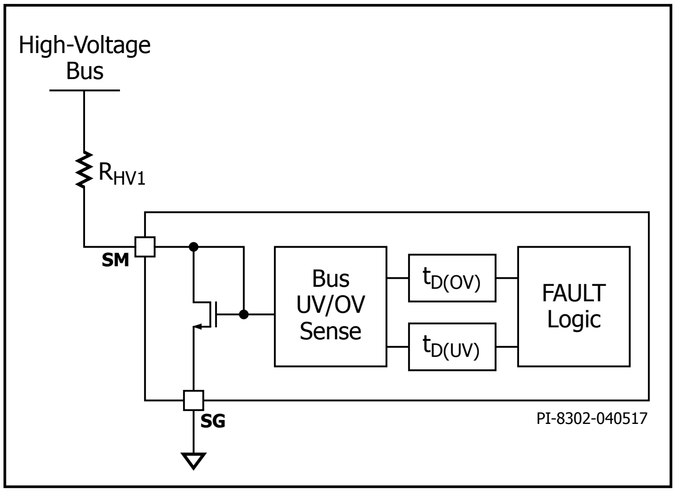


Figure 13. High-Voltage Bus Monitoring with SYSTEM MONITOR Pin.

The bus voltage sensing circuitry has five distinct current thresholds as shown in Figure 14. Thresholds I_{UV55}, I_{UV70}, I_{UV85}, and I_{UV100} are used to detect high-voltage-bus undervoltage conditions. Threshold I_{OV} is used to detect a high-voltage bus overvoltage condition. The device reports a high-voltage bus fault through the STATUS COMMUNICATION pin any time the current into the SM pin either drops below one of the four undervoltage thresholds or exceeds the overvoltage threshold (see Table 7 for details).

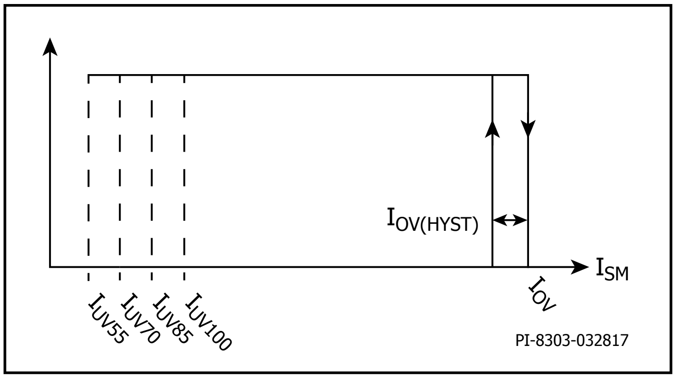


Figure 14. System Monitor Input Current Thresholds.

An undervoltage condition has to be present for at least $t_{D(UV)}$ (typically 40 ms) before it is reported to the system MCU. The device also reports if a given undervoltage condition clears for at least $t_{D(UV)}$.

Note: during a bus brown-out condition, the device will report (for example a UV 70% status update) if the bus voltage falls below 177 V for at least $t_{D(UV)}$ with a 7 MΩ sensing resistance (refer to Tables 5 and 7). If in this example the bus voltage recovers and rises above 177 V for at least $t_{D(UV)}$, the UV 70% condition clears and the device will provide a UV 85% status update.

If the SM pin current exceeds I_{OV} for at least $t_{D(OV)}$ (typically 80 µs), BridgeSwitch-2 terminates the current low-side or high-side power FREDFET on-time and reports the fault to the system MCU through the FAULT pin. It ignores any subsequent FREDFET turn-on signals received at either INL or /INH until the SM pin current has dropped by at least $I_{OV(HYST)}$ for the duration $t_{D(OV)}$. The FAULT pin provides a status update once the high voltage bus overvoltage condition has cleared.

The system MCU may decide to stop sending turn-on signals to other BridgeSwitch-2 devices in the inverter while the bus OV condition is asserted. This may cause the high-side BYPASS pin capacitors to discharge due to the disablement of the low side FREDFET during the bus OV fault. It is therefore recommended that a full power up sequence is initiated after the fault is cleared. Table 5 lists nominal high-voltage bus monitoring thresholds with three different sensing resistor R_{HV1} values

Sensing Resistor R_{HV1}	6 MΩ	7 MΩ	8 MΩ
	Bus Voltage UV or OV Threshold		
I_{OV} (typically 60 µA)	362 V	422 V	482 V
I_{UV100} (typically 35 µA)	212 V	247 V	282 V
I_{UV85} (typically 30 µA)	182 V	212 V	242 V
I_{UV70} (typically 25 µA)	152 V	177 V	202 V
I_{UV55} (typically 20 µA)	122 V	142 V	162 V

Table 5. Effective High-Voltage Bus Monitoring Thresholds.

Using multiple sense resistors with different values on more than one device further reduces the bus voltage sensing granularity. Over-voltage protection can be disabled by limiting the current into the SM pin to less than the I_{OV} threshold by inserting through Zener diode V_{R1} and resistor R_{HV2} as shown in Figure 16. Bus undervoltage sensing remains active in this configuration.

Adding a small capacitor (maximum 100 pF) to the SM pin can improve bus monitoring accuracy in noisy environments.

System Level Temperature Monitoring

The SYSTEM MONITOR pin enables temperature monitoring of an external component through an NTC thermistor as shown in Figure 15. Resistor R_2 allows fine-tuning of the actual over-temperature threshold to achieve desired level with a given NTC resistor.

Current source I_{TM} (typically 100 µA) periodically injects a current into the NTC thermistor R_{NTC}. Its resistance falls as temperature rises. Once the voltage level at the SM pin drops below $V_{TH(TM)}$ (typically 1.2 V), the detected system level over-temperature fault is reported via the FAULT pin after delay timer $t_{D(TM)}$ expires (see Table 7 for details). The resistance of thermistor $R_{NTC(TSYS)}$ at the desired system over-temperature threshold T_{SYS} determines R_2:

$$R_2 = 12.5\ k\Omega - R_{NTC(TSYS)}$$

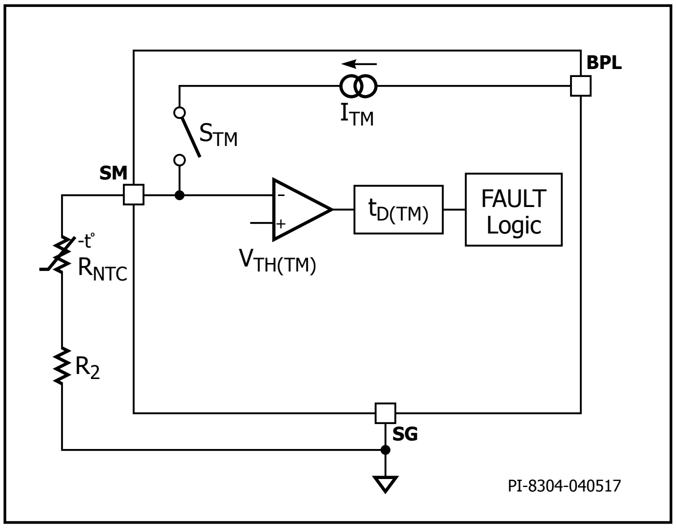


Figure 15. External Component Thermal Monitoring with SYSTEM MONITOR Pin.

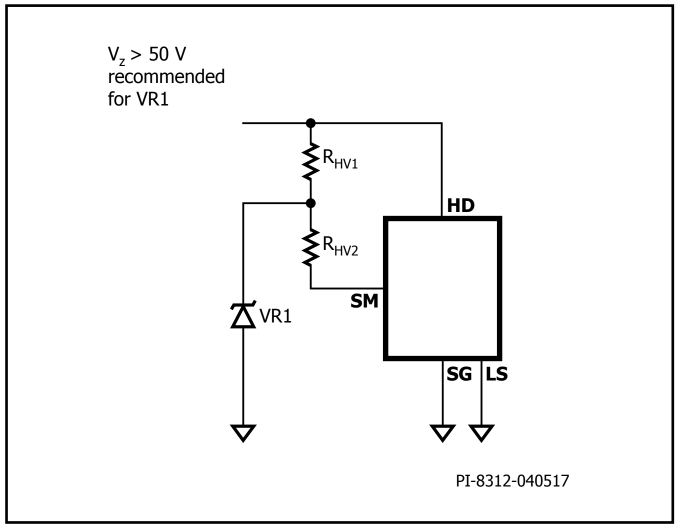


Figure 16. High-Voltage Bus Monitoring with Overvoltage Protection Disabled.

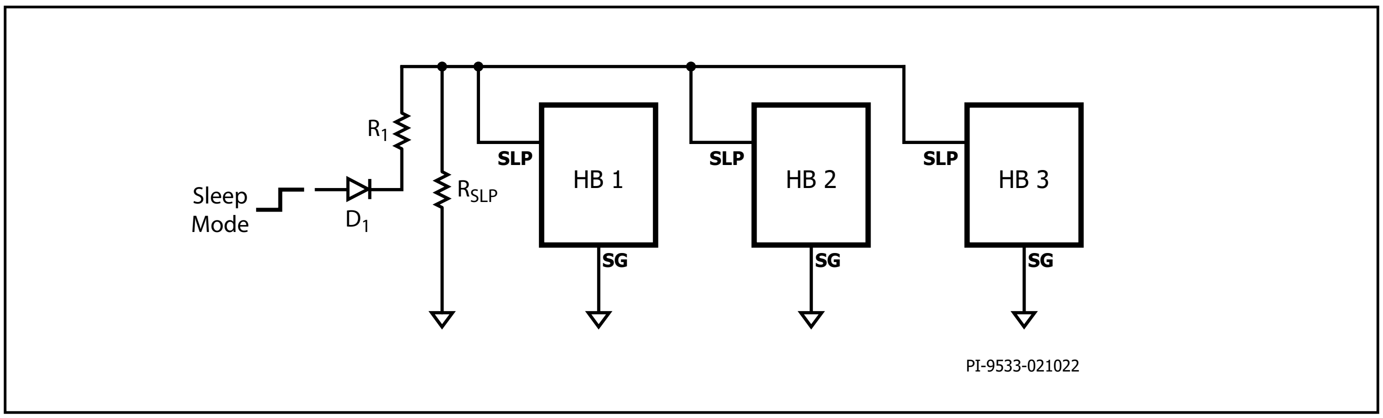


Figure 17. Programming of Sleep Mode, plus Over-Current and Over-Temperature Fault Handling.

Sleep Mode and Programming

The Sleep Mode and Programming pin has two functions. It sets the device into a optional sleep mode and it allows programming how BridgeSwitch-2 responds to sustained over-current and over-temperature faults.

At power-up, the BridgeSwitch-2 determines the resistance of the resistor R_{SLP} connected to SLP (refer to Figure 17) and sets fault response shown in Table 6. If no external resistor (R_{SLP}) is connected to the SLP pin, the BridgeSwitch IC assumes default mode. Default mode is cycle-by-cycle current limit and latching over-temperature protection which is triggered when the low-side FREDFET temperature reaches the shutdown temperature threshold T_{SD}.

R_{SLP} (kΩ)	Low-Side Current Limit	Over-Temperature Response
9.53	Cycle-by-cycle	Hysteretic protection
133	Latching after 16 consecutive over-current switch cycles	Latching protection
Open[1]	Cycle-by-cycle	Latching protection

Table 6. Fault Response Programming.
Notes:
1. Default setting.

The programming resistor values listed in Table 6 can be used for either a single SLP pin (Sleep Mode function is not used), or for two connected SLP pins (Sleep Mode function used in a single phase motor drive inverter) or for three connected SLP pins (Sleep Mode function used in a three phase motor driver inverter).

Sleep mode fully disables the device and reduces its power consumption to less than 4 mW when operating in self-supplied mode. During steady state operation, the SLP pin internal pull-down resistance keeps the voltage below the Sleep Mode Threshold Voltage $V_{SLP(TH)}$. A control signal applied to diode D1 (refer to Figure 17) sets the device into Sleep Mode by pulling the voltage level above the threshold $V_{SLP(TH)}$. Upon releasing the control signal applied at D1, BridgeSwitch-2 starts a standard power-up cycle (refer to Figure 8) and re-enables normal operation. Resistor R1 limits the current into the SLP pin. The recommended resistance for a 5 V control signal is 3.3 kΩ. A standard silicon diode is recommended for a 5 V control signal. A low forward voltage Schottky diode is recommended for a 3.3 V control signal.

Sleep mode is only active for devices operating with internal self-supply. That is BPL or BPH pins are not supplied externally through a resistor from a voltage source.

A resistor connected from the DC bus to the SM pin will increase overall inverter consumption depending on the value chosen (refer to R_{HV1} in Figure 13). For example, a 7 MΩ sense resistor consumes 16 mW from a 340 VDC bus.

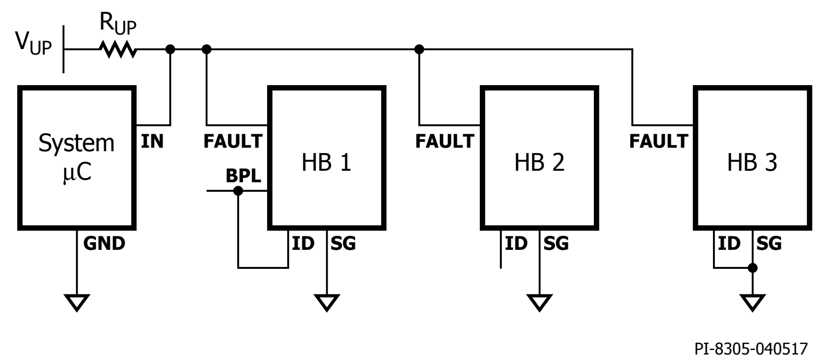


Figure 18. Single Wire Status Communication Bus with Device ID Programming.

The Status Communication Bus

BridgeSwitch-2 IC provides status updates, including device or system level faults, to the system MCU through its open Drain FAULT pin. All FAULT pins connect to a single bus minimizing the number of pins occupied at the system MCU (as shown Figure 18). The bus is pulled up to the system supply voltage through pull-up resistance R_{UP}. The minimum pull-up resistance R_{UP} is 2 kΩ for V_{UP} = 3.3 V or V_{UP} = 5 V. Pull-up resistance R_{UP} should not exceed 100 kΩ.

Status Word

BridgeSwitch-2 uses a 7-bit word followed by a parity bit to provide a status update (refer to Figure 20 for the timing diagram). Table 7 summarizes how various conditions are encoded. The 7-bit word consists of five blocks with status changes that cannot occur at the same time grouped together. This enables simultaneous reporting of multiple fault conditions to the system MCU. Grouping status conditions also allows reporting if a given fault condition has cleared. Cleared fault reporting applies to system level faults (bits 0, 1, and 2) and to low-side FREDFET thermal warning and loss of internal communication (bits 3 and 4). The status register entry in the bottom row (7-bit word "000 00 0 0") encodes Device Ready status and is used to report a successful power-up sequence. The BridgeSwitch-2 IC device also sends this message to acknowledge a status request sent by the system MCU when a no-fault condition is present (see Table 10 for details). The parity bit is generated using odd parity.

Table 8 lists examples of possible status update codes the device may send to the system MCU and the resulting transmit time for the respective status update. Transmission times range from 290 µs to 470 µs.

Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I_{OV}	0	0	1	X	X	X	X
High-voltage bus UV 100%	I_{UV100}	0	1	0	X	X	X	X
High-voltage bus UV 85%	I_{UV85}	0	1	1	X	X	X	X
High-voltage bus UV 70%	I_{UV70}	1	0	0	X	X	X	X
High-voltage bus UV 55%	I_{UV55}	1	0	1	X	X	X	X
System thermal fault	$V_{TH(TM)}$	1	1	0	X	X	X	X
LS Driver not ready[1]	n/a	1	1	1	X	X	X	X
LS FET thermal warning	T_{WA}	X	X	X	0	1	X	X
LS Device shutdown[3]	$T_{SD,}$ $t_{D(OCL)}$	X	X	X	1	0	X	X
HS Driver not ready[2]	I_{COM}	X	X	X	1	1	X	X
LS FET over-current	$V_{X(TH)}$	X	X	X	X	X	1	X
HS FET over-current	$V_{X(TH)}$	X	X	X	X	X	X	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

Table 7. Status Word Encoding.
Notes:
1. Includes XL pin open/short-circuit fault and IPH pin to XL pin short-circuit.
2. Includes internal communication loss, supply out of range, and XH pin short-circuit fault.
3. Includes LS FET thermal latching or hysteretic shutdown and LS FET sustained over-current protection.

Fault	7-Bit Word	Parity Bit	Transmit Time $t_{TRANSMIT}$[1]
Device Ready (no faults)	000 00 0 0	1	290 µs
High-voltage bus UV 100%	010 00 0 0	0	290 µs
LS FREDFET thermal warning and over-current	000 01 1 0	1	350 µs
System thermal fault, LS FET thermal warning, HS & LS FET over-current	110 01 1 1	0	410 µs
Maximum transmission duration	111 01 1 1	1	470 µs

Table 8. Example Status Update Codes and Resulting Transmit Times.
Notes:
1. Assumes t_{ID} = 80 µs (device ID #3).

Device ID Selection

At power-up, each device assigns itself a unique device ID depending on the DEVICE ID pin connection. This device ID allows reporting of the physical location of a detected fault condition to the system MCU. The device ID is also used for bus arbitration purposes. Table 9 lists the device ID, resulting Device ID Time Period t_{ID}, and how to program the respective ID through the ID pin (refer to Figure 18). Note that the system MCU is assigned automatically a default t_{ID} = 160 μs, thereby ensuring that it always wins bus arbitration.

Device ID	t_{ID}	ID Pin Connection
1	40 μs	Connected to BPL pin
2	60 μs	Floating
3	80 μs	Connected to SG pin
System MCU	160 μs	n/a

Table 9. Device ID Selection Through the ID Pin at Power-Up.

Status Communication

Communication on the FAULT bus initiates for one of the following three conditions:

1. Ready-for-mission mode communication after a successful power-up.
2. A FAULT-status-register-update communication initiated by one of the devices.
3. A current-status communication following a query by the system micro-controller.

Figure 19 summarizes the status communication flowchart for all three cases listed above.

As well as a status query, the system micro-controller can also send a command to reset the status register (see Table 10 and steps 16 and 17 in Figure 19). A power-up sequence is recommended after sending this reset command (refer to Figure 8).

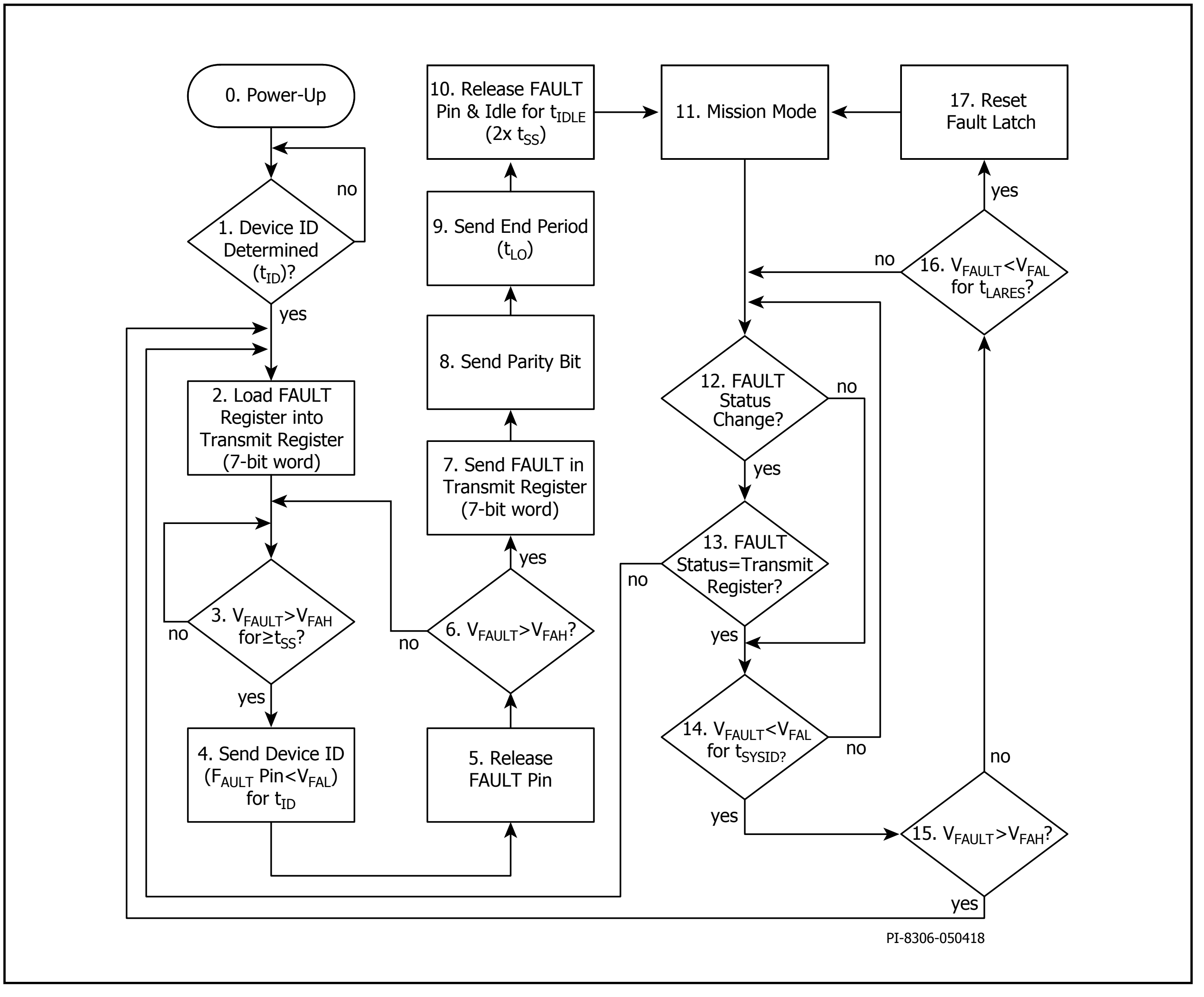


Figure 19. Status Communication Flowchart.

Figure 20 depicts the bit stream timing diagram BridgeSwitch-2 uses for a status update communication. The two logic states are encoded with two different voltage signal high-time periods at the STATUS COMMUNICATION pin followed by a low-time period t_{LO} (typically 10 μs). A logic "1" is encoded with a period t_{BIT1} (typically 40 μs) and a logic "0" is encoded with a period t_{BIT0} (typically 10 μs).

Each time BridgeSwitch-2 IC detects a status change, it loads the actual FAULT register into the Transmit register (see step 2 in Figure 19) and proceeds with a status update transmission.

The BridgeSwitch-2 IC starts a status update transmission only if the bus has been idle for at least the steady-state time period t_{SS} (typically 80 μs) to ensure that no other device is already using the bus (see step 3 in Figure 19).

A status update transmission starts always with bus arbitration initiated by the communicating device. It pulls the FAULT pin low for its assigned Device ID Time Period t_{ID} (refer to Table 9), releases the pin and then verifies that the communication bus stays high (see steps 4 to 6 in Figure 19). If this is the case, the device has won bus arbitration and can proceed with transmitting its status update (see steps 7 to 10 in Figure 19). If the bus stays low after sending its ID, another device started a transmission attempt (or bus arbitration) at approximately the same time. In this case the device will make another communication attempt by proceeding back to step 3 in Figure 19. After each completed transmission the device will idle for t_{IDLE} (typically $2 \times t_{SS}$ = 160 μs) before starting a new communication. This enables other devices on the bus to report a possible status change or to respond to a status inquiry sent by the system MCU.

A BridgeSwitch-2 IC transmits each detected status update only once. It also reports a status change for all system level faults to the system MCU. This includes DC bus undervoltage and overvoltage conditions and external temperature monitor faults. It also reports all status level changes for device internal faults with the exception of the LS power FREDFET thermal shutdown fault (a cleared LS power FREDFET thermal warning is reported).

Status Query and Fault Latch Reset

Each BridgeSwitch-2 IC monitors the STATUS COMMUNICATION pin for possible commands sent by the system MCU once it is in mission mode. This could be a status update inquiry (see step 15 in Figure 19) initiated by the MCU, achieved by pulling the bus low for a period of t_{SYSID} (typically 160 μs). Alternatively, it could be a command to reset the device status register, including the over-temperature shutdown latch, and to enter the power-up sequence mode (see step 17 in Figure 19) initiated by the MCU pulling the FAULT bus low for a period of t_{LARES} (2x t_{SYSID} = typically 320 μs). Note, a power-up sequence (refer to Figure 8) is recommended after the MCU has sent a latch reset command. This ensures that the bypass high-side voltage is at the nominal level before switching resumes. Table 10 summarizes available system MCU commands.

Bus Pull-Down Period	Command
t_{SYSID}	Status query
t_{LARES} (2x t_{SYSID})	Status register including over-temperature latch reset and power-up sequence mode

Table 10. System MCU Commands.

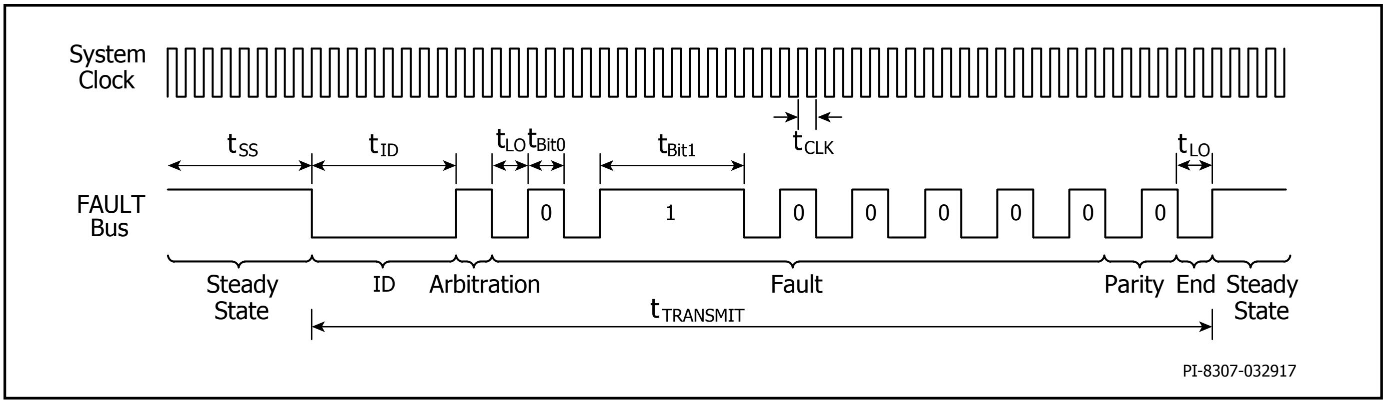


Figure 20. Status Communication Bit Stream.

Error Flag

The Error Flag function (BRD236X/BRD246X) enables simple inter-device communication in case one device detects a severe fault requiring the entire inverter to shut down. All EF pins connect to a single bus as shown in Figure 21. The bus is pulled to the system supply voltage through pull-up resistance R_{UP}. The recommended pull-up resistance is 43 kΩ for V_{CC} = 3.3 V or 5 V.

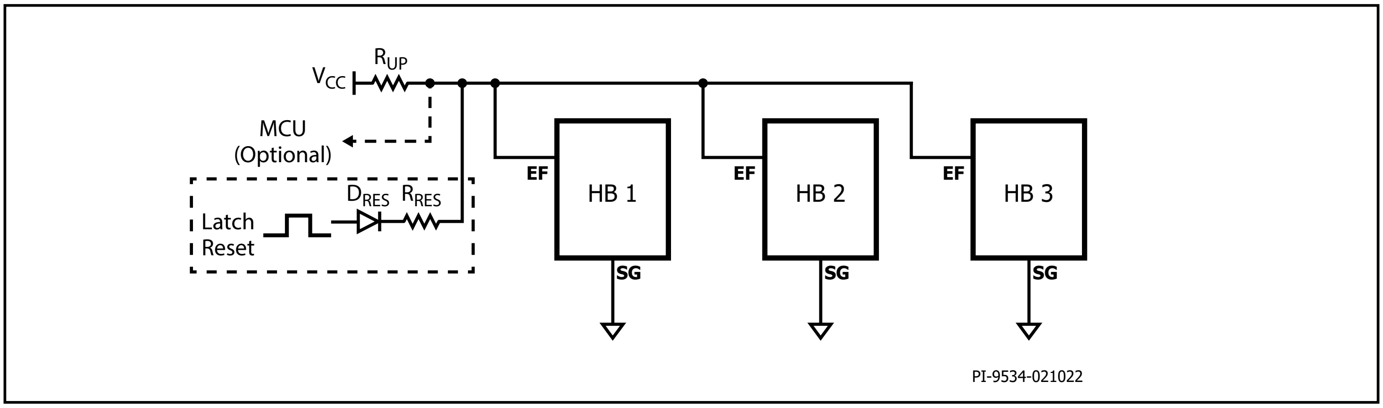


Figure 21. Error Flag Inter-Device Communication and Optional Latch Reset.

If a BridgeSwitch-2 IC detects any of the faults listed in Table 11, it pulls the EF pin low for as long as the detected fault is present. It releases the EF pin again after the fault has cleared or after having received a latch reset signal.

Fault	Note
DC Bus Overvoltage	Device flags a fault when current into SM pin exceeds the I_{OV} threshold and releases it again after the fault clears (current drops below I_{OV}-$I_{OV(HYST)}$).
Latching or Hysteretic Over-Temperature	Device flags a fault when the low-side FREDFET temperature reaches the shutdown threshold T_{SD} and releases it again after either having received a latch reset signal (rising edge) on the EF bus, or after a power-up, or when the temperature drops below the restart temperature T_{RES} for devices configured for hysteretic over-temperature protection through the SLP pin (refer to Table 6).
Sustained Over-Current	Device flags a fault if configured for latching sustained over-current shutdown protection through the SLP pin (refer to Table 6 with Sleep Mode and Programming section). It releases it again after either having received a latch reset signal on the EF bus or after a power-up.

Table 11. Faults Covered by Error Flag.

As long as the voltage level is below the Error Flag Voltage Low Threshold V_{EFL}, all other devices connected to the ERROR FLAG bus inhibit switching irrespective of the status of INL and /INH control inputs after delay time $t_{D(EF)}$ (see Figure 22). A BridgeSwitch-2 IC re-enables switching after the EF inter-device communication bus voltage exceeds the Error Flag Voltage High threshold V_{EFH}. A rising edge at the EF bus also triggers a latch reset for devices configured with a latching shutdown protection (refer to Table 6).

Resetting the latch is also possible by temporarily pulling the EF bus high through an external signal applied to the EF bus through D_{RES} and R_{RES} (see Figure 21). Resistor R_{RES} limits the current into the EF pin while providing a pull-up current greater than the device internal Error Flag Output Sink Current I_{EFS}. A typical resistance value for a 3.3 V or 5 V external latch reset signal is 3.3 kΩ.

The device has an internal pull-up current I_{EFPU} to ensure steady-state operation for cases where the EF pin is left floating.

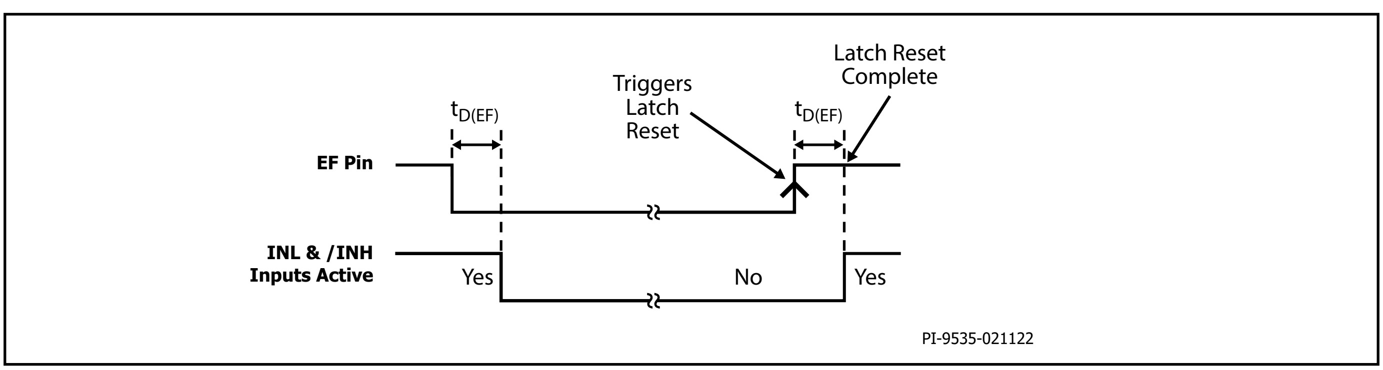


Figure 22. Error Flag Timing and Latch Reset.

Application Example

A High Efficiency, 150 W, Three-Phase Inverter

The schematic shown in Figure 23 is a three-phase inverter with three BRD2463C devices used to drive a high-voltage, three-phase brushless DC (BLDC) motor from a rectified AC input voltage. It can provide up to 150 W of continuous inverter output power at 340 VDC input voltage, 750 mA rms phase current, and 10 kHz PWM switching frequency without an external heat sink.

With sleep mode turned on, all three BridgeSwitch devices consume 10 mW offering exceptional standby efficiency. This design can support various motor control schemes through the available microcontroller interface. Using the external supply configuration allows higher efficiency across a wide load range. Self-supply mode which eliminates the external supply components can also be used to reduce component count.

Two current feedback modes are available on this board – the shunt resistor and IPH feedback. The former utilizes low-side current shunt resistors fed into an op-amp signal conditioning circuit to implement the traditional current sensing approach. For further part count optimization, the IPH signal can be used as feedback instead.

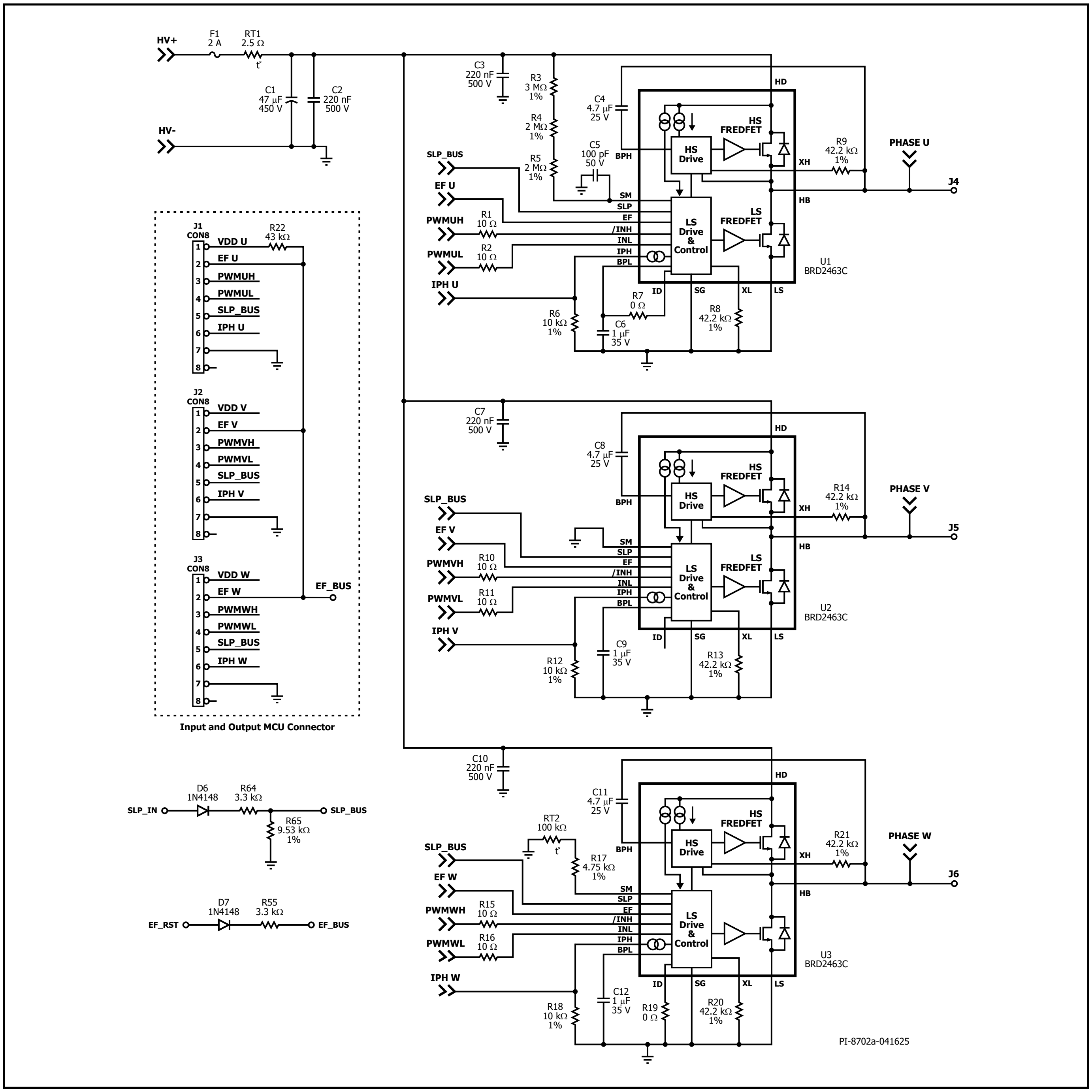


Figure 23. Three-Phase Inverter Example using BRD2265C.

The BridgeSwitch-2 device offers improved built-in fault protection through the new Error Flag (EF) pin. This allows critical faults such as sustained low-side over-current (OC), over-temperature (OT), and over voltage (OV) conditions to inhibit inverter switching without MCU intervention. Additional protection schemes provided by the System Monitor (SM) pin include the high-voltage DC bus sensing and system temperature monitoring.

Input Stage

The input stage comprises of fuse F1, NTC RT1 and capacitors C1 and C2. These components should be rated based on the calculated input current and the maximum DC Bus voltage. The input voltage can either be directly from the AC mains or from a Power Factor Correction (PFC) front-end circuit.

Three-Phase BridgeSwitch-2 Inverter

The BridgeSwitch-2 devices U1, U2, and U3 form the three-phase inverter. The outputs of the inverter connect to the high voltage three-phase BLDC motor through connectors J1, J2, and J3. Capacitors C3, C7 and C10 provide local high frequency decoupling of the DC bus voltage to each BridgeSwitch-2 device.

Bias Supply

Capacitors C6, C9, and C12 provide stable voltage supply for the BridgeSwitch-2 integrated low-side controller and gate driver. Capacitors C4, C8, and C11 provide stable voltage supply for the integrated high-side controller and gate driver. These capacitors are required for proper BridgeSwitch-2 operation.

PWM Inputs

Input signals PWMUH, PWMUL, PWMVH, PWMVL, PWMWH, and PWMWL control the switching state of the integrated high-side and low-side power FREDFETs. Resistors R1, R2, R10, R11, R15, and R16 situated between the MCU and BridgeSwitch-2 INL and /INH pins improve integrity of control signals from the MCU. BridgeSwitch-2 offers a trim option that allows the /INH pin to be active HIGH instead of active LOW to provide more flexibility for various motor control schemes.

Current Limit Programming

Resistors R8, R13, and R20 set the cycle-by-cycle current limit level for the integrated low-side FREDFETs while R9, R14, and R21 set the cycle-by-cycle current limit level for the integrated high-side power FREDFETs. The selected value of 42.2 kΩ sets the current limit at 100% of the default value or 2.5 A for BRD2463C (refer to Table 4 for current limit selection).

Phase Current Information

Each BridgeSwitch-2 device provides instantaneous phase current information through the IPH pin. Resistors R6, R12, and R18 convert the scaled current output of this pin to a usable voltage signal that can directly connect to the MCU ADC pin. With R6, R12, and R18 set to 10 kΩ, and an IPH gain of 75 μA/A for BRD2463C, a 1 A low-side FREDFET phase current will translate into a 0.75 V current feedback signal.

Over-Current (OCP) / Over-Temperature (OTP) Programming

A programming resistor R65 at the SLP pin allows selecting between three different implementations of over-current and over-temperature fault handling. During power-up, the device locks in the selected fault handling implementation (refer to Table 6 for SLP pin OCP/OTP fault handling programming options). For this application, the 9.53 kΩ resistor R65 connected to the SLP pin sets the OCP fault handling to cycle-by-cycle, and OTP fault handling to hysteretic.

Sleep Mode Interface

Sleep mode disables all functionality of the LS driver by disabling the internal high-voltage current source connected to HD. During steady state operation, the SLP pin internal pull-down resistance keeps the voltage below the Sleep Mode Threshold Voltage $V_{SLP(TH)}$. To activate sleep mode, a sleep mode control signal SLP is applied to diode D6, pulling the voltage level above the $V_{SLP(TH)}$ (minimum 2.5 V). When the control signal is released, the internal pull-down resistance of the SLP pin pulls the voltage below $V_{SLP(TH)}$, prompting the BridgeSwitch-2 devices to commence a regular power-up cycle and re-enable its normal operation. In the design shown in Figure 23, the SLP pin of each BridgeSwitch-2 device is tied together, allowing simultaneous sleep mode activation using only one sleep mode control signal. The current entering the SLP pins is limited by resistor R64, with a recommended value of 3.3 kΩ for a 5 V control signal amplitude.

Error Flag

This application uses the new BridgeSwitch-2 Error Flag function which enables simple inter-device communication in case one device detects a severe fault. If BridgeSwitch-2 detects any of the faults listed in Table 11, the EF pin is pulled low for as long as the detected fault is present, inhibiting switching for all devices. When the fault is cleared or after having received a latch reset signal EF_RST, the EF pin is released, enabling the BridgeSwitch-2 to resume switching.

In the design shown in Figure 23, the EF pins of U1, U2, and U3 are tied together to the EF_BUS and pulled up by resistor R22 (33 kΩ) to the auxiliary supply voltage (5 V). A latch reset signal is applied by temporarily pulling the EF_BUS high through an external signal applied through D7 and R55 (3.3 kΩ). A rising edge at the EF bus triggers a latch reset for devices configured with a latching shutdown protection (refer to Table 6).

Overvoltage (OV) Detection

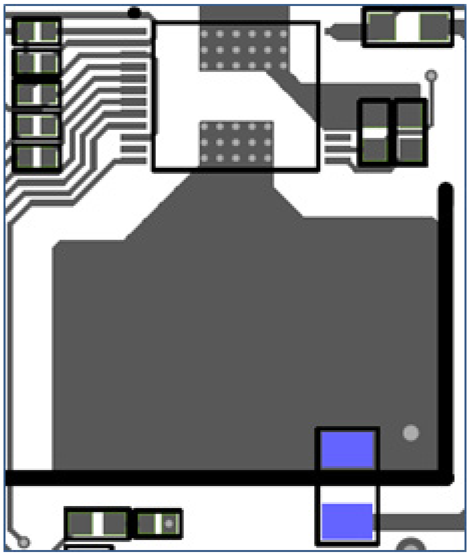
BridgeSwitch-2 U1 monitors the DC bus voltage through resistors R3, R4, and R5. The combined resistance of R3, R4 and R5 sets the overvoltage and undervoltage thresholds as shown in Table 5. Optional capacitor C5 provides high frequency noise decoupling at the SM pin in noisy environments. The recommended maximum value is 100 pF.

The EF bus flags detected DC bus overvoltage conditions. For the BridgeSwitch-2 EF variant (BRD236X/BRD246X), the EF pin is only pulled down during the overvoltage condition and is automatically pulled up once the DC Bus moves below the hysteretic reset voltage threshold.

System Level Temperature Monitoring

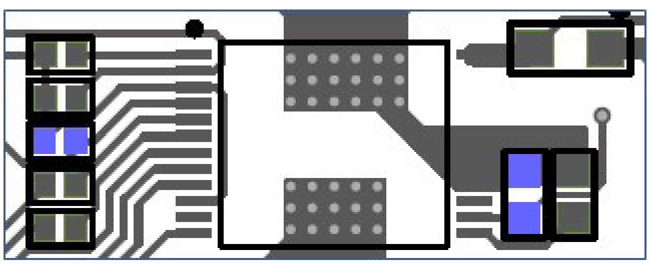
In addition to the device-level thermal protection, U3 monitors the system temperature through thermistor RT2 connected to the SM pin. Resistor R17 tunes the threshold of the system-level fault temperature to the desired level, which is 90°C for this application.

PCB Design Guidelines

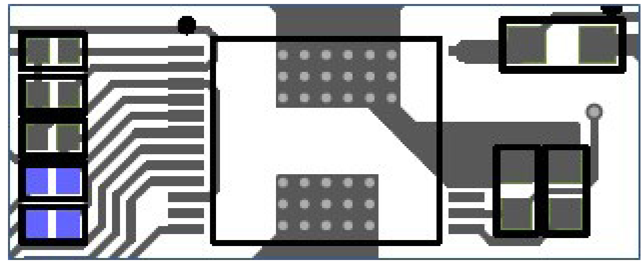


DC Bus Decoupling Capacitors
The HD pin decoupling capacitor provides local high frequency decoupling of the DC bus voltage to BridgeSwitch-2. The capacitor is placed before the DC bus (HD) connection to the device pin and close to the IC with required creepage and clearance distances considered.

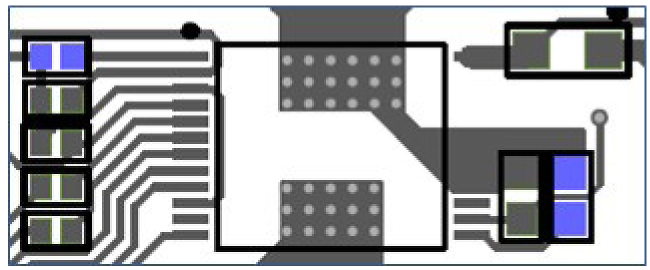
For the example shown above, the decoupling capacitor is placed directly beside the bulk capacitor positive. This filters out the DC bus signal before it connects to the HD pad.



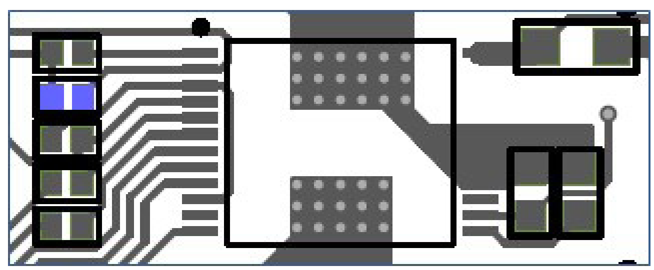
BPL and BPH Capacitor
The BPL and BPH decoupling capacitors are placed as close as possible to their respective pins to maximize noise immunity and ensure a stable supply to the device. The BPL capacitor returns directly to the SG pin, while the BPH decoupling capacitor returns directly to the HB pin.



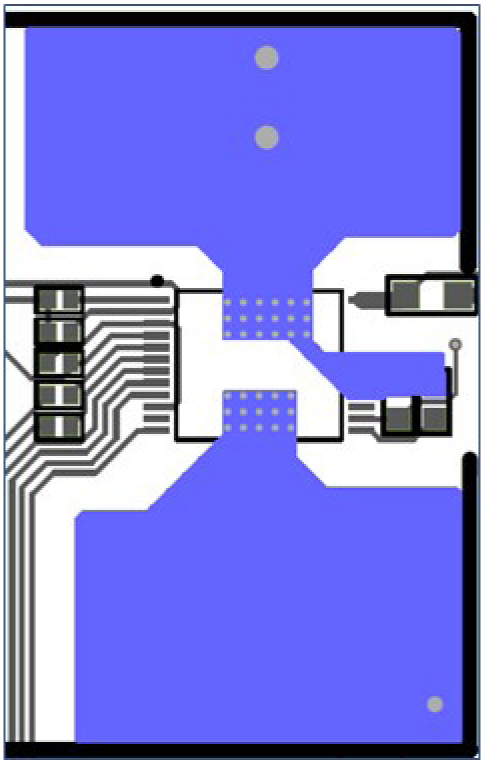
INL and /INH Input Resistors
The INL and INH resistors are placed as close as possible to their respective pins since they serve as filters for the PWM signals. The PWM signal traces from the MCU to the BridgeSwitch-2 input pins should be minimized for good signal integrity.



XL and XH Resistors
The XL resistor is placed near the XL pin and returns to the SG pin. The XH resistor is placed near the XH pin with a minimized loop area to the high-side return reference, the HB pin. This ensures proper current limit setting for both low-side and high-side FREDFETs.



IPH Resistor
The IPH resistor placement should be close to its respective pin and is referenced to SG. The IPH signal trace length from the BridgeSwitch-2 device to the MCU must be minimized to avoid noise pick-up and maintain signal integrity



HD and HB Plane for Maximum PCB Heat sinking
The BridgeSwitch-2 HD and HB exposed pad layout is configured to provide sufficient copper area for heat sinking.

Absolute Maximum Ratings[1,2]

HD Pin Voltage[2]: .... -1.3 V to 600 V
HB Pin Voltage: .... -15 V to 600 V
DC Output Current[6,7]: BRD2x60 .... 1.0 A
BRD2x61 .... 1.7 A
BRD2x63 .... 3.0 A
BRD2x65 .... 5.5 A
BRD2x67 .... 11.5 A
BPH Pin Voltage[3] .... -0.3 V to 16.5 V
BPL/ID Pin Voltage .... -0.3 V to 16.5 V
BYPASS Pin Current .... 15 mA
XH PIN[3] Voltage .... -0.3 V to 5.3 V
XL PIN Voltage .... -0.3 V to 5.3 V
EF/SLP/FAULT/INL/INH Pin Voltage .... -0.3 V to 5.3 V
SM Pin Voltage .... -0.3 V to 5.3 V
SM Pin Current .... 2 mA
IPH Pin Voltage .... -0.3 V to 5.3 V
IPH Pin Current .... 2 mA
LS Pin to SG Pin Voltage[5] .... ±0.33 V

Junction Temperature[7]: FREDFET .... -40 °C to 160 °C
Driver .... -40 °C to 150 °C
Storage Temperature .... -65 °C to 150 °C
Lead Temperature[4] .... 260 °C

Notes:
1. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
2. All voltages referenced to low-side Source LS and signal ground SG except noted otherwise, T_A = 25 °C.
3. Referenced to Half-Bridge Connection HB, T_A = 25 °C.
4. 1/16" from case for 5 seconds.
5. With external current sense resistor in series with LS pin. T_J = -20 °C to 125 °C.
6. Continuous DC output current per FREDFET calculated at 25 °C case and 125 °C junction temperature.
7. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance (θ_{JA})[3]: InSOP-24C Package
BRD2x60C .... 80 °C/W[1], 65 °C/W[2]
BRD2x61C .... 78 °C/W[1], 63 °C/W[2]
BRD2x63C .... 74 °C/W[1], 59 °C/W[2]
BRD2x65C .... 68 °C/W[1], 53 °C/W[2]
BRD2x67C .... 63 °C/W[1], 51 °C/W[2]
(θ_{JC})[4]: InSOP-24C Package
BRD2x60C .... 10 °C/W[4]
BRD2x61C .... 7 °C/W[4]
BRD2x63C .... 5 °C/W[4]
BRD2x65C .... 3 °C/W[4]
BRD2x67C .... 1.1 °C/W[4]

Notes:
1. Exposed pads soldered to 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
2. Exposed pads soldered to 1.0 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.
3. Both power switches each dissipating half the total power.
4. The case temperature is measured at the bottom of the package body on the exposed pads.

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)			Min	Typ	Max	Units
Bypass Supply Function								
BYPASS Voltages	V_{BPL} V_{BPH}	T_J = 25 °C See Note D			12.1	12.8	13.4	V
BYPASS Shunt Regulator Voltages	$V_{BPL(SHUNT)}$ $V_{BPH(SHUNT)}$	$I_{BPL} = I_{BPH}$ = 6 mA T_J = 25 °C See Note D			12.6	13.3	14.0	V
BYPASS Voltage Hysteresis	$V_{BPL(HYST)}$ $V_{BPH(HYST}$	T_J = 25 °C			1.9	2.4	2.9	V
BYPASS Low-Side Supply Current	$I_{BPL(S1)}$	V_{BPL} = 12.8 V See Note A	$V_{INL} < V_{IL}$, $V_{/INH} > V_{IH}$			0.37	0.45	mA
	$I_{BPL(S2)}$		$V_{INL} > V_{IL}$, $V_{/INH} < V_{IH}$	BRD2x60 BRD2x61 BRD2x63 BRD2x65		0.53	0.8	
				BRD2x67		0.70	0.94	
BYPASS High-Side Supply Current	$I_{BPH(S1)}$	V_{BPH} = 12.8 V See Note A	$V_{INL} < V_{IL}$, $V_{/INH} > V_{IH}$			0.33	0.42	mA
	$I_{BPH(S2)}$		$V_{INL} > V_{IL}$, $V_{/INH} < V_{IH}$	BRD2x60 BRD2x61 BRD2x63 BRD2x65		0.51	0.67	
				BRD2x67		0.68	0.75	

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Bypass Supply Function (cont.)							
BYPASS Low-Side Charge Current	$I_{CH1(LS)}$	T_J = 25 °C	V_{BPL} = 0 $V_{HD\text{-}to\text{-}LS}$ = 50 V	3.0			mA
	$I_{CH2(LS)}$		V_{BPL} = 12.8 V $V_{HD\text{-}to\text{-}LS}$ ≥ 100 V See Note C	1.7			
BYPASS High-Side Charge Current	$I_{CH1(HS)}$	$V_{HB} = V_{LS}$ T_J = 25 °C	$V_{BPH\text{-}to\text{-}HB}$ = 0 $V_{HD\text{-}to\text{-}HB}$ = 50 V	1.8			mA
	$I_{CH2(HS)}$		$V_{BPH\text{-}to\text{-}HB}$ = 12.8 V $V_{HD\text{-}to\text{-}HB}$ ≥ 100 V See Note C	10			
High-Side and Low-Side FREDFET Control							
INL Pull-Down Current	I_{INL}	V_{INL} = 2.5 V		0	1	1.15	μA
/INH Pull-Up Current	I_{INH}	V_{INH} = 2.5 V See Note J for BRD2X6XC-H450		-1.15	-1	0	
Input Voltage High	V_{IH}			2.5			V
Input Voltage Low	V_{IL}					0.8	V
Dead Time Low Off to High On	t_{DLH}	$V_{BPL} = V_{BPH}$ = 12.8 V, V_{DS} = 325 V, I_D = 0.1 A See Figures 10 and 24 See Note B		470	588	705	ns
Dead Time High Off to Low On	t_{DHL}	$V_{BPL} = V_{BPH}$ = 12.8 V, V_{DS} = 325 V, I_D = 0.1 A See Figure 10		470	588	705	ns
Switching Time FREDFET Turn-On	t_{ON}	$V_{BPL} = V_{BPH}$ = 12.8 V, V_{DS} = 325 V, I_D = 0.1 A /INH > V_{IH}, See Figure 24, Note C			0.7		μs
Switching Time FREDFET Turn-Off	t_{OFF}	$V_{BPL} = V_{BPH}$ = 12.8 V, V_{DS} = 325 V, I_D = 0.1 A /INH > V_{IH}, See Figure 24, Note C			0.4		μs
SLP Threshold Voltage	$V_{SLP(TH)}$	T_J = 25 °C		2.5			V

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Device Protection and System Level Monitoring							
FREDFET Junction Warning Temperature	T_{WA}	See Note C			125		°C
FREDFET Junction Shutdown Temperature	T_{SD}	See Note C		143	150	157	°C
FREDFET Junction Restart Temperature	T_{RES}	R_{SLP} = 3.3 kΩ See Note C			100		°C
Current Limit Threshold	$I_{LIM(DEF)}$	R_{XL} = R_{XH} = 42.2 kΩ T_J = 25 °C See Note 3, 7, 1, 10 See Note 3, 7, 1, 16	BRD2x60	0.855	0.90	0.945	A
			BRD2x61	1.425	1.50	1.575	
			BRD2x63	2.375	2.50	2.625	
			BRD2x65	3.135	3.30	3.465	
			BRD2x67	4.180	4.40	4.620	
	$I_{LIM(RED)}$	R_{XL} = R_{XH} = Open T_J = 25 °C di/dt = 100 mA/µs	BRD2x60	0.372	0.40	0.428	
			BRD2x61	0.605	0.65	0.696	
			BRD2x63	0.995	1.07	1.145	
			BRD2x65	1.302	1.40	1.498	
			BRD2x67	1.721	1.85	1.980	
Current Limit Delay Time	t_{ILD}	See Note B			150		ns
Leading Edge Blanking Time	t_{LEB}	See Note B		300			ns
Phase Current Output Gain	g_{IPH}	R_{XL} = R_{XH} = 42.2 kΩ, T_J = 25 °C $I_{D(LS)}$ = 0.75x $I_{LIM(DEF)}$ ON-time ≥ 2 µs	BRD2260/BRD2460	174.6	180	185.4	µA/A
			BRD2261/BRD2461	116.4	120	123.6	
			BRD2263/BRD2463	72.7	75	77.3	
			BRD2265/BRD2465	58.2	60	61.8	
			BRD2267/BRD2467	43.6	45	46.4	
Phase Current Output Delay Gain	t_{IPH}	R_{XL} = R_{XH} = 42.2 kΩ, T_J = 25 °C $I_{D(LS)}$ = 0.75x $I_{LIM(DEF)}$, di/dt = 100 mA/µs ON-time ≥ 2 µs, See Note B, I			500		ns

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Device Protection and System Level Monitoring (cont.)						
XL/XH Pin Voltage	V_{XL} V_{XH}	$V_{BPL} = V_{BPH}$ = 12.8 V $R_{XL} = R_{XH} \geq 42.2$ kΩ T_J = 25 °C	2.09	2.25	2.41	V
SM Pin Voltage	V_{SM}	SM Pin configured as bus voltage sense I_{SM} = 35 µA		1.6	1.9	V
High-Voltage Bus UV55 Threshold Current	I_{UV55}	T_J = 25 °C See Note C	18	20	22	µA
High-Voltage Bus UV70 Threshold Current	I_{UV70}	T_J = 25 °C See Note C	23	25	27	µA
High-Voltage Bus UV85 Threshold Current	I_{UV85}	T_J = 25 °C See Note C	28	30	32	µA
High-Voltage Bus UV100 Threshold Current	I_{UV100}	T_J = 25 °C	33	35	37	µA
High-Voltage Bus UV Delay Time	$t_{D(UV)}$	$I_{SM} = I_{UV100}$ See Note B		40		ms
High-Voltage Bus OV Threshold Current	I_{OV}	T_J = 25 °C	57	60	63	µA
High-Voltage Bus OV Delay Time	$t_{D(OV)}$	See Note B		80		µs
High-Voltage Bus OV Turn-Off Hysteresis	$I_{OV(HYST)}$			4		µA
System Over-Temperature Threshold	$V_{TM(TH)}$	SM Pin configured as external temperature sense See Figure 15	1.10	1.17	1.23	V
Over-Temperature Delay Time	$t_{D(TM)}$	See Note B		1		ms
Temperature Monitor Output Current	I_{TM}			100		µA
Temperature Monitor Current On-Time	$t_{ON(TM)}$	See Note C		10		ms
Temperature Monitor Current Duty Ratio	D_{ITM}	See Note B and C		1		%
Status Communication Bus						
INL High Time For Internal Communication	$t_{INLH(COM)}$	/INH > V_{IH} for ≥ t_{DHL} See Note G and Figure 25	2			µs
FAULT Pin Voltage High	V_{FAH}	R_{UP} = 267 Ω, V_{UP} = 3.3 V	2.5			V
FAULT Pin Voltage Low	V_{FAL}	R_{UP} = 267 Ω, V_{UP} = 3.3 V			0.8	V
FAULT Pin Current Sink	I_{FAS}	R_{UP} = 267 Ω, V_{UP} = 3.3 V, See Note F	3			mA

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Status Communication Bus (cont.)							
Device ID Time Period	t_{ID}	$V_{FAULT} < V_{FAL}$ T_J = 25 °C	$V_{ID} = V_{BPL}$	38	40	42	µs
			V_{ID} = Floating	57	60	63	µs
			$V_{ID} = V_{SD}$	76	80	84	µs
Steady-State Time Period	t_{SS}	$V_{FAULT} > V_{FAH}$ See Note B			80		µs
Logic Bit 0 Time Period	t_{Bit0}	T_J = 25 °C		9.5	10	10.5	µs
Logic Bit 1 Time Period	t_{Bit1}	T_J = 25 °C		38	40	42	µs
Low Time Period	t_{LO}	T_J = 25 °C		9.5	10	10.5	µs
Idle Time Period	t_{IDLE}	See Note C			2x t_{SS}		µs
System Control ID Time Period	t_{SYSID}	$V_{FAULT} < V_{FAL}$ See Note C			160		µs
Fault Latch Reset Time	t_{LARES}	$V_{FAULT} < V_{FAL}$ See Note C			2x t_{SYSID}		µs
Error Flag							
EF Pin Voltage High	V_{EFH}	R_{UP} = 43 kΩ, V_{UP} = 3.3 V		2.5			V
EF Pin Voltage Low	V_{EFL}	R_{UP} = 43 kΩ, V_{UP} = 3.3 V				0.8	V
EF Pin Output Sink Current	I_{EFS}	V_{EF} = 0.8 V T_J = 25 °C to 125 °C		112		320	µA
Error Flag Delay Time	$t_{D(EF)}$	R_{UP} = 43 kΩ, V_{UP} = 3.3 V See Note C			15		µs

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Power FREDFETs Channel and Diode							
DRAIN to SOURCE Breakdown Voltage	BV_{DSS}	I_D = 250 μA, T_J = 25 °C		600			V
High-Side DRAIN Supply Voltage	$V_{HD(START)}$			50			V
OFF-State Drain Leakage Current	I_{DSS1}	V_{DS} = 540 V T_J = 100 °C See Note H				65	μA
ON-State DRAIN-to-SOURCE Resistance	$R_{DS(ON)}$	BRD2x60 $V_{BPH} = V_{BPL}$ = 12.8 V $I_D = 0.1 \times I_{LIM(DEF)}$	T_J = 25 °C		6.84	8.21	Ω
			T_J = 100 °C		9.65	11.58	
		BRD2x61 $V_{BPH} = V_{BPL}$ = 12.8 V $I_D = 0.1 \times I_{LIM(DEF)}$	T_J = 25 °C		2.95	3.54	
			T_J = 100 °C		4.28	5.14	
		BRD2x63 $V_{BPH} = V_{BPL}$ = 12.8 V $I_D = 0.1 \times I_{LIM(DEF)}$	T_J = 25 °C		1.53	1.84	
			T_J = 100 °C		2.11	2.53	
		BRD2x65 $V_{BPH} = V_{BPL}$ = 12.8 V $I_D = 0.1 \times I_{LIM(DEF)}$	T_J = 25 °C		0.83	0.99	
			T_J = 100 °C		1.13	1.35	
		BRD2x67 $V_{BPH} = V_{BPL}$ = 12.8 V $I_D = 0.1 \times I_{LIM(DEF)}$	T_J = 25 °C		0.47	0.56	
			T_J = 100 °C		0.61	0.73	
DRAIN Voltage Fall Time	t_{VF}	V_{HVBUS}= 325 V See Figure 24 See Notes C and E			115		ns
DRAIN Voltage Rise Time	t_{VR}	V_{HVBUS} = 325 V See Figure 24 See Notes C and E			95		ns
Sleep Mode Drain Leakage Current	$I_{D(SLP)}$	V_{DS} = 325 V T_J = 75 °C V_{SLP} > 2.5 V See Note C			10		μA

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Power FREDFETs Channel and Diode (cont.)							
Diode Forward Voltage	V_{SD}	BRD2x60, I_S = 0.5 A See Note C	T_J = 25 °C		1.60		V
			T_J = 100 °C		1.42		
		BRD2x61, I_S = 0.7 A See Note C	T_J = 25 °C		1.49		
			T_J = 100 °C		1.22		
		BRD2x63, I_S = 1 A See Note C	T_J = 25 °C		1.46		
			T_J = 100 °C		1.13		
		BRD2x65, I_S = 1 A See Note C	T_J = 25 °C		1.09		
			T_J = 100 °C		0.91		
		BRD2x67, I_S = 1 A See Note C	T_J = 25 °C		0.91		
			T_J = 100 °C		0.80		
Diode Reverse Recovery Time	t_{RR}	V_R = 400 V T_J = 125 °C See Note C	BRD2x60, I_S = 0.5 A di/dt = 50 A/μs		120		ns
			BRD2x61, I_S = 0.75 A di/dt = 50 A/μs		100		
			BRD2x63, I_S = 1 A di/dt = 50 A/μs		130		
			BRD2x65, I_S = 1 A di/dt = 75 A/μs		120		
			BRD2x67, I_S = 1 A di/dt = 75 A/μs		130		

NOTES:

A. Total current consumption is the sum of $I_{BPL(S1)}$ or $I_{BPH(S1)}$ and I_{DSS} when both FREDFETs are off and the sum of $I_{BPL(S2)}$ or $I_{BPH(S2)}$ and I_{DSS} when one FREDFET is switching (20 kHz maximum commutation frequency assumed).

B. Guaranteed by design. Not tested in production.

C. Guaranteed through characterization. Not tested in production.

D. Bypass shunt regulator voltage exceeds bypass voltage guaranteed by design.

E. Tested in a typical 3-phase inverter application circuit. Normally limited by internal circuitry.

F. Measured indirectly during device timing tests.

G. Assumes control input /INH was high for an idling period of $t_{IDLE} > t_{DHL}$. The required minimum INL high time for internal communication increases by $t_{DHL} - t_{IDLE}$ if $t_{IDLE} < t_{DHL}$ (refer to Figure 25).

H. Controller BYPASS pin voltage at V_{BPL} + 0.1 V or V_{BPH} + 0.1 V during FREDFET off-state.

I. IPH output connected to a 10 kΩ resistor in parallel to series RC network of 8 kΩ and 7 pF.

J. I_{INH} is a Pull-down Current for BRD2X6XC-H450 and matches I_{INL} parameters.

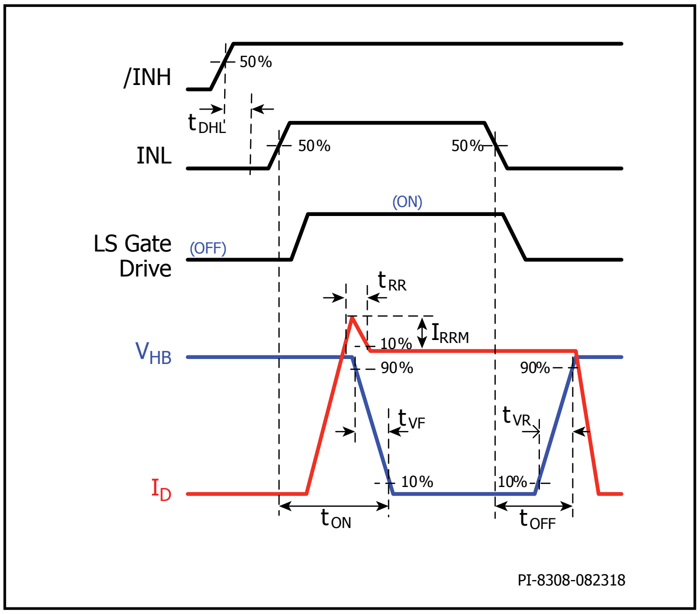


Figure 24. Low-Side FREDFET Switching Timing.

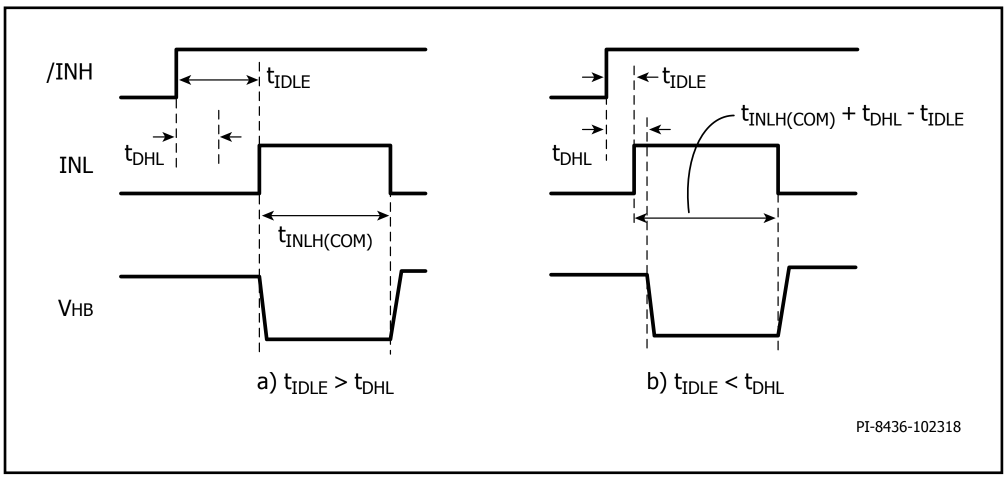


Figure 25. Minimum INL High Time Required for Device Internal High-Side Status Update a) $t_{IDLE} > t_{DHL}$ b) $t_{IDLE} < t_{DHL}$.

Typical Performance Characteristics

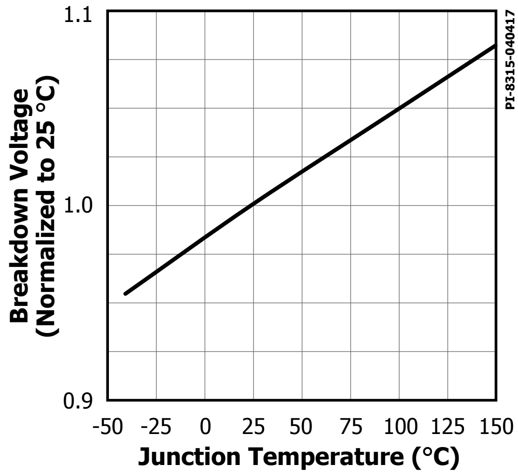


Figure 26. Power FREDFET Breakdown vs. Temperature.

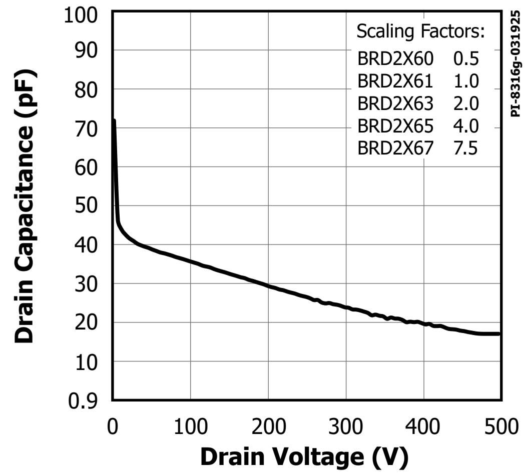


Figure 27. Power FREDFET C_{OSS} vs. Voltage.

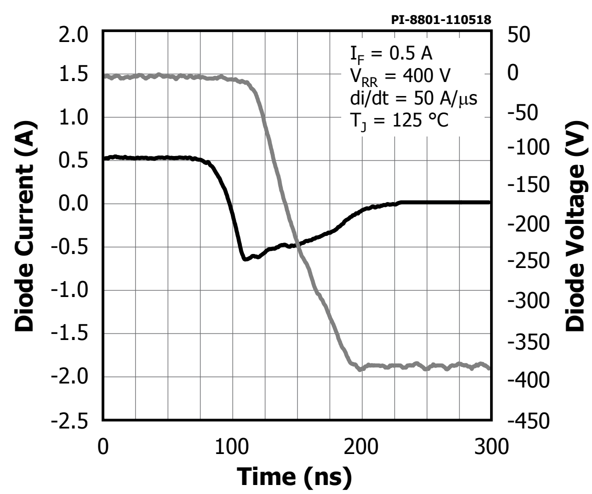


Figure 28. Typical Diode Reverse Recovery (BRD2X60).

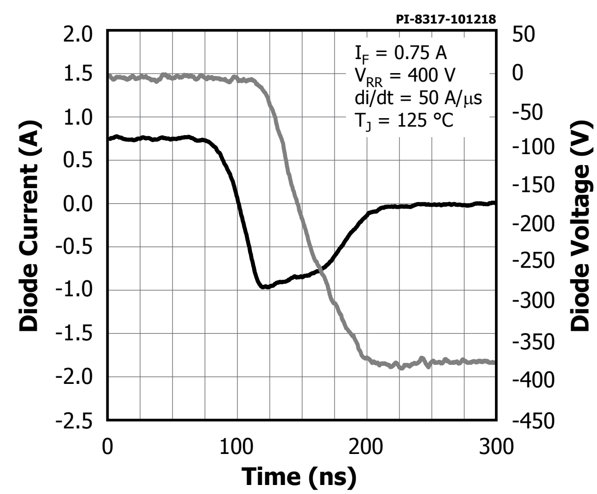


Figure 29. Typical Diode Reverse Recovery (BRD2X61).

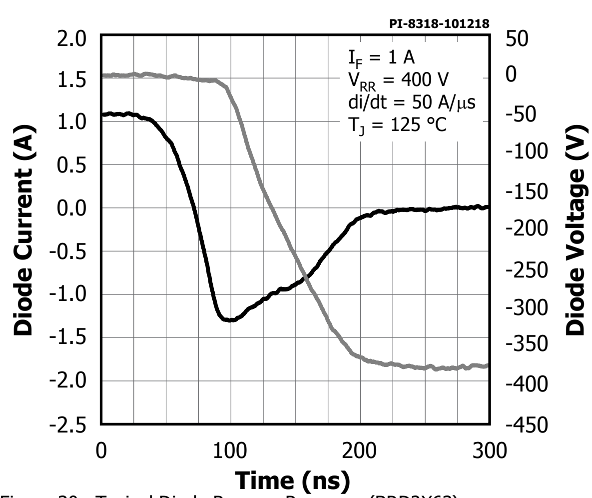


Figure 30. Typical Diode Reverse Recovery (BRD2X63).

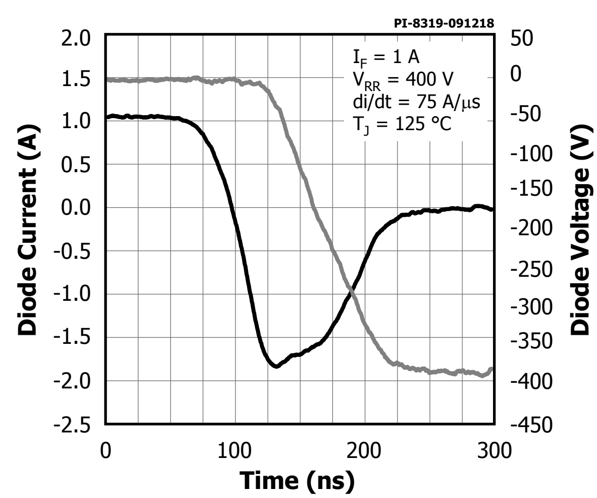


Figure 31. Typical Diode Reverse Recovery (BRD2X65).

Typical Performance Characteristics (cont.)

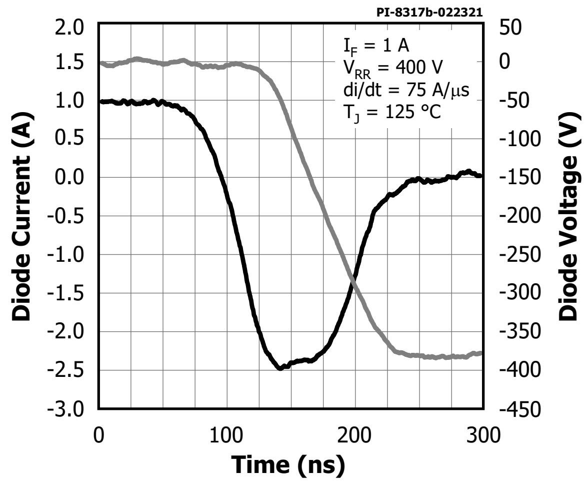


Figure 32. Typical Diode Reverse Recovery (BRD2X67).

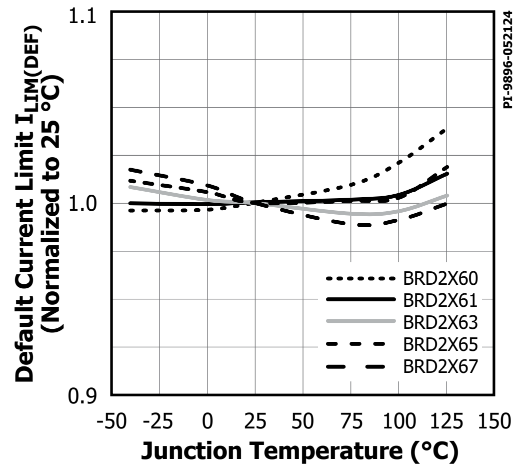


Figure 33. Default Current Limit vs. Temperature.

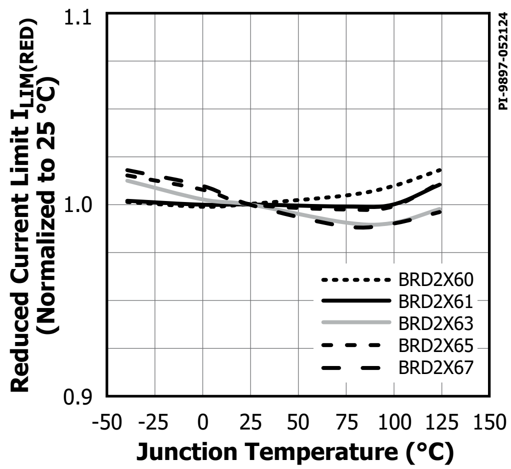


Figure 34. Reduced Current Limit vs. Temperature.

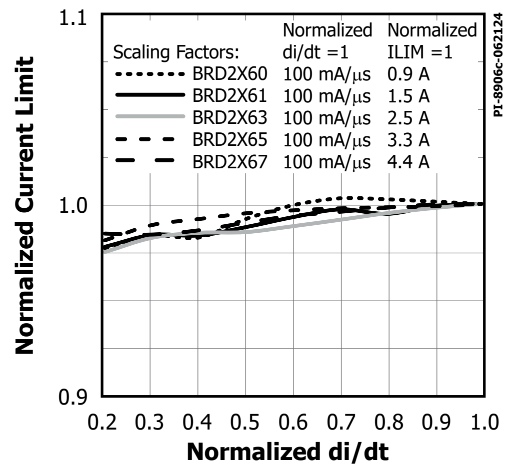


Figure 35. Default Current Limit vs. di/dt.

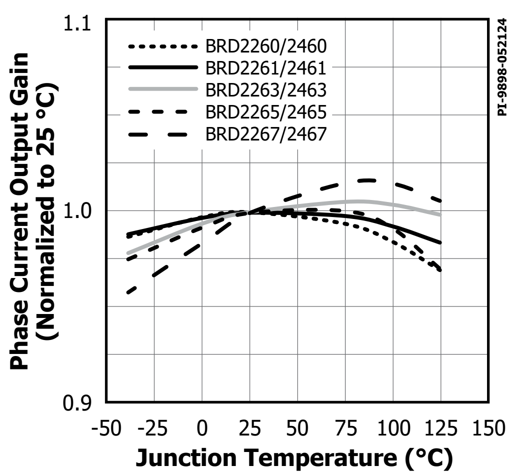


Figure 36. Phase Current Output Gain vs. Temperature

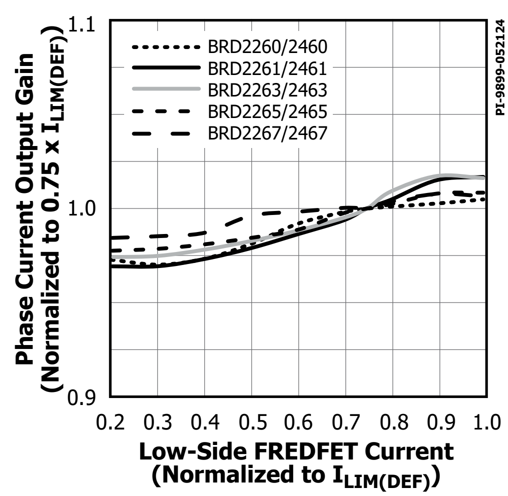


Figure 37. Phase Current Output Gain vs. Low-Side FREDFET Current.

Typical Performance Characteristics (cont.)

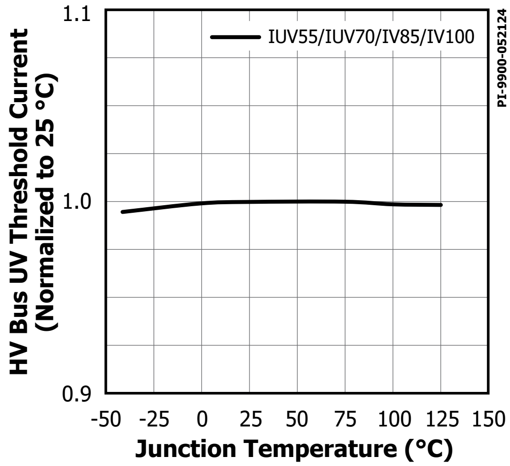


Figure 38. HV Bus UV Threshold Current vs. Temperature.

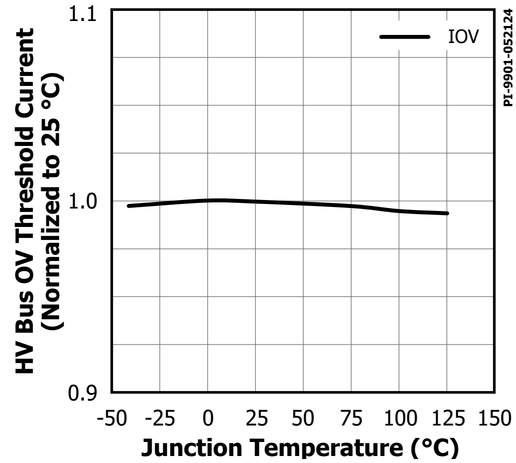
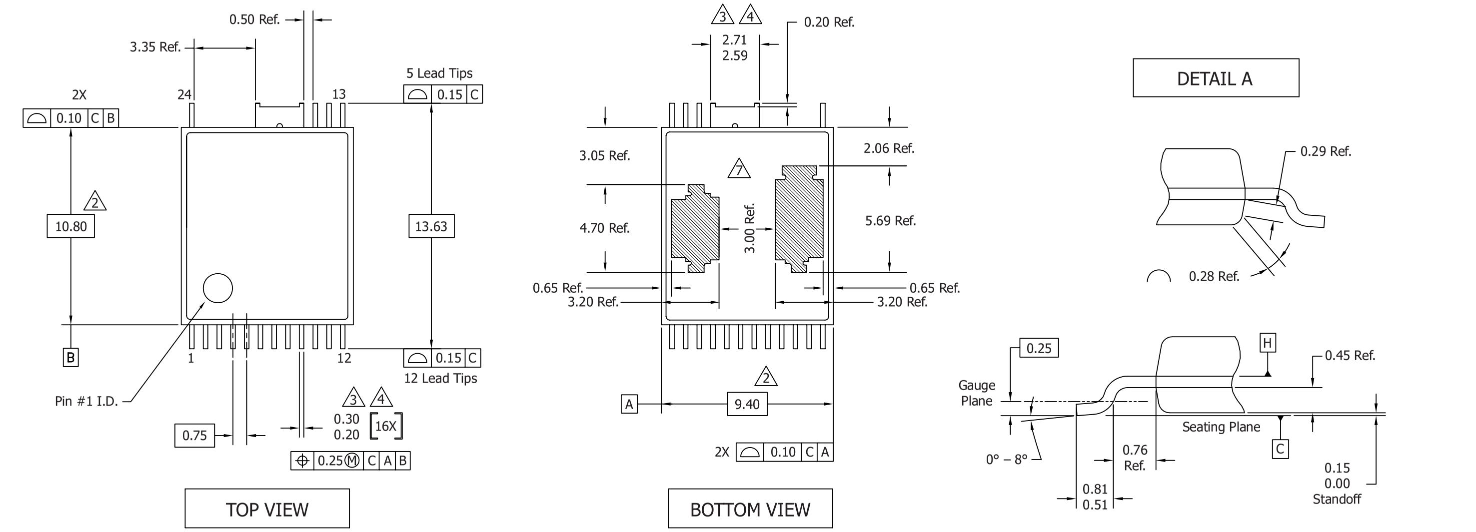
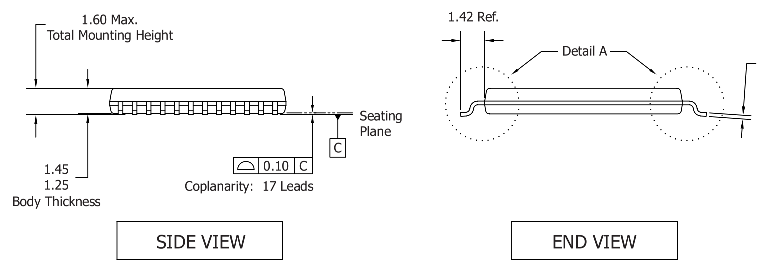
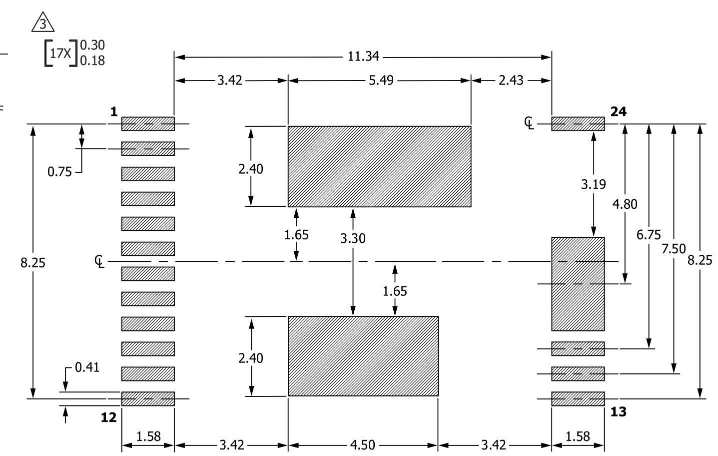


Figure 39. HV Bus OV Threshold Current vs. Temperature.

InSOP-24C







Note: The PCB footprint shown is the minimum recommended layout for basic thermal, mechanical and electrical interconnect, including package-to-PCB creepage. Modifications are expected, based on application-specific requirements, to add copper areas for improved thermal performance or reduce for increased on-PCB creepage.

PCB PAD LAYOUT

Notes:

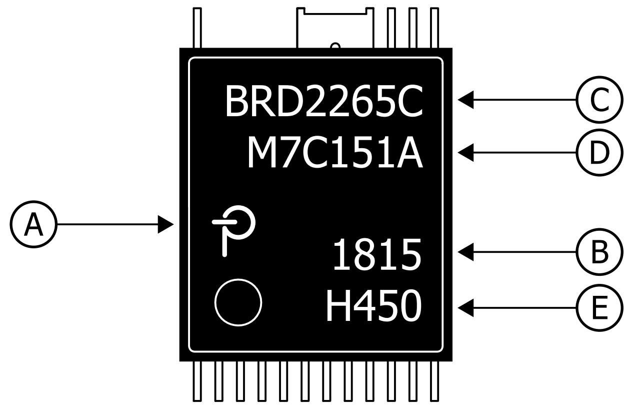
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. (△) Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 mm per side.
3. (△) Dimensions noted are inclusive of plating thickness.
4. (△) Does not include inter-lead flash or protrusions.
5. Dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. (△) Exposed pad size and location dimensions are for reference only.

POD_inSOP-24C_B_031417

PI-8294-051619

PACKAGE MARKING

InSOP-24C



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Feature Code

PI-8836h-042225

Feature Code Table

Summary Features	H450
Active High INL and INH Logic Level Control Inputs for Low- and High-Side FREDFETs	Yes

Part Ordering and MSL Table

Product / Part Number	MSL Rating
BRD2160C	3
BRD2161C	3
BRD2163C	3
BRD2165C	3
BRD2167C	3
BRD2260C	3
BRD2261C	3
BRD2263C	3
BRD2265C	3
BRD2267C	3
BRD2360C	3
BRD2361C	3
BRD2363C	3
BRD2365C	3
BRD2367C	3
BRD2460C	3
BRD2461C	3
BRD2463C	3
BRD2465C	3
BRD2467C	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information

BRD 2263 C - H450 - TL

- **BridgeSwitch Product Family**
- **Series Number**
- **Package Identifier**
  - C | InSOP-24C
- **Feature Code**
- **Tape & Reel and Other Options**
  - TL | Tape & Reel, 2 k pcs per reel.

Revision	Notes	Date
B	Introduction release.	05/24
C	Text, reference changes and updated Figure 38.	07/24
D	Updated Figures 3, 23, 27, I_{INL}, I_{INH}, BRD2x65 $I_{LIM(DEF)}$ parameter and unused IPH function pin recommendation updates, added feature code.	05/25

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