# Application Note AN-52
# HiperPFS Family

## Design Guide

### Introduction

Electronic equipment and power supplies without any active or passive power factor correction (PFC) circuits have an input current waveform which has a poor power factor and high harmonic distortion. Poor power factor and high distortion of current drawn by equipment is a key contributor of losses in the power distribution network. In order to enforce a limit on the amount of harmonic distortion and power factor degradation caused by electrical and electronic equipment, IEC/EN standard 61000 stipulates limits on the harmonic distortion of different classes of equipment. It is difficult to meet these limits without the use of an active or passive power factor correction circuit. Active power factor correction using a boost PFC is one of the most cost effective methods of power factor correction and is the chosen topology of the HiperPFS product family.

The HiperPFS™ is a family of highly integrated ICs that provides active power factor correction for switching power supplies. The HiperPFS enables the design of power factor corrected, rectifier front ends for switching power supplies rated up to a load of 425 W for universal input applications and up to 900 W for power supplies with a 230 VAC input. The resulting input current waveform has very low distortion, and the voltage and current waveforms achieve near unity power factor, enabling the power supply to meet the requirements of EN61000-3. Several innovative features of the HiperPFS result in a circuit that is easy to design, and reduces design effort and cycle time. The HiperPFS family also improves design reliability via features such as input undervoltage protection, built-in overload protection and hysteretic thermal shutdown protection.

Each member of the family has a high-voltage power MOSFET and a highly integrated controller in a compact package that enables design of low profile power supplies. The PFC engine uses a novel constant amp-seconds control to determine the on time and a constant volt second control to determine the off-time. The resulting switching waveform has inherent frequency modulation which simplifies input filter design by spreading the EMI energy over a wider frequency range. The integrated soft-start feature ensures that the start-up is graceful without any abnormal input current and any significant output voltage overshoot. In addition, the ICs have integrated functions that provide system-level protection. The soft-shutdown feature provides a graceful shutdown of the converter during a line brown-out. The open feedback pin detection feature ensures that the power factor correction stage operates only when the feedback circuit is correctly configured. EcoSmart™ technology continuous frequency slide, results in an automatic reduction in operating frequency as the load level reduces which ensures that operating efficiency remains high down to extremely light load levels. This simplifies meeting energy efficiency standards such as the European Code of Conduct, 80 PLUS and ENERGY STAR.

This application note describes the operation of the HiperPFS. Supporting information is provided to facilitate design optimization and selection of required components together with guidelines for system design. Design steps are described using the PIXIs spreadsheet to facilitate design of a PFC circuit using the HiperPFS.

For additional information regarding active power factor correction in general, see Application Note AN-53 Active Power Factor Correction – Basics.

#### Need for Power Factor Correction

For a sinusoidal AC supply with a linear load, Power Factor (PF) is a measure of the ratio of real power and apparent power supplied by the AC source. Real power is measured in watts and represents the energy consumed by the load to do useful work. Reactive power is the power that flows back and forth between the source and the load and is a result of the reactive nature of components on the load side. Apparent power is the vector sum of the real and reactive power. When the reactive power is high, the AC source must supply a large apparent power to support the operation of the load which results in higher RMS current. High reactive power not only demands a higher source capacity to support the load, but also results in higher transmission losses. For a pure sinusoidal voltage and current waveform, PF is the cosine of the phase angle between the voltage and current waveforms. The value of PF therefore can vary from 0 to 1 and can be leading or lagging. In situations where the power factor is lagging, PF improvement is achieved by connecting capacitor banks across the source. The resulting current from the source is in phase with the source voltage and PF correction is achieved. PF is therefore a figure of merit indicating how effectively energy is transmitted between the source and the load.

$$PF = \frac{P_{AVERAGE}}{V_{RMS} \times I_{RMS}} \quad (1)$$

AC-DC switching power supplies with a rectifier front end draw a current waveform which is not sinusoidal. The waveform contains harmonics at frequencies higher than the fundamental frequency. This often introduces some distortion in the supply voltage waveform. The AC source waveform in real life is often distorted due to the increased number of non-linear loads that are connected on the grid. The AC power being transmitted to the switching power supply load now consists of power transmission at the harmonic frequencies in addition to power being supplied at the fundamental frequency.

The average power is now calculated using the equation:

$$P_{AVERAGE} = V_0 I_0 + \sum_{N=1}^{\infty} \frac{V_N I_N}{2} \cos(\varphi_N - \theta_N) \quad (2)$$

N represents the harmonic number and the term. $Cos(\varphi_N-\theta_N)$ is a displacement term which accounts for the phase displacement between the harmonic voltage and respective harmonic current. The equation indicates that only when the voltage and current waveform contain the same harmonic, power is transmitted at the harmonic frequency. If the AC supply voltage is purely sinusoidal and free of harmonic distortion at any other frequency, the presence of harmonics in the current waveform alone, only increases the RMS value of the current waveform and leaves the average power unchanged. Increase in the RMS value of current therefore only results in added transmission line losses.

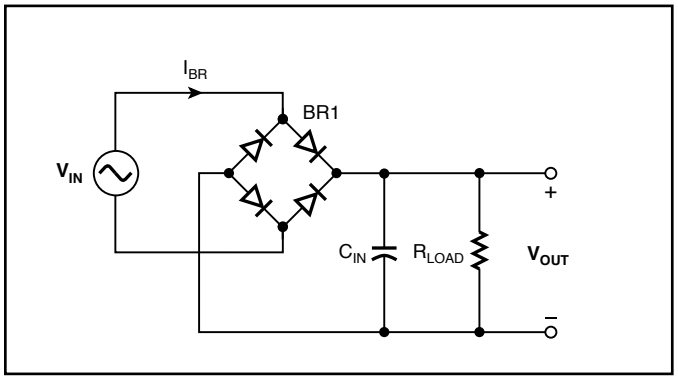



*Figure 1. Full Wave Rectifier.*

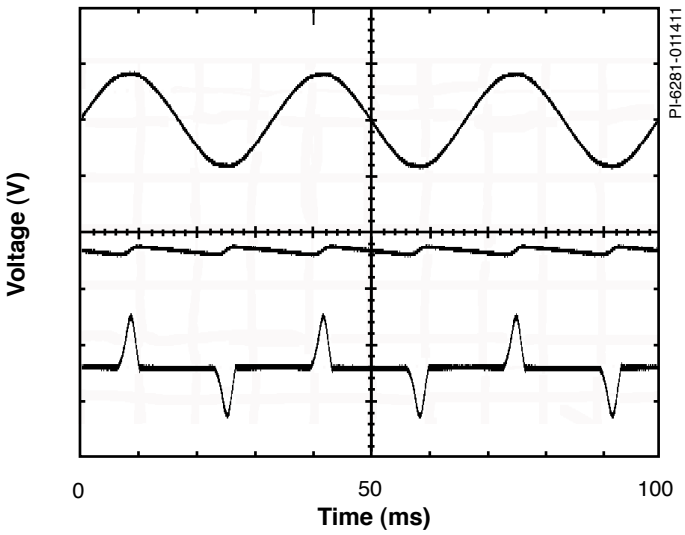



*Figure 2. Full Wave Rectifier Stage Waveforms. Top: Input Voltage. Middle: Output Voltage. Bottom: Input Current.*

The equivalent circuit of a typical non-PFC switching power supply front end is shown in Figure 1. Figure 2 shows the resulting non-sinusoidal input current waveform. Several passive and active techniques to improve the current waveform and achieve a near sinusoidal wave shape are described in AN-53. A VF-CCM (Variable Frequency – Continuous Conduction Mode) boost PFC circuit designed using the HiperPFS, when used as a power supply front end, results in a sinusoidal low distortion input current waveform compliant to most requirements including EN61000-3.

Figure 3 shows the input current waveform of a typical VF-CCM boost PFC stage designed using the HiperPFS. Near unity power factor is achieved while simultaneously maintaining overall high efficiency across load range.

Figure 4 shows the schematic of a typical boost PFC designed using the HiperPFS.

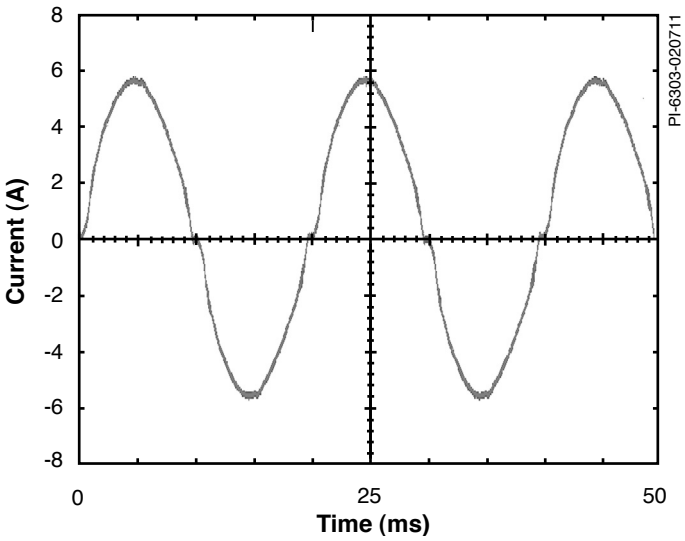



*Figure 3. Input Current Waveform at 115 VAC for a Typical 425 W PFC using HiperPFS (2 A, 1 ms / div).*

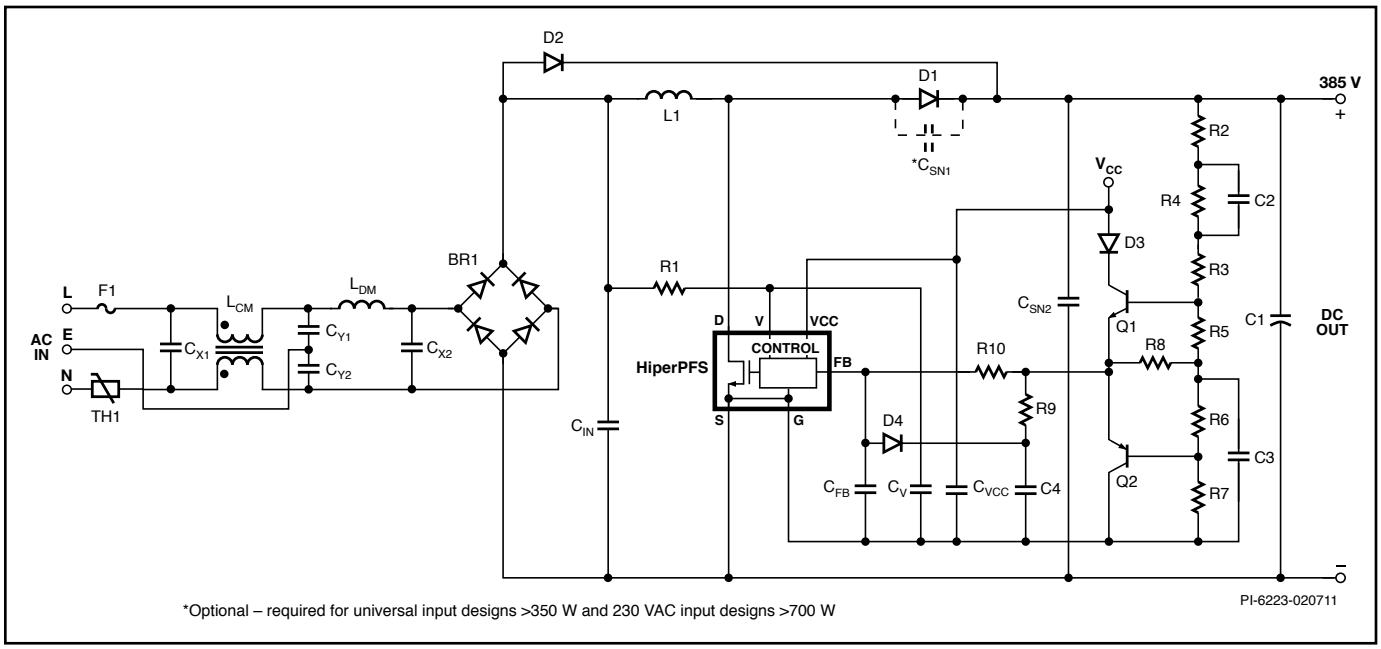



*Figure 4. Typical PFC Frontend Designed using HiperPFS (385 V Output).*

## Scope

This application note is intended for engineers designing an active PFC circuit using the HiperPFS family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable inductor design. To simplify the task this application note refers directly to the PIXls design spreadsheet that is part of the PI Expert™ design software suite. The basic configuration used in a PFC designed using the HiperPFS is shown in Figure 4, which also serves as the reference circuit for component identifications used in the description throughout this application note.

In addition to this application note the reader may also find the HiperPFS Reference Design Kit (RDK-236) containing an engineering prototype board, engineering report and device samples useful as an example of a working power supply. Further details on downloading PI Expert, obtaining a RDK and updates to this document can be found at www.power.com.

### Theory of Operation

The HiperPFS employs a novel control method that creates an input current waveform that follows the shape of the input voltage waveform by varying the on time and the off time of the power switch.

More specifically, the control technique sets constant volt-seconds for the off time. The off-time is controlled such that:

$$(V_{OUT} - V_{IN}) \times t_{OFF} = K_1 \quad (3)$$

Since the volt-seconds during the on time must equal the volt-seconds during the off time, to maintain flux equilibrium in the PFC choke, the on time is controlled such that:

$$V_{IN} \times t_{ON} = K_1 \quad (4)$$

The controller also sets a constant value of charge during each on cycle of the power MOSFET. The charge per cycle is varied gradually over many switching cycles in response to load changes so can be regarded as substantially constant for a half line cycle. With this constant charge (or Amp-Second) control, the following relationship is therefore also true:

$$i_{IN} \times t_{ON} = K_2 \quad (5)$$

Substituting $t_{ON}$ from (4) into (5) gives:

$$i_{IN} = V_{IN} \times \frac{K_2}{K_1} \quad (6)$$

The relationship of (6) demonstrates that by controlling a constant amp-second on time and constant volt-second off time, the input current $I_{IN}$ is proportional to the input voltage $V_{IN}$, therefore providing the fundamental requirement of power factor correction.

This control produces a continuous mode power switch current waveform that varies both in frequency and peak current value across a line half cycle to produce an input current proportional to the input voltage.

### PFC Control Engine

Figure 5 illustrates at a high level the PFC control engine of the HiperPFS device. It comprises of two main sections; an on-time controller and an off-time controller which both interface to a latch to generate the control gate-drive signal to the power MOSFET.

The on-time controller comprises of a current source proportional to the switch current, a resettable integrator and a comparator. The scaled switch current (from the sense-FET) is used to charge an integrating capacitor up to a level defined by the output voltage regulator (error-voltage). The output of the on-time control comparator 'resets' the latch to terminate the on-time and begin the off-time of that particular cycle. In a given input line frequency cycle, the error-voltage from the output voltage regulating error-amplifier is quasi-static providing the constant amp-second relationship described in equation (5).

The off-time controller comprises of a current source proportional to the difference between the output and input voltage ($V_{OUT}$-$V_{IN}$), a resettable integrator and a comparator. In this circuit block the integrating capacitor voltage level is controlled by a fixed reference providing an off-time that has constant volt-second relationship described in (3). The output of the off-time control comparator 'sets' the latch to terminate the off-time and begin the on-time of that particular cycle.

The idealized pertinent control signals of the on-time and off-time controllers are shown below.

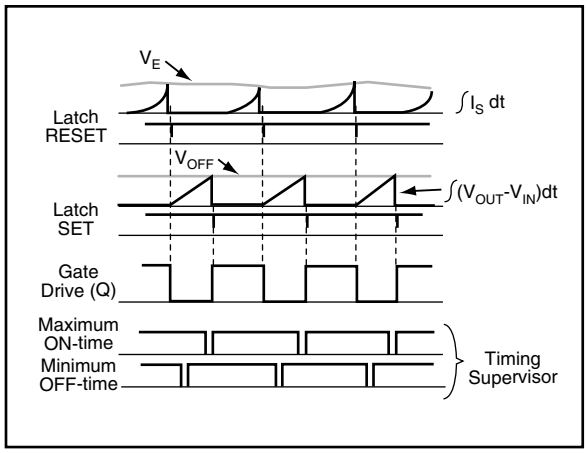



*Figure 6. Idealized Control Waveform.*

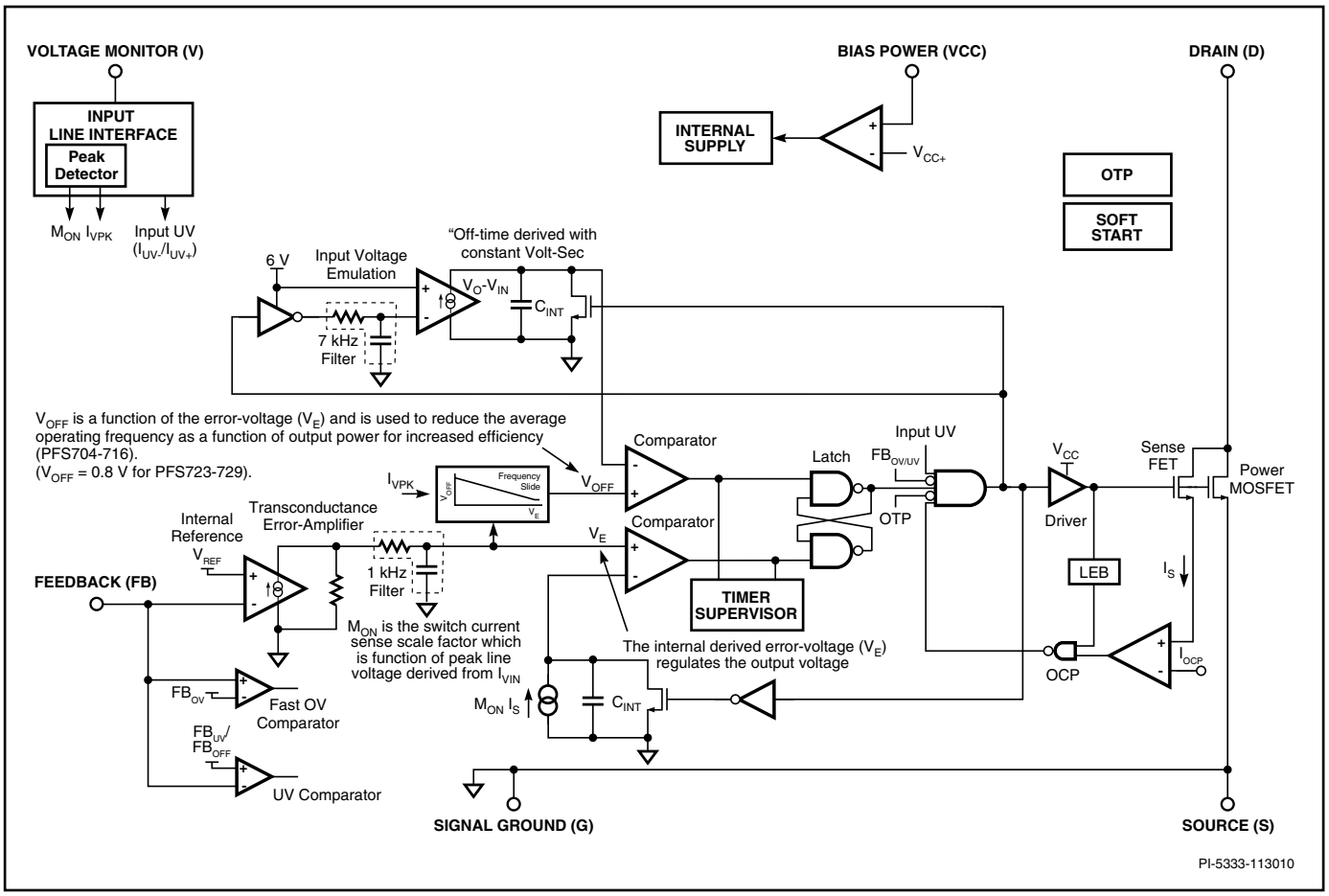



*Figure 5. HiperPFS Block Diagram.*

### Off-time Control

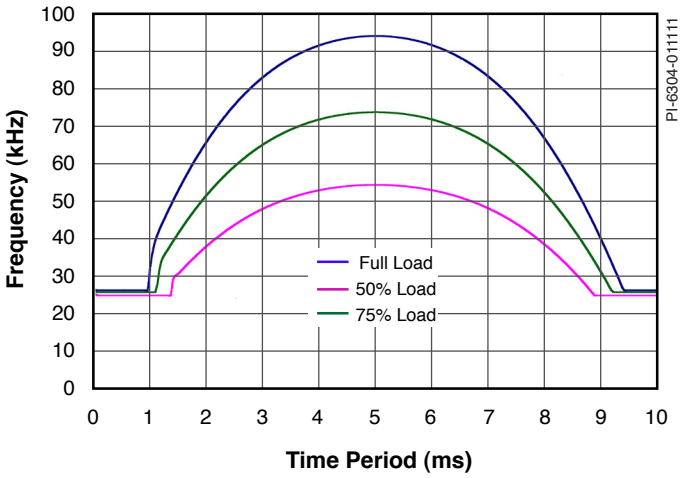



*Figure 7. Frequency Variation with Load.*

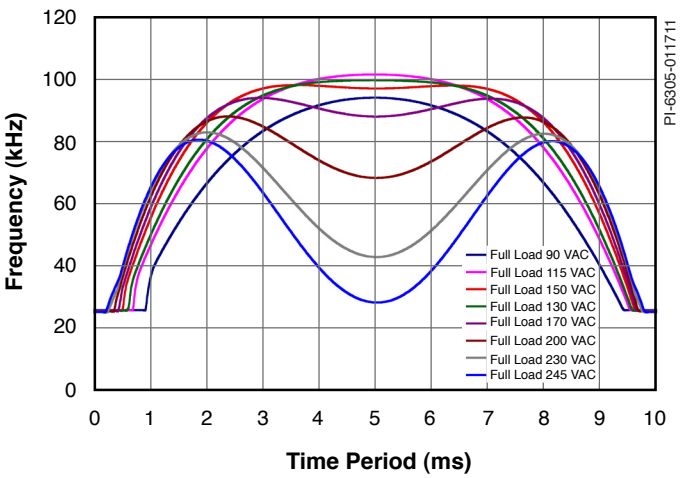



*Figure 8. Frequency Variation with Input Voltage Change (100% Load at Output).*

As the peak input voltage approaches the output voltage the difference between these two quantities approaches zero and the required time to satisfy volt-second balance increases. This relationship is apparent upon closer examination of the off-time controller shown in Figure 6.

The off-time is derived through a transconductance amplifier which produces a current that is proportional to the difference between $V_{OUT}$ and $V_{IN}$. As $V_{OUT}$-$V_{IN}$ approaches zero, which is the case when the peak of the input voltage is close to the set output voltage regulation threshold, the off-time current source reduces.

As a natural consequence the rate in which the integrating capacitor is charged toward the off-time control reference is decreased causing the off-time to increase. Theoretically for this type of control, the resultant off-time when $V_{OUT}$ is equal to $V_{IN}$ is infinity.

The HiperPFS includes a timer supervisor function to limit both the minimum and maximum switch on and off times. Specifically, limiting the maximum off-time prevents the controller from causing audible noise in the boost choke if the required switching frequency falls below ~20 kHz for a load in excess of 20% of the device peak power rating. The specified maximum off-time in the HiperPFS is limited to between 30 µs to 40 µs.

The operating frequency of the PFC changes as a function of load level and also as a function of line voltage. The frequency plots shown in Figure 7 and Figure 8 can be used to estimate the operating frequency depending on input voltage and load.

## Designing with HiperPFS

### Quick Start

Readers willing to start immediately can use the following information to quickly design the inductor and select the components for a first prototype. Only the information described below needs to be entered into the PIXIs spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter the voltage range for the design [B3]
  - Universal should be selected if the application requires a wide operating voltage range. High-line should be selected for applications that only are required to work with 220 V / 240 V nominal AC supply.
- Enter AC input voltage range $VAC_{MIN}$, $VAC_{MAX}$ and minimum line frequency $f_L$ [B4, B5, B10]
- Enter nominal output voltage $V_O$ [B8]
- Enter maximum continuous output power [B9]
- Enter efficiency estimate at $VAC_{MIN}$ [B12]
  - 0.93 for universal input voltage (85 - 265 VAC) or single 100 / 115 VAC (85 -132 VAC) and 0.96 for a single 230 VAC (180 - 265 VAC) design. Correct the number after measuring the efficiency of the prototype board at full load and $VAC_{MIN}$.
- Enter maximum operating temperature [B11]
  - If left unpopulated the default value is 40 ºC
- Enter maximum output ripple [B15]
  - If no specific information is provided a default value of 20 V is used
- Enter hold-up time required [B16]
  - 16 ms or 20 ms are standard requirements for most high performance designs
  - Use 10 ms if long hold-up time is not a requirement
  - If this cell is left blank then the output capacitance value is calculated for a hold-up time of 20 ms
- Enter minimum PFC output voltage at the end of the hold-up interval [B17]
  - 310 V is typically adequate for most second stage converters to maintain regulation.
  - Use 310 V if no specific information is available
- Select a suitable HiperPFS device and enter directly [B23]
  - Select the device in Table 1 according to output power and line input voltage. If this filed is left as “Auto” a suitable device will be selected automatically.

### Output Power Table

| Product | Maximum Continuous Output Power Rating at 90 VAC | Peak Output Power Rating at 90 VAC |
|---|---|---|
| **PFS704EG** | 110 W | 120 W |
| **PFS706EG** | 140 W | 150 W |
| **PFS708EG** | 190 W | 205 W |
| **PFS710EG** | 240 W | 260 W |
| **PFS712EG** | 300 W | 320 W |
| **PFS714EG** | 350 W | 385 W |
| **PFS716EG** | 388 W | 425 W |
| **Product** | **Maximum Continuous Output Power Rating at 180 VAC** | **Peak Output Power Rating at 180 VAC** |
| **PFS723EG** | 255 W | 280 W |
| **PFS724EG** | 315 W | 350 W |
| **PFS725EG** | 435 W | 480 W |
| **PFS726EG** | 540 W | 600 W |
| **PFS727EG** | 675 W | 750 W |
| **PFS728EG** | 810 W | 900 W |
| **PFS729EG** | 900 W | 1000 W |

*Table 1. Output Power Table.*

Notes:
1. Maximum practical continuous power at 90 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.
2. Maximum practical continuous power at 180 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.

### Table 1 Output Power Table

- Enter core type (if desired) from drop down menu [B51]
  - A suggested core size will be selected automatically if none is entered

If any warnings are generated, make changes to the design by following instructions in spreadsheet column F
- Build the inductor
- Select key components
  - See Steps 7 through 12.
- Build prototype and iterate design as necessary, entering measured values into spreadsheet where estimates were used (e.g. efficiency, $V_{MIN}$).

## Step-by-Step Design Procedure Introduction

The design flow allows for design of a PFC stage for a rated continuous output power requirement. Operating conditions of a power supply and test results of evaluation may require design changes for performance optimization and this design flow should be used to iterate a design as necessary.

The power table (Table 1) provides guidance for selection of a suitable HiperPFS device for a design. Selection should be based on the operating conditions such as maximum operating temperature and the desired operating voltage range. This approach ensures that the selected device can deliver the required output power at minimum input line voltage.

### Step 1 – Enter Application Variables $VAC_{MIN}$, $VAC_{MAX}$, $f_L$, $V_O$, $P_O$, $\eta$, $K_P$, $V_{OUTRIPPLE}$, $t_{HOLDUP}$, $V_{HOLDUP}$, $I_{INRUSH}$

Determine the input voltage range from Table 2.

| Nominal Input Voltage (VAC) | $VAC_{MIN}$ | $VAC_{MAX}$ |
|---|---|---|
| 100 / 115 | 90 | 132 |
| 230 (High-Line Only) | 180 | 265 |
| Universal | 90 | 265 |

*Table 2. Standard Worldwide Input Line Voltage Ranges.*

#### Brownout Voltage $V_{BROWNOUT}$ (V)

This is the voltage at which the power supply will shutdown due to input undervoltage. During the initial design stage the desired value should be adjusted by changing $V_{AC(MIN)}$ and will determine the correct value of the V pin resistors to program $V_{BROWNOUT}$. Once a prototype has been constructed the actual measured value of the lowest line voltage at which the converter still operates should be entered.

#### Nominal Output Voltage, $V_O$ (V)

Enter the nominal output voltage of the PFC. The HiperPFS is designed for continuous operation at an output voltage of 385 VDC. Higher output voltages are not recommended due to increased voltage stress on the internal MOSFET. A lower output voltage may be used for applications that require operation only at 100 / 115 VAC nominal, providing the output

| Enter Applications Variables | | | | | |
|---|---|---|---|---|---|
| Input Voltage Range | **Universal** | | **Universal** | | Select Universal or High_Line option |
| VACMIN | | | 90 | V | Minimum AC input voltage |
| VACMAX | | | 265 | V | Maximum AC input voltage |
| VBROWNIN | | | 77.76 | | Expected Minimum Brown-in Voltage |
| VBROWNOUT | | | 70.4 | V | Specify brownout voltage. |
| VO | 385 | | | V | Nominal Output voltage |
| PO | 347 | | | W | Nominal Output power |
| fL | | | 50 | Hz | Line frequency |
| TA Max | | | 40 | °C | Maximum ambient temperature |
| n | | | 0.93 | | Enter the efficiency estimate for the boost converter at VACMIN |
| KP | 0.677 | | 0.677 | | Ripple to peak inductor current ratio at the peak of VACMIN |
| VO_MIN | | | 365.75 | V | Minimum Output voltage |
| VO_RIPPLE_MAX | | | 20 | V | Maximum Output voltage ripple |
| tHOLDUP | 16 | | 16 | ms | Holdup time |
| VHOLDUP_MIN | | | 310 | V | Minimum Voltage Output can drop to during holdup |
| I_INRUSH | | | 40 | A | Maximum allowable inrush current |
| Forced Air Cooling | **Yes** | | **Yes** | | Enter "Yes" for Forced air cooling. Otherwise enter "No" |

*Figure 9. Application Variable Section of HiperPFS Design Spreadsheet.*

voltage is greater than the peak of the maximum AC input voltage.

**Nominal Output Power, $P_O$ (W)**
Enter the maximum continuous output power of the PFC. If the PFC is required to meet a peak power specification, the peak power should be entered in this cell.

**Line Frequency, $F_L$**
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst case or based on the product specification, reduce these numbers by 6% (47 Hz or 56 Hz) as necessary.

**Ambient Temperature, $T_{A(MAX)}$**
A default value of 40 ºC is assumed for maximum ambient temperature. If the ambient temperature inside the power supply enclosure is higher than this value, the expected internal ambient temperature should be entered in this cell. This value will be used for calculation of the estimated thermal resistance of the heat sinks for the HiperPFS and the PFC output diode.

**Power Supply Efficiency, η**
Enter the estimated efficiency of the PFC stage at the lowest input voltage specified as $VAC_{MIN}$. Start with a value of 0.93 for universal input designs and 0.96 for 230 VAC only designs. Once a prototype has been constructed, the measured efficiency should be entered and further inductor design iteration performed if required.

**Ripple to Peak Current Ratio, $K_P$**
The HiperPFS is a (Continuous Conduction Mode) CCM PFC. The factor $K_P$ is a ratio of the ripple component in the inductor current as compared to the peak inductor current at the peak of the sine wave as shown in Figure 10. For a CCM mode operation the value of $K_P$ is required to be less than 1.

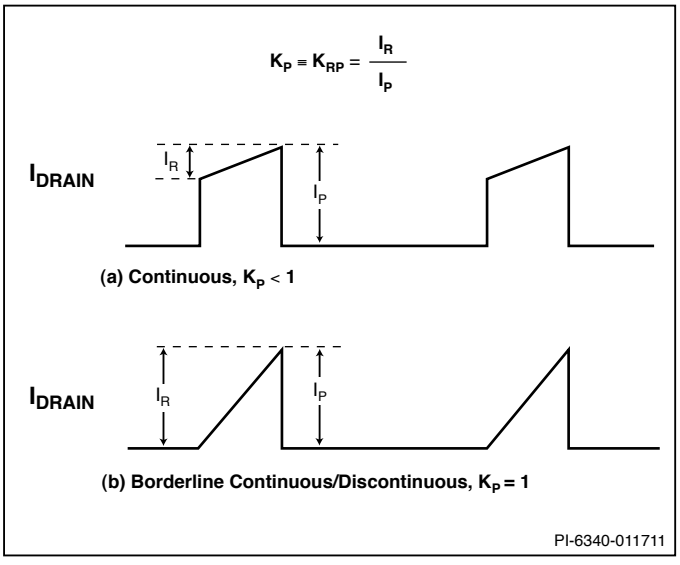



*Figure 10. Continuous Mode Current Waveform, $K_P \leq 1$.*

A lower value of $K_P$ results in a higher inductance however a higher inductance results in lower THD of input current and a higher PF. As a start, for high-line only designs, a starting value of 0.5 or 0.675 should be used for ferrite core and powder core designs respectively. For universal input designs, a value of 0.25 or 0.675 should be used for ferrite core and powder core designs respectively. If further improvement in PF is required after evaluation of the PFC performance, one option to improve PF is to lower the value of $K_P$ and iterate the inductor design.

**Output Voltage Ripple, $V_{OUTRIPPLE(MAX)}$**
Enter maximum permissible output ripple voltage. A default value of 20 V is used if this field is left blank which is typical for most applications.

**Hold-Up Time, $t_{HOLDUP}$**
Enter the hold-up time specification required to be met, this being the time the PFC stage output capacitor must supply to load during a line dropout during which the output voltage falls to $V_{HOLDUP(MIN)}$.

**Voltage at the end of Hold-Up Time, $V_{HOLDUP(MIN)}$**
In order to sustain operation, the load on the PFC will often require that the PFC output voltage remain above a certain minimum value at the end of hold-up time. Enter the minimum voltage expected at the output of the PFC at the end of hold-up time. A value of 310 V will be acceptable for most designs that use a second stage converter based on the HiperTFS.

Both $V_{OUTRIPPLE(MAX)}$, $t_{HOLDUP}$ and $V_{HOLDUP(MIN)}$ are used to calculate the output capacitance.

**Maximum Inrush Current Permissible, $I_{INRUSH}$**
Enter total maximum permissible inrush current in this cell. This information is used by the spreadsheet to determine the minimum resistance of the inrush limiting thermistor required.

**Forced Air Cooling - Option**
Enter “YES” if forced air cooling is used otherwise enter “NO”. In a forced air cooled design, higher current density can be used in the inductor winding which enables use of thinner wires reducing cost, size and weight of the inductor.

### Step 2 – Enter HiperPFS Variables: HiperPFS Device, Line Sense Resistor $R_V$, $T_{J(MAX)}$, Thermal Resistance of HiperPFS Assembly

**Select the Correct HiperPFS Device**
Refer to the HiperPFS power table and select a device based on the output power of the design. If the continuous power exceeds the value given in the power table then the next largest device should be selected. If the “Auto” option is selected, the spreadsheet will automatically select the most suitable device based on application variables entered in Step 1. Close attention should be paid to the notes associated with the power table. For some designs, it may be necessary to use the next higher device depending on the specifics of the application.

**Select the Line Sense Resistor Value, $R_V$**
The line sense resistor programs the feed forward gain for the PFC controller and also sets the brown-in and brown-out thresholds. The recommended value of the line sense resistor

| PFS Parameters | | | | | |
|---|---|---|---|---|---|
| PFS Part Number | Auto | | PFS714 | | Selected PFS device |
| IOCP min | | | 9 | A | Minimum Current limit |
| IOCP typ | | | 9.95 | A | Typical current limit |
| IOCP max | | | 10.9 | A | Maximum current limit |
| RDSON | | | 0.46 | ohms | Typical RDSon at 100 'C |
| RV | | | 4 | Mohms | Line sense resistor |
| C_VCC | | | 1 | uF | Supply decoupling capacitor |
| C_V | | | 100 | nF | V pin decoupling capacitor |
| C_FB | | | 10 | nF | Feedback pin decoupling capacitor |
| FS_PK | | | 84.93 | kHz | Estimated peak frequency of operation |
| FS_AVG | | | 69.13 | kHz | Estimated average frequency of operation |
| IP | | | 8.84 | A | MOSFET peak current |
| PFS_IRMS | | | 4.02 | A | PFS MOSFET RMS current |
| PCOND_LOSS_PFS | | | 7.43 | W | Estimated PFS conduction losses |
| PSW_LOSS_PFS | | | 2.85 | W | Estimated PFS switching losses |
| PFS_TOTAL | | | 10.28 | W | Total Estimated PFS losses |
| TJ Max | | | 100 | °C | Maximum steady-state junction temperature |
| Rth-JS | | | 3 | °C/W | Maximum thermal resistance (Junction to heat sink) |
| HEAT SINK Theta-CA | | | 2.83 | °C/W | Maximum thermal resistance of heat sink |

*Figure 11. PFS Parameters Section of the HiperPFS Spreadsheet.*

for Universal input applications is 4 MΩ and the recommended for a high-line only application is 9 MΩ. These values may be adjusted to change the brown-in and brown-out voltage levels by entering the desired value in MΩ in this cell. A warning will be generated if a change is being made to the value of this resistance beyond permissible limits.

**Select the Operating Junction Temperature Maximum for the HiperPFS, $T_{J(MAX)}$**

The default value of the operating junction temperature for the HiperPFS is set to 100 ºC. This ensures that there is sufficient margin to ensure reliability and safe operation including during brown-out testing. A different value may be used if required however higher value are generally not recommended.

**Select the Thermal Resistance-Junction to Heat Sink for the HiperPFS, $R_{th-JS}$**

The default value of the thermal resistance is set to 3 ºC/W assuming use of a heat spreader and thermally conductive insulator between the heat spreader and the heat sink. If no better information is available, the value of 3 ºC/W should be used. Additional information regarding thermal design and its effects on thermal resistance are explained in subsequent sections of the application note. The spreadsheet calculates the estimated value of the thermal resistance (surface – ambient) for the heat sink that may be necessary for the HiperPFS part selected, based on the estimated losses in the device.

### Step 3 – Choose Core and Winding Based on Output Power and Enter $A_E$, $L_E$, $A_L$, BW, MLT

Core effective cross-sectional area, $A_E$: ($mm^2$)
Core effective path length, $L_E$: (mm).
Core ungapped effective inductance factor, $A_L$: ($nH/turn^2$).
Bobbin width, BW: (mm)
Mean length per turn: (mm)

**Core Type**

By default, if the "Core Type" cell is left empty, the spreadsheet will select the smallest commonly available core suitable for the continuous (average) output power specified. The entire list of cores available can be shown by selecting the drop down list in the tool bar of the PIXls design software. The gray override cells can be used to enter the core and bobbin parameter directly by the user. This is useful if a core is selected that is not on the list or the specific core or bobbin information differs from that recalled by the spreadsheet.

Sendust, ferrite and iron powder are three choices that are available for selection. Sendust cores are a cost effective option. Ferrite core inductors have the lowest core loss; however it is often difficult to achieve a high inductance without using a large core size. Iron powder cores offer the cheapest alternative however, core loss can be significant.

**Core Material**

When the Sendust core type is selected, four different permeability options are available for selection using a drop down menu. Core material with 60 μ, 75 μ, 90 μ or 125 μ, can be selected. High permeability materials will yield a higher 0-bias inductance for the same number of turns. Inductors made with high permeability cores will typically reduce in inductance with flux bias. The increase in inductance with drop in current helps the PFC to maintain CCM operation at light load levels and is beneficial in maintaining a high PF and low input current THD ($I_{THD}$) even at light load levels.

Only the -52 material is supported for iron powder cores and PC44 material is supported for ferrite cores. Other material types may also be used, however the loss calculations will not be accurate.

**Core Geometry**

A choice of EE or toroidal core geometry is available for Sendust core type. For ferrite, either EE or PQ core geometry is available as a standard choice. Only toroid geometry is available as a choice for iron powder cores. Parameter values for the selected core are updated automatically. If the core parameters are different as compared to the ones shown in the spreadsheet, they can be entered in the gray cells in the list and the spreadsheet will update the calculation results.

| Inductor Construction Parameters | | | | | |
|---|---|---|---|---|---|
| Core Type | **Sendust** | | **Sendust** | | Enter "Sendust", "Pow Iron" or "Ferrite" |
| Core Material | **Auto** | | **125u** | | Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44 or equivalent for Ferrite cores. Fixed at 52 material for Pow Iron cores. |
| Core Geometry | **Auto** | | **TOROID** | | Select from Toroid or EE for Sendust cores and from EE, or PQ for Ferrite cores |
| Core | **77324 (OD=36.7)** | | **77324 (OD=36.7)** | | Core part number |
| AE | | | 67.8 | mm^2 | Core cross sectional area |
| LE | | | 89.8 | mm | Core mean path length |
| AL | | | 119 | nH/t^2 | Core AL value |
| VE | | | 6088 | mm^3 | Core volume |
| HT | | | 11.35 | mm | Core height/Height of window |
| MLT | | | 43.4 | cm | Mean length per turn |
| BW | | | N/A | mm | Bobbin width |
| NL | | | 108 | | Inductor turns |
| LG | | | N/A | mm | Gap length (Ferrite cores only) |
| ILRMS | | | 4.77 | A | Inductor RMS current |
| Wire type | **LITZ** | | | | Select between "Litz" or "Regular" for double coated magnet wire |
| AWG | 40 | | 40 | AWG | Inductor wire gauge |
| Filar | 125 | | 125 | | Inductor wire number of parallel strands |
| OD | | | 0.079 | mm | Outer diameter of single strand of wire |
| AC Resistance Ratio | | | 1.09 | | Ratio of AC resistance to the DC resistance (using Dowell curves) |
| J | | | 7.84 | A/mm^2 | Estimated current density of wires. It is recommended that 6 < J < 8 |
| BM_TARGET | | | N/A | Gauss | Target flux density at VACMIN (Ferrite cores only) |
| BM | | | 2591 | Gauss | Maximum operating flux density |
| BP | | | 6898 | Gauss | Peak Flux density (Estimated at VBROWNOUT) |
| LPFC_CORE_LOSS | | | 2.26 | W | Estimated Inductor core Loss |
| LPFC_COPPER_LOSS | | | 2.59 | W | Estimated Inductor copper losses |
| LPFC_TOTAL LOSS | | | 4.85 | W | Total estimated Inductor Losses |

*Figure 12. Inductor Core and Construction Variables Section of Spreadsheet.*

### Wire Type
By default the LITZ wire option is selected. Litz wires offer the lowest proximity and skin effect losses and hence provide the highest efficiency for most designs. Regular (double coated) magnet wires with a single or multi strand construction may also be used by entering REGULAR.

### Wire Gauge AWG
If the Litz wire option is selected, PIXIs will select a Litz wire with the appropriate number of strands and wire gauge and the result will be updated. If a different Litz wire is preferred, the wire gauge (AWG) and number of strands should be entered in the cells.

### Number of Strands
For a Litz wire selection, the number of strands is selected automatically. This choice can be changed by entering the number of strands in the cell [B67]. While a multi-filar construction reduces AC losses, it can also lead to higher proximity losses. The copper loss calculation corrects for proximity loss based on the wire gauge (AWG) selected.

### Wire Diameter
If the wire diameter is different from the wire diameter displayed, cell [B68] can be changed to show the actual diameter of wire.

### Target Flux Density
For ferrite cores, the target flux density is set to 3000 G (0.3 T). If a higher flux density is to be selected, cell [B71] should be changed. Choice of a higher flux density should be made after careful consideration of core material saturation characteristics at high temperature.

The spreadsheet will calculate the number of turns required and the inductance value. The expected inductance with no DC-bias is calculated. This is the expected inductance value when measured using an LCR meter.

### Step 4 – Iterate Inductor Design and Generate Initial Design

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warnings have been cleared, the inductor design parameters can be used to either wind a prototype inductor or sent to a vendor for samples.

The Key Inductor Electrical Parameters:

### Primary Inductance, $L_{PFC(0\text{-}BIAS)}$ (µH)
This is the target nominal primary inductance of the transformer.

### Primary Inductance Tolerance, $L_{P(TOLERANCE)}$ (%)
This is the assumed primary inductance tolerance. A value of 12% is used by default, however if specific information is known from the magnetics vendor, then this may be entered in the gray override cell.

| Basic Inductor Calculation | | | | | |
|---|---|---|---|---|---|
| LPFC | | | 150.47 | uH | Value of PFC inductor at peak of VACMIN and Full Load |
| LPFC (0 Bias) | | | 1383.32 | uH | Value of PFC inductor at No load. This is the value measured with LCR meter |
| LPFC_RMS | | | 4.77 | A | Inductor RMS current (calculated at VACMIN and Full Load) |

*Figure 13. Induction Calculation Section of HiperPFS Design Spreadsheet.*

### Gapped Core Effective Inductance, $A_{LG}$ (nH/t²)
Used by the transformer vendor to specify the core (gap). This information is only required for ferrite core designs.

### Maximum Operating Flux Density, $B_M$ (Gauss)
For ferrite cores, a maximum value of 3000 Gauss (0.3 T) during normal operation is recommended to limit the maximum flux density under start-up and output overload conditions.

### Peak Flux Density, $B_P$ (Gauss)
For ferrite cores, a maximum value of 4200 Gauss (0.42 T) is recommended to limit the maximum flux density under start-up and output overload conditions. This calculation assumes worst-case current limit specification and inductance value. In high ambient temperature applications, such as sealed adapters, this value may need to be reduced to 3600 Gauss. To determine the correct value, verify that core saturation does not occur at maximum ambient during start-up.

### Step 5 – Selection of Output Diode

For a CCM PFC, use of ultrafast recovery diodes is recommended to reduce losses. Special diodes optimized for PFC application are available from various manufacturers and are also suitable for HiperPFS designs. These diodes have both soft recovery characteristics and low $Q_{RR}$ that reduce EMI under the hard switching of CCM operation while simultaneously reducing forward conduction and switching losses.

The spreadsheet automatically selects a diode with forward current rating suitable for the specified output power. The peak current through the PFC output diode is same as the PFS-MOSFET peak current. A different diode can be selected from the drop down list. If any warnings are generated, selection of a different diode is necessary.

The diode parameters such as $t_{RR}$, $V_F$ etc. can be modified based on actual operating conditions and data sheet information. Change of diode $V_F$ or $t_{RR}$ parameter affects diode losses. If a different diode is used, these numbers should be updated in the diode parameter cells [B91] and [B92].

Typically the diodes will be required to have a forward continuous current rating of at least 1.2 A to 1.5 A for every 100 W of output power.

| Diode Part Number | Type | Manufacturer | Voltage Rating (V) | Current Rating (A) |
|---|---|---|---|---|
| LQA03TC600 | Special | Power Integrations | 600 | 3 |
| LQA05TC600 | Special | Power Integrations | 600 | 5 |
| LQA08TC600 | Special | Power Integrations | 600 | 8 |
| LXA04T600 | Special | Power Integrations | 600 | 4 |
| LXA06T600 | Special | Power Integrations | 600 | 6 |
| LXA08T600 | Special | Power Integrations | 600 | 8 |
| STTH1R06 | Ultrafast | ST | 600 | 2 |
| STTH2R06 | Ultrafast | ST | 600 | 2 |
| STTH3R06 | Ultrafast | ST | 600 | 3 |
| STTH506 | Ultrafast | ST | 600 | 5 |
| STTH506D | Ultrafast | ST | 600 | 5 |
| STTH5R06 | Ultrafast | ST | 600 | 5 |
| STTH806 | Ultrafast | ST | 600 | 8 |
| STTH806TTI | Ultrafast | ST | 600 | 8 |
| STTH8R06 | Ultrafast | ST | 600 | 8 |
| STTH8S06 | Ultrafast | ST | 600 | 8 |
| STTH12R06 | Ultrafast | ST | 600 | 12 |
| CSD01060 | SiC | CREE | 600 | 1 |
| CSD02060 | SiC | CREE | 600 | 2 |
| CSD04060 | SiC | CREE | 600 | 4 |
| CSD06060A | SiC | CREE | 600 | 6 |
| CSD08060A | SiC | CREE | 600 | 8 |
| CSD10060A | SiC | CREE | 600 | 10 |
| HFA04TB60 | Ultrafast | Vishay | 600 | 4 |
| HFA08TB60 | Ultrafast | Vishay | 600 | 4 |
| HFA16TA60C | Ultrafast | Vishay | 600 | 16 |

*Table 3. Diodes Suitable for PFC Application.*

### Diode Junction Temperature, $T_{JMAX}$
A default value of 125 ºC as the maximum junction operating temperature is used for the diode. If a lower stress level is desirable, this value should be entered in the cell [B96]. The diode thermal resistance depends on the package selected. If the thermal resistance of the package is different as compared to the one used by the spreadsheet, enter the value in cell [B97].

| Output Diode | | | | | |
|---|---|---|---|---|---|
| Part Number | Auto | | STTH8S06 | | PFC Diode Part Number |
| Type | | | ULTRAFAST | | Diode Type - Special - Diodes specially catered for PFC applications, SiC - Silicon Carbide type, UF - Ultrafast recovery type |
| Manufacturer | | | ST | | Diode Manufacturer |
| VRRM | | | 600 | V | Diode rated reverse voltage |
| IF | | | 8 | A | Diode rated forward current |
| TRR | | | 33 | ns | Diode Reverse recovery time |
| VF | | | 1.1 | V | Diode rated forward voltage drop |
| PCOND_DIODE | | | 0.99 | W | Estimated Diode conduction losses |
| PSW_DIODE | | | 2.15 | W | Estimated Diode switching losses |
| P_DIODE | | | 3.14 | W | Total estimated Diode losses |
| TJ Max | | | 125 | °C | Maximum Operating temperature |
| Rth-JS | | | 3 | °C/W | Maximum thermal resistance (Junction to heat sink) |
| HEAT SINK Theta-CA | | | 23.57 | °C/W | Maximum thermal resistance of heat sink |

*Figure 14. Output Diode Section Of HiperPFS Design Spreadsheet.*

The spreadsheet calculates the maximum permissible heat sink thermal resistance that may be usable for the diode selected and based on the output power of the PFC. Heat sink temperature should be measured on a prototype unit and necessary changes made in order to optimize the design.

### Step 6 – Selection of PFC Output Capacitor

Selection of the output capacitor depends on the expected hold-up time and the permissible output ripple. The spreadsheet automatically selects the most suitable capacitor depending on the hold-up time and output ripple specified in the applications variable section.

The low frequency ESR value is the specified ESR at 100 Hz / 120 Hz and the high frequency ESR value is the ESR at 20 kHz. If the low frequency and high frequency ESR values are different for the capacitor selected, enter the appropriate values in cell [B106] and [B107].

Power is dissipated in the output capacitor due to the low frequency and high frequency ripple currents. The spreadsheet estimates these losses which can be used for thermal calculations to estimate temperature rise of the capacitor.

### Step 7 – Selection of Other Circuit Components

The spreadsheet provides recommended values or parameter values for selection of the balance circuit components to complete the design.

#### Fuse Current Rating and I²t Rating

Fuse continuous current rating and the required I²t rating are calculated in the spreadsheet. These values can be used to select a suitable fuse.

#### Input Bridge Rectifier

The average input rectifier current, peak inverse voltage and total power dissipation is calculated in the spreadsheet. The estimated bridge rectifier power dissipation is dependent on the forward voltage drop of the diodes in the bridge rectifier. If the forward voltage drop is different from the one shown in cell [E119], enter the diode forward voltage drop in the cell [B119]. Bridge rectifier with at least a 600 V PIV rating is recommended for a universal input design. For designs with only a 115 V / 100 V nominal input voltages, bridge rectifiers with PIV rating as low as 400 V can be used.

#### Input Filter Capacitor

A filter capacitor with low ESR and low ESL is recommended to be placed after the bridge rectifier. This capacitor helps to reduce EMI. The required value is estimated by the spreadsheet.

#### Input Thermistor $R_T$

The cold state resistance of the thermistor required to guarantee the maximum inrush current specification in the applications variables section is calculated. A thermistor with a continuous current rating exceeding the calculated input RMS current and the calculated value of $R_T$ should be used.

#### Output Capacitor Pre-Charge Diode

A diode is used to bypass the PFC inductor at start in order to route the charging current for the output capacitor away from the inductor. In the absence of this diode, the capacitor charging current flows through the inductor and the resonance between the inductor and the output capacitor causes the output voltage to be as high as twice the input voltage which can result in failure of the capacitor and other circuit components.

| **Output Capacitor** | | | | | |
|---|---|---|---|---|---|
| CO | **Auto** | | **270** | uF | Minimum value of Output capacitance |
| VO_RIPPLE_EXPECTED | | | 11.4 | V | Expected ripple voltage on Output with selected Output capacitor |
| T_HOLDUP_EXPECTED | | | 18.4 | ms | Expected holdup time with selected Output capacitor |
| ESR_LF | | | 0.68 | ohms | |
| ESR_HF | | | 0.27 | ohms | |
| IC_RMS_LF | | | 0.64 | A | Low Frequency Capacitor RMS current |
| IC_RMS_HF | | | 1.83 | A | High Frequency Capacitor RMS current |
| **Critical Parameters** | | | | | |
| IRMS | | | 4.15 | A | AC input RMS current |
| IO_AVG | | | 0.9 | A | Output average current |

*Figure 15. Output Capacitor Section of HiperPFS Design Spreadsheet.*

| **Input Bridge and Fuse** | | | | | |
|---|---|---|---|---|---|
| I^2t Rating | | | 18.96 | A^2s | Minimum I^2t rating for fuse |
| Fuse Current rating | | | 6.3 | A | Minimum Current rating of fuse |
| VF | | | 0.9 | V | Input bridge Diode forward Diode drop |
| IAVG | | | 3.92 | A | Input average current at 70 VAC. |
| PIV_INPUT BRIDGE | | | 375 | V | Peak inverse voltage of input bridge |
| PCOND_LOSS_BRIDGE | | | 6.72 | W | Estimated Bridge Diode conduction loss |
| CIN | | | 1 | uF | Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating |
| RT | | | 7.54 | ohms | Input Thermistor value |
| D_Precharge | | | 1N5407 | | Recommended precharge Diode |

*Figure 16. Input and Bridge Section of HiperPFS Design Spreadsheet.*

| **Critical Parameters** | | | | | |
|---|---|---|---|---|---|
| IRMS | | | 4.15 | A | AC input RMS current |
| IO_AVG | | | 0.9 | A | Output average current |

*Figure 17. Critical Parameters Section of HiperPFS Design Spreadsheet.*

The spreadsheet selects either the 1N4007 or the 1N5407 diode to ensure that the diode surge current rating is not exceeded during the pre-charge of the output capacitor.

**Feedback Circuit Components**

A feedback circuit arrangement comprising of a voltage divider network, compensation elements and a set of general purpose transistors is recommended for use with the HiperPFS. This simple arrangement ensures that loop stability is achieved while simultaneously ensuring that the circuit responds to any transient conditions rapidly, without the delays of a low bandwidth control loop. Figure 18 shows the minimum recommended circuit with the reference designators matching those in Figure 19.

The feedback circuit components are calculated in the feedback components section. Component values closest to the values shown should be used. If component values used are different from the values shown in the spreadsheet, the output voltage of the PFC will be different and some adjustment of resistor values will be required.

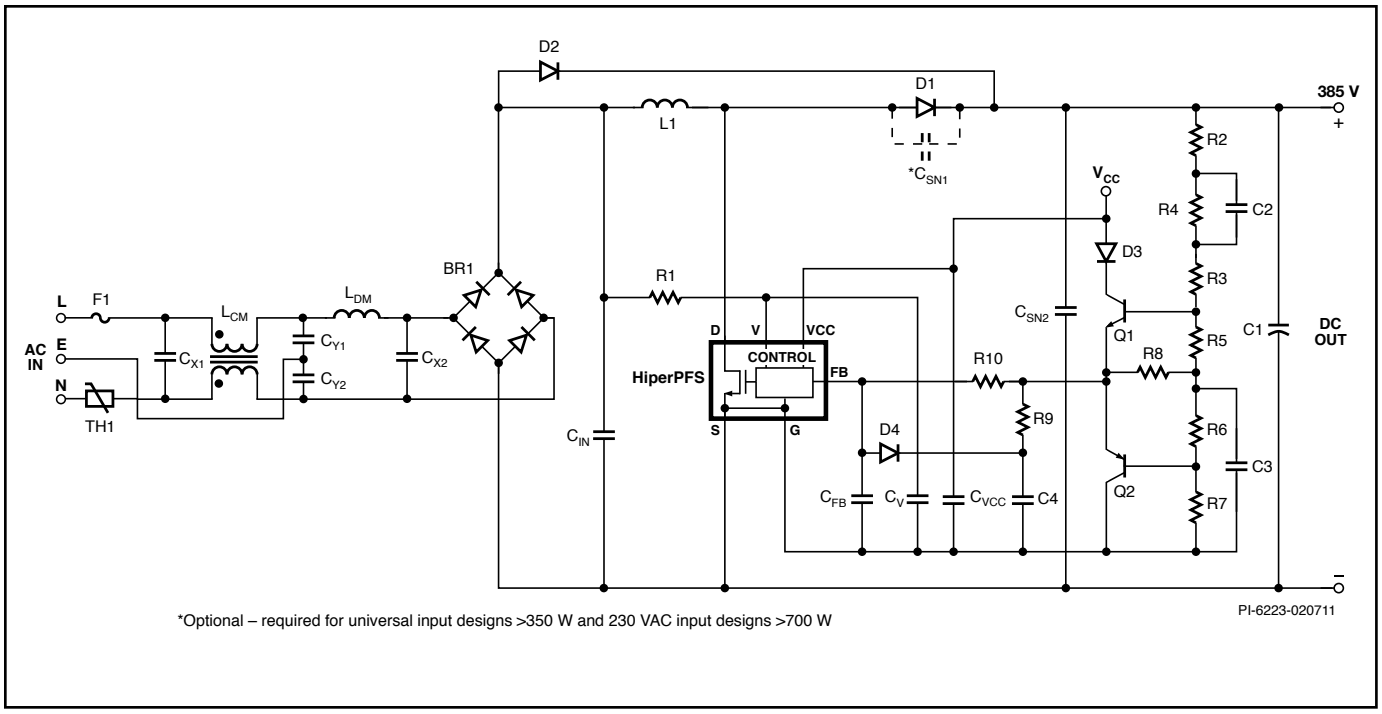



*Figure 18. Minimum Recommended Circuit for HiperPFS.*

| Feedback Components | | | | | |
|---|---|---|---|---|---|
| R2 | | | 1.54 | Mohms | Feedback network, first high voltage divider resistor |
| R3 | | | 1.54 | Mohms | Feedback network, second high voltage divider resistor |
| R4 | | | 698 | kohms | Feedback network, third high voltage divider resistor |
| C2 | | | 100 | nF | Feedback network, loop speedup capacitor |
| R5 | | | 2.2 | kohms | Feedback component, NPN transistor bias resistor |
| R6 | | | 2.2 | kohms | Feedback component, PNP transistor bias resistor |
| R7 | | | 57.6 | kohms | Feedback network, lower divider resistor |
| C3 | | | 470 | pF | Feedback component- noise suppression capacitor |
| R8 | | | 160 | kohms | Feedback network - pole setting resistor |
| R9 | | | 2.32 | kohms | Feedback network - zero setting resistor |
| R10 | | | 10 | kohms | Feedback pin filter resistor |
| C4 | | | 10 | uF | Feedback network - compensation capacitor |
| D3 | | | 1N4148 | | Feedback network reverse blocking Diode |
| D4 | | | 1N4001 | | Feedback network - capacitor failure detection Diode |
| Q1 | | | 2N4401 | | Feedback network - speedup circuit NPN transistor |
| Q2 | | | 2N4403 | | Feedback network - speedup circuit PNP transistor |

*Figure 19. Feedback and Components Section of HiperPFS Design Spreadsheet.*

| Loss Budget (Estimated at VACMIN) | | | | | |
|---|---|---|---|---|---|
| PFS Losses | | | 10.28 | W | Total estimated losses in PFS |
| Boost diode Losses | | | 3.14 | W | Total estimated losses in Output Diode |
| Input Bridge losses | | | 6.72 | W | Total estimated losses in input bridge module |
| Inductor losses | | | 4.85 | W | Total estimated losses in PFC choke |
| Output Capacitor Loss | | | 1.18 | W | Total estimated losses in Output capacitor |
| Total losses | | | 26.18 | W | Overall loss estimate |
| Efficiency | | | 0.93 | | Estimated efficiency at VACMIN. Verify efficiency at other line voltages |

*Figure 20. Loss Budget Section of HiperPFS Design Spreadsheet.*

### Step 8 – Verify Loss Budget

Power dissipation in the key components of the circuit is calculated and listed in the spreadsheet.

The estimated losses are expected to be close to the actual losses. In real life the power dissipated in the components may be slightly different depending on parasitic elements and material properties of components used. The loss budget helps to verify the estimated efficiency. If the estimated efficiency based on the loss budget is different to the efficiency at $VAC_{MIN}$ used in the applications variables section, the efficiency specification should be changed and the design should be iterated. The loss budget provides insight into the power dissipated in the key elements and helps with the thermal design of the power supply.

## Designing with HiperPFS

### Feedback Circuit Design – Analysis and Calculations

The typical feedback network tied to the FEEDBACK pin is shown in the Figure 21.

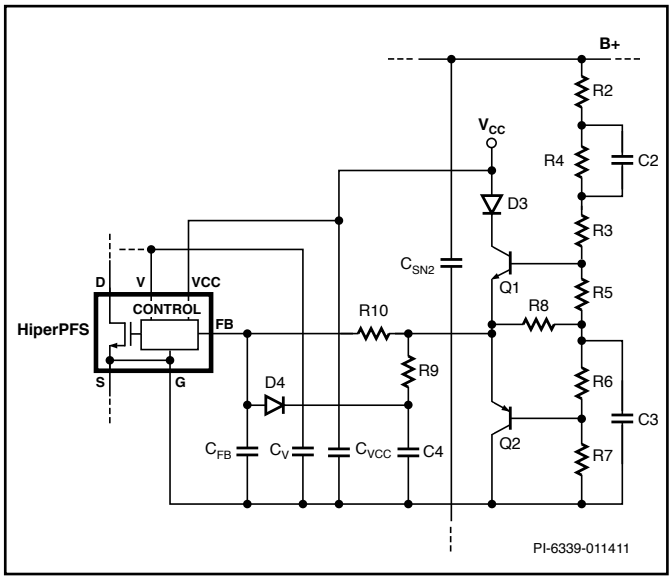



*Figure 21. Typical External Feedback Network (Including Transient Response Loop Speed-Up).*

Resistors R2 to R7 comprise of the main output voltage divider network. The sum of resistors R2, R3, R4 and R5 is the upper divider resistor and the lower feedback resistor is comprised of the sum of resistors R6 and R7. Capacitor C2 is a soft-finish capacitor that reduces output voltage overshoot at start-up. Resistor R10 and capacitor $C_{FB}$ form a low pass filter to filter any switching noise from coupling into the FEEDBACK pin. Resistor R9 and capacitor C4 form a loop compensation network which introduces a low frequency zero required to tailor the loop response to ensure low cross-over frequency and sufficient loop phase margin. Resistor R8 isolates the fast portion (resistor voltage divider network comprising of resistors R2 to R7) and the slow feedback loop compensator circuit (resistor R9 and capacitor C4). Transistors Q1 and Q2, biased with resistors R5 and R6 respectively, detect output voltage transient conditions and provide the FEEDBACK pin with “fast” information to increase the loop response of the system dynamically. Diode D4 is included to ensure a safe shutdown under the single point fault condition of capacitor C4 shorted. In this event the FEEDBACK pin would be forced below the $FB_{UV}$ threshold through diode D4 and subsequently turn the HiperPFS off.

Only a standard recovery diode should be used for D4. Use of ultrafast or fast recovery diode is not recommended due to the difference in behavior in the presence of high frequency noise that maybe coupled into the FEEDBACK pin.

**Steady-State Analysis**

In steady-state operation transistors Q1 and Q2 must be in the "off" state to prevent any distortion of the input current waveform. The FEEDBACK pin is the high input impedance inverting terminal of a transconductance amplifier; the internal non-inverting terminal is tied to a precision reference voltage. The steady-state current into the FEEDBACK pin is assumed to be zero in this analysis, thus the current through R10 and R8 is also zero. In steady-state the mid-point voltage of the voltage divider network is at internal reference voltage potential. The output voltage can be computed as a function of the resistor values in the divider network and the internal FEEDBACK pin reference voltage as:

$$B+ = \left(\frac{R_2 + R_3 + R_4 + R_5}{R_6 + R_7} + 1\right)V_{FB}$$

Using typical values for the resistor divider network; R2+R3= 3.1 MΩ, R4=732 kΩ, R5=2.2 kΩ, R6=2.2 kΩ, and R7=57.6 kΩ and the internal reference voltage: $V_{FB}$ = 6 V, we find that the output voltage (B+) is:

$$B+ = \left(\frac{3100 + 732 + 2.21}{2.21 + 57.6} + 1\right) \times 6 = 385.4\,V$$

The steady-state current through the divider network sourced from the output voltage is given as:

$$I_{B+} = \left(\frac{385.4\,V}{(3100 + 732 + 2.21 + 2.21 + 57.6)k\Omega}\right) = 99\,\mu A$$

The voltage across the bias resistors R5 and R6 is:

$$V_{R5/R6} = 99\,\mu A \times 2.21\,k\Omega \approx 219\,mV$$

At this bias level, transistors Q1 and Q2 are in the "off" state confirming the original assumption for steady-state operation. It is important to ensure that the voltage across R5 and R6 remain safely below the $V_{BE(ON)}$ thresholds of Q1 and Q2 in steady-state operation, which must also include any line frequency ripple which may be present across the B+ output capacitor.

Diode D4 is not required for normal operation and is only required to protect the circuit in case of failure of capacitor C4 resulting in a short-circuit across capacitor C4, or a short resulting from manufacturing defect. Diode D3 prevents delay in start-up when the PFC is remotely turned-on by turning the $V_{CC}$ supply on. If start-up delay after turn-on of $V_{CC}$ is not a concern, diode D3 is not required and collector of transistor Q1 can be connected directly to $V_{CC}$.

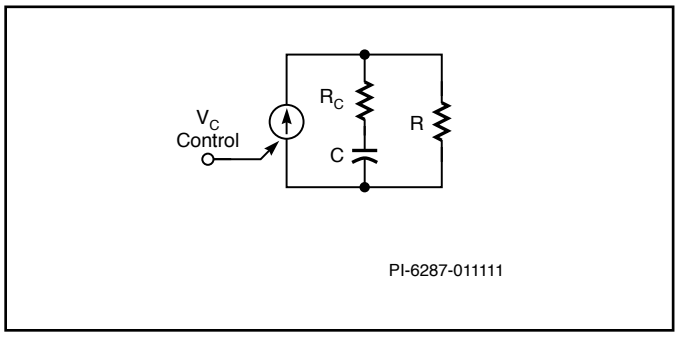



*Figure 22. Outer Voltage Loop – Small Signal Model.*

**Loop Compensation – Compensator Design**

The simplified low frequency small signal model of the outer loop is shown in Figure 22. In order to ensure that the input current has low harmonic distortion while simultaneously maintaining good output voltage regulation, the loop gain crossover frequency of the outer loop of a boost PFC is considerably lower than the line frequency. For frequencies significantly lower than the switching frequency, the model shown in Figure 22 provides accurate results. The resistor R represents the load resistance and the capacitance C represents the load capacitance. Resistance $R_C$ is the ESR of the output capacitor C. With a source resistance equal to the load resistance at all times for a current mode controlled power source, the dominant pole of the loop shown in Figure 23 is at 2/RC.

With a control to output response of a single pole for the outer loop with a very low pole frequency, which is usually less than one or two hertz, compensation of the converter is achieved by using an amplifier in the outer voltage loop that provides sufficient overall gain to improve regulation of output voltage while simultaneously increasing the loop gain cross over frequency to achieve ripple reduction.

The inner current loop generally has a high bandwidth to ensure a low distortion of the current waveform. Although the bandwidth of the inner current loop is higher than the frequency of the input, supply, it can be significantly lower than the switching frequency and yet achieve a low current waveform distortion.

The small signal control to output voltage loop gain varies with the square of the input voltage and hence is line voltage dependent. With a feed-forward of line voltage using the V pin signal, the loop gain can be made independent of line voltage and improves line regulation.

A simplified voltage feedback loop for the PFC using HiperPFS is shown in Figure 23.

The ESR of the output capacitor is not included in this analysis only because the zero contributed by the ESR of the output capacitor is at frequencies significantly beyond the loop gain crossover frequency.

The block diagram in Figure 24 shows the voltage feedback loop as a block diagram.

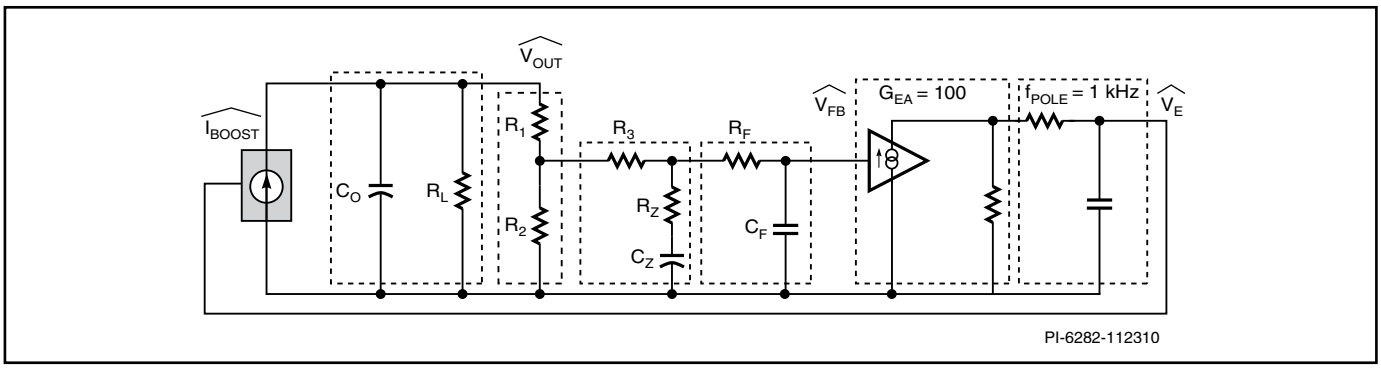



*Figure 23. Simplified Representation of Voltage Feedback Loop.*

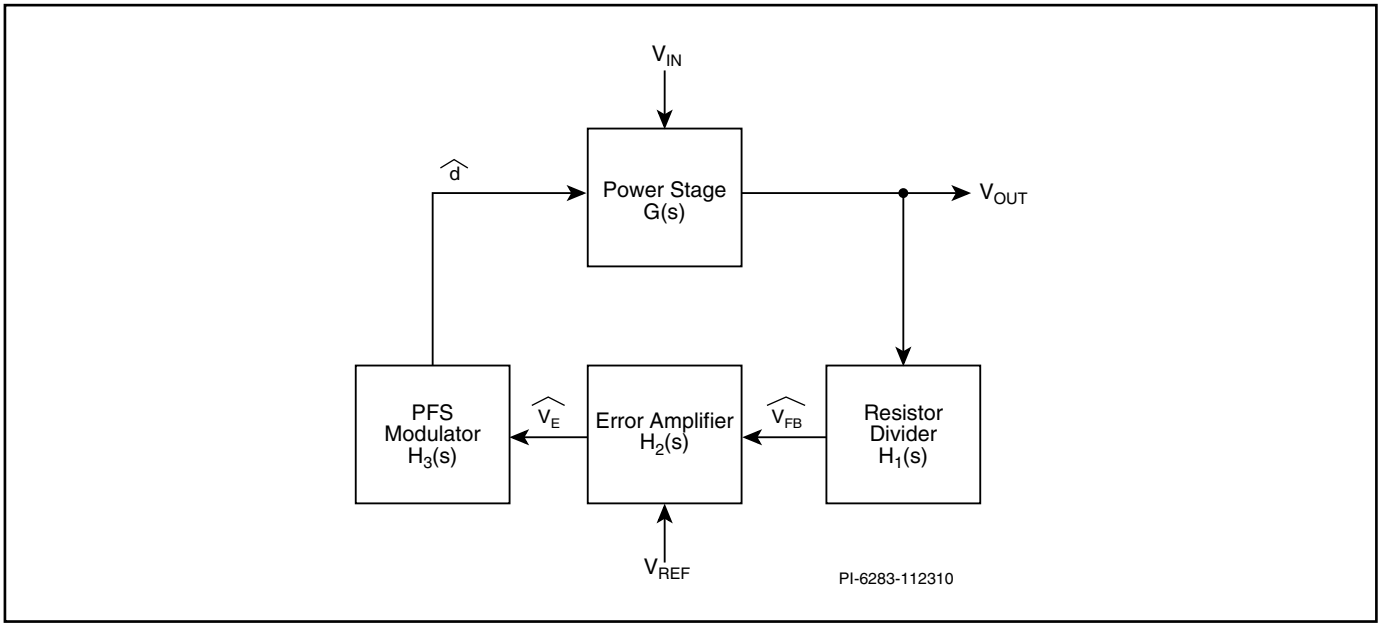



*Figure 24. Simplified Block Diagram of the Outer Voltage Loop.*

The total loop gain of the outer voltage loop is:

$$T(s) = H_1(s) \times H_2(s) \times H_3(s) \times G(s)$$

$$H_1(s) \times H_2(s) = \left(\frac{R_2}{R_1 + R_2}\right) \times \left(\frac{1}{1 + s/\omega_F}\right) \times \left(\frac{1 + s/\omega_Z}{1 + s/\omega_{P1}}\right) \times G_{EA} \times \left(\frac{1}{s/\omega_{1\,kHz} + 1}\right)$$

$$\omega_F = \frac{1}{R_F \times C_F}$$

$$\omega_Z = \frac{1}{R_Z \times C_Z}$$

$$\omega_{P1} = \frac{1}{(R_3 + R_Z) \times C_Z}$$

$$H_3(s) \times G(s) = \left(\frac{\hat{i}_{BOOST}}{\hat{v}_E}\right) \times \left(\frac{\hat{v}_O}{\hat{i}_{BOOST}}\right)$$

for a constant power load

$$\frac{\hat{v}_O}{\hat{i}_{BOOST}} = \frac{1}{s \times C_O}$$

for a resistive load

$$\frac{\hat{v}_O}{\hat{i}_{BOOST}} = \frac{R_L/2}{1 + s/\left(\frac{2}{C_O \times R_L}\right)}$$

The PFS Modulator gain is dependent on a number of parameters and it can be determined from Figure 25. The resulting system has a loop gain which is a single pole response. As stated above, the control to output gain of the power stage has a pole which is at a very low frequency and typically occurs below 2 Hz. The zero contributed by $R_Z$ and $C_Z$ restores the phase lag created by the pole associated with R3, $R_Z$ and $C_Z$. The zero is placed in the 4 Hz to 10 Hz region which is at a frequency above the pole. The high frequency pole contributed by $R_F$, $C_F$ ensures that the system does not respond to noise and has a gain roll off at higher frequencies. The resulting loop gain and phase plot are shown in Figure 26.

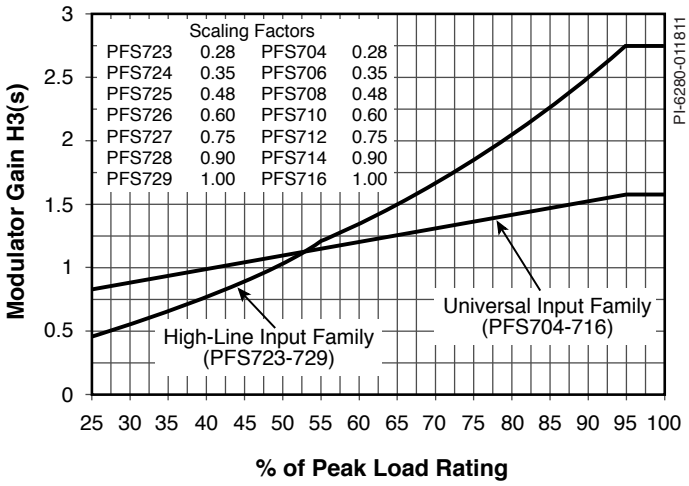



*Figure 25. Modulator Gain.*

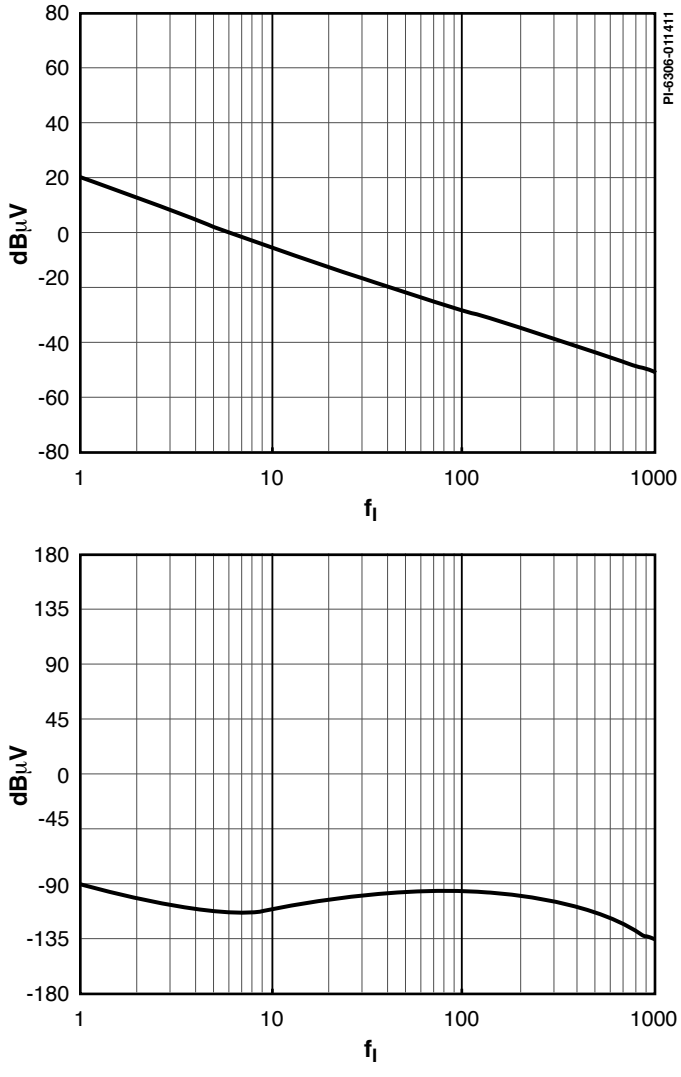



*Figure 26. Theoretical Loop Gain for the PFC.*

Value of capacitor $C_Z$ can be increased to reduce phase lag at low frequency and restore the gain slope to a near single pole response.

### Loop Gain Measurement – Test Set-Up and Load Step Response Measurement

Measurement of control loop response of a switching power converter such as the boost PFC designed using the HiperPFS, requires use of a specialized test set-up. This test set-up uses a network analyzer to inject a signal into the feedback loop and measure the amplitude of the signal appearing in the output of the power supply. The phase shift in the injected signal and the returning signal together with the difference in their amplitudes can be plotted as a Bode plot to evaluate the stability of the converter. The test set-up shown in Figure 27 can be used to obtain a bode plot

### Loop Gain Measurement – Procedure

- The PFC stage is supplied from a adjustable DC source for this test
- Connect the circuit as shown in the picture. Open the top end of the feedback divider network and insert a 100 Ω, 2 W resistor in series as shown. The signal injected in the loop for gain-phase measurement will be injected across this resistor.

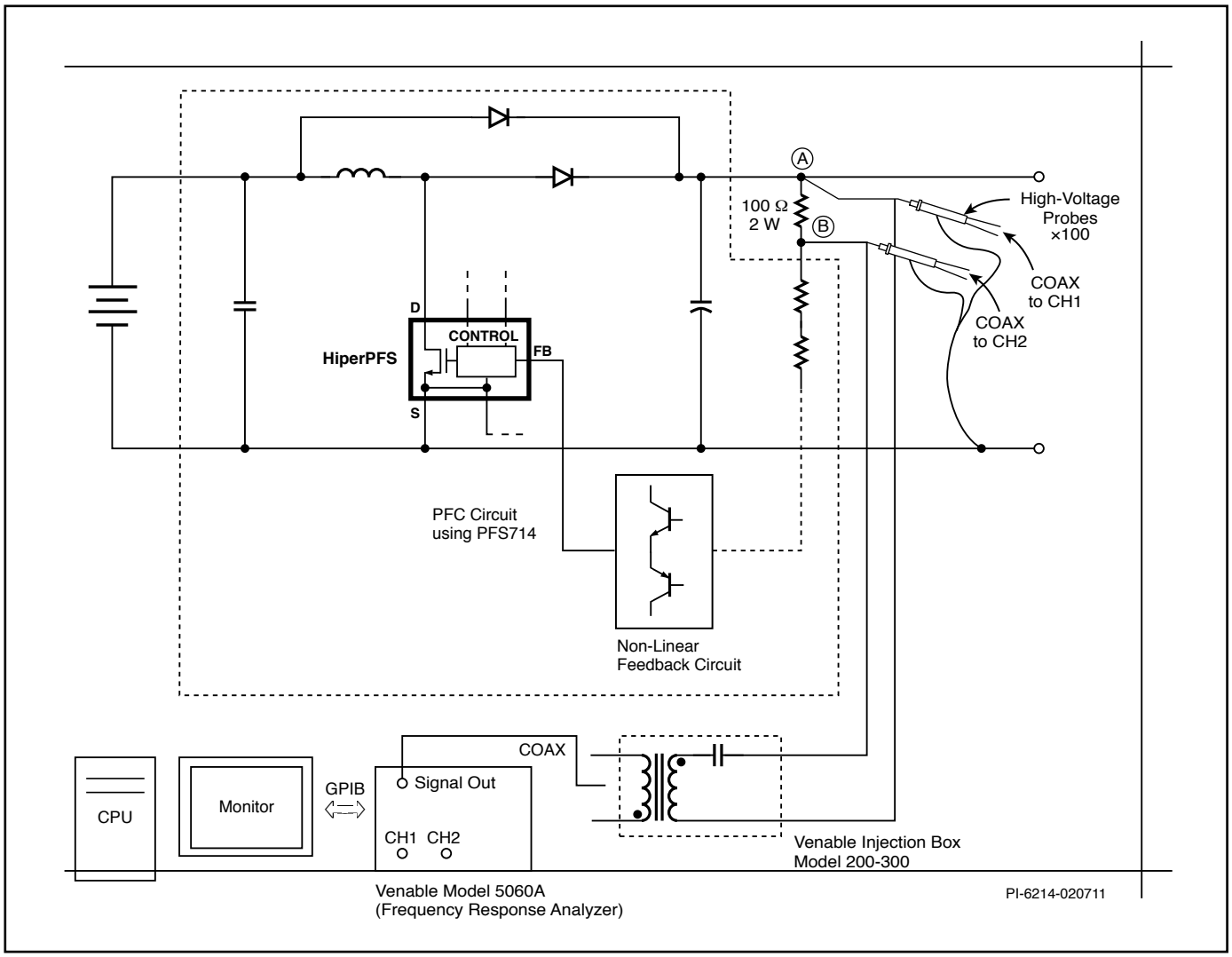



*Figure 27. Loop Gain Measurement Set-Up.*

- Nodes A and B (two ends of the injection resistor) are connected to Channel 1 and Channel 2 of the frequency response analyzer using high-voltage x100 attenuator probes. GND leads of both probes are connected to output return as shown.
- The signal to be injected is isolated using the Bode box injection transformer model – 200-000 from Venable Industries.

Test Procedure:

1. Adjust the input voltage to 150 VDC and confirm that the PFC output voltage is within regulation limits.
2. Adjust the output load to full rated load and reduce the input voltage to 100 VDC for universal input power supplies and 200 VDC for 230 V only power supplies.
3. Inject a signal from the frequency response analyzer.
4. The injected signal should be seen in the output voltage ripple of the PFC.
5. Plot the Gain Phase Plot by sweeping the injected signal frequency from 1 ~ 2 Hz to 90Hz.

### Loop Gain Measurement – Test Result

Figure 28 shows a typical gain phase plot obtained using the measurement method described above. The gain-phase plot shows a healthy phase margin in excess of 60º. It can be seen from the gain-phase plot that system has a single-pole role off and the gain goes up with increasing load level.

Taking measurements using the procedure provided is often difficult. Stability can be evaluated using load step response as shown in Figure 48a. It is necessary to connect the feedback divider network directly to the output capacitor. The loop shorting capacitor $C_{SN2}$ should always be connected directly between the cathode of the output diode D9 and the SOURCE pin of the HiperPFS device.

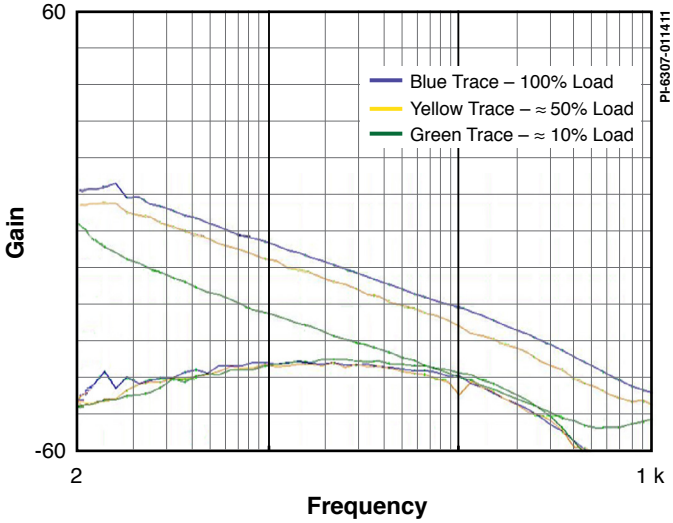



*Figure 28. Gain-Phase Plot Example for a 347 W PFC using HiperPFS PFS714EG.*

### $V_{CC}$ Decoupling Requirements

A low-ESR decoupling capacitor of at least 1 µF is recommended to be connected across the VCC and G pins of the HiperPFS. The VCC pin supplies power to not only the internal control circuit of the HiperPFS but also the MOSFET driver which draws pulsating current with each switching transition of the high-voltage MOSFET. Ceramic capacitors are most suitable for this application and use of surface mount capacitors is recommended to minimize stray inductance. It is recommended that the $V_{CC}$ be decoupled using an electrolytic capacitor of at least 10 µF in addition to the low ESR 1 µF capacitor placed physically close to the HiperPFS with short trace length between the capacitor leads and the HiperPFS pins. Note that when using ceramic capacitors verify the voltage coefficient of the dielectric for the selected capacitor. Some dielectrics can have a capacitance -80% of nominal when the rated voltage is applied.

### V Pin and FEEDBACK Pin Decoupling Capacitor Requirements

Switching noise can be easily coupled into the FEEDBACK pin and the V pin of the HiperPFS. To ensure reliable operation, it is required that a ceramic dielectric capacitor of 10 nF to 20 nF be connected from the FEEDBACK pin to the GROUND pin of the HiperPFS. The V pin needs to be decoupled using a 100 nF capacitor for the universal input parts and a 47 nF capacitor for the high-line only parts. The capacitor should be connected from the V pin to the G pin of the HiperPFS.

### Line Sense Network

The line sense resistor is connected from the bridge rectifier output to the V pin of the HiperPFS. The voltage drop across this resistor is in excess of 350 V peak when operating at the higher end of the input voltage range for universal Input or high-line only applications. It is therefore necessary to divide this resistor into two or more resistors to distribute the voltage stress between multiple resistors. The line sense resistors are required to be 4 MΩ for most universal input applications and 9 MΩ for most 230 V only (180 VAC - 264 VAC) applications. The resistors should be physically located close to the V pin of the HiperPFS to prevent noise injection due to the high dv/dt switching waveforms of the main power loop.

### Inrush Limiting

Without the use of any limiting mechanism, the input current of a boost PFC at start can be significantly large and even exceed 100 A. This current is due to the charging of the output capacitor. The current is only limited by the parasitic impedance of the components in the circuit such as the ESR of the output capacitor and the impedance of the common mode and differential mode filters. This current can often damage components in the circuit and result in fuse failure. Power supply specifications typically limit the magnitude of the inrush current and make it necessary to use a suitable limiting mechanism to keep this current below safe limits.

A simple and inexpensive method to limit inrush current is to use a NTC thermistor in series with the line. The resistance of the thermistor limits the inrush current at start and the rapid drop in its resistance thereafter ensures that the effect on system efficiency is minimal. There are two locations in which the thermistor can be used. The location TH1 shown in Figure 30 is the preferred location although in this location since the input current is high when the input voltage is low, it results in some efficiency degradation especially at lower input voltages. When used in location TH2, there is a reduced efficiency penalty, however there is an increase in the MOSFET drain source

voltage at switch-off and hence this is not particularly desirable. For most high performance PFC circuits when the thermistor is used in location TH1, it is common practice to use a relay to bypass the thermistor after start-up. This has the advantage that the highest efficiency is achieved and also it ensures that the thermistor is cold and hence will limit the inrush current if the input is switched off and switched on again.

A third arrangement uses a thermistor in series with the bypass diode D2 (Figure 30). While this provides some inrush current limiting, it is not as effective as putting the thermistor in location TH1, since some inrush current flows through the inductor and the PFC output diode. Placement of the thermistor in this path is therefore not recommended.

**PCB Design Guidelines**

The boost PFC circuit is a combination of a high-voltage switch mode converter, a control circuit consisting of the line sense network, the output voltage feedback divider network and compensation elements. The line sense network and the feedback network use large resistance values in order to minimize power dissipation in the feedback and line sense network.

Care should be taken to place the feedback circuit and the line sense network away from the high-voltage and high current nodes to minimize any interference. Any noise injected in the feedback network or the line sense network will typically manifest as degradation of power factor. Excessive noise injection can lead to waveform instability or dissymmetry.

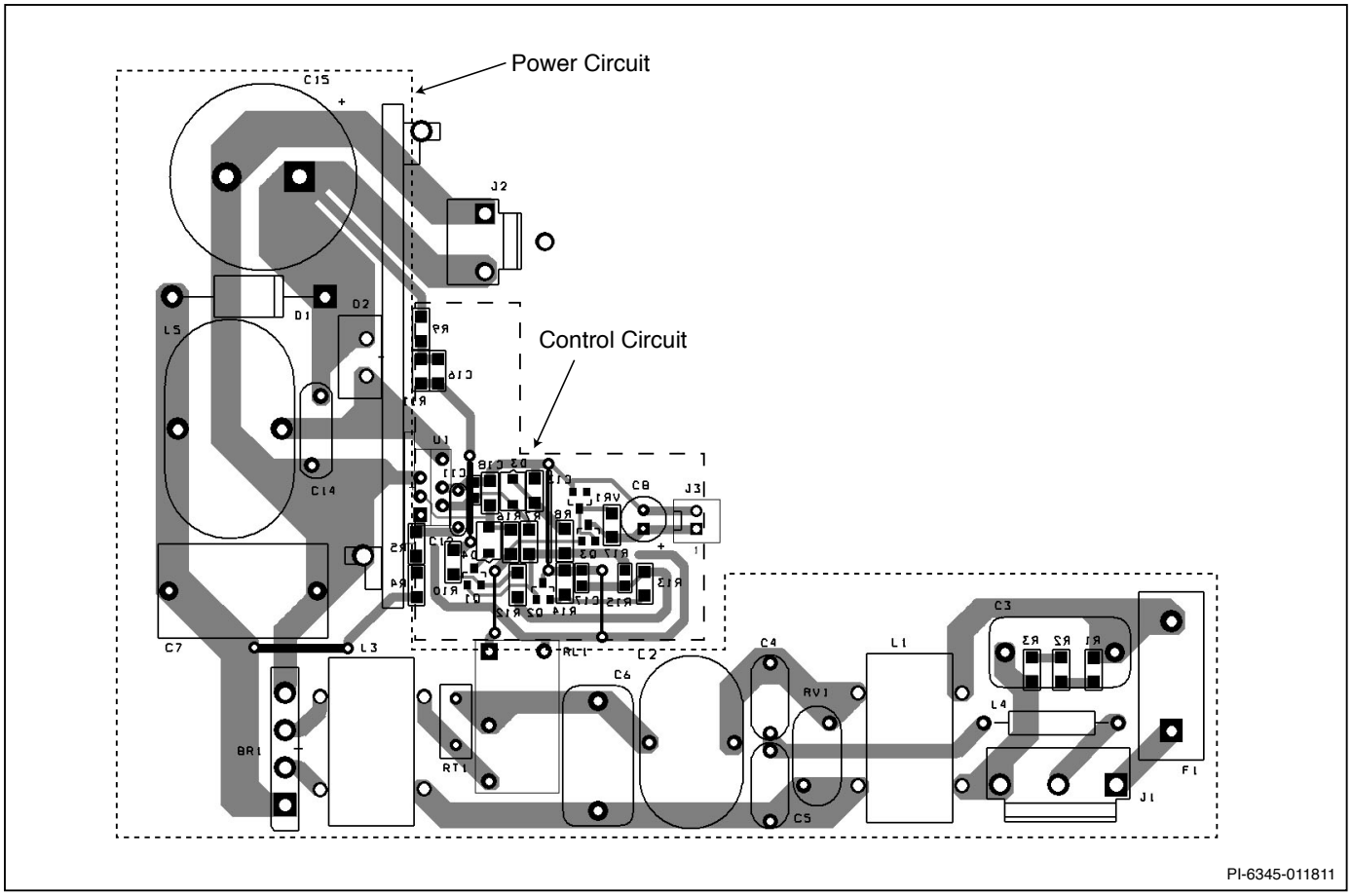



*Figure 29. Example Layout of Power and Control Circuit for a PFC Stage.*

The EMI filter components should be clustered together to improve filter effectiveness. The placement of the EMI filter components on the circuit board should be such that the input circuit is located away from the drain node, the output diode of the PFC and the PFC inductor.

A filter or decoupling capacitor should be placed at the output of the bridge rectifier. This capacitor together with the X capacitance in the EMI filter and the differential inductance of the source, works as a filter to reduce the switching frequency current ripple in the input current. This capacitor also helps to minimize the loop area of the switching frequency current loop thereby reducing EMI.

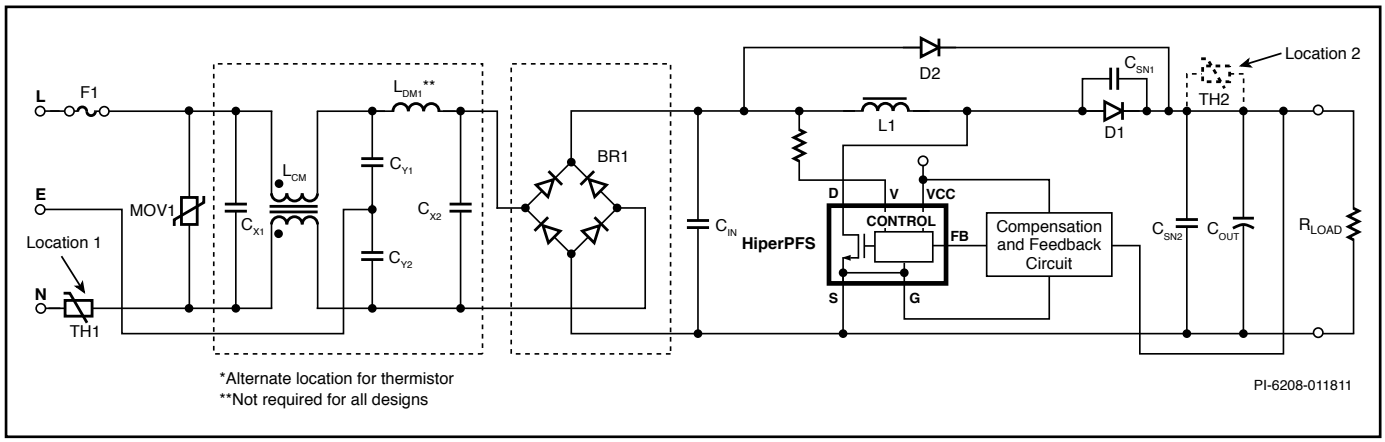
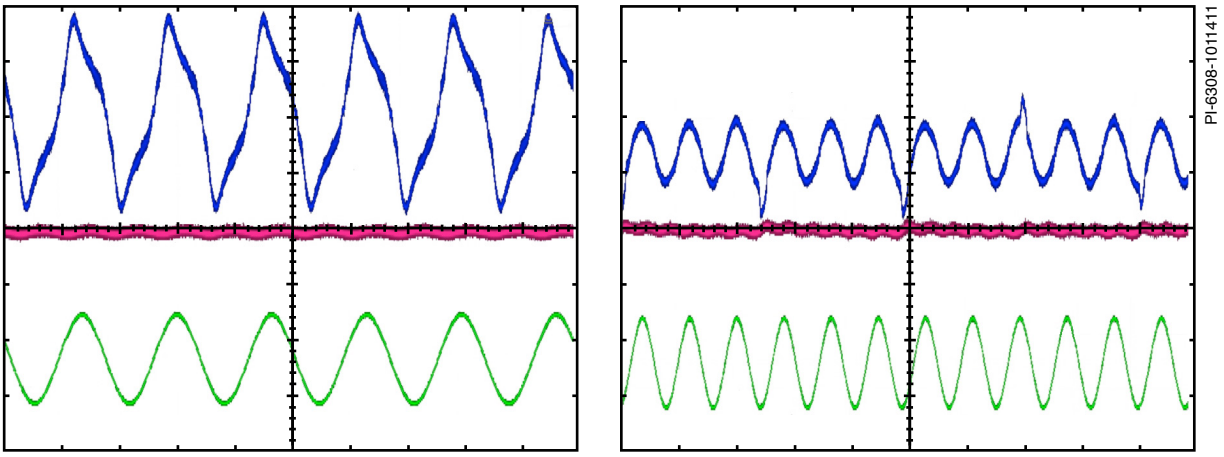



*Figure 30. PFC Schematic Showing Locations Where an Inrush Limiter may be Placed.*




Upper: Line Current, 2 A / div.
Middle: Output Voltage, 100 V / div.
Lower: Line Voltage, 200 V / div.

Upper: Line Current, 5 A / div.
Middle: Output Voltage, 100 V / div.
Lower: Line Voltage, 200 V / div.

*Figure 31. Examples of Waveform Distortion due to Violation of PCB Design Rules.*

The connection between the HiperPFS drain node, output diode anode terminal and the PFC inductor should be kept as small as possible.

A low loss ceramic dielectric capacitor should be connected between the cathode of the PFC output diode and the source terminal of the HiperPFS. This ensures that the loop area of the loop carrying high frequency currents at the transition of switch-off of the MOSFET and helps to reduce radiated EMI due to high frequency pulsating nature of the diode current.

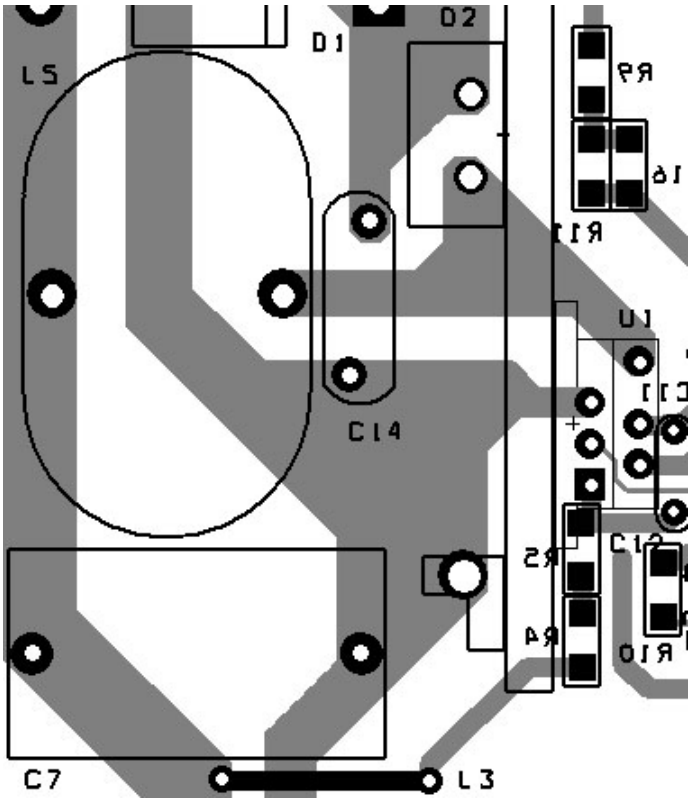



*Figure 32. Low Loop Area Routing of High-Frequency Loops.*

During placement of components on the board, it is best to place the V pin, FEEDBACK pin and VCC pin decoupling capacitors close to the HiperPFS before the other components are placed and routed.

To minimize effect of trace impedance affecting regulation, output feedback should be taken directly from the output capacitor positive terminal. The upper end of the line sense resistors should be connected to the high frequency filter capacitor connected at the output of the bridge rectifier.

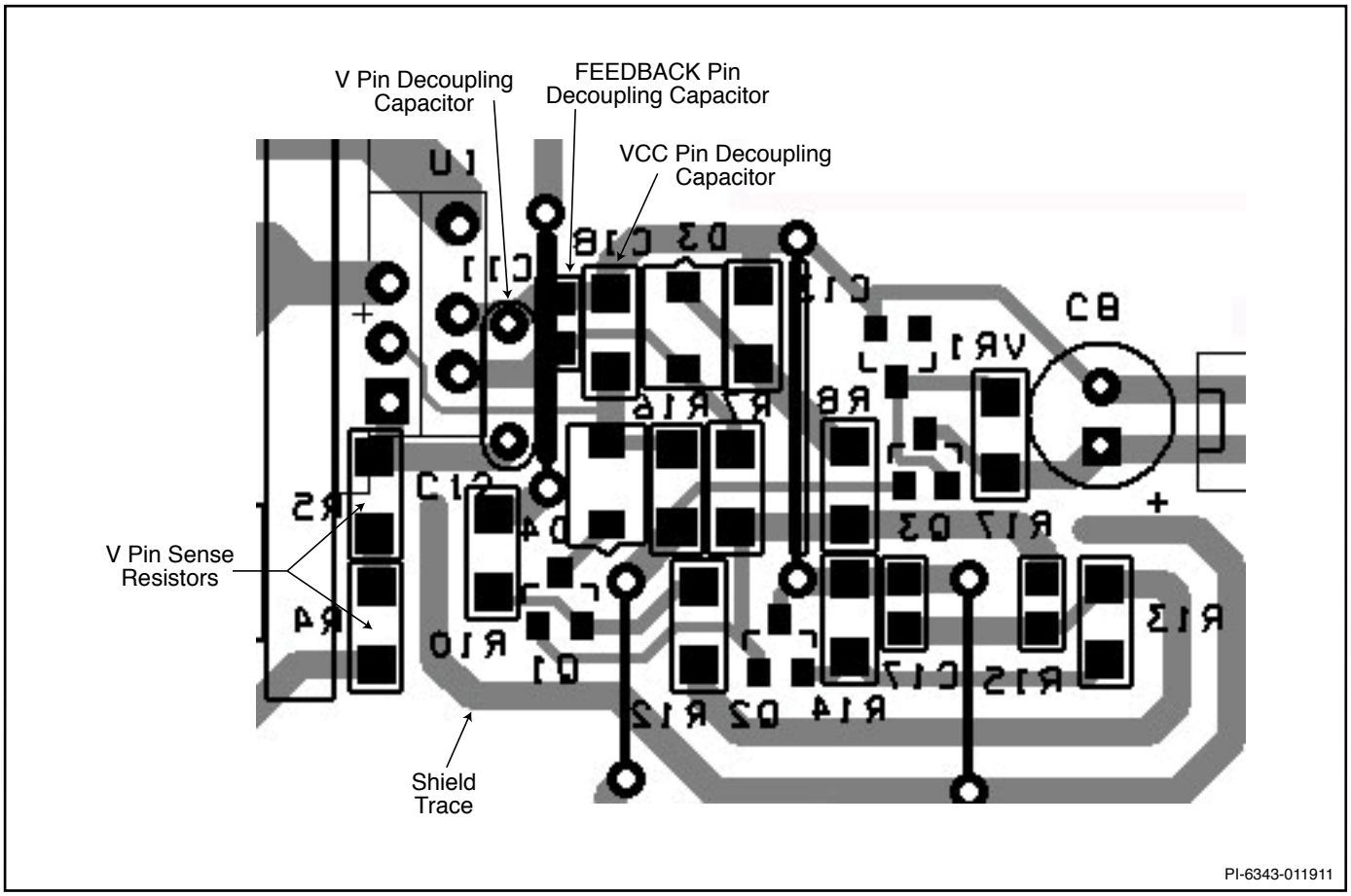



*Figure 33. Placement of Decoupling Capacitor and Control Circuit Components.*

## PCB Design Example

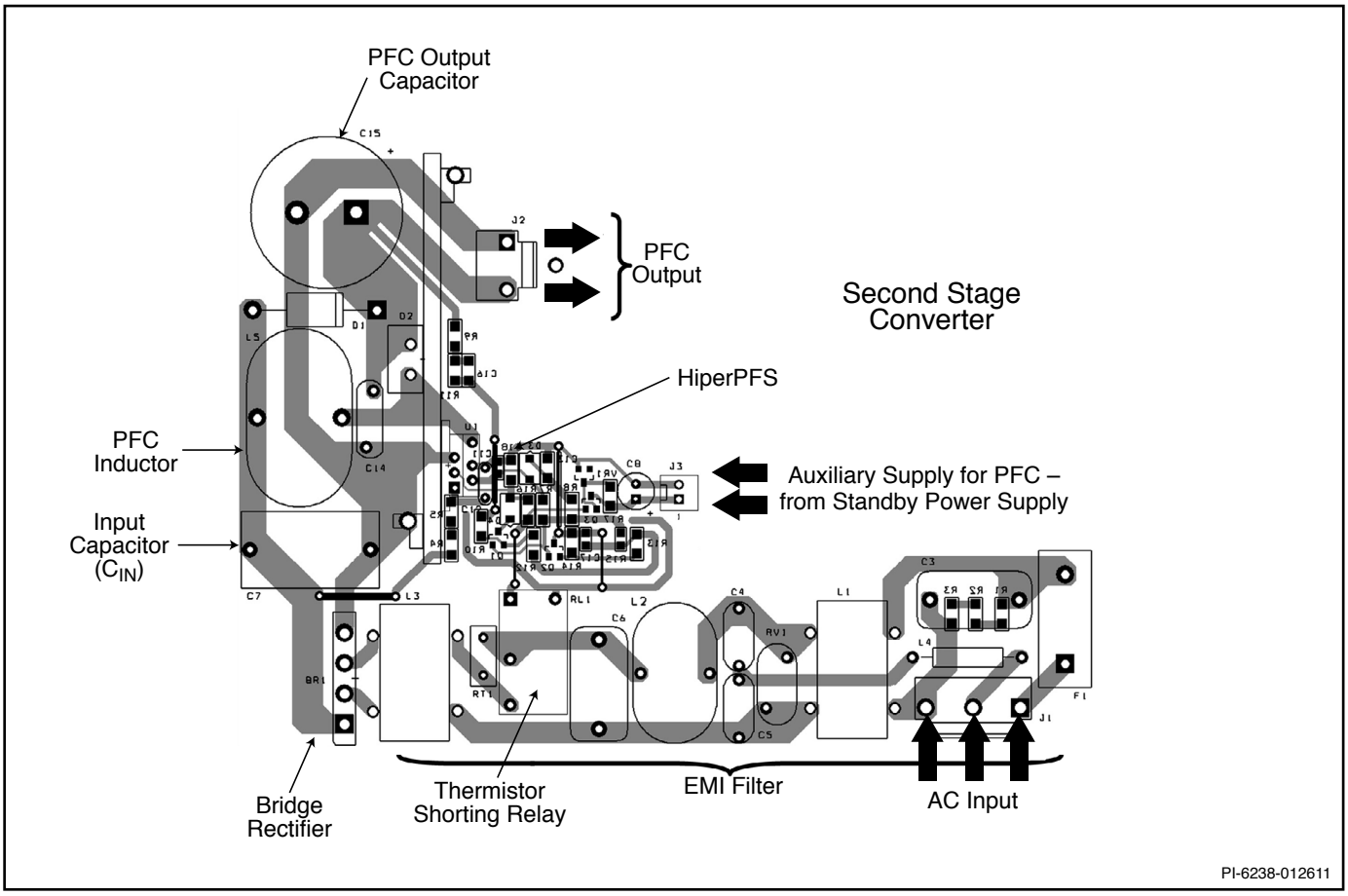
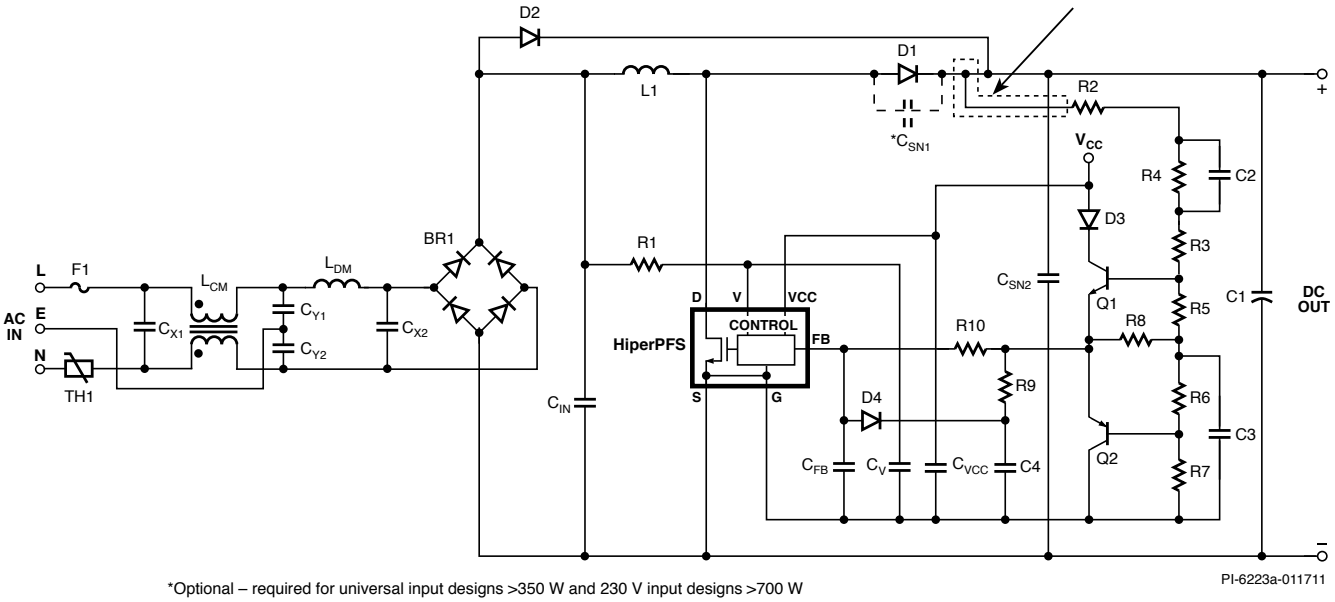



*Figure 34. PCB Layout Example for System Power Supply Consisting of a PFC and a Second Stage Converter.*

### Common Layout Problems to Avoid

A poor layout will often result in performance issues that may be time consuming to analyze and occur especially at the end of a development cycle when PCB design changes are difficult to make. Figures 35-38 should be useful in quickly identifying the root cause and correct the layout. Figures 35-38 schematically show common layout mistakes and the reason they should be avoided

✘ Poor Choice of Location for Termination of Feedback Divider Network

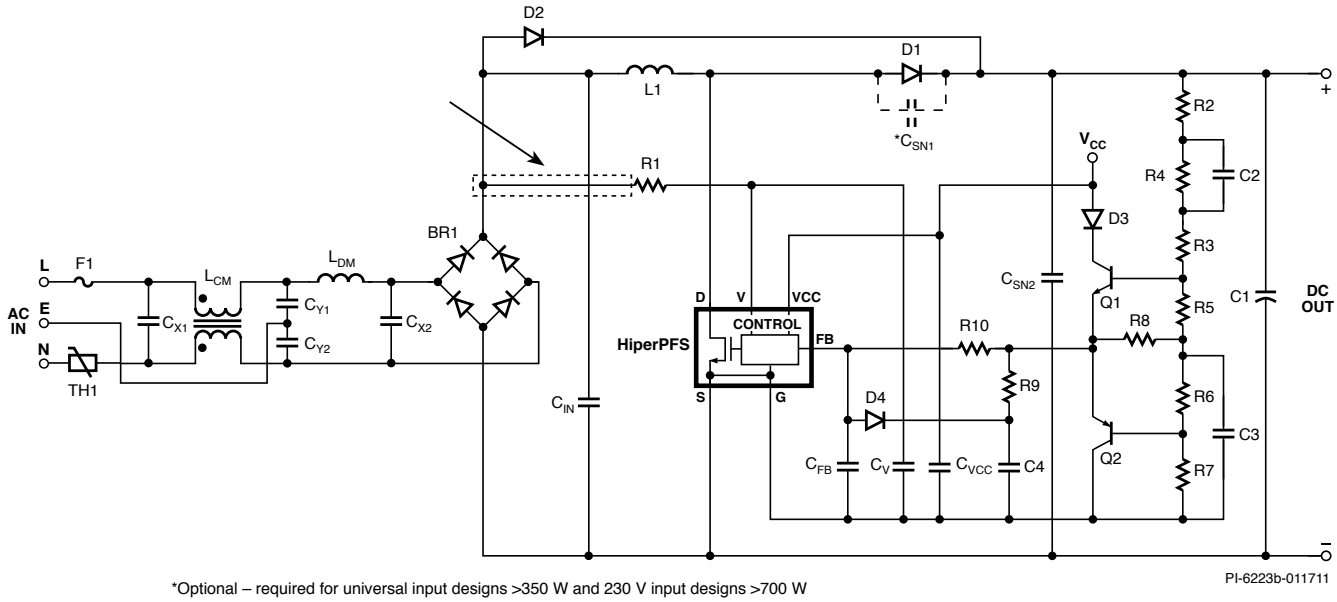



*Optional – required for universal input designs >350 W and 230 V input designs >700 W

Note: Feedback divider network should be connected as close to the output capacitor as possible. Connecting the feedback divider network close to the output ensures the best possible load regulation.

*Figure 35. Feedback Divider Network Location.*

✘ Poor Choice of Location for Termination of Line-Sense Resistor

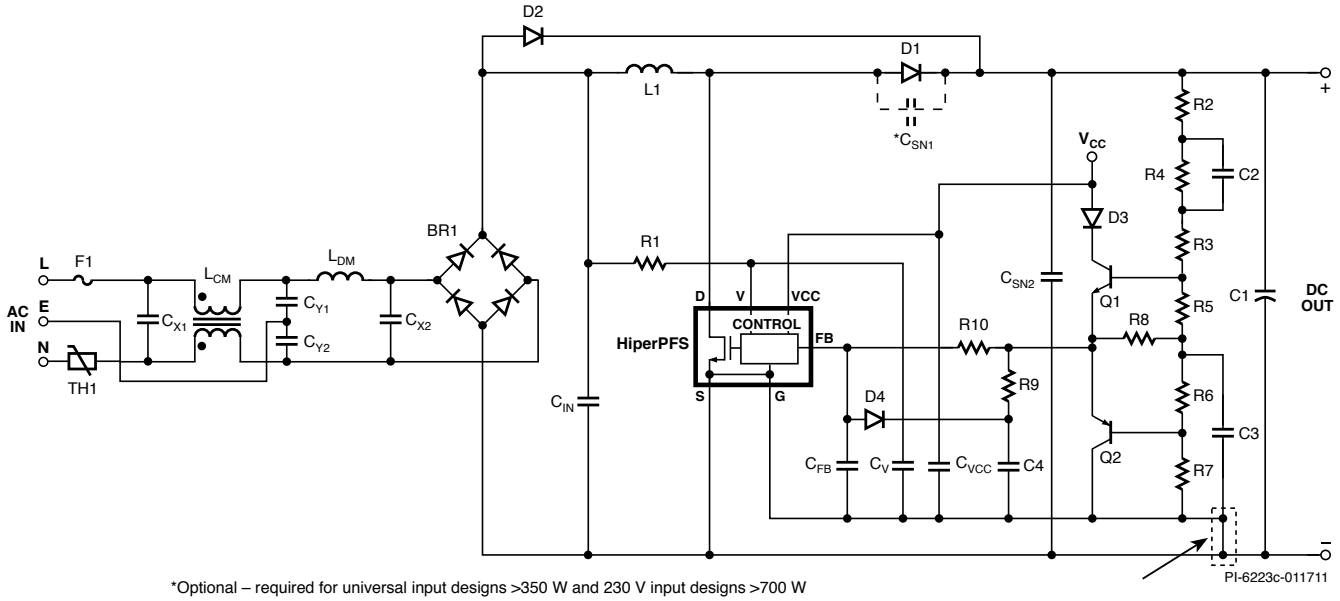



*Optional – required for universal input designs >350 W and 230 V input designs >700 W

Note: Line sense resistor network should only be connected directly to the filter capacitor after the bridge rectifier. If connected as shown in the picture above, it could result in noise injection into the V pin signal that can result in power limited operation or incorrect brown-out threshold.

*Figure 36. Location of Line Sense Network Resistor Termination.*

✘ Indirect Short Between “G” and “S” Pin on the Circuit Board

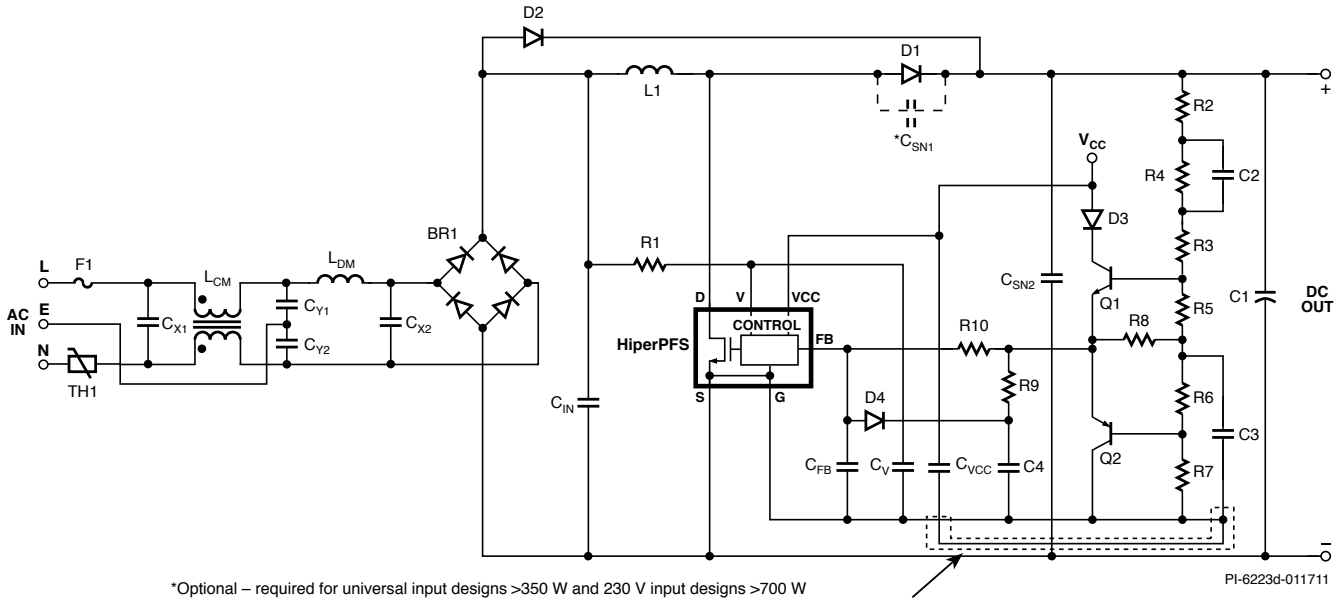



*Optional – required for universal input designs >350 W and 230 V input designs >700 W

Note: The lower resistor of the feedback network and the decoupling capacitors for the HiperPFS pins should only be returned to the G pin which is the internal controller ground. This pin is internally connected to the SOURCE pin. The G pin and the S pin should not be connected externally. If a connection is made as shown in the figure, it will typically result in erratic input current and poor load regulation.

*Figure 37. Signal Ground for Feedback Network.*

✘ Poor Grounding of $C_{VCC}$




*Optional – required for universal input designs >350 W and 230 V input designs >700 W

Note: The $V_{CC}$ decoupling capacitor should be terminated close to the G pin. If the trace connecting this capacitor to the G pin is shared by the feedback circuit, it will result in common impedance coupling thereby introducing switching noise on the feedback signal resulting in waveform distortion. Inappropriate decoupling can cause failure of the brown-out feature. See Figure 31 for example of waveform distortion due to this configuration.

*Figure 38. Grounding for $V_{CC}$ Decoupling Capacitor.*

Figure 39 shows the parts of the boost converter stage that have high frequency switching currents. Parts of these loops are shared between the two loops shown. The segments that are shared have a small AC component of current. The segments that are highlighted have a large AC component of current. These segments can be a source of significant amount of electromagnetic interference if their length is large. PCB design effort should be directed at keeping the length of these segments small and also keeping the loop area of the two loops shown in Figure 45 as small as practical.

The segments that carry pulsating currents are highlighted in Figure 39.

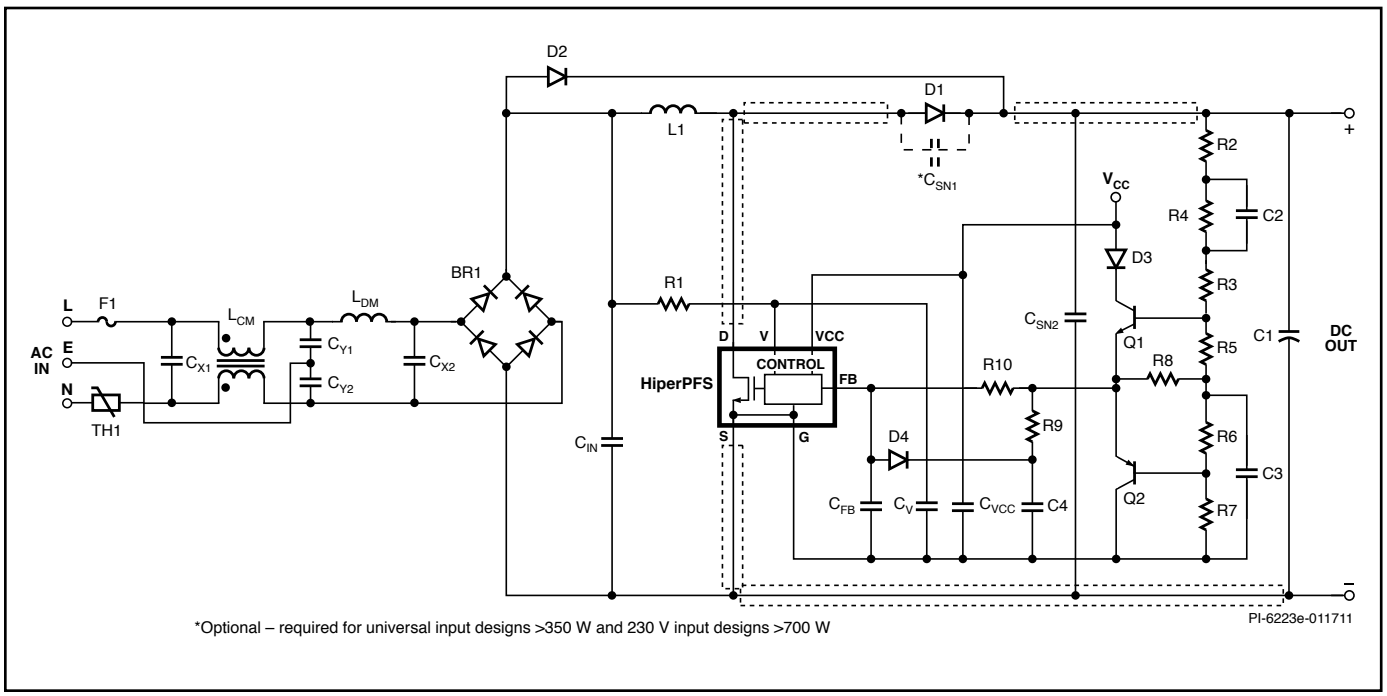



*Figure 39. Parts of PFC Circuit Carrying Pulsating Currents.*

### Thermal Design

The eSIP package enables design of compact and high density PFC design due to its low profile. A heat spreader is recommended for use with the HiperPFS parts to enhance thermal performance, especially in universal input designs over 150 W and 230 V only designs over 300 W. The rear surface of a HiperPFS eSIP part is the MOSFET Drain connection. This being a high-voltage switching node, it is essential to isolate the package from the heat sink. A low thermal resistance silicone rubber insulator such as the Bergquist – Kapton®-K10 insulator is recommended to be placed between the heat spreader and the heat sink.
A heat spreader is a rectangular piece of aluminum or copper.

While the physical size may depend on the actual size of heat sink and mounting arrangement, a larger size yields lower thermal resistance. The assembly shown in Figure 40 uses a Kapton K-10 insulator and a 0.76 mm thick aluminum heat spreader of 16 mm width and 21 mm height. This assembly provides a junction to heat sink combined thermal resistance of approximately 3.1 °C/W for the heat sink shown.

It is important to ensure a good quality surface finish for the aluminum heat spreader to achieve low thermal resistance and efficient heat transfer between the heat spreader and the HiperPFS.

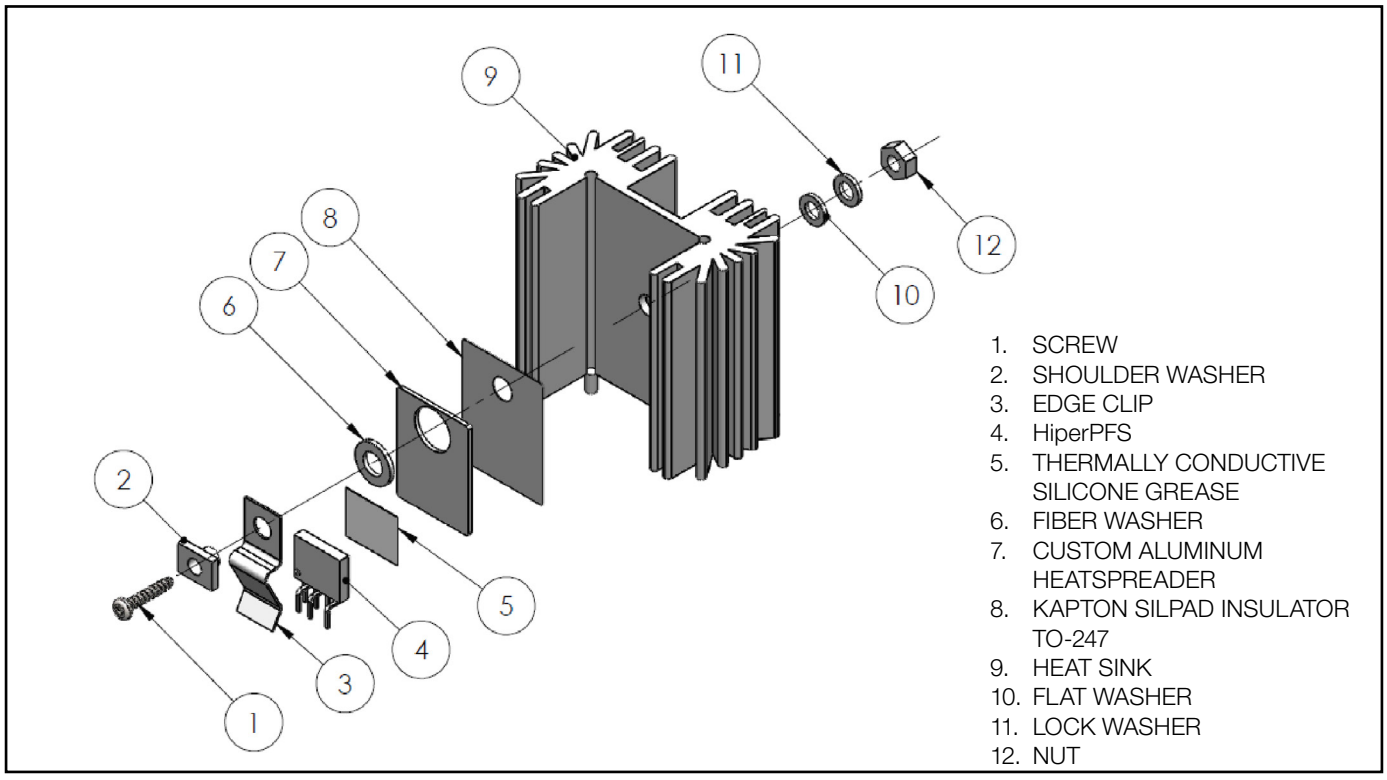



*Figure 40. Heat Sink Assembly Example for Designs >150 W (Universal Input) and >300 W (230 V Input).*

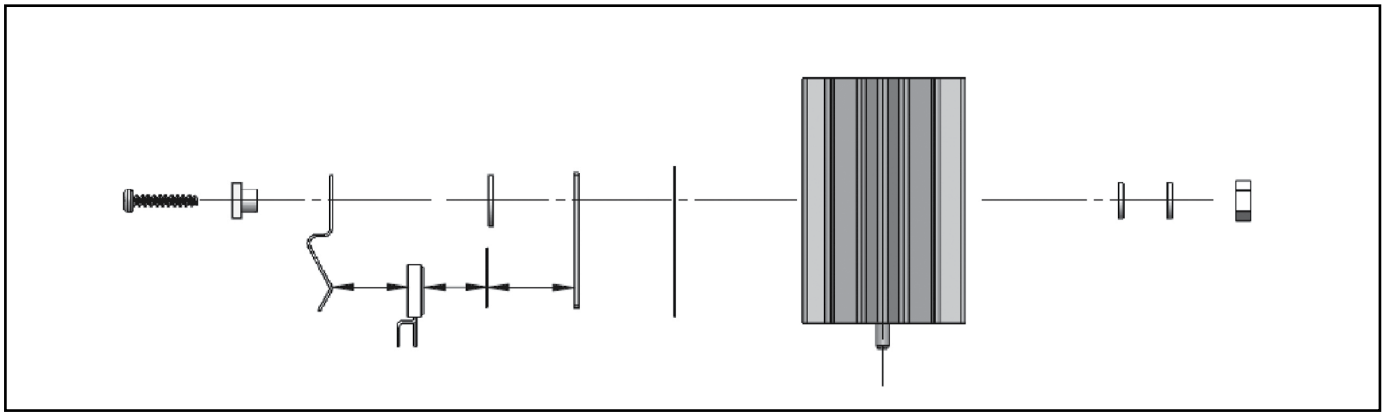


*Figure 41. Heat Sink Assembly – Side View.*

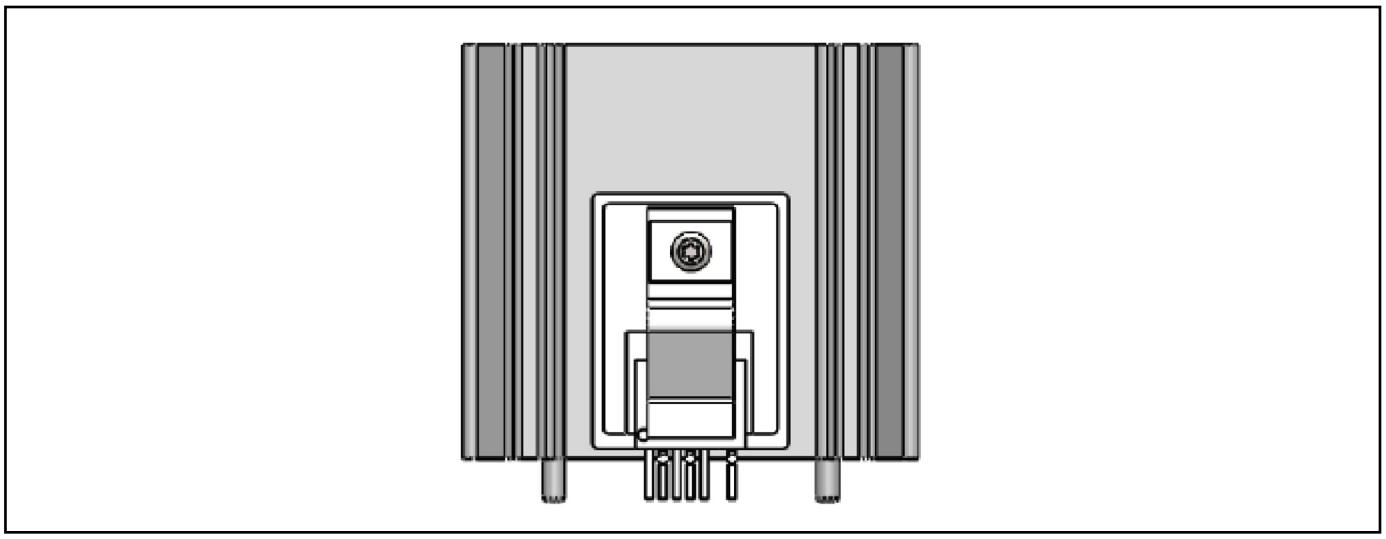


*Figure 42. Heat Sink Assembly – Front View.*

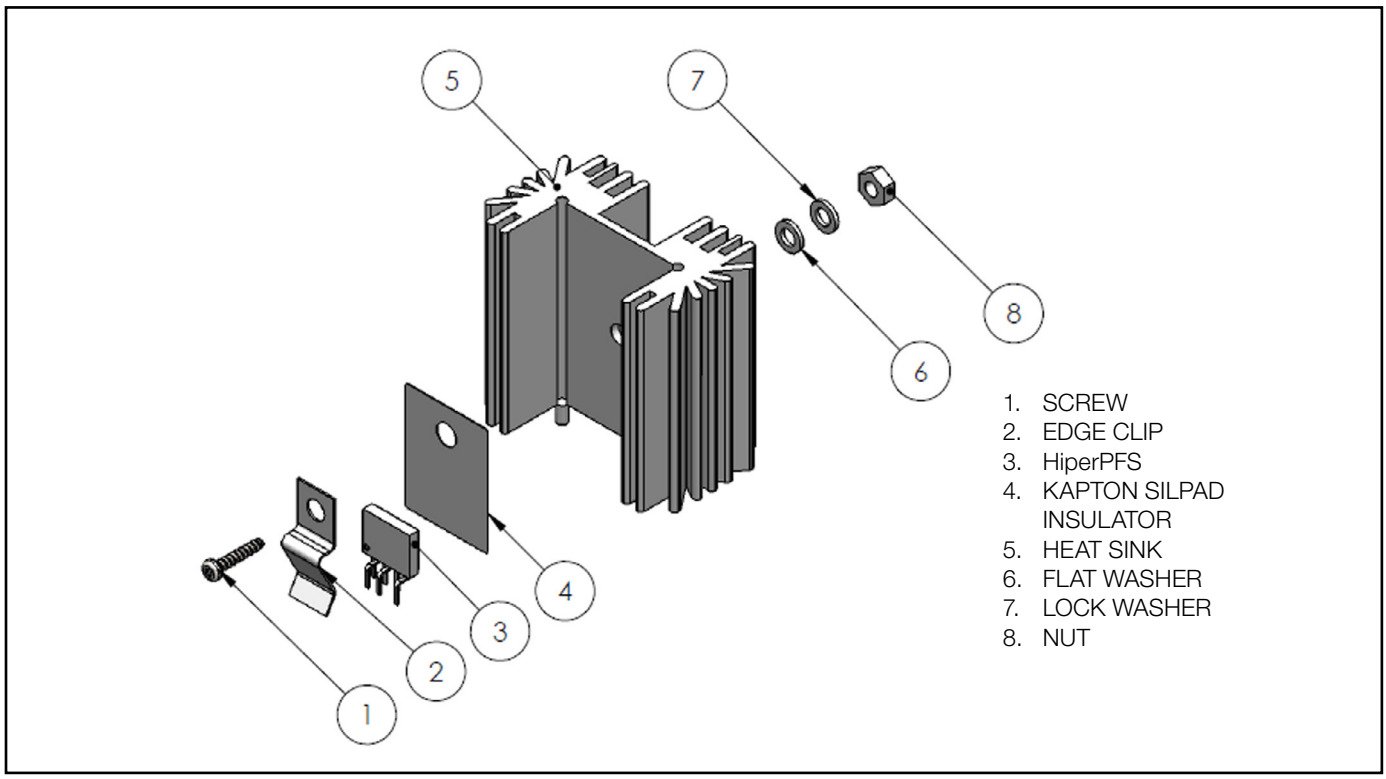



*Figure 43. Heat Sink Assembly Example – Low Power Designs (< 150 W (Universal Input) and < 300 W (230 V Input)).*

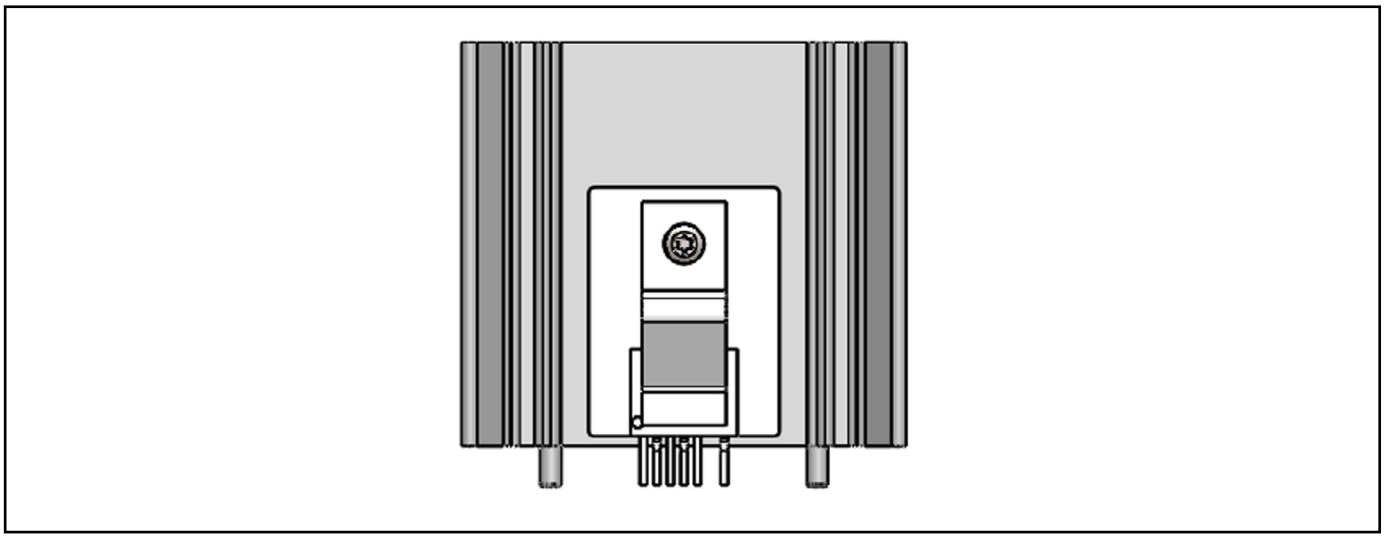


*Figure 44. Heat Sink Assembly – Low Power Designs.*

It is necessary to apply suitable thermally conductive silicone grease to the rear surface of the eSIP package to ensure low thermal impedance between the heat spreader and the eSIP.

Thermal impedance of the assembly also depends on the clamping force with which the eSIP assembly is pressed together. Metallic clips such as the one shown in Figure 43 provide a mounting force of 25 N. Beyond 20 N to 30 N there is no significant change in the total thermal resistance of the assembly.

The heat sink should be connected to the source terminal of the HiperPFS on the circuit board. This ensures that the heat sink is a quiet node electrically and hence not a source of EMI.

When using a heat spreader that is electrically connected to the high-voltage drain node and a heat sink which is electrically connected to the source terminal, a voltage as high as the output voltage exists between the heat spreader and the heat sink. As such care needs to be taken to ensure that there is sufficient creepage and clearance between surfaces that have high-voltage between them. One way to achieve the required clearance is to use a shoulder washer as shown in Figure 40.

In order to evaluate the thermal performance of the assembly, it is necessary to make temperature measurements. Temperature can often be measured by using infrared thermometers. Infrared thermometers being non-contact type, greatly simplify thermal measurements however care should be taken when using this method. The emissivity of the surface being measured is required to be programmed into these instruments without which there is an error in the measured temperature.

Temperature can also be measured by using thermocouples glued to the part being measured using a thermally conductive epoxy. There can be some measurement inaccuracy when using this method due to the physical size of the thermocouple junction. Often a reading inaccuracy as high as 10 °C is noticed when temperature of flat surfaces is measured using this method. Thermocouples also suffer from measurement inaccuracy due to noise pickup from adjacent high-voltage switching circuitry.

A third method that is often inexpensive is to use RTD (Resistance Temperature Detector). The RTD devices are available in packages that have a flat surface that can be attached to the surface of the device being measured using a highly conductive epoxy such as Arctic Silver®. The resistance of the RTD changes as a function of temperature and a simple ohm-meter or multi-meter with a resistance range can be used for this measurement. The much larger currents used to measure the resistance makes this method less noise sensitive.

**Design Considerations for Controlling EMI**

The boost converter designed using the HiperPFS is a switching converter. Without the use of an EMI filter at input, this converter will not meet conducted and radiated EMI limits imposed by regulatory agencies. A single stage common mode filter with X capacitors connected across the line will be generally adequate for meeting conducted EMI limits for most designs. The differential inductance of the common mode filter together with the X capacitors forms a low pass filter that attenuates switching frequency components in the input current. If this attenuation is insufficient, in some design a small differential inductance will often be necessary.

The Drain node of the HiperPFS and the PFC inductor should be routed away from the input EMI filter. The effectiveness of the EMI filter is compromised if the switching noise is coupled into the input wires directly thereby bypassing the EMI filter.

Power Integrations application note AN-15 TOPSwitch Power Supply Design Techniques for EMI and Safety and application note AN-53 Active Power Factor Correction - Basics, offer detailed explanation of causes of conducted and radiated EMI and guidelines on selection of components for EMI filter. Addition of X capacitors in the EMI filter will attenuate the switching frequency components and will reduced low frequency

conducted EMI. Excess X capacitance will degrade PF at light load levels. Power supply specification such as the 80 PLUS Bronze require that at 230 VAC and 50% load, the input power factor be better than 0.9. This limits the amount of X capacitance that can be used in the EMI filter.

A HiperPFS part mounted on a floating heat sink will often cause unstable PFC operation and also cause radiated and conducted EMI failures. The heat sink should be connected to the source terminal of the HiperPFS and as close to the source terminal as possible.

The windings of the PFC inductor can be a source of V-field and H-field interference. The PFC inductor should be located away from the EMI filter components.

It is most economical to minimize EMI at source. Filtering conducted and radiated EMI often requires use of expensive components such as X capacitors and inductors. EMI can be reduced by ensuring shortest possible loop areas of the high frequency loops or parts of circuit that carry voltages or currents with sharp rise and fall times.

There are two such loops in the boost PFC designed using the HiperPFS as shown in Figure 45. The first loop is completed between input capacitor $C_{IN}$, Inductor L1 and MOSFET Q1. The second loop is completed between input capacitor $C_{IN}$, inductor L1, output diode D1 and output capacitor C1. The loop area of these loops should be minimized. The most significant sources of EMI are the portions of these loops that experience pulsating currents. The Drain node of the MOSFET has a high-voltage switching waveform with respect to the source terminal which is also the circuit common. This makes the copper trace on the circuit board connected to the drain node a source of V-field. The trace length of the traces connecting components to this node should be kept short.

A third loop exists as shown in Figure 45 when the MOSFET turns on, the reverse recovery current of output diode D1 flows through the MOSFET. This current is a short duration pulse that can result in excess EMI if the loop area of this loop is not kept very small

One way to reduce the loop area of the second loop is to place a low ESR capacitor from the PFC output diode cathode

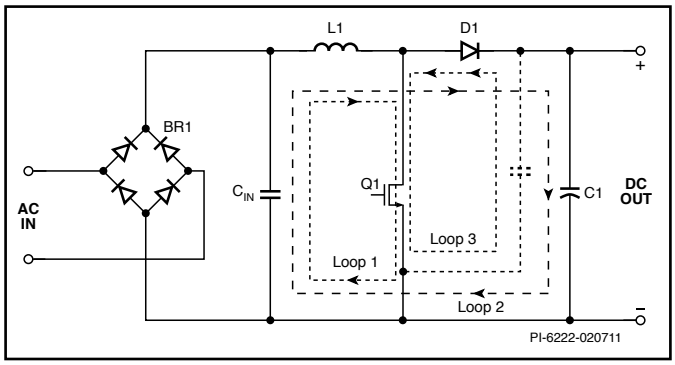



*Figure 45. Critical Loops of Current Resulting in Radiated and Conducted EMI.*

terminal directly to the MOSFET source terminal. Use of these capacitors is advised. Generally a 10 nF 1 kV capacitor will suffice. Use of multilayer surface mount capacitors can drastically reduce the parasitic lead inductance however these capacitors have been found to be very fragile. They often develop cracks easily during PCB assembly or handling or even due to unequal expansion and contraction of the board due to thermal cycling. Capacitors that are not coated by the manufacturer should be avoided as these may suffer from surface arc-over when a high-voltage is first applied that initiates a degradation process which finally leads to a catastrophic failure. Use of high-voltage surface mount capacitors vs. leaded type should be carefully considered for application as a loop shortening capacitor in the output of a boost PFC designed using HiperPFS.

Use of a low ESR and high ripple current capacitor is recommended for PFC output filter. Use of a low ESR capacitor ensures low switching ripple in the output of the PFC thereby reducing EMI coupled from the output stage of the PFC.

Figure 46 shows a typical EMI filter example. Generally a single common mode inductor will suffice for most applications. Inductor $L_{DM}$ and capacitor $C_{X3}$ form a differential low pass filter. Splitting the inductor $L_{DM}$ and inserting one of the inductors in series with the inrush limiter shown has the added benefit of reducing the common mode EMI further. The common mode filter inductance will typically be over 8 mH and values as high as 15 mH to 22 mH are not uncommon.

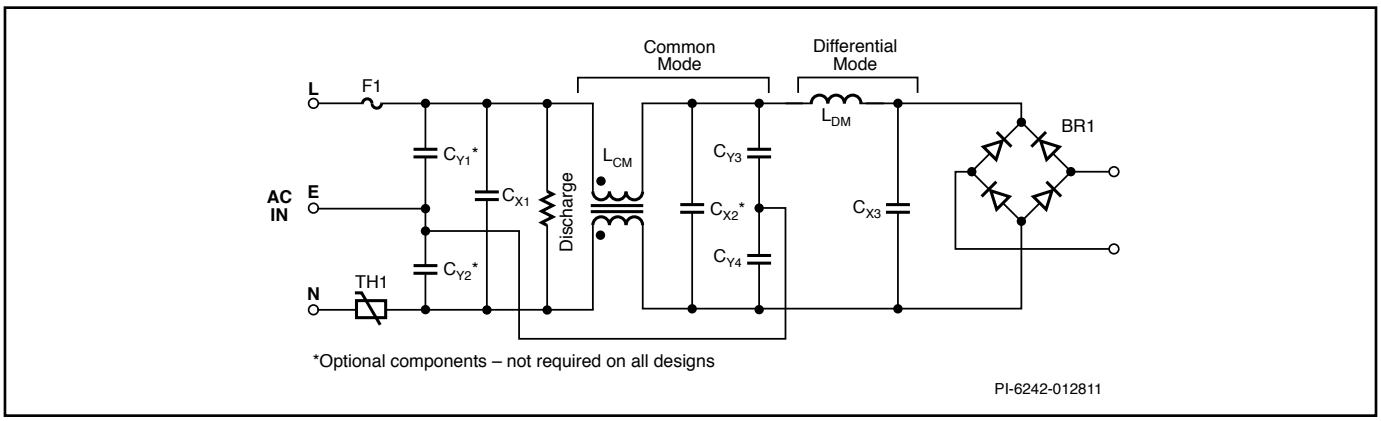



*Figure 46. Typical Common Mode and Differential Mode Filter.*

Although use of a high X capacitance helps in reducing the differential noise, excess X capacitance degrades the input power factor at light load and hence is counterproductive.

HiperPFS has variable frequency architecture. Frequency of operation can vary between devices which can result in slight variation between EMI signatures of multiple units. When optimizing EMI performance of a prototype designed using the HiperPFS, it is recommended that during development the conducted EMI measurement be made from 140 kHz to 30 MHz. If a high level of conducted noise is seen in the 140 kHz to the 150 kHz region, the EMI filter should be adjusted to offer sufficient attenuation for this noise as in some units the operating frequency may be higher shifting this noise signature to the 150 kHz - 160 kHz region where conducted EMI compliance is required.

When designing the EMI filter, care should to be taken to ensure that the EMI filter has a damped response and does not result in under damped ringing superimposed on the current waveform. The effect of this can be seen both in EMI measurements and also unexpected dips in measured efficiency and PF, typically at ~50% load.

**Design for Safety Compliance**

Power supplies are required to have capability of withstanding surge voltages which typically are a result of events such as lightning strikes. It is expected that such events do not lead to failure of any components or loss of functionality. Standards such as IEC61000-4-5 defines surge voltage and current waveforms as well as source impedance, which emulate typical worst case transients for testing of protection mechanisms for line connected power circuits and data line connected equipment.

Components of the EMI filter and the capacitors used in the power supply input stage as well as the PFC output, help in limiting the voltage and current stress that the components of the power supply are subjected to during these events.

MOVs will often be required to be added at the input of the power supply. These MOVs are placed after the input fuse and help in clamping the voltage at the input of the power supply when a surge event occurs.

The following checklist can be used to ensure that the design is compliant to the applicable requirements:

- Define the target market for PFC converter.
- Determine the equipment class to determine Common-Mode (CM) and Differential-Mode (DM) surge levels.
- Design boost converter front-end: ensure that EMI filter has at least one CM inductor stage to provide adequate leakage inductance for spike suppression.
- If DM surge >1000 V, then you will likely need to include an MOV across the AC line at the front-end of the EMI filter
- Select a MOV for North America 115 VAC or universal input with adequate stand-off voltage during normal operation as well as adequate rated surge current and energy capacity.
- An example of selecting an MOV: Assume that you have a North America application within a Class 3 equipment installation for which you need to select a MOV for differential-mode protection, connected across the AC line. The DM Spike Energy will be less than 6.9 J. A device rated for 150 VAC continuous operation would provide adequate stand-off voltage for 115 VAC nominal applications. Littelfuse part number V150LA5 provides 25 J and 2500 A surge capability with adequate margin to minimize degraded performance due to accumulated strikes over the life of the MOV. For a universal input design, the V320LA10 provides 48 J and 2500 A surge capability.
- Conduct both Common-Mode and Differential-Mode surge tests on the converter and observe voltages across key components and currents where necessary to validate SOA operation of components. Verify all voltage and current extremes are within the rated specification of each X and Y capacitor. If not, specify a component with a higher rating.
- Verify surge transient current rating of the diode bridge used.
- Verify rise time of voltage across the film capacitor connected after the bridge rectifier and ensure that it is within specified maximum dv/dt for the component selected. If not, specify a larger capacitor, a capacitor with higher dv/dt rating, or increase inductance in series with AC line in order to reduce inrush surge currents.
- Verify MOSFET switch BV rating is greater than surge voltage on switching node. If not, you may need to increase bulk capacitor size for greater current sink, or clamp drain node with TVS diode.
- Ensure that bulk capacitor surge voltage rating is not exceeded during testing. If surge voltage rating is exceeded, you may need to increase capacitance.
- Ensure that the bulk capacitor surge voltage does not exceed BV ratings of the second stage DC-DC converter.
- Select an AC line fuse which has an $I^2t$ rating that will accommodate power-on inrush current at maximum line voltage and which is rated for continuous AC line current and will not interrupt due to surge $I^2t$. Do not oversize the fuse more than necessary to withstand transient currents so as to ensure that the fuse will interrupt line current in the event of a line-to-line MOV failure.
- Thermistor selection/location: If large differential mode surge levels are required, it is recommended that the thermistor not be located in series with the output bulk capacitor, as this location causes the drain node to rise up to hundreds of volts above the bulk capacitor (refer Figure 30). A thermistor located in series with the AC line will increase design robustness during line surges.

When making measurements on a power supply during a line surge or safety test, care should be taken to ensure that the test equipment is galvanically isolated. If alternate paths for the surge energy are created as a result of connection of test probes, the test result will be incorrect. Care must be taken to use voltage probes that are rated for measurement of high-voltages in excess of the voltages likely to be encountered during the test.

**Do's and Don'ts**

**Location of $V_{CC}$ Decoupling Capacitor**

Ensure that the $V_{CC}$ decoupling capacitor is located close to the IC. If the $V_{CC}$ decoupling capacitor is located further away from

the IC and the trace is tapped at additional points for connection to other circuit sections, it will result in common impedance coupling and result in unexpected waveform distortion.

### Grounding of Feedback Circuit Components

Feedback pin decoupling capacitor and V pin decoupling capacitors should be placed next to the HiperPFS with minimum trace length for the interconnecting traces. This maximizes the effectiveness of these capacitors in filtering any noise coupled into the FEEDBACK pin or the V pin.

### Effects of Floating Heat Sink

The heat sink on which the HiperPFS is assembled, should never be floated. The heat sink should always be connected electrically to the source terminal of the PFS. The drain node is a high-voltage node. Since this node is a switching node, a small displacement current due to the capacitance between the heat sink and the PFS flows through the capacitance between the heat sink and the PFS. A floating heat sink thus becomes a V-field antenna, coupling noise into the sensitive FEEDBACK pin and the V pin which can make operation unstable.

This recommendation should be followed even if any additional power devices are assembled on the same heat sink.

This typically manifests as poor PF or waveform dissymmetry or occasional glitch in the waveform.

## Measurement Techniques

### Drain Source – Voltage Measurement

When measuring Drain-Source voltage of the MOSFET, a high-voltage probe should be used. When the probe tip is removed, a silver ring in the vicinity of the probe tip can be seen. This ring is at ground potential and the ultimate ground connection is at this point. A stiff wire can be wrapped around the ground ring and then the probe can be connected to the drain and source terminals of the HiperPFS with the shortest possible wire length.

### Inductor – Drain Current Measurement

A DC current probe is typically the most useful tool to measure the inductor current and input current of the PFC. When measuring the Inductor current, the probe should be inserted between the bridge rectifier and the inductor. The bridge rectifier end of the inductor is a relatively quiet node as compared to the end of the inductor which is connected to the MOSFET drain and the output diode. This minimizes common mode noise coupling into the probe thereby avoiding distortion in the measurement.

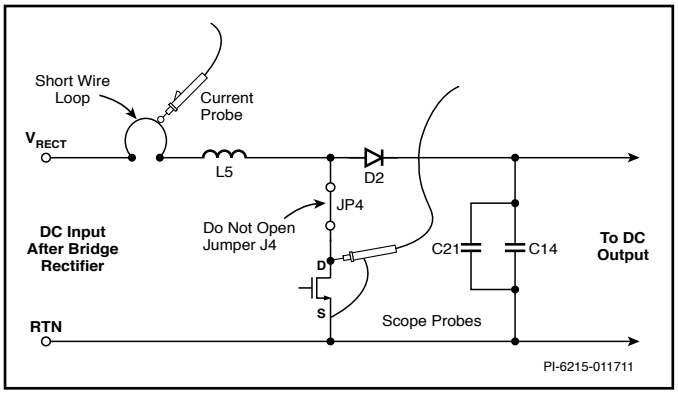



*Figure 47. Current Probe and Scope Probe Jack Insertion Locations.*

Most of the required information regarding the drain current at the turn-on and turn-off of the MOSFET can be obtained from the inductor current waveform. It is therefore recommended that the current probe should not be inserted in the connection between the drain node and the output diode-inductor junction. Inserting the current probe between the drain node and the output diode-PFC inductor connection requires that a small loop of wire be inserted in this location as shown in Figure 47. This loop contributes some stray inductance which causes increased voltage spike across the MOSFET at turn-off.

### No-Load Power and PF Measurement

The HiperPFS features an EcoSmart mode which results in burst mode of operation when the PFC is unloaded. The timing between the bursts is dependent on the size of the output capacitor and hence can vary between designs. It is often difficult to accurately measure input power to the circuit when the input power is pulsating at a low frequency. Many power meters feature special modes that allow for a long integration interval which can be used under such conditions. The power meter modes should be carefully programmed to achieve an error free measurement. The EPRI (Electric Power Research Institute) recommends inserting a LISN between the AC source used and the equipment under test. A 1 μF X capacitor is also required to be connected at the output of the LISN. The power analyzer should be connected close to the equipment under test so that voltage drops in the interconnecting wires do not result in measurement errors. This arrangement ensures that the impedance mismatch between the AC source and the PFC does not result in unwanted behavior such as source voltage distortion or oscillation which typically results in inaccuracy of no-load input power measurement or PF measurement at light loads.

## Tips for Design and Performance Improvement

### PF Improvement with Higher Inductance

The size of the PFC inductor is a trade-off between cost and required performance in terms of PF and THD of input current. For some designs it is a requirement that the input PF be above a certain value at 50% load. If the inductor value selected is failing to provide the required PF, the PF can be generally improved by increasing the inductance value.

PF at light load can often degrade because of excessive X capacitance in the EMI filter. Before increasing the size of the inductor, value of the X capacitance should be checked. If the conducted EMI measurement shows sufficient margin, it may be possible to improve PF at light load by reducing the size of the X capacitance.

### Selection of Suitable Diodes

Diode choice can have significant effect on overall performance. It is often difficult to gauge diode performance on the basis of

the data presented in the data sheet of the diode. Generally ultrafast diodes with soft recovery characteristics are best suited for PFC application.

Change of diode can have a very significant effect on efficiency. Diode choice should be carefully evaluated based on efficiency measurement. For high performance applications, use of a Silicon Carbide (SiC) Schottky diode may be considered if the increased cost is acceptable. Efficiency improvement of the order of 0.5% is possible when Silicon Carbide Schottky diodes are used instead of ultrafast recovery diodes.

A number of ultrafast recovery diodes are available however their data sheets often lack sufficient information to ensure that they are suitable. Reverse recovery parameters are often specified at current levels significantly lower than the rated current. Such diodes should be treated with caution and their performance carefully verified before use.

Several manufacturers provide diodes that are specially designed for PFC applications including Qspeed diodes from Power Integrations. These diodes have soft recovery characteristics with low $Q_{RR}$ and can provide efficiency performance between that of ultrafast and SiC diodes.

### Powder Core Inductor – Potential Benefits

The variable frequency architecture of the HiperPFS provides significant improvement in light load efficiency as compared to traditional fixed frequency architectures. The higher the value of the inductance, the lower is the load level at which the PFC will become discontinuous. The PF and waveform THD performance is superior when the converter remains in CCM mode of operation. It is often difficult to achieve a high inductance value using ferrite cores. Powder cores such as Sendust, Kool-mu and MPP yield a permeability that drops with DC bias. These cores can be effectively used to design inductors that offer higher inductance at light load and the inductance drops with DC bias resulting in a lower inductance at higher load levels. This can significantly improve PF at light load levels.

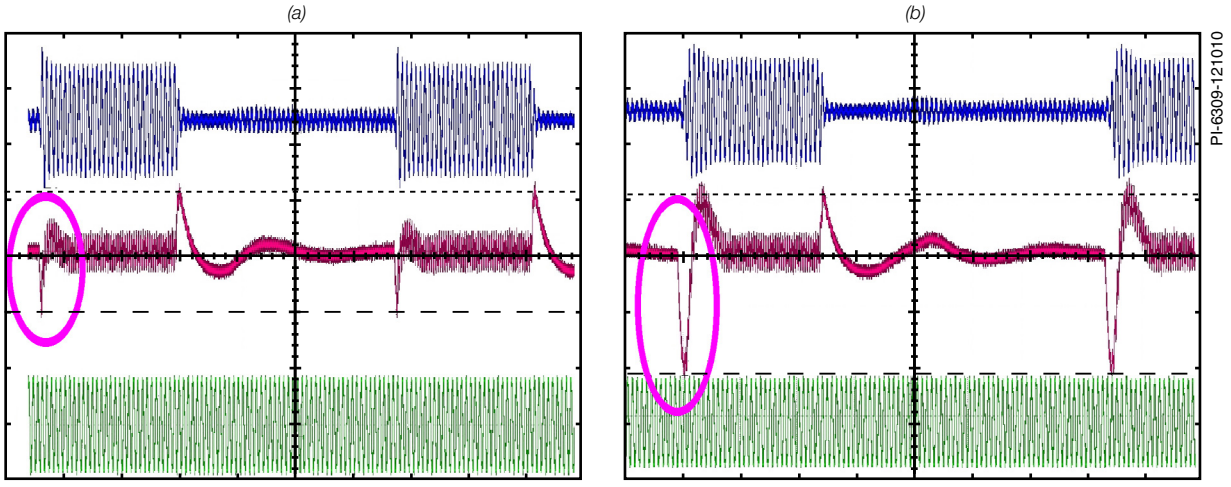
### Improving Efficiency

Efficiency improvement can be achieved by:

- Reducing the temperature of the parts by improving the thermal design.
- Using Litz wire instead of magnet wire for the inductor.
- Using a core material with lower core loss. Iron powder inductors will generally result in a lower efficiency.
- Using a high performance PFC output diode.
- Using a low ESR output capacitor.
- Using the next higher HiperPFS part.

### Bring-Up Procedure – Feedback Circuit Check

A defective feedback circuit will result in inadequate feedback voltage and could lead to catastrophic failure of the HiperPFS or the output capacitor. If the defect in the feedback circuit results in a floating FEEDBACK pin or a low voltage on the FEEDBACK pin, that will prevent the HiperPFS from switching and will not result in any failure.




Upper: Line Current, 5 A / div.
Middle: Output Voltage AC Coupled, 20 V / div.
Lower: Line Voltage, 200 V / div.

Upper: Line Current, 5 A / div.
Middle: Output Voltage AC Coupled, 20 V / div.
Lower: Line Voltage, 200 V / div.

*Figure 48. Waveforms – Effect on Non-Linear Amplifier on PFC Response (a). Effect of Linear Amplifier on PFC Response (b).*

One easy way to determine if the feedback divider network is correctly wired is to connect a bench power supply to the output of the PFC and raise its voltage gradually. If the external voltage source is raised to a level such that at a voltage equal to the rated PFC output voltage, the FEEDBACK pin voltage is around 6 V, which indicates that the FEEDBACK pin resistor divider is correctly configured. This simple test can often prevent damage at start if there are any mistakes in the feedback circuit divider network.

**Verification of Non-Linear Amplifier Using Dynamic Load Response**

The non-linear amplifier which is a part of the feedback network is made using a set of NPN and PNP transistors. The transistors are biased in a way that they do not conduct during normal operation. When the output experiences undershoot or overshoot, due to dynamic load changes, these transistors conduct momentarily to rapidly correct the feedback pin voltage in order to ensure a rapid response. The examples shown in Figure 48b shows the difference in performance if the PNP transistor is removed from the circuit. A step load response is an easy way to verify the operation of the transistors.

## Quick Design Checklist

As with any power supply design, all HiperPFS designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

- Maximum drain voltage – Verify that peak $V_{DS}$ does not exceed 530 V at lowest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just above the highest rated load or before the power supply output voltage starts falling out of regulation.
- Maximum drain current – At maximum ambient temperature, minimum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of inductor saturation and excessive leading edge current spikes. HiperPFS has a leading edge blanking time of 220 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit for the drain current waveform at the end of the 220 ns blanking period.
- Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the HiperPFS, PFC inductor, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of HiperPFS, as specified in the data sheet. A maximum package temperature of 110 °C is recommended to allow for these variations.

## Appendix A – Application Example

### A High Efficiency, 347 W, 380 VDC Universal Input PFC

The circuit shown in Figure 11 is designed using a PFS714EG device from the HiperPFS family of integrated PFC controllers. This design is rated for a continuous output power of 347 W and provides a regulated output voltage of 380 VDC nominal maintaining a high input power factor and overall efficiency from light load to full load.

Fuse F1 provides protection to the circuit and isolates it from the AC supply in case of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C3, C4, C5, C6 and C19 together with inductors L1, L2, L3 and L4 form the EMI filter reducing the common mode and differential mode noise. Resistors R1, R3 and CAPZero, IC U2 are required to discharge the EMI filter capacitors once the circuit is disconnected. CAPZero eliminates static losses in R1 and R2 by only connecting these components across the input when AC is removed.

The boost converter stage consists of inductor L5, diode rectifier D2 and the HiperPFS IC U1. This converter stage works as a boost converter and controls the input current of the power supply while simultaneously regulating the output DC voltage. Diode D1 prevents a resonant build up of output voltage at start-up by bypassing inductor L5 while simultaneously charging output capacitor C15. Thermistor RT1 limits the inrush input current of the circuit at start-up and prevents saturation of L5. In most high-performance designs, a relay will be used to bypass the thermistor after start-up to improve power supply efficiency. Therefore efficiency measurement, that represents the high performance configuration, the thermistors should be shorted. Capacitors C14 and C21 are used for reducing the loop length and area of the output circuit to reduce EMI and overshoot of voltage across the drain and source of the MOSFET inside U1 at each switching instant.

The PFS714EG IC requires a regulated supply of 12 V for operation and must not exceed 13.4 V. Resistors R6, R16, R17, Zener diode VR1, and transistor Q3 form a shunt regulator that prevents the supply voltage to IC U1 from exceeding 12 V. Capacitors C8, C18 and C20 filter the supply voltage and provide decoupling to ensure reliable operation of IC U1. Diode D5 prevents destruction of U1 if the auxiliary input is inadvertently connected reverse polarity.

The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R4, R5 and R19. The capacitor C12 filters any noise on this signal.

Divider network comprising of resistors R9, R10, R11, R12, R13, and R14 are used to scale the output voltage and provide feedback to IC U1. The circuit comprising of diode D4, transistor Q1, Q2 and the resistors R12 and R13 form a non-linear feedback circuit which improves the load transient response by improving the response time of the PFC circuit.

Resistor R7, R8, R15, and capacitors C13 and C17 are required for shaping the loop response of the feedback network. The combination of resistor R8 and capacitor C13 provide a low frequency zero and the resistor R15 and capacitor C13 form a low frequency pole.

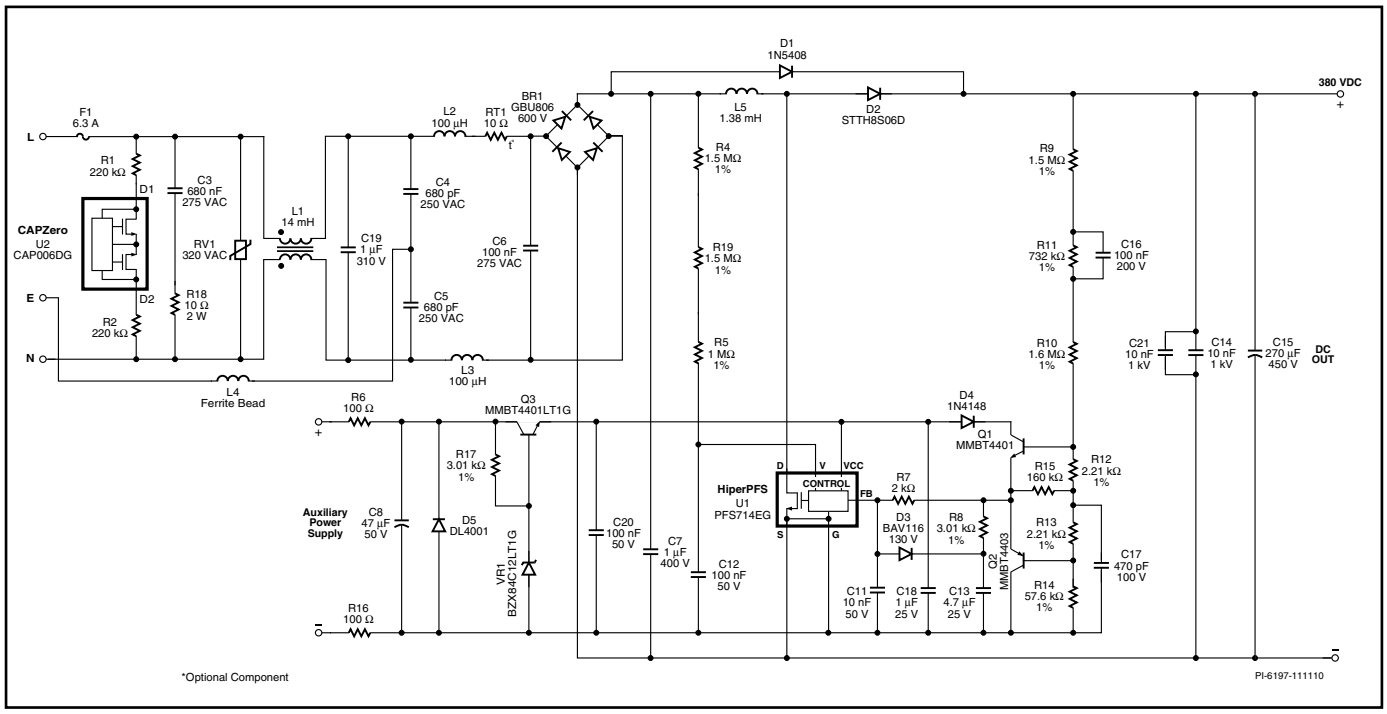



*Figure 49. 347 W PFC using PFS714EG.*

## Appendix B – Failure Mode Analysis Summary

### Device Level Failure Mode Analysis

Figure 50 is the device level failure mode analysis including the system effects of an open-circuit for each pin as well as adjacent pin-pin shorts. In each case a safe failure is expected.

### Feedback Network Failure Mode Analysis

Table 4 is the feedback network level failure mode analysis including the system effects of an open and short-circuit conditions for each component. In each case a safe failure is expected. [Refer Figure 18]

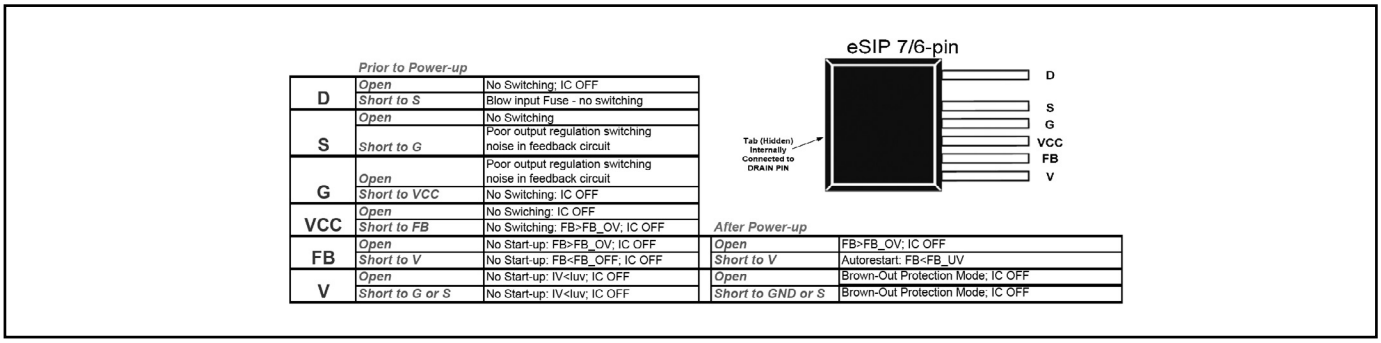



*Figure 50. Device Lev el Failure Mode Analysis.*

| | Open | Short |
|---|---|---|
| R2/R3 | Lost feedback signal;<br>Q2 pulls FEEDBACK pin below $FB_{UV}$ -> IC OFF | Reduced voltage divider; output voltage reduced |
| R4 | Lost feedback signal;<br>Q2 pulls FEEDBACK pin below $FB_{UV}$ -> IC OFF | Reduced voltage divider; output voltage reduced |
| R5 | Lost feedback signal;<br>Q2 pulls FEEDBACK pin below $FB_{UV}$ -> IC OFF | Reduced voltage divider; output voltage reduced;<br>fast UV threshold increases |
| R6 | Lost feedback signal; feedback above $FB_{OV}$ -> IC OFF | Reduced voltage divider; output voltage reduced;<br>fast UV threshold increases |
| R7 | Lost feedback signal; feedback above $FB_{OV}$ -> IC OFF | Q2 pulls FEEDBACK pin below $FB_{OV}$ -> IC OFF |
| R8 | Lost feedback signal;<br>internal IFB pulls feedback above $FB_{OV}$ -> IC OFF | Fast loop disabled; lost of loop speed-up circuit |
| R9 | No loop compensation; unstable operation; poor power factor | Poor loop compensation; unstable operation; poor power factor |
| R10 | Lost feedback signal;<br>Internal IFB pulls feedback above $FB_{OV}$ -> IC OFF | Increased noise susceptibility; unstable operation; poor power factor |
| C2 | Loss of soft-start; increased output overshoot at start-up | Reduced voltage divider; B+ reduced |
| C4 | No loop compensation, unstable operation; poor power factor | FEEDBACK pin below $FB_{UV}$ -> IC OFF |
| CFB | Increased noise susceptibility; unstable operation; poor power factor | Feedback pulled below $FB_{UV}$ -> IC OFF |
| C4 | No affect to circuit operation | Loss of fast OV/UV loop |
| Q1-E | Loss of fast OV loop | Short to Q1-B: Feedback above $FB_{OV}$ -> IC OFF<br>Short to Q1-C: Feedback above $FB_{OV}$ -> IC OFF |
| Q1-B | Loss of fast OV loop | Short to Q1-C: Feedback above $FB_{OV}$ -> IC OFF |
| Q1-C | Loss of fast OV loop | |
| Q2-E | Loss of fast OV loop | Short to Q2-B: No loop compensation<br>Short to Q2-E: Feedback below $FB_{UV}$ -> IC OFF |
| Q2-B | Loss of fast UV loop | Short to Q2-C: FEEDBACK pin below $FB_{UV}$ -> IC OFF |
| Q2-C | Loss of fast UV loop | |

*Table 4. Feedback Network Failure Mode Analysis.*

## Appendix C – Troubleshooting Matrix

| Problem Symptoms | Possible Causes of the Problem | Solutions to the Problem |
|---|---|---|
| No voltage at the output of the PFC | No AC input voltage at bridge rectifier input terminals. | 1. Check voltage at the input of the bridge rectifier.<br>2. Check components and connections in the EMI filter stage including the thermistor. |
| | Input fuse is open. | 1. Verify input fuse is functional. |
| Input fuse blows at start-up / HiperPFS blows at start-up | Components in the power stage are incorrectly assembled or damaged. | 1. Verify polarities of the components used (Ex. – Bridge rectifier polarity).<br>2. Verify interconnections between components. Check connection between PFC output diode and HiperPFS Drain terminal. |
| | HiperPFS Drain terminal is shorted to the Source terminal on the circuit board. | 1. Check for solder bridging and short-circuits on PCB.<br>2. Verify if HiperPFS is damaged with Drain and Source short.<br>3. Verify PFC output diode D1 polarity and make sure the part is functional. |
| | Failed insulation between HiperPFS and heat sink. | 1. Verify heat sink assembly.<br>2. Check for damaged insulator.<br>3. Violation of creepage or clearance distance in heat sink assembly causes arcing, resulting in failure of HiperPFS. |
| | Insufficient fuse current rating. | 1. Verify fuse rating using PIXIs.<br>2. Replace fuse with sufficient current rating and $I^2t$ rating. |
| | Overload at output. | 1. Check the load current. |
| Output voltage goes up above 400 V and decreases slowly | Load is disconnected intermittently when the PFC is on. | 1. Turn off the AC input and verify the connection to the load. |
| | NPN transistor Q1 is not functional. | 1. Check transistor Q1 connection.<br>2. Check if diode D3 is open or its polarity is reversed.<br>3. Check if capacitor C2 is open. |
| Output voltage is permanently over 105% of the nominal output rating | Incorrect values of feed back circuit components. | 1. Verify values of components used in the feedback circuit. |
| | Defective or missing capacitors in feed back network. | 1. Replace the defective capacitors and install any missing components. |
| | Input voltage peak is higher than the $V_{OUT}$ nominal rating. | 1. Verify the PFC input voltage. |
| | Transistor Q2 conducts during normal operation. | 1. Verify values of components used in the feed back circuit.<br>2. Confirm transistor Q2 is not defective or connected incorrectly. |
| PFC output voltage is below the nominal voltage permanently | Voltage divider network has a shorted resistor or resistors with incorrectly values. | 1. Check short connections of R2/R3/R4/R5/R6/C2.<br>2. Check line-sensing network resistors R1. |
| | $V_{CC}$ of the HiperPFS part is below specified limits. | 1. Verify voltage across VCC and GROUND pins is greater than 10.2 V. |

| Problem Symptoms | Possible Causes of the Problem | Solutions to the Problem |
|---|---|---|
| PFC does not start-up. | HiperPFS pins are incorrectly connected on the circuit board. | 1. Confirm that none of the HiperPFS pins are open or are accidentally connected to the adjacent pins on the circuit board. |
| | Output capacitor polarity is reversed. | 1. Verify polarity of the output capacitor. |
| | FEEDBACK pin is floating. | 1. Check feedback circuit components R2/R3/R4/R5/R6/R7/R8/R10 and ensure that correct component values are used. |
| | Low-voltage on FEEDBACK pin. | 1. Check feedback circuit components R7, C4 and $C_{VCC}$ for likely short.<br>2. Check PNP transistor Q2 base, emitter and collector terminals for accidental short between the pins. |
| | High-voltage on FEEDBACK pin. | 1. Check for short between collector, base and emitter of NPN transistor Q1 |
| | V pin current is less than $I_{UV-}$ | 1. Verify the values of line sensing resistor R1 and its connections. |
| $V_{OUT}$ voltage undershoot >40 V during load transient. | PNP transistor Q2 is not functional. | 1. Check Q2 connections.<br>2. Check function of Q2.<br>3. Check bias of Q2 refer to AN-52 for more information on waveforms. |
| Excessive output voltage overshoot and undershoot during startup or during a load transient. | Transistors Q1 and Q2 are both not functional. | 1. Check if resistor R8 is shorted or of incorrect value.<br>2. Check values of resistors R5 and R6. |
| | Loss of loop-compensation. | 1. Check the values of components R8, R9 and capacitor C4. |
| Unstable operation and/or poor input power factor. | Feedback compensation is incorrect. | 1. Check for component values of components R8, R9, R10, C4 and $C_{FB}$. |
| | Noise injection in the feedback circuit. | 1. Verify layout according to data sheet recommendation.<br>2. Verify the placement of decoupling capacitors.<br>3. Check the PCB layout of ground loops. |
| | Noise injection in the V pin signal. | 1. Verify layout according to data sheet recommendation.<br>2. Verify the placement of V pin decoupling capacitor.<br>3. Check the layout of ground loops in PCB. |
| | Noise injection due to floating heat sinks. | 1. Connect heat sinks close to the source terminal with the shortest possible trace. |
| | Undersized PFC inductor used. | 1. Verify the inductor L1 value used. |
| | Undersized bridge rectifier decoupling capacitor. | 1. Choose the correct value and low ESR/ESL capacitor to limit the high frequency ripple across this capacitor ($C_{IN}$). |
| | Incorrect EMI filter stage components used. | 1. Inadequate differential mode filter or filter resonance is resulting in instability. Verify input current waveform for signs of resonance. |
| | Excessive voltage ripple on VCC pin. | 1. Verify VCC pin decoupling capacitor and filter capacitor value and circuit board layout.<br>2. Verify the operation of the linear regulator if used.<br>3. Reduce high frequency switch noise on $V_{CC}$. |
| HiperPFS part fails to brown-in. | Excess noise on VCC pin. | 1. Inadequate VCC pin decoupling capacitor and filter capacitor.<br>2. Verify the operation of the linear regulator if used.<br>3. Reduce high frequency switch noise on $V_{CC}$.<br>4. Check for layout errors which results in poor grounding of decoupling capacitor. |

| Problem Symptoms | Possible Causes of the Problem | Solutions to the Problem |
|---|---|---|
| Huge resonant voltage ringing on $V_{DS}$ during start up, which results in HiperPFS failure. | By pass diode D2 is not functional or it is missing. | 1. Replace bypass diode D2 with a diode with appropriate current rating. |
| Brown-in / Brown-out at incorrect voltage levels. | Incorrect line-sense resistor value. | 1. Verify line sensing network resistor R1 value (recommend 4 MΩ for universal input parts, 9 MΩ for 230 VAC only parts. 1% tolerance parts are recommended). |

Note: For reference diagram, refer to Figure 4.

| Revision | Notes | Date |
|---|---|---|
| A | Initial Release | 02/11 |
| B | Updated Equations on page 14 | 12/11 |
| C | Updated with new PI style. | 12/17 |

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