# Application Note AN-92
# MinE-CAP Family

Design Guide

## Introduction

The MinE-CAP IC Family enables the implementation of universal-input AC/DC power converters and allow power densities greater than 25 W/in$^3$. It does this by significantly reducing the physical size of what has typically been one of the largest components in an off-line power supply – the input bulk capacitor. With the MinE-CAP IC, a reduction of up to 50% in bulk capacitor volume is possible. In addition, the MinE-CAP IC manages inrush current during AC turn-on and eliminates the need for an NTC thermistor and a large slow-blow fuse in the input stage which leads to further space savings.

Off-line power supplies like the one shown in Figure 1 typically use a filter capacitor to "smoothen" the rectified mains voltage and to supply current when the rectifier diodes turn off during each line cycle. For universal AC input designs, the capacitance of the filter capacitor is sized to support the lowest AC input, while the voltage rating is based on the maximum AC line voltage. However, the physical size of capacitors increase with capacitance and more so with voltage-rating, thus typical designs will have physically large capacitors with –

A. Enough capacitance but with a voltage rating that is too high for low-line input
B. Appropriate voltage rating but unnecessarily large capacitance for high-line input

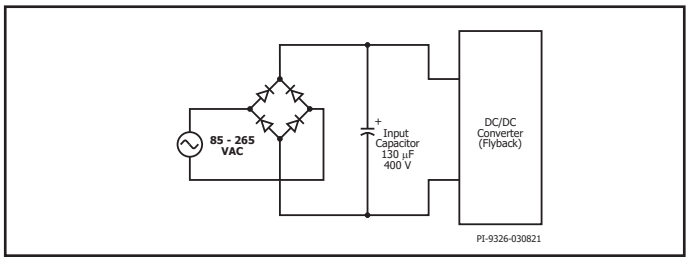



Figure 1. Input Stage of a Typical Off-Line AC-DC Converter.

The MinE-CAP IC addresses issues (A) and (B) by splitting the input capacitance between two capacitors, $C_{HV}$ (high-voltage) and $C_{LV}$ (low-voltage), as shown in Figure 2. During high-line operation, the MinE-CAP IC disconnects $C_{LV}$ leaving $C_{HV}$ to function as the only input capacitor. At low-line, the MinE-CAP IC adds $C_{LV}$ to the system to increase the input capacitance and maintain input voltage ripple at an appropriate level. This scheme allows the designer to allocate the majority of the required capacitance for low-line conditions to $C_{LV}$ and use low-capacitance, high-voltage capacitors for $C_{HV}$. This translates to bulk capacitors with significantly less volume and better form-factor than those seen in conventional designs.

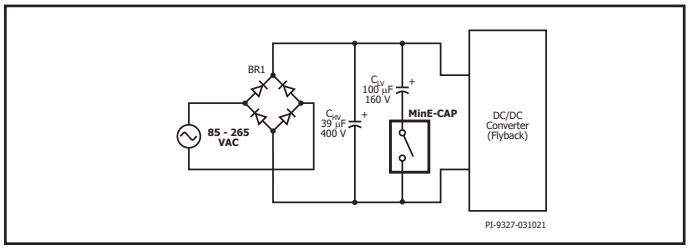



Figure 2. Off-line AC-DC Converter with MinE-CAP.

## Example Design Comparison

Table 1 and Figure 3 show the volume reduction that can be achieved with the MinE-CAP IC when used for a 60 W USB-C PD power supply design. DER-803 is a 60 W USB-C PD power supply using and InnoSwitch3-Pro (INN3379C) IC with a single 100 µF input capacitor. DER-822 has the same specification as DER-803 but the single input capacitor is replaced by a MinE-CAP IC-based circuit employing a 160 V 68 µF low-voltage (LV) Capacitor, and a 400 V 33 µF high-voltage (HV) capacitor.

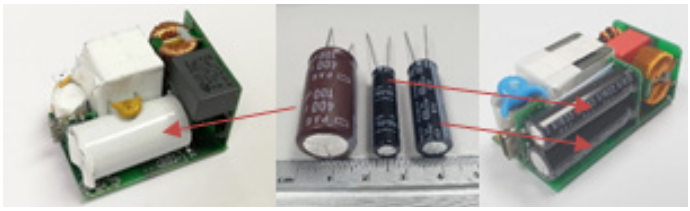


Figure 3. Size Comparison Between a Design Employing a Single 400 V 100 µF Capacitor (DER-803 - left) and One Using a Combination of a 160 V 68 µF and a 400 V 33 µF Capacitors (DER-822 - right).

The schematics for both DERs shown are similar – the only major difference being the input bulk capacitor circuit. Electrical performance for both designs is also similar. The use of the MinE-CAP IC allows the DER-822 volume to be 40% less than that of DER-803.

| DER-803 | | DER-822 |
|---|---|---|
| (1) 400 V 100 µF Rubycon BXW Series | **Input Capacitor(s)** | (1) 68 µF 160 V Rubycon TXV Series (LV Cap) and (1) 33 µF 400 V Rubycon BXW Series (HV Cap) |
| 47 mm x 35 mm x 29 mm | **Unit Form Factor (L x W x H)** | 52 mm x 26 mm x 22 mm |
| 20.62 | **Power Density (W/in$^3$) (No Enclosure)** | 33.15 |
| EQ25 | **Transformer Core** | ATQ23.7/16 |

Table 1. DER-803 and DER-822 Comparison.

## Scope

This application note is intended as a design guide for engineers designing an isolated AC-DC single-stage flyback power supply using the MinE-CAP family of devices. This document describes the proper selection of components, particularly the input bulk capacitors. It is assumed that the designer is using the MinE-CAP together with the InnoSwitch3 family of power conversion ICs. However, the design equations shown can be used for applications beyond the scope of this document.

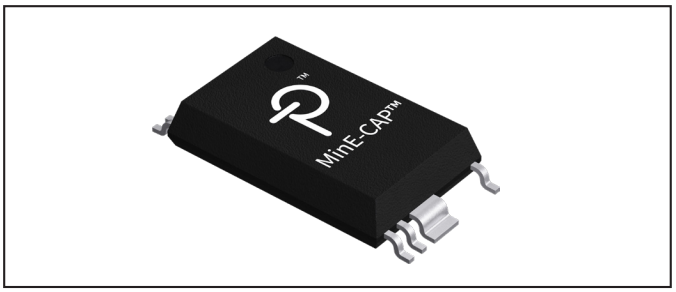



Figure 4. MinE-CAP MINSOP16 Package.

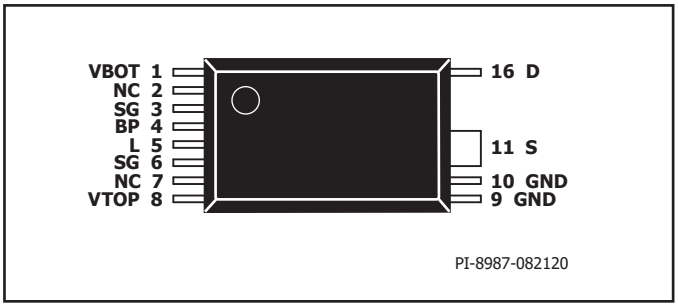



Figure 5. MinE-CAP Pin Configuration.

## Pin Descriptions

The MinE-CAP is a 12-pin device that is housed in Power Integration's proprietary MinSOP-16 package (refer to Figure 5). The functions of each pin are described below:

**VBOT (Pin 1)**
A high-voltage pin connected to the negative terminal of capacitor $C_{LV}$ through a resistor. The VBOT pin is used in tandem with the VTOP to determine the voltage across $C_{LV}$. This pin is also used for trickle charging of $C_{LV}$.

**NO CONNECTION (NC) (Pins 2, 7)**
Must be left OPEN. Do not connect to any node or traces.

**SIGNAL GROUND (SG) (Pins 3, 6)**
The ground node for the internal digital controller. Must be connected externally to the S Pin.

**BYPASS Pin (BP) (Pin 4)**
Connection point for an external bypass capacitor for the IC's internal regulator. Also serves as the IC's bias supply pin and must be connected to an external power supply or the BPP pin of an InnoSwitch3 device. The recommended bypass capacitor value is between 10 nF and 100 nF.

**LINE (L) (Pin 5)**
Connects directly to the V pin of an InnoSwitch3 IC and is used to relay bulk capacitor voltage, start-up and fault information when the MinE-CAP is used with another controller, this pin can either be connected to ground or to external fault detection circuitry.

**VTOP (Pin 8)**
A high-voltage pin connected to the positive terminal of $C_{LV}$ through a resistor. The VTOP pin is used to monitor bulk voltage as well as the voltage across $C_{LV}$.

**GROUND (GND) (Pins 9, 10)**
Must be connected to the SOURCE pin.

**SOURCE (S) (Pin 11)**
The Source node of the internal switch.

**DRAIN (D) (Pin 16)**
The Drain node of the internal switch.

## Typical Application Example

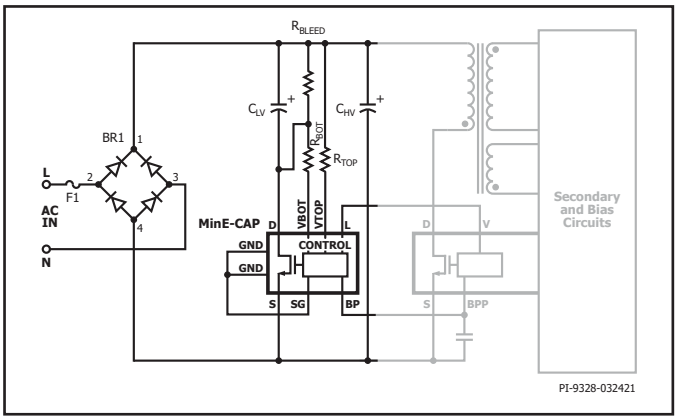



Figure 6. Typical Application Example.

Figure 6 shows the schematic of the MinE-CAP when used together with the InnoSwitch3 family of controllers. Description for each discrete component is listed below:

1. **$R_{TOP}$ and $R_{BOT}$** – The currents through these resistors are used by the MinE-CAP to determine the voltage across $C_{HV}$ and $C_{LV}$ input capacitors. These resistors also program the regulation voltage and ripple across $C_{LV}$ as well as the OV/UV levelIs for the InnoSwitch3 IC.
2. **$R_{BLEED}$** – Bleeder resistor connected in parallel with $C_{LV}$. This resistor is used to discharge or shunt current away from $C_{LV}$ when the MinE-CAP switch is off to help maintain regulation across the LV capacitor. A 4 MΩ 1206 SMD resistor is recommended.
3. **$C_{HV}$ and $C_{LV}$** – The high-voltage and low-voltage input bulk capacitors.

## Component Selection Guide

**$R_{TOP}$ and $R_{BOT}$ Selection**
When used with the InnoSwitch3 family of controllers, the recommended values for $R_{TOP}$ and $R_{BOT}$ are

$$R_{TOP} = 3.8\ M\Omega \text{ and } R_{BOT} = 931\ k\Omega$$

This combination will program the MinE-CAP to regulate the voltage across $C_{LV}$ to a maximum of approximately 140 V with a maximum voltage ripple of 16.9 V. This $R_{TOP}$ value will also program the InnoSwitch3 IC's UV/OV nominal thresholds to

$$V_{InnoSwtich,OV} = 261\ VAC$$
$$V_{InnoSwitch,Brown\text{-}In} = 57\ VAC$$
$$V_{InnoSwitch,Brown\text{-}Out} = 50\ VAC$$

All resistors must be 1% tolerance or better with sufficient voltage rating. For wide-range or high-line input voltage designs, a 1206 SMD resistor package is recommended.

If a different InnoSwitch3 UV/OV threshold is desired, calculate $R_{TOP}$ using the desired threshold*. The value for $R_{BOT}$ should be recalculated using the following equations:

$$V_{LVCAP(MAX)} = VTOP - \left(\frac{R_{BOT}}{R_{BOT(BASE)}}\right) \times \left(VTOP\left(\frac{R_{TOP(BASE)}}{R_{TOP}}\right) - V_{TRKLCHRG(MAX)}\right)$$

$$V_{LVCAP(MIN)} = VTOP - \left(\frac{R_{BOT}}{R_{BOT(BASE)}}\right) \times \left(VTOP\left(\frac{R_{TOP(BASE)}}{R_{TOP}}\right) - V_{TRKLCHRG(MIN)}\right)$$

Where

$V_{LV\ CAP(MAX)}$ = maximum allowable $C_{LV}$ voltage (typ. 140 V)

$R_{BOT(BASE)}$ = 1.0 MΩ; $R_{TOP(BASE)}$ = 4.0 MΩ

$V_{TRKLCHG(MAX)}$ = 140 V; $V_{TRKLCHG(MIN)}$ = 130 V

$V_{TOP}$ = Peak Bulk Voltage = √2 $V_{IN(RMS)}$

*Refer to InnoSwitch3 family data sheet

Take care when selecting the values for $R_{TOP}$ and $R_{BOT}$. Always check to confirm that the maximum LV capacitor voltage does not exceed the capacitor voltage rating at any point in the AC input range. Figure 7 and Figure 8 show the maximum LV capacitor voltage across universal AC input with either $R_{TOP}$ or $R_{BOT}$ fixed.

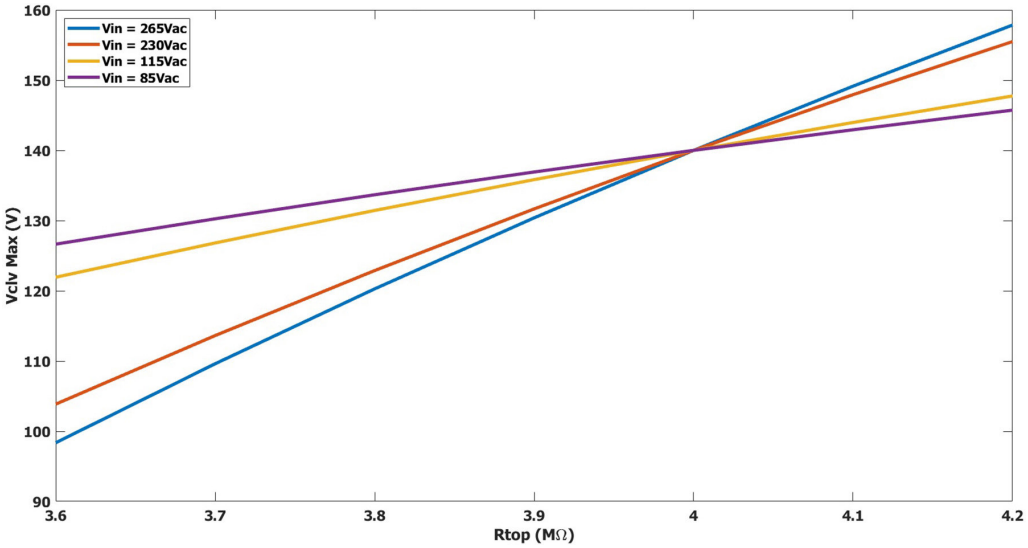



Figure 7. Maximum Voltage Across $C_{LV}$ vs. Varying $R_{TOP}$; $R_{BOT}$ = 1.0 MΩ.

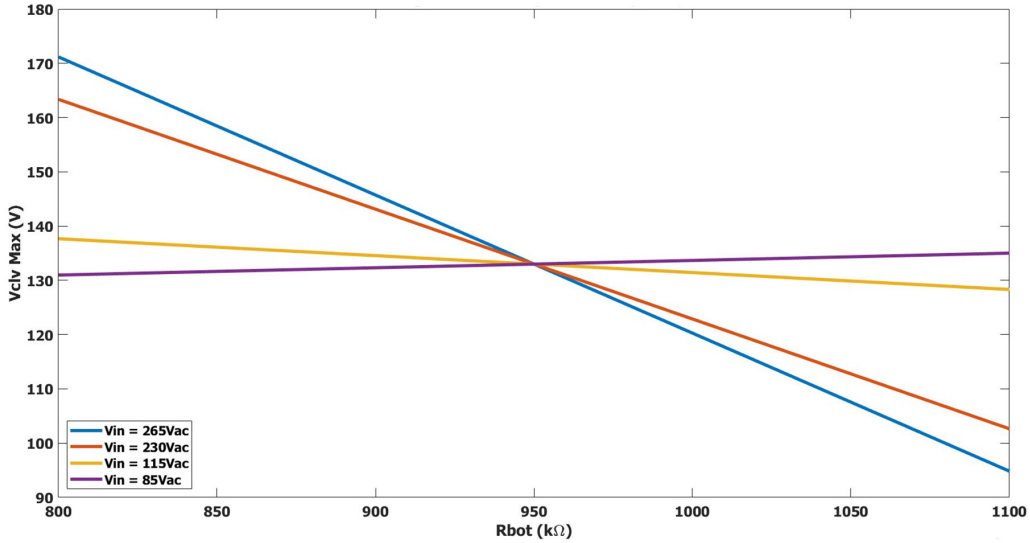



Figure 8. Maximum Voltage across $C_{LV}$ vs. Varying $R_{BOT}$; $R_{TOP}$ = 3.8 MΩ.

## Step-by-Step Input Capacitor Selection Guide

This section outlines the steps required for the calculation of the bulk capacitors values. Derivation of relevant equations can be found in Appendix A at the end of this document.

1. Identify key design parameters:
   a. Maximum output power ($P_{OUT}$)
   b. Assumed efficiency ($\eta$)
   c. Minimum allowable bulk capacitor voltage ($V_{DC(MIN)}$)
   d. AC Input Range. 85 V to 265 V VAC is typical.

2. Solve for the minimum required capacitance at the minimum AC Input. This capacitance value is the required minimum total capacitance value for the design, $C_{TOTAL(MIN)}$.

3. Solve for the minimum required high-voltage capacitance (HV-Cap), $C_{HV(MIN)}$. Determine the HV capacitor value at the low-end of high-line input. There are no hard rules when setting constraints for the HV capacitor, but the following must be considered:

   a. For high-line operation, the MinE-CAP IC disconnects $C_{LV}$ from the system. This will cause a significant increase in EMI emissions due to the sudden increase in input capacitor ESR, thus a high-voltage capacitor with low ESR is necessary.
   b. If we calculate $C_{HV}$ using $V_{DC(MIN)}$, the resulting capacitance will be very low which means conduction time for the bridge diodes will also significantly increase. This will adversely affect the EMI and may decrease efficiency.
   c. Theoretically, it is possible to use very low capacitance values for the HV capacitor. However, this may cause the design to fail during surge testing especially at high-line when $C_{LV}$ is disconnected from the circuit.
   d. Given the above concerns, calculate $C_{HV(MIN)}$ using a new minimum DC bus voltage, $V_{HVDC(MIN)}$, which is significantly higher than $V_{DC(MIN)}$.
   e. In general, choose $C_{HV}$ with the highest capacitance and lowest ESR that fits within size constraints.

4. Once $C_{HV(MIN)}$ has been calculated, select the next-higher standard value capacitor available. Make sure the chosen capacitor meets thermal requirements. This will be the actual capacitance used for $C_{HV(ACT)}$.

5. Subtract $C_{HV(ACT)}$ from the minimum total value calculated in Step 2 ($C_{TOTAL(MIN)} – C_{HV(ACT)}$). The result is $C_{LV(MIN)}$.

6. The actual LV capacitor will be the next higher standard value capacitor to $C_{LV(MIN)}$. This will then be used as the actual LV capacitor, $C_{LV(ACT)}$.

7. Calculate all line, rectifier and capacitor voltage and current parameters using $C_{TOTAL(ACT)} = C_{HV(ACT)} + C_{LV(ACT)}$. These values will be used to select the appropriate rectifier and EMI filter components for the design.

Note: As described above it is possible to select HV capacitors with very low capacitance and assign the majority of the required input capacitance to the LV capacitor. However, low HV capacitor values might negatively impact efficiency, EMI, and surge immunity.

## Design Example

Find the capacitors to be used for a charger design with the following specifications:

A. Universal AC input (85 to 265 VAC)
B. 60 Hz at low-line, 50 Hz at high-line
C. 65 W output power, 92% assumed efficiency
D. $V_{MIN}$ = 85 VDC
E. Form factor: 82 mm (L) × 51 mm (W) × 12 mm (H)

### Step 1: Calculate for $C_{TOTAL(MIN)}$

Use $V_{IN}$ = 85 $V_{AC(VMIN)}$ = 85 VDC and the given output power and efficiency. The total input capacitance required is

$$C_{TOTAL(MIN)} = 128.92\ \mu F$$

### Step 2: Find $C_{HV(MIN)}$ and $C_{HV(ACT)}$

Assume minimum high-line voltage of 180 VAC. To reduce losses at high-line, we want the bulk voltage to always be greater than 180 VDC. The HV capacitor diameter must be at most 10 mm to comply with form factor requirements.

Calculating for $C_{HV(MIN)}$, we get

$$C_{HV(MIN)} = 33.11\ \mu F$$

Peak voltage at $V_{IN}$ = 265 VAC is 375 V.

The next higher value capacitor is 39 µF so the HV capacitor should have the following specifications

$$C_{HV(ACT)} = 39\ \mu F\ 400\ V$$

### Step 3: Find $C_{LV(MIN)}$ and $C_{LV(ACT)}$

$$C_{LV(MIN)} = C_{TOTAL(MIN)} – C_{HV(ACT)} = 89.92\ \mu F$$

Next higher standard value is 100 µF. The MinE-CAP regulates the LV capacitor voltage to approximately 140 V so the LV capacitor specifications should be

$$C_{LV(ACT)} = 100\ \mu F\ 160\ V$$

### Step 4: Use $C_{TOTAL(ACT)}$ to Solve for the Maximum Line, Rectifier and Capacitor Currents at 85 VAC Input

$$C_{TOTAL(ACT)} = 139\ \mu F$$

$$I_{LINE(RMS)} = 1.52\ A$$

$$I_{LINE(PEAK)} = I_{RECTIFIER(PEAK)} = 4.98\ A$$

$$I_{RECTIFIER(RMS)} = 1.07\ A\ (per\ diode)$$

$$I_{RECTIFIER(AVERAGE)} = 0.34\ A\ (per\ diode)$$

$$I_{CAPACITOR(RMS)} = 1.35\ A$$

$$I_{CAPACITOR(RIPPLE)} = 4.98\ A_{pk\text{-}pk}$$

### Step 5: Solve for the Capacitor Current at Minimum of High-Line (180 VAC Input and $V_{MIN}$ = 180 VDC in this Example.)

$$I_{CAPACITOR,\ R_{MS(HL)}} = 0.64\ A$$

$$I_{CAPACITOR,\ RIPPLE(HL)} = 2.4\ A_{PK-PK}$$

### Step 6: Finalize Capacitor Specifications

At low-line, the capacitor current is split between the HV and LV capacitor. Using capacitor current division and solving for the capacitor currents we get

$$I_{CLV(RMS)} = 0.97\ A$$

$$I_{CLV(RIPPLE)} = 3.58\ A_{PK-PK}$$

$$I_{CHV(RMS)} = 0.39\ A$$

$$I_{CHV(RIPPLE)} = 1.4\ A_{PK-PK}$$

Compare the high-line and low-line currents and use the maximum when specifying required capacitors.

Complete Specifications are:

LV Capacitor: 100 µF, 160 V, 3.58 A ripple rating

HV Capacitor: 39 µF, 400 V, 2.4 A ripple rating

Both capacitors must have a maximum diameter 10 mm and a length of 40 mm to fit into the capacitor landing area in the PCB.

Note that ripple rating is at 120 Hz.

### Step 7: Use Calculated Values to Specify Rectifier and EMI Components

#### Rectifier Requirements

A. Average current rating of the rectifier must be greater than $I_{RECTIFIER(AVERAGE)}$.
B. Use $I_{RECTIFIER(RMS)}$ and $I_{RECTIFIER(AVERAGE)}$ to estimate power loss for thermal management and component power ratings.
C. Voltage rating must be greater than $\sqrt{2}V_{IN,AC(MAX)}$ where $V_{IN,AC(MAX)}$ is the maximum AC input voltage.

#### EMI Component Requirements

A. Use $I_{LINE(RMS)}$ to calculate losses in the common-mode and differential-mode chokes. Excessive losses may lead to high temperature and saturation.
B. Use $I_{LINE(PEAK)}$ to determine for the maximum flux density for the filter chokes. This is extremely important when stand-alone differential-mode chokes are used (as compared to the leakage from CM chokes).

#### Other Input Components

A. Use the calculated currents to appropriately size wires and PCB tracks to minimize losses and for correct sizing of the slow blow fuse.

## MinE-CAP Start-Up

During initial AC turn-on, the MinE-CAP IC controls the charging current for the high capacitance, low-voltage capacitor effectively controlling the total inrush current. Depending on whether the power supply starts at high or low-line, the MinE-CAP employs one of the charging methods described below. The complete start-up sequence is shown in the flowchart in Figure 9.

#### Active Charging

- Initiated when $V_{BULK} \leq V_{HL(START-UP)}$
- Constant power charging limited to $P_{ACTV(CHG)}$
- Active charging only happens once during start-up
- Once complete, subsequent re-charging of the LV capacitor uses trickle charging
- A high-voltage capacitor is charged using current pulses with a period of $t_{ACTV(CHG)PRD}$ and duty cycle from 3 – 39% through the MinE-CAP switch
- Charging current is limited to $I_{ACTV(CHG)}$
- Active charge time is less than or equal to $t_{ACTV(CHG)MAX}$.

#### Trickle Charging

- Initiated when $V_{BULK} > V_{HL(START-UP)}$
- An internal switch is turned on and the LV capacitor is charged though resistor $R_{BOT}$
- After start-up, trickle charge occurs when the MinE-CAP switch is off and
  - LV capacitor voltage is below $V_{LVCAP(MIN)}$
- Trickle charge is disabled when the MinE-CAP switch is off and
  - LV capacitor voltage reaches $V_{LVCAP(MAX)}$.

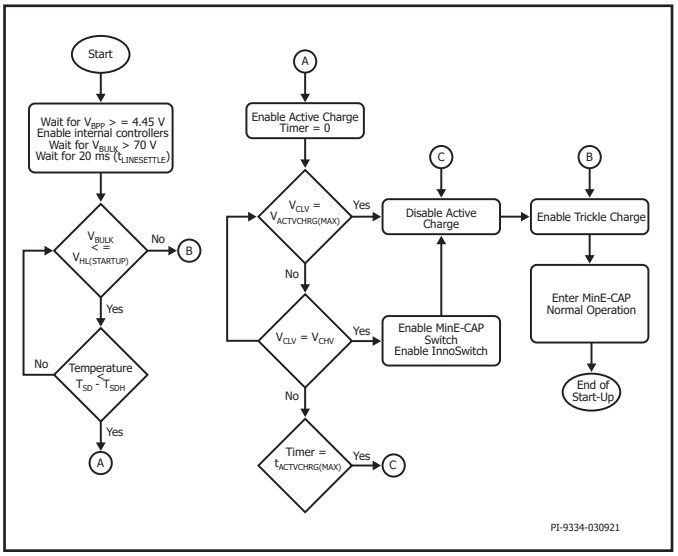



Figure 9. MinE-CAP Start-up Flowchart.

| Parameter | Symbol | Nominal Value |
|---|---|---|
| High-Line Start-up Threshold | $V_{HL(STARTUP)}$ | 214 VDC |
| Input Line Settling Time | $t_{LINESETTLE}$ | 20 ms |
| Maximum Active Charge-up Voltage | $V_{ACTVCHRG(MAX)}$ | 114 VDC |
| Maximum Trickle Charge Voltage | $V_{TRKLCHRG(MAX)}$ | 134 VDC |
| Active Charge Constant Power | $P_{ACTV(CHRG)}$ | 10 W |
| Maximum Active Charge-up Time | $t_{ACTVCHRG(MAX)}$ | 173.3 ms |
| Active Charge Pulse Period | $t_{ACTVCHRG(PRD)}$ | 1.365 ms |
| Active Charge Maximum Current | $I_{ACTV(CHRG)}$ | 1.2 A |
| Thermal Shutdown | $T_{SD}$ | 140 °C |
| Thermal Shutdown Hysteresis | $T_{SD(H)}$ | 70 °C |

Table 2. Parameters That Influence MinE-CAP Start-Up.

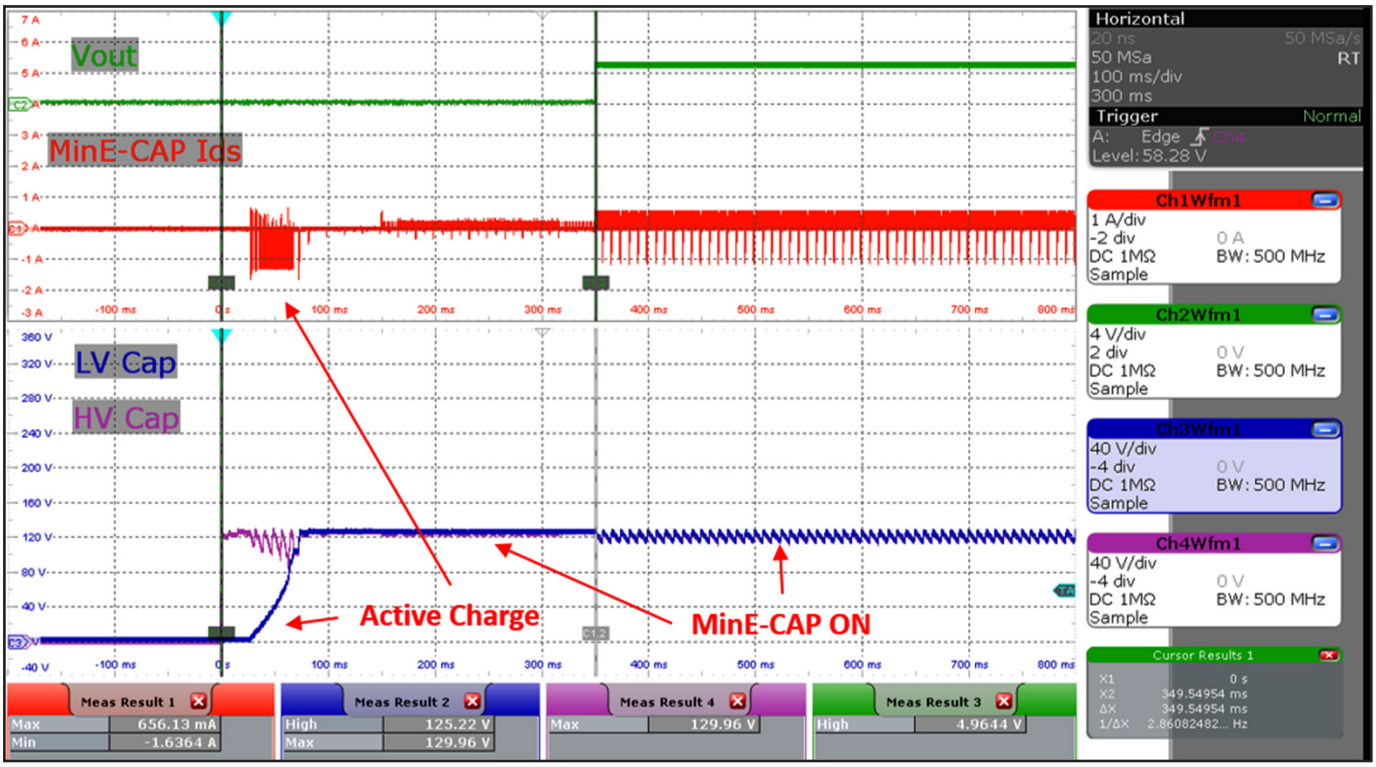



Figure 10. MinE-CAP IC Circuit Start-up Waveforms (VIN = 90 VAC, Load = 5 V, 3 A), MinE-CAP IC Turns On After Active Charge.

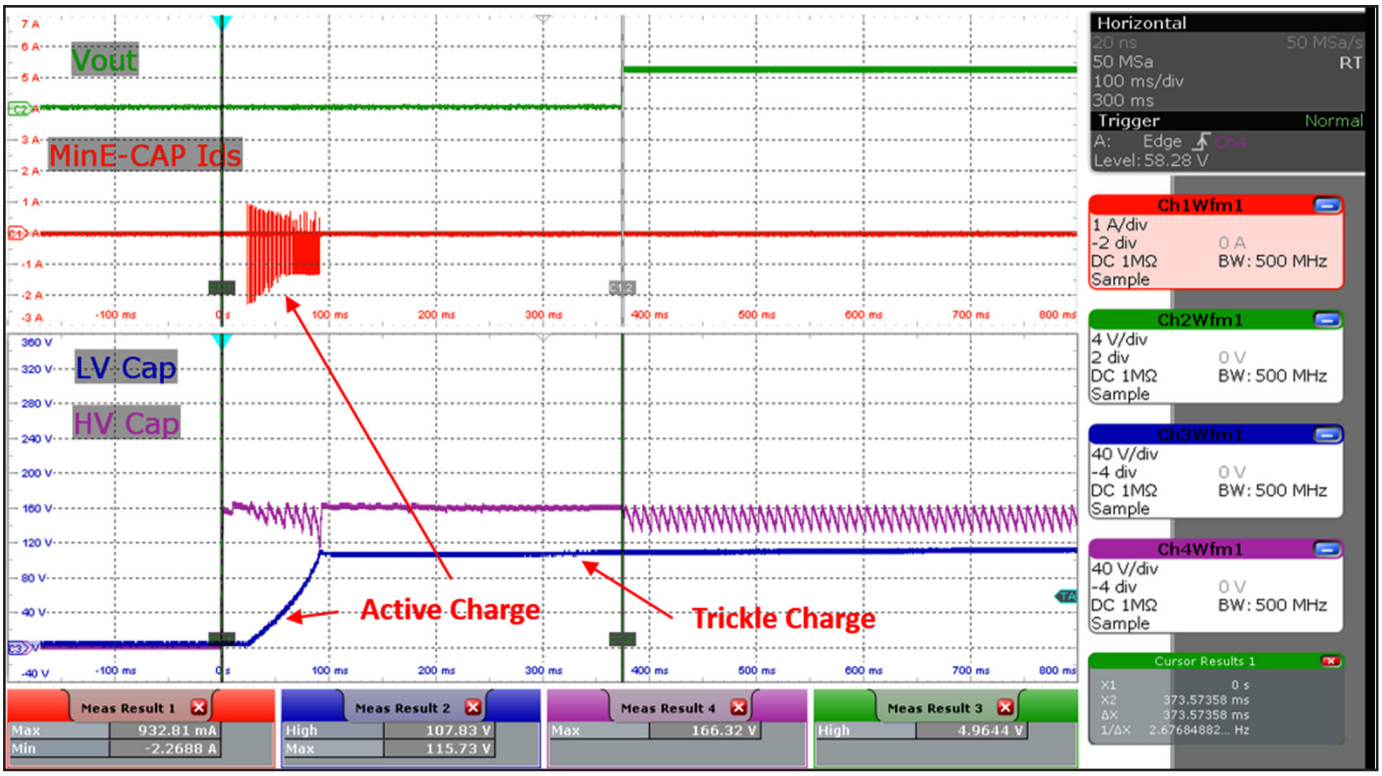



Figure 11. MinE-CAP IC Circuit Start-up Waveforms (VIN = 115 VAC, Load = 5 V, 3 A), MinE-CAP IC Turns Off Until Bulk Voltage Drops $C_{LV}$ Voltage.

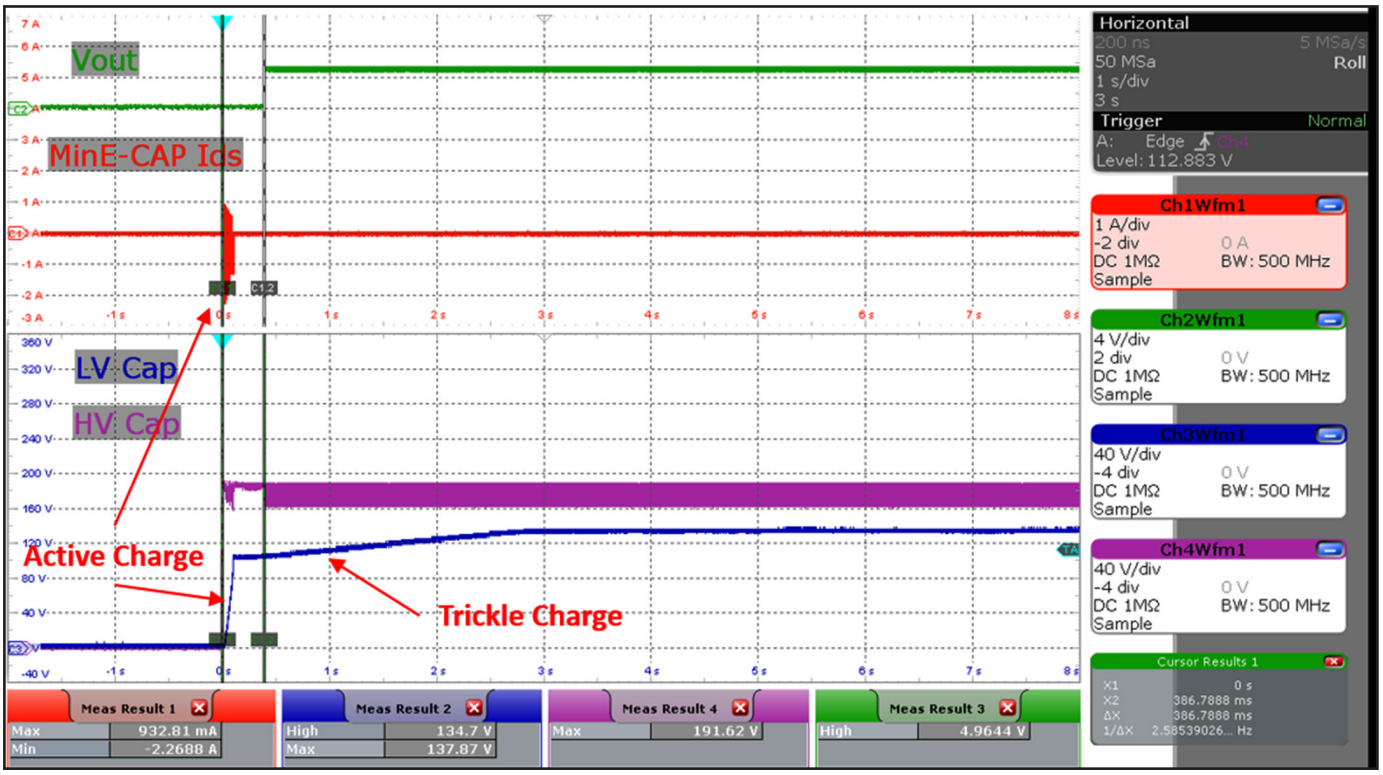



Figure 12. MinE-CAP IC Start-up Waveforms ($V_{IN}$ = 132 VAC, Load = 5 V, 3 A).

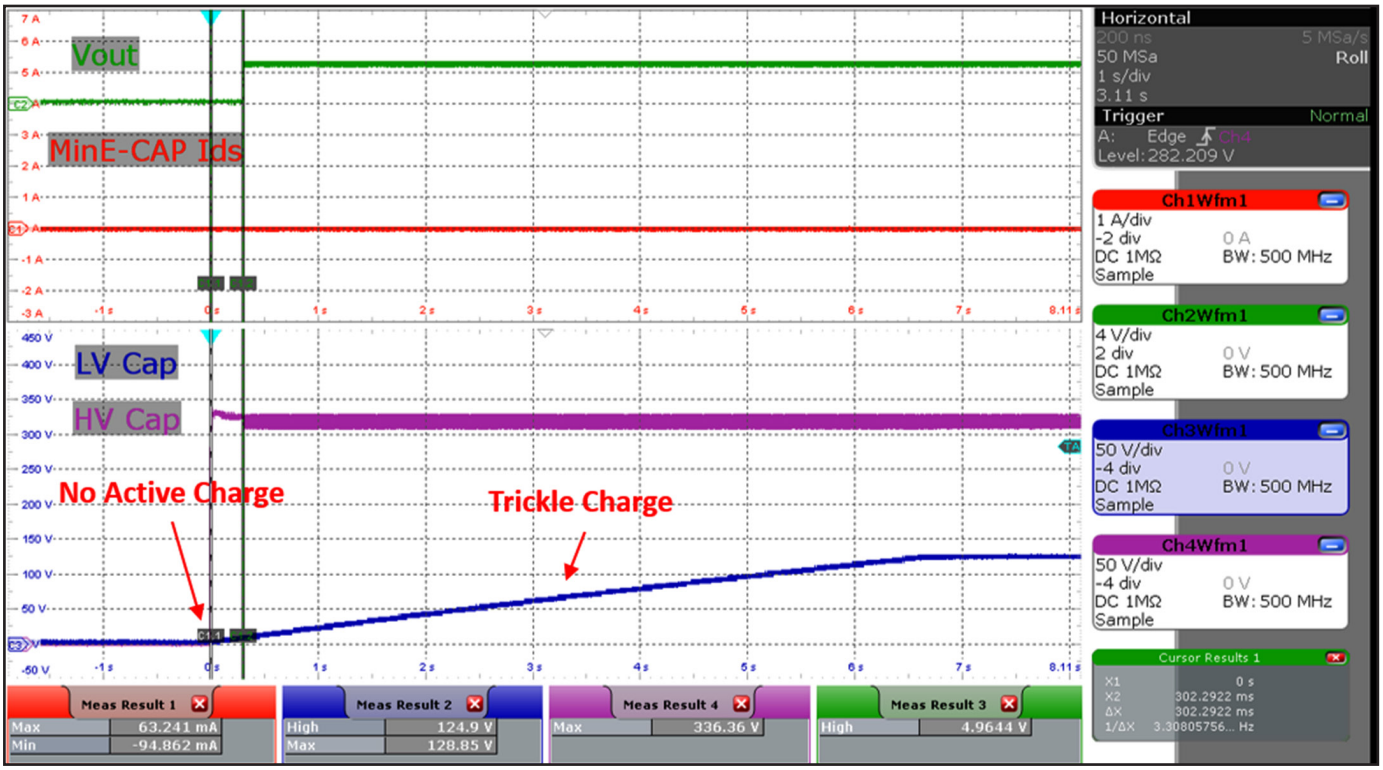
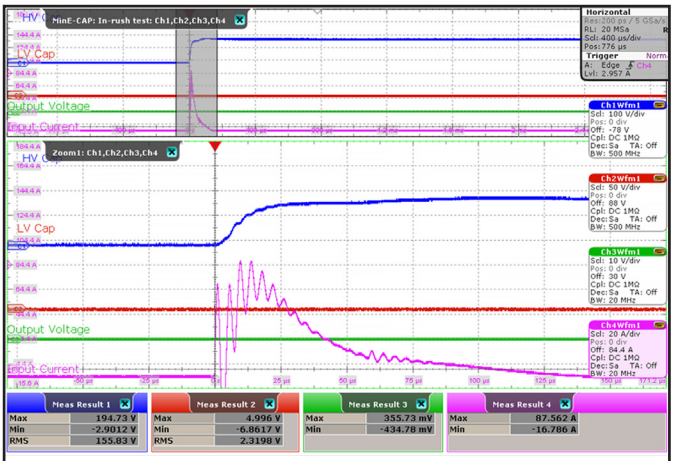



Figure 13. MinE-CAP IC Start-up Waveforms ($V_{IN}$ = 230 VAC, Load = 5 V, 3 A).

The process described above significantly reduces the $I^2t$ stresses experienced by the input components during start-up. This offers the designer the option to use smaller fuses with lower $I^2t$ ratings while also removing the need for an inrush-limiting NTC thermistor. Figures 14 to 17 shows the inrush current for a design with a total input capacitance of 100 µF with and without a MinE-CAP.




Vin = 132 VAC, Vout = 20V, Io = 3.25 A (Full Load)

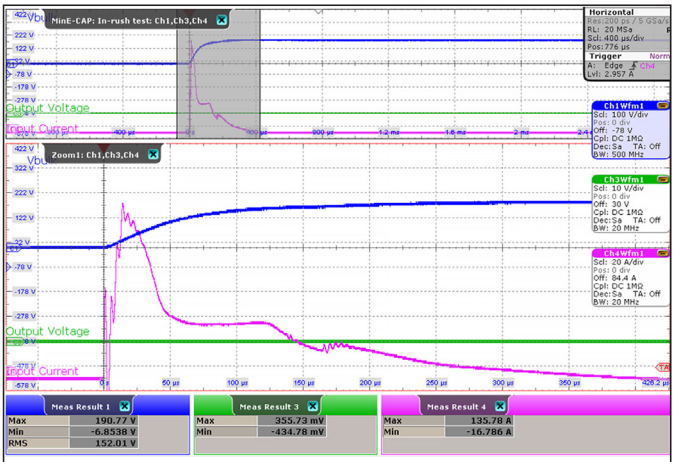
Time Scale: 400 µs/div.
CH1: HV Cap – 100 V/div.
CH3: Vout – 10 V/div.

Zoom Time Scale: 25 µs/div.
CH2: LV Cap – 50 V/div.
CH4: Input Current – 20 A/div.

Peak Input Current ($I_{peak}$) = 87.562 A, $t_{pulse}$ = 125 µs

$$I^2t = \frac{1}{2} {I_{peak}}^2 t_{pulse} = 0.958\ A^2s$$

Figure 14. Inrush Current for $V_{IN}$ = 132 VAC and 100 µF Input Capacitor with MinE-CAP IC Circuit.




Vin = 132 VAC, Vout = 20V, Io = 3.25 A (Full Load) No MinE-CAP

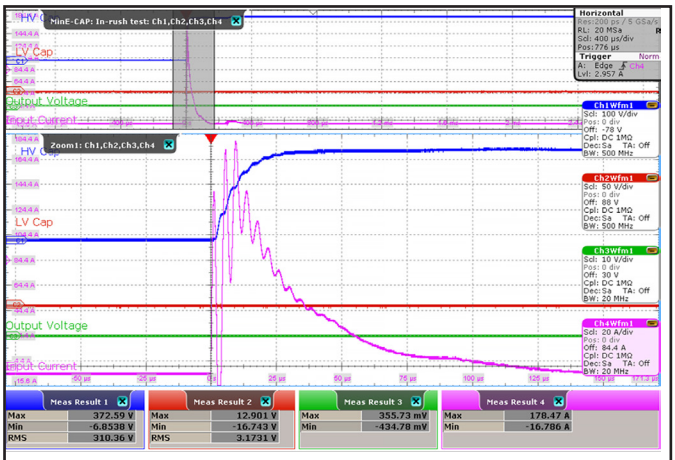
Time Scale: 400 µs/div.
CH1: HV Cap – 100 V/div.
CH4: Input Current – 20 A/div.

Zoom Time Scale: 25 µs/div.
CH3: Vout – 10 V/div.

Peak Input Current ($I_{peak}$) = 135.78 A, $t_{pulse}$ = 350 µs

$$I^2t = \frac{1}{2} {I_{peak}}^2 t_{pulse} = 6.4527\ A^2s$$

Figure 15. Inrush Current for $V_{IN}$ = 132 VAC and 100 µF Input Capacitor without MinE-CAP IC Circuit.




Vin = 265 VAC, Vout = 20V, Io = 3.25 A (Full Load)

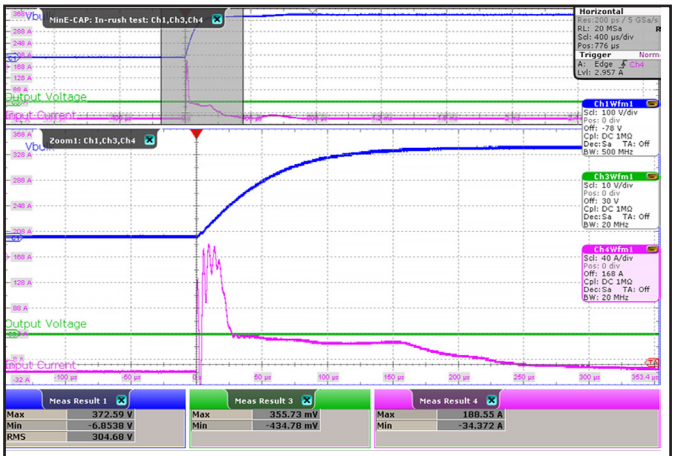
Time Scale: 400 µs/div.
CH1: HV Cap – 100 V/div.
CH3: Vout – 10 V/div.

Zoom Time Scale: 25 µs/div.
CH2: LV Cap – 50 V/div.
CH4: Input Current – 20 A/div.

Peak Input Current ($I_{peak}$) = 178.47 A, $t_{pulse}$ = 125 µs

$$I^2t = \frac{1}{2} {I_{peak}}^2 t_{pulse} = 3.9814\ A^2s$$

Figure 16. Inrush Current for $V_{IN}$ = 265 VAC and 100 µF Input Capacitor with MinE-CAP IC Circuit.




Vin = 265 VAC, Vout = 20V, Io = 3.25 A (Full Load) No MinE-CAP

Time Scale: 400 µs/div.
CH1: HV Cap – 100 V/div.
CH4: Input Current – 20 A/div.

Zoom Time Scale: 25 µs/div.
CH3: Vout – 10 V/div.

Peak Input Current ($I_{peak}$) = 135.78 A, $t_{pulse}$ = 250 µs

$$I^2t = \frac{1}{2} {I_{peak}}^2 t_{pulse} = 8.8877\ A^2s$$

Figure 17. Inrush Current for $V_{IN}$ = 265 VAC and 100 µF Input Capacitor without MinE-CAP IC Circuit.

## Fast AC Reset

The InnoSwitch3 family of ICs feature a primary sensed OV protection feature that can be used to latch-off/AR the power supply. This protection feature is still operational even when a MinE-CAP IC is used. Once the power supply is in latch-off/AR, it can be reset if the VTOP pin current is reduced to zero. Even after the input supply is turned off, it can take a considerable amount of time to reset the InnoSwitch3 IC, since the energy stored in the DC bus will continue to provide a bias supply to the controller. Fast AC reset can be provided using the circuit configuration shown in Figure 19. The voltage across the 100 nF 400 V capacitor reduces rapidly after the input supply is disconnected pulling the $V_{TOP}$ to zero.

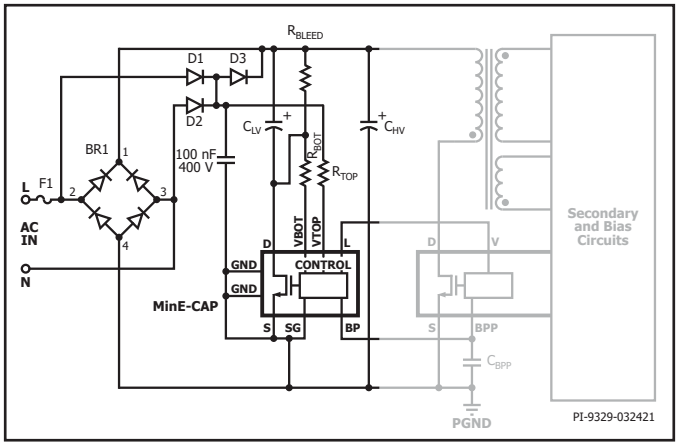



Figure 18. Circuit Schematic to Implement Fast AC Reset when using a MinE-CAP IC Circuit.

## PCB Layout Guidelines

The following layout considerations are specifically for the MinE-CAP circuit components. For placement and layout of controller-specific and power components, check the corresponding power controller data sheet.

1. The MinE-CAP sense pins (VBOT and VTOP) and InnoSwitch3 IC's V pin use current in the µA range to measure line and capacitor voltages. Avoid routing lines with high dV/dt or dI/dt signals near these pins. This must also be observed for the L pin. $R_{TOP}$ and $R_{BOT}$ must be placed as close as possible to VTOP and VBOT pins, respectively.

2. Signal lines going to the pins stated above must also be routed away from high dV/dt or dI/dt nodes or tracks to avoid capacitive or inductive noise coupling.

3. All resistors ($R_{TOP}$ and $R_{BOT}$) associated with the MinE-CAP IC except for the bleed resistor in parallel with $C_{LV}$ must be placed near the MinE-CAP. If this is not possible, said resistors can be placed farther away but routes going to the MinE-CAP IC must not be routed near noisy nodes or must be shielded.

4. Place the MinE-CAP IC as close as possible to the InnoSwitch3 (if used) to minimize the trace from the L pin to the V pin of the InnoSwitch3 IC. Placing the MinE-CAP IC next to the InnoSwitch3 also allows the use of a single bypass capacitor for both devices.

5. Tie the GND pins to a copper plane for heat dissipation. If a large copper plane is not possible, thermal vias can also be used for boards with 2 or more copper layers. The MinE-CAP IC and InnoSwitch3 IC can share the same GND plane.

6. Place both input bulk capacitors ($C_{LV}$ and $C_{HV}$) in such a way to minimize the primary switching loops, loops 1 and 2 as shown in Figure 19. Prioritize placing the high-voltage capacitor closer to the transformer and InnoSwitch3 since this capacitor is always part of the high-frequency switching loop.

Figures 24 and 25 show a sample MinE-CAP layout following the recommendations stated above.

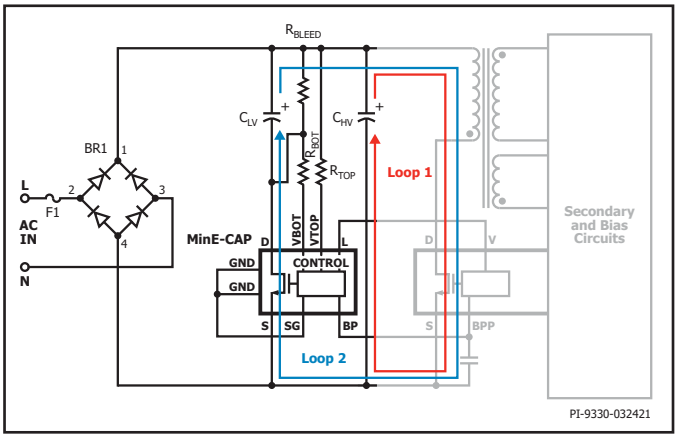



Figure 19. Basic MinE-CAP Schematic Showing Primary Switching Loops.

## EMI Considerations

When the MinE-CAP disconnects the low voltage capacitor, $C_{LV}$, from the circuit during high-line operation, the conducted EMI may increase. For designs that utilize the EMI filter topology shown in Figure 20, removal of the low-voltage capacitor (C3) increases the total input bulk capacitor ESR. This translates to an increase in differential-mode noise at high-line.

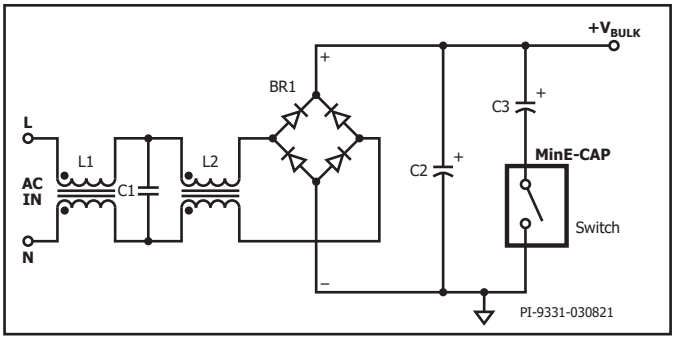



Figure 20. T-Filter Topology.

When using the T-Filter topology with the MinE-CAP IC circuit, consider the following:

1. If the leakage inductance of the common-mode choke is inadequate to filter differential mode noise, a separate DM-choke can be placed in series with the CMC.

2. Increase the value of C1 if size constraints permit.

3. When using a DM choke, take note of the peak line current at both high-line and low-line operation. Use the peak line current to check for core saturation and power losses.

4. Use a high-voltage capacitor with the lowest ESR possible.

An alternative approach is to use a Pi-filter to suppress differential-mode noise. The schematic for this alternative technique is shown in Figure 21. An advantage of this topology is that the required inductance value of the common-mode chokes may be significantly less than that of the T-Filter since a large leakage inductance is no longer needed to suppress differential mode noise. A disadvantage is that the HV Capacitor must be split into two devices whose overall value is equal to or greater than the calculated capacitance for high-line operation.

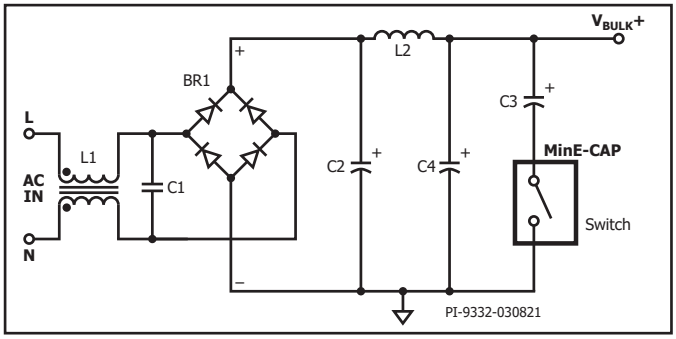



Figure 21. DC Side Pi-Filter Topology.

When the Pi-Filter topology is used, consider the following:

1. The values of the chosen capacitors need not be equal and can be calculated to meet the desired response of the pi-filter.

2. The value of L2 must be chosen to avoid excessive impedance at the maximum switching frequency of the converter. Design L2 to ensure it will not saturate at maximum output load at low-line conditions.

3. In general, for stability the output impedance of the filter must be less than 10% of the impedance of the converter at full load.

4. The low-voltage capacitor (C3) should be placed after the inductor, L2. This ensures that current from the low-voltage capacitor is not hindered by the impedance of L2 when operating at low-line. This will also ensure that noise due to the switching of the MinE-CAP IC attenuated.

## Surge Immunity Considerations

The MinE-CAP IC has a built-in surge detector to protect the device and the LV capacitor during surge events.

1. During normal operation, MinE-CAP IC is on – and it detects a surge event by monitoring the voltage across the $R_{DS(ON)}$ of its internal power switch. A surge fault is triggered if the voltage corresponds to a drain current greater than or equal to the Surge Current Detection Current, $I_{SURGE}$.

2. Start-up, Active Charge – The MinE-CAP IC issues a fault when the measured $V_{TOP}$ exceeds $V_{HL(STARTUP)}$ during start-up. Line swell during start-up will also be treated as a surge event.

During surge events, the MinE-CAP will turn off the MinE-CAP IC's power switch for 100 μs. The MinE-CAP IC returns to normal operation after the 100 μs timer expires.

The MinE-CAP IC cannot detect surge events if the internal high-voltage switch is off. Therefore, the following must be considered to ensure surge immunity when using the MinE-CAP in any design.

1. For designs with very low HV capacitor values, a surge event may cause the bulk voltage to rise to levels high enough to trigger OVP. If the magnitude of this voltage rise is excessive, or if auto-restart is not desired during surge events, either add a metal-oxide varistor (MOV) to the design or increase the HV capacitor capacitance if size constraints allow.

2. The voltage rise due to surge events also varies based on the EMI filter used. It is possible to prevent OVP by adjusting the values of the EMI filter components.

## PCB Layout Examples

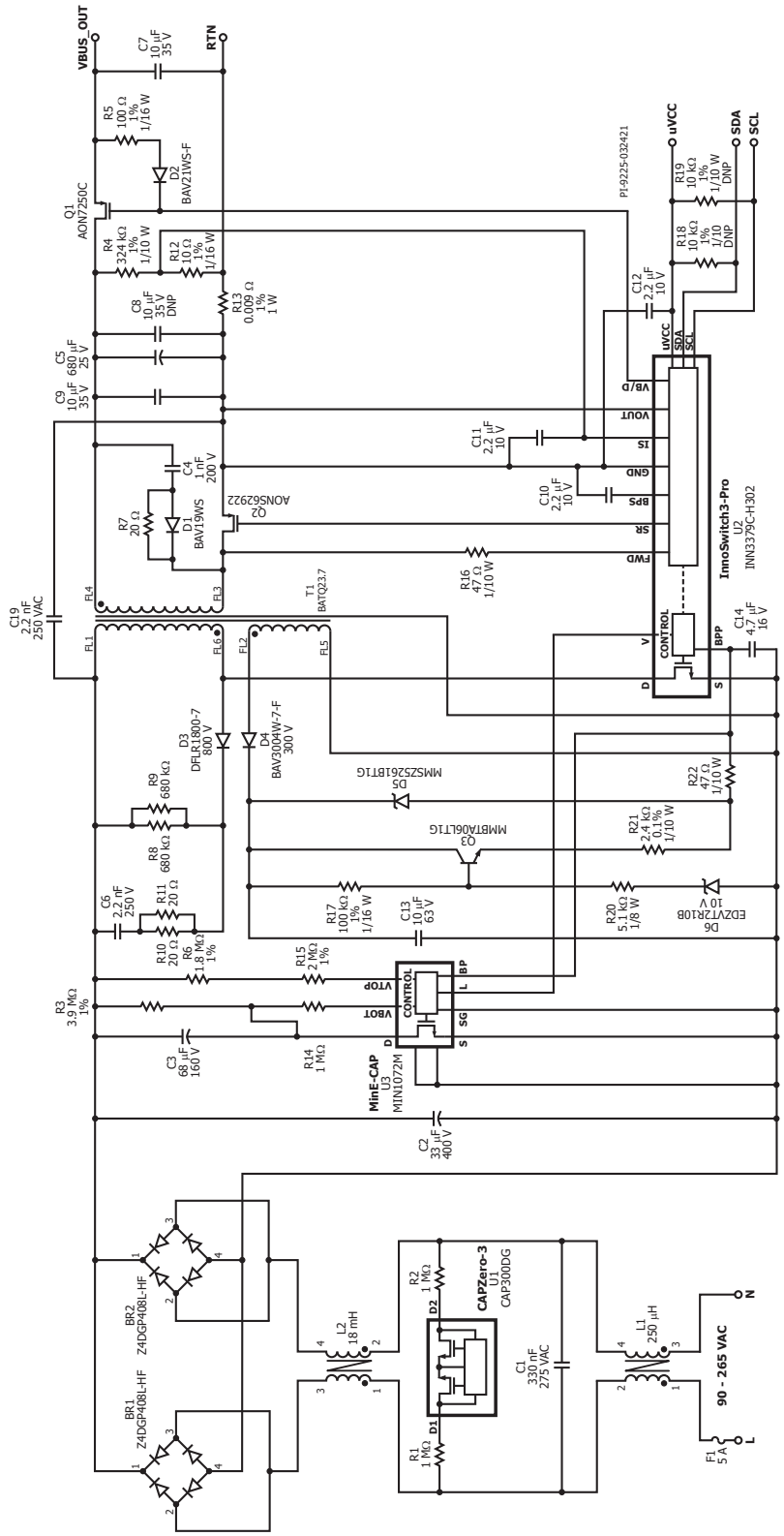



Figure 22. DER-822 Power Section Schematic. 60 W USB-C PD using INN3379C-H302, MinE-CAP, and AC-side T-filter for EMI (PD Controller Section not included; see DER-822 documentation).

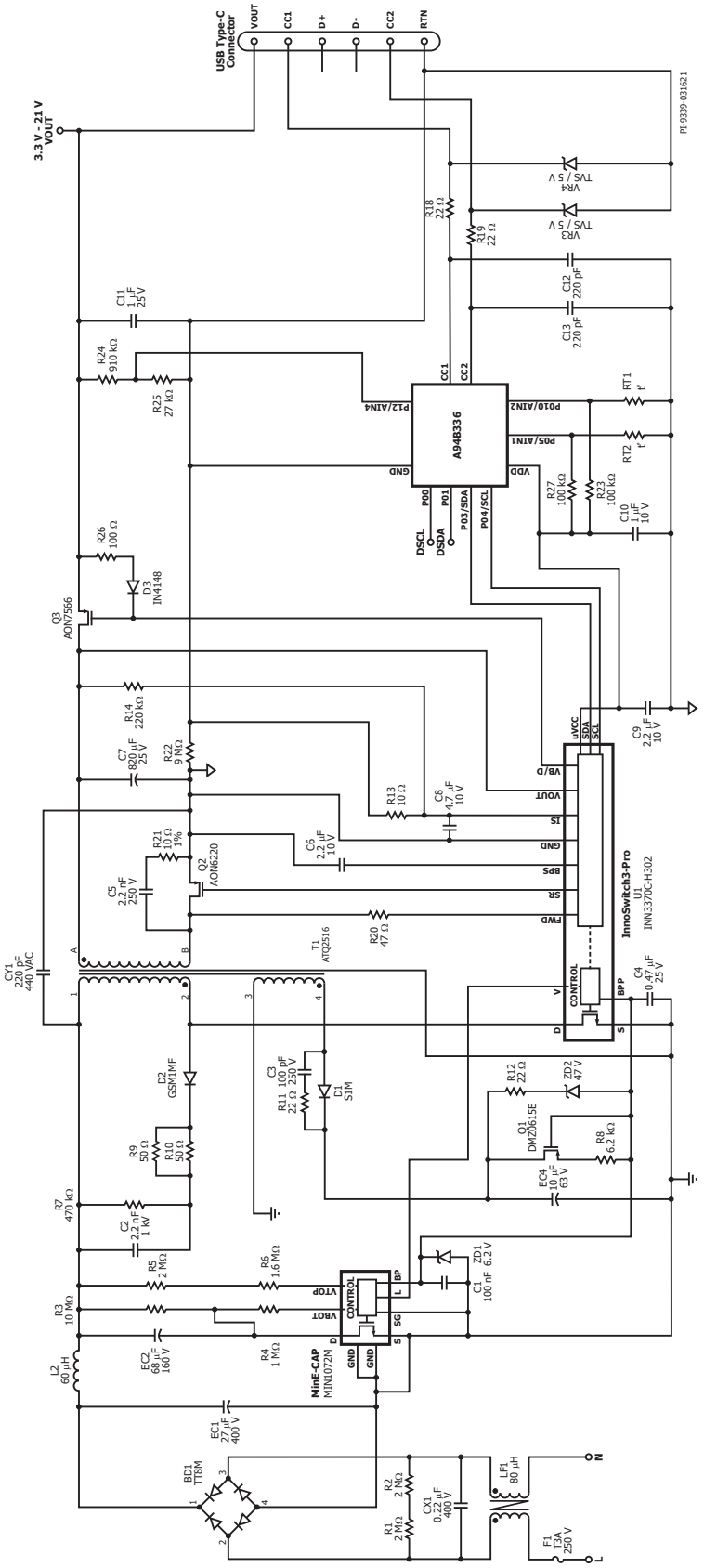



Figure 23. 65 W USB-C PD PPS using INN3370C-H302 with MinE-CAP and Pi EMI Filter.

## PCB Layout Examples

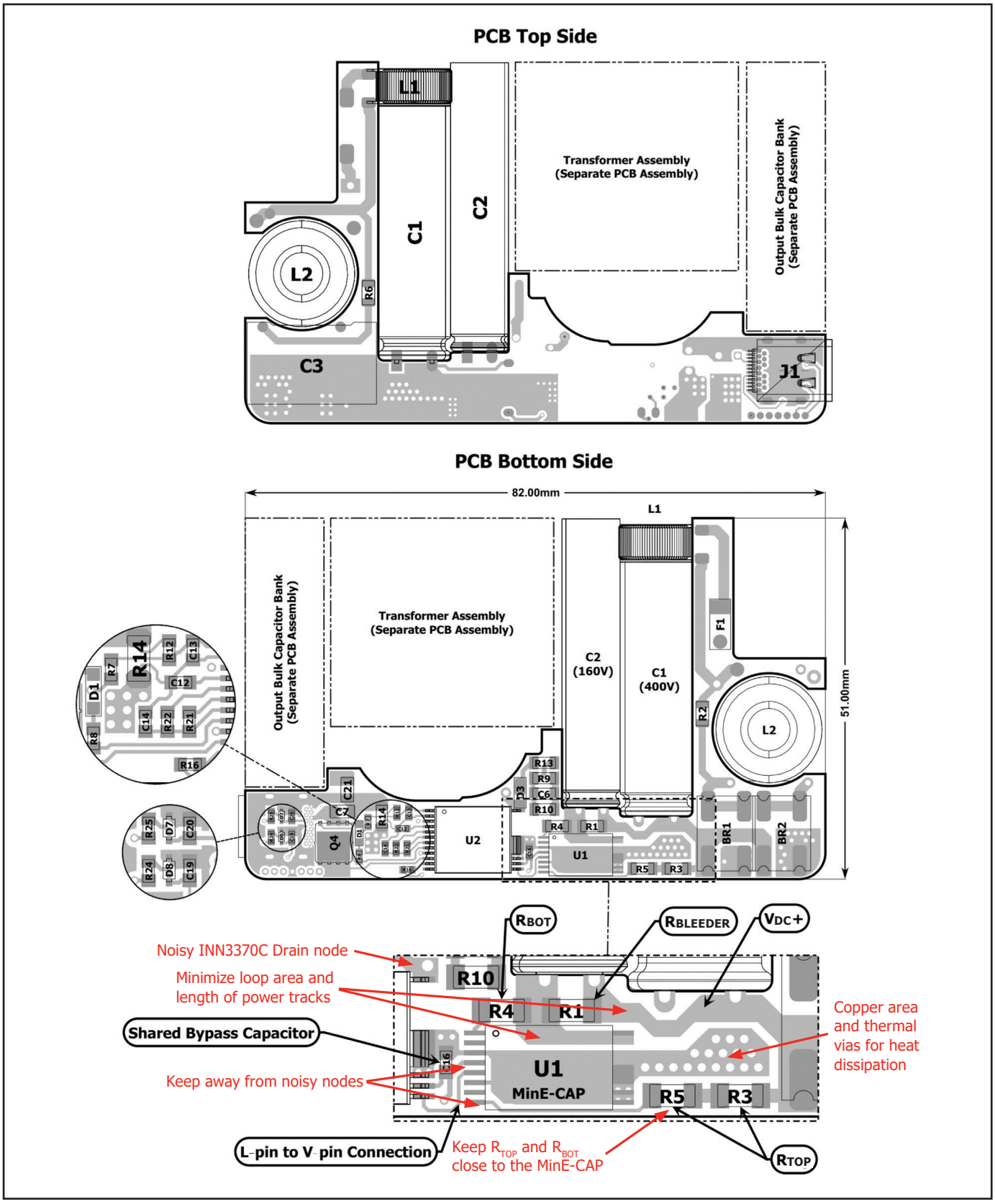



Figure 24. MinE-CAP IC Circuit Example Layout from DER-626 (65 W USB-C PD using INN3370C-H302).

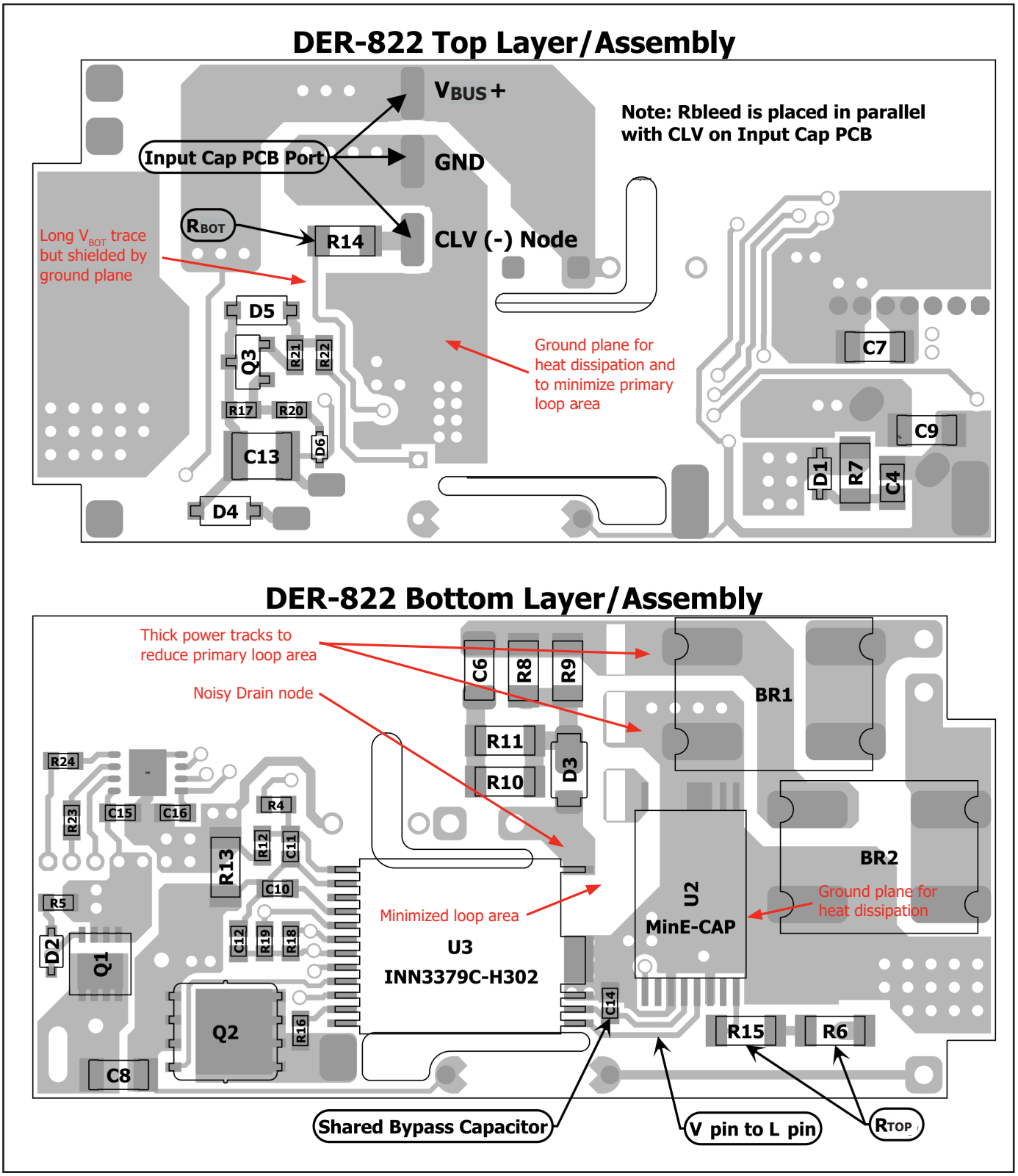



Figure 25. MinE-CAP IC Circuit Example Layout from DER-822 (60 W USB-C PD using INN3379C-H302).

## Appendix A

### Input Capacitor Derivation

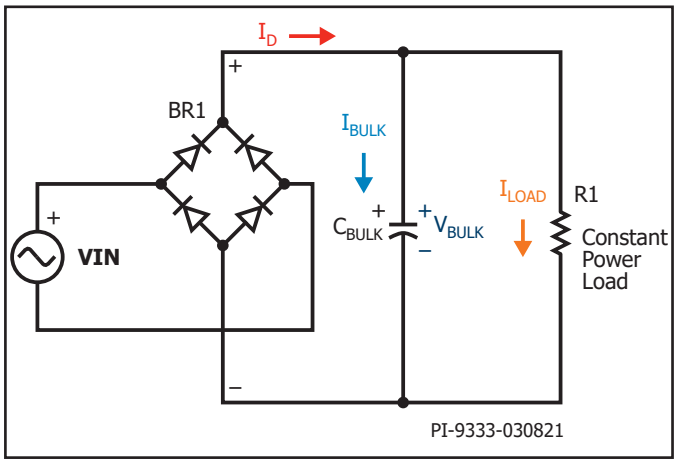



Figure 26. Basic Rectifier Circuit with Constant Power Load.

The circuit in Figure 26 shows the schematic of a basic full wave rectifier with constant power load. To solve for the input capacitor, we need the following parameters:

- $V_{MIN}$ = Minimum voltage required by the constant power load
- $P_{OUT}$ = maximum output power of the converter
- Efficiency ($\eta$) = Assumed converter efficiency

For this analysis, the high frequency input current ripple due to the flyback converter is ignored.

To solve for the capacitor, we begin with the capacitor current,

$$I_{BULK}(t) = C_{BULK}\frac{dV_{BULK}(t)}{dt}$$

During the time the diode bridge is conducting, $t_c$, $V_{BULK}$ is equal to the rectified input voltage, $V_{RECT}$

$$V_{REC}(t) = V_{IN(PK)}\sin(\omega t)$$

Where

$$\omega = 2\pi f_{LINE}, V_{IN(PK)} = \sqrt{2}V_{AC(RMS)}$$

$$f_{LINE} = \text{AC line frequency}, P_{IN} = \frac{P_{OUT}}{\eta}$$

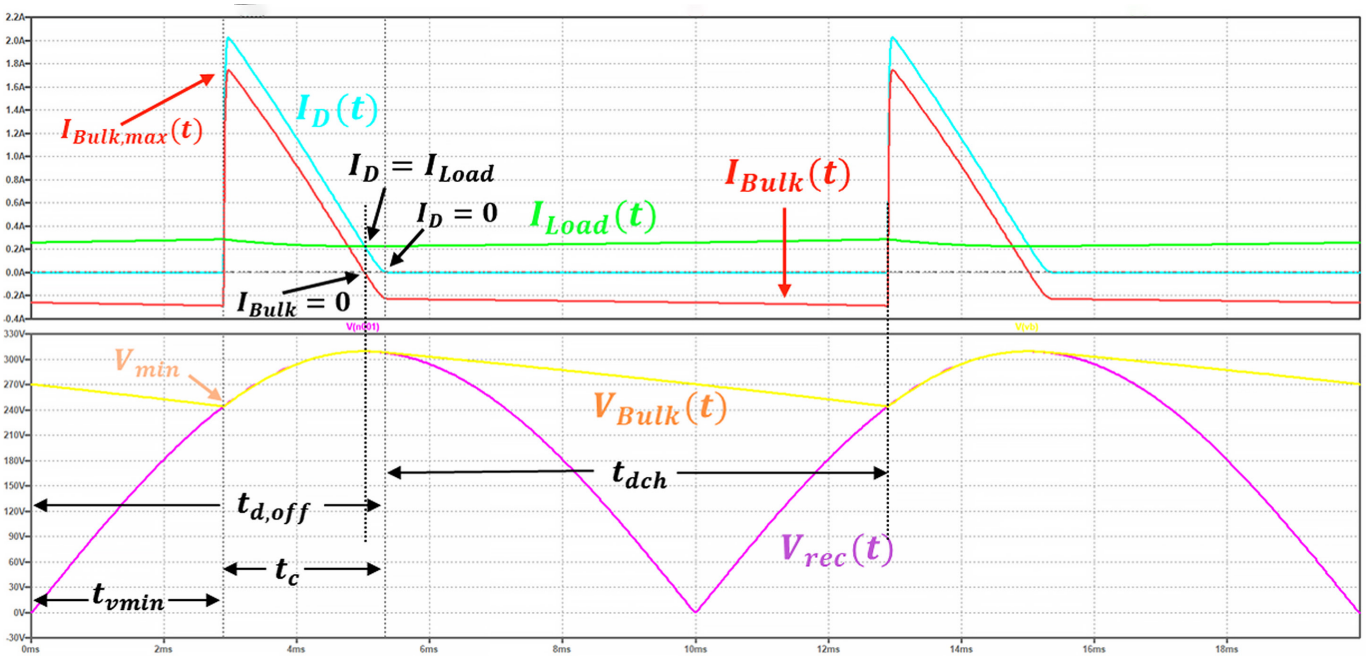



Figure 27. Current (Top) and Voltage (Bottom) Waveforms for the Circuit in Figure 26.

The bulk capacitor current during charging is

$$I_{BULK}(t) = C_{BULK}\frac{d(V_{IN(PK)}\sin(\omega t))}{dt}$$

$$I_{BULK}(t) = C_{BULK}\omega V_{IN(PK)}\cos(\omega t)$$

We can estimate the peak bulk capacitor current by evaluating the above equation at the time when the bridge diodes turn on.

$$I_{BULK(PK)} = C_{BULK}\omega V_{IN(PK)}\cos(\omega t_{V(MIN)})$$

Solving for $t_{V(MIN)}$,

$$V_{MIN} = V_{IN(PK)}\sin(\omega t_{VMIN})$$

$$t_{V(MIN)} = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{MIN}}{V_{IN(PK)}}\right)$$

When the bridge diodes are on, power comes from the AC line. We need to determine the time the diodes turn off to be able to compute $C_{BULK}$.

The bridge diodes turn-off when the load current is supplied solely by the capacitor.

$$-I_{BULK}(t) = I_{LOAD}(t)$$

The instantaneous load current is

$$I_{LOAD}(t) = \frac{P_{IN}}{V_{BULK}(t)}$$

$$\frac{P_{IN}}{V_{IN(PK)}\sin(\omega t)} = -C_{BULK}\omega V_{IN(PK)}\cos(\omega t)$$

Simplifying,

$$\frac{-P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}} = \frac{1}{2}\sin(2\omega t)$$

Solving for $t_{D(OFF)}$,

$$t_{D(OFF)} = \frac{1}{2\omega}\sin^{-1}\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)$$

The inverse sine function has a range $[-\pi,\pi]$ so the output of the inverse sine must be corrected by subtracting it from $\pi$

$$t_{D(OFF)} = \frac{1}{2\omega}\left(\pi - \sin^{-1}\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)\right)$$

Total bridge conduction time is

$$t_{D(OFF)} - T_{VMIN} = t_{D(ON)} = \frac{1}{2\omega}\left(\pi - \sin^{-1}\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)\right) - \frac{1}{\omega}\sin^{-1}\left(\frac{V_{MIN}}{V_{IN(PK)}}\right)$$

When the bridge turns off, the capacitor must be able to supply the energy needed by the load. The discharge time of the capacitor is

$$t_{DCH} = \text{period} - t_{D(ON)} = \frac{1}{2f_{LINE}} - t_{D(ON)}$$

Plugging in all relevant expressions to the previous equation yields

$$P_{IN}\left(\frac{1}{2f_{LINE}} - \left(\frac{1}{2\omega}\left(\pi - \sin^{-1}\left(\frac{-2P_{OUT}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)\right) - \frac{1}{\omega}\sin^{-1}\left(\frac{V_{MIN}}{V}\right)\right)\right)$$
$$= \frac{1}{2}C_{BULK}\left(\left(V_{IN(PC)}\cos\left(\frac{1}{2}\sin^{-1}\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)\right)\right)^{2} - V_{MIN}^{2}\right)$$

Further simplifying, we get

$$\frac{P_{IN}}{\omega}\left(\pi - \sin^{-1}\left(\frac{2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right) + 2\sin^{-1}\left(\frac{V_{MIN}}{V_{IN(PK)}}\right)\right) =$$
$$C_{BULK}\left(V_{IN(PK)}^{2}\left(\frac{1+\sqrt{1-\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)^{2}}}{2}\right) - V_{MIN}^{2}\right) = 0$$

which has no closed-form solution. However, $C_{BULK}$ can be solved by searching for the roots of the following equation using numerical methods or trial-and-error:

$$\frac{P_{IN}}{\omega}\left(\pi - \sin^{-1}\left(\frac{2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right) + 2\sin^{-1}\left(\frac{V_{MIN}}{V_{IN(PK)}}\right)\right) -$$
$$C_{BULK}\left(V_{IN(PK)}^{2}\left(\frac{1+\sqrt{1-\left(\frac{-2P_{IN}}{\omega C_{BULK}V_{IN(PK)}^{2}}\right)^{2}}}{2}\right) - V_{MIN}^{2}\right) = 0$$

Note that all variables above except $C_{BULK}$ are user defined parameters.

**Example**

$P_{OUT}$ = 65 W, $\eta$ = 0.92, $V_{IN}$ = 230 VAC 60 Hz, $V_{MIN}$ = 220 VDC
Solve for $C_{BULK}$ using Newton-Raphson Method.

$$\text{Let } A = \frac{P_{IN}}{\omega} = 187.42\text{ m; } B = \frac{2P_{IN}}{\omega V_{IN(PK)}^{2}} = 3.5427\mu$$
$$C = 2\sin^{-1}\left(\frac{V_{MIN}}{V_{IN(PK)}}\right) = 1.4856 \text{ and } x = C_{BULK}$$

NR Method requires the first derivative of f(x),

$$f(X) = \left((A\pi + AC) - A\sin^{-1}\left(B\frac{1}{X}\right)\right) - 4500x - \frac{V_{IN(PC)}^{2}}{2}\sqrt{X^{2}-B^{2}}$$
$$f'^{(X)} = \left(\frac{AB}{\sqrt{X^{4}-B^{2}X^{2}}}\right) - \frac{X}{2\sqrt{X^{2}-B^{2}}} - 4500$$

With an initial value of $C_{BULK}$ = 6 µF and iterating, we get

$$C_{BULK} = 15\ \mu F$$

The computed capacitor is verified thru simulation as can be seen in Figure 28 where the simulated $V_{MIN}$ is near the desired value of 220 VDC.

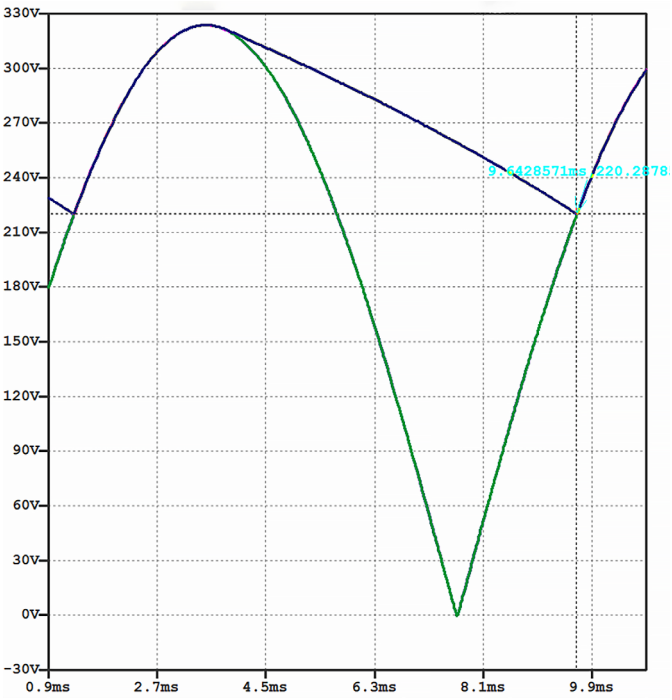



Figure 28. Circuit Simulation of Figure 9 using $P_O$ = 65 W, $\eta$ = 0.92, $V_{IN}$ = 230 VAC and $C_{BULK}$ = 15 µF; Rectified Voltage (Green), Capacitor Voltage (Blue).

Once the capacitor value has been chosen, we can calculate the current passing thru the input stage of the converter. The instantaneous capacitor current when the bridge is ON is,

$$I_{BULK}(t) = C_{BULK}\omega V_{IN(PK)}\cos(\omega t), \text{ when bridge in ON}$$

$$I_{BULK}(t) = \frac{-P_{IN}}{\sqrt{V_{BULK(PK)}^2 - \frac{2P_{IN}t}{C_{BULK}}}}, \text{ when bridge is OFF}$$

And the capacitor RMS current can be found as

$$I_{BULK(RMS)} = \sqrt{2f_{LINE}\left(\int_{t_{VMIN}}^{t_{DOFF}}(C_{BULK}\omega V_{IN(PK)}\cos(\omega t))^2 dt + \int_0^{DCH}\left(\frac{P_{IN}}{\sqrt{V_{BULK(PK)}^2 - \frac{2P_{IN}t}{C_{BULK}}}}\right)^2 dt\right)}$$

$$I_{BULK(RMS)} = \sqrt{\left(\left(\frac{C_{BULK}\omega V_{IN(PK)}^2}{2}\left(t + \frac{\sin(2\omega t)}{2\omega}\right)\right)\Big|_{t_{VMIN}}^{t_{DOFF}} - \left(\frac{P_{IN}C_{BULK}}{2}\ln\left|V_{BULK(PK)}^2 - \frac{2P_{IN}t}{C_{BULK}}\right|\right)\Big|_0^{t_{DHC}}\right)}$$

We can also compute for the RMS current going through the AC input. It is composed of the load current and the capacitor current when the diodes are conducting

$$I_{LINE}(t) = \frac{P_{IN}}{V_{IN(PK)}\sin(\omega t)} + C_{BULK}\omega V_{IN(PK)}\cos(\omega t),$$
$$t_{V(MIN)} \le t \le t_{DOFF} \text{ (zero otherwise)}$$

Peak line current occurs at $t_{VMIN}$. This is also equal to the peak current through each bridge diode

$$I_{LINE(PK)} = I_{DIODE(PK)} = \frac{P_{IN}}{V_{IN(PK)}\sin(\omega t_{VMIN})} + C_{BULK}\omega V_{IN(PK)}\cos(\omega t_{V(MIN)})$$

RMS current of the line is given by

$$I_{LINE(RMS)} = \sqrt{\left[\frac{A^2}{\pi}\cot(\omega t) + \frac{2AB}{\pi}\ln|\sin(\omega t)| + f_{LINE}t + \frac{\sin(2\omega t)}{4\pi}\right]\Big|_{t_{VMIN}}^{t_{DOFF}}}$$

where

$$A = \frac{P_{IN}}{V_{IN(PK)}} \text{ and } B = C_{BULK}\omega V_{IN(PK)}$$

Finally, the average and RMS current going through each diode in the bridge can be found to be

$$I_{DIODE(AVE)} = \frac{1}{2\pi}\left[-A\ln|\csc(\omega t) + \cot(\omega t)| + B\sin(\omega t)\right]\Big|_{t_{V(MIN)}}^{t_{D(OFF)}}$$

$$I_{DIODE(RMS)} = \frac{I_{LINE(RMS)}}{\sqrt{2}}$$

where

$$A = \frac{P_{IN}}{V_{IN(PK)}} \text{ and } B = C_{BULK}\omega V_{IN(PK)}$$

| Revision | Notes | Date |
|---|---|---|
| A | Initial release. | 07/21 |

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